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**EE 4540L/6540L/CEG4322L/CEG6322L**

**FALL 2023**

**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Alex Yeoh**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Alex Yeoh Date: 12 September 2023**

**Report due date: 15 September 2023**

1. **OBJECTIVE**

To learn how to navigate virtuoso and to build a 4-bit prime number detector.

1. **PROCEDURE**

Design the circuit with a truth table, simplify the resulting equation with a k-map, draw a schematic with the simplified circuit, build the circuit with 2-input logic gates with given parameters, and simulate the circuit with given parameters to generate graphs of the input and output signals.

1. **RESULT**

A close-up of a graph

Description automatically generated

This is a truth table for a 4-bit prime number detector that does not detect 1 as a prime number.

A drawing of a grid with numbers and letters

Description automatically generated

This is a k-map used to simplify the truth table above into a sum of products form.

A diagram of a circuit

Description automatically generated

This is a logic diagram built with the k-map simplified equation from above.

A computer screen shot of a computer program

Description automatically generated

This is the logic diagram built following the logic diagram above with only 2-input logic gates in virtuoso.

A graph of a graph

Description automatically generated with medium confidence

This is the signal graph of each of the inputs and the output of the logic diagram built in virtuoso above.

1. **CONCLUSION**

The output signal graph is as expected and satisfies the requirement of being a 4-bit prime number detector. I am currently unsure of a way to improve the design to get better results. I have learned how to better navigate virtuoso from this lab.