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**EE 4540L/6540L/CEG4322L/CEG6322L**

**FALL 2023**

**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Alex Yeoh**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Alex Yeoh Date: September 24, 2023**

**Report due date: September 27, 2023**

1. **OBJECTIVE**

To learn how to build layouts in virtuoso and to build a 3-input NAND layout.

1. **PROCEDURE**

Draw a transistor schematic, choose an Euler path for the designed schematic, draw a stick diagram with the Euler path, and draw the layout in virtuoso based on the stick diagram while using design rule check to ensure there are no errors.

1. **RESULT**

A drawing of a diagram

Description automatically generated

This is a transistor schematic for an inverter.

A group of handwritten text

Description automatically generated

This is the Euler path for the inverter.

A diagram of a circuit

Description automatically generated

This is the stick diagram for the inverter based on the Euler path above.

A colorful squares and dots

Description automatically generated with medium confidence

This is the layout for the inverter based on the stick diagram above.

A screenshot of a computer

Description automatically generated

This is the DRC output for the inverter layout above.

A drawing of a circuit

Description automatically generated

This is a transistor schematic for a NAND3.

A group of black circles and circles with letters

Description automatically generated

This is the Euler path for the NAND3.

A diagram of a circuit

Description automatically generated

This is the stick diagram for the NAND3 based on the Euler path above.

A computer screen shot of a grid

Description automatically generated

This is the layout for the NAND3 based on the stick diagram above.

A screenshot of a computer

Description automatically generated

This is the DRC output for the NAND3 layout above.

1. **CONCLUSION**

Both my inverter and NAND3 layouts satisfy the requirements of having no errors after the DRC. The NAND3 layout could have potentially been a little smaller, but I’m not sure. I learned how to build layouts in virtuoso.