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**EE 4540L/6540L/CEG4322L/CEG6322L**

**FALL 2023**

**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Alex Yeoh**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Alex Yeoh Date: 9th October 2023**

**Report due date: 11th October 2023**

1. **OBJECTIVE**

To learn how to simulate layouts in virtuoso and determine average propagation delay.

1. **PROCEDURE**

Design and create a layout, put pins and layouts for all the inputs and outputs, export the layout, set appropriate values for the inputs, mark the mid-points for rising and falling time, and calculate the average propagation delay for the layout.

1. **RESULT**

A graph with lines and text

Description automatically generated with medium confidence

Result of the simulated inverter, with an average propagation delay of 24.72905ps.

A diagram of a diagram

Description automatically generated

Result of the simulated NAND3, with an average propagation delay of 69ps.

A drawing of a diagram

Description automatically generated

Transistor schematic for NOR3.

A close-up of a whiteboard

Description automatically generated

Euler path for the transistor above.

A diagram of electrical wiring

Description automatically generated

Stick diagram for the euler path above.

A screen shot of a computer screen

Description automatically generated

Layout for the stick diagram above.

A screen shot of a graph

Description automatically generated

Simulated result for the layout above with a propagation delay of 96.736ps.

A drawing of a circuit

Description automatically generated

Transistor schematic for NAND2.

A white board with black text

Description automatically generated with medium confidence

Euler path for the transistor schematic above.

A diagram of a circuit

Description automatically generated

Stick diagram for the euler path above.

A screen shot of a computer screen

Description automatically generated

Layout for the stick diagram above.

A screen shot of a graph

Description automatically generated

Simulated result for the layout above with a propagation delay of 56.83935ps.

A diagram of a circuit

Description automatically generated

Transistor schematic for XOR2.

A whiteboard with black text

Description automatically generated

Euler path for the transistor schematic above.

A diagram of a wiring diagram

Description automatically generated

Stick diagram for the euler path above.

A diagram of a computer

Description automatically generated

Layout for the stick diagram above, with modification to fit height requirements.

A screenshot of a computer screen

Description automatically generated

Simulated result for the layout above with an average propagation delay of 125.03ps.

1. **CONCLUSION**

My results satisfy the requirements, as all layouts have the correct outputs with the given inputs. It is possible to slightly lower propagation delay by making the layouts slightly smaller. I have learned how to simulate and analyze propagation delay in Virtuoso.