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**EE 4540L/6540L/CEG4322L/CEG6322L**

**FALL 2023**

**TA: Kanchan Vissamsetty**

**Lab section: 01**

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**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Alex Yeoh Date: 23rd October 2023**

**Report due date: 25th October 2023**

1. **OBJECTIVE**

To learn how to build more complex layouts in virtuoso with premade circuits.

1. **PROCEDURE**

Design and create layouts for a 1-bit adder’s Cout and Sum with gates such as XOR2, NAND2, and NAND3. Use the Cout and Sum layouts to build a 1-bit adder, and use the 1-bit adder to build a 2-bit adder.

1. **RESULT**

A table with numbers and symbols

Description automatically generated

The truth table for a 1-bit adder that shows the output values of Cout and Sum.

A drawing of a plane

Description automatically generated

The gate diagram for Sum.

A diagram of a circuit

Description automatically generated with medium confidence

The gate diagram for Cout.

A close-up of a circuit board

Description automatically generated

A transistor layout for a 1-bit adder where A, B, C, SUM, and COUT are A0, B0, Cin, Sum, and Cout respectively.

A diagram of a graph

Description automatically generated with medium confidence

Result of the 1-bit adder, with an average Cout propagation delay of 130.31ps and an average Sum propagation delay of 271.835ps.

A computer screen with red and blue lines

Description automatically generated

A transistor layout for a 2-bit adder where A, B, C, D, E, SUM, and COUT are A0, B0, A1, B1, Cin, Sum, and Cout respectively.

A screen shot of a computer screen

Description automatically generated

Result of the 2-bit adder, with an average Cout propagation delay of 301.23285ps, an average Sum propagation delay of 289.0036ps, and an average Sum1 propagation delay of 338.0911ps.

A table of numbers with a number in the center

Description automatically generated with medium confidence

The truth table for a 2-bit adder that corresponds with the outputs shown in the result for a 2-bit adder above.

1. **CONCLUSION**

My results satisfy the requirements, as all layouts have the correct outputs with the given inputs. It is likely possible to improve the propagation delay by slightly shortening the wires used. I have learned how to quickly build more complex circuits with circuits I have previously built.