****

**EE 4540L/6540L/CEG4322L/CEG6322L**

**FALL 2023**

**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Alex Yeoh**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Alex Yeoh Date: 31st October 2023**

**Report due date: 1st November 2023**

1. **OBJECTIVE**

To learn how to rapidly test layouts in virtuoso with a test bench.

1. **PROCEDURE**

Create a layout for gates that have minimal skew. Use the gate layouts to build a D flip flop.

1. **RESULT**

A diagram of a graph

Description automatically generated

The output for a 720nm width NAND3 gate.

A screen shot of a graph

Description automatically generated

The output for a 1440nm width NAND3 gate graph

A colorful lines and dots on a black background

Description automatically generated

The layout for a 660nm NAND3 gate.

A screen shot of a computer screen

Description automatically generated

The output for a 660nm NAND3 gate that has minimal skew.

A screen shot of a computer screen

Description automatically generated

The layout for a 960nm inverter.

A diagram of a graph

Description automatically generated

The output for a 960nm inverter with minimal skew

A computer screen shot of a circuit board

Description automatically generated

The layout for the D flip flop.

A screen shot of a computer screen

Description automatically generated

The result for the D flip flop with a Q Tphl of 284.606ps and Q Tplh is 276.616ps with an average Q propagation delay is 280.611ps. As seen in the output, the rising edge of the clock occurs just before D changes.

A table with black text and white text

Description automatically generated

As seen in the truth table and the resulting waveform graph above, the wave form follows the truth table. When preset and clear are off, Q follows D; when preset is off and clear is on, Q outputs a 0; and when preset is on and clear is off, Q outputs a 1.

1. **CONCLUSION**

My results satisfy the requirements, as all layouts have the correct outputs with the given inputs. It is potentially possible to make the propagation delay more even by looking for gate widths that would have a more even propagation delay. I have learned how to quickly test my circuit designs with a test bench.