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**EE 4540L/6540L/CEG4322L/CEG6322L**

**FALL 2023**

**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Alex Yeoh**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Alex Yeoh Date: 9th November 2023**

**Report due date: 15th November 2023**

1. **OBJECTIVE**

To learn how to complex circuits at a transistor level with individual transistors and symbols representing transistor level schematics.

1. **PROCEDURE**

Describe lab procedure by your own words.

We first build the necessary NAND, NOR, and inverter gates at a transistor level and make symbols for them. We then use the gates to build AND, OR, and D type flip flop circuits and make symbols for them. Next, we build the 4 bit binary and decimal down counter with the previously made gates. Finally, we test the counter with the given inputs and identify the fastest clock rate for the circuit where the outputs remains correct.

1. **RESULT**

A screenshot of a computer

Description automatically generated

A transistor level schematic for an inverter.

A computer screen shot of a circuit board

Description automatically generated

A transistor level schematic for NAND2.

A computer screen shot of a circuit board

Description automatically generated

A transistor level schematic for NAND3.

A computer screen shot of a circuit board

Description automatically generated

A transistor level schematic for NOR2.

A computer screen shot of a diagram

Description automatically generated

A transistor level schematic for NOR4.

A screenshot of a video game

Description automatically generated

A transistor level schematic for AND2 using a NAND2 and inverter.

A screenshot of a video game

Description automatically generated

A transistor level schematic for AND3 using a NAND3 and inverter.

A screenshot of a video game

Description automatically generated

A transistor level schematic for OR2 using a NOR2 and inverter.

A screenshot of a video game

Description automatically generated

A transistor level schematic for OR4 using a NOR4 and inverter.

A computer screen shot of a diagram

Description automatically generated

A transistor level schematic for D type flip flop using NAND3s and inverters.

A computer screen shot of a diagram

Description automatically generated

A transistor level schematic for the 4 bit binary and decimal down counter using various previously built gates.

A screen shot of a graph

Description automatically generated

The output waveform for the 4 bit binary and decimal down counter with the given inputs.

A screen shot of a computer screen

Description automatically generated

The output waveform for the 4 bit binary and decimal down counter with the shortest clock period of 1.2ns without errors.

1. **CONCLUSION**

My results satisfy the requirements, as the 4 bit binary and decimal down counter’s output waveforms are correct and I found the minimum clock period that still has a correct output waveform. I may be able to get a shorter clock period by changing the widths of the transistors to minimize the propagation delays. I have learned how to build complex circuits at the transistor level.