Solutions UE4002 Summer 2006

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an NMOS in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.
In each question, capacitances other than those mentioned may be ignored.

Question 1

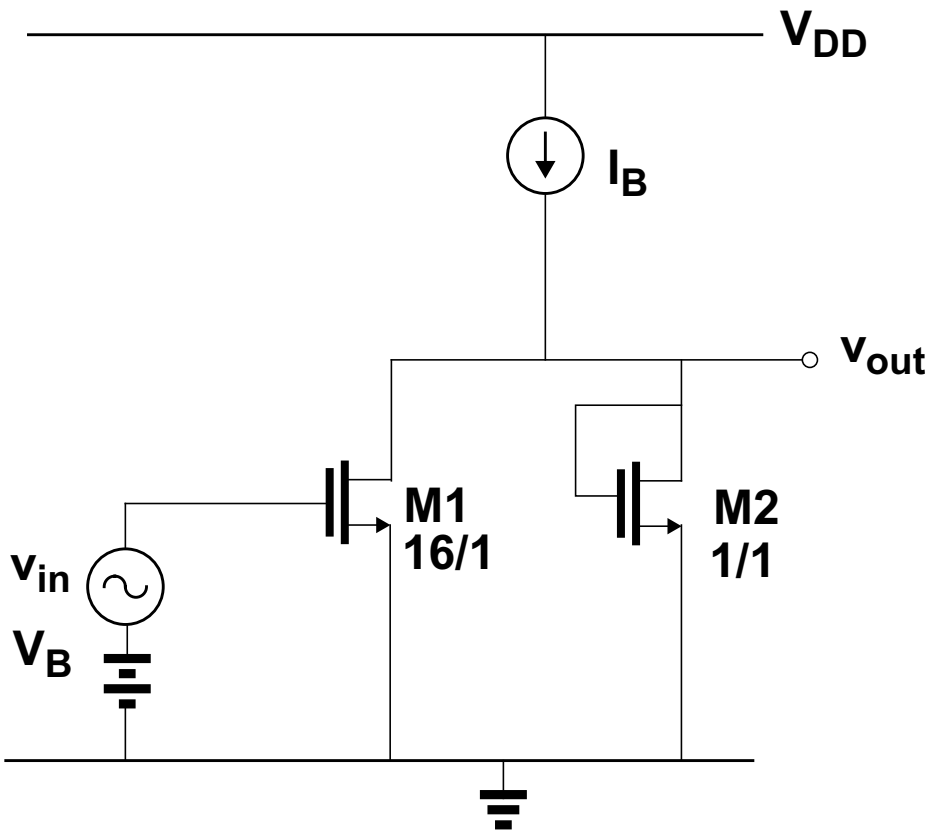

Figure 1

Figure 1 shows a common-source stage with a folded NMOS diode load.

(i) Draw the small-signal equivalent circuit for the circuit shown in Figure 1.
(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal transistor parameters of M1 and M2.
(iii) Calculate the small-signal voltage gain in dB if
V_B = 1.0V, V_{tn} = 0.75V, K_n'=200μA/V^2, I_B=200μA. Transistor dimensions in microns are as shown in Figure 1.
Assume g_{m1}, g_{m2} >> g_{ds1},g_{ds2} .
(iv) What value of bias current I_B would be needed to increase the gain by 6dB?

(i) Draw the small-signal equivalent circuit for the circuit shown in Figure 1.

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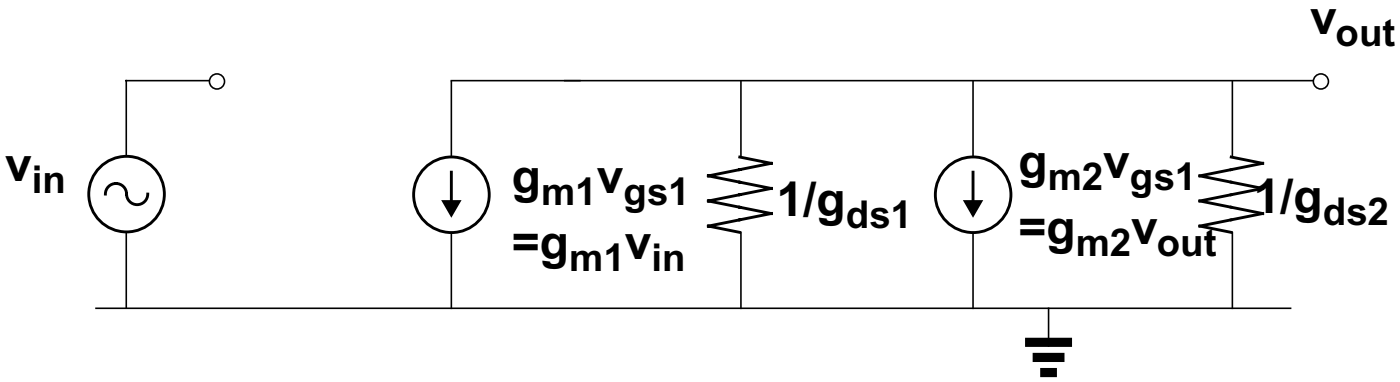

(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal transistor parameters of M1 and M2.

$$g_{m1}v_{in} + v_{out}g_{ds1} + g_{m2}v_{out} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \approx -\frac{g_{m1}}{g_{m2}}$$

Alternatively recognise that M2 is equivalent to a small-signal resistance $1/g_{m2}$ and write result directly

(iii) Calculate the small-signal voltage gain in dB if
V_B = 1.0V, V_{tn} = 0.75V, K_n'=200μA/V^2, I_B=200μA. Transistor dimensions in microns are as shown in Figure 1.
Assume g_{m1}, g_{m2} >> g_{ds1},g_{ds2}

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$$I_{D1} = \frac{K_n'}{2}\frac{W}{L}(V_{GS1}-V_{tn})^2 = \frac{200\mu A/V^2}{2}\cdot\frac{16}{1}\cdot(1-0.75)^2 = 100\mu A$$

=> 100μA through M2

$$g_{m1} = \sqrt{2K_n'\frac{W}{L}I_{D1}} = \sqrt{2\times 200\mu A/V^2\times\frac{16}{1}\times 100\mu A} = 800\mu A/V$$

$$g_{m2} = \sqrt{2K_n'\frac{W}{L}I_{D2}} = \sqrt{2\times 200\mu A/V^2\times\frac{1}{1}\times 100\mu A} = 200\mu A/V$$

$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}}{g_{m2}} = -\frac{800\mu A/V}{200\mu A/V} = -4$$

$$20\log\left|\frac{v_{out}}{v_{in}}\right| = 12dB$$

(iv) What value of bias current I_B would be needed to incease the gain by 6dB?

If IBIAS changes, bias conditions of M1 do not change.
For 6dB extra gain, g_{m2} needs to halve=> I_{D2} needs to reduce to one quarter (25μA)
=> I_B=125μA

Question 2

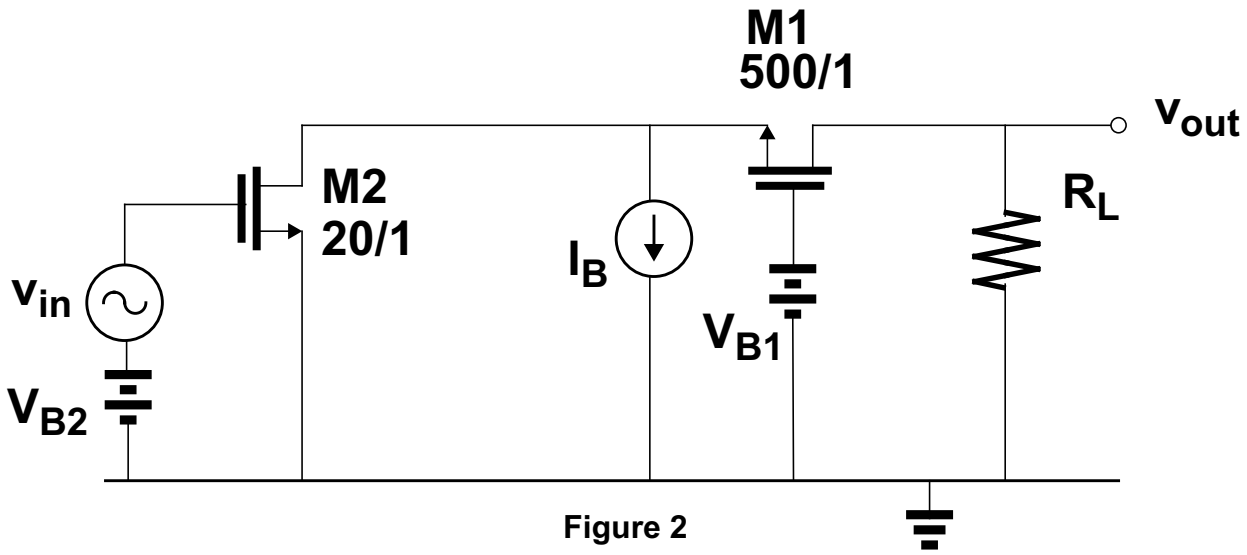

Figure 2

For this question K_n'=200μA/V^2, V_{tn}= 750mV, λ_n=0.04V^{-1}, V_{B2}=1.25V, I_B=1.5mA.
The device sizes of M1, M2 and M3 in microns are as indicated in Figure 2.
All devices are biased in saturation.

(i) Figure 2 shows a common-source stage cascaded with a common-gate stage.
Draw a small-signal equivalent circuit of of the common-gate stage, with its resistive load, showing how to measure the small-signal input resistance i.e. the resistance looking into the source of M1?

(ii) Derive an expression for the small-signal resistance looking into the source of M1, in terms of R_L and the small-signal parameters of M1. Simplify the expression assuming $g_{m1} >> g_{ds1}$.

(iii) Calculate the small-signal resistance looking into the source of M1 in Figure 2.

(iv) Calculate the small-signal voltage gain (v_{out}/v_{in}) in dB of the circuit shown in Figure 2.
Note: the common-gate stage has unity current gain.

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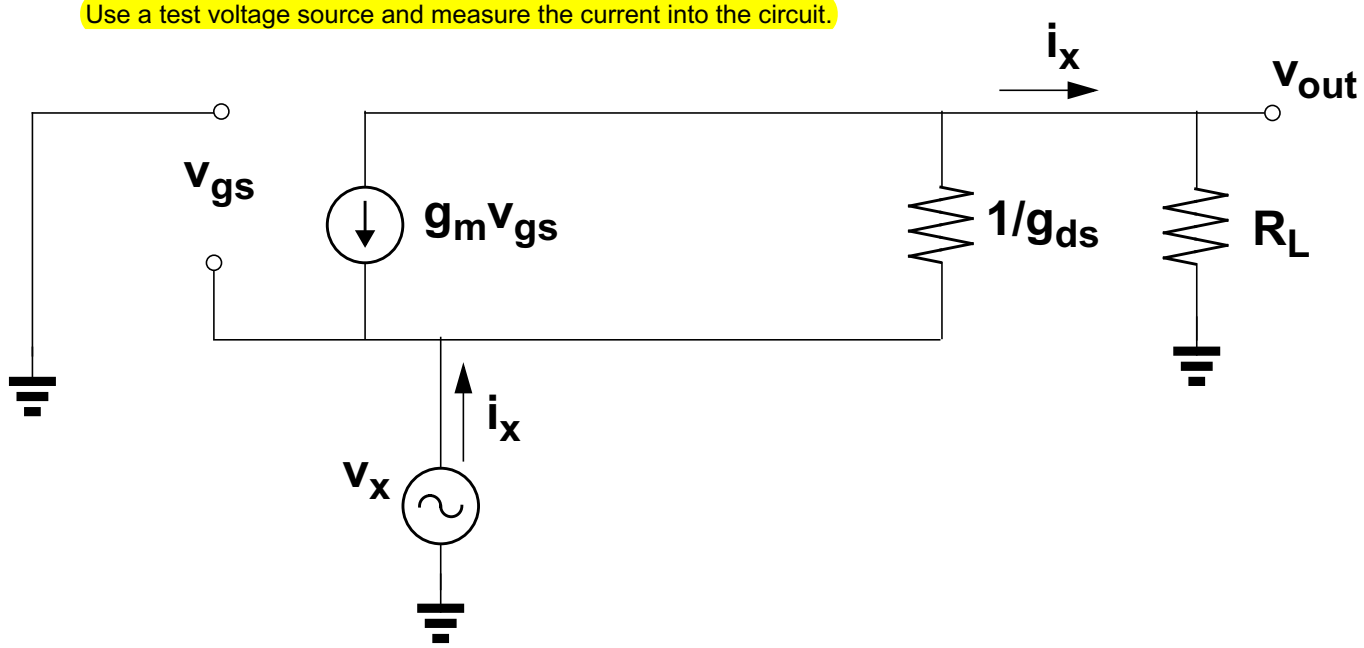
(i) Figure 2 shows a common-source stage cascaded with a common-gate stage.
Draw a small-signal equivalent circuit of of the common-gate stage, with its resistive load, showing how to measure the small-signal input resistance i.e. the resistance looking into the source of M1?

Use a test voltage source and measure the current into the circuit.



(ii) Derive an expression for the small-signal resistance looking into the source of M1, in terms of R_L and the small-signal parameters of M1. Simplify the expression assuming $g_{m1} >> g_{ds1}$.

$$i_x = (v_x - v_{out})g_{ds} - g_m v_{gs}$$

$$i_x = (v_x - i_x R_L)g_{ds} + g_m v_x$$

$$\frac{v_x}{i_x} = \frac{1 + g_{ds}R_L}{g_m + g_{ds}} \approx \frac{1}{g_m} + \frac{R_L}{\frac{g_m}{g_{ds}}}$$

(iii) Calculate the small-signal resistance looking into the source of M1 in Figure 2.

$$I_{D2} = \frac{K_n'}{2}\frac{W}{L}(V_{GS2}-V_{tn})^2 = \frac{200\mu A/V^2}{2}\cdot\frac{20}{1}\cdot(1.25-0.75)^2 = 500\mu A$$

=> 500µA through M2
=> total 2mA through M1

$$g_{m1} = \sqrt{2K_n'\frac{W}{L}I_{D1}} = \sqrt{2\times 200\mu A/V^2\times\frac{500}{1}\times 2000\mu A} = 20mA/V$$

$$g_{ds1} = \lambda I_{D1} = 0.04V^{-1}\times 2000\mu A = 80\mu A/V$$

$$r_{in} = \frac{1}{g_{m1}} + \frac{R_L}{\frac{g_{m1}}{g_{ds1}}} = \frac{1}{20mA/V} + \frac{1k\Omega}{\frac{20mA/V}{80\mu A/V}} = 50+4 = 54\Omega$$

(iv) Calculate the small-signal voltage gain (v_{out}/v_{in}) in dB of the circuit shown in Figure 2.
Note: the common-gate stage has unity current gain.

The small-signal gain is given by the product of gm of the common-source drive stage, and the resistance at the output node, which is dominated by R_L

$$g_{m1} = \sqrt{2K_n'\frac{W}{L}I_{D1}} = \sqrt{2\times 200\mu A/V^2\times\frac{20}{1}\times 500\mu A} = 2mA/V$$

$$\frac{v_{out}}{v_{in}} \approx -g_{m1}R_L = -2mA/V\times 1k\Omega = -2$$

$$20\log\left|\frac{v_{out}}{v_{in}}\right| = 6dB$$

Question 3

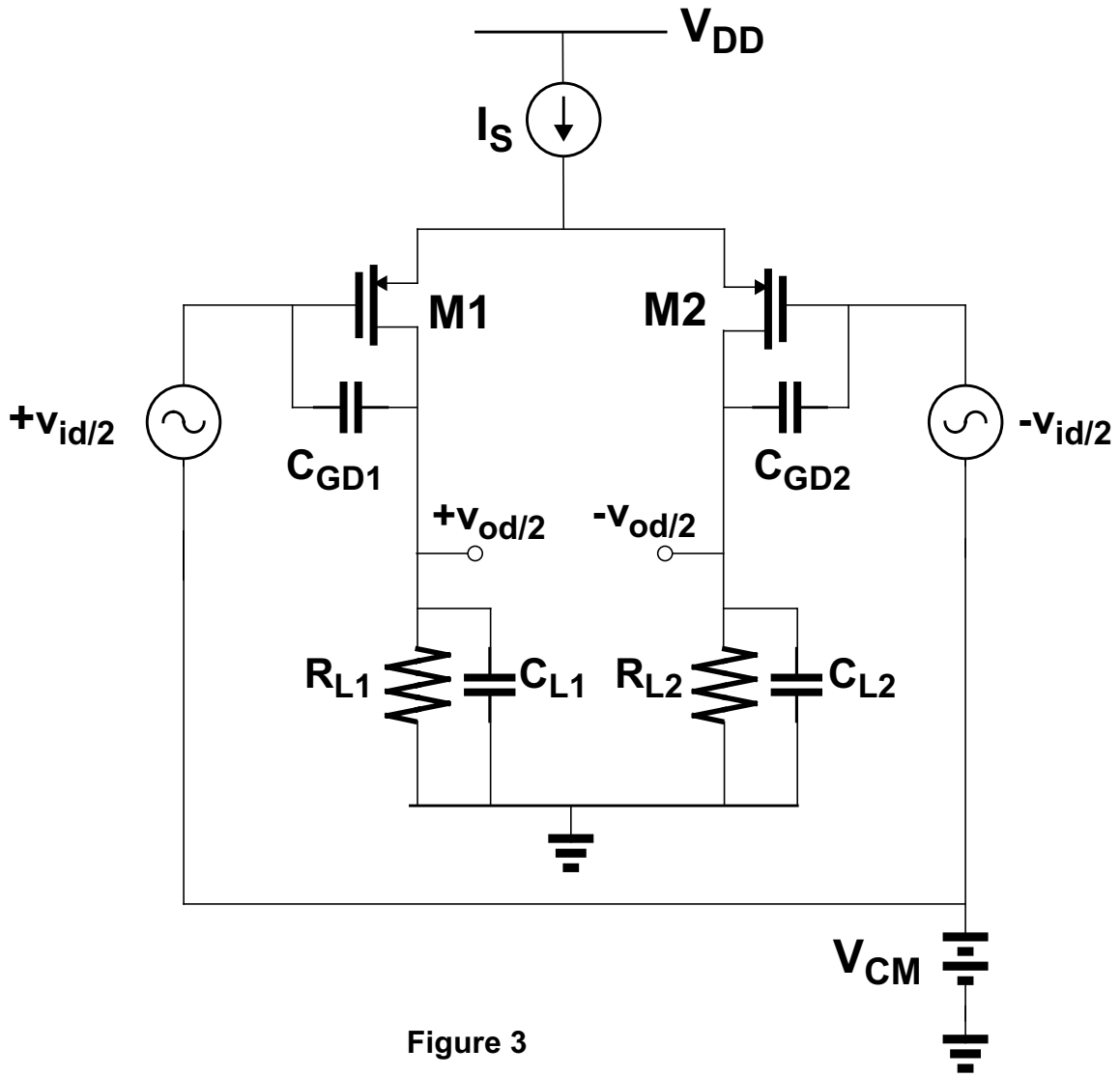


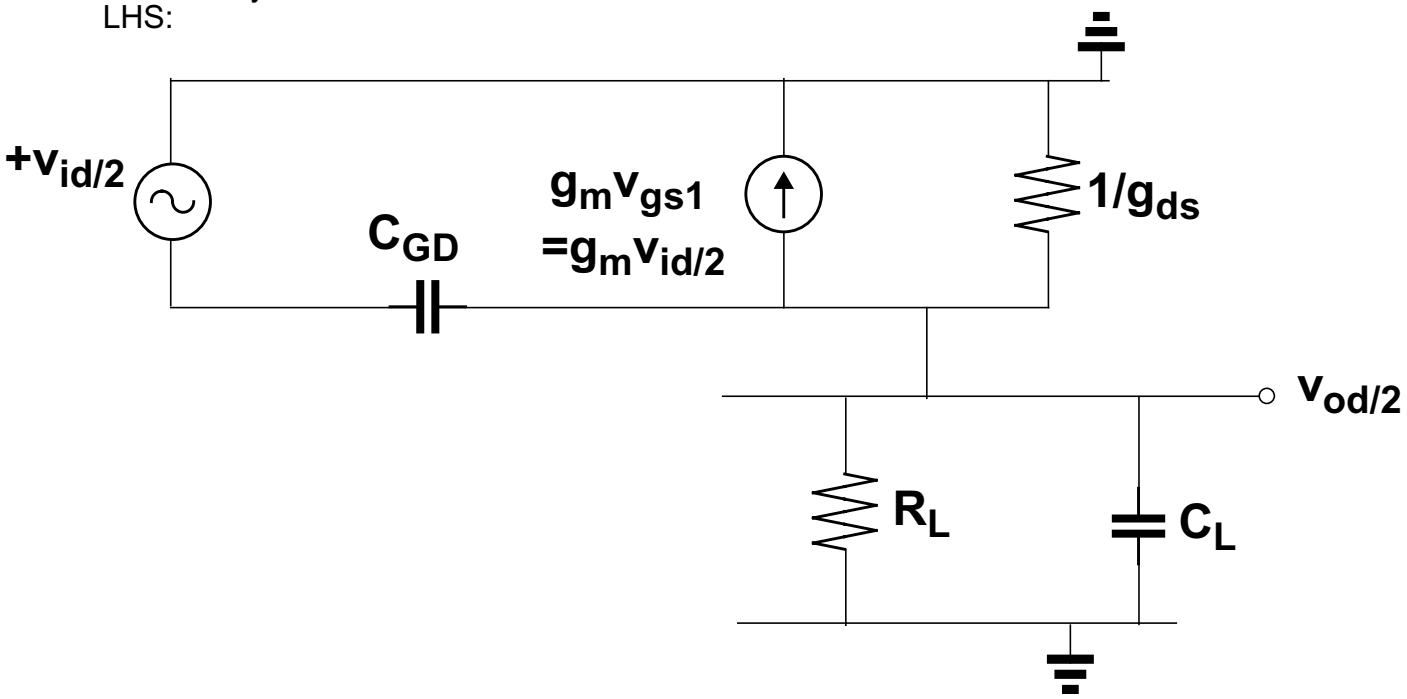
Figure 3

Figure 3 shows a PMOS differential stage with resistive and capacitive load.
The stage is symmetric i.e. M1 and M2 have the same dimensions, $R_{L1}=R_{L2}$, $C_{GD1}=C_{GD2}$.
For the questions below you may assume g_{ds1}, g_{ds2} << $1/R_{L1}$, $1/R_{L2}$ and that all devices are biased in saturation.

(i) It is required to derive the high-frequency transfer function of the small-signal voltage gain (v_{out}/v_{in}). Draw a small-signal model to enable the high-frequency transfer function to be derived.
(ii) Derive an expression for the high-frequency transfer function.
(iii) Calculate the low-frequency gain (v_{out}/v_{in}) in dB, and the break (i.e. pole and/or zero) frequencies, if $K_p'=50\mu A/V^2$, $I_S = 200\mu A$, $R_{L1} = R_{L2} = 20k\Omega$, $C_{GD1} = C_{GD2} = 0.1pF$, $C_{L1}= C_{L2}= 0.9pF$.
(iv) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the break frequencies.

(i) It is required to derive the high-frequency transfer function of the small-signal voltage gain (v_{out}/v_{in}). Draw a small-signal model to enable the high-frequency transfer function to be derived.
Derive an expression for the high-frequency transfer function.

Circuit is symmetrical => use half-circuit method.
LHS:



(ii) Derive an expression for the high-frequency transfer function.

KCL at output node

$$g_m\frac{v_{id}}{2}+\frac{v_{od}}{2}g_{ds1}+\frac{v_{od}}{2}\frac{1}{R_L}+\frac{v_{od}}{2}s(C_L)-\left(\frac{v_{id}}{2}-\frac{v_{od}}{2}\right)sC_{GD}=0$$

$$\frac{\frac{v_{od}}{2}}{\frac{v_{id}}{2}}=-\frac{g_m-sC_{GD}}{\frac{1}{R_L}+g_{ds}+s(C_L+C_{GD})}$$

$$\frac{\frac{v_{od}}{2}}{\frac{v_{id}}{2}}=-\frac{g_m\left(1-\frac{sC_{GD}}{g_m}\right)}{\left(\frac{1}{R_L}+g_{ds}\right)\left(1+\frac{s(C_{GD}+C_L)}{\frac{1}{R_L}+g_{ds}}\right)}$$

Simplify assuming $1/R_L >> g_{ds}$

$$\frac{\frac{v_{od}}{2}}{\frac{v_{id}}{2}}\approx-\frac{g_mR_L\left(1-\frac{sC_{GD}}{g_m}\right)}{(1+sR_L(C_{GD}+C_L))}$$

An analysis of the RHS would give the same result:

$$\frac{-\frac{v_{od}}{2}}{-\frac{v_{id}}{2}}\approx-\frac{g_mR_L\left(1-\frac{sC_{GD}}{g_m}\right)}{(1+sR_L(C_{GD}+C_L))}$$

Subtracting the two results gives

$$\frac{v_{od}}{v_{id}}\approx-\frac{g_mR_L\left(1-\frac{sC_{GD}}{g_m}\right)}{(1+sR_L(C_{GD}+C_L))}$$

(iii) Calculate the low-frequency gain (v_{out}/v_{in}) in dB, and the break (i.e. pole and/or zero) frequencies, if $K_p'=50\mu A/V^2$, $I_S = 200\mu A$, $R_{L1} = R_{L2} = 20k\Omega$, $C_{GD1} = C_{GD2} = 0.1pF$, $C_{L1}= C_{L2}= 0.9pF$.

$I_S/2$ through M1

$$g_{m1} = \sqrt{2K_p'\frac{W}{L}I_{D1}} = \sqrt{2\times 50\mu A/V^2 \times \frac{25}{1}\times 100\mu A} = 500\mu A/V$$

Low-frequency gain given by

$$\frac{v_{out}}{v_{in}} \approx -g_m R_L = 500\mu A/V \times 20k\Omega = -10 = 20dB$$

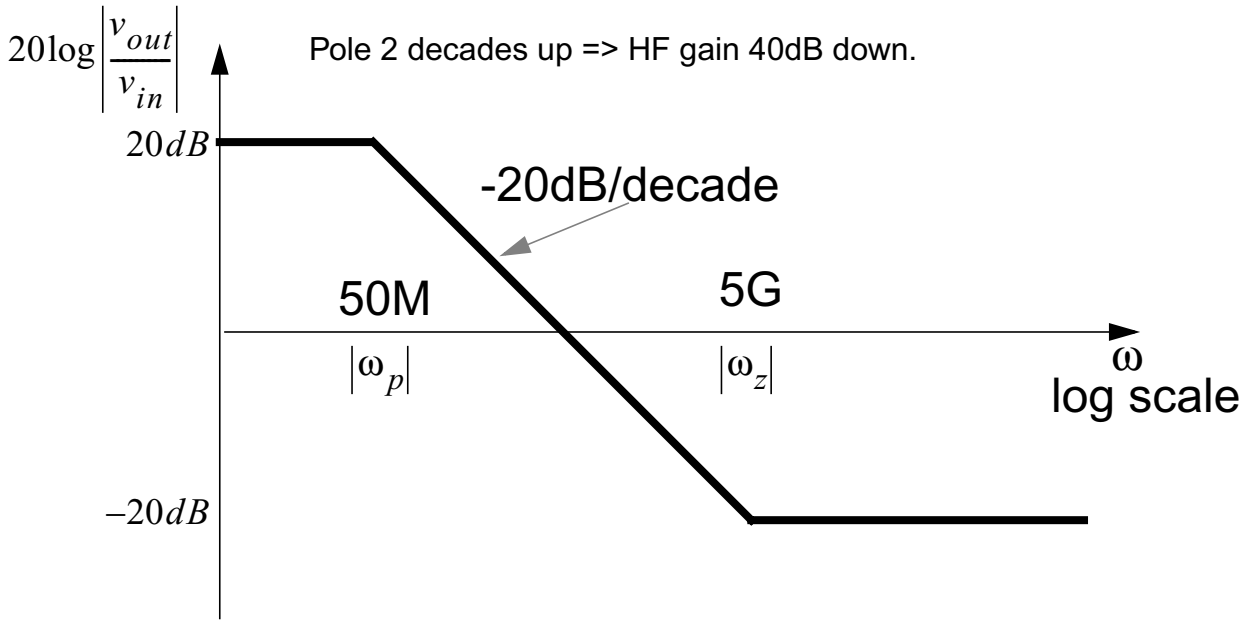
Zero frequency given by

$$|\omega_z| = \frac{g_m}{C_{GD}} = \frac{500\mu A/V}{0.1\,pF} = 5Grad/s$$

Pole frequency given by

$$|\omega_p| = \frac{1}{R_L(C_{GD}+C_L)} = \frac{1}{20k\Omega(0.1\,pF+0.9\,pF)} = 50Mrad/s$$

(iv) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the break frequencies.



Question 4

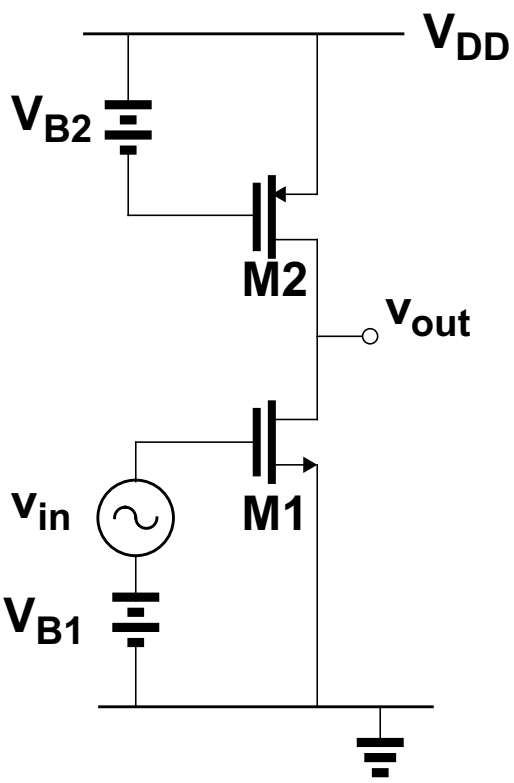


Figure 4a

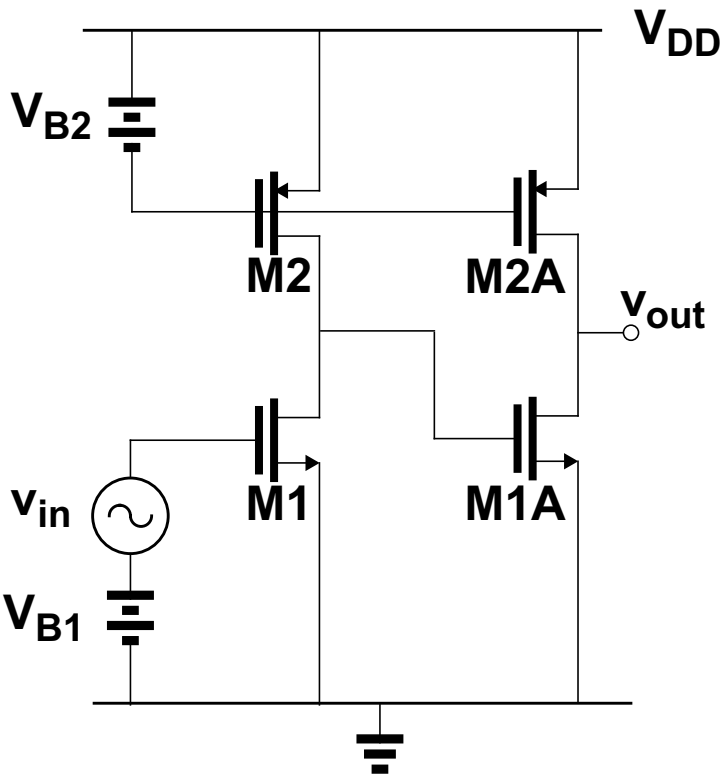


Figure 4b

For the circuits shown in Figure 4a and 4b, assume all transistors are operating in saturation.
Only thermal noise sources need be considered.

Take Boltzmann's constant $k=13.8X10^{-24}J/^oK$, temperature $T=300^oK$.

(i) Draw the small-signal model for the circuit shown in Figure 4a.
What is the small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters of M1 and M2?

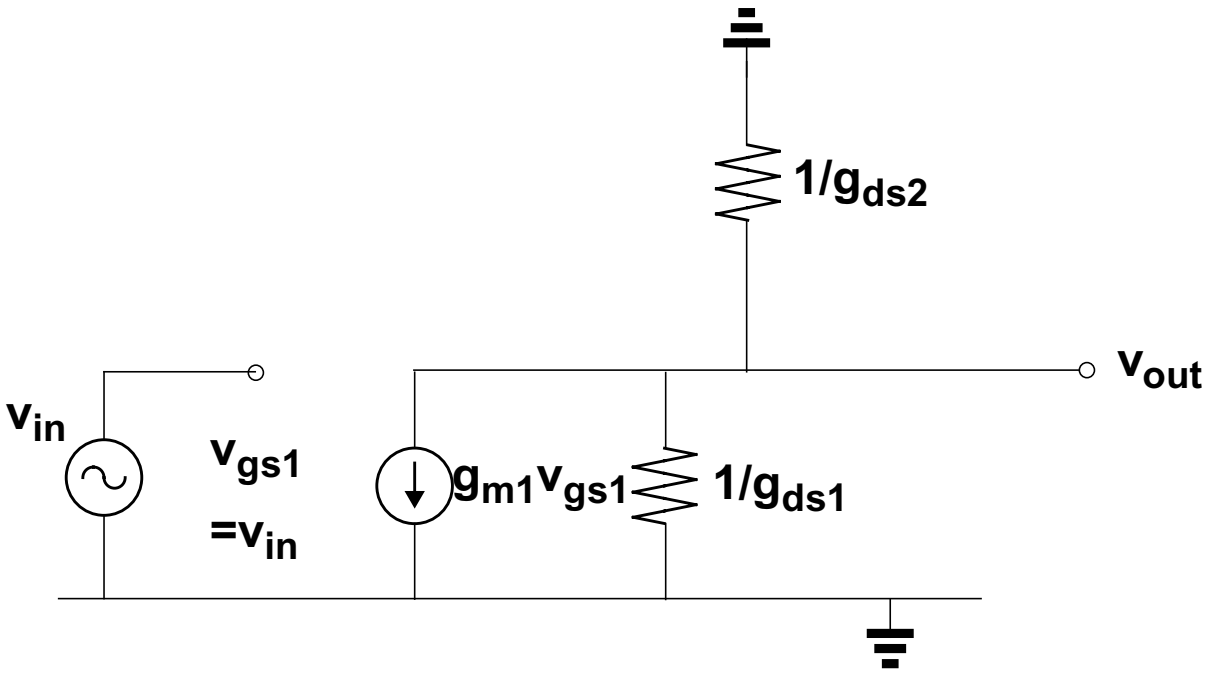
(ii) What is the input-referred noise voltage density in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T?

(iii) Calculate the input-referred noise voltage density if $g_{m1}=200\mu A/V$, $g_{m2}=50\mu A/V$, $g_{ds1}=g_{ds2}=5\mu A/V$.
What is the noise voltage density at the output?
(Note: the units $\mu A/V$ are equivalent to μS).

(iv) The gain stage shown in Figure 4a is cascaded with an identcal gain stage, with identical transistor dimensions and biasing conditions, as shown in Figure 4b. Calculate the input-referred noise voltage density of this circuit.
What is the total input-referred voltage noise in a bandwidth of 10MHz to 100MHz?

Solution

(i) Draw the small-signal model for the circuit shown in Figure 4a.
What is the small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters of M1 and M2?

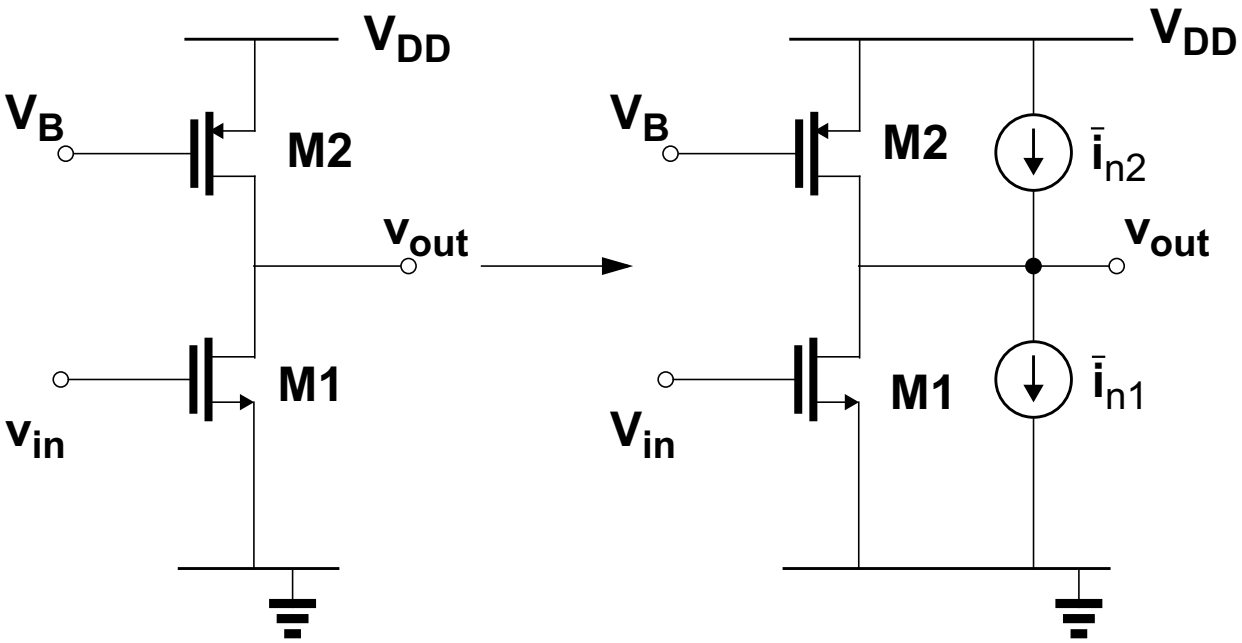


Current at output node

$$g_{m1}v_{in} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

(ii) What is the input-referred noise voltage density in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T?



Noise current of MOS: $\overline{i_n^2} = 4kT\left(\frac{2}{3}g_m\right)$

Noise sources uncorrelated => total noise is the sum of squares

$$\overline{i_{nt}^2} = i_{n1}^2 + i_{n2}^2 \qquad \text{or} \qquad \overline{i_{nt}} = \sqrt{i_{n1}^2 + i_{n2}^2} \qquad \text{rms value}$$

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}}{g_{m1}} \qquad \text{rms noise} \quad V/\sqrt{Hz}$$

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \sqrt{4kT \cdot \frac{2}{3}\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2}\right)}$$

(iii) Calculate the input-referred noise voltage density if g_{m1}=200μA/V, g_{m2}=50μA/V, g_{ds1}=g_{ds2}=5μA/V. What is the noise voltage density at the output?
(Note: the units μA/V are equivalent to μS).

Noise density at input

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \sqrt{4kT \cdot \frac{2}{3}\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2}\right)} = \sqrt{4kT \cdot \frac{2}{3}\left(\frac{1}{200\mu A/V} + \frac{50\mu A/V}{(200\mu A/V)^2}\right)} = 8.3nV/(\sqrt{Hz})$$

To get voltage noise at output multiply input-referred noise by gain of circuit

$$\overline{v_{no}} = \overline{v_{ni}}\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

$$Gain = \frac{g_{m1}}{g_{ds1} + g_{ds2}} = \frac{200\mu A/V}{5\mu A/V + 5\mu A/V} = 20$$

$$\overline{v_{no}} = 8.3nV/(\sqrt{Hz}) \times 20 = 166nV/(\sqrt{Hz})$$

(iv) The gain stage shown in Figure 4a is cascaded with an identcal gain stage, with identical transistor dimensions and biasing conditions, as shown in Figure 4b. Calculate the input-referred noise voltage density of this circuit. What is the total input-referred voltage noise in a bandwidth of 10MHz to 100MHz?

Input Noise density of second stage is divided by gain of second stage and added quadratically to noise of first stage

$$\overline{v_{nitot}} = \sqrt{v_{ni1}^2 + \left(\frac{v_{ni2}}{Gain}\right)^2} = \sqrt{8.3^2 + \left(\frac{8.3}{20}\right)^2} \approx 8.3nV/(\sqrt{Hz})$$

Alternatively point out that noise of second stage divided by gain of first stage makes it negligible.

$$\overline{v_{nitot10to100MHz}} = v_{nitot}\sqrt{90MHz} = (8.3nV/(\sqrt{Hz}))\sqrt{90MHz} \approx 78.8\mu V$$