Solutions UE4002 Summer 2008

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an NMOS in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS} - V_{tn})^2(1 + \lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n = \lambda_p = 0$.
In each question, capacitances other than those mentioned may be ignored.

Question 1

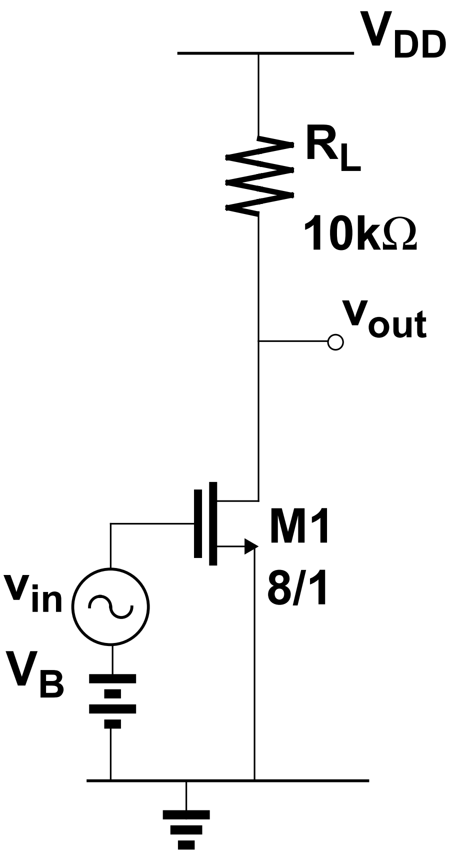

Figure 1

(i) Draw the small-signal equivalent circuit for the common-source stage shown in Figure 1.
(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) of this circuit in terms of the small-signal transistor parameters and R_L.
(iii) Calculate the small-signal voltage gain (v_{out}/v_{in}) in dB if
V_{DD}=5V, V_B = 1.25V, V_{tn} = 0.75V, K_n'=200µA/V^2.
Assume M1 is in saturation and $R_L << 1/g_{ds1}$.
Transistor dimensions in microns, and resistor value are as shown in Figure 1.
(iv) What is the maximum gain that can be achieved by increasing the width of M1?
Assume again $R_L << 1/g_{ds1}$.

(i) Draw the small-signal equivalent circuit for the CMOS common-source stage shown in Figure 1.

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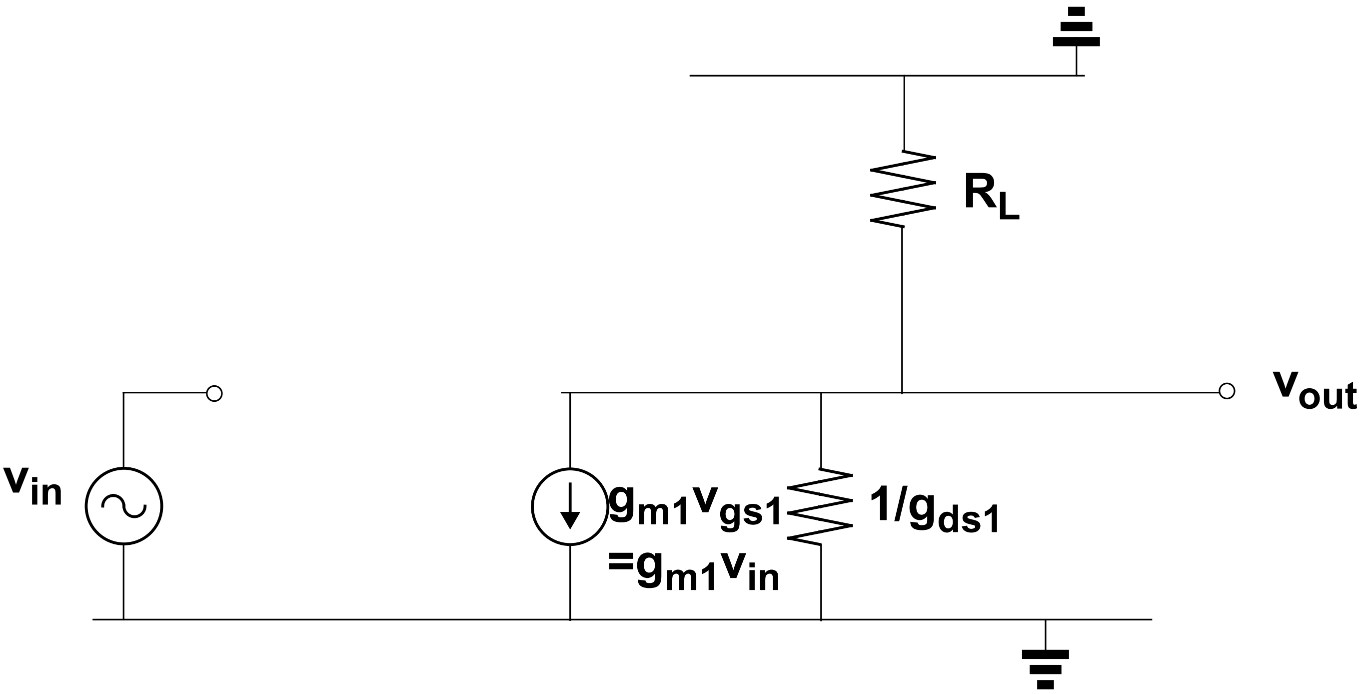

(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) of this circuit in terms of the small-signal transistor parameters and R_L.

KCL at output node

$$g_{m1}v_{in} + v_{out}g_{ds1} + \frac{v_{out}}{R_L} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + \frac{1}{R_L}}$$

(iii) Calculate the small-signal voltage gain (v_{out}/v_{in}) in dB if V_{DD}=5V, V_B = 1.25V, V_{tn} = 0.75V, K_n'=200μA/V^2.
Assume M1 is in saturation and $R_L \ll 1/g_{ds1}$.

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$$I_{D1} = \frac{K_n'}{2}\frac{W}{L}(V_{GS1}-V_{tn})^2 = \frac{200\mu A/V^2}{2}\cdot\frac{8}{1}\cdot(1.25-0.75)^2 = 200\mu A$$

$$g_{m1} = \sqrt{2K_n'\frac{W}{L}I_{D1}} = \sqrt{2\times 200\mu A/V^2\times\frac{8}{1}\times 200\mu A} = 800\mu A/V$$

$$\frac{v_{out}}{v_{in}} \approx -g_{m1}R_{L1} = -800\mu A/V\times 10k\Omega = -8$$

$$20\log\left|\frac{v_{out}}{v_{in}}\right| = 18dB$$

(iv) What is the maximum gain that can be achieved by increasing the width of M1?
Assume again $R_L \ll 1/g_{ds1}$.

If only the width of M1 is increased, then the current increases proportionally, but V_{GS}-V_t is unchanged. The increase in current will increase gm1, increasing gain until the extra voltage drop across the load resistor will push M1 out of saturation. At this point the gain is maximum.

$$V_{GS1}-V_{tn} = 1.25V-0.75V = 0.5V$$

For M1 in saturation: $V_{DS1min} = V_{GS1}-V_{tn}$

$$V_{D1min} = V_{outmin} = 0.5V$$

$$V_{R_{Lmax}} = V_{DD}-V_{outmin} = 5V-0.5V = 4.5V$$

$$I_{max} = \frac{V_{R_{Lmax}}}{R_{L1}} = \frac{4.5V}{10k} = 450\mu A$$

$$g_{m1max} = \frac{2I_D}{(V_{GS1}-V_{tn})} = \sqrt{\frac{2\times 450\mu A}{0.5V}} = 1800\mu A/V$$

$$\left(\frac{v_{out}}{v_{in}}\right)_{max} \approx -g_{m1max}R_{L1} = -1800\mu A/V\times 10k\Omega = -18 = \underline{\underline{25.1dB}}$$

Question 2

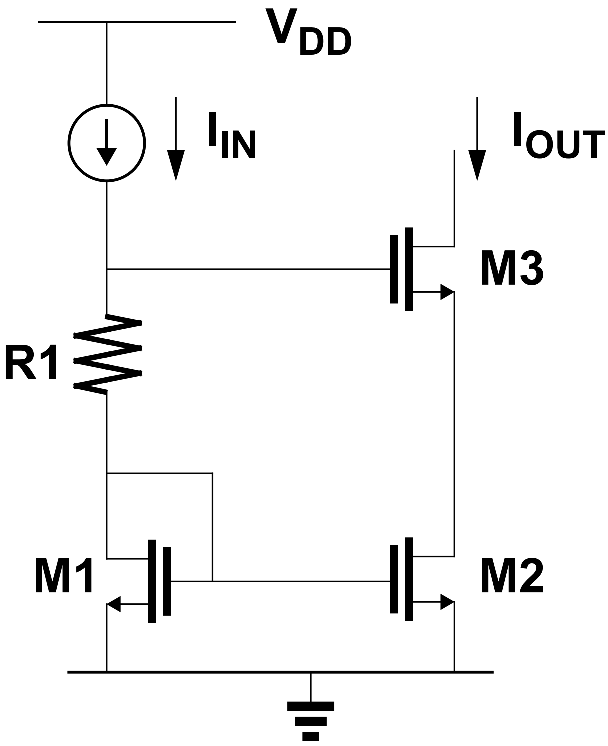


Figure 2

Figure 2 shows a cascoded current mirror.
Assume $K_n' = 200\mu A/V^2$, $V_{tn} = 800mV$.
All transistors have W/L=25/2.

(i) If $I_{IN} = I_{OUT} = 200\mu A$, what is the minimum voltage at the output node, i.e. the drain of M3, such that all transistors are biased in saturation?
What minimum value of R1 is required to ensure M2 is in saturation?

(ii) The current mirror is modified by changing R1 and M2 only.
What value of R1, and W/L of M2 would be required to increase the output current to 800µA and still ensure all transistors are in saturation?

(iii) It is required to measure the small-signal output resistance of the current mirror (i.e. the small-signal resistance looking into the drain of M3). Draw a small signal model showing how this can be done.

(iv) Derive an expression for the small-signal output resistance.
Show by assuming $g_{m1}, g_{m2}, g_{m3} >> g_{ds1}, g_{ds2}, g_{ds3}$ that this approximates to

$$r_{out} = \frac{g_{m3}}{g_{ds3}} \cdot \frac{1}{g_{ds2}}$$

(i) If $I_{IN}=I_{OUT}=200\mu A$, what is the minimum voltage at the output node, i.e. the drain of M3, such that all transistors are biased in saturation?
What minimum value of R1 is required to ensure M2 is in saturation?

Bias current of M1, M2, M3 is 200µA. All have same W/L so same V_{GT}

$$I_{D1} = \frac{K_n'}{2}\frac{W}{L}(V_{GS1}-V_t)^2 \Rightarrow V_{GS1}-V_t = \sqrt{\frac{2I_{D1}}{K_n'\frac{W}{L}}} = \sqrt{\frac{2\cdot 200\mu A}{200\mu A/V^2\frac{25}{2}}}$$

$$V_{GS1}-V_t = 400mV$$

$$V_{D3min} = (V_{GS2}-V_t)+(V_{GS3}-V_t) = 0.4V+0.4V = \underline{\underline{0.8V}}$$

Then

$$V_{G3} = (V_{GS2}-V_t)+(V_{GS3}-V_t)+V_t = 0.4V+0.4V+0.8V = 1.6V$$

$$R_1 = \frac{V_{G3}-V_{G1}}{I_{IN}} = \frac{1.6V-1.2V}{200\mu A} = \underline{\underline{2k\Omega}}$$

(ii) The current mirror is modified by changing R1 and M2 only.
What value of R1, and W/L of M2 would be required to increase the output current to 800µA and still ensure all transistors are in saturation?

$$I_{D2} = \frac{K_n'}{2}\frac{W}{L}(V_{GS2}-V_t)^2$$

For I_{D2} = 800µA, same V_{GS}-V_t, W/L needs to increase by 4 times, e.g. to 50/2

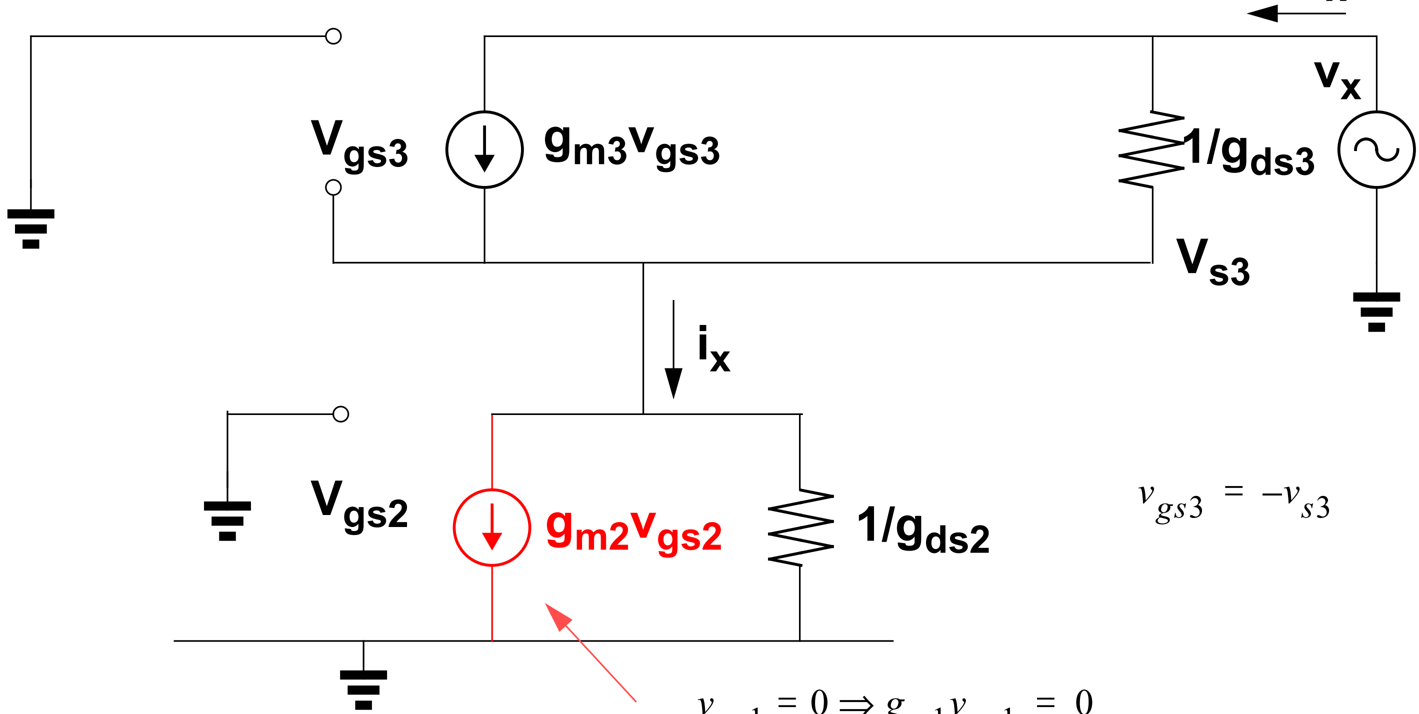
For I_{D3} = 800µA, V_{GS3}-V_t needs to increase by 2 times, i.e. to 0.8V, so V_{G3}=2V

$$R_1 = \frac{V_{G3}-V_{G1}}{I_{IN}} = \frac{2V-1.2V}{200\mu A} = \underline{\underline{4k\Omega}}$$

(iii) It is required to measure the small-signal output resistance of the current mirror (i.e. the small-signal resistance looking into the drain of M3). Draw a small signal model showing how this can be done.

Cascode: Output Resistance R_{out}

Short input, apply test voltage at output:, measure current i_x



$$v_{gs3} = -v_{s3}$$

$$v_{gs1} = 0 \Rightarrow g_{m1}v_{gs1} = 0$$

(iv) Derive an expression for the small-signal output resistance.
Show by assuming $g_{m1}, g_{m2}, g_{m3} >> g_{ds1}, g_{ds2}, g_{ds3}$ that this approximates to

$$r_{out} = \frac{g_{m3}}{g_{ds3}} \cdot \frac{1}{g_{ds2}}$$

$$i_x = g_{m3}v_{gs3} + (v_x - v_s)g_{ds3}$$

$$i_x = -g_{m3}v_{s3} + v_x g_{ds3} - v_s g_{ds3}$$

Since $$v_{s3} = \frac{i_x}{g_{ds2}}$$

$$i_x = -g_{m3}\frac{i_x}{g_{ds2}} + v_x g_{ds3} - \frac{i_x}{g_{ds2}}g_{ds3}$$

$$r_{out} = \frac{v_x}{i_x} = \frac{1}{g_{ds3}}\left(1 + \frac{g_{m3}}{g_{ds2}} + \frac{g_{ds3}}{g_{ds2}}\right) \approx \frac{1}{g_{ds2}}\left(\frac{g_{m3}}{g_{ds3}}\right)$$

Question 3

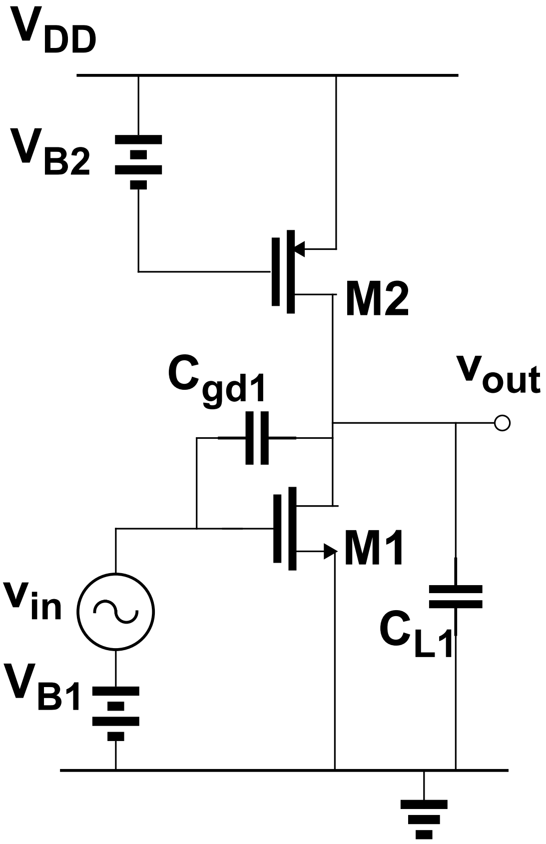


Figure 3a

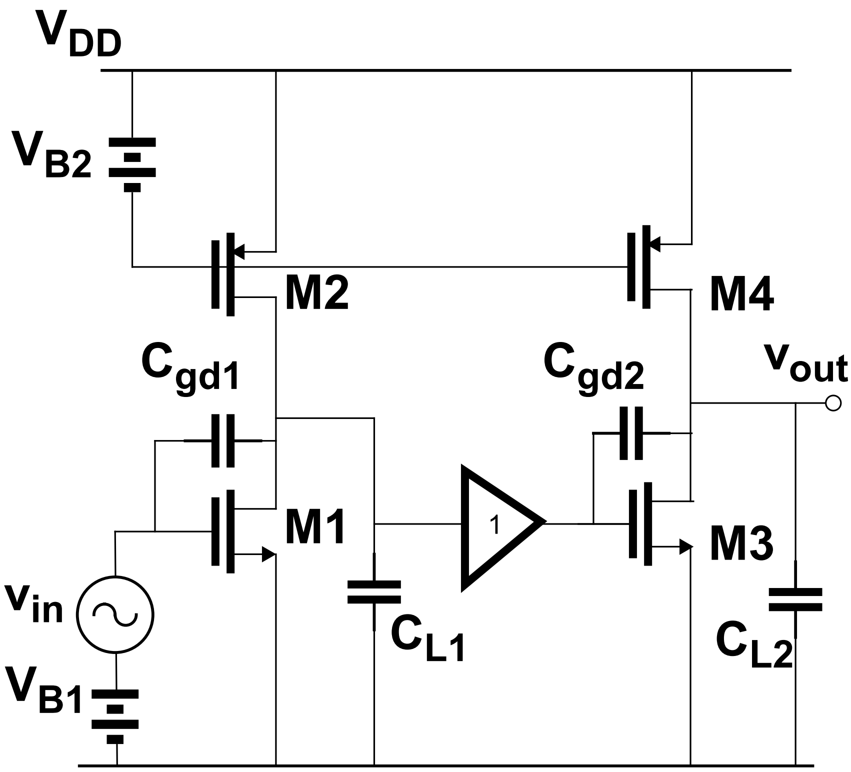
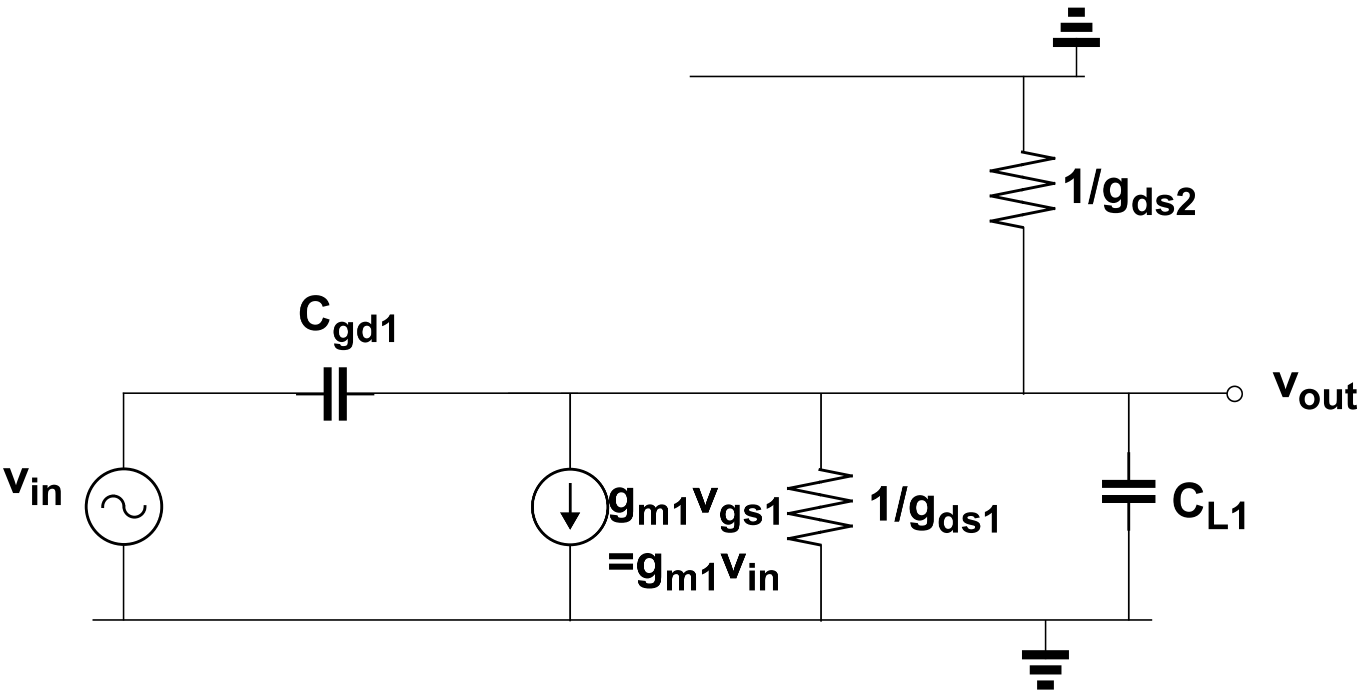


Figure 3b

(i) Draw the small-signal equivalent circuit for the gain stage shown in Figure 3a.
(ii) Derive an expression for the high frequency transfer function of the small-signal voltage gain (v_{out}/v_{in}).
(iii) Calculate the dc gain in dB, the break frequencies (i.e. pole and/or zero frequencies) if V_{B1}=1.1V, V_{tn}=0.7V, $\lambda_n=\lambda_p$=0.025V^{-1}, C_{L1}=0.9pF, C_{gd1}=0.1pF.
Assume both transistors are in saturation with a drain current of 200µA.
(iv) The circuit shown in Figure 3a is cascaded with an ideal unity gain buffer and an identical stage with an identical load capacitance as shown in Figure 3b. Assuming M3 and M4 have the same DC operating points as M1 and M2 respectively, draw the Bode diagram of the gain of the cascaded circuit, indicating the values of the DC gain in dB, roll-off, and the value of the gain at frequencies well above the highest break frequency.

(i) Draw the small-signal equivalent circuit for the gain stage shown in Figure 3a.



(ii) Derive an expression for the high frequency transfer function (v_{out}/v_{in}).

KCL at output node

$$g_{m1}v_{in} + v_{out}g_{ds1} + v_{out}g_{ds2} + v_{out}sC_{L1} + (v_{out} - v_{in})(sC_{gd1}) = 0$$

$$(g_{m1} - sC_{gd1})v_{in} = -(g_{ds1} + g_{ds2} + sC_L + sC_{gd1})v_{out}$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} - sC_{gd1}}{g_{ds1} + g_{ds2} + sC_L + sC_{gd1}}$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}\left(1 - \frac{sC_{gd1}}{g_{m1}}\right)}{(g_{ds1} + g_{ds2})\left(1 + \frac{s(C_L + C_{gd1})}{g_{ds1} + g_{ds2}}\right)}$$

(iii) Calculate the dc gain in dB, the break frequencies (i.e. pole and/or zero frequencies) if V_{B1}=1.1V, V_{tn}=0.7V, $\lambda_n=\lambda_p=0.025V^{-1}$, C_{L1}=0.9pF, C_{gd1}=0.1pF.
Assume both transistors are in saturation with a drain current of 200µA.

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{(g_{ds1}+g_{ds2})\left(1+\frac{sC_L}{g_{ds1}+g_{ds2}}\right)}$$

DC Gain given by

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1}+g_{ds2}}$$

$$g_{m1} = \frac{2I_D}{(V_{GS1}-V_{tn})} = \frac{2\times 200\mu A}{1.1-0.7} = 1mA/V$$

$$g_{ds1} = \lambda I_D = 0.025V^{-1}\times 200\mu A = 5\mu A/V$$

$$g_{ds2} = \lambda I_D = 0.025V^{-1}\times 200\mu A = 5\mu A/V$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1}+g_{ds2}} = \frac{1mA/V}{5\mu A/V+5\mu A/V} = 100 \Rightarrow \underline{\underline{40dB}}$$

Pole frequency given by

$$|\omega_p| = \frac{g_{ds1}+g_{ds2}}{C_{L1}+C_{gd1}} = \frac{5\mu A/V+5\mu A/V}{0.9pF+0.1pF} = \underline{\underline{10Mrad/s}}$$

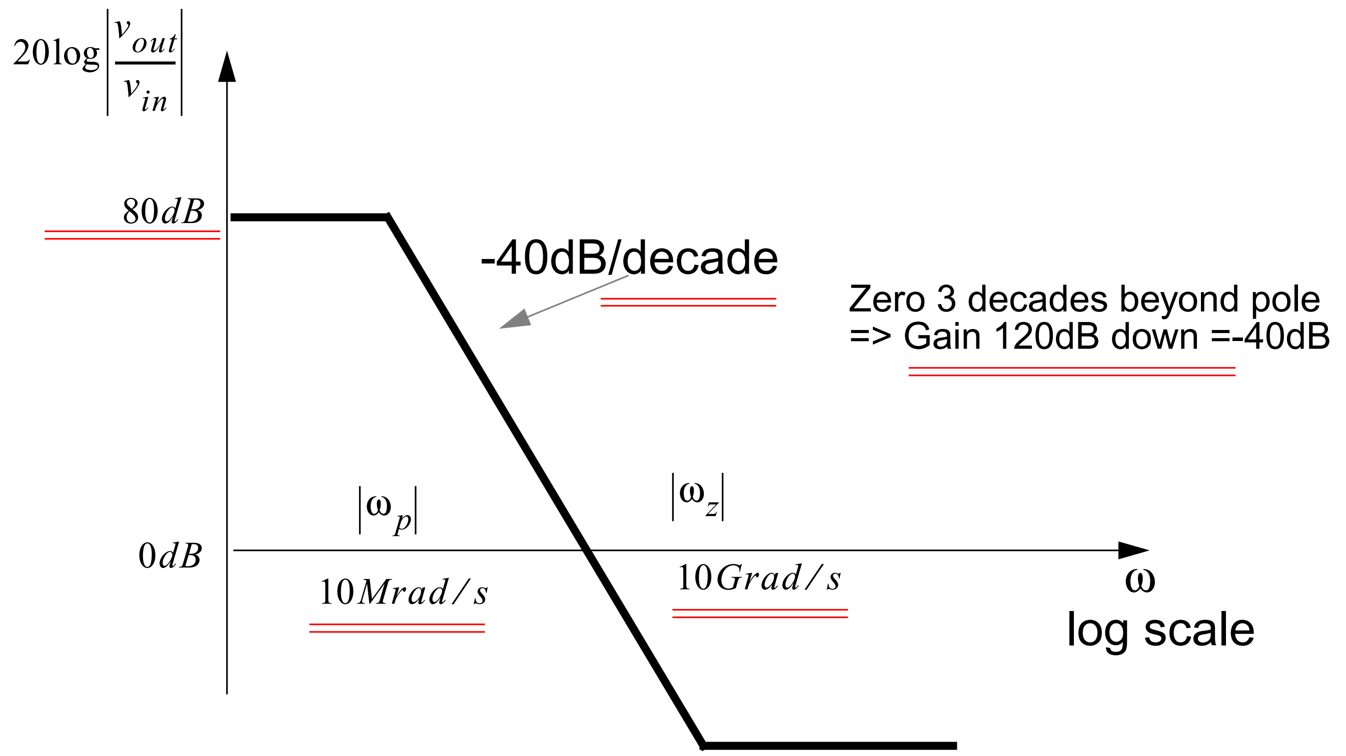
Zero frequency given by

$$|\omega_z| = \frac{g_{m1}}{C_{L1}+C_{gd1}} = \frac{1mA/V}{0.1pF} = \underline{\underline{10Grad/s}}$$

(iv) The circuit shown in Figure 3a is cascaded with an ideal unity gain buffer and an identical stage with an identical load capacitance as shown in Figure 3b. Assuming M3 and M4 have the same DC operating points as M1 and M2 respectively, draw the Bode diagram of the gain of the cascaded circuit, indicating the values of the DC gain in dB, roll-off, and the value of the gain at frequencies well above the highest break frequency.

Gain given by

$$\frac{v_{out}}{v_{in}} = \left(-\frac{g_{m1}}{g_{ds1} + g_{ds2}}\right)^2 = 100^2 \Rightarrow 80dB$$



Question 4

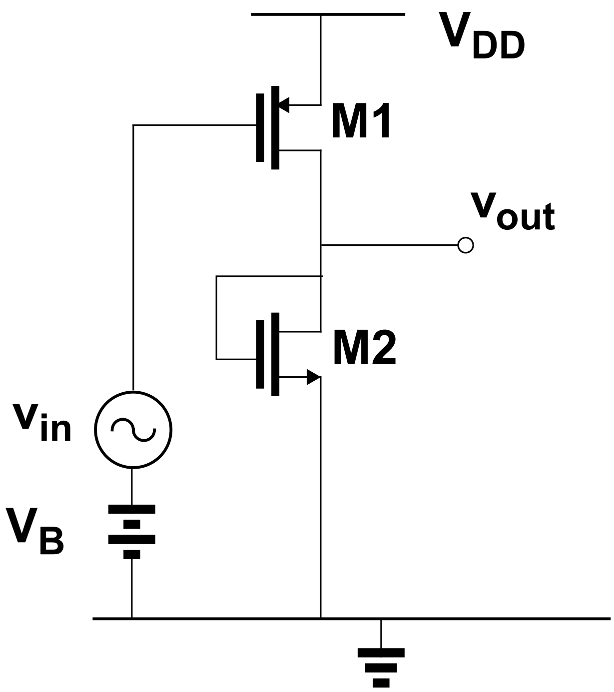


Figure 4

Assume M1 and M2 are operating in saturation. Only thermal noise sources need be considered.
For calculations take Boltzmann's constant $k=1.38X10^{-23}J/^oK$, temperature $T=300^oK$

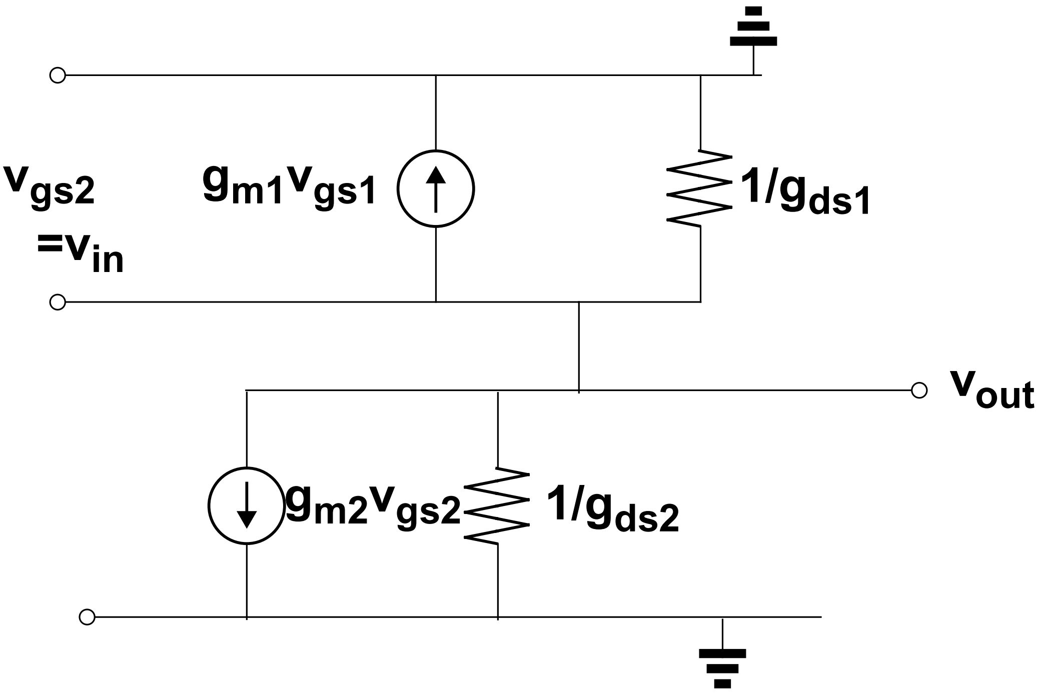
(i) Draw the small-signal model for the circuit shown in Figure 4.
What is the low-frequency small signal voltage gain (v_{out}/v_{in}) of the circuit shown in Figure 4?
Assume that $g_{m1},g_{m2} >> g_{ds1},g_{ds2}$.

(ii) What is the input-referred thermal noise voltage density in terms of the small signal parameters of M1 and M2, Boltzmann's constant k and temperature T?

(iii) Calculate the input-referred thermal noise voltage density of the circuit.
For this calculation take $|V_{GS1}| = 1V$, $V_{GS2} = 2.8V$, $V_{tn} = 0.8V$, $V_{tp} = -0.8V$.
The drain current of M1 is 100µA.

(iv) Calculate the total noise voltage at the output over a bandwidth of 1MHz.
If the input signal v_{in} is a $1mV_{rms}$ sine wave in this bandwidth, calculate the signal-to-noise ratio in dB at the output over the bandwidth of 1MHz.

(i) What is the low-frequency small signal voltage gain (v_{out}/v_{in}) of the circuit shown in Figure 4? Assume that $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$.



Assume that $g_{m1} >> g_{ds1}, g_{ds2}$ and that $g_{m2} >> g_{ds1}, g_{ds2}$

Current at output node

$$g_{m1}v_{gs1} + g_{m2}v_{gs2} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

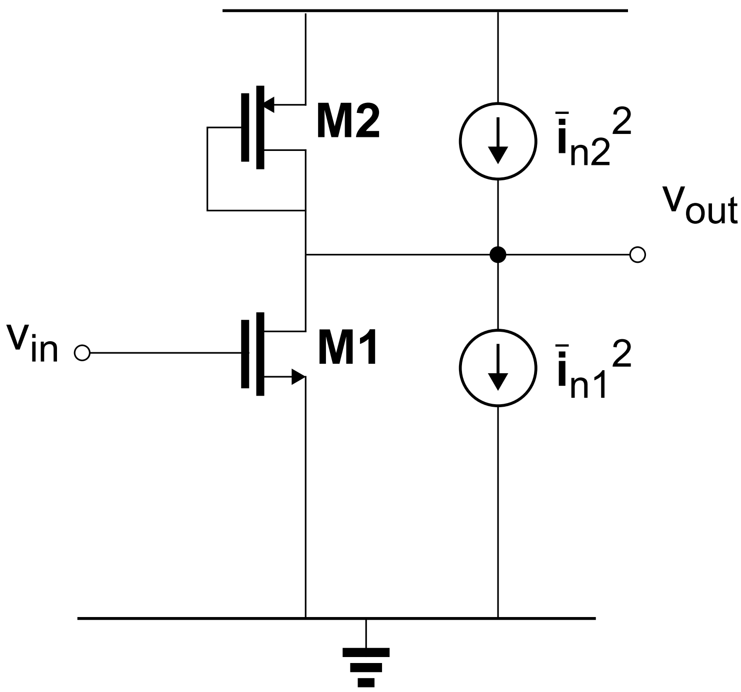
$$g_{m1}v_{in} + g_{m2}v_{out} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \cong -\frac{g_{m1}}{g_{m2}}$$

Alternatively recognise that the current of the current-source $g_{m2}v_{gs2}$ is determined by voltage across its terminals i.e. is equivalent to a resistance $1/g_{m2}$.
Since $1/g_{m2} << 1/g_{ds2}$, $1/g_{m2} << 1/g_{ds1}$, can write directly

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2}}$$

(ii) What is the input-referred thermal noise voltage in terms of the small signal parameters of M1 and M2, Boltzmann's constant k and temperature T?



Total noise current at output is square root of the individual noise currents

$$\overline{i_{nt}} = \sqrt{i_{n1}^2 + i_{n2}^2} = \sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}$$

Input-referred noise voltage density given by

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}}{g_{m1}} \qquad V/\sqrt{Hz}$$

(iii) Calculate the input-referred thermal noise voltage density of the circuit.
For this calculation take $|V_{GS1}| = 1V$, $V_{GS2} = 2.8V$, $V_{tn} = 0.8V$, $V_{tp} = -0.8V$.
The drain current of M1 is 100μA.

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}}{g_{m1}} \qquad V/\sqrt{Hz}$$

g_m given by

$$g_{m1} = \frac{2I_D}{(V_{GS} - V_T)} = \frac{2 \cdot 100\mu A}{1V - 0.8V} = 1mA/V$$

$$g_{m2} = \frac{2 \cdot 100\mu A}{2.8V - 0.8V} = 100\mu A/V$$

Input-referred noise of M1

$$\overline{v_{ni}} = \frac{\sqrt{(4 \cdot 1.38\times10^{-23} \cdot 300)\left(\frac{2}{3}\right)(1mA/V + 100\mu A/V)}}{1mA/V} = \underline{\underline{3.48nV/\sqrt{Hz}}}$$

(iv) Calculate the total noise voltage at the output over a bandwidth of 1MHz.
If the input signal v_{in} is a $1mV_{rms}$ sine wave in this bandwidth, calculate the signal-to-noise ratio in dB at the output over the bandwidth of 1MHz.

Gain of stage

$$Gain = -\left(\frac{g_{m1}}{g_{m2}}\right) = -\frac{1mA/V}{100\mu A/V} = -10$$

Total noise at output given by

$$\overline{v_{notot}} = \overline{v_{nitot}} \cdot \left(\frac{g_{m1}}{g_{m2}}\right) \cdot \sqrt{BW} = 4.15nV/\sqrt{Hz} \cdot 10 \cdot \sqrt{1MHz} = \underline{\underline{34.8\mu V_{rms}}}$$

Output signal

$$v_{out} = -\left(\frac{g_{m1}}{g_{m2}}\right)v_{in} = -10 \cdot 1mV_{rms} = 10mV_{rms}$$

Signal-to-Noise ratio given by

$$\frac{S}{N} = \frac{10mV}{34.8\mu V_{rms}} = 287 \qquad \underline{\underline{\text{or } 49.2\text{ dB}}}$$