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THE NATIONAL UNIVERSITY OF IRELAND, CORK

COLÁISTE NA hOLLSCOILE, CORCAIGH
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SAMPLE PAPER – MARCH 2004

B. E. (ELECTRICAL & ELECTRONIC)
B.E. (MICROELECTRONIC)
M.ENG.SC. (MICROELECTRONIC)
H.DIP. (MICROELECTRONIC)

RFIC DESIGN
EE4011

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Time allowed: *3 hours*

Answer *five* questions

All questions carry equal marks.
The use of a Casio fx570w or fx570ms calculator is permitted.
Smith Charts are available on request.

1. (a) Show a small-signal model of a MOS transistor suitable for first-order analysis and from this derive an expression for the cut-off frequency of a MOS transistor. Assume the transistor is biased in saturation and that the current can be approximated by:

$$I_{DS} = \frac{1}{2}\frac{W}{L}\mu C_{OX}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

where the symbols have their usual meaning. Also assume that the only capacitance to be considered is the gate-source capacitance.

[*10 marks*]

(b) A MOS transistor is biased in saturation and configured as a common-source two-port amplifier with the input applied to the gate (port 1) and the output taken from the drain (port 2). Determine the transistor cut-off frequency. Also determine the 4 two-port y-parameters at a frequency of 1GHz. The following bias conditions and device parameters should be used:

$W=10\mu m$, $L=0.25\mu m$, $T_{ox}=4nm$, $\mu=400cm^2/Vs$, $V_{GS}=2.5V$, $V_{TH}=0.5V$, $\lambda=0.1\ V^{-1}$.

[*10 marks*]

2. (a) Derive an expression for the noise figure of a two-port network driven by a source with impedance R_S. Assume that the two-port can be represented by a noiseless two-port with equivalent input-referred noise voltage and current sources.

[*10 marks*]

(b) The equivalent input referred noise voltage and current sources of a bipolar transistor at moderate frequencies are given by:

$$\overline{v^2} = 4kT\left(r_b + \frac{1}{2g_m}\right)\Delta f \quad \overline{i^2} = 2q\frac{I_C}{\beta_f}\Delta f$$

where the symbols have their usual meaning and r_b is the parasitic base resistance.

A BJT is biased in the forward active region with a collector current, I_C=1mA at 300K. It has a forward active current gain of 100 and a parasitic base resistance of 50Ω. Determine the noise figure for a bandwidth of 1Hz if it is driven by a source with the following impedances: (i) 10Ω, (ii)100Ω, (iii)1000Ω.

Make a rough estimate of the optimum source impedance to give the lowest noise figure.

[*10 marks*]

3. (a) Determine an expression for the 1dB compression point (P1dB) of an amplifier which can be described by the following equation:

$$y(t) = \alpha_1 x(t) + \alpha_3 x^3(t)$$

where x(t) and y(t) are the amplifier input and output waveforms respectively.

[*10 marks*]

(b) For the amplifier described in part (a), determine the input amplitude corresponding to the 1dB compression point if α_1=10 and α_2=0.1.

[*5 marks*]

(c) An RF amplifier is supplied with ~~an~~ two input signals with power of 0dBm. The output power at the fundamental frequency is 20dBm and the output power ~~at the third harmonic~~ of the 3rd order IM is –10dBm. Determine by graphical means or otherwise the input third-order intercept point (input IP3).

[*5 marks*]

4. Outline the design procedure used when designing a microwave amplifier for maximum gain.

[*8 marks*]

A microwave junction transistor has the following characteristics (at 5 GHz with 50 ohm reference);

$$S_{11} = 0.5 \angle -145°$$
$$S_{12} = 0.05 \angle 25°$$
$$S_{21} = 2.75 \angle 190°$$
$$S_{22} = 0.5 \angle -40°$$

Check the stability of the device and design input and output matching networks for maximum power gain.

[*12 marks*]

5. (a) What do you understand by the "unilateral figure of merit" of a high-frequency amplifier?

[*8 marks*]

(b) Discuss the issue of "image frequencies" in RFIC transceiver design and the resulting effects on choice of topology.

[*12 marks*]

6. (a) Illustrate a suitable topology for VCO based on the "negative-g_m" concept using MOSFETs.

[*5 marks*]

(b) An LC-based negative-g_m oscillator uses an on-chip inductor of 3nH and has a parasitic capacitance of 1pF at the output nodes. If a diode with a M_J=0.5 and V_J=0.8V is available, determine which value of the zero-biased capacitance is needed to ensure a minimum oscillation frequency of 1.8GHz from the VCO. Also determine what reverse bias is needed on the diodes if an operation frequency of 2GHz is desired.

[*10 marks*]

(c) Illustrate by means of suitable equations, the characteristic which primarily determines the linearity of the output frequency-control voltage relationship in varactor-diode based VCOs and suggest a diode structure which would give an ideal linear frequency-voltage relationship.

[*5 marks*]

7 (a) Show a block diagram for a Type I Phase Locked Loop (PLL) consisting of a phase detector, a low-pass filter, a voltage controlled oscillator and a feedback divider (M) and from this determine the closed-loop transfer function of the Type I PLL.

[*10 marks*]

(b) Determine the damping-factor and the natural frequency of a Type I PLL with the following characteristics:
K_{VCO}=100MHz/V, K_{PD}=1 V/rad, f_{LPF}=1MHz, M=1000.

[*10 marks*]