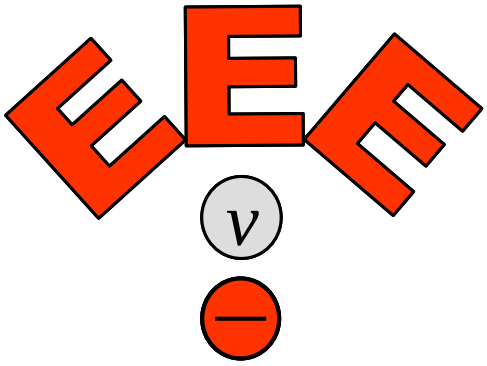

University College Cork

Department of Electrical and Electronic Engineering

Module UE4002 – Analog IC Design

Op-Amp Design Assignment

Student Name: Cian O'Mahony

Student No.: 108444897

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1 Introduction

This assignment required the design of an op-amp circuit with the following specifications:

Table 1.1: Op-Amp Specifications

DC Loop Gain	> 80dB
Phase Margin	> 60°
Gain Bandwidth Product	> 15MHz
Power Dissipation	< 1mW

The external conditions under which the op-amp was to be simulated are as follows:

Table 1.2: Op-Amp External Conditions

Supply Voltage	3.3V
Input Bias Current	100µA
Common-mode Voltage Reference	1.5V
Capacitive Load	10pF
Process	c35b4

The top-level schematic of the design is thus as shown in the figure below:

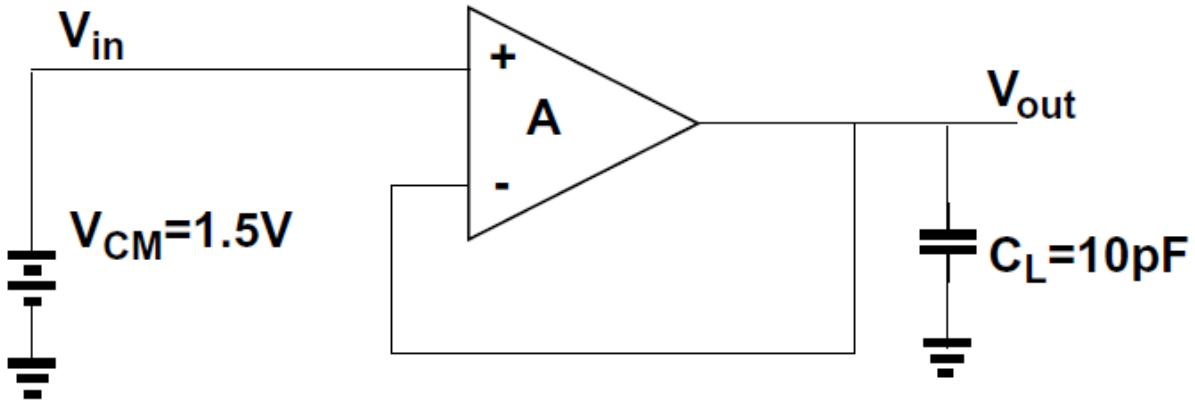

Figure 1.1: Top-level Amplifier Schematic

2 Op-Amp Architecture Description

The open-loop architecture chosen for this design is a two stage operational amplifier shown below in Figure 2.1. A differential amplifier with a diode load (M1-4 and M7) is the first stage, the output of which feeds into a PMOS common source stage (M5 and M6). The bias currents relative to the input bias current $2I_B$ in both stages are determined by the (W/L) ratios of M7 and M6 to the (W/L) ratio of M8.

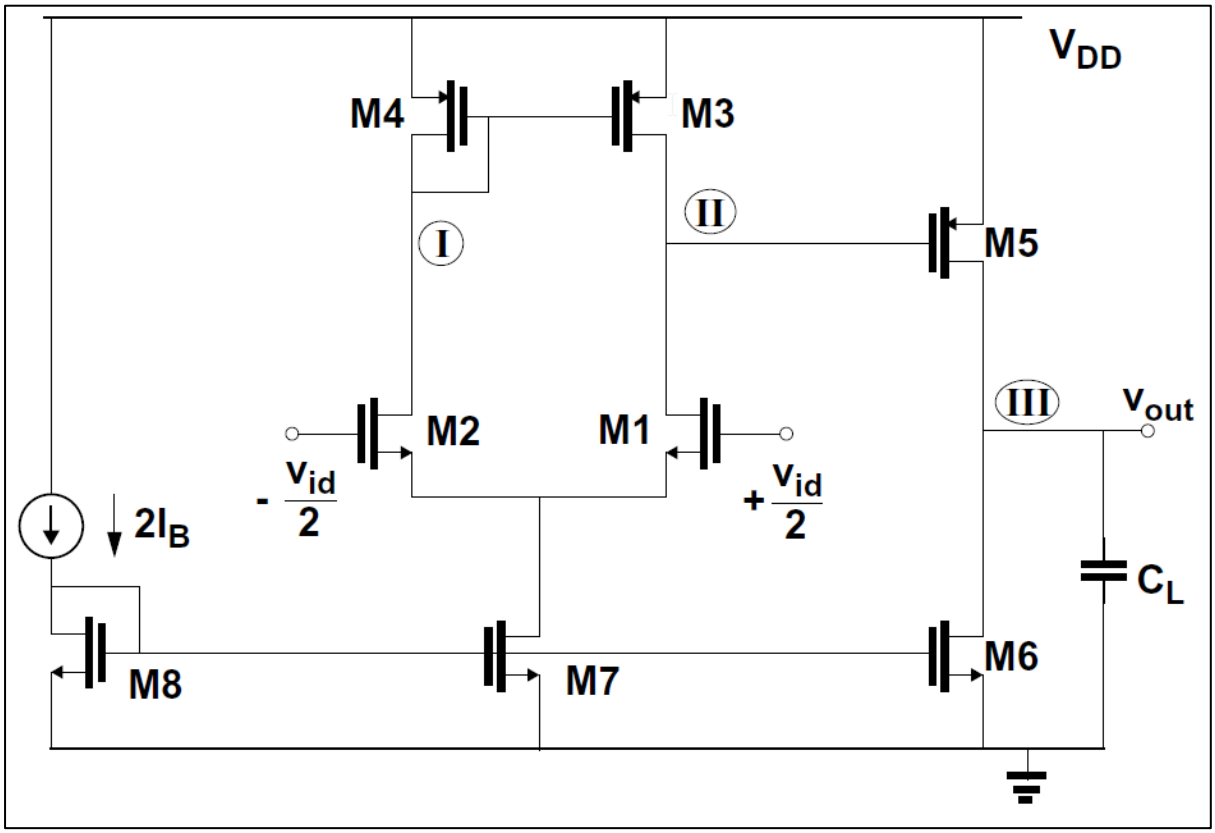

Figure 2.1: Two-stage Op-Amp Architecture

The gain of the first stage in terms of the small-signal parameters (assuming all transistors are operating in saturation) is given by:

$$Gain_1 = \frac{g_{m1}}{g_{ds1} + g_{ds3}}$$

The gain of the common source stage (again assuming both transistors are biased in saturation) is given by:

$$Gain_2 = \frac{g_{m5}}{g_{ds5} + g_{ds6}}$$

Therefore, the total open-loop gain of the op-amp is given by the product of both these terms:

$$Gain_{tot} = Gain_1 * Gain_2 = \frac{g_{m1}}{g_{ds1} + g_{ds3}} . \frac{g_{m5}}{g_{ds5} + g_{ds6}}$$

A frequency compensation element is also added to the circuit by placing a resistor and capacitor in series between the gate and drain of M5 as shown in Figure 2.2 below.

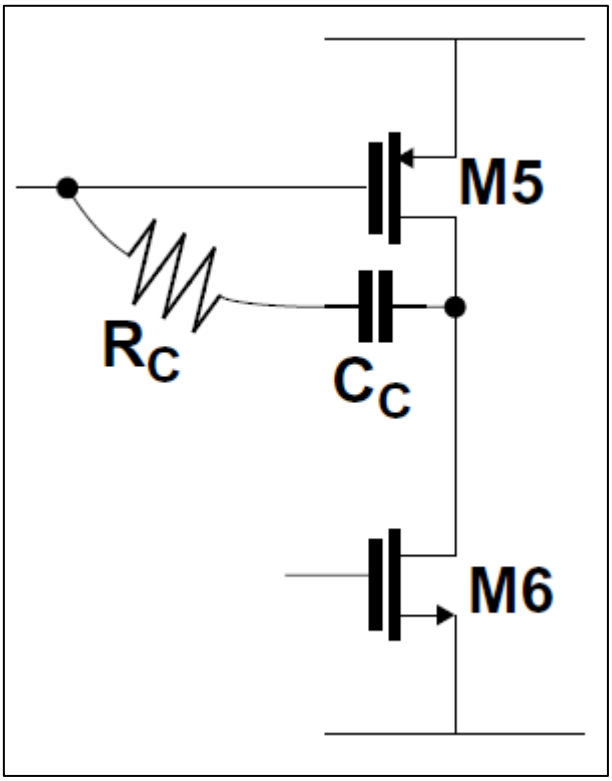

Figure 2.2: Frequency Compensation Components

The capacitor has the effect of splitting the poles of the circuit by reducing the frequency of the first-stage pole and increasing the frequency of the second-stage pole, and so the first pole becomes dominant and the second can be neglected in some of the terms of the transfer function. Just adding a capacitor would however also introduce a zero to the transfer function which ruins the stability of the op-amp. This effect is negated by the addition of the resistor in series which can theoretically push the zero frequency to infinity.

3 Op-Amp Design and Specifications

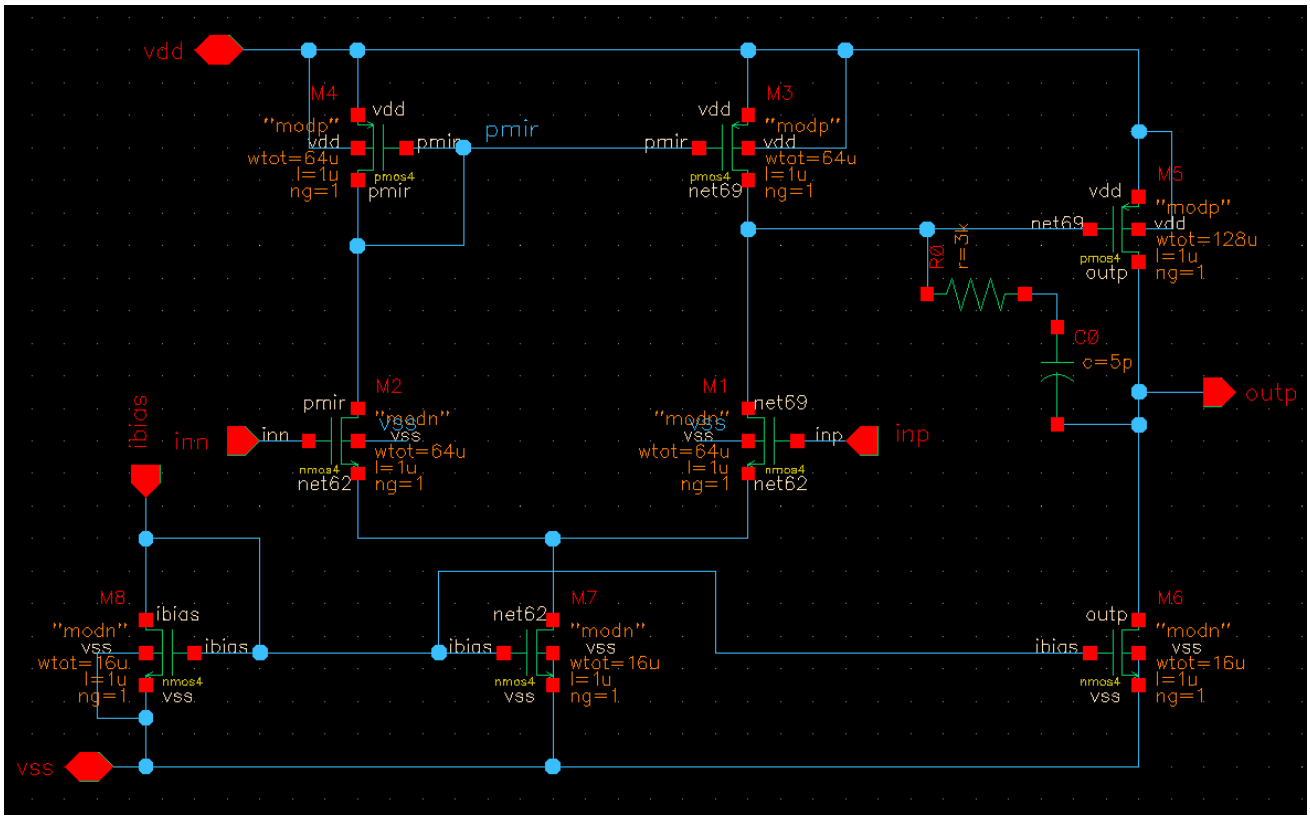

Figure 3.1: Finalised Op-Amp Design

The finalised design for the op-amp is shown above. The external bias current input to the op-amp is specified in the assignment as being 100µA. With a 3.3V supply voltage also specified along with a maximum power of 1mW, this limits the total current allowed to flow in the circuit to ~300µA. Hence, the (W/L) values of both M7 and M6 were set to be the same as M8 (16/1) to ensure that 100µA flowed in each of the three branches of the circuit.

By experimenting with the values of the compensation resistor and capacitor, the best results were observed with R=3kΩ and C=5pF.

The final specifications of the op-amp are recorded in Table 3.1 below:

Table 3.1: Op-Amp Design Characteristics

Power	1mW
DC Gain	90.94dB
Phase Margin	72.05°
Gain Bandwidth Product	24.23MHz
3dB Frequency	687.2Hz
Overshoot	0.78%

An interesting observation from the design is that a power saving of approximately 33% can be obtained from the design if the (W/L) ratios of M7 and M6 are halved, while the other

device specifications are still acceptable, with only the Gain Bandwidth product (marginally) failing to meet the requirements. This would be useful in such applications where minimising the power dissipation is more important than maximising specifications. When this is done for the above design the following specifications result:

Power	0.66mW
DC Gain	93.88dB
Phase Margin	60.94°
Gain Bandwidth Product	14.57MHz
3dB Frequency	249.9Hz
Overshoot	2.792%

4 Testbenches

The testbenches used to simulate the op-amp design are shown below. The frequency plots and step response of the system are shown on the following page.

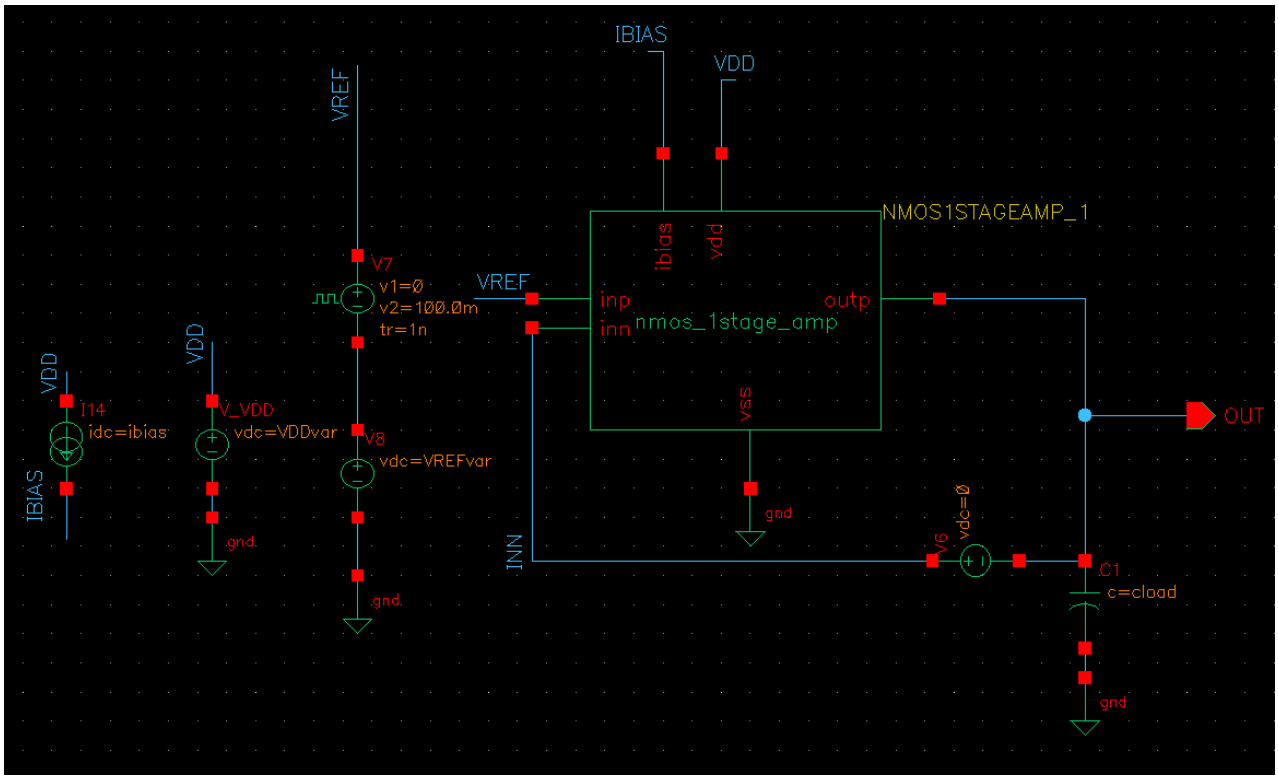

Figure 4.1: AC Simulation Testbench

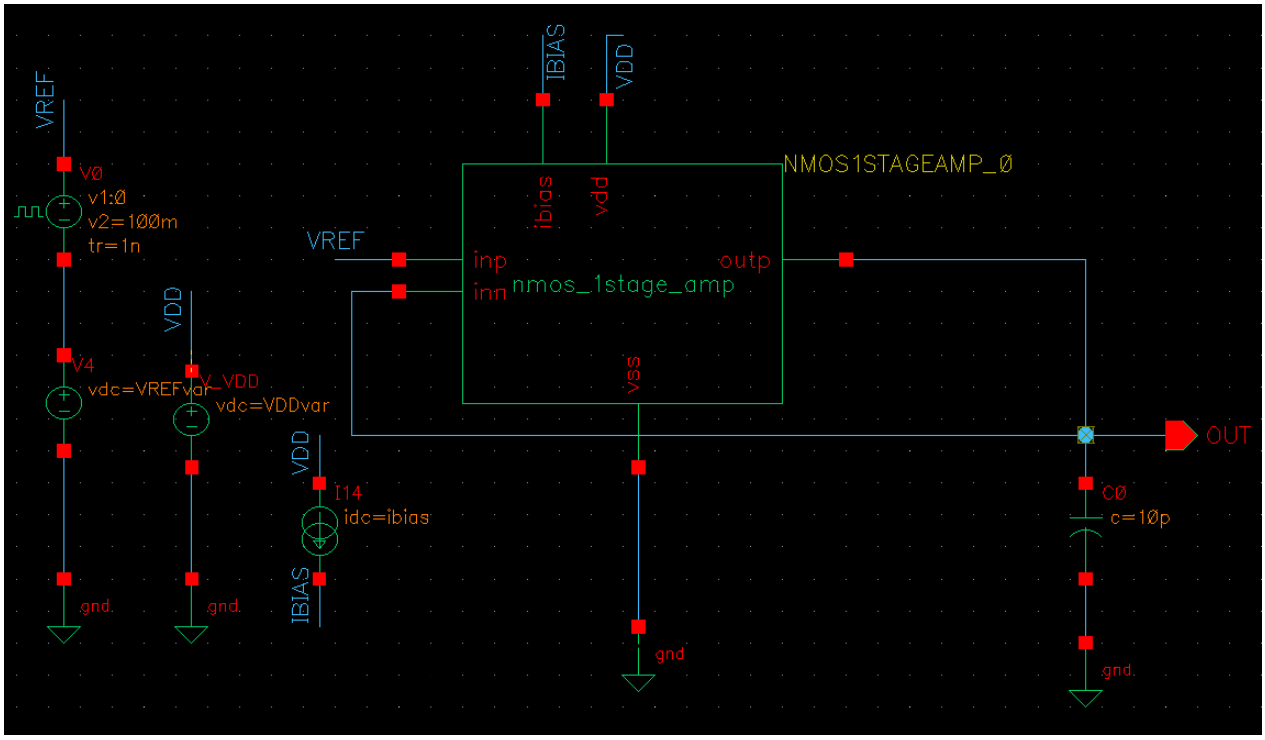

Figure 4.2: Transient Stability Testbench

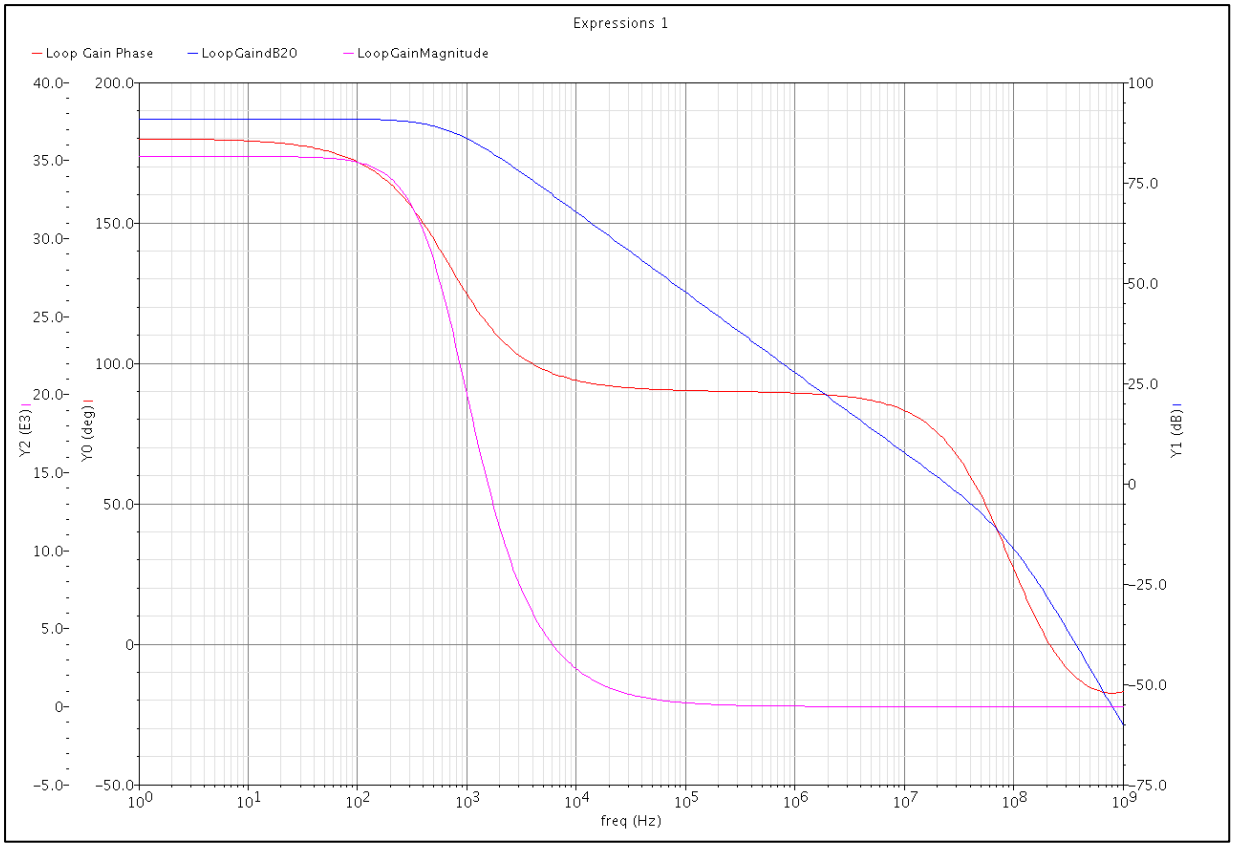

Figure 4.3: Phase Margin and Gain vs. Frequency Plots

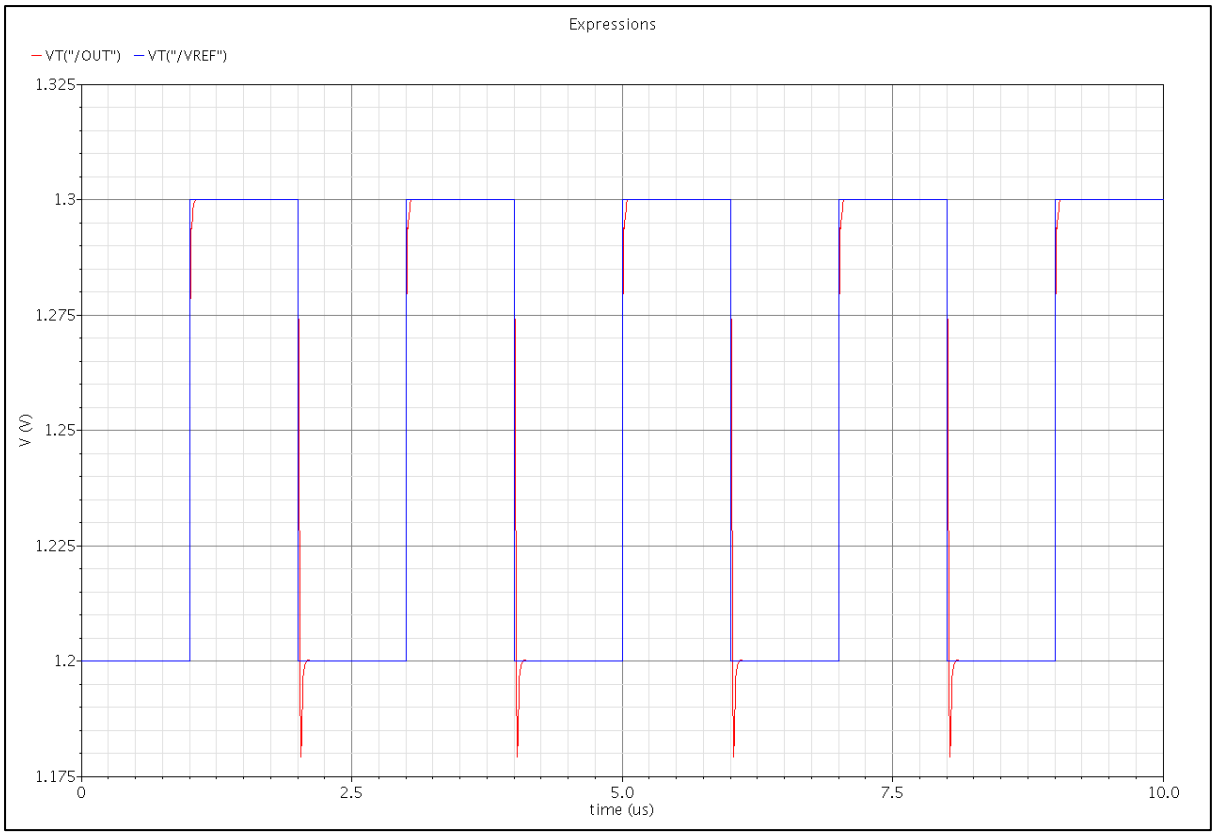

Figure 4.4: Op-Amp Step Response

5 Conclusion

A two-stage operational amplifier has been designed exceeding each of the minimum specified criteria in the assignment. The design was simulated in Cadence with frequency and step responses plotted and included in this report. The use of a capacitor and resistor for frequency compensation to control the placement of the dominant pole was also included in the design to improve the basic performance of the two-stage amplifier.