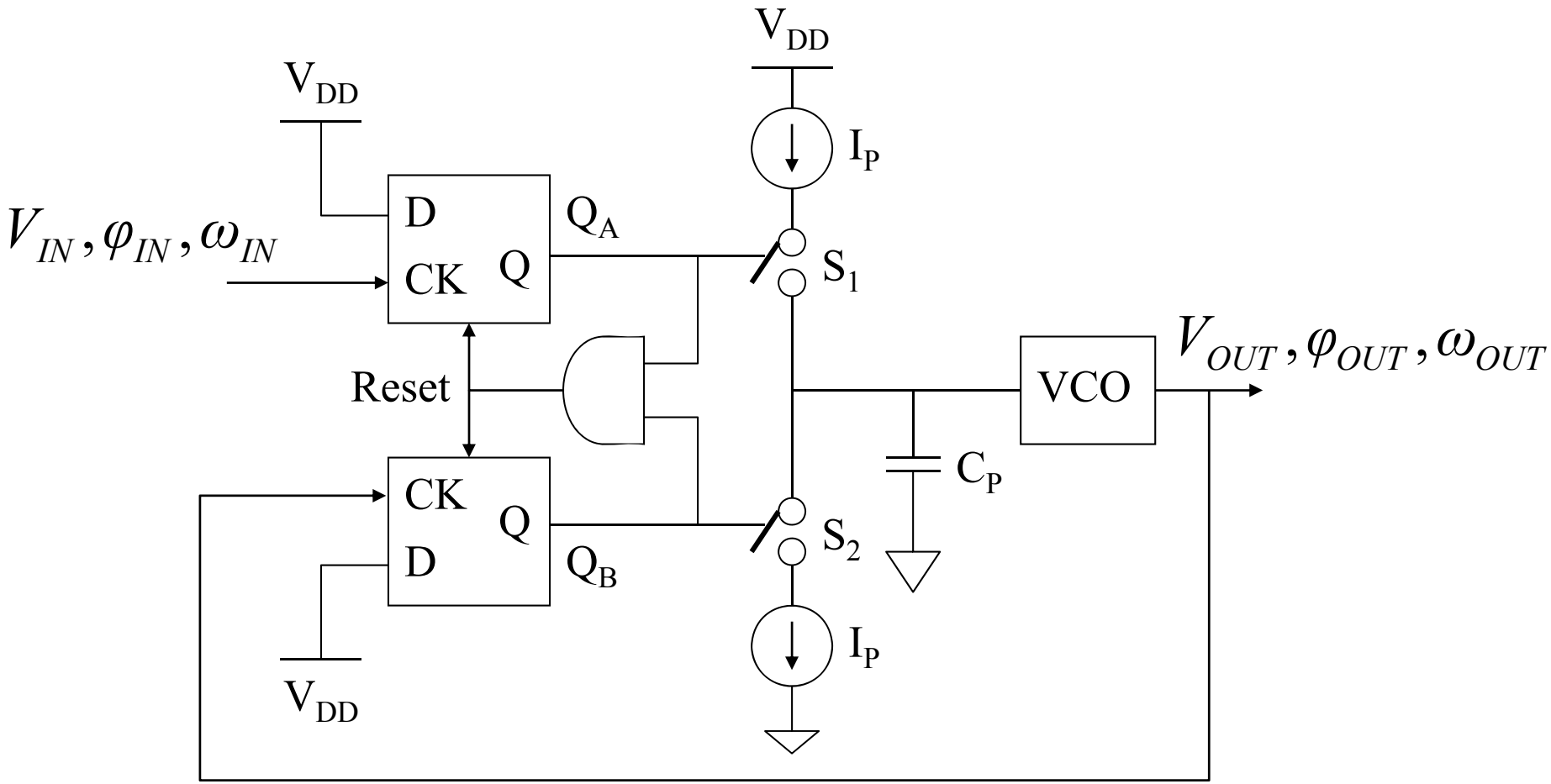
EE4011: RF IC Design

Type II PLLs and Charge Pump Phase Detectors

Type II PLLs

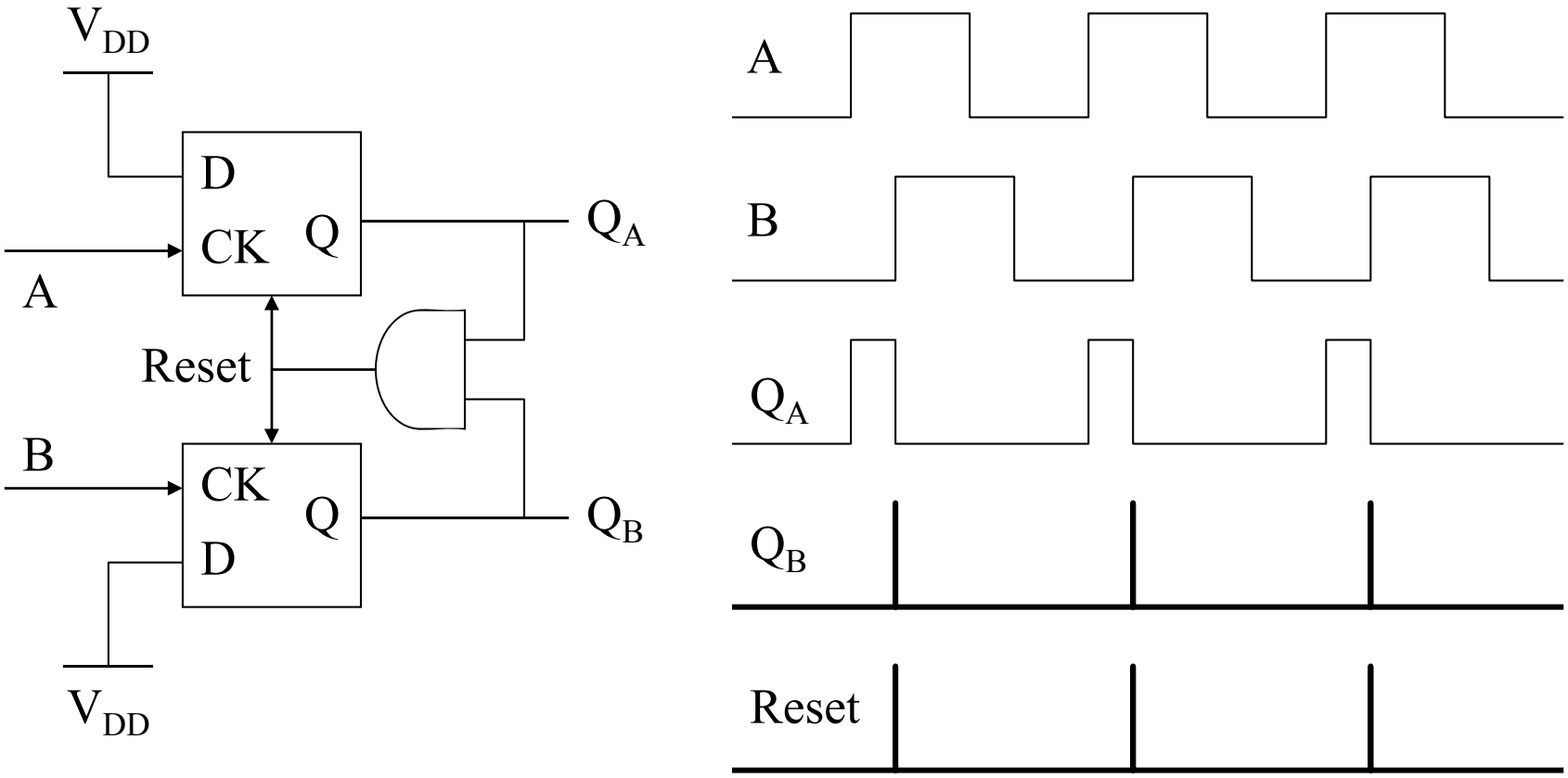
An architecture which overcomes some of the limitations of the Type I PLL is the Phase-Frequency-Detector (PFD)/Charge-Pump PLL (CPPLL):



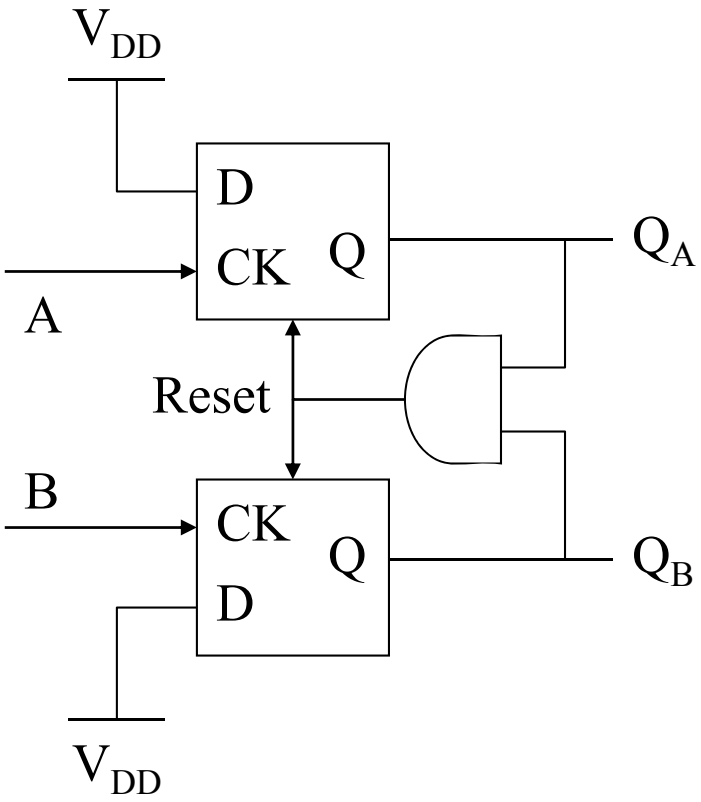
Operation of PFD for same i/p Frequency

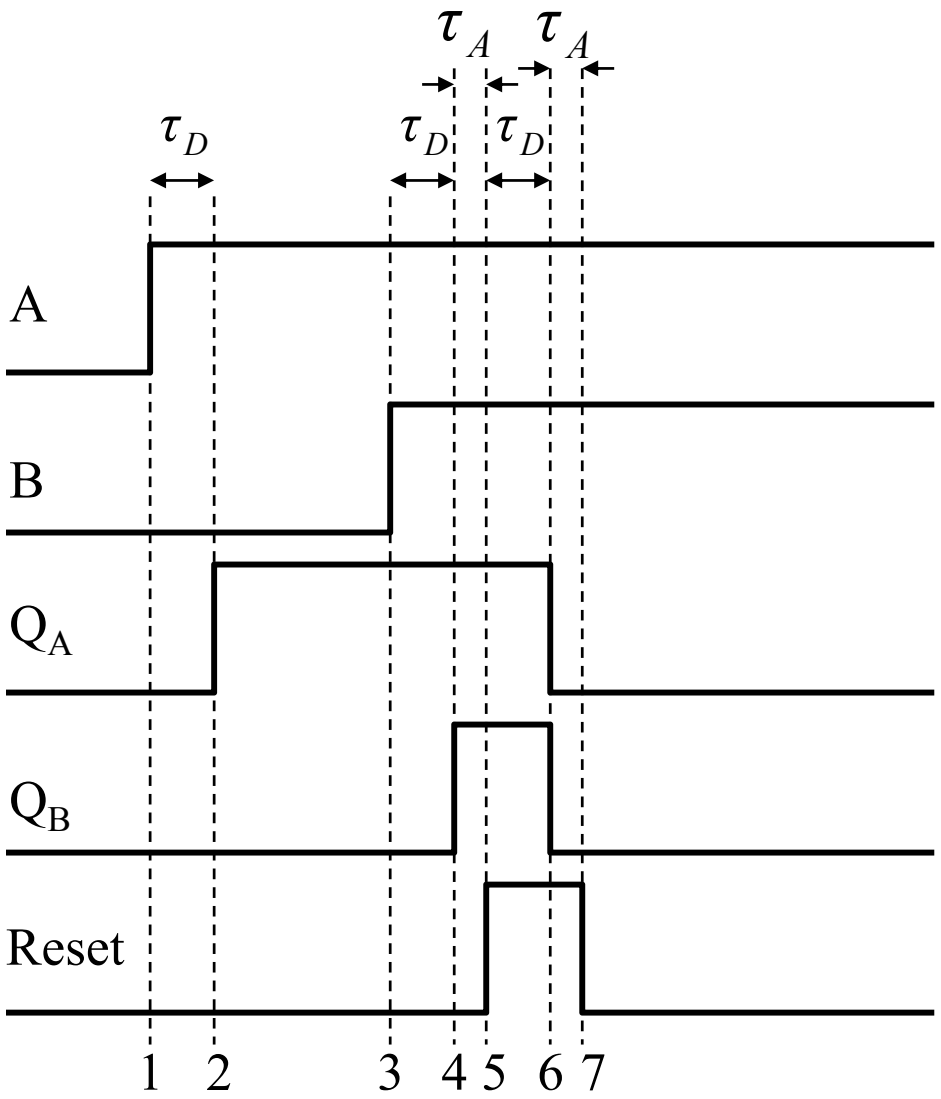
The PFD based on two D-type flip flops and an AND gate generate outputs whose mark/space ratio depends on the difference in frequency and phase of the two input signals.

Example where the inputs at A and B are the same frequency but A *leads* B:



Zoom-in to show pulse timing - 1

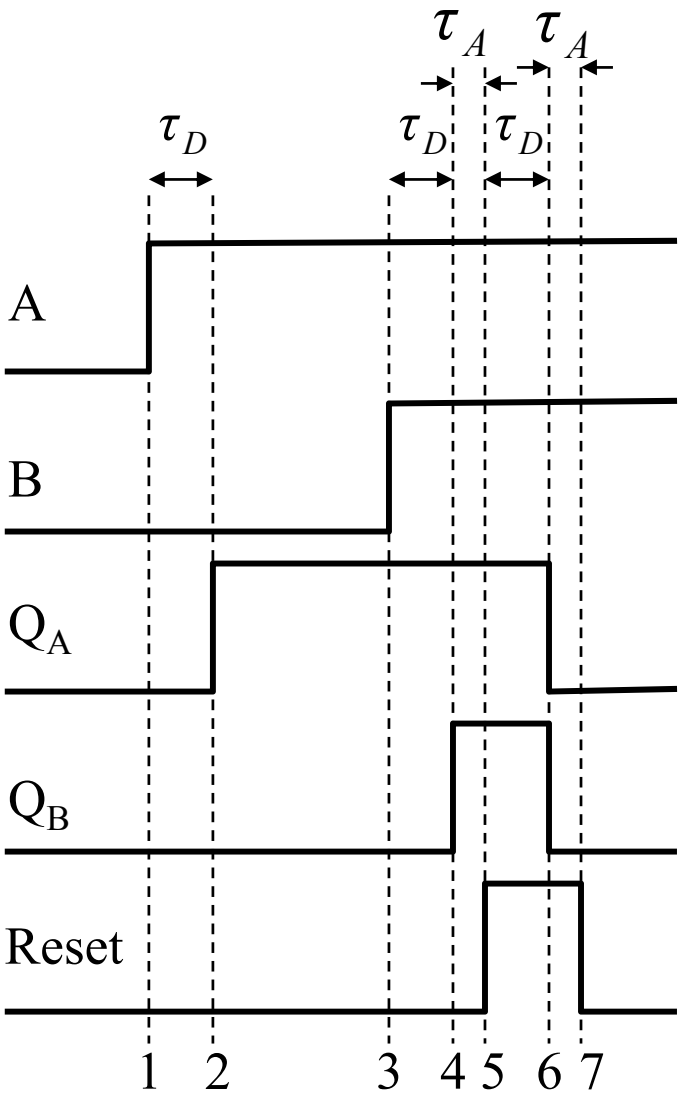




τ_D is the propagation delay through the D-type flip-flop

τ_A is the propagation delay through the AND gate

Zoom-in to show pulse timing - 2

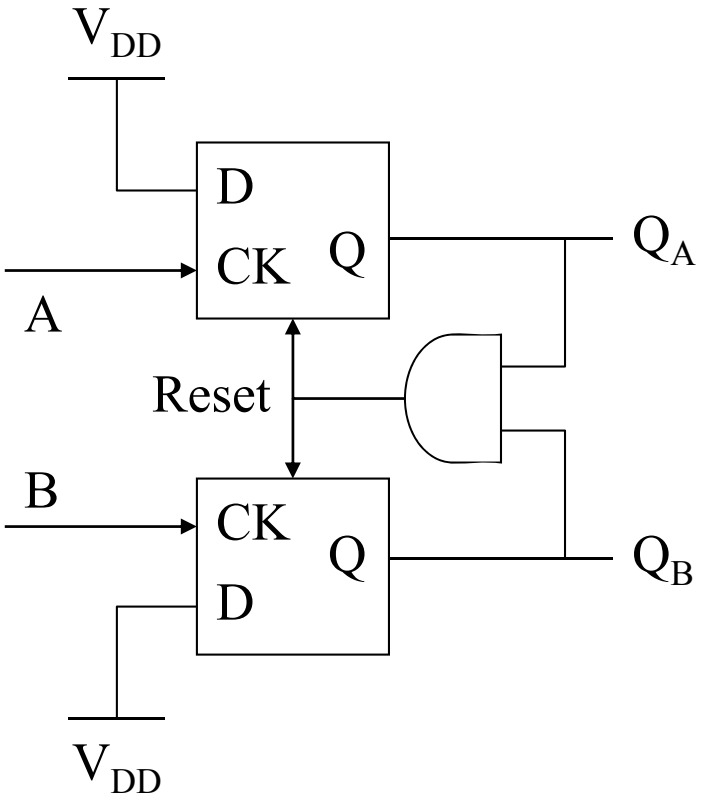


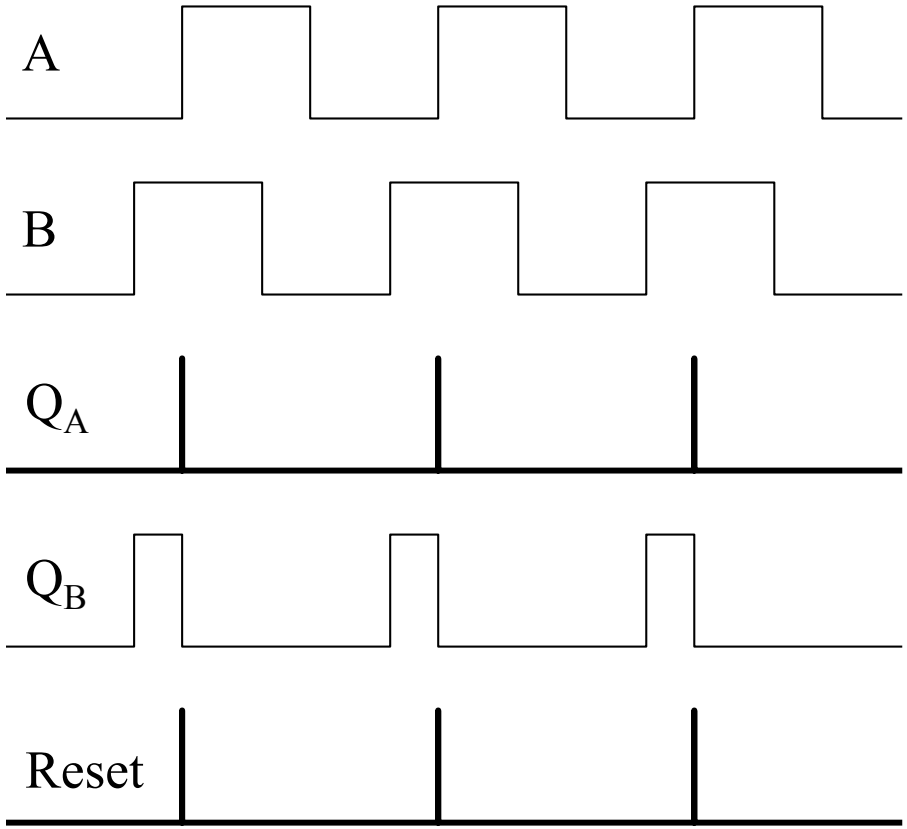
1. Input A goes high.
2. Signal A propagates through the D latch and the output Q_A goes high.
3. Input B goes high.
4. Signal B propagates through the D latch and the output Q_B goes high.
5. As Q_A is already high, Q_B propagates through the AND gate causing its output (Reset) to go high.
6. The reset signal propagates through both latches and Q_A and Q_B go low.
7. Q_A and Q_B propagate through the AND gate so its output (Reset) goes low.

Q_A is a wide pulse determined by the phase difference between A and B. Q_B and Reset are narrow pulses determined by the propagation delays through the gates.

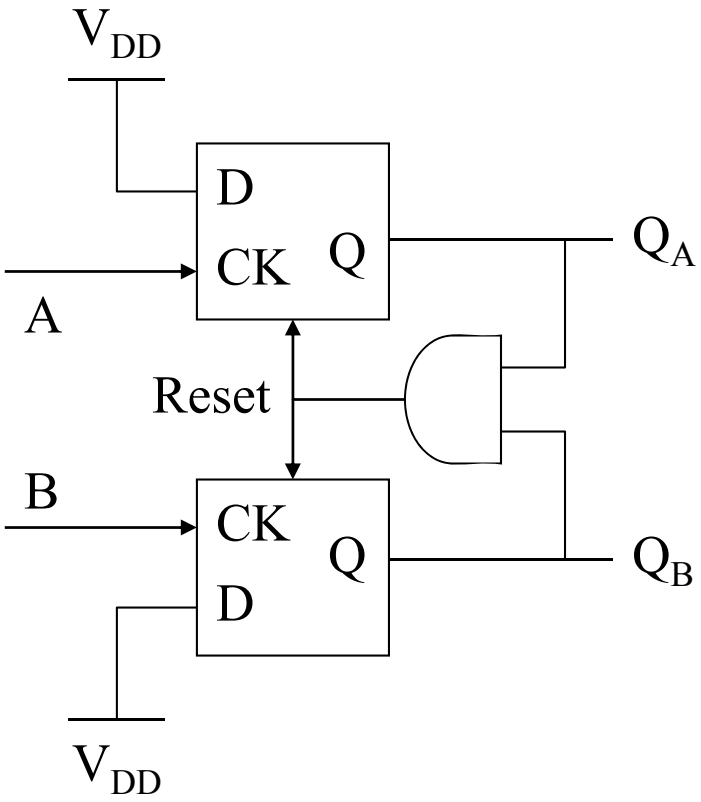
Operation of PFD for same i/p Frequency

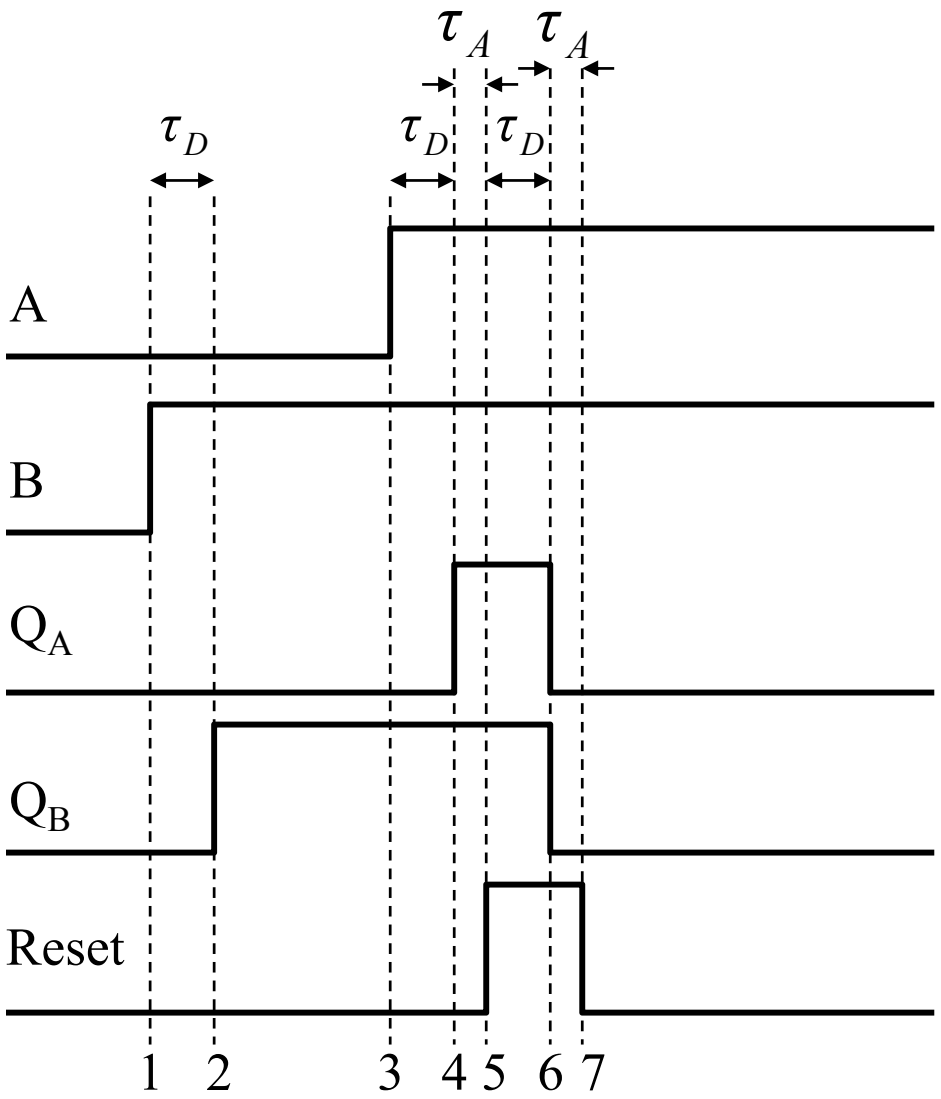
Case where the inputs at A and B are the same frequencies but B *leads* A.





Zoom-in to show pulse timing - 3



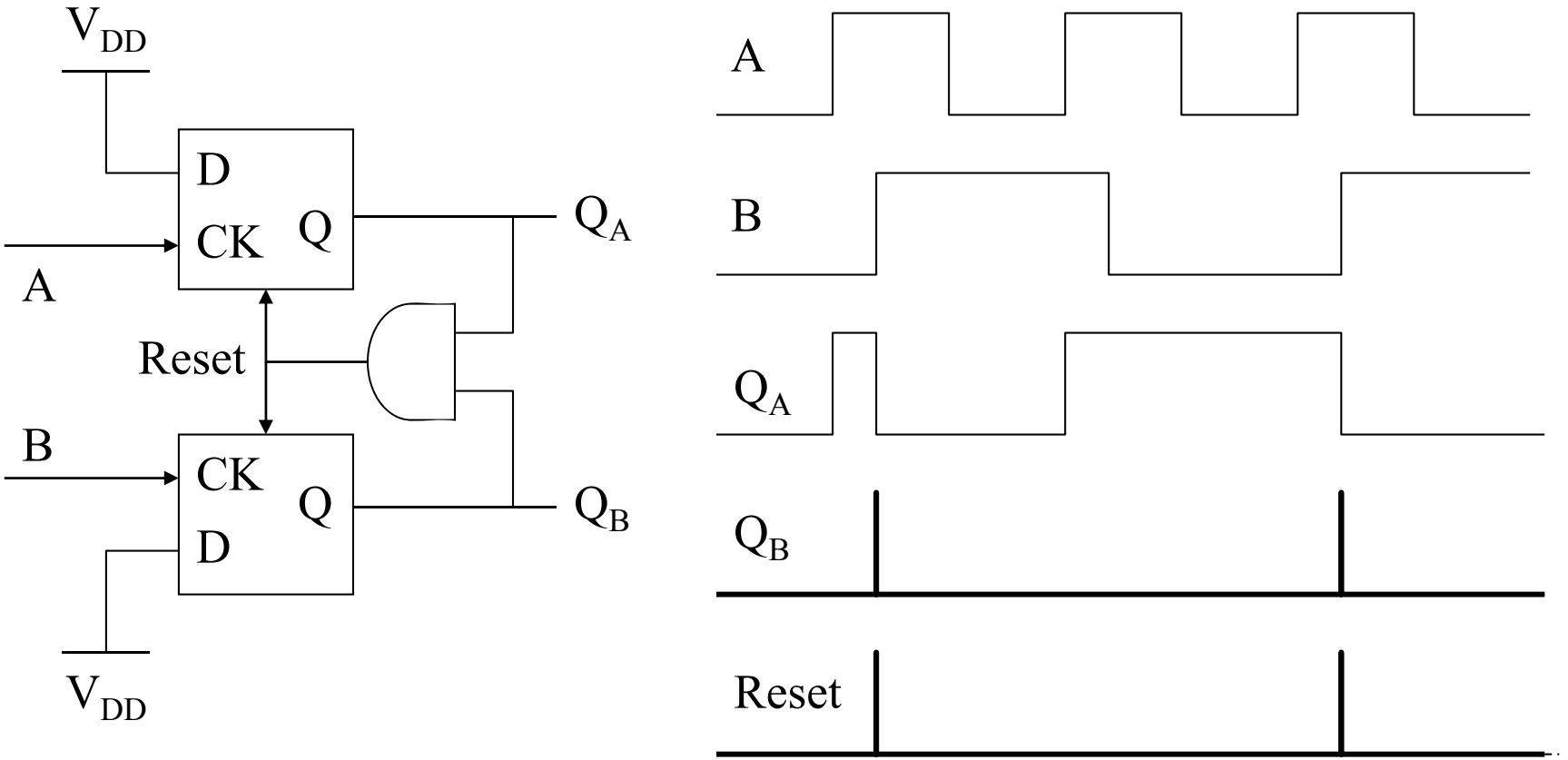


τ_D is the propagation delay through the D-type flip-flop

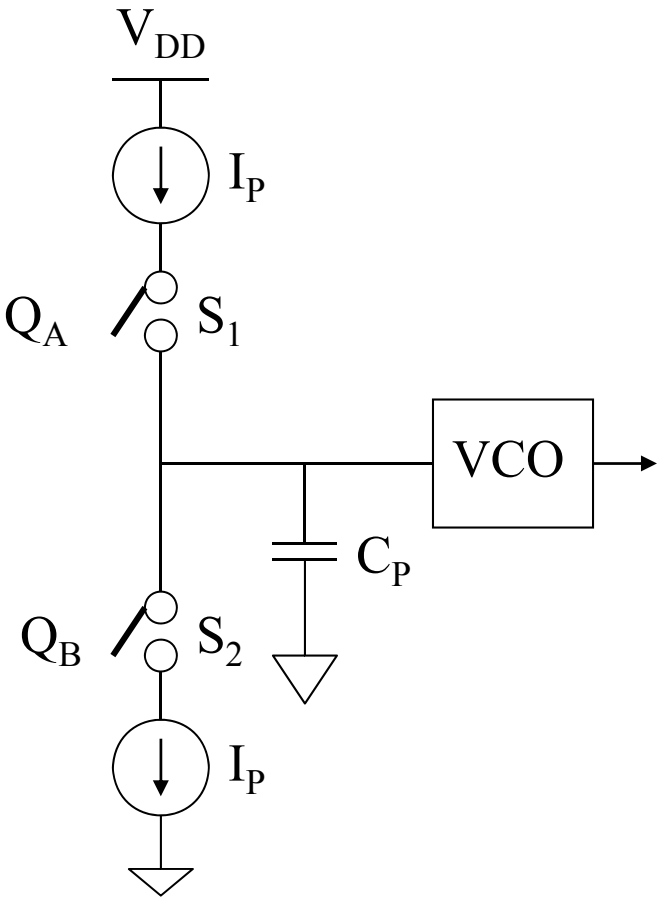
τ_A is the propagation delay through the AND gate

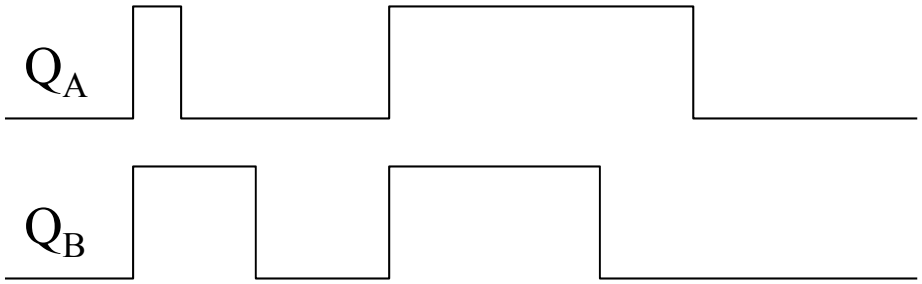
Operation of PFD for different i/p frequencies

Case where input A is twice the frequency of B. There are very wide pulses on Q_A which will cause the charge pump capacitor to charge quickly.



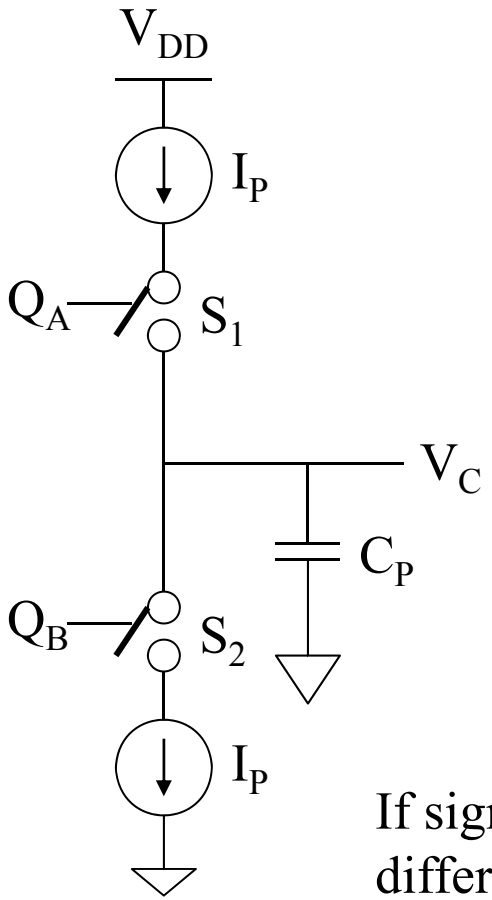
The Charge Pump

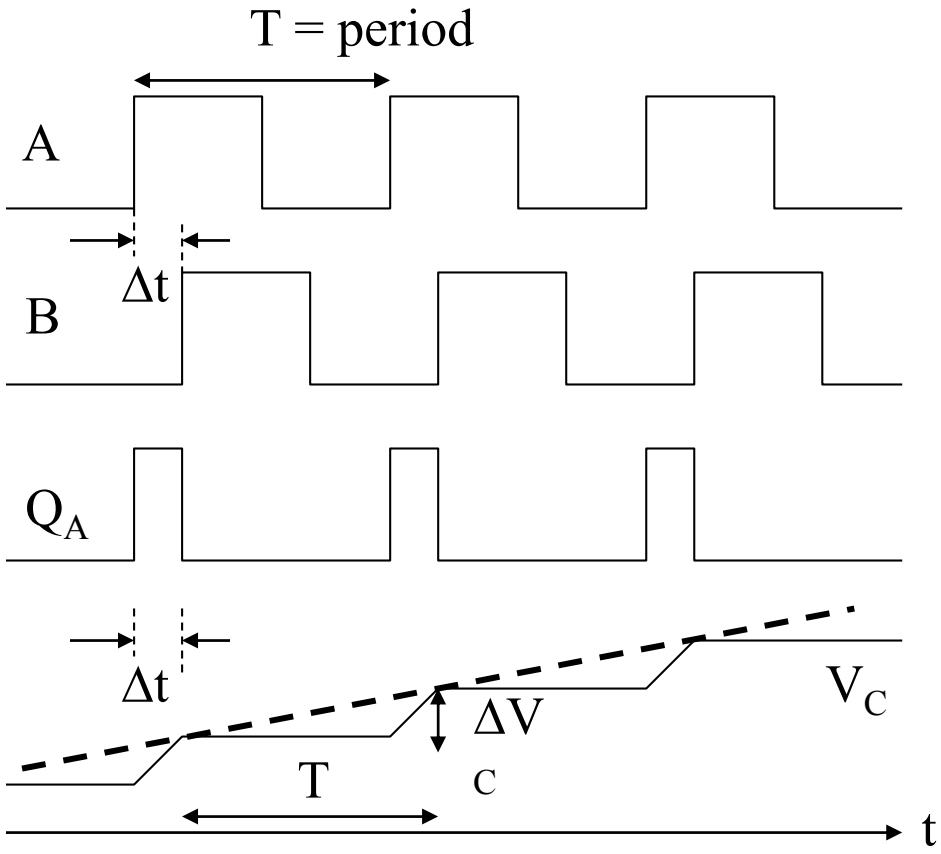




S_1 and S_2 are CMOS switches (or just single MOSFETs) driven by the logic signals Q_A and Q_B. When Q_A is high S_1 is closed and the capacitor is charged with current I_P causing its voltage to rise and thus the VCO frequency to increase. When Q_B is high, S_2 is closed and the capacitor is discharged with current I_P causing its voltage to drop and the VCO frequency to decrease.

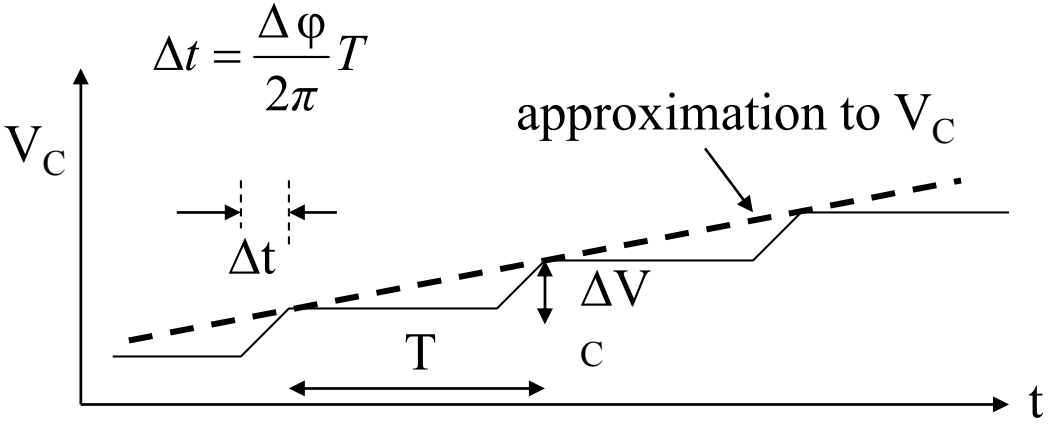
Model of Simplest PFD/CP - 1





If signals A and B have the same frequency but a phase difference $\Delta\phi$ then the time between their rising edges is $\Delta t=(\Delta\phi/2\pi)T$. During this time interval switch S_1 is on and the capacitor is charged with current I_P.

Model of Simplest PFD/CP - 2



During the interval Δt the capacitor is charged with current I_P giving a voltage rise rate of I_P/C_P V/s. The total voltage rise in this interval is:

$$\Delta V_C = \frac{I_P}{C_P}\Delta t = \frac{I_P}{C_P}\frac{\Delta\varphi}{2\pi}T$$

During the remainder of the period of A the switches are turned off and the voltage on the capacitor remains constant. Thus on average, the voltage rises by ΔV_C in one period, T. The behaviour can be approximated by a straight line:

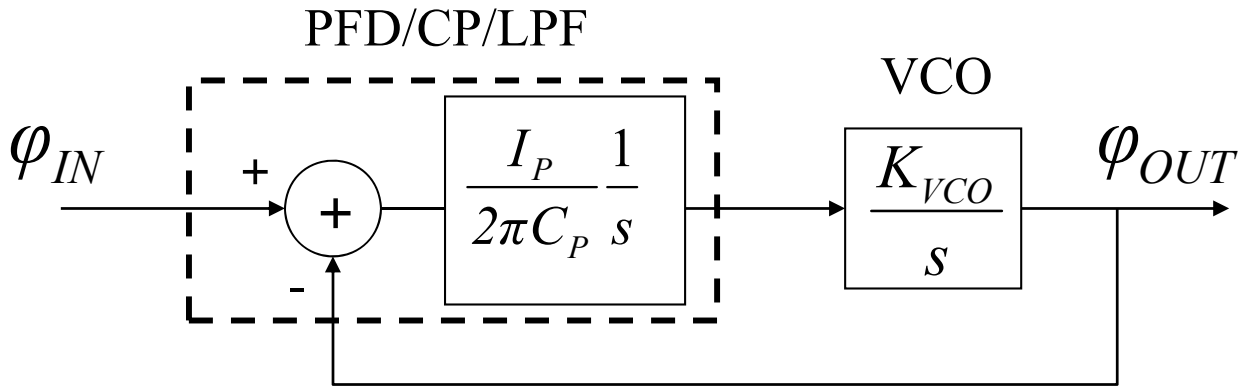
$$slope = \frac{dV_C}{dt} \approx \frac{\Delta V_C}{T} = \frac{I_P}{C_P}\frac{\Delta\varphi}{2\pi}T\frac{1}{T} = \frac{I_P}{2\pi C_P}\Delta\varphi$$

$$\Rightarrow \frac{dV_C}{dt} = \frac{I_P}{2\pi C_P}\Delta\varphi \Rightarrow V_C = \frac{I_P}{2\pi C_P}\int \Delta\varphi$$

$$\Rightarrow V_C(s) = \frac{I_P}{2\pi C_P}\frac{1}{s}\Delta\varphi(s)$$

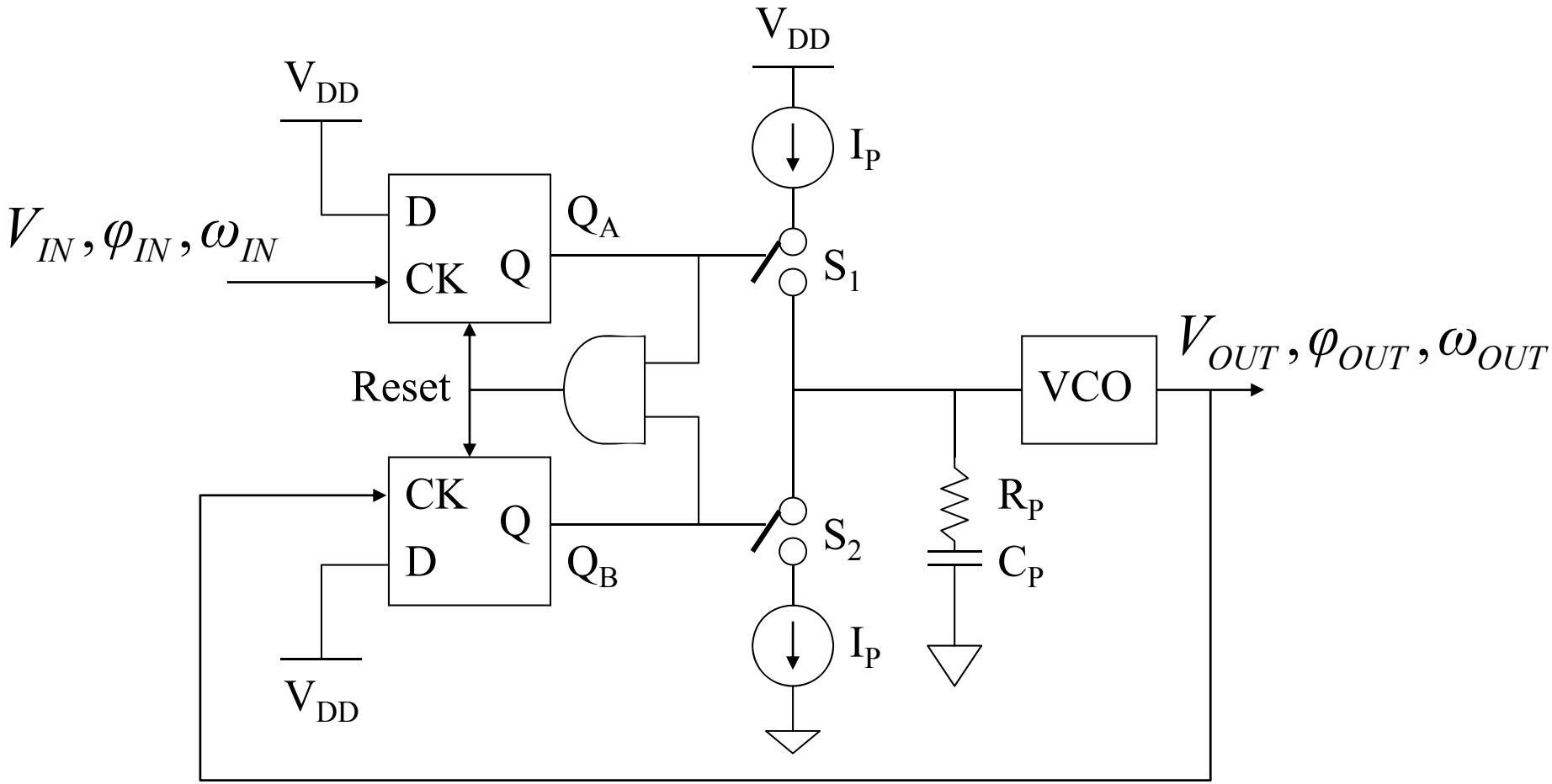
Simplest Type II PLL

The configuration seen so far can be represented by the following blocks:

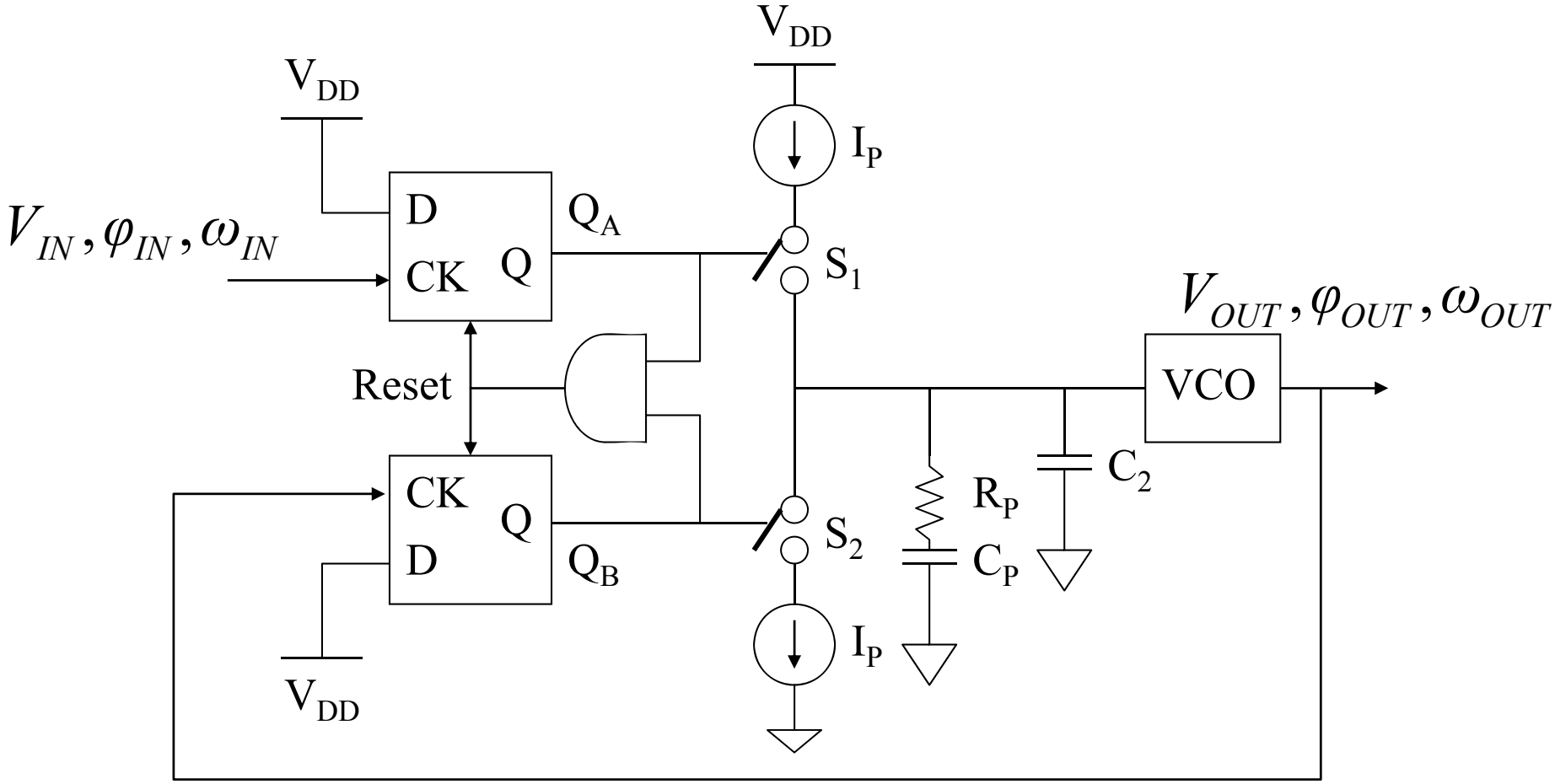


Unfortunately, the closed-loop transfer function of this system has two imaginary poles and can be unstable. To avoid stability problems, a zero is added to the open loop transfer function by placing a resistor in series with the charge pump capacitor. An extra smoothing capacitor is often used to smooth out the rapid voltage steps which would occur from a capacitor being charged through a resistor by means of a switch which is opening and closing. All this makes the analysis of the system more difficult but a linear model can be created by using an “average current” approach.

Type II PLL with added zero



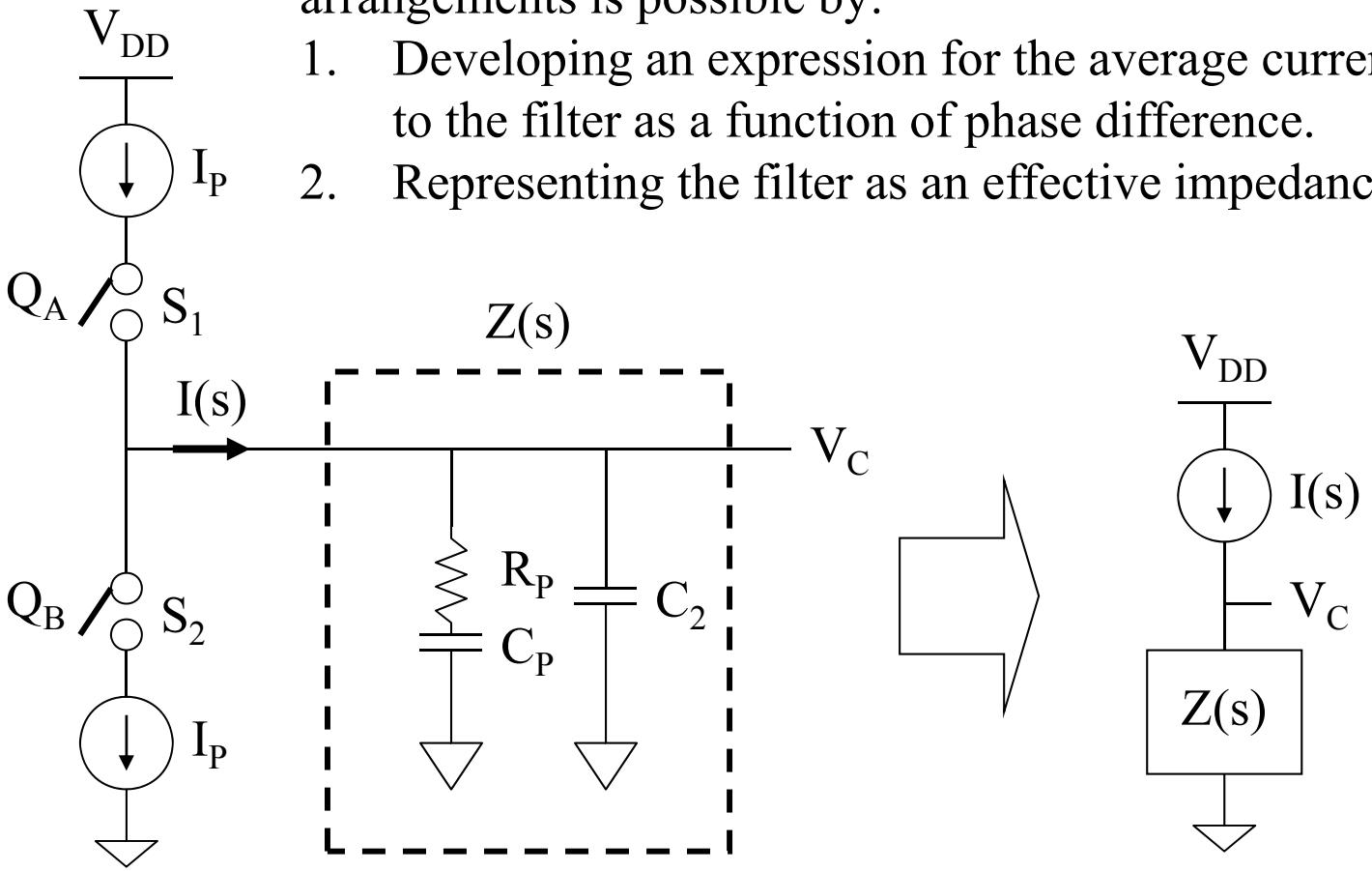
Type II PLL with added zero and smoothing capacitor



A Linear Model of the CPPLL

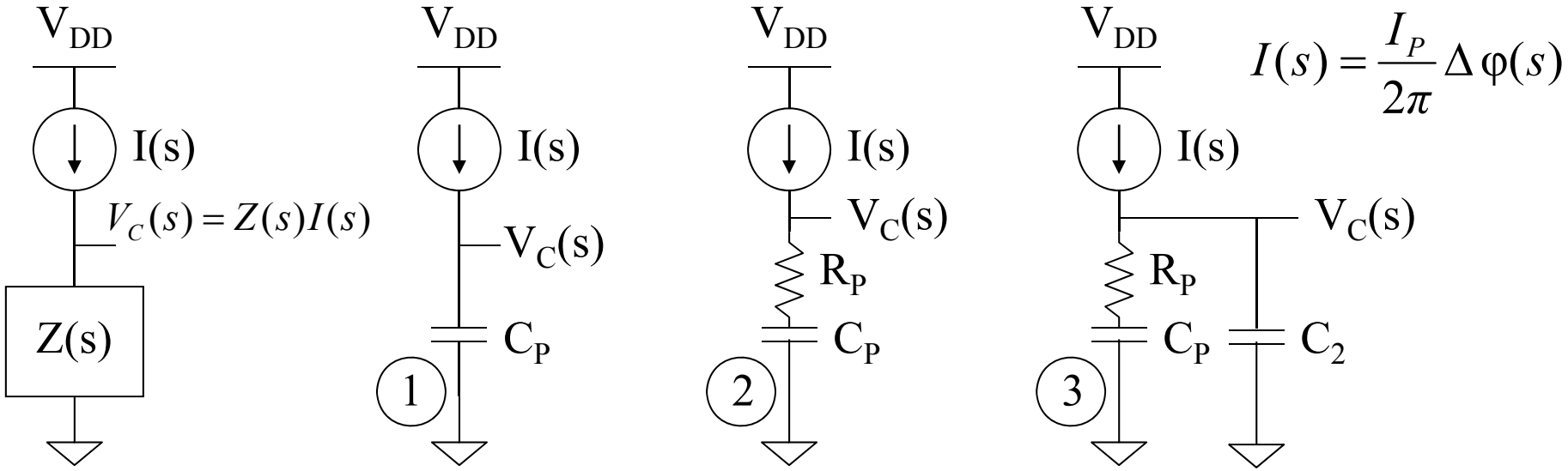
Linear modelling of more complicated charge pump filter arrangements is possible by:

1. Developing an expression for the average current supplied to the filter as a function of phase difference.
2. Representing the filter as an effective impedance.



Treating the capacitor/filter as an impedance

With the average current I(s) known, the capacitor/resistor combination can be treated as an impedance and the voltage determined from Ohm's law.



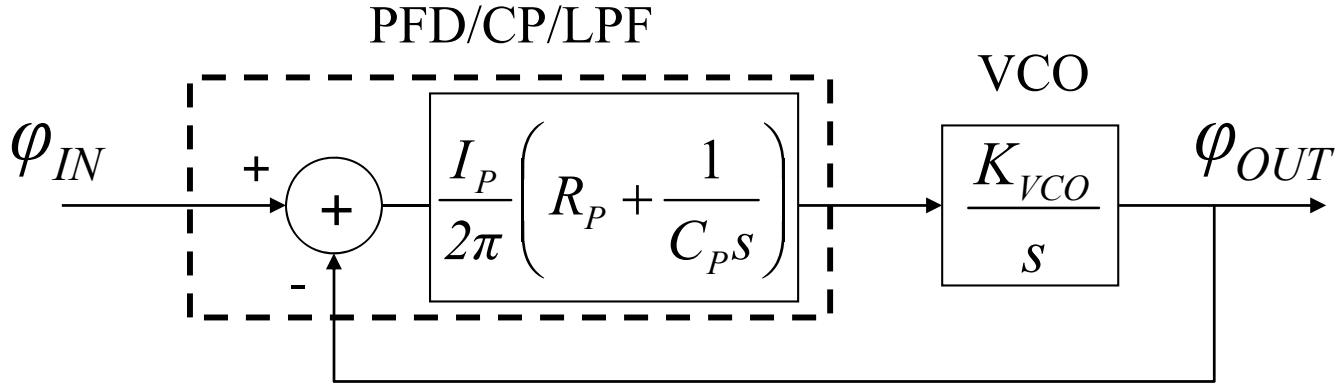
$$I(s) = \frac{I_P}{2\pi}\Delta\varphi(s)$$

(1) $$Z(s) = \frac{1}{sC_P} \Rightarrow V_C(s) = \frac{1}{sC_P} I(s) = \frac{I_P}{2\pi C_P}\frac{\Delta\varphi(s)}{s}$$

(2) $$Z(s) = R_P + \frac{1}{sC_P} \Rightarrow V_C(s) = \left(R_P + \frac{1}{sC_P}\right) I(s) = \frac{I_P}{2\pi}\left(R_P + \frac{1}{sC_P}\right)\Delta\varphi(s)$$

(3) $$Z(s) = \left(R_P + \frac{1}{sC_P}\right) \| \left(\frac{1}{sC_2}\right) \Rightarrow V_C(s) = \frac{I_P}{2\pi}\left(\frac{R_P C_P s + 1}{\left(R_P C_P C_2 s + C_P + C_2\right)s}\right)\Delta\varphi(s)$$

PFD/CP PLL with C_P/R_P - 1



Open loop transfer function:

$$H(s)=\frac{\varphi_{OUT}(s)}{\varphi_{IN}(s)}=\frac{I_P K_{VCO}}{2\pi s}\left(R_P+\frac{1}{C_P s}\right)$$

Closed loop:

$$H_{Closed}(s)=\frac{H(s)}{1+H(s)}$$

$$=\frac{\frac{I_P K_{VCO}}{2\pi s}\left(R_P+\frac{1}{C_P s}\right)}{1+\frac{I_P K_{VCO}}{2\pi s}\left(R_P+\frac{1}{C_P s}\right)}=\frac{\frac{I_P K_{VCO}}{2\pi C_P}\left(R_P C_P s+1\right)}{s^2+\frac{I_P K_{VCO}}{2\pi}R_P s+\frac{I_P K_{VCO}}{2\pi C_P}}$$

PFD/CP PLL with C_P/R_P - 2

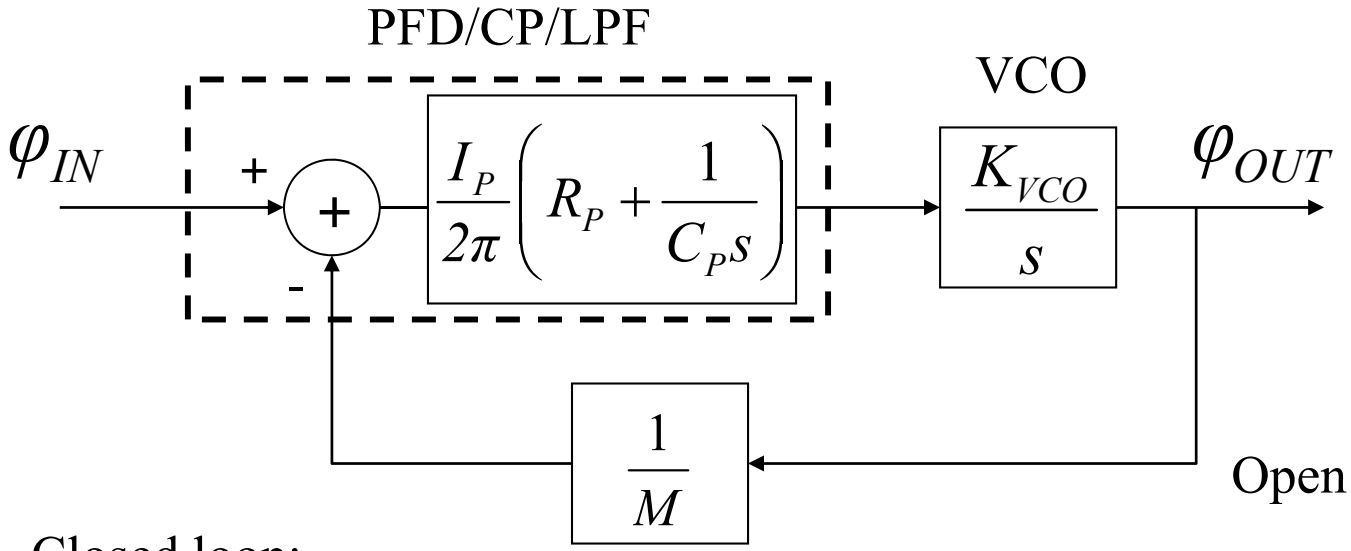
$$H_{Closed}(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}\left(R_P C_P s + 1\right)}{s^2 + \frac{I_P K_{VCO}}{2\pi} R_P s + \frac{I_P K_{VCO}}{2\pi C_P}} = \frac{\frac{I_P K_{VCO}}{2\pi C_P}\left(R_P C_P s + 1\right)}{s^2 + 2\varsigma\omega_n s + \omega_n^2}$$

$$\Rightarrow \omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P}} \quad \varsigma = \frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi}} \quad \tau = \frac{1}{\varsigma\omega_n} = \frac{4\pi}{I_P R_P K_{VCO}}$$

The denominator has been arranged to show up the 2nd-order system characteristics such as the natural frequency, the damping factor and the time-constant.

If R_P is zero then the damping factor is zero and the time constant is infinity i.e. the system will not converge to a steady-state solution in response to a step input.

PFD/CP PLL with Feedback Divider - 1



Open loop:

$$H(s)=\frac{I_P K_{VCO}}{2\pi s}\left(R_P+\frac{1}{C_P s}\right)$$

Closed loop:

$$\varphi_{OUT}(s)=\left(\varphi_{IN}(s)-\frac{\varphi_{OUT}(s)}{M}\right)H(s)$$

$$\Rightarrow H_{Closed}(s)=\frac{H(s)}{1+\frac{H(s)}{M}}=\frac{\frac{I_P K_{VCO}}{2\pi s}\left(R_P+\frac{1}{C_P s}\right)}{1+\frac{I_P K_{VCO}}{2\pi M s}\left(R_P+\frac{1}{C_P s}\right)}$$

PFD/CP PLL with Feedback Divider - 2

After some manipulation:

$$H_{Closed}(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}\left(R_P C_P s + 1\right)}{s^2 + \frac{I_P K_{VCO}}{2\pi M} R_P s + \frac{I_P K_{VCO}}{2\pi C_P M}} = \frac{\frac{I_P K_{VCO}}{2\pi C_P}\left(R_P C_P s + 1\right)}{s^2 + 2\varsigma\omega_n s + \omega_n^2}$$

$$\Rightarrow \omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P M}} \quad \varsigma = \frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi M}} \quad \tau = \frac{1}{\varsigma\omega_n} = \frac{4\pi M}{I_P R_P K_{VCO}}$$

Placing a divider, M, in the feedback loop decreases the natural frequency and the damping factor and increases the settling time. To maintain the same stability as a PLL without a divider, the other loop parameter such as K_{VCO} or I_P have to be increased. In terms of the step response, the CPPLL with a divider behaves like a PLL with a VCO whose gain constant is K_{VCO}/M.