OLLSCOIL NA hÉIREANN
THE NATIONAL UNIVERSITY OF IRELAND

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

SUMMER EXAMINATIONS 2012

B.E. DEGREE (ELECTRICAL AND ELECTRONIC)

Processing of Integrated Circuits

UE 4008

Dr. Luke Seed
Prof. Nabeel A. Riza
Mr. Brendan O'Neill

Time allowed **1 ½ Hours**
Answer three out of four questions

Approved calculator permitted.

Question 1

a) Describe the evolution of the metal-oxide-semiconductor (MOS) device structure from processes with gate lengths > 1.0um through to current state-of-the-art devices with minimum geometries < 45nm. Particular attention should be paid to the gate stack and source/drain regions. Use diagrams to illustrate the answer. (21 marks)

b) If in a technology where the gate dielectric of a MOS device is silicon dioxide (dielectric constant 3.9) with a thickness of 1.2nm the dielectric is changed to hafnium dioxide (dielectric constant 25) without a change in the dielectric capacitance value;
   i. What is the dielectric capacitance?
   ii. What is the resultant dielectric thickness?
   iii. What is the capacitance of a device with a gate length of 45nm and a device width of 100nm? (13 marks)

Given:
The permittivity of free space is 8.86×10^{-14} F/cm

Question 2

a) Explain how an image is transferred from a photomask to a wafer surface in the photolithography process using positive photoresist. Use diagrams to illustrate the answer. (8 marks)
b) Describe the influence of the radiation (light) wavelength in the photolithography process, particularly on the minimum resolution and on the depth of field. (7 marks)
c) Briefly describe the equipment and process used in Reactive Ion Etching (RIE), using a diagram to illustrate the answer. (8 marks)
d) Using the linear etch model for a silicon etch with photoresist as a masking material, How deep is the silicon etched in the vertical direction well away from the mask edge, and in a lateral direction under the mask edge, if the etch time is 15 minutes? (10 marks)

Given:

$$\boldsymbol{R = \frac{S_c K_f F_c + K_i F_i}{N}}$$

Where R= Etch rate
S_c=0.01 Sticking coefficient, K_f=0.02 and K_i=1.0 and are the relative rate constants for the two processes (ion bombardment chemical etch). $F_c=2.5x10^{18}$ atoms.cm^{-2}s^{-1} and $F_i=1x10^{16}$ atoms.cm^{-2}s^{-1} are the chemical and ion fluxes and N is the density at $5x10^{22}$ atoms cm^{-3}

Question 3

a) In relation to a high energy beam of ions striking the surface of crystalline silicon explain the following:
    (i) Energy loss in the implanted ions (8 marks)
    (ii) Projected range and Straggle (8 Marks)
b) What is the junction depth of a phosphorus implant into a boron doped substrate, doping concentration 1 x 10^{15} atoms cm^{-3}, if the phosphorus implant dose is 1 x 10^{16} atoms cm^{-2}? The implant has an energy that puts the peak of the implant at the interface between the silicon surface and an oxide which is 0.035μm thick. Assume that the heat treatment needed to activate the implant does not add to the junction depth. (17 marks)

Given:

$C_{(x)} = C_p.\exp[-(x-R_p)^2/2\Delta R_p^2]$

Projected Range and Projected Standard Deviation Graphs attached.

Question 4

a) Describe how an enhancement mode NMOS transistor, in terms of holes and electrons, can go from an “off” state to “on” state (12 marks)
b) With the aid of diagrams describe the structure of a FinFET or TriGate SOI MOS structure. (10 marks)
c) If the polysilicon gate of an NMOS transistor in a Self-Aligned LOCOS process is over etched during processing by 0.1μm per side, calculate the change in maximum saturated current that would result on a transistor with a design gate length of 1.0μm and width of 10μm. What would the effect be if the LOCOS processing meant the “birds beak” (LOCOS edge) encroached into the active area 0.5μm all round (as well as the over etched polysilicon)? (11marks)

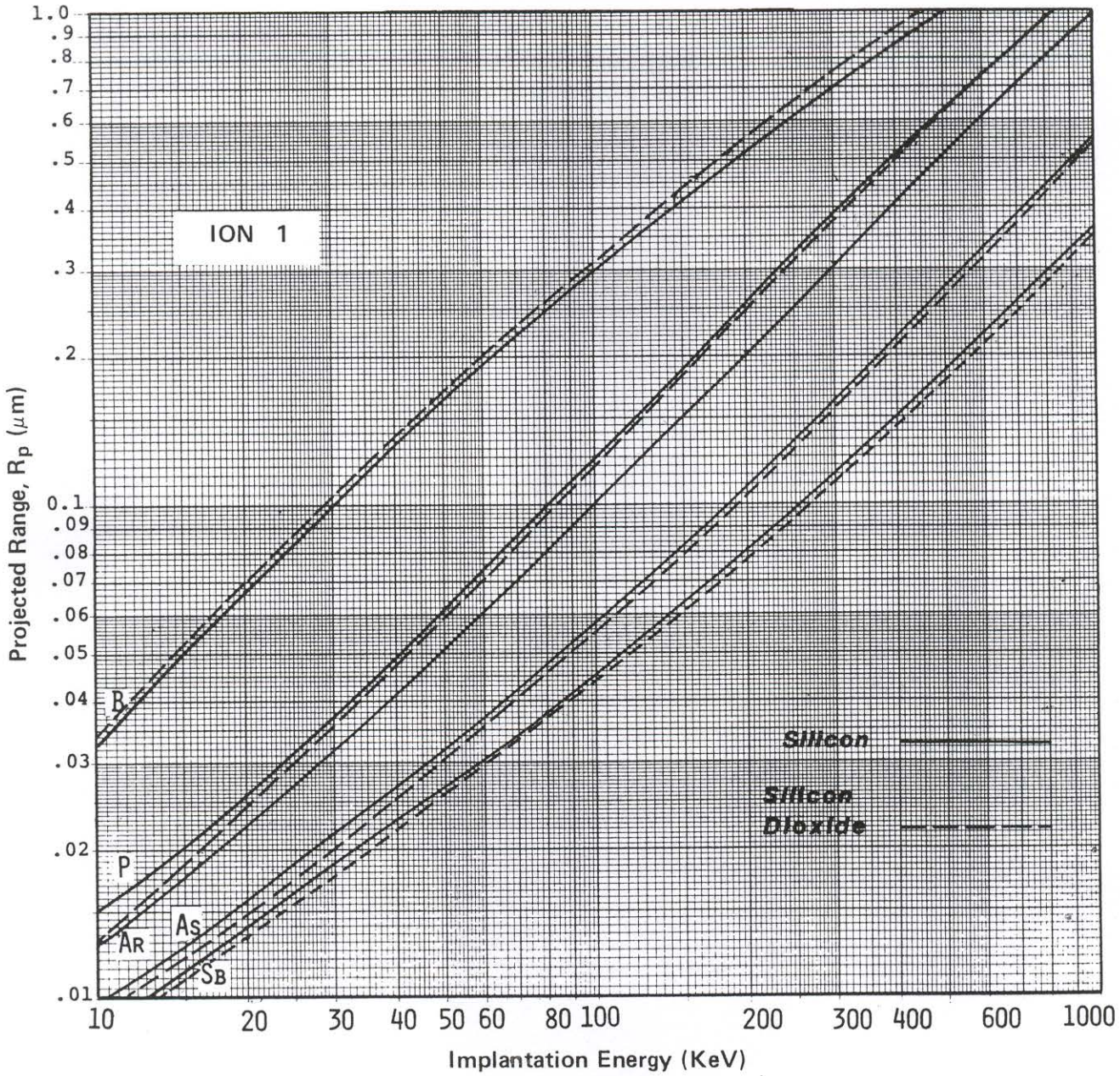
Given

V_t = 0.8V and the maximum power supply voltage is 5.0V

μ_n = 1450cm^2/V.s

C_{ox} = 5 x 10^{-8}F/cm^2

PROJECTED RANGE IN SILICON & SILICON DIOXIDE[1]



PROJECTED STANDARD DEVIATION IN SILICON & SILICON DIOXIDE[1]