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THE NATIONAL UNIVERSITY OF IRELAND, CORK

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

SUMMER EXAMINATIONS, 2011

B. E. (ELECTRICAL AND ELECTRONIC)
M.ENG.SC. (MICROELECTRONICS)
VSEU (VISITING EUROPEAN)

RF IC Design
EE4011

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Answer *five* questions.

All questions carry equal marks.
The use of departmental approved non-programmable calculators is permitted.
Smith Charts are appended to this paper. Detach and use as required. Write your examination number on any charts you use and return them with your examination script.

The following physical constants may be used if necessary:
Boltzmann's Constant: $k = 1.381 \times 10^{-23}$ J/K
Elementary Charge: $q = 1.602 \times 10^{-19}$ C
Vacuum Permittivity: $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m

Time allowed: *3 hours*

1. (a) Starting with equations for collector and base currents in a bipolar junction transistor (BJT), determine suitable expressions for the small-signal transconductance, output conductance and input (base-emitter) resistance of a BJT.

[*4 marks*]

(b) Draw a cross-section of a typical BJT and using this cross-section as a starting-point briefly describe the most important capacitances that contribute to the small-signal model of the BJT.

[*4 marks*]

(c) Develop an expression for the base-emitter capacitance of a BJT biased in the forward active region, in terms of the applied bias, V_{BE} and the collector current, I_C.

[*4 marks*]

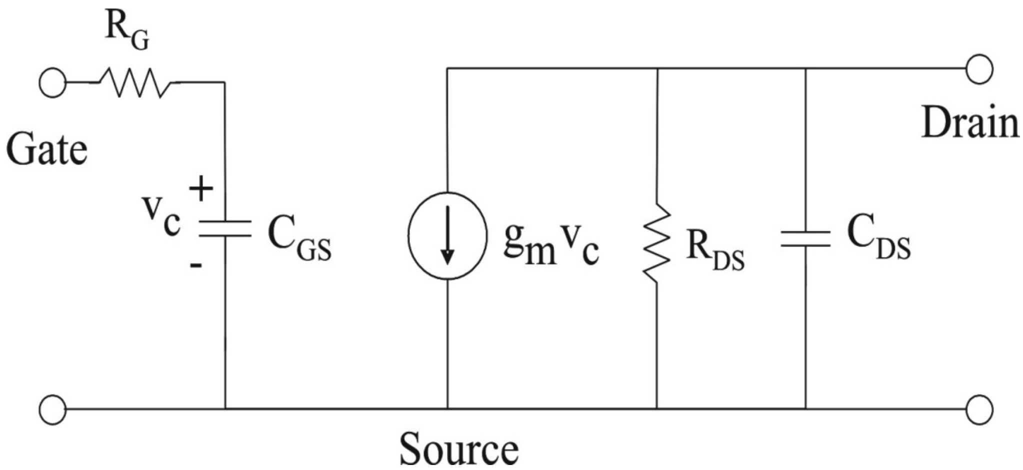
(d) Determine the y-parameters of a BJT, biased in the forward-active region with the following operating conditions and parameters:

Operating frequency: 1.5GHz
Operating temperature: 300K
Applied Bias: $V_{BE} = 0.75V$, $V_{CE} = 3.0V$
Device Parameters: $I_S = 1x10^{-15}A$, $V_A = 10V$, $\beta = 100$,
$C_{JE} = 0.3pF$, $M_{JE} = 0.5$, $V_{JE} = 1.0V$, $\tau_F = 0.1ns$.

[*8 marks*]

Note: Assume that for this device, only the base-emitter capacitance components are significant.

2. (a) The diagram below shows a simplified small-signal model of a GaAs MESFET. If this device is considered to be a two-port network with port 1 at the gate, port 2 at the drain and the source grounded, derive expressions for the y-parameters of the device in terms of the circuit elements.



[*8 marks*]

(b) The *y*-parameters of a MESFET device with the equivalent circuit and measurement conditions as described in part (a) have been measured at a frequency of 2GHz with the following results:

$y_{11} = 0.01 \angle 87.7°$ $y_{12} = 0$ $y_{21} = 0.20\angle -2.3°$ $y_{22} = 0.004 \angle 73.6°$

Determine the values of the small-signal circuit elements for this device.

[*6 marks*]

(c) Define the *ABCD* parameters for a two-port network and determine the *ABDC* parameters for the device with *y*-parameters given in (b).

[*6 marks*]

3. (a) Two cosinusioidal waveforms with amplitudes A_1 and A_2 (V) and frequencies ω_1 and ω_2 (rad/s) respectively, are applied to the input of a balanced (differential) RF amplifier, giving an output waveform as follows:

$$
\begin{aligned}
y(t) = &\left[\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2\right]\cos(\varpi_1 t) \\
&+\left[\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_1^2 A_2\right]\cos(\varpi_2 t) \\
&+\frac{1}{4}\alpha_3 A_1^3 \cos 3\varpi_1 t + \frac{1}{4}\alpha_3 A_2^3 \cos 3\varpi_2 t \\
&+\frac{3}{4}\alpha_3 A_1^2 A_2 \cos(2\varpi_1 + \varpi_2)t + \frac{3}{4}\alpha_3 A_1^2 A_2 \cos(2\varpi_1 - \varpi_2)t \\
&+\frac{3}{4}\alpha_3 A_1 A_2^2 \cos(2\varpi_2 + \varpi_1)t + \frac{3}{4}\alpha_3 A_1 A_2^2 \cos(2\varpi_2 - \varpi_1)t
\end{aligned}
$$

Using the formula for y(t) as a starting point and assuming that α_1 and α_3 have opposite signs, derive an expression for the input-referred 3rd-order intermodulation intercept point (*IIP3*) of the amplifier.

[5 *marks*]

(b) Starting with the definition of the noise factor for an amplifier, develop an expression for the sensitivity of the amplifier which specifies the minimum input power that is required to give an acceptable minimum signal-to-noise ratio, SNR_{min}, at the output. Assume the amplifier has bandwidth B, and also assume that the amplifier input forms a conjugate match to the source so that the noise power delivered from the source is given by

$$P_{RS} = kT \quad W/Hz$$

From the expression you derive, identify the noise floor of the system.

[*8 marks*]

(c) Illustrate the concept of spurious free dynamic range (SFDR) using a suitable diagram and calculate the SFDR for a receiver system that requires a minimum SNR of 15dB at the output. The system characteristics are as follows:

NF=10 dB, P_{IIP3}= -5dBm, B=2MHz, T=300K

[*7 marks*]

4. (a) A transistor has the following S-parameters and noise parameters (with Z_0=50Ω) at 5GHz:

$$s_{11} = 0.33\angle -150° \quad s_{12} = 0.01\angle 60° \quad s_{21} = 4.0\angle -50° \quad s_{22} = 0.50\angle -45°$$

$$F_{\min} = 3.0\ dB \quad \Gamma_{opt} = 0.75\angle 180° \quad R_N = 10.0\Omega$$

(i) State the conditions necessary to ensure that the device will be stable in an amplifier configuration and determine if the device satisfies these conditions.

[*2 marks*]

(ii) Determine the Maximum Unilateral Transducer Gain available from this device.

[*2 marks*]

(iii) Determine the Unilateral Figure of Merit for the device and determine the error in predicting gain when using the unilateral assumption in (ii) above.

[*2 marks*]

(b) Using Smith-Chart procedures, design input and output matching networks to obtain the maximum unilateral transducer gain from the device in part (a) at 5GHz and in a system with both source and load impedances of 50Ω. Show your work clearly using the Smith Charts provided and determine the component values of the input and output matching networks.

[*10 marks*]

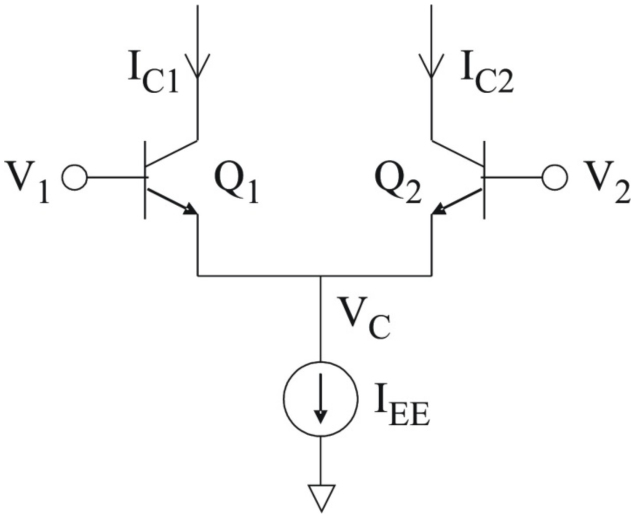
(c) If the device in part (a) uses input and output matching networks that give the maximum unilateral transducer gain in a 50Ω system at 5GHz, determine the best noise figure that can be achieved, to the nearest dB.

Note: The following equations specify noise circles where the symbols have their usual meaning:

$$N_i = \frac{F_i - F_{\min}}{4R_N / Z_0}\left|1+\Gamma_{opt}\right|^2 \quad C_{Fi} = \frac{\Gamma_{opt}}{N_i+1} \quad R_{Fi} = \frac{\sqrt{N_i\left(N_i+1-\left|\Gamma_{opt}\right|^2\right)}}{\left(N_i+1\right)}$$

[*4 marks*]

5. (a) The circuit below shows a bipolar common-emitter pair formed using identical transistors Q_1 and Q_2 and a current source I_{EE}.



Starting with an expression for the current flowing in a BJT, determine an expression for the difference between the collector currents ($\Delta_{IC} = I_{C1} - I_{C2}$) as a function of the differential input voltage ($\Delta V = V_1 - V_2$) and provide an approximate sketch of Δ_{IC} vs. ΔV.

[*12 marks*]

(b) Perform a small-signal analysis on the circuit in part (a) for differential input signals and compare the result you obtain with the formula you have derived for part (a) when taken in the limit as $\Delta V \rightarrow 0$.

[*4 marks*]

(c) Illustrate, using a circuit diagram, how emitter coupled pairs such as shown in (a) can be combined to form a Gilbert-cell double-balanced mixer for RF applications.

[*4 marks*]

6. (a) Illustrate a Type 1 Phase Locked Loop (PLL) using an integer feedback divider.

[*4 marks*]

(b) Determine the closed-loop transfer function of the PLL in (a) making sure that the denominator follows the form of a standard second-order system where the symbols have their usual meaning:

$$s^2 + 2\varsigma\omega_n s + \omega_n^2$$

[8 *marks*]

(c) A Type 1 PLL using an integer feedback divider is to be used as a frequency synthesizer to generate frequencies from 925 MHz to 960 MHz in steps of 200kHz.

(i) Determine the appropriate input reference frequency.

[2 *marks*]

(ii) Determine the range of divider values to give the desired frequency range.

[2 *marks*]

(iii) Determine the cut-off frequency of the low pass filter using an appropriate rule of thumb.

[2 *marks*]

(iv) Outline the most important limitation on PLL performance arising from the use of an integer feedback divider and suggest a possible solution to this limitation.

[2 *marks*]

7. (a) Draw a detailed block-level architecture of a single-chip GPS/Galileo receiver and outline the functions of the main blocks in the IC providing detail of frequencies, bandwidth, gain, noise levels and data rates as appropriate.

[*10 marks*]

(b) With reference to the single-chip GPS/Galileo receiver outlined in (a), provide a detailed discussion of **ONE** of the following topics:

(i) Operation of the GPS/Galileo System, or

(ii) Front-end specifications and operation, or

(iii) Dual-band low-noise amplifiers (LNAs), or

(iv) RF mixers, or

(v) Voltage controlled oscillators (VCOs), or

(vi) Pierce oscillators, or

(vii) Phase-locked-loops (PLLs), or

(viii) Layout and testing issues for RFICs.

[*10 marks*]