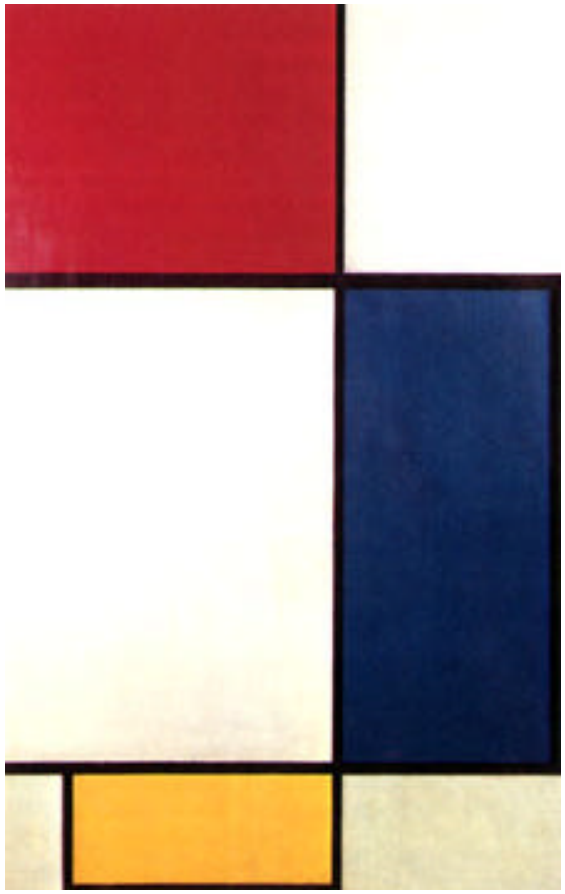
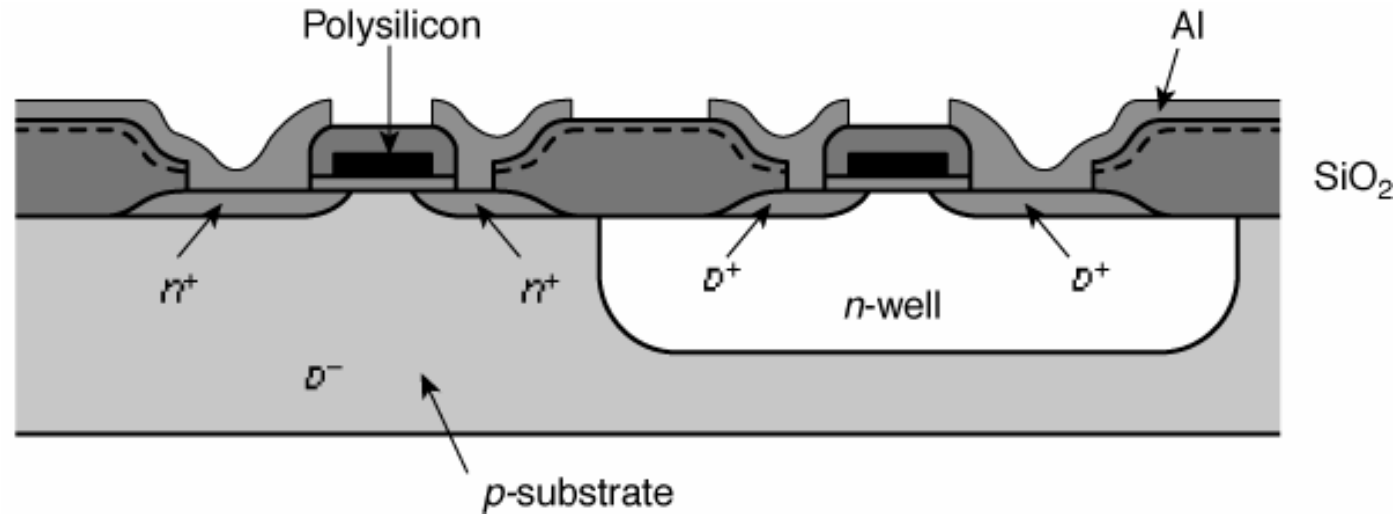
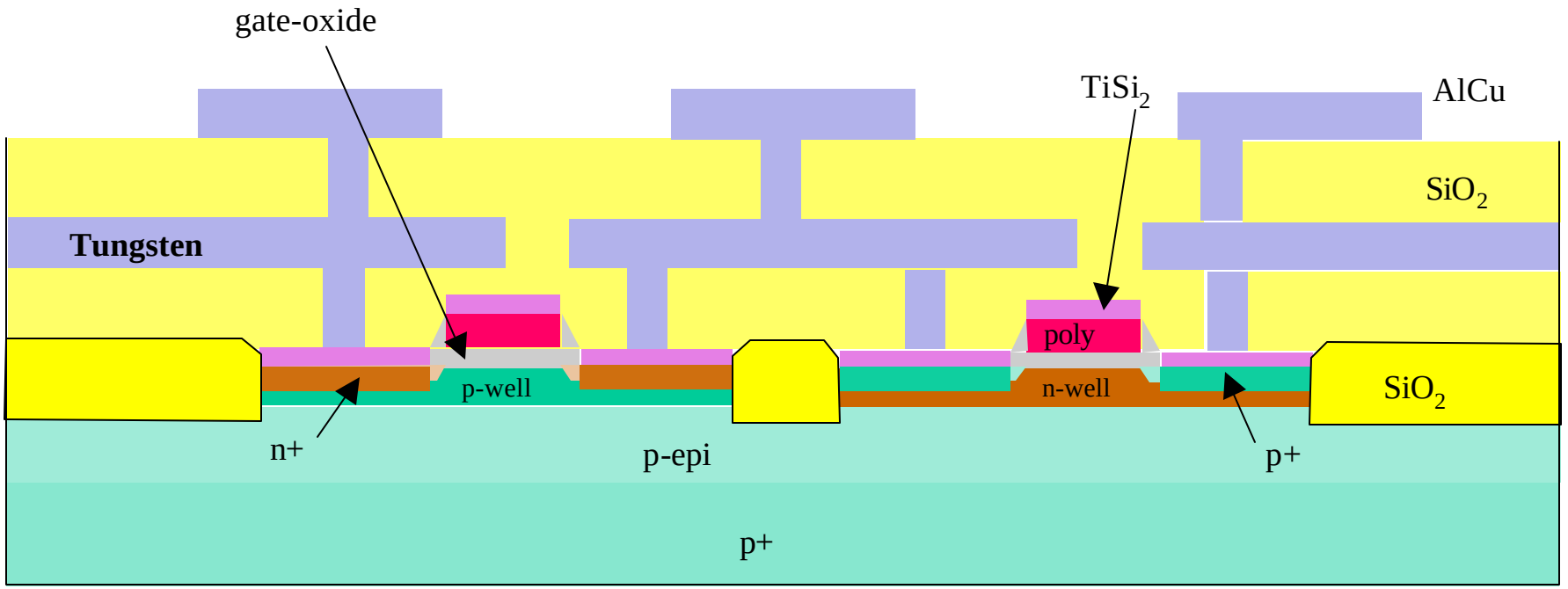
CMOS Manufacturing Process



CMOS Process

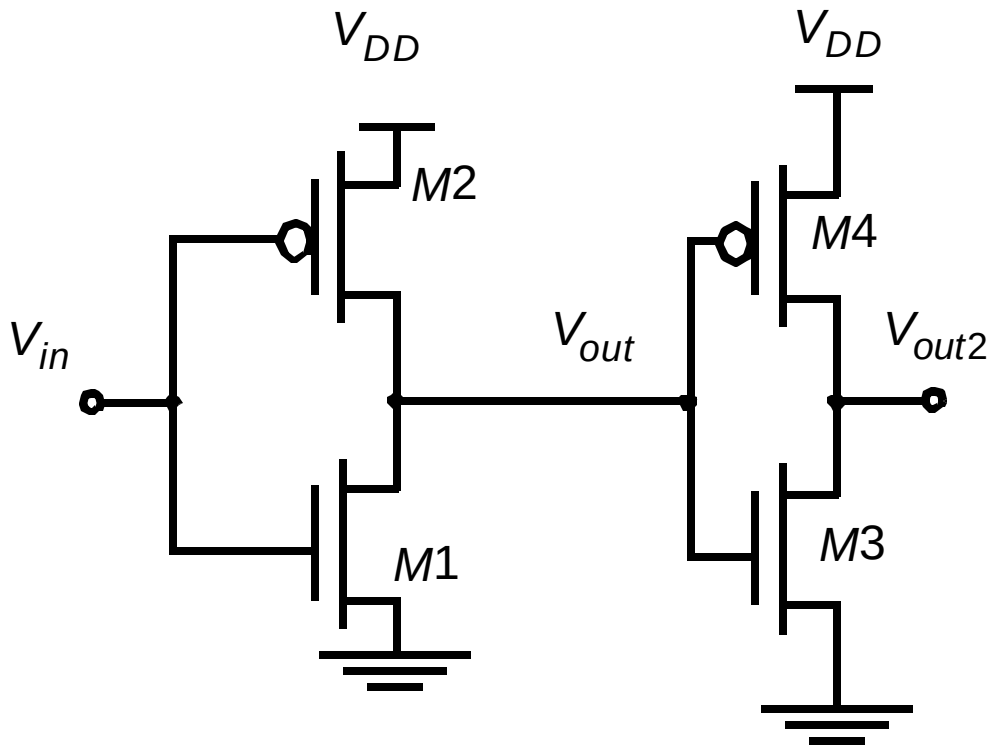


A Modern CMOS Process



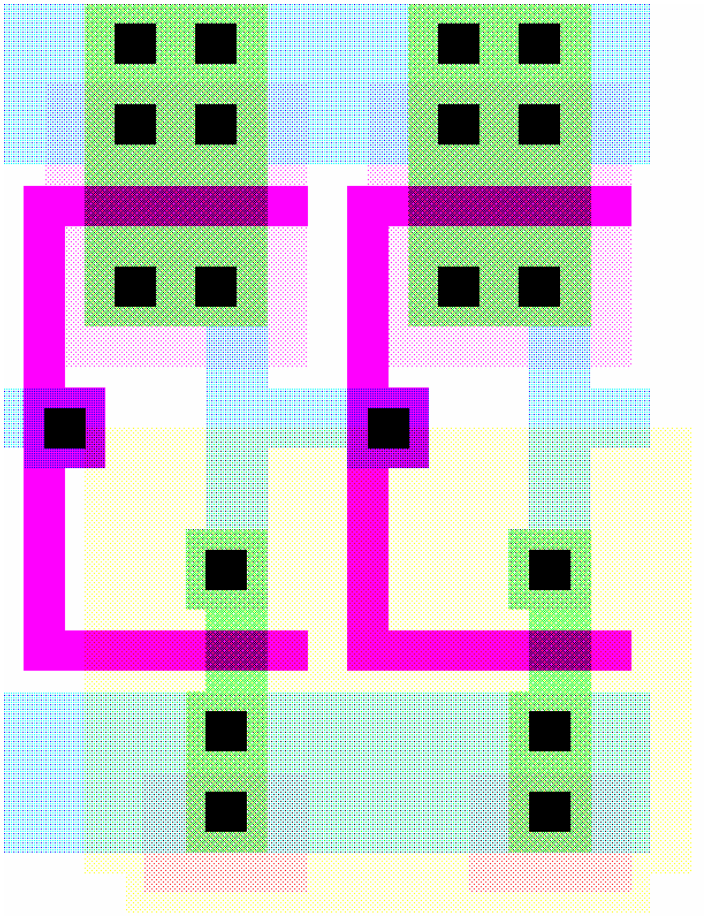
Dual-Well Trench-Isolated CMOS Process

Circuit Under Design



This two-inverter circuit (of Figure 3.25 in the text) will be manufactured in a twin-well process.

Circuit Layout



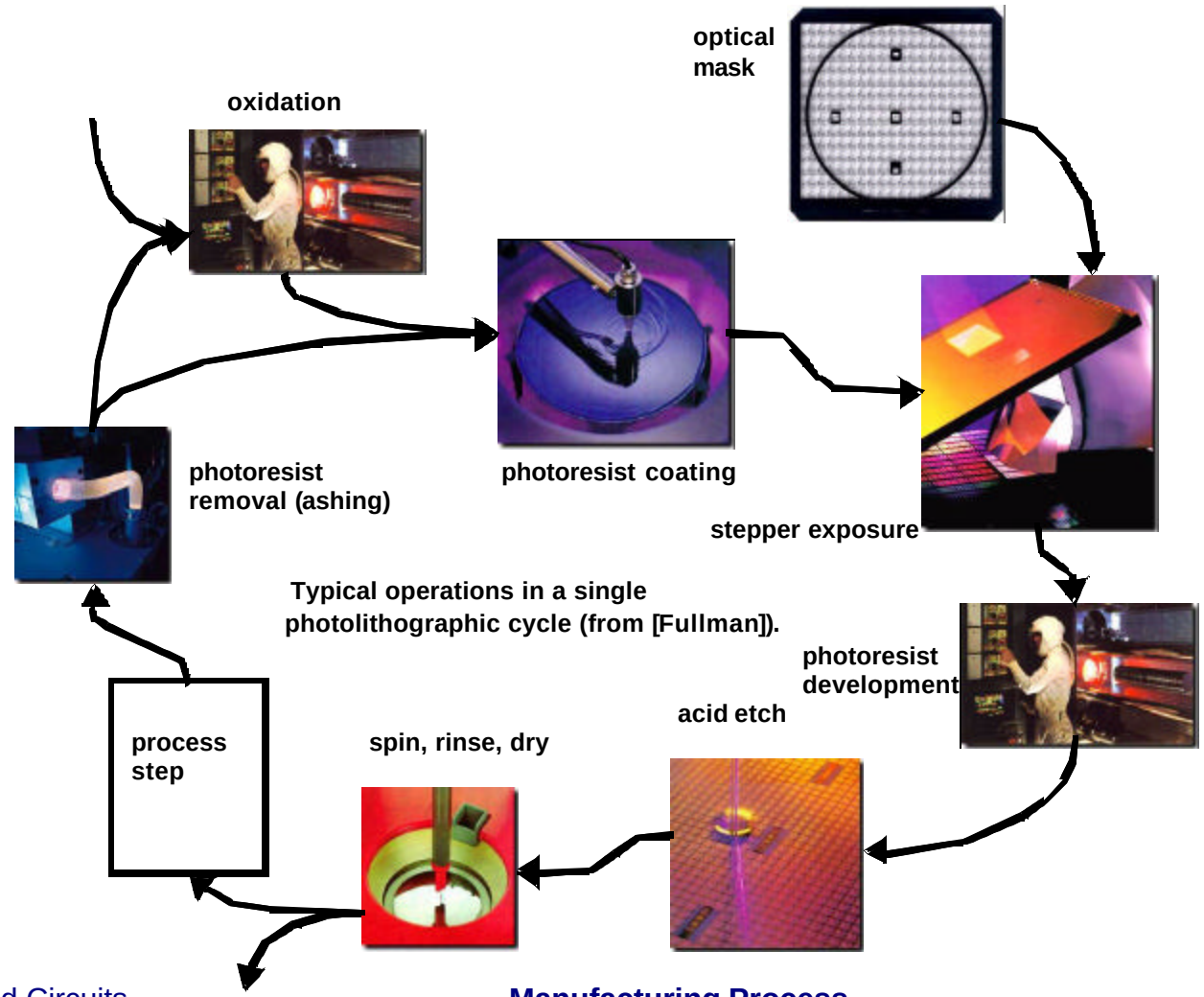
The Manufacturing Process

For a great tour through the process and its different steps, check
http://www.fullman.com/semiconductors/semiconductors.html

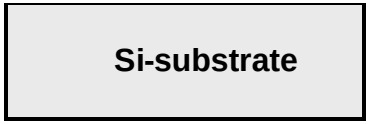
For a complete walk-through of the process (64 steps), check the Book web-page

http://bwrc.eecs.berkeley.edu/Classes/IcBook

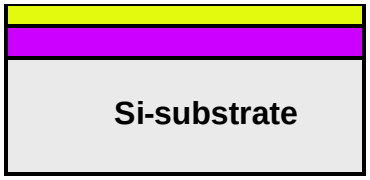
Photo-Lithographic Process



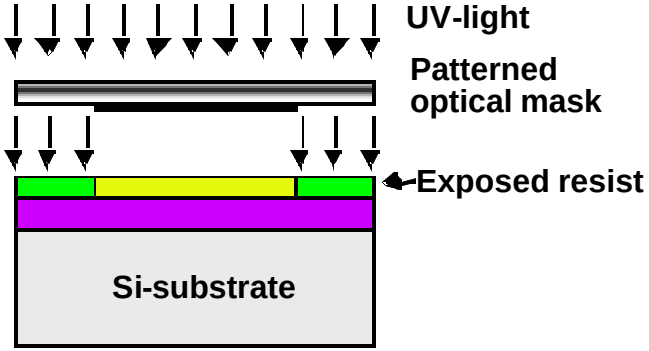
Patterning of SiO2



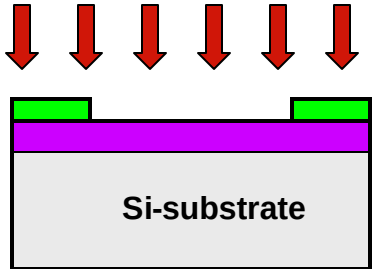
(a) Silicon base material



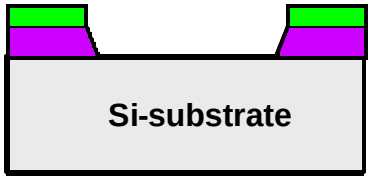
(b) After oxidation and deposition of negative photoresist



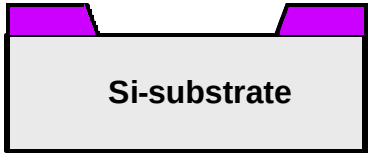
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2

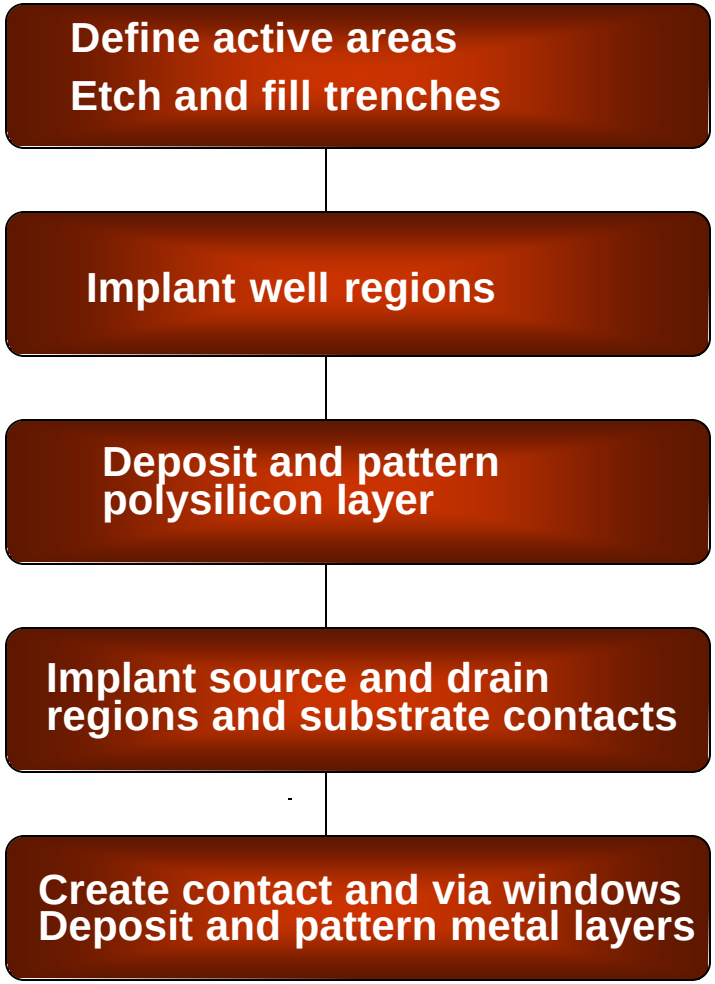


(e) After etching

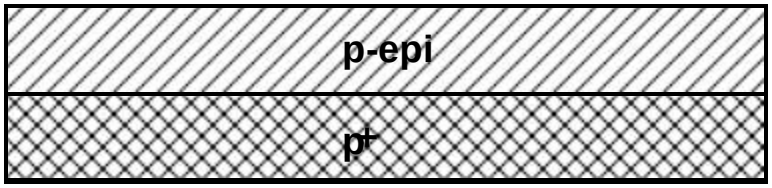


(f) Final result after removal of resist

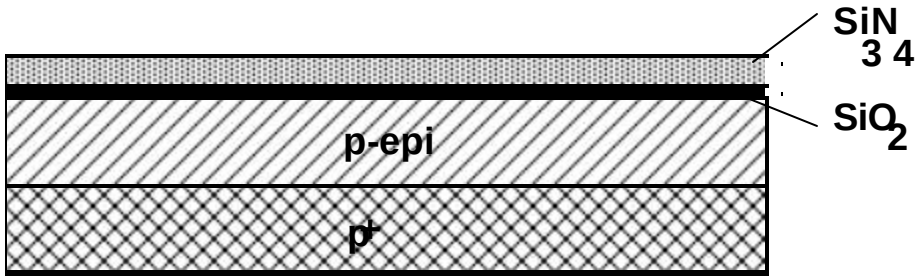
CMOS Process at a Glance



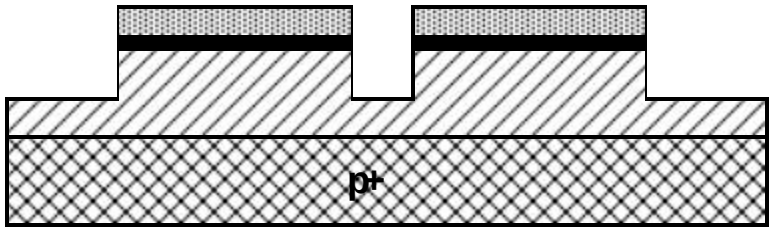
CMOS Process Walk-Through



(a) Base material: p+ substrate with p-epi layer

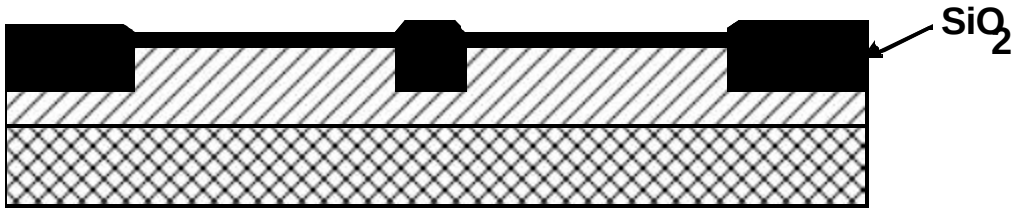


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

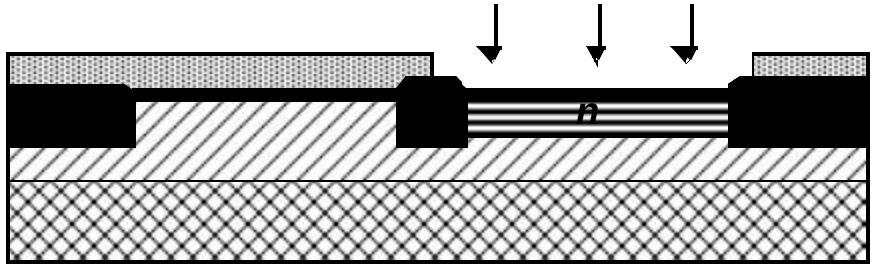


(c) After plasma etch of insulating trenches using the inverse of the active area mask

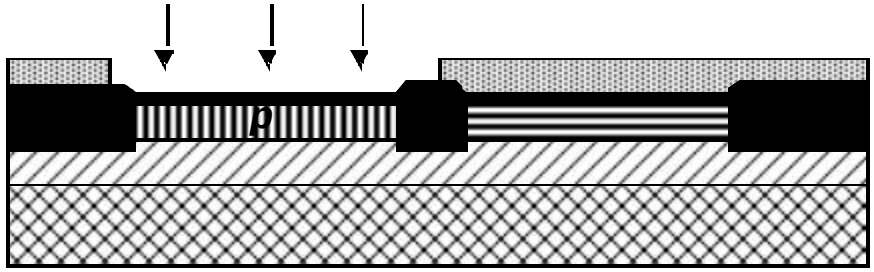
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

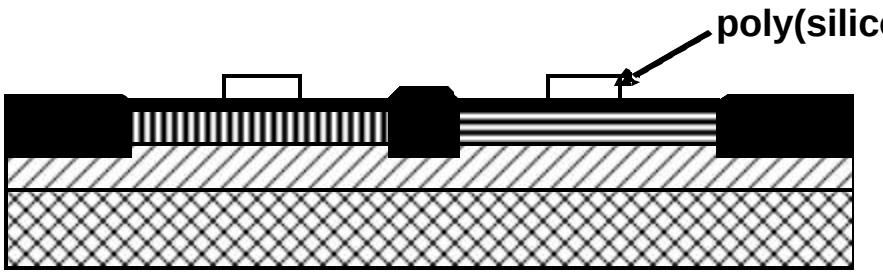


(e) After n-well and V_{Tp} adjust implants

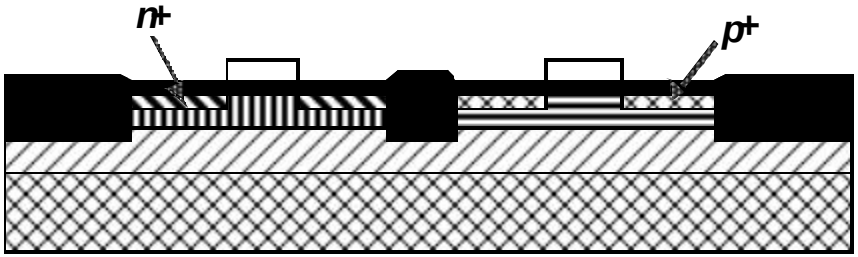


(f) After p-well and V_{Tn} adjust implants

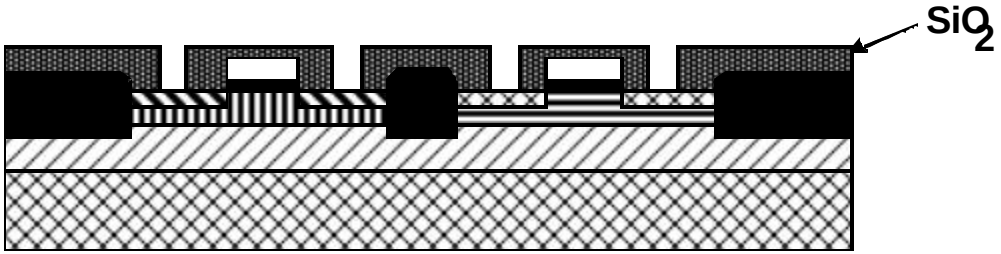
CMOS Process Walk-Through



(g) After polysilicon deposition and etch

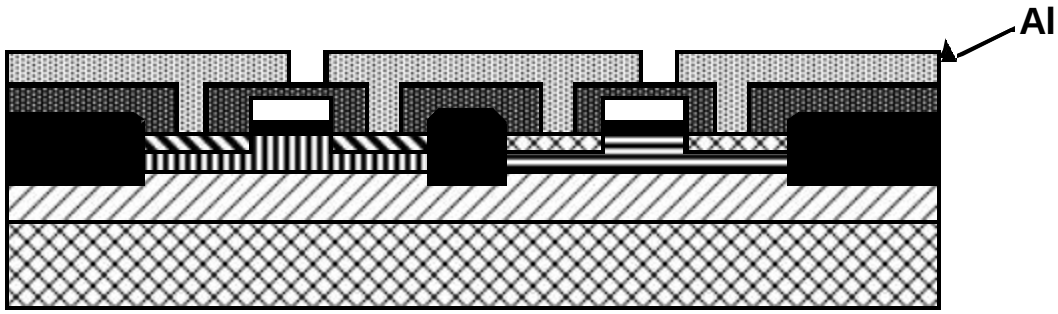


(h) After *n*+ source/drain and *p*+ source/drain implants. These steps also dope the polysilicon.

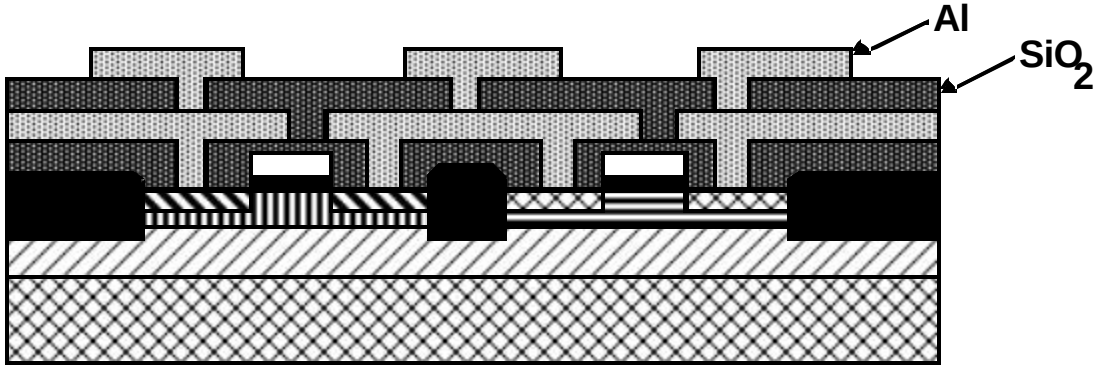


(i) After deposition of SiO_2 insulator and contact hole etch.

CMOS Process Walk-Through

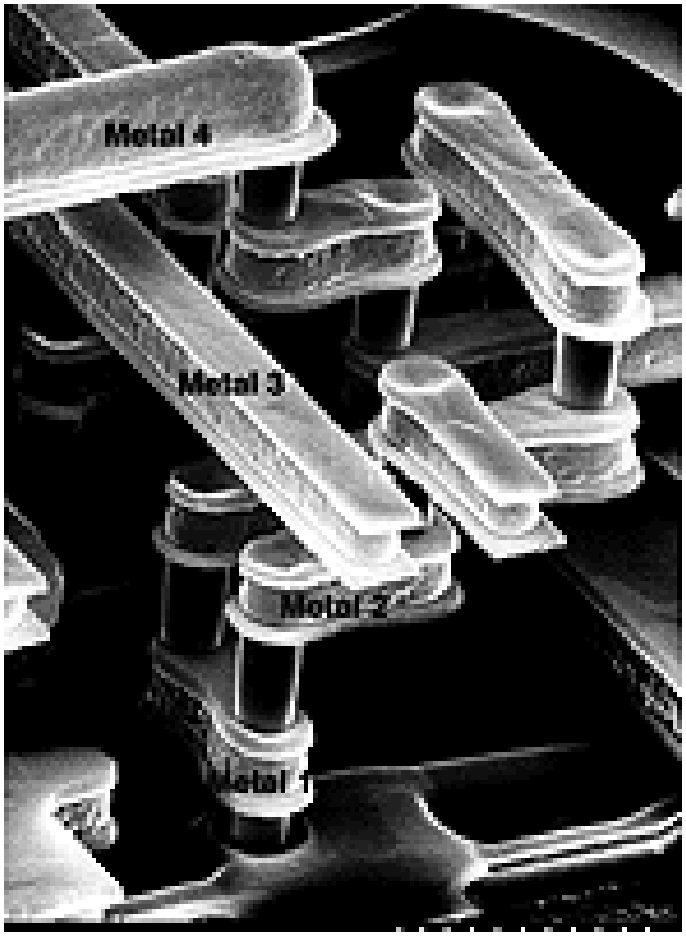


(j) After deposition and patterning of first Al layer.

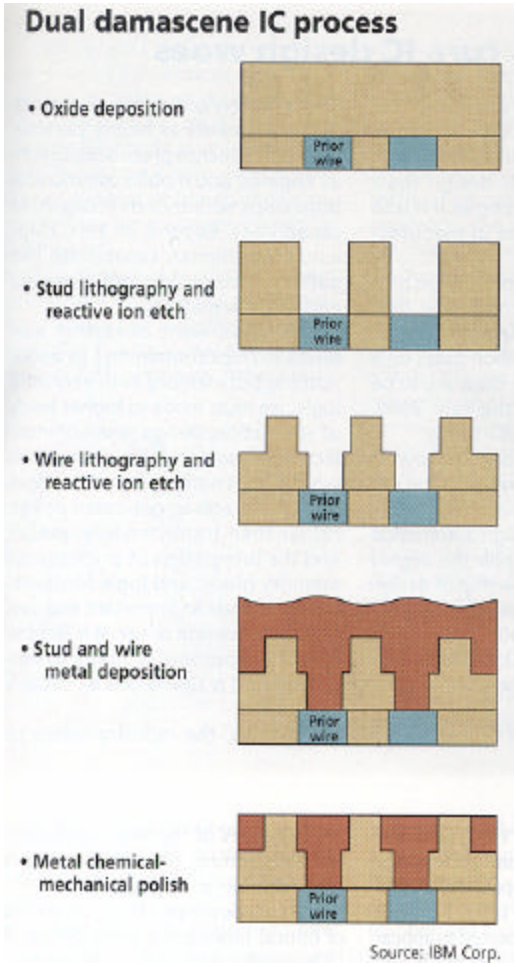


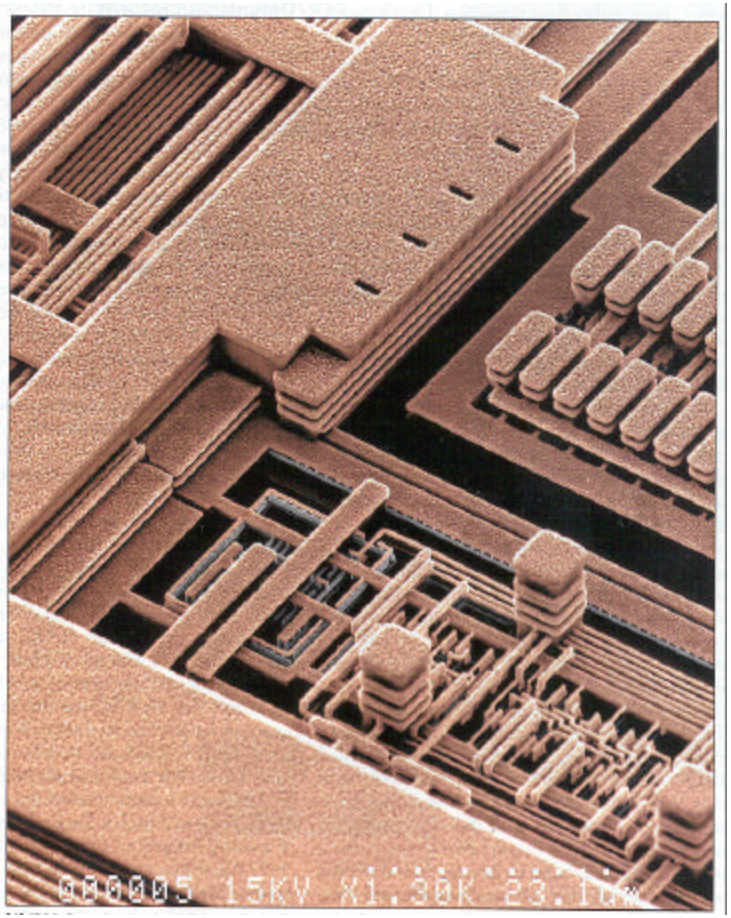
(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

Advanced Metalization



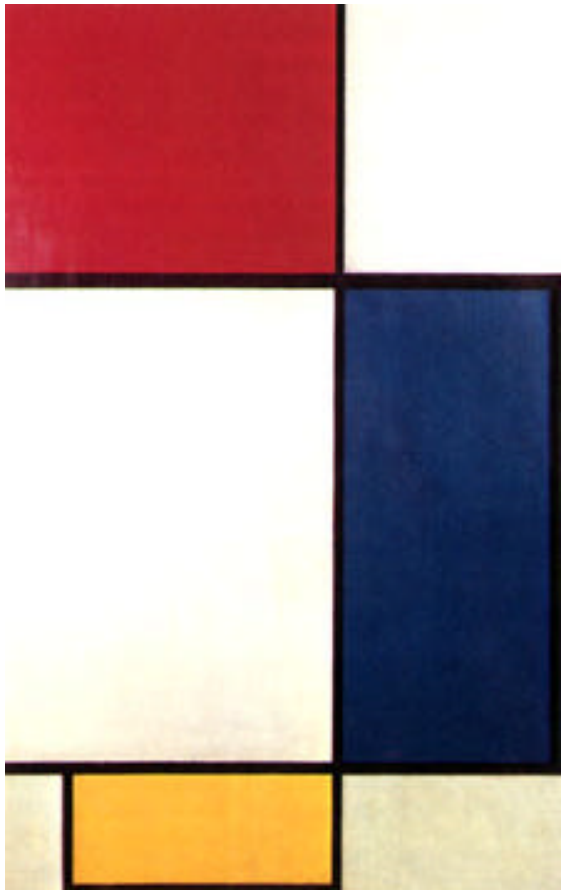
Advanced Metalization



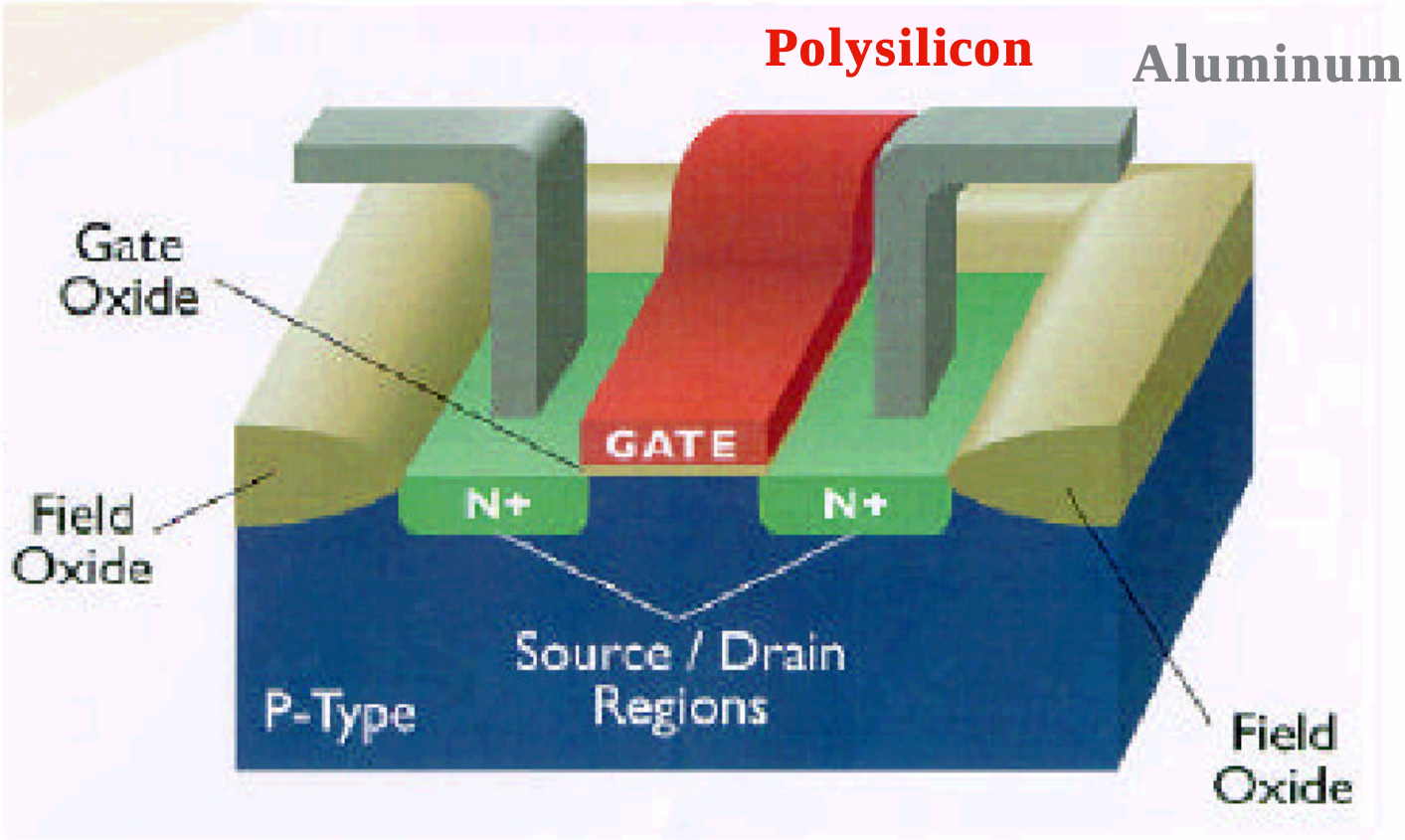


Design Rules

Jan M. Rabaey



3D Perspective



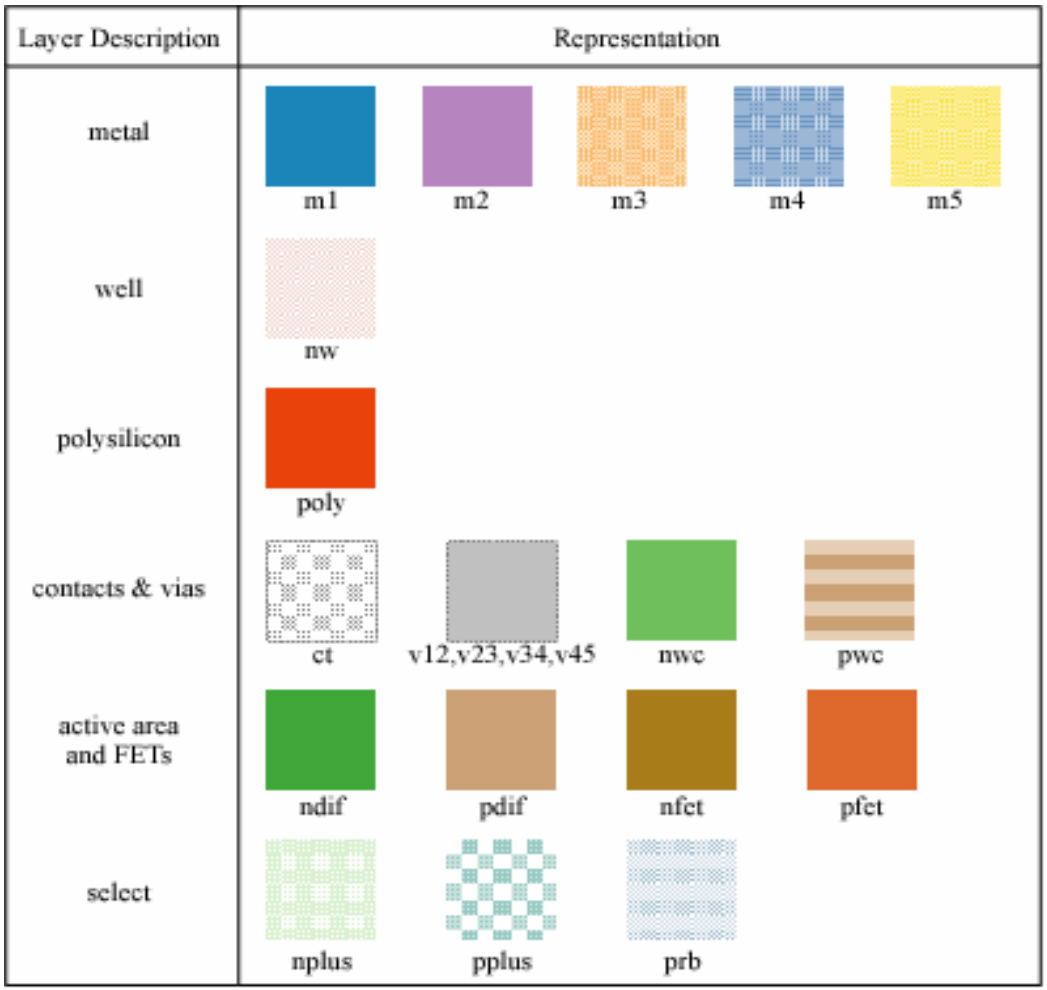
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - » scalable design rules: lambda parameter
  - » absolute dimensions (micron rules)

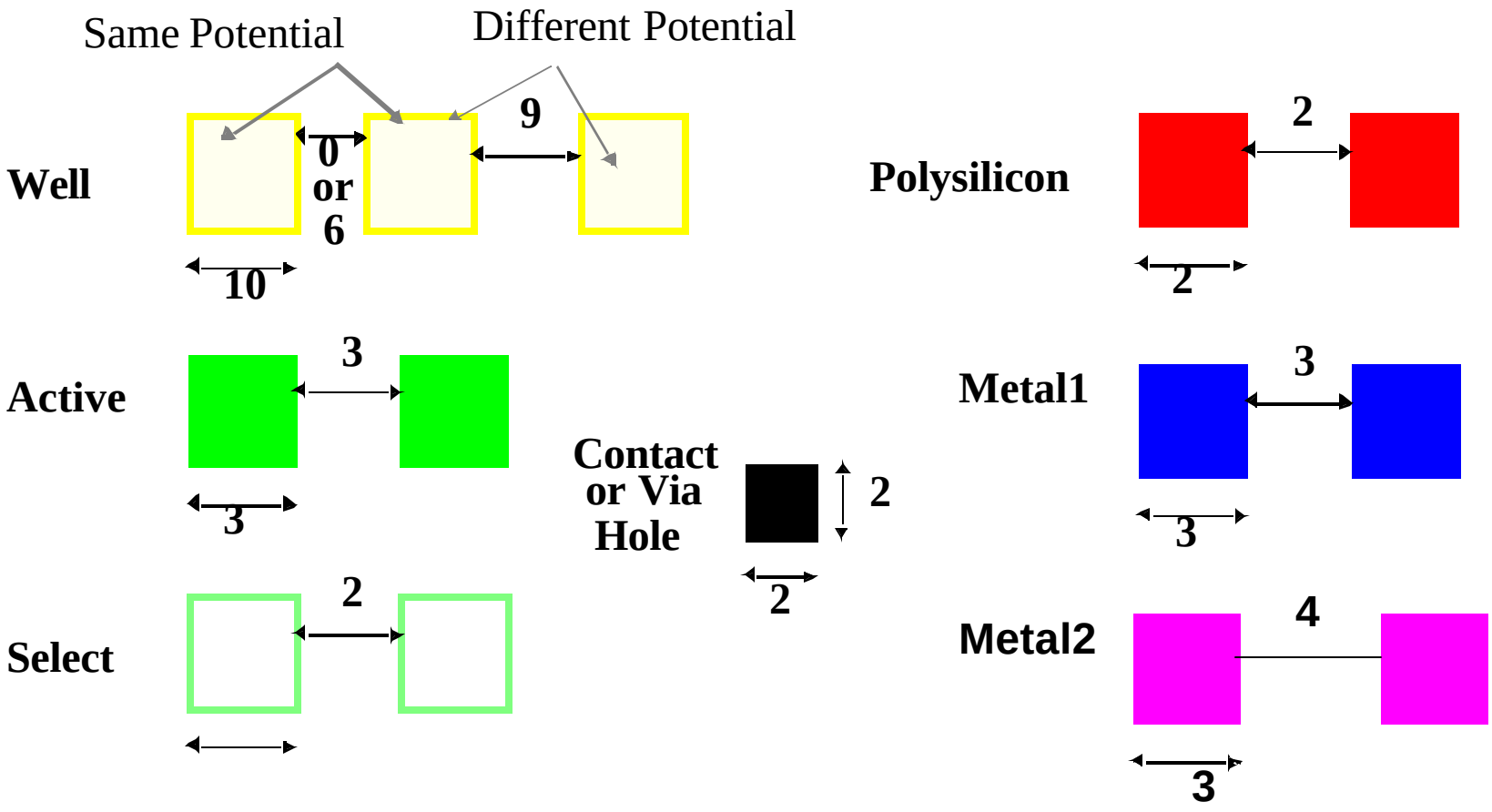
CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

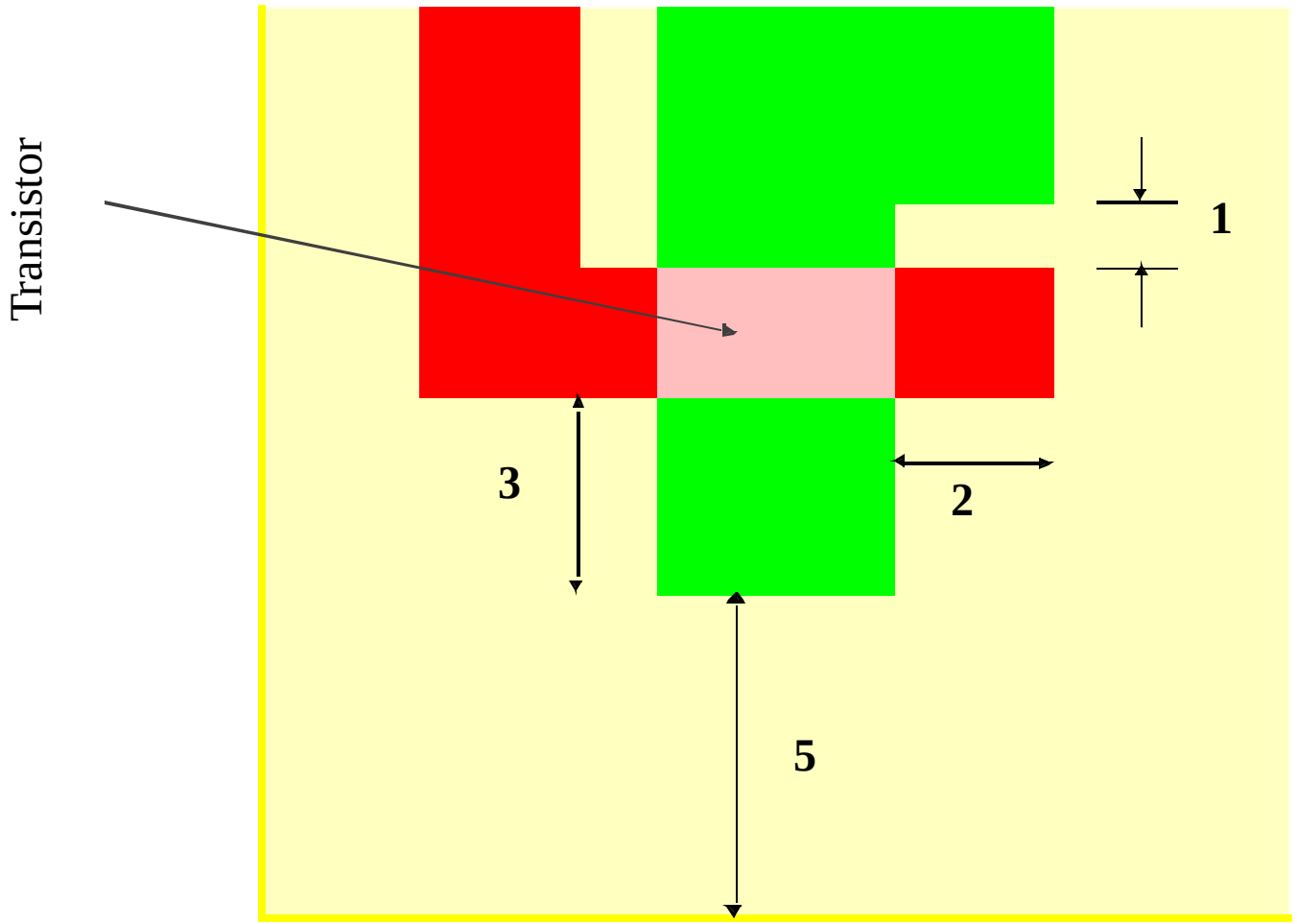
Layers in 0.25 µm CMOS process



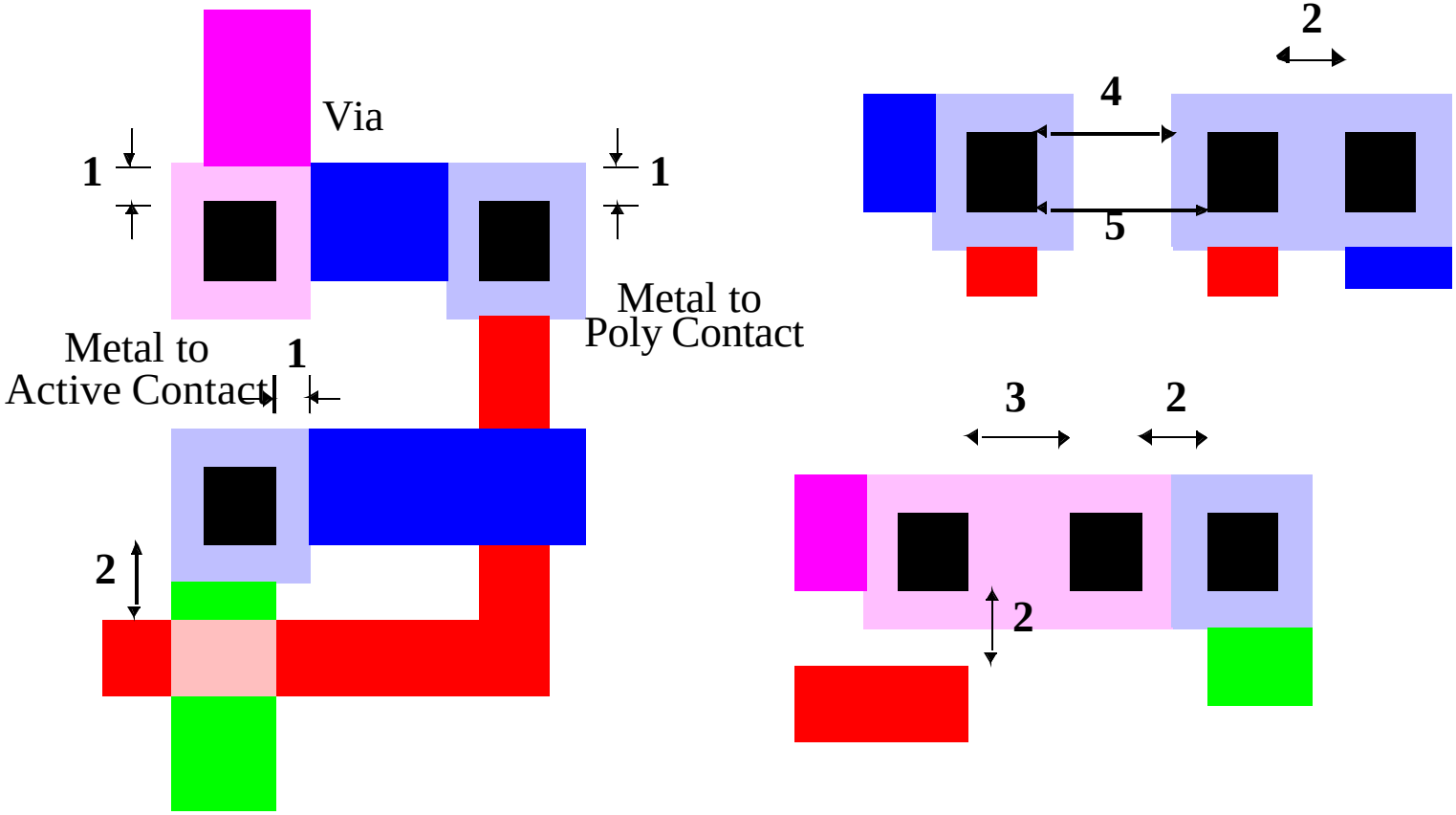
Intra-Layer Design Rules



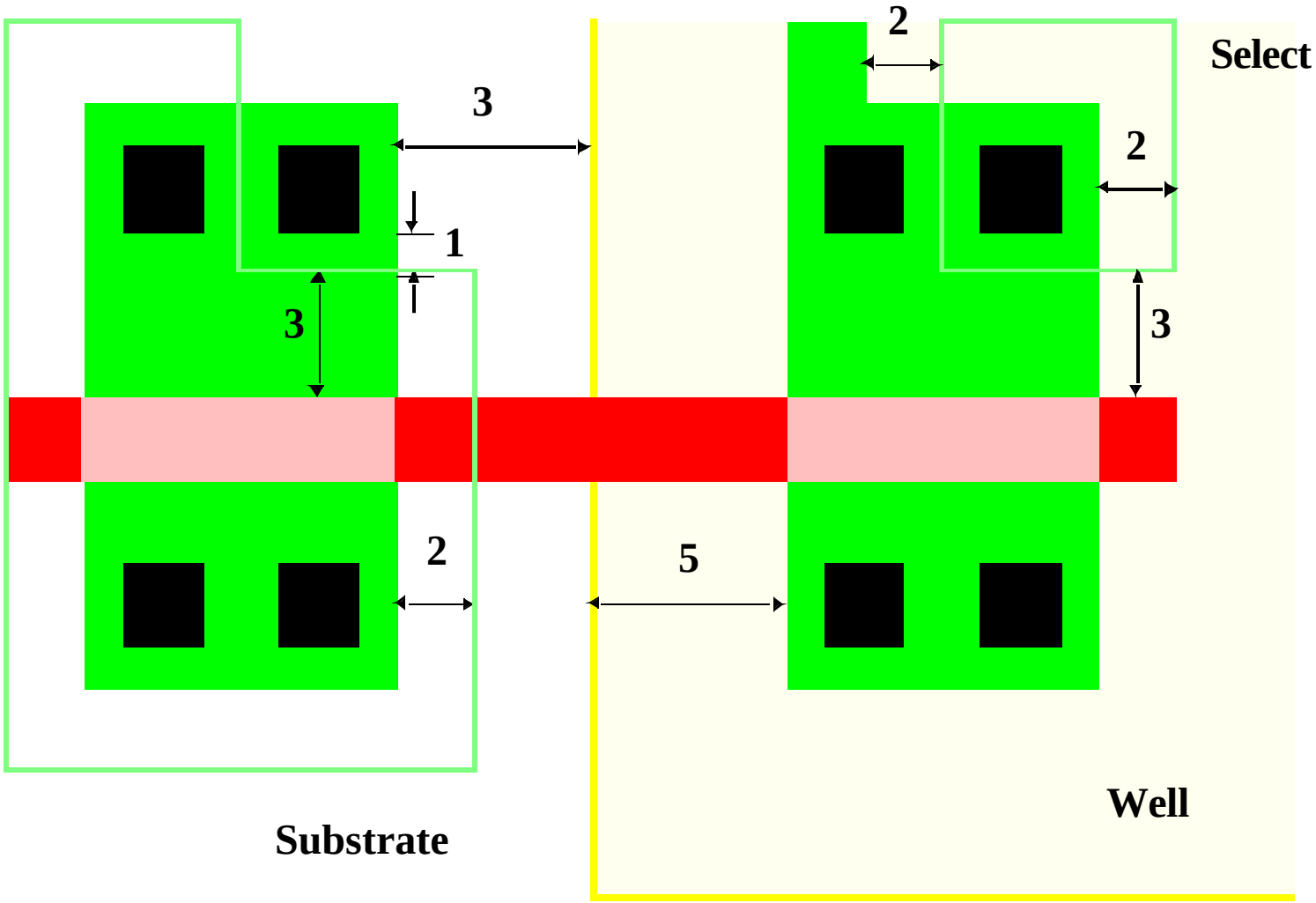
Transistor Layout



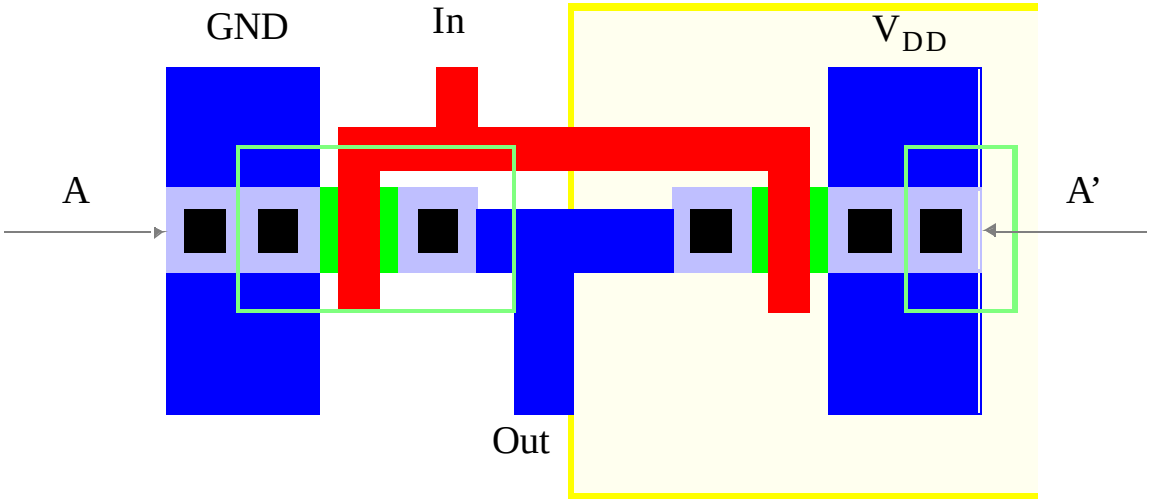
Vias and Contacts



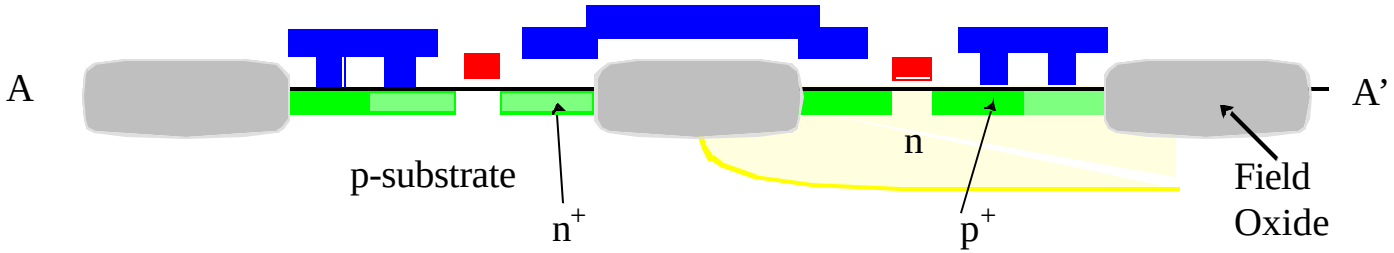
Select Layer



CMOS Inverter Layout

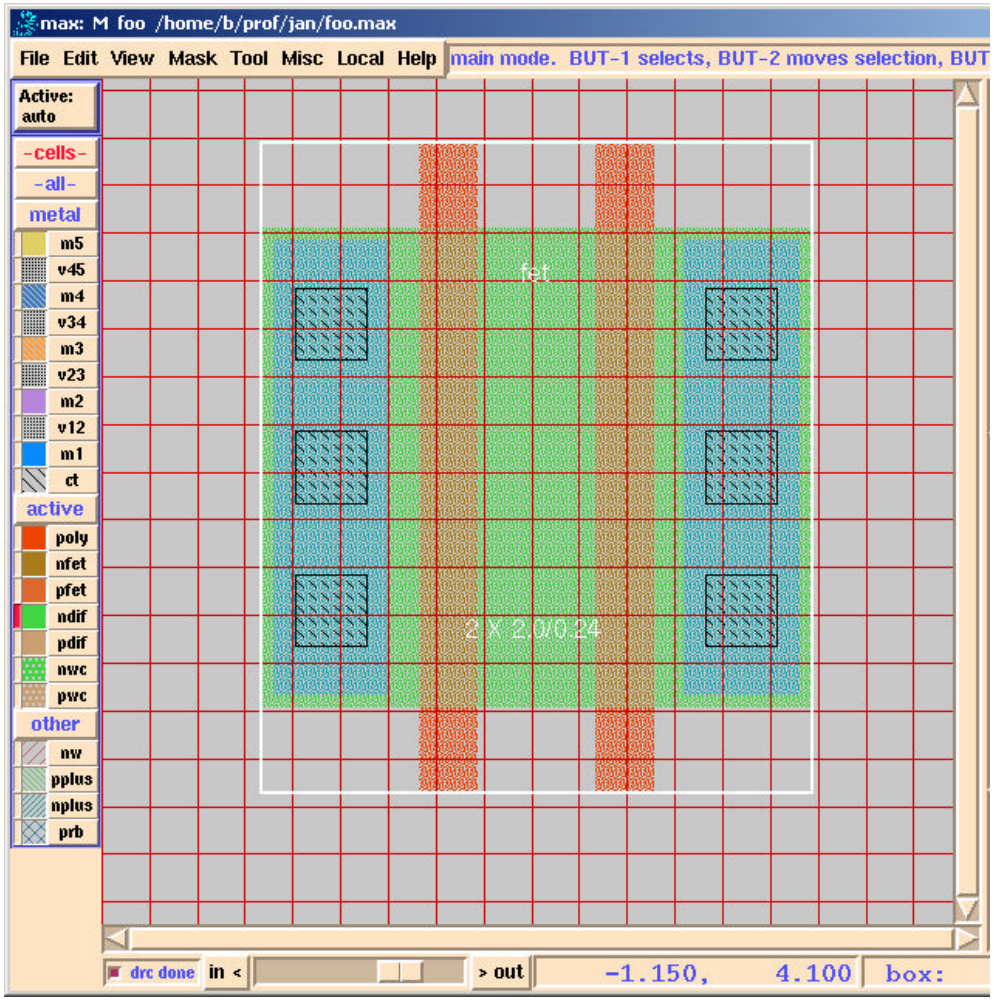


(a) Layout

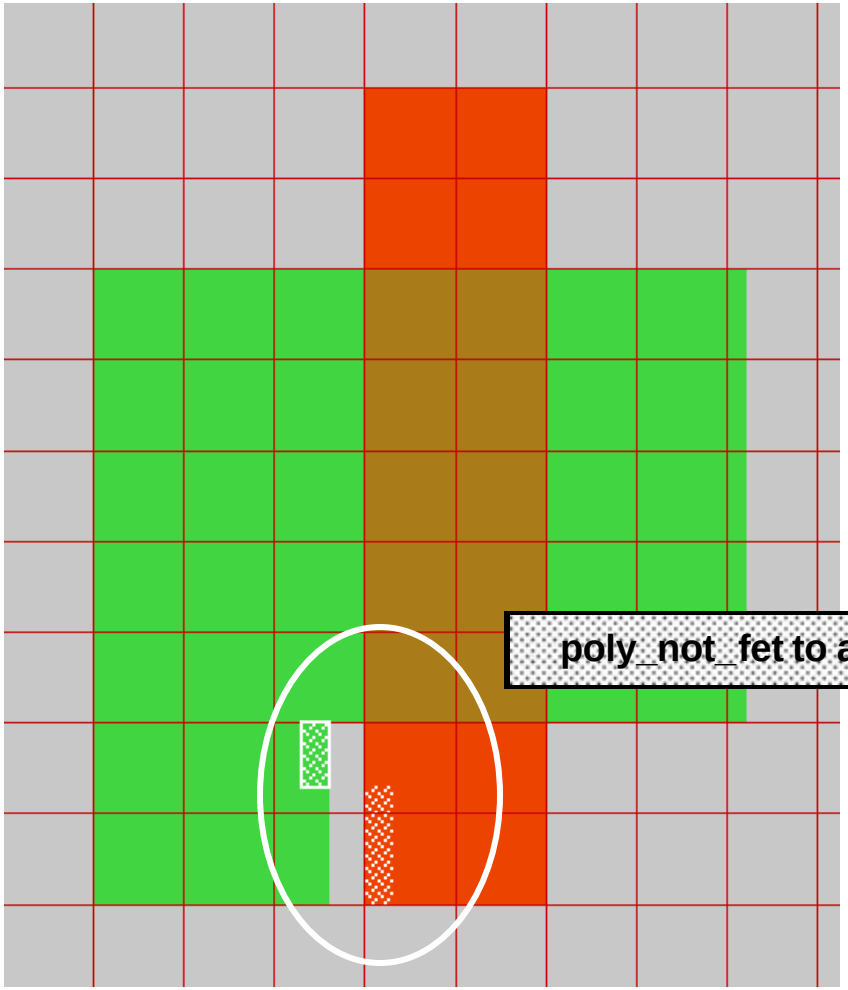


(b) Cross-Section along A-A'

Layout Editor

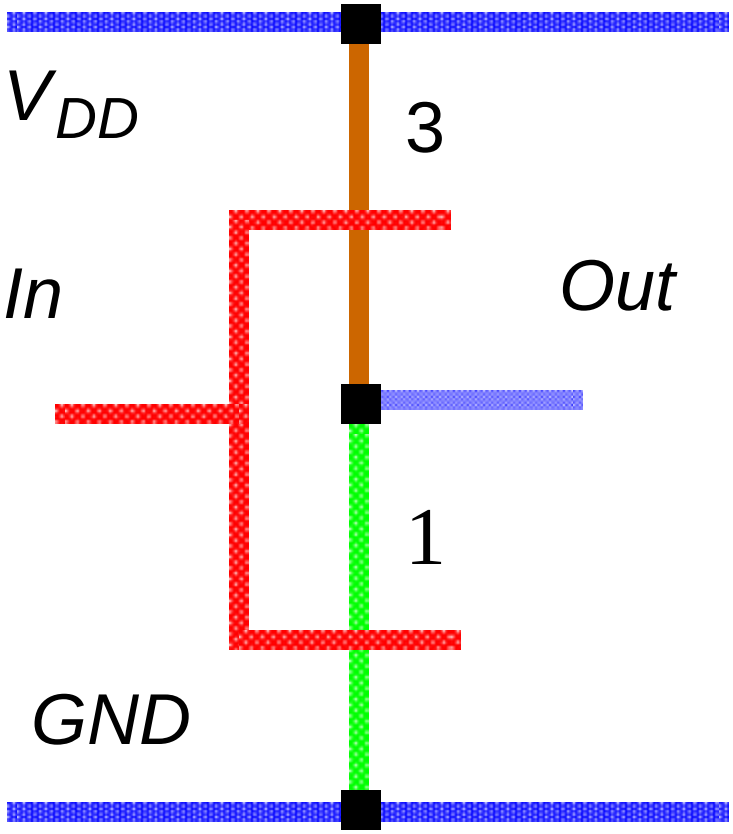


Design Rule Checker



poly_not_fet to all_diff minimum spacing = 0.14 um.

Sticks Diagram



Stick diagram of inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by "compaction" program