Silicon-on-Insulator

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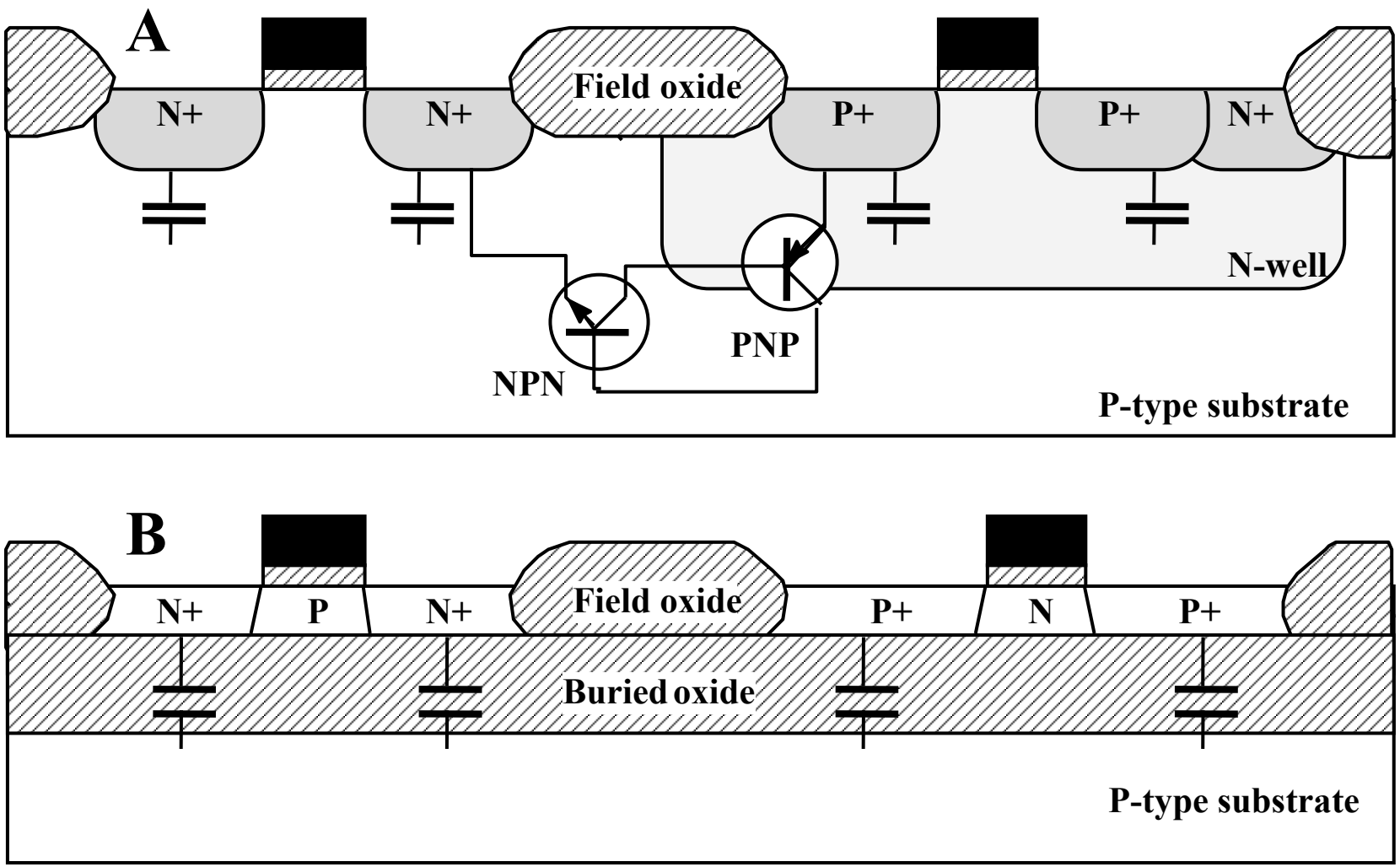
Tyndall National Institute

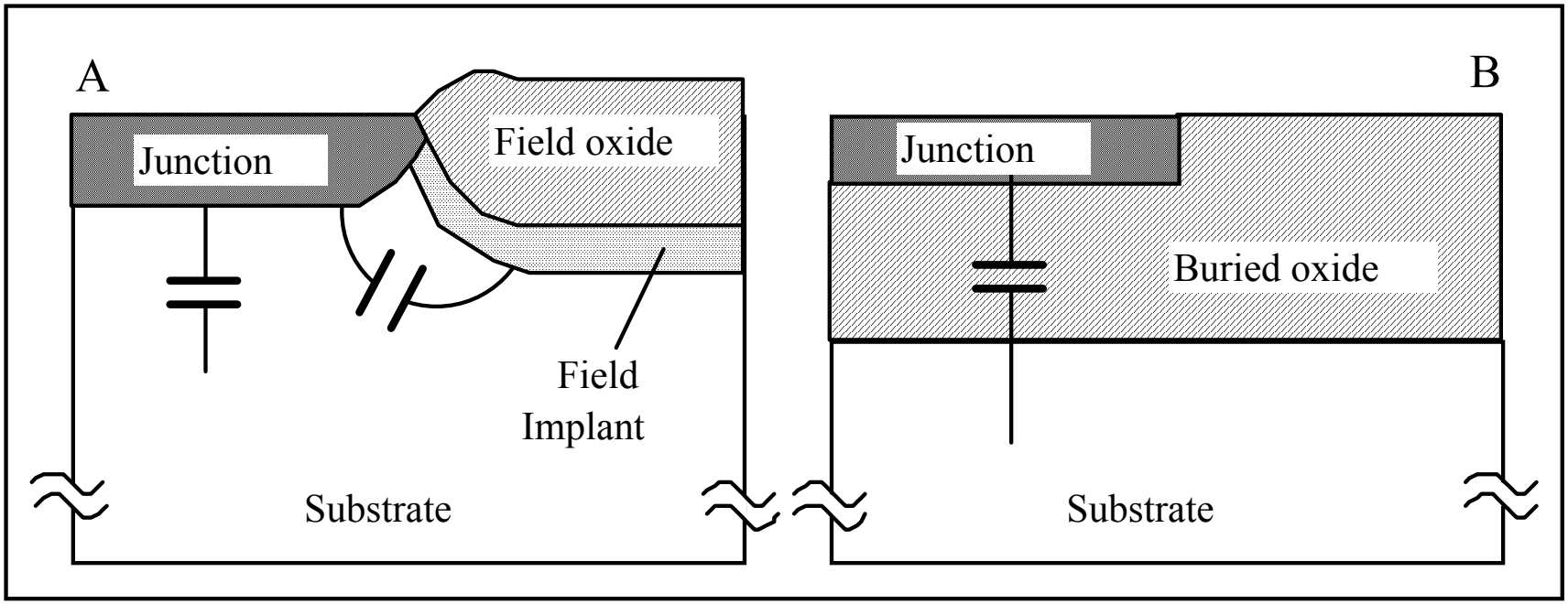
Outline

- Types of SOI MOSFETs and their basic properties
  - SOI vs. bulk
  - Partially depleted MOSFET
  - Fully depleted MOSFET
- Particularities of IC processing using SOI wafers

Latchup and junction capacitances



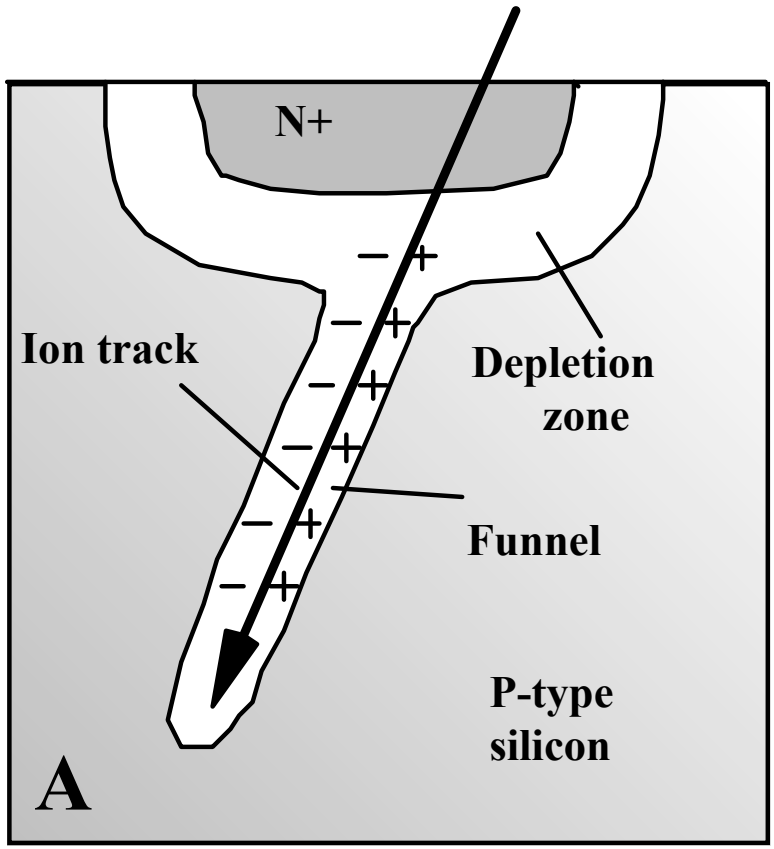
Junction capacitances



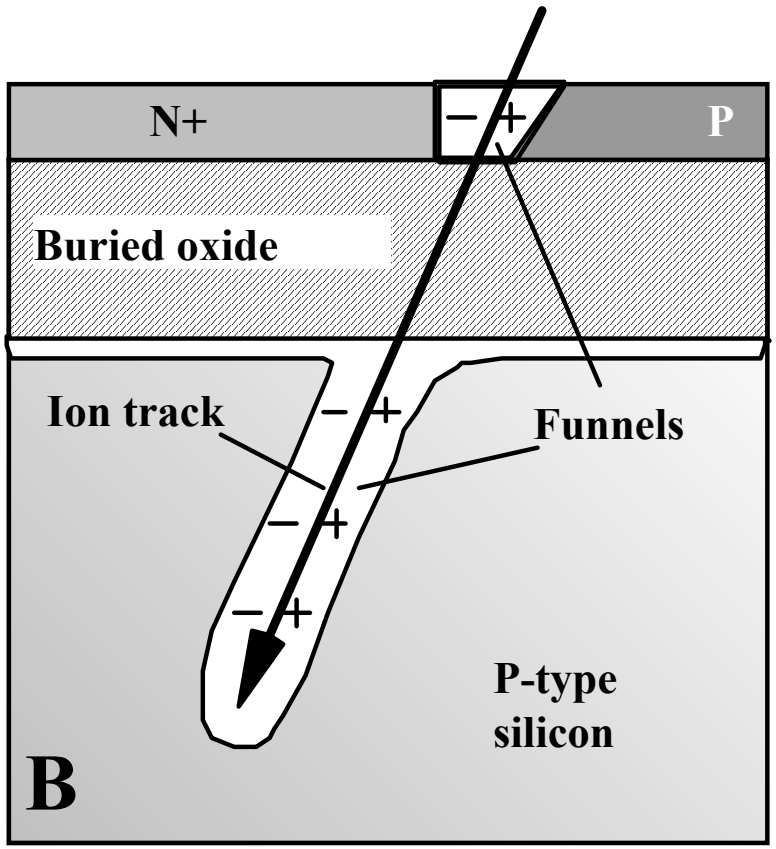
A: Bulk junction capacitance; B: SOI junction capacitance

Junction capacitance is 4 to 10 times smaller in SOI

Single-event upset / Soft errors

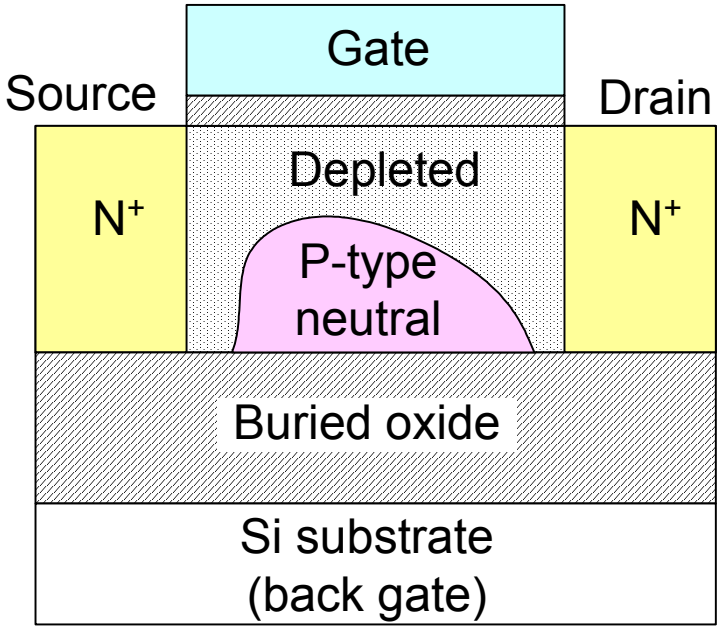


Bulk

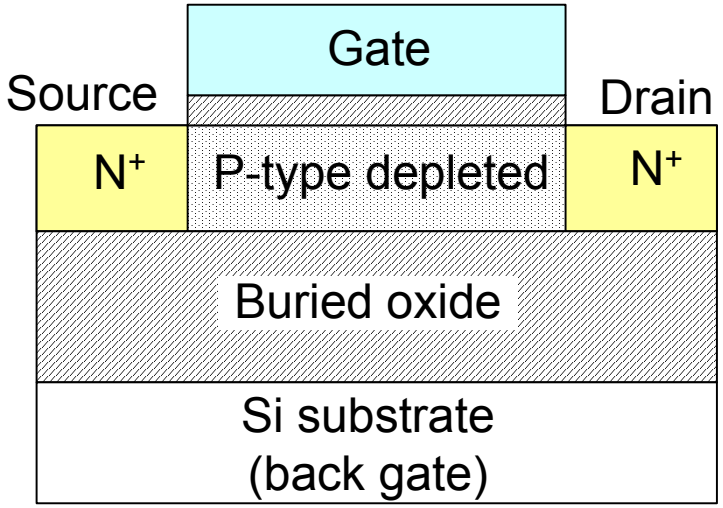


SOI

Partially Depleted and Fully Depleted SOI MOSFETs



Partially depleted
SOI MOSFET



Fully depleted SOI
MOSFET

Outline

- Types of SOI MOSFETs and their basic properties

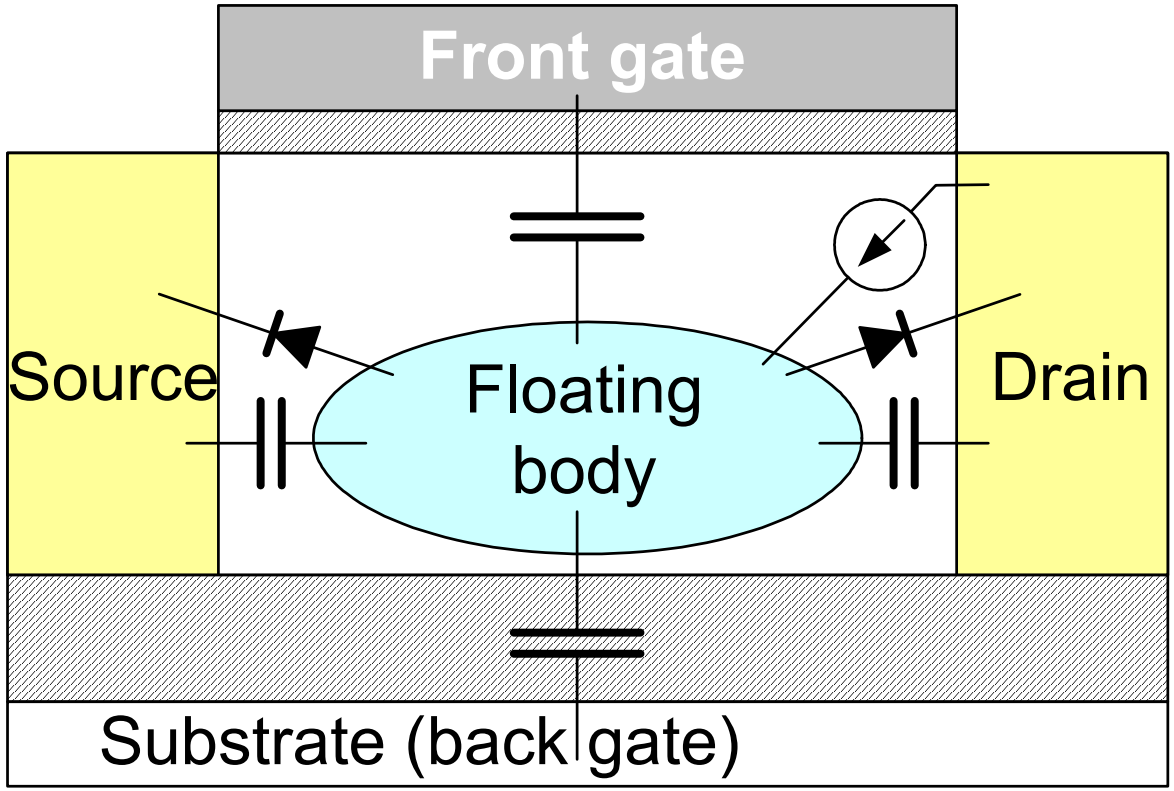
  SOI vs. bulk

  Partially depleted MOSFET

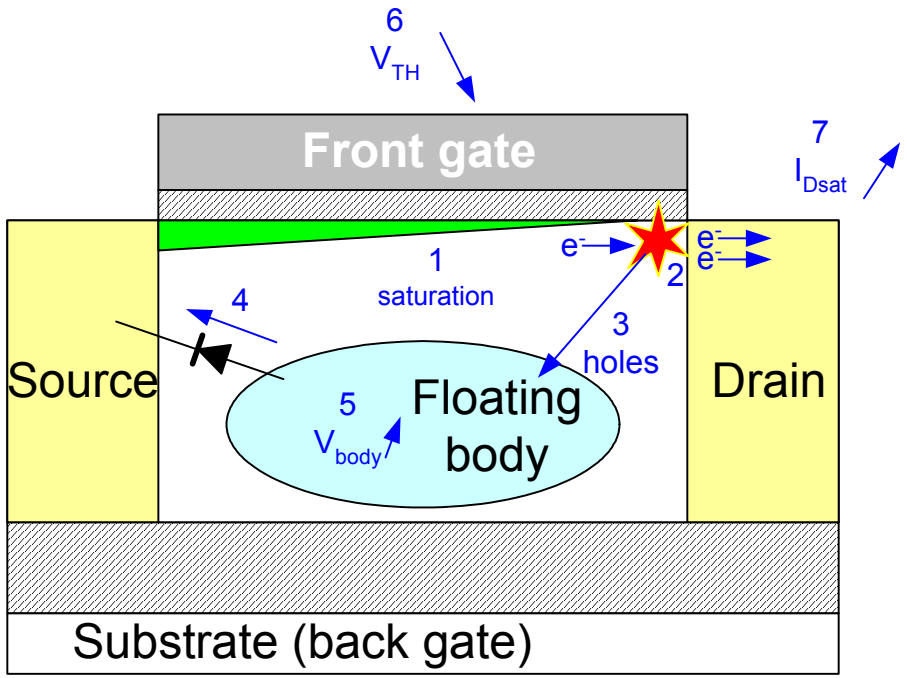
  Fully depleted MOSFET

- Particularities of IC processing using SOI wafers

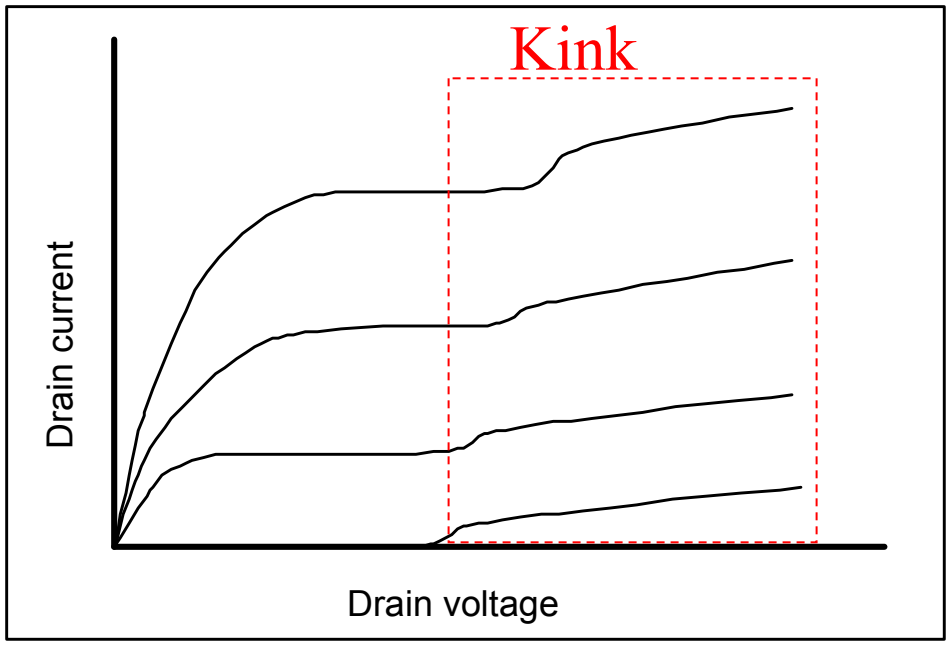
Partially Depleted SOI MOSFET: Couplings to the floating body



Partially Depleted SOI MOSFET: Kink EffectMechanism



Kink Effect
Output Characteristics



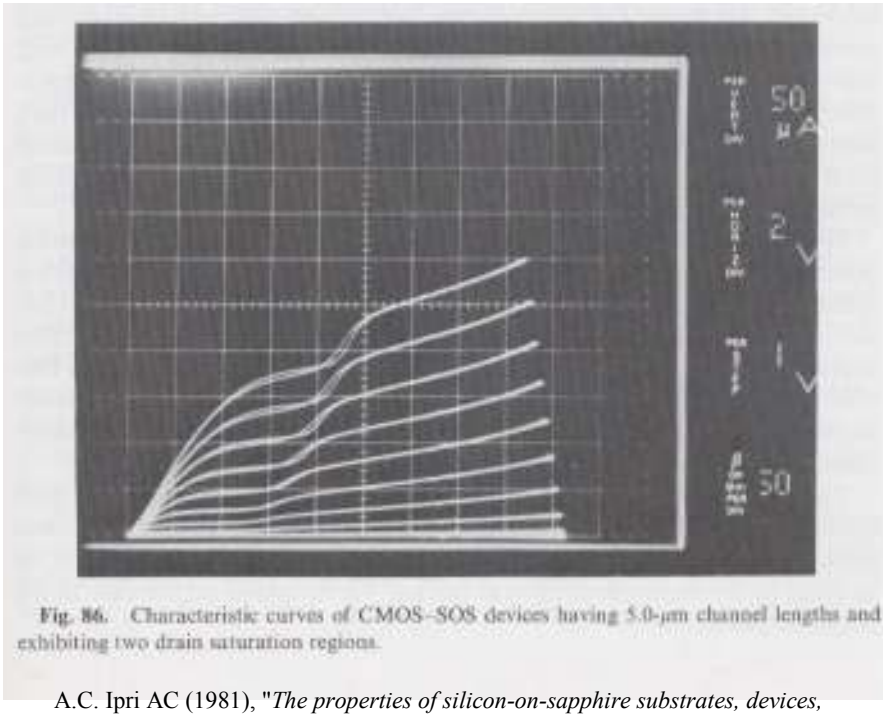


Fig. 86. Characteristic curves of CMOS–SOS devices having 5.0-μm channel lengths and exhibiting two drain saturation regions.

A.C. Ipri AC (1981), "*The properties of silicon-on-sapphire substrates, devices, and integrated circuits*", Applied Solid-State Sciences, Supplement 2, Silicon Integrated Circuits, Part A, Ed. by. D. Kahng, Academic Press, pp. 253-395, 1981

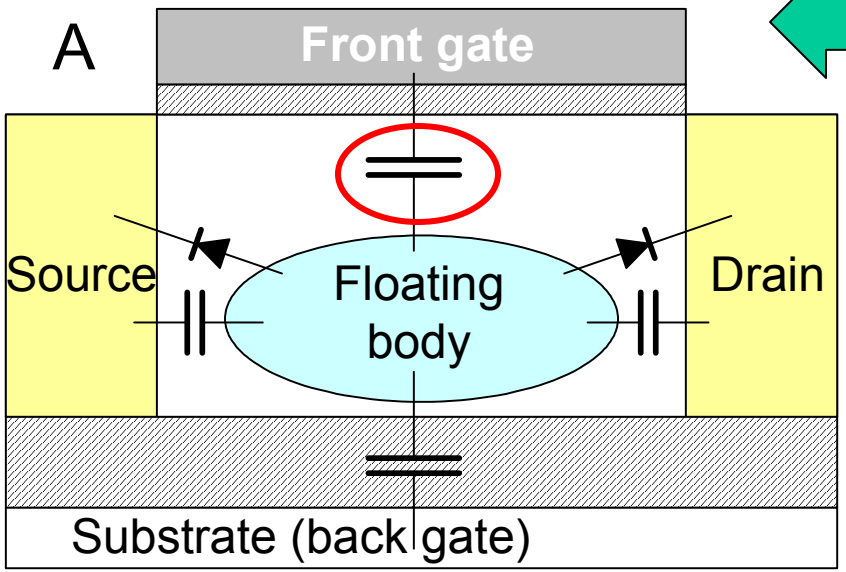
Good: - increased drain current

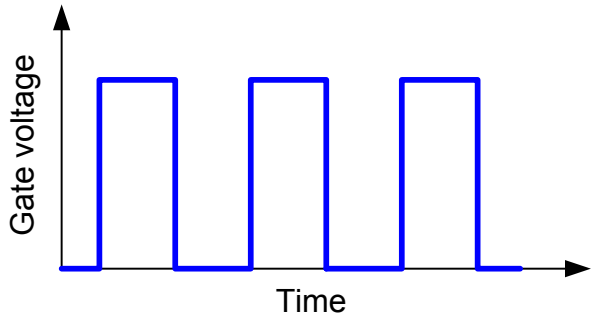
Bad: - poor output conductance, low Early voltage

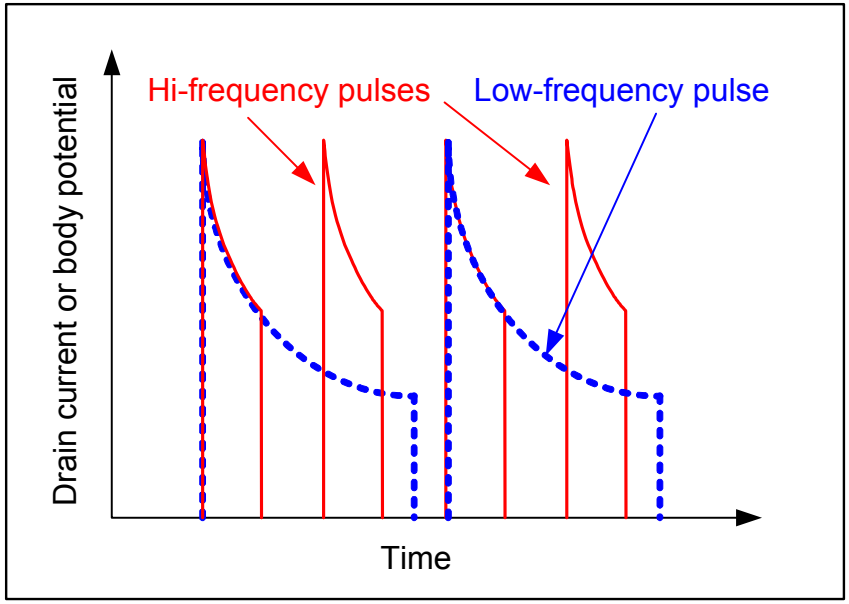
- impact ionization generates noise *

* Simoen E, Magnusson U, Rotondaro ALP. The kink-related excess low-frequency noise in silicon-on-insulator MOST's. *IEEE Transactions on Electron Devices, vol.41, no.3, March 1994, pp.330-9*

Partially Depleted SOI MOSFET Drain Current Overshoot

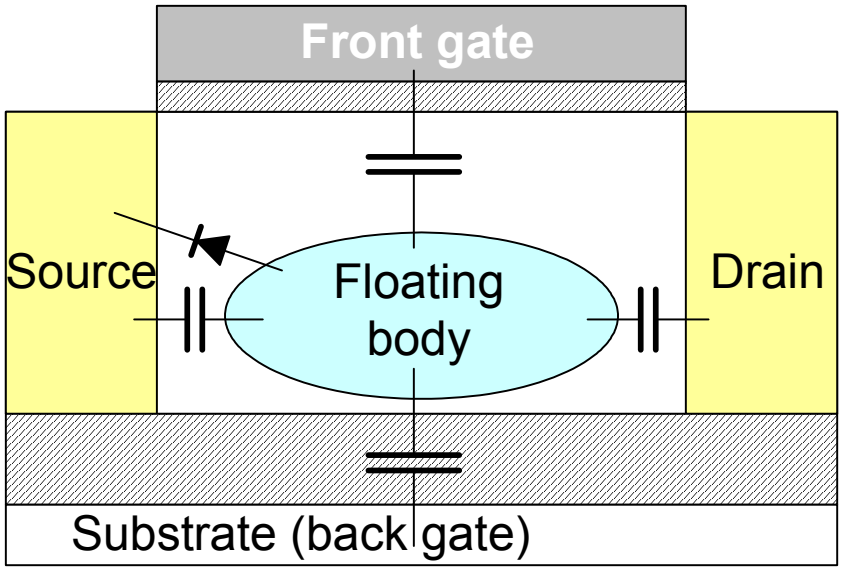


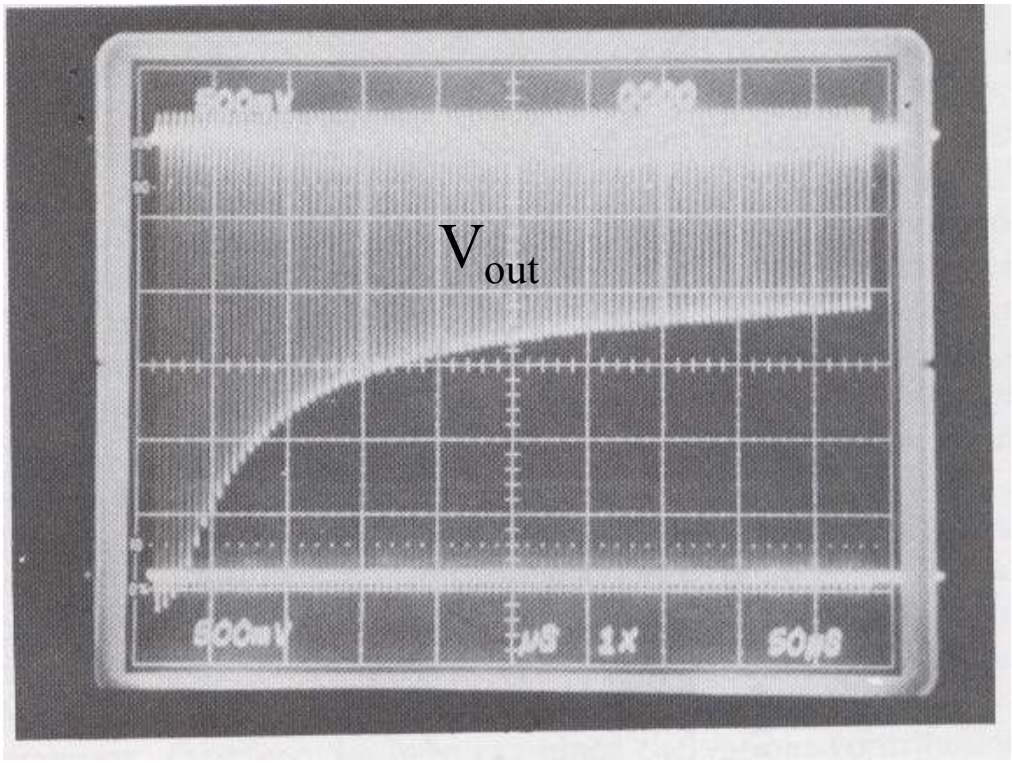


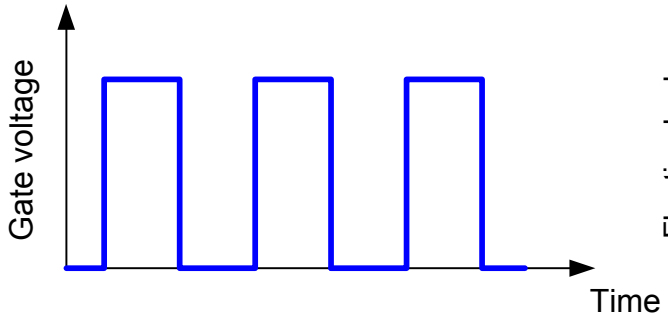


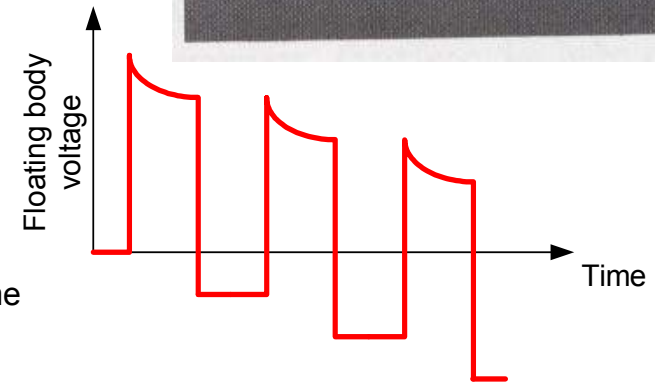
History-Dependent Output Voltage

CMOS/SOS ring oscillator (1981)



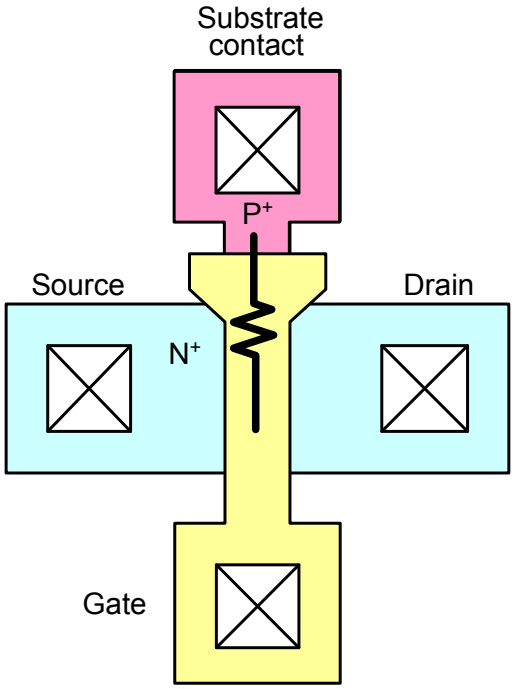




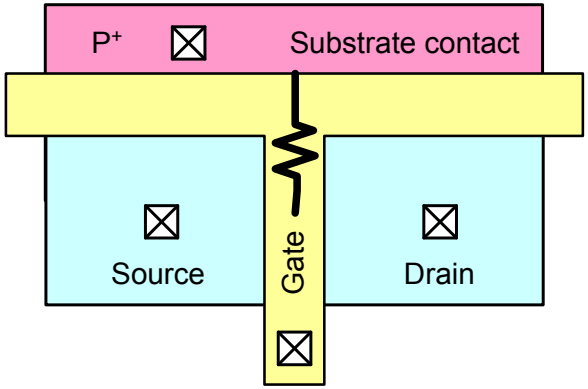


A.C. Ipri AC (1981), "*The properties of silicon-on-sapphire substrates, devices, and integrated circuits*", Applied Solid-State Sciences, Supplement 2, Silicon Integrated Circuits, Part A, Ed. by. D. Kahng, Academic Press, pp. 253-395, 1981

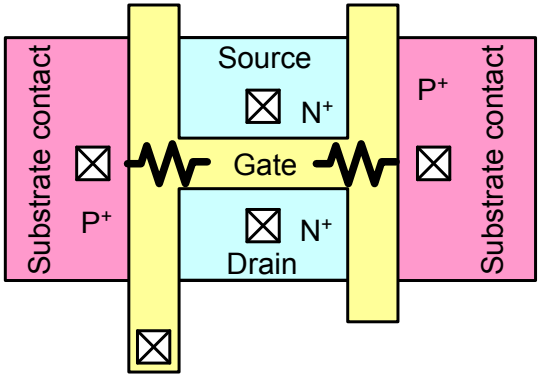
Body Contact(s) – Body Ties For Partially Depleted Devices



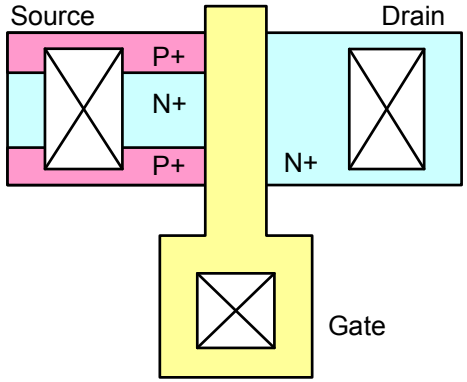
I gate



T gate



H gate



N-channel transistor with source body ties

Contact resistance is not zero: some floating-body effects subsist.

Floating Body increases Drain Current, and thus speed performance

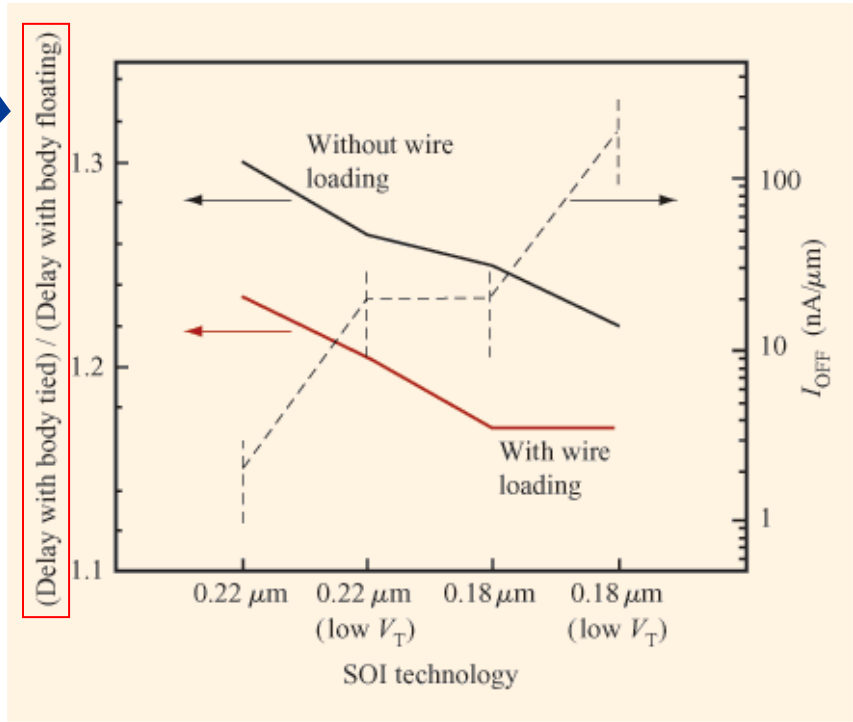


Figure 6

Simulated impact of the floating body on critical path delay for various SOI technologies, and the I_{OFF} for the corresponding technologies.

G.G. Shahidi, “SOI technology for the GHz era”, IBM Journal or Research and Development, Volume 46, Numbers 2/3,pp. 121-131, 2002

Outline

- Types of SOI MOSFETs and their basic properties

  SOI vs. bulk
  Partially depleted MOSFET
  Fully depleted MOSFET

- Particularities of IC processing using SOI wafers

Basic MOSFET equations

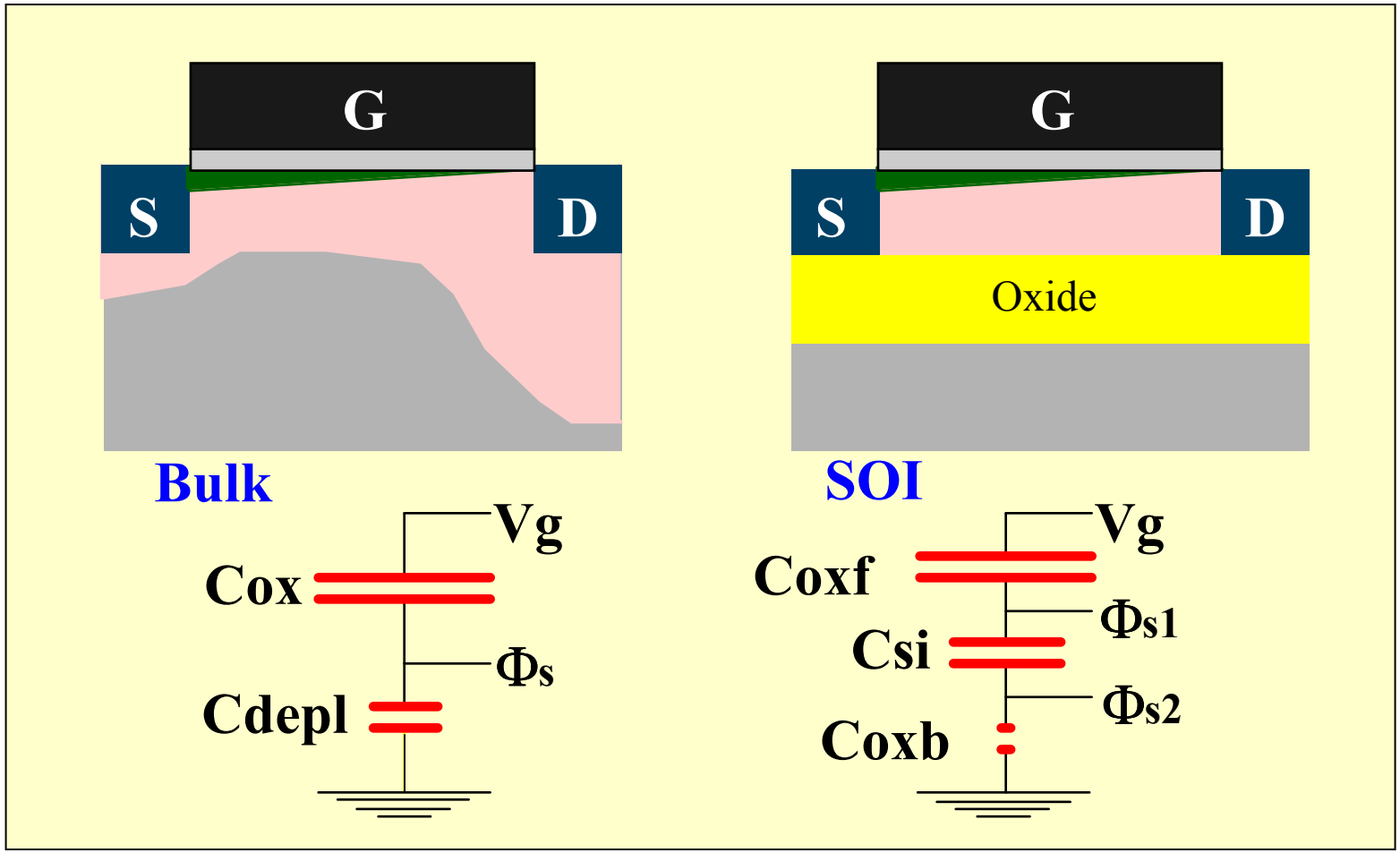
- Triode $$I_D = \mu C_{ox} \frac{W}{L}\left[(V_G - V_{TH})V_D - \frac{1}{2} n V_D^2\right]$$

- Saturation $$I_{Dsat} = \frac{1}{2n} \mu \ C_{ox} \frac{W}{L}(V_G - V_{TH})^2$$

- Subthreshold swing $$S = n \frac{kT}{q} \ln(10)$$

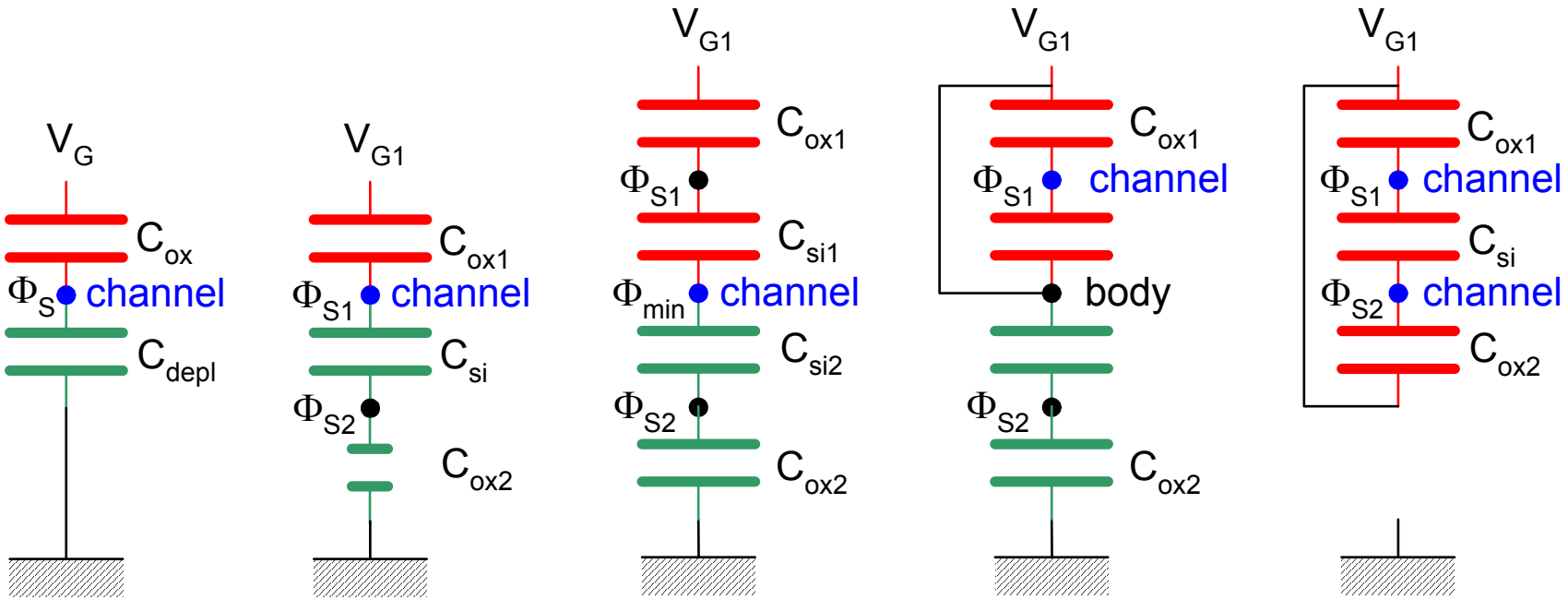
- Reduced transconducance $$\frac{g_m}{I_D} = \sqrt{\frac{2\mu C_{ox} W/L}{n I_D}}$$

Gate-to-channel coupling



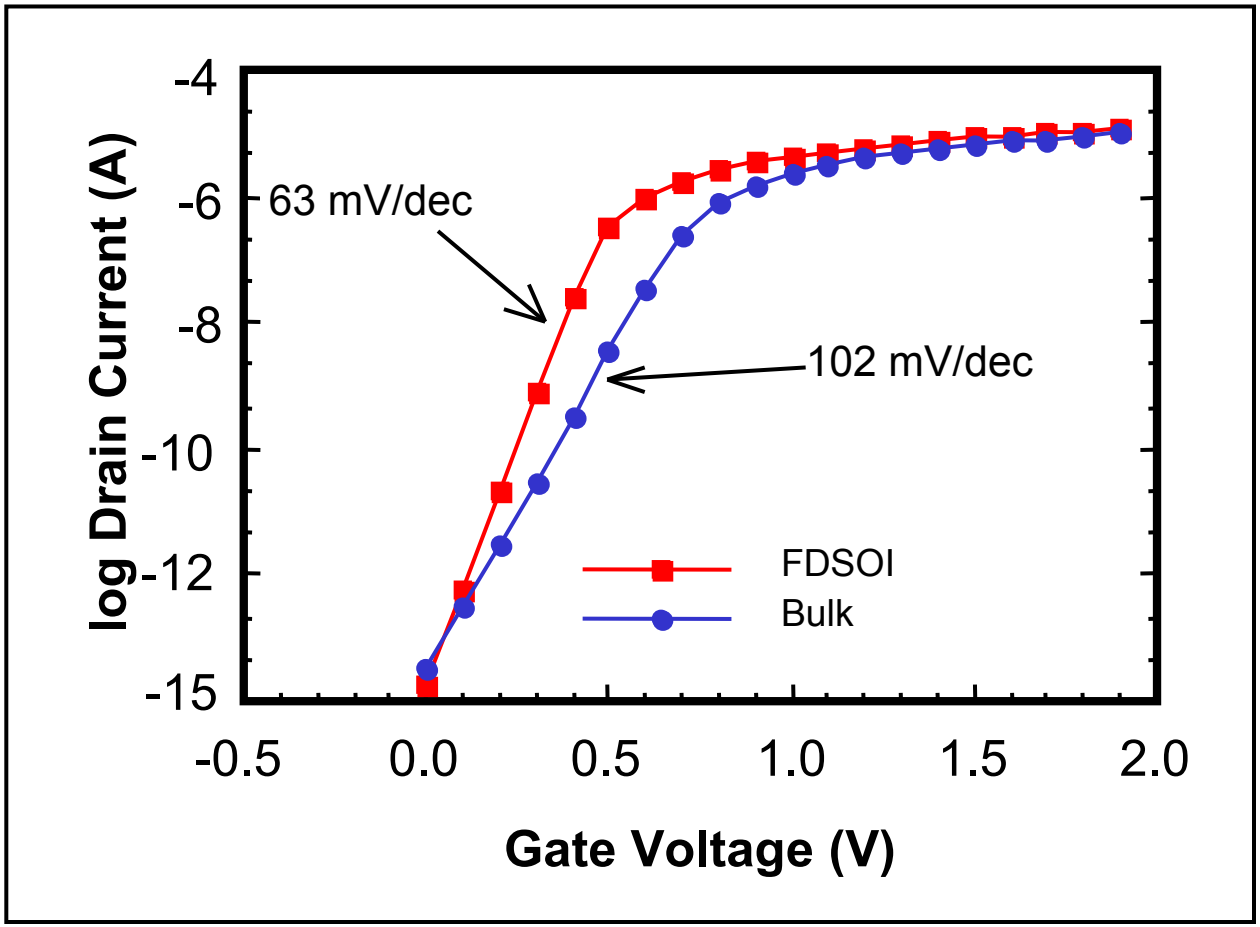
Body factor: n = …1.5… in Bulk; n = …1.05... in FDSOI

Gate-to-channel coupling and Body factor

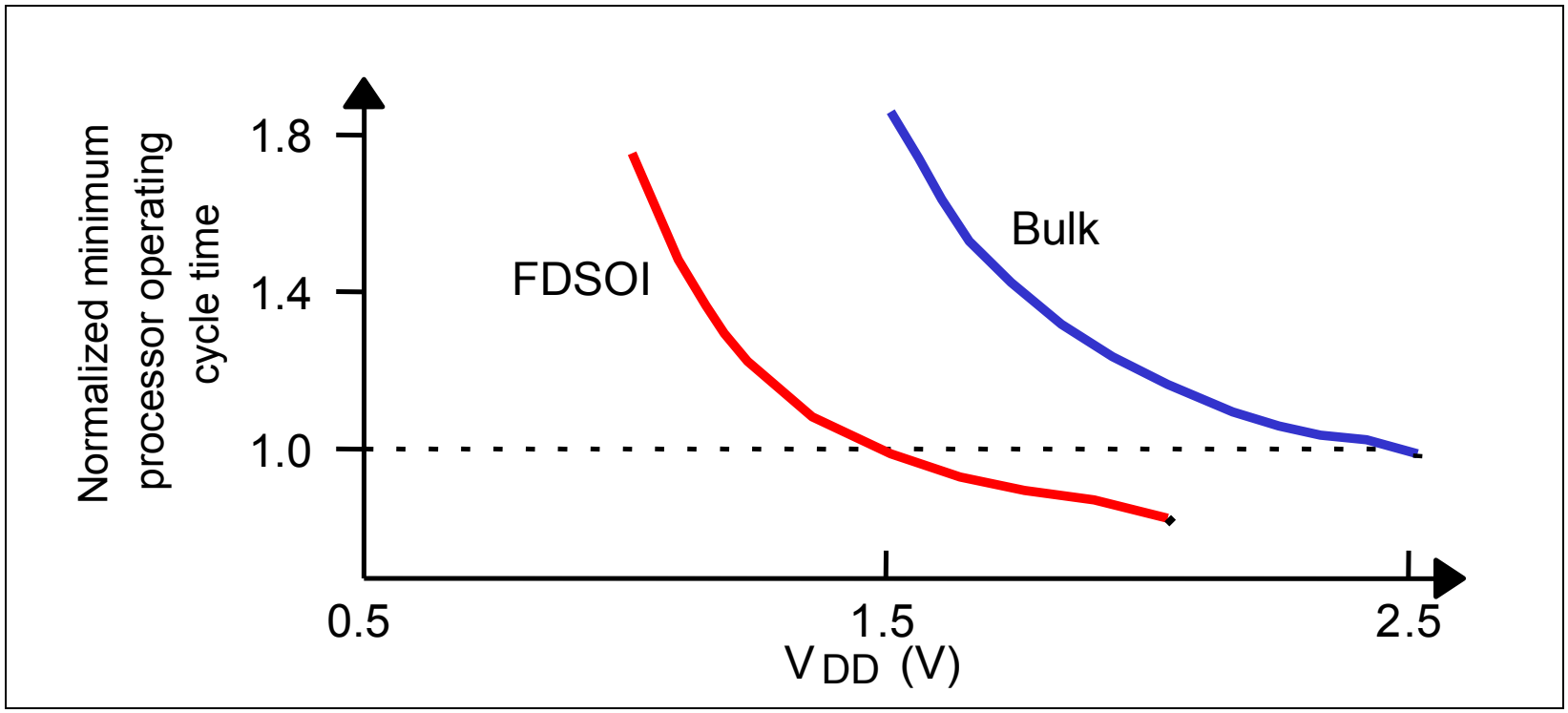


Bulk, Partially depleted SOI	Fully depleted SOI	Accumulation-mode SOI (subthreshold)	MTCMOS/ DTMOS	Double-gate FDSOI
n=1.3 ... 1.5	n=1.07	n=1.1	n=1	n=1

Subthreshold slope



Low-voltage speed advantage due to lowering V_{TH}



Cycle time in bulk and FD SOI processors *vs.* supply voltage.

Threshold voltage control

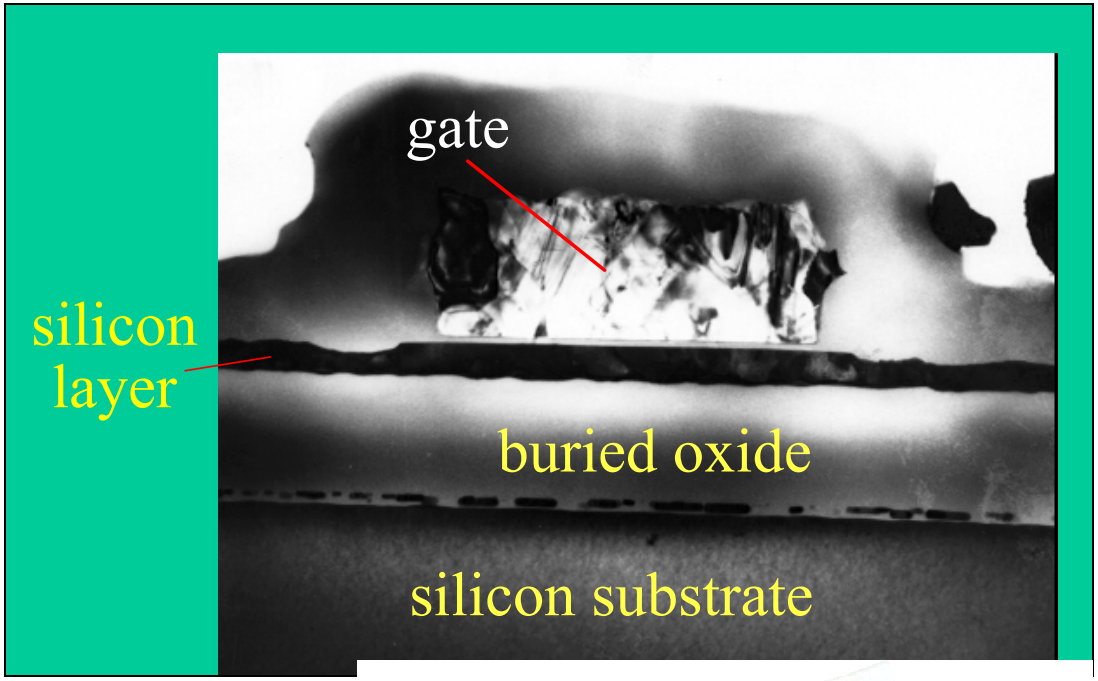
- In fully depleted SOI MOSFETs the threshold voltage is a function of silicon film thickness.

- This caused problems of V_{TH} control and reproducibility in early FDSOI; this is the main reason for today's use of PDSOI.

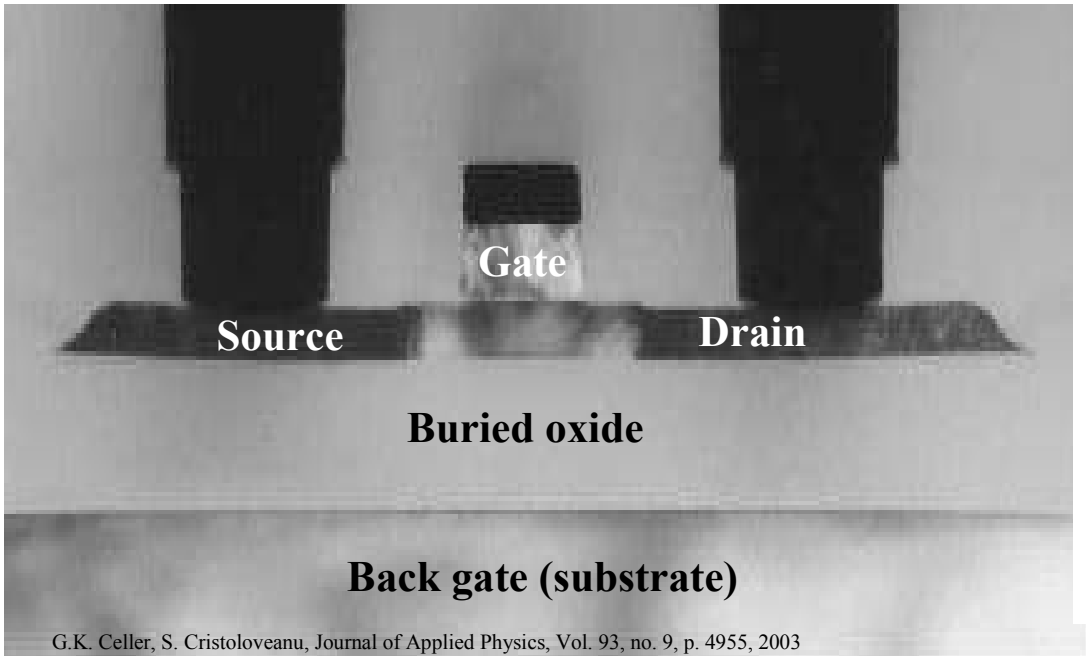
- This is no longer a problem with modern SOI materials and $\sigma V_{TH} < 10$ mV, similar to bulk is now common place.

SOI MOSFETs

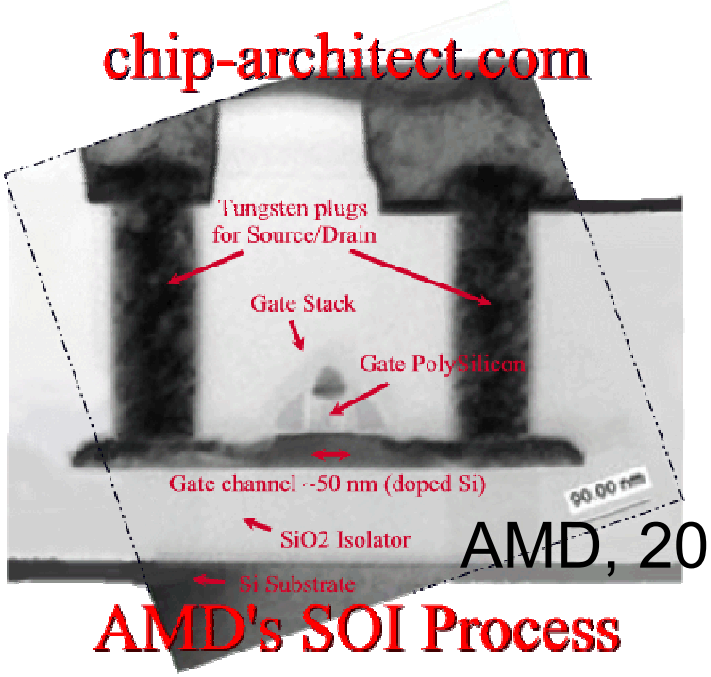
HP, 1985



Lucent, circa 2000



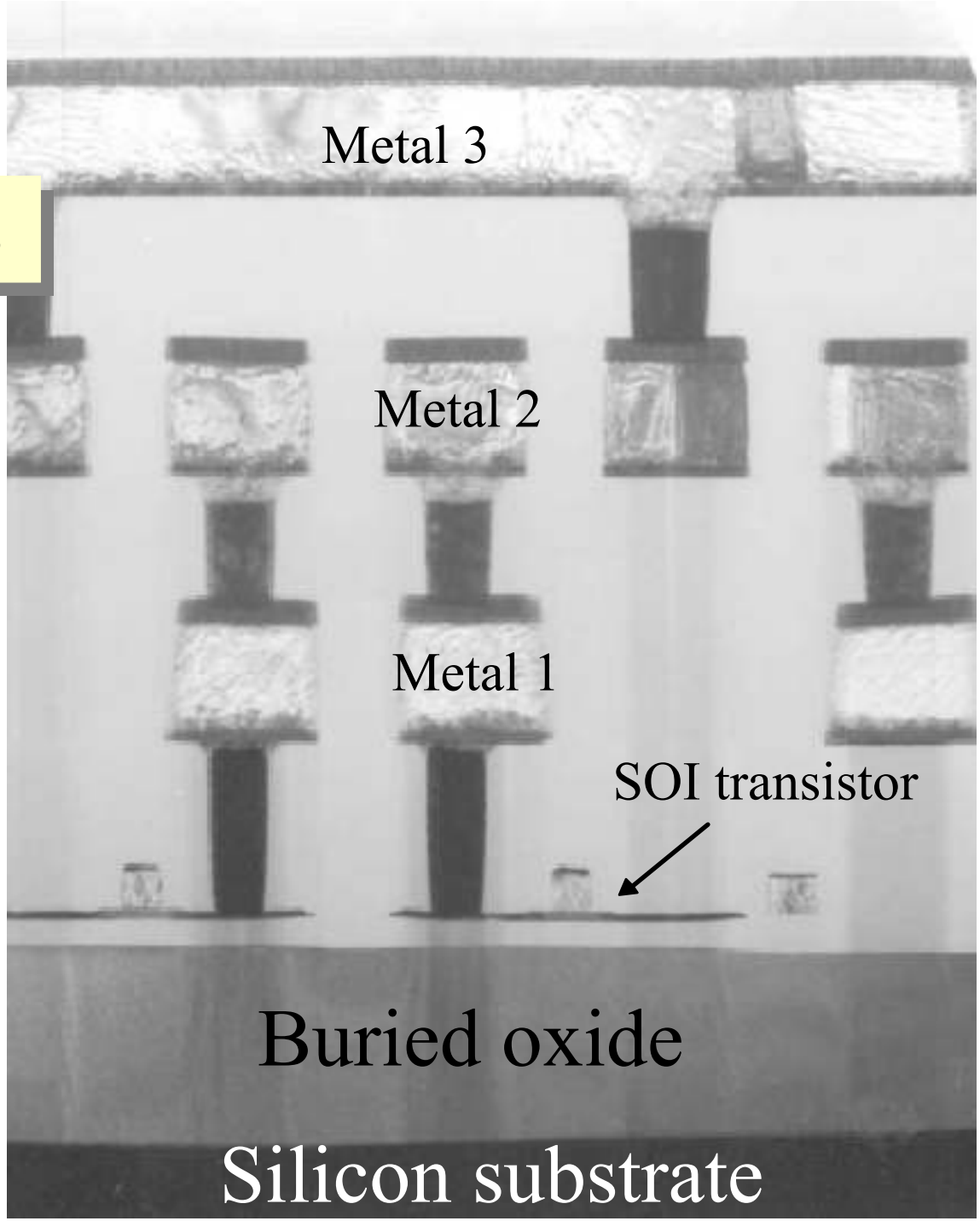
G.K. Celler, S. Cristoloveanu, Journal of Applied Physics, Vol. 93, no. 9, p. 4955, 2003



AMD, 2001

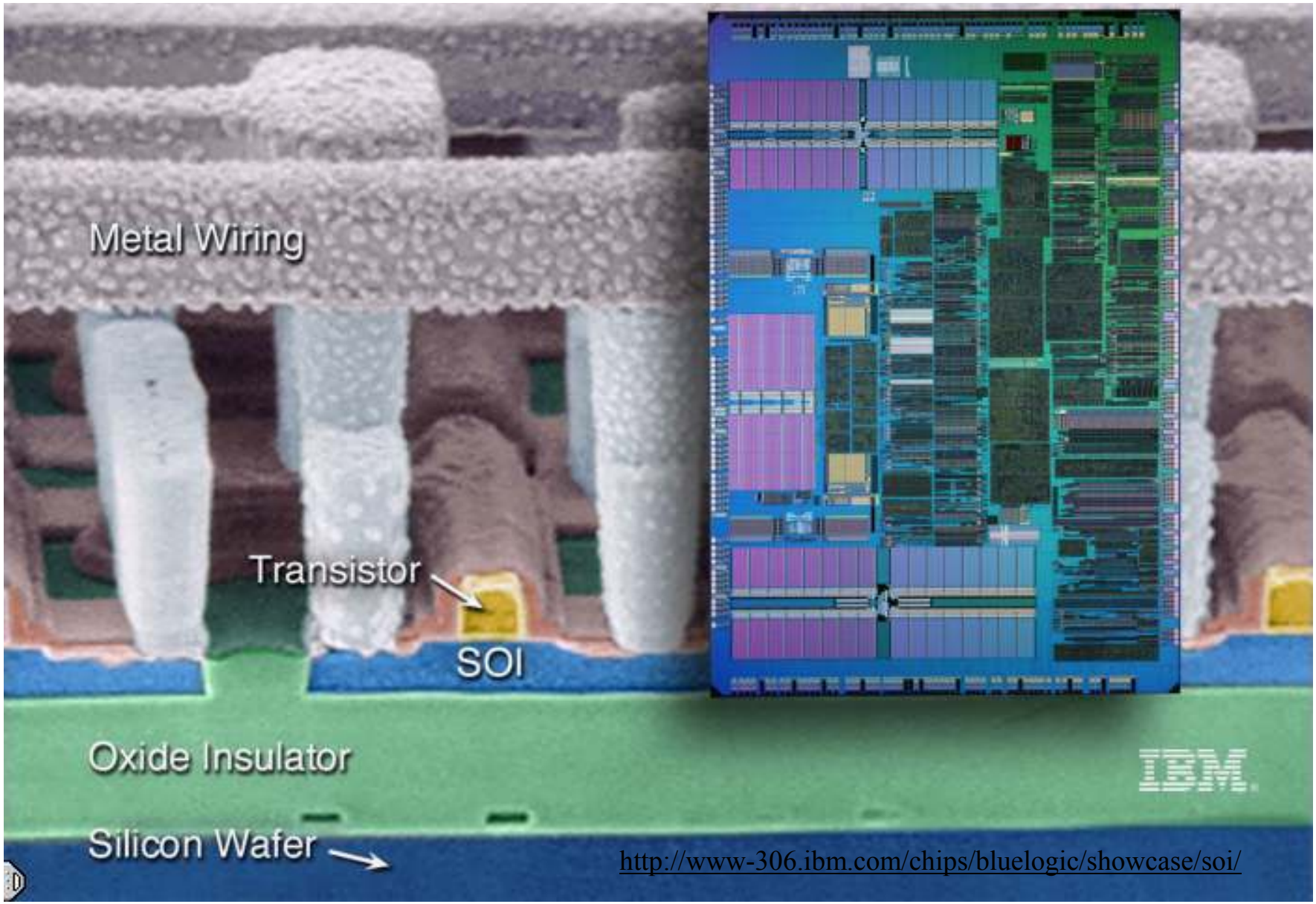
SOI MOSFETs

OKI, 2001



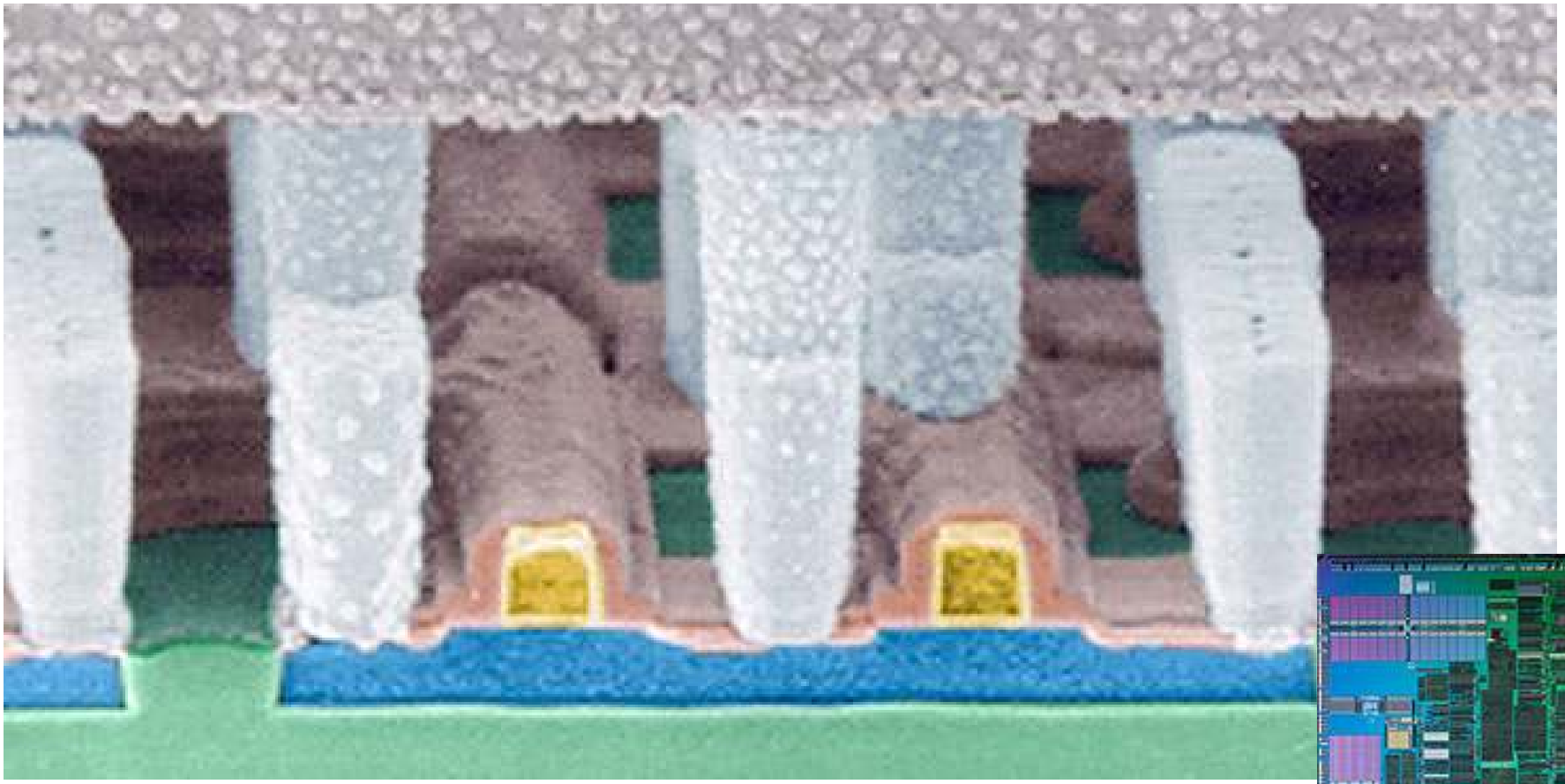
M. Itoh, Y. Kawai, S. Ito, K. Yokomizo, Y. Katakura, Y. Fukuda, F. Ishikawa, Electrochemical Society Proceedings, Vol. 2001-3, p. 331, 2001

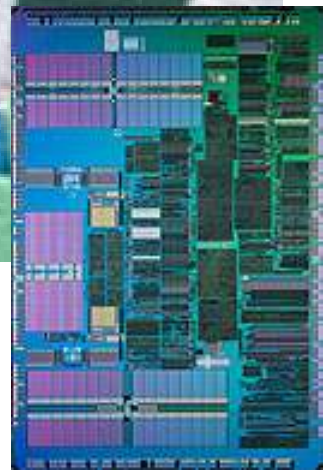
SOI CMOS at IBM (Partially Depleted)



http://www-306.ibm.com/chips/bluelogic/showcase/soi/

SOI CMOS at IBM





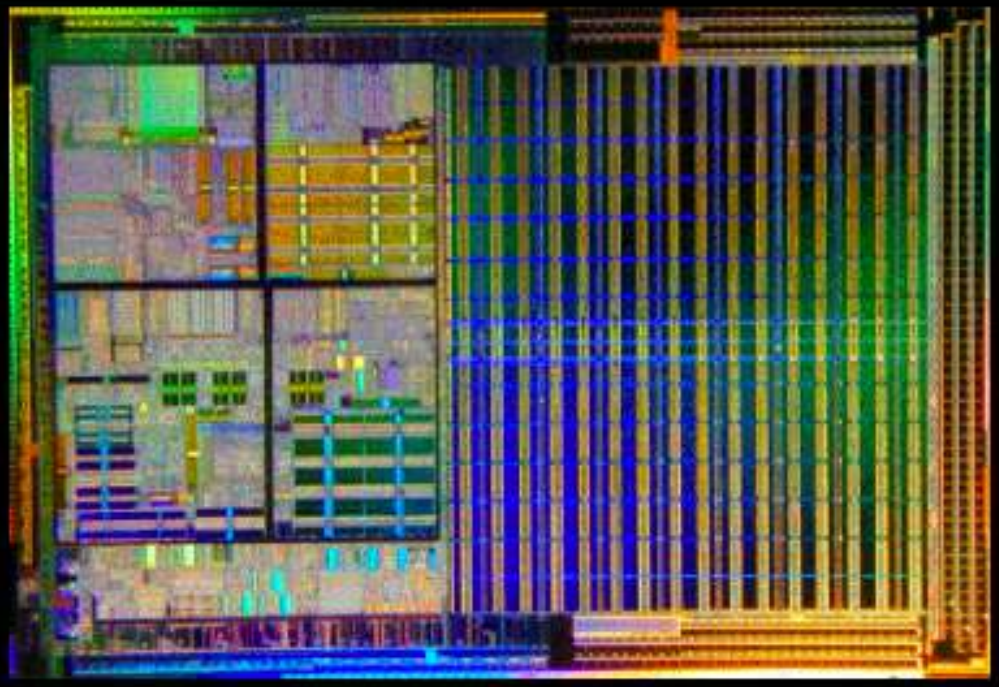
1999: IBM has built and tested SOI-based chips that have 20-35 percent (frequency) performance gain or 2-3X lower power at the same frequency as bulk CMOS technology. This is equivalent to about two years of progress in bulk CMOS technology.

http://www-306.ibm.com/chips/bluelogic/showcase/soi/

SOI CMOS at AMD (Partially Depleted)

Product Application:
AMD's Opteron X86-64

AMD

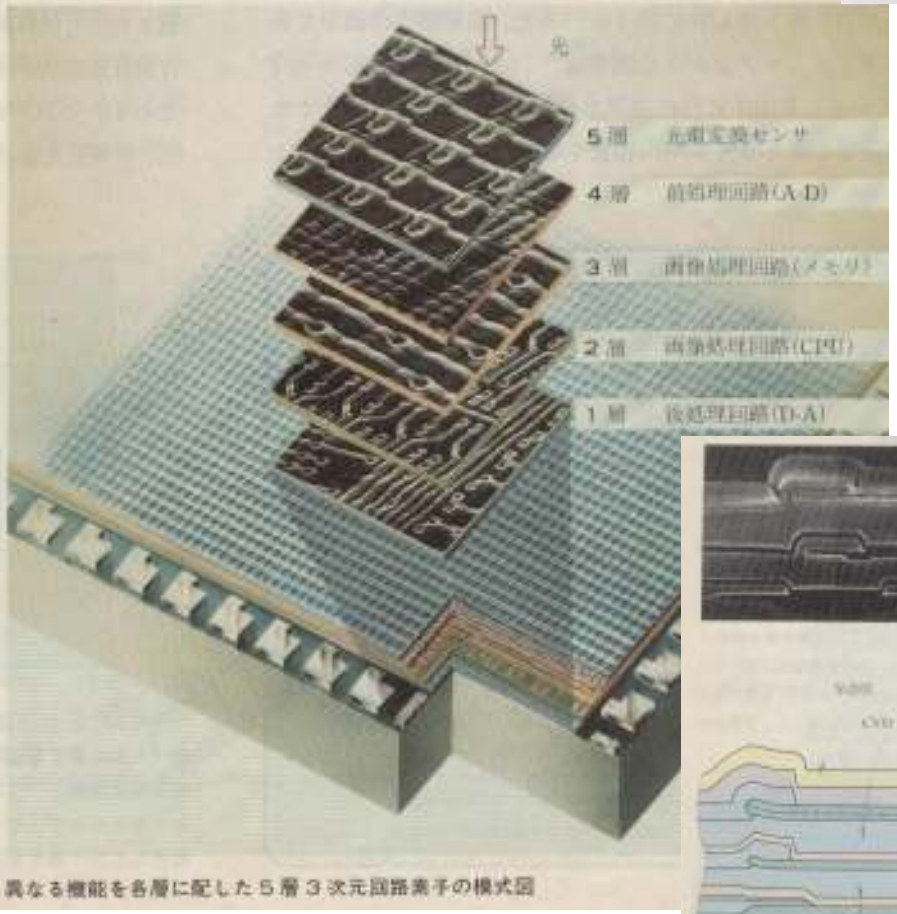


- 8th generation processor (SledgeHammer) w/ 1MB L2 Cache
- Working on 1st (SOI) silicon; > 100 million transistors
- ~180mm² on 130nm technology with Cu metallization and low k

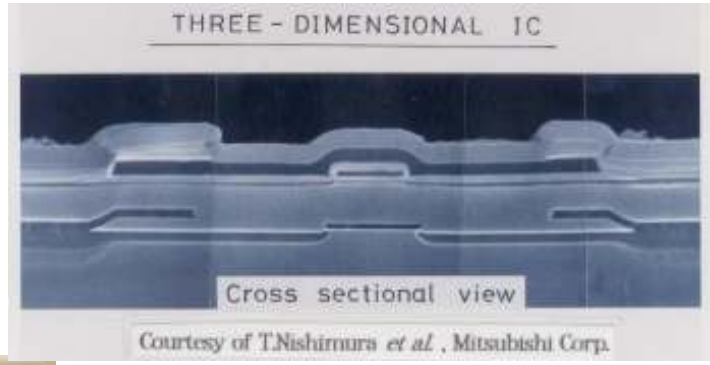
高集積，多機能デバイスとして姿が見えてきた３次元LSI

赤坂 洋一
三菱電機 LSI研究所
LSIプロセス開発第一部 参事
西村 正
同 主事

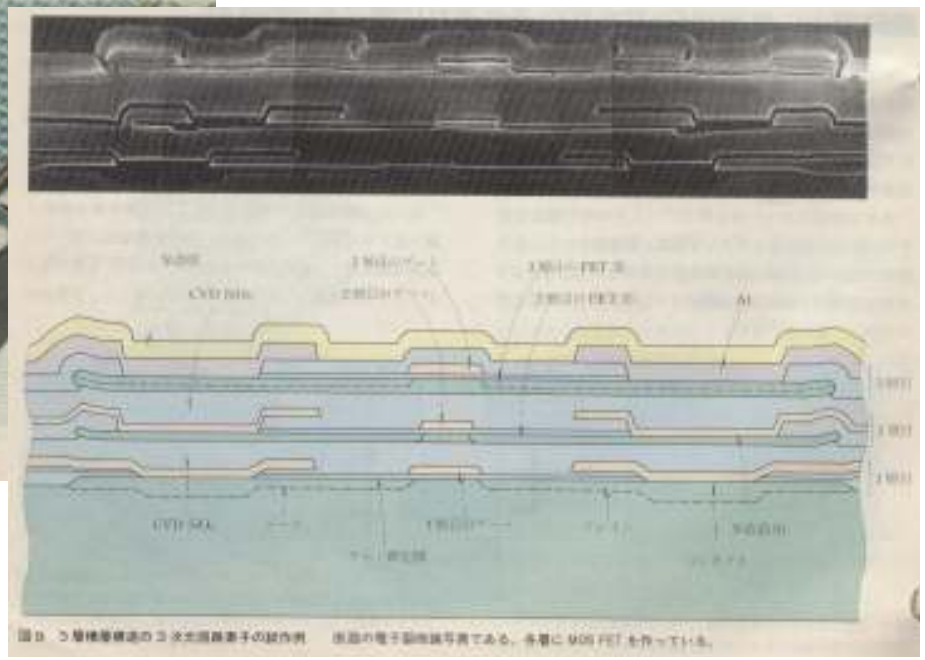
NIKKEI ELECTRONICS 1985. 10. 7



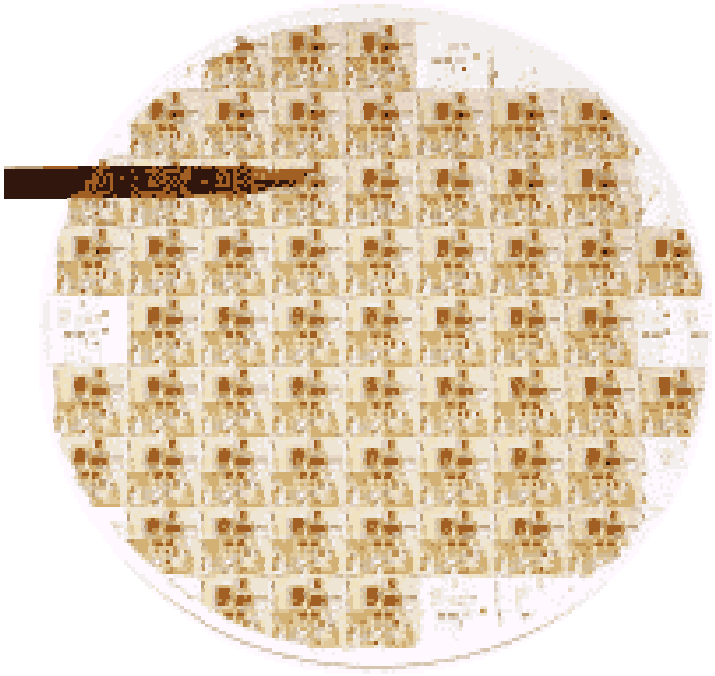
異なる機能を各層に配した５層３次元回路素子の模式図



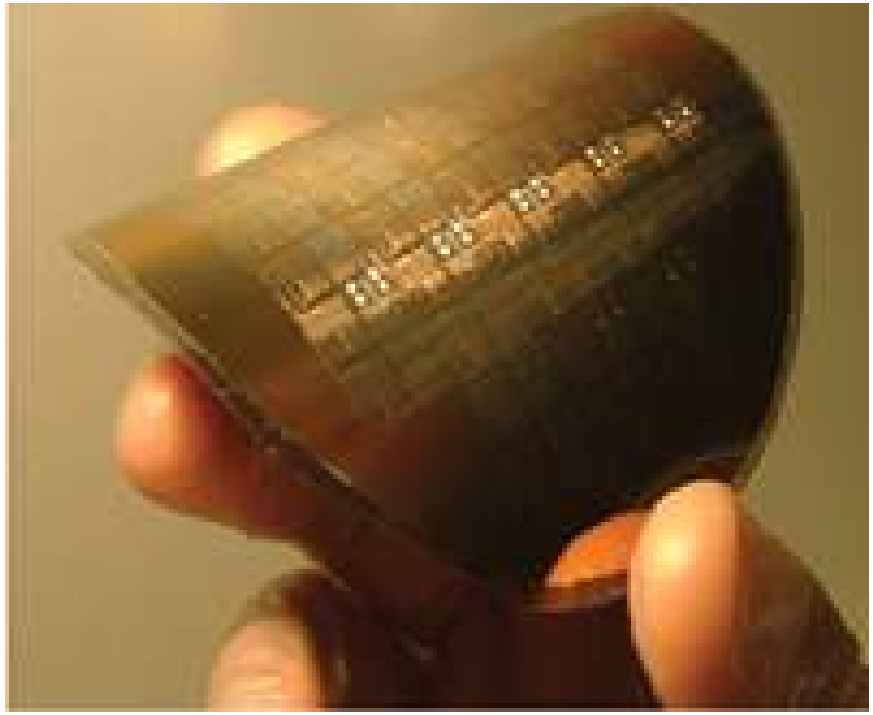
Courtesy of T.Nishimura *et al.*, Mitsubishi Corp.



Layer transfer using bonding Techniques



SOI devices transferred
onto 200 mm fused silica wafer



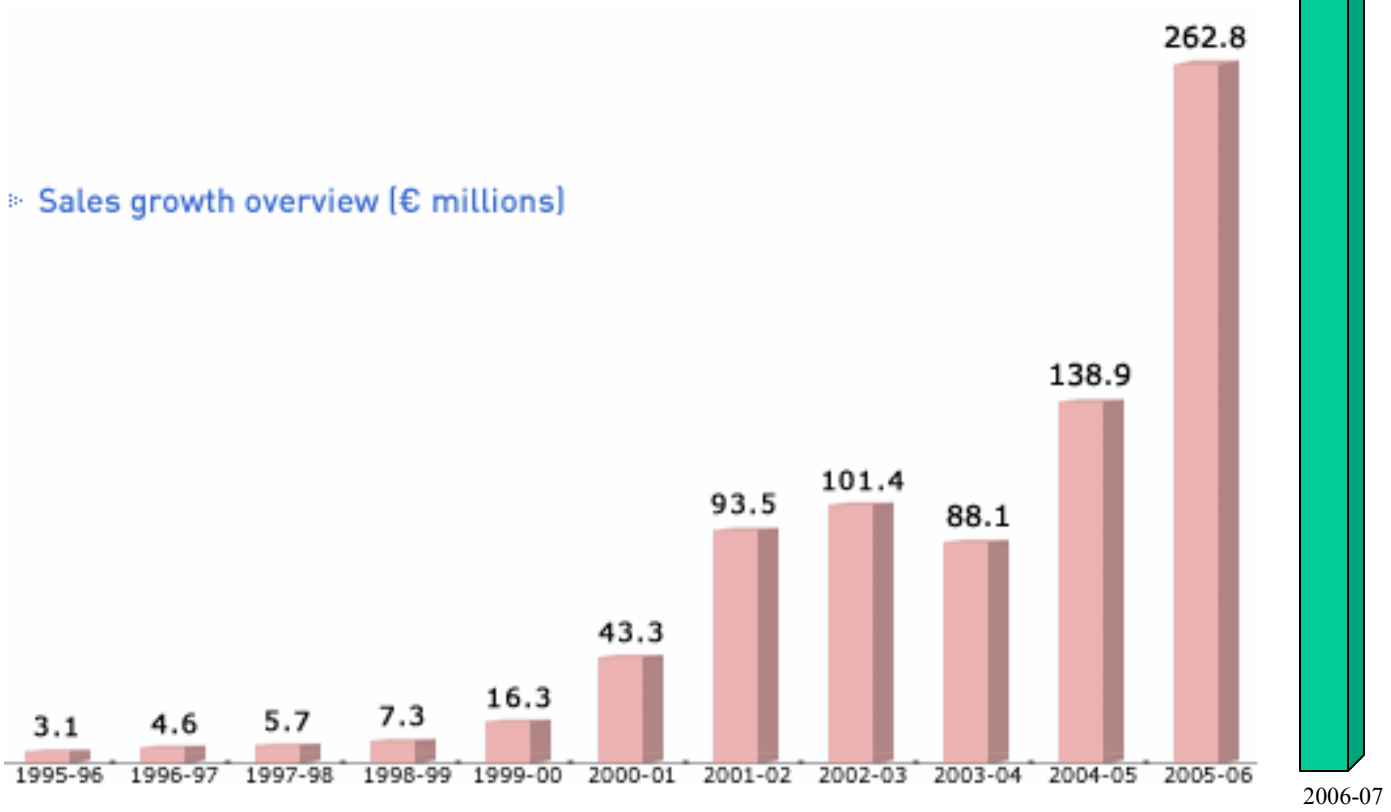
Bulk devices thinned down to 35 µm and
transferred onto a plastic film

http://www.tracit-tech.com/transfer.html

SOI chips

- All 64-bit processors made by AMD, IBM or Freescale
- The Playstation 3 and XBOX 360 processors (Sony/Toshiba/IBM)
- Countless new chips ranging from Swatch wristwatches, cell phones, audio amplifiers to low-energy light bulb ballasts

More and more companies turn to SOI
AMD, IBM, Sony/Toshiba, OKI, Philips…



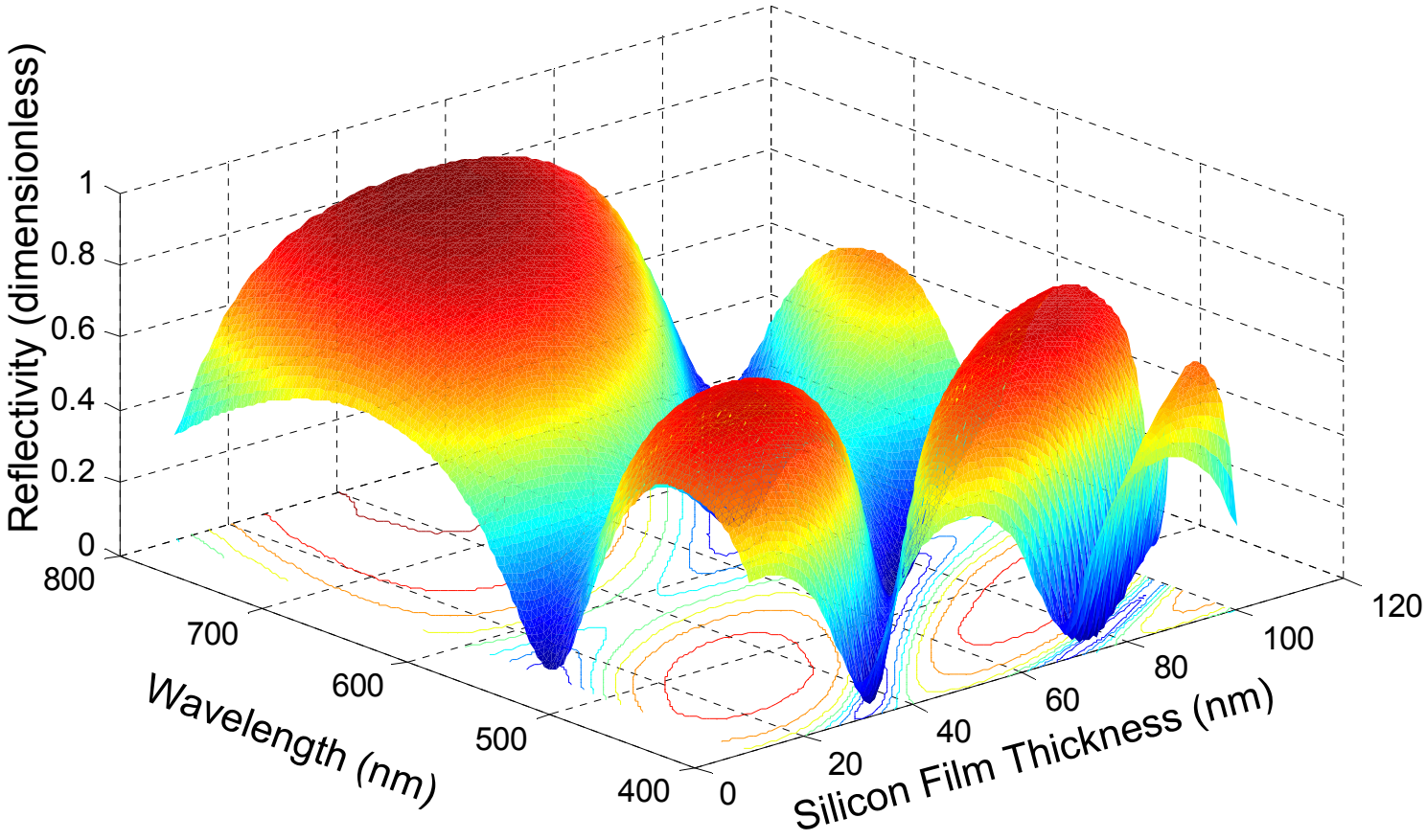
SOI wafer sales

http://soitec.com/en/finance/f_info_full06.htm

- Particularities of IC processing using SOI wafers

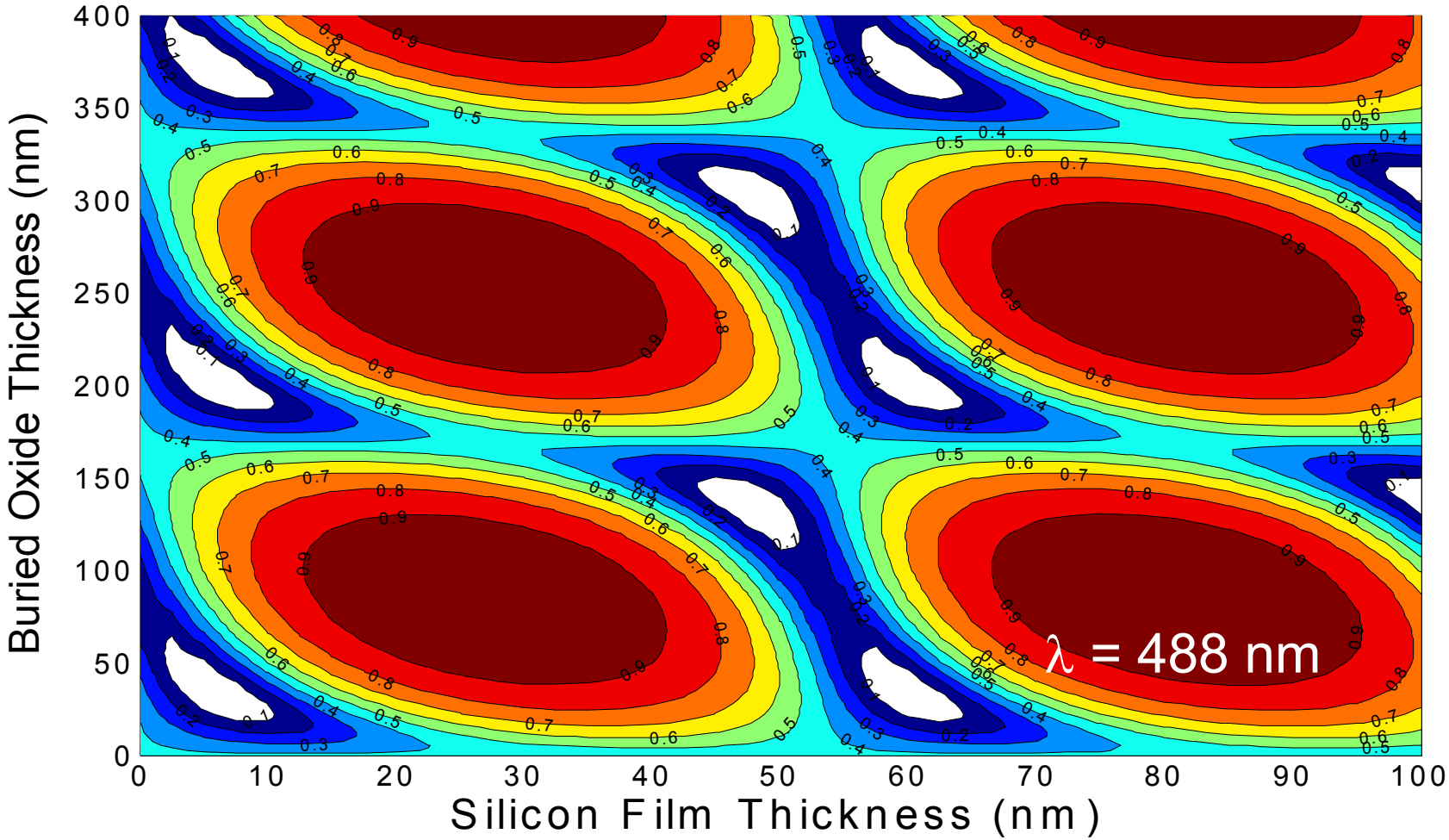
  - Evaluation of SOI wafers
  - SOI vs. bulk CMOS processing
  - Process steps and processing issues specific to SOI

Thickness measurement/Reflectometry



Reflectivity of the SOI structure as a function of wavelength and silicon film thickness. The BOX thickness is 400 nm.

Metrology issue: haze/particulate detection



Apparent particulate size depends on reflectivity !

C. Maleville, E. Neyret, L. Ecarnot, T. Barge, A.J. Auberton, Proceedings of the IEEE International SOI Conference, p. 19, 2001
C. Maleville, Electrochemical Society Proceedings Vol. 2003-05, p. 33, 2003
C. Maleville, C. Moulin, E. Neyret, Proceedings of the IEEE International SOI Conference, p. 194, 2002

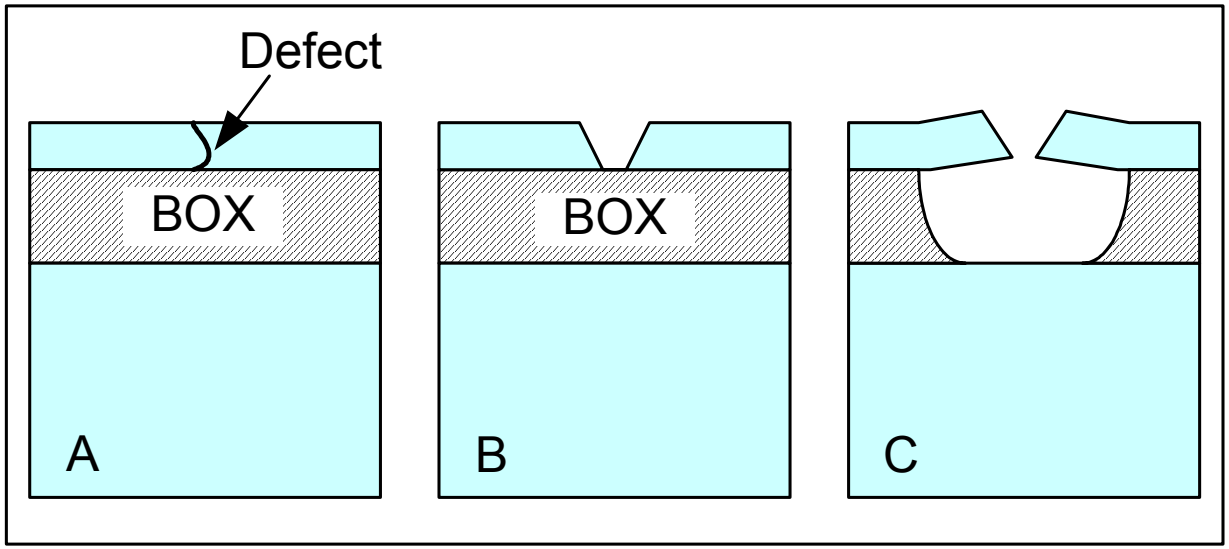
Chemical decoration of defects

Dash etch	$HF:HNO_3:CH_3COOH$ 1:3:10
Schimmel etch	HF:1M CrO_3 2:1
Secco etch	HF:0.15M $K_2Cr_2O_7$ 2:1
Stirl etch	HF:5M CrO_3 1:1
Wright etch	60ml HF:30 ml HNO_3:30 ml 5M CrO_3: 2 grams $Cu(NO_3)_2$:60 ml H_2O
Electrochemical etch	5% wt HF
Iodine etch	2M KI:0.5M I_2:2.5M HF:28.5M CH_3OH:66.5M H_2O

W.C. Dash, J. Appl. Phys, Vol. 27, p. 1993, 1956
D.G. Schimmel, J. Electrochem. Soc, Vol. 126, p. 479, 1979
F. Secco d'Aragona, J. Electrochem. Soc., Vol. 119, p. 948, 1972
E. Sirtl and A. Adler, Zeitung für Metallkunde, Vol. 52, p. 529, 1961
M. Wright Jenkins, J. Electrochem. Soc., Vol. 124, p. 757, 1977
T.R. Guilinger, M.J. Kelly, J.W. Medernach, S.S. Tsao, J.O. Steveson, and H.D.T. Jones, Proceedings of the IEEE SOS/SOI Technology Conference, p. 93, 1989
M.J. Kelly, T.R. Guilinger, J.W. Medernach, S.S. Tsao, H.D.T. Jones, and J.O. Steveson, Electrochemical Society Proceedings, Vol. 90-6, p. 120, 1990
K. Imamura, K. Daido, K. Mimegishi, H. Nakanishi, Japanese Journal of Applied Physics, Vol.16, suppl.1, p. 547, 1977
Y. Moriyasu, T. Morishita, M. Matsui, A. Yasujima, M. Ishida, Electrochemical Society Proceedings, Vol. 99-3, p. 137, 1999

Chemical decoration of defects

Problem: Si film may be too thin and is etched before defects are decorated.



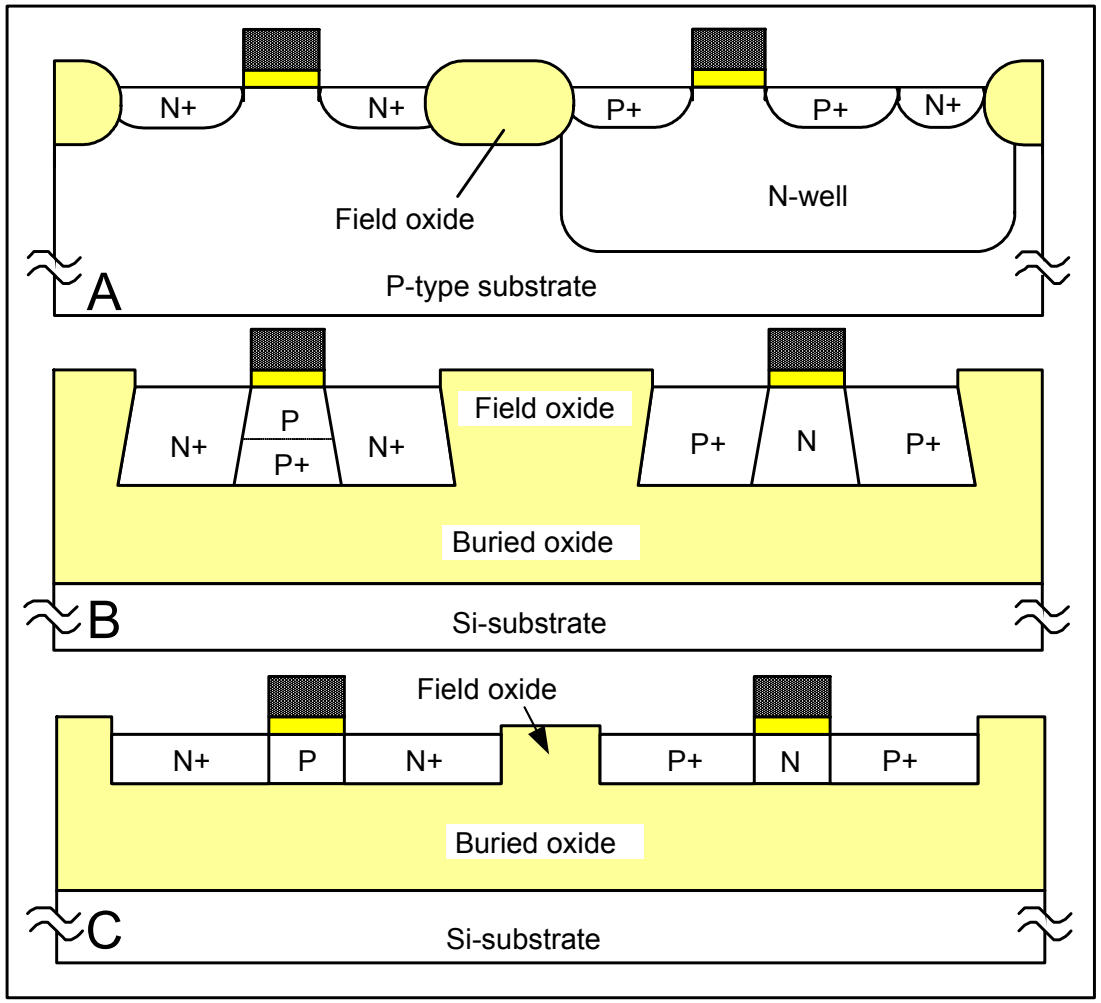
Defect in thin SOI layer (A) revealed by Secco etch (B) followed by HF etch (C)

H. Moriceau, B. Aspar, M. Bruel, A.M. Cartier, C. Morales, A. Soubie, T. Barge, S. Bressot, C. Maleville, A.J. Auberton, Electrochemical Society Proceedings, Vol. 99-3, p. 173, 1999

- Particularities of IC processing using SOI wafers

  - Evaluation of SOI wafers
  - SOI vs. bulk CMOS processing
  - Process steps and processing issues specific to SOI

CMOS Processing



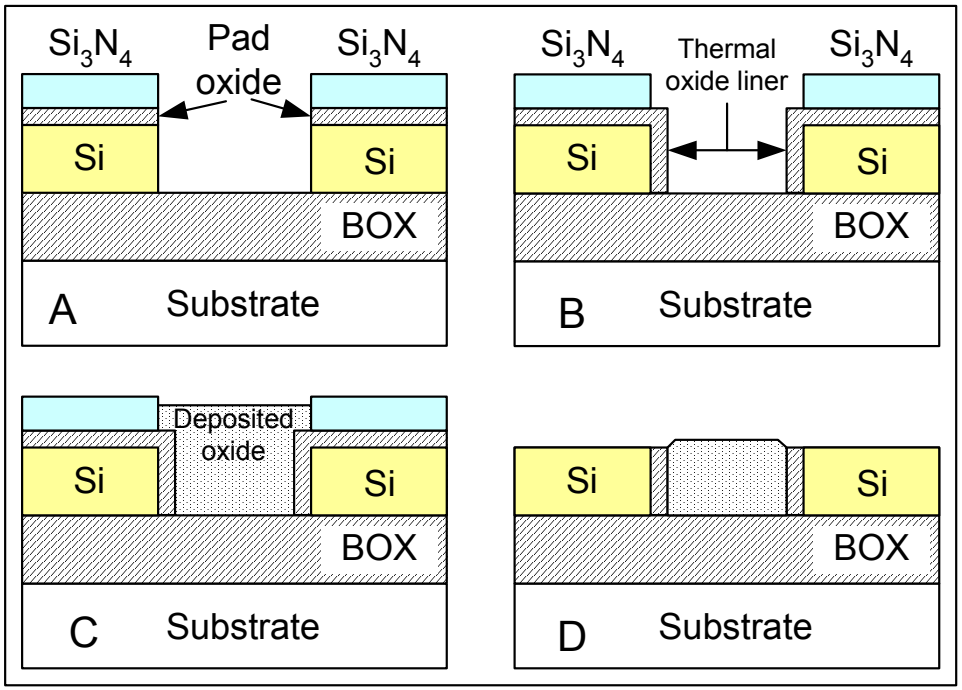
Cross-section of
A: bulk CMOS inverter
B: partially depleted SOI CMOS inverter, and
C: fully depleted SOI CMOS inverter

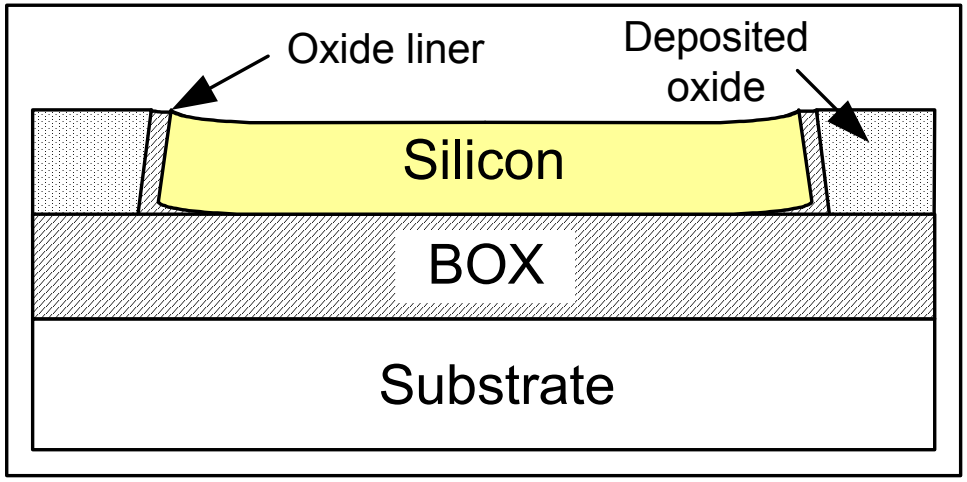
- Particularities of IC processing using SOI wafers

  - Evaluation of SOI wafers
  - SOI vs. bulk CMOS processing
  - Process steps and processing issues specific to SOI

Shallow Trench Isolation (STI)

Shallow trench isolation; A: lithography and nitride/pad oxide/silicon etch; B: growth of sidewall thermal oxide, C:CVD oxide deposition and CMP; D: nitride and pad oxide strip.

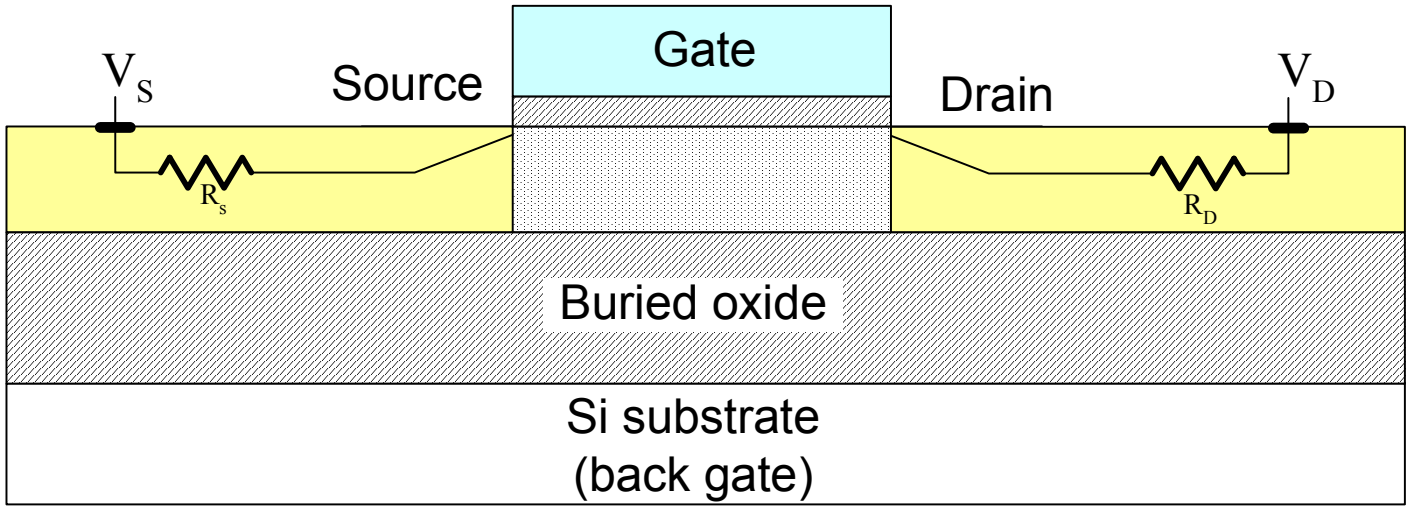




Silicon island bending caused by oxide liner growth → lower surface mobility for electrons

H. Shang, M.H. White, D.A. Adams, Proceedings of the IEEE International SOI Conference, p. 37, 2002

Source and drain resistance

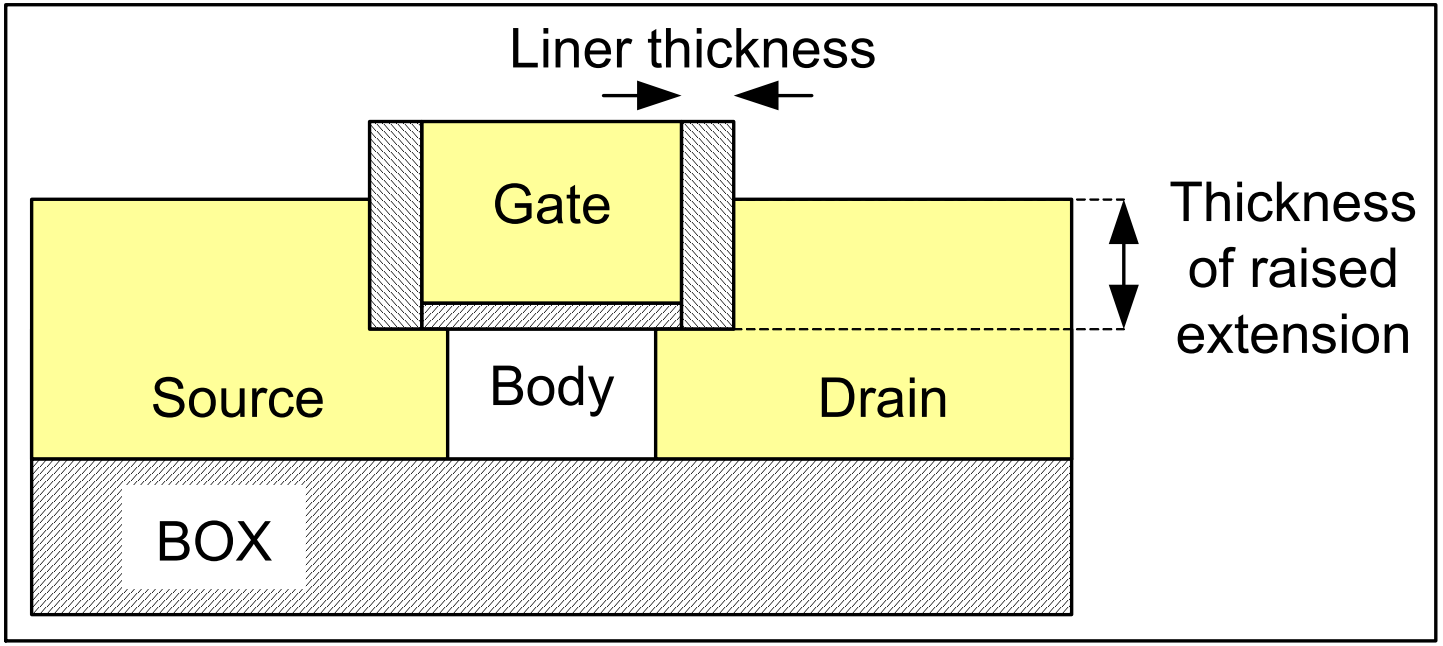


- S&D resistance become important as silicon film thickness is reduced.

- Solutions: elevated S&D
  full or partial S&D silicidation
  metal (Schottky) S&D

Ref: 41-43

Elevated source and drain

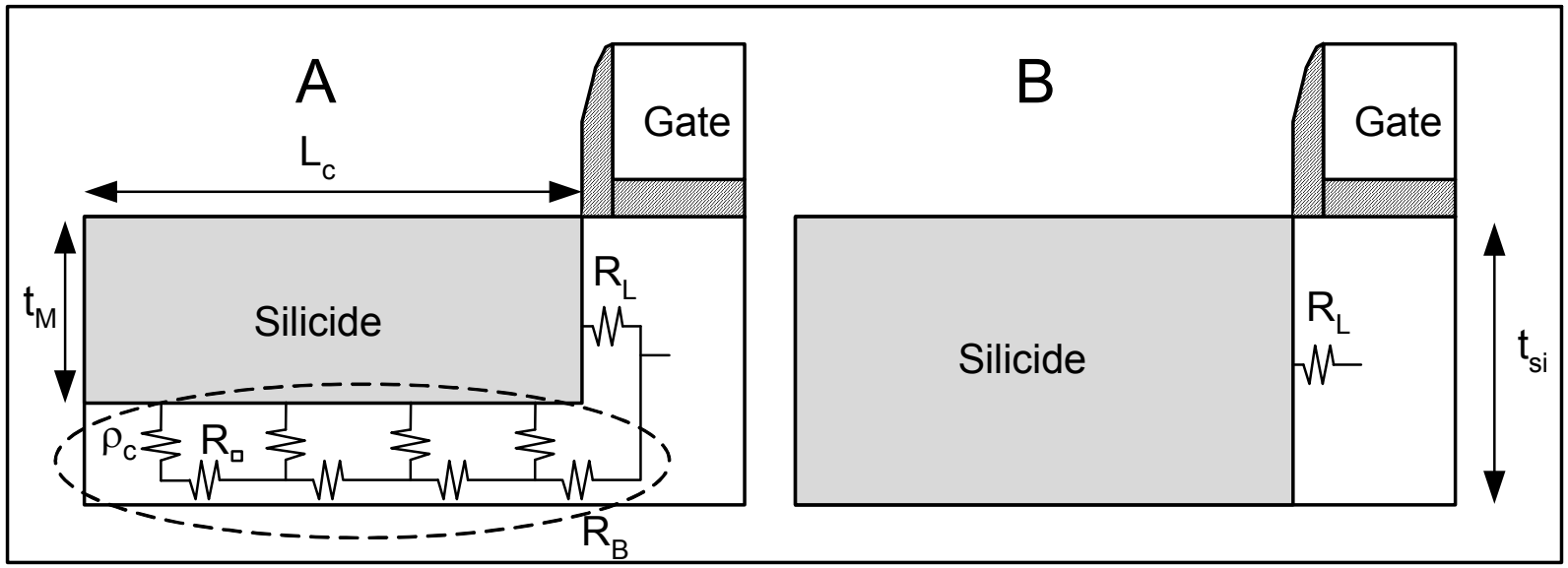


A. Vandooren, A. Barr, L. Mathew, T.R. White, S. Egley, D. Pham, M. Zavala, S. Samavedam, J. Schaeffer, J. Conner, B.Y. Nguyen, B.E. White, Jr., M.K. Orlowski, J. Mogab, IEEE Electron Device Letters, Vol. 24, no. 5, p. 342, 2003

S.S. Kim, T.H. Choe, H.S. Rhee, G.J. Bae, K.W. Lee, N.I. Lee, K. Fujihara, H.K. Kang, J.T. Moon, Proceedings of the IEEE International SOI Conference, p. 74, 2000

J.L. Egley, A. Vandooren, B. Winstead, E. Verret, B. White, B.Y. Nguyen, Electrochemical Society Proceedings, Vol. 2003-05, p. 307, 2003

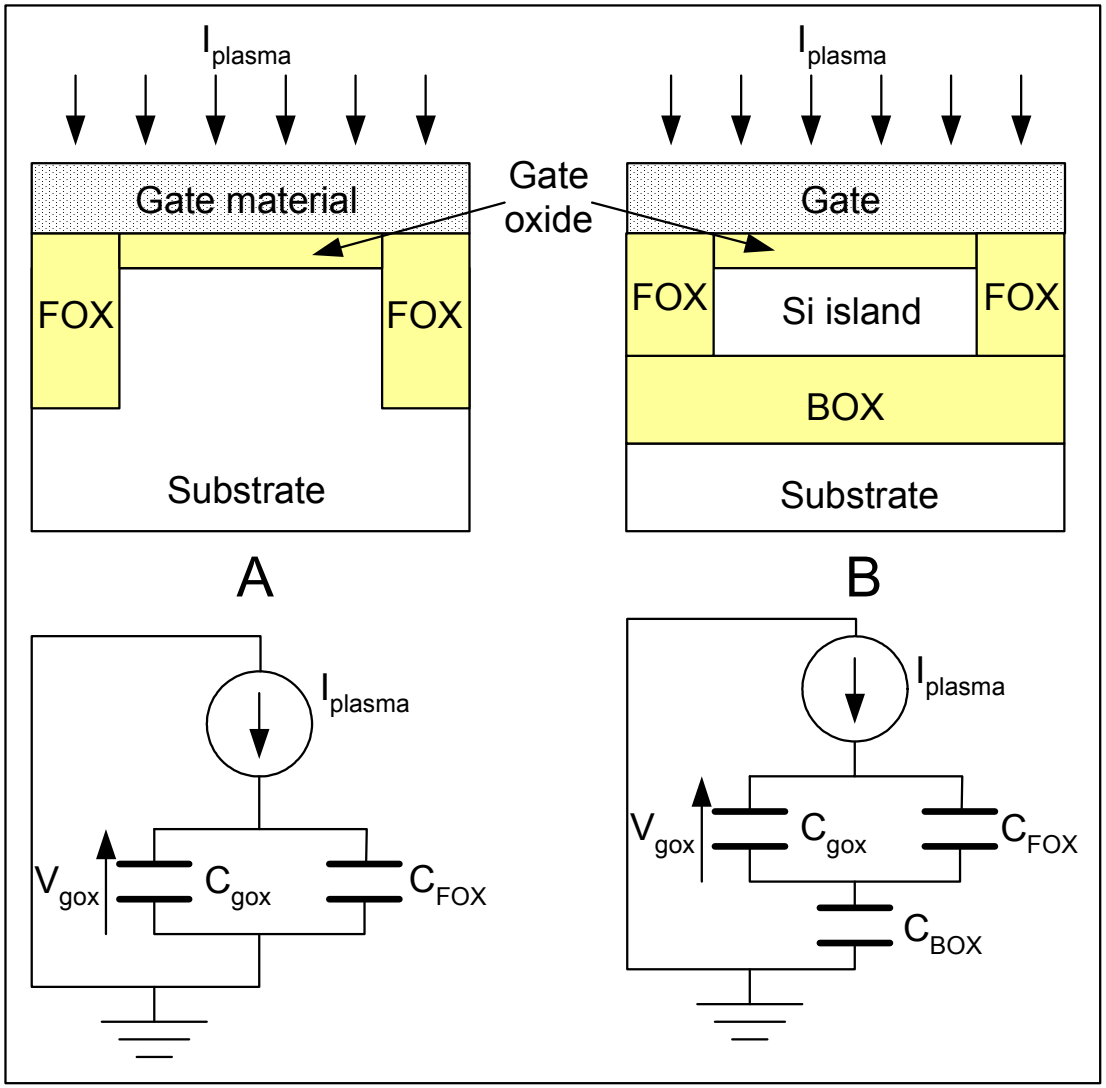
Silicided source and drain



Current flow path in a silicide junction. A: the silicide is thinner than the silicon film; B: the silicide reaches the BOX

H.I. Liu, J.A. Burns, C.L. Keast, P.W. Wyatt, IEEE Transactions on Electron Devices, Vol. 45, no. 5, p. 1099, 1998
T. Ichimori, N. Hirashita, 2000 IEEE International SOI Conference. Proceedings, p. 72, 2000
T. Ichimori, N. Hirashita, Japanese Journal of Applied Physics Part 1, Vol. 40, no. 4B, p. 2881, 2001

Reduced antenna effect

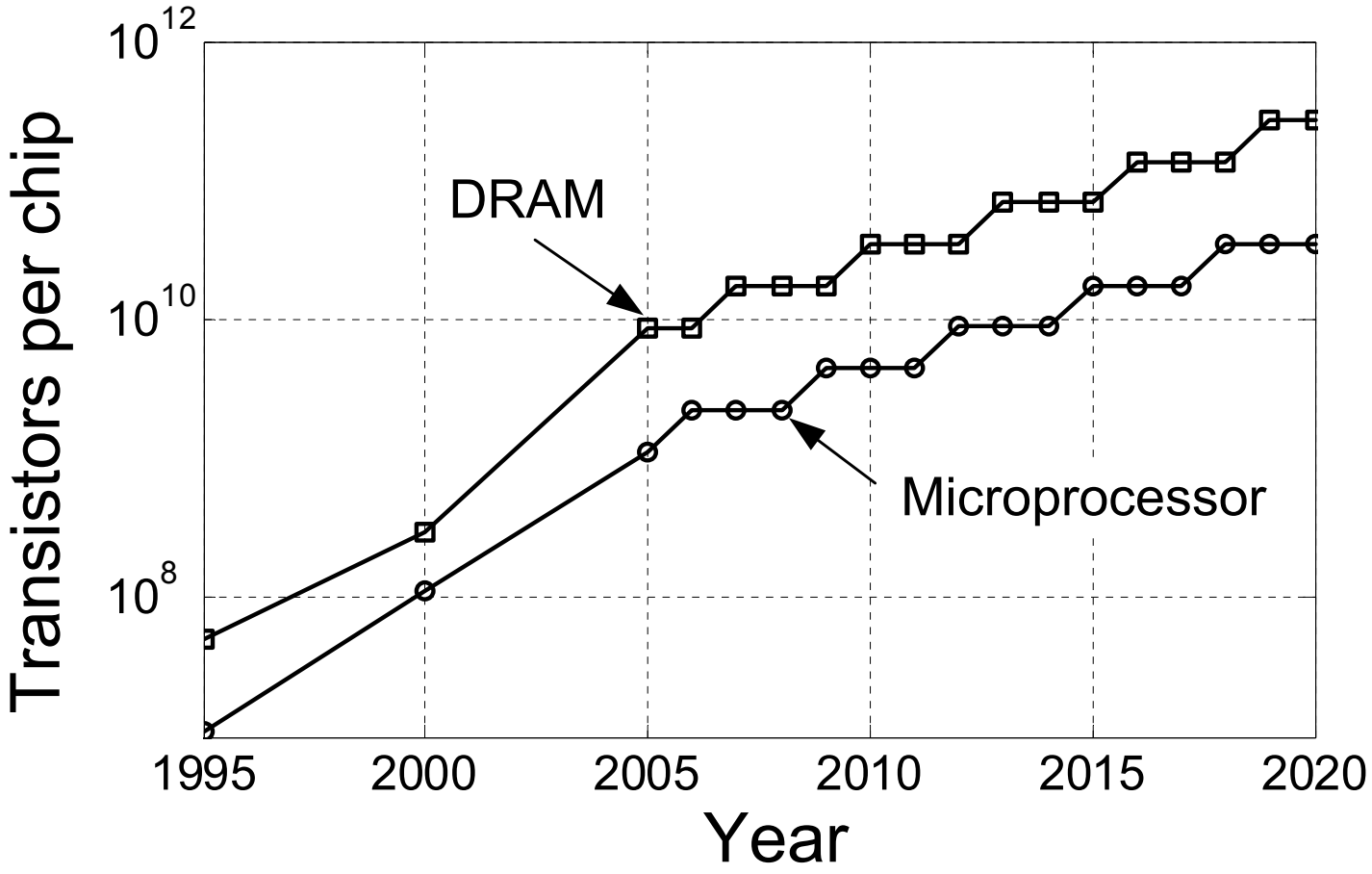


Antenna effect during plasma etch step in bulk (A) and SOI (B)

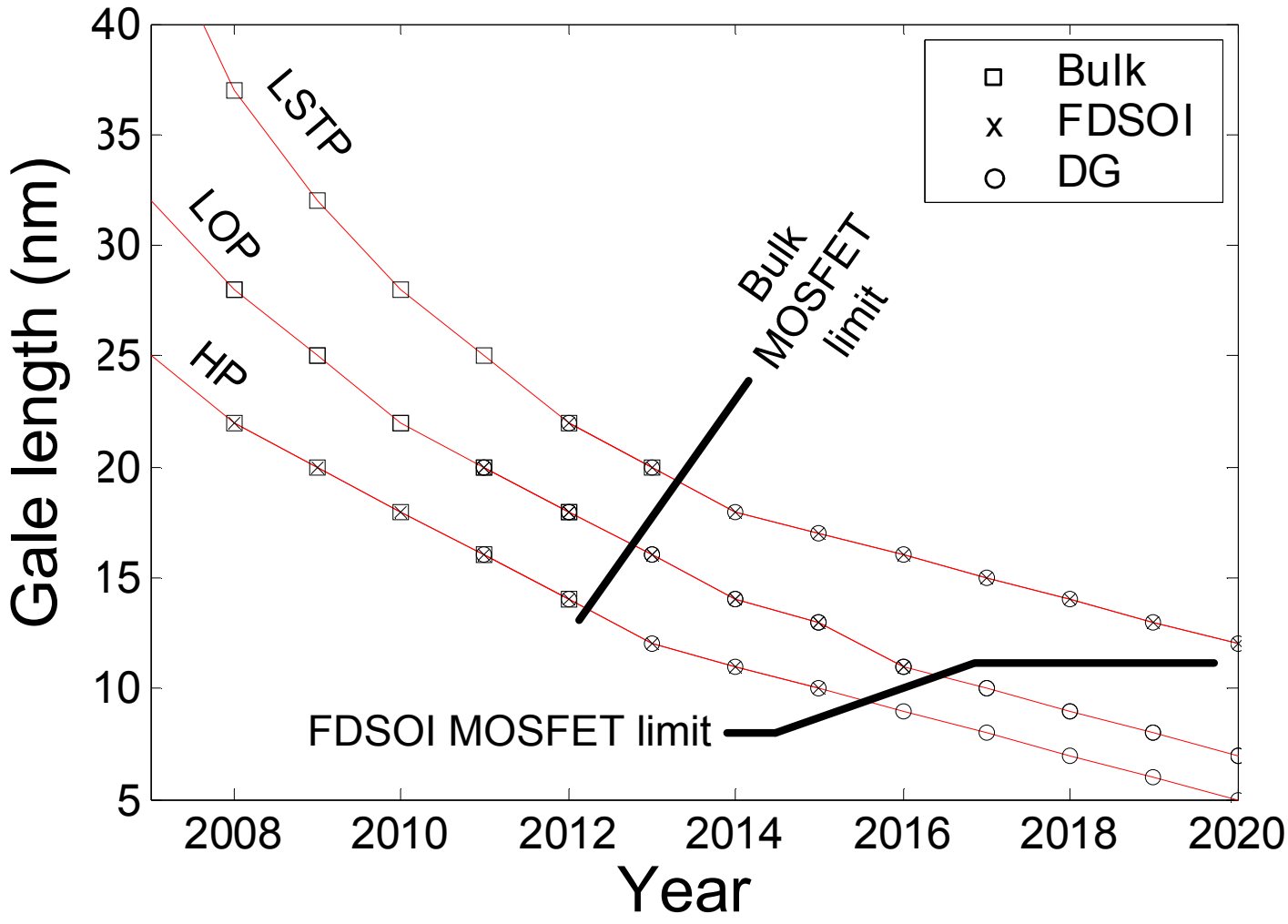
A.O. Adan, T. Naka, A. Kagisawa, H. Shimizu, Proceedings of the IEEE International SOI Conference, p. 9, 1998

Future Trends…

Moore's law

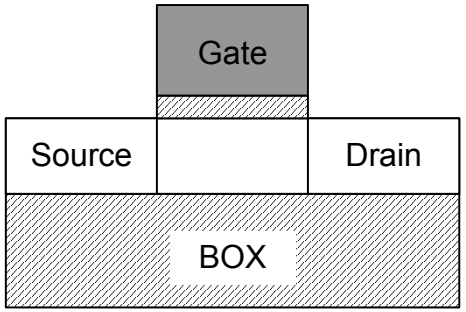

Transistors per chip
10^{12}
10^{10}
10^{8}
DRAM
Microprocessor
1995
2000
2005
2010
2015
2020
Year

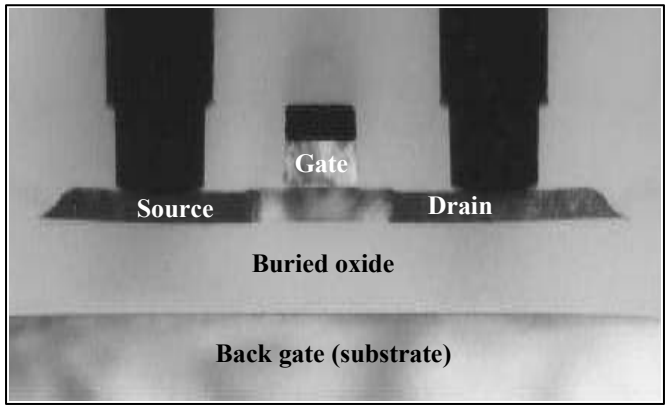
End of Roadmap



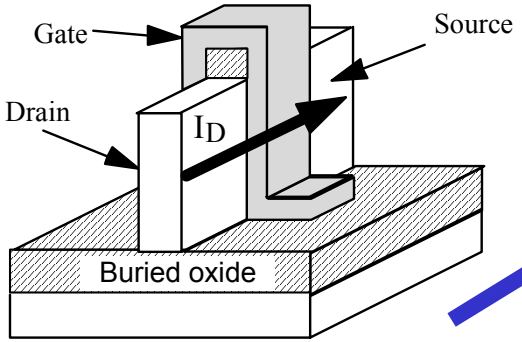
Evolution of CMOS (I)

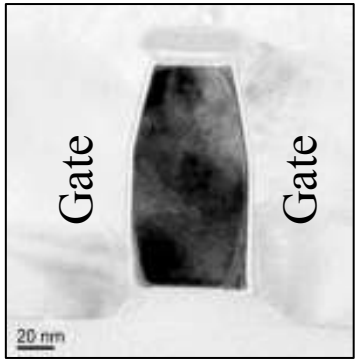
"1 Gate"



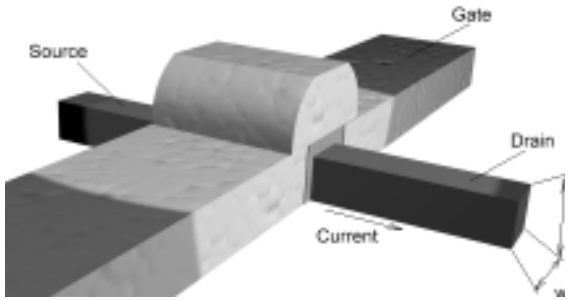


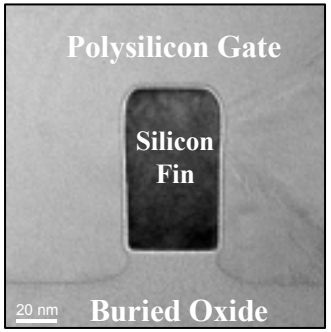
"2 Gates"





FinFET

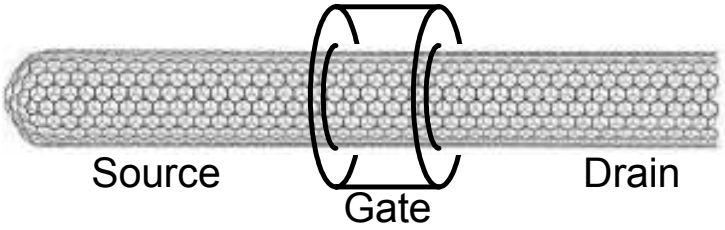


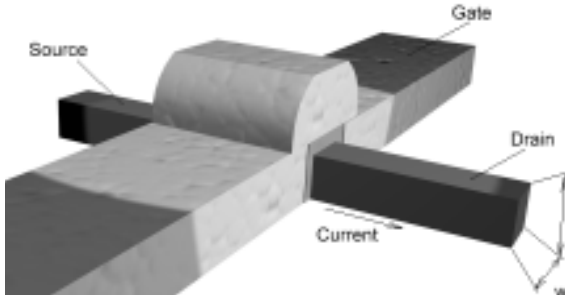


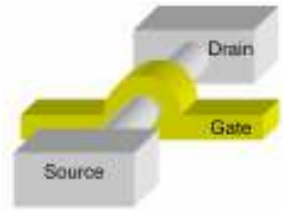
"3 Gates"

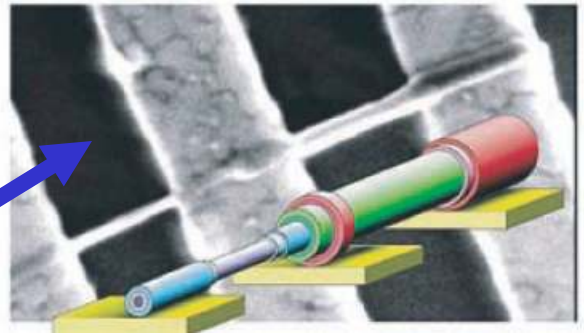
Trigate FET

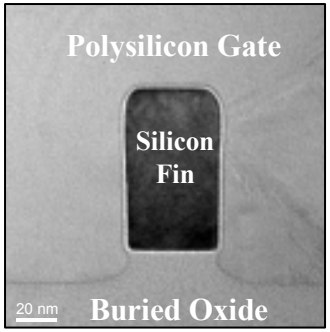
Evolution of CMOS (II)









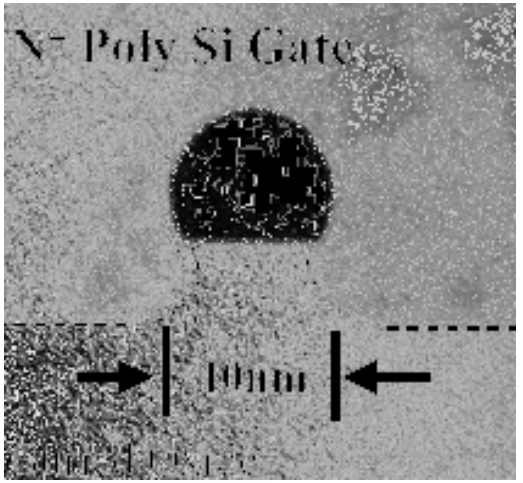


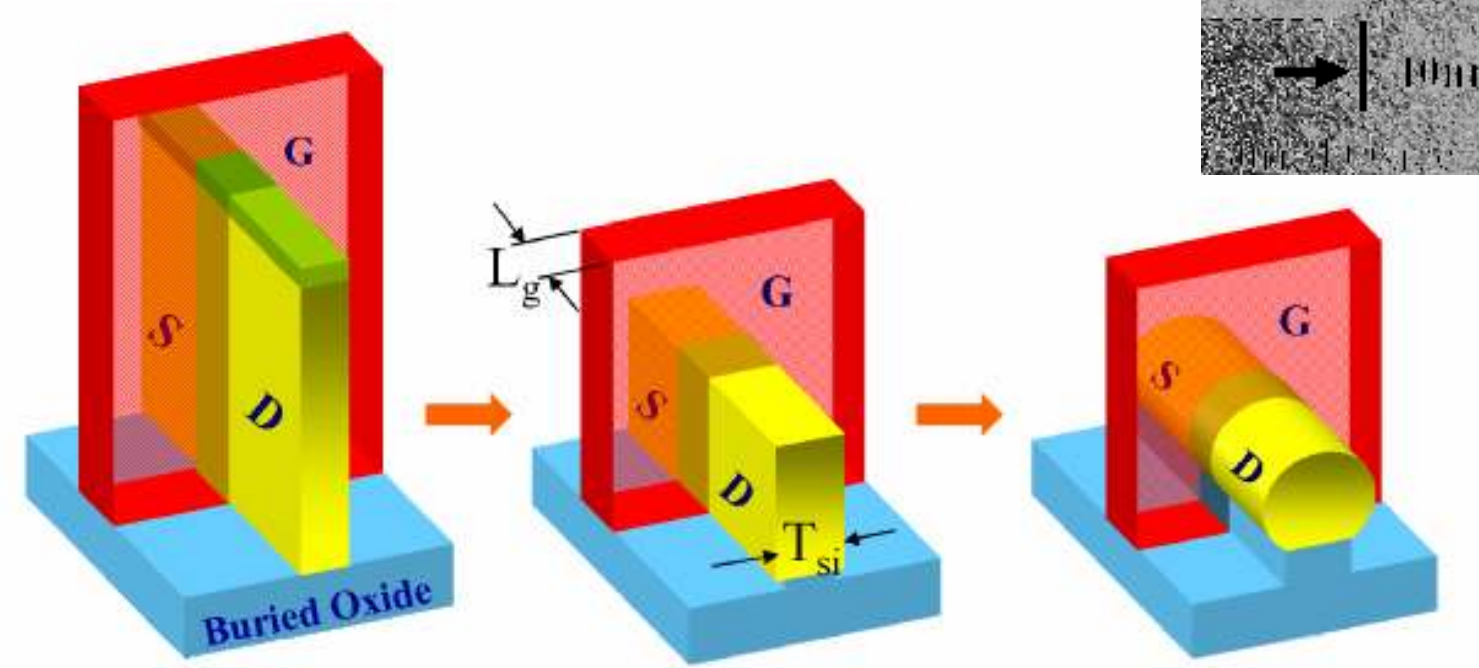
"3 Gates"

Quantum Silicon Nanowire CMOS

Carbon Nanotube CMOS

TSMC's Nanowire FET (VLSI'04)

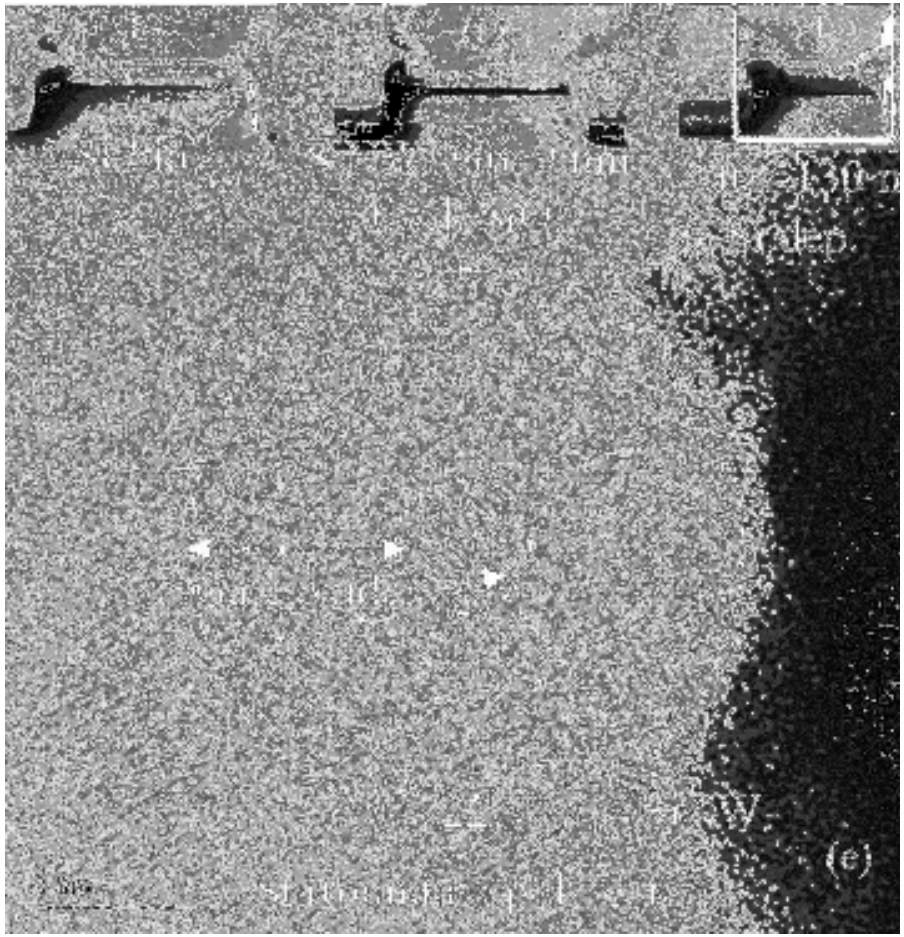


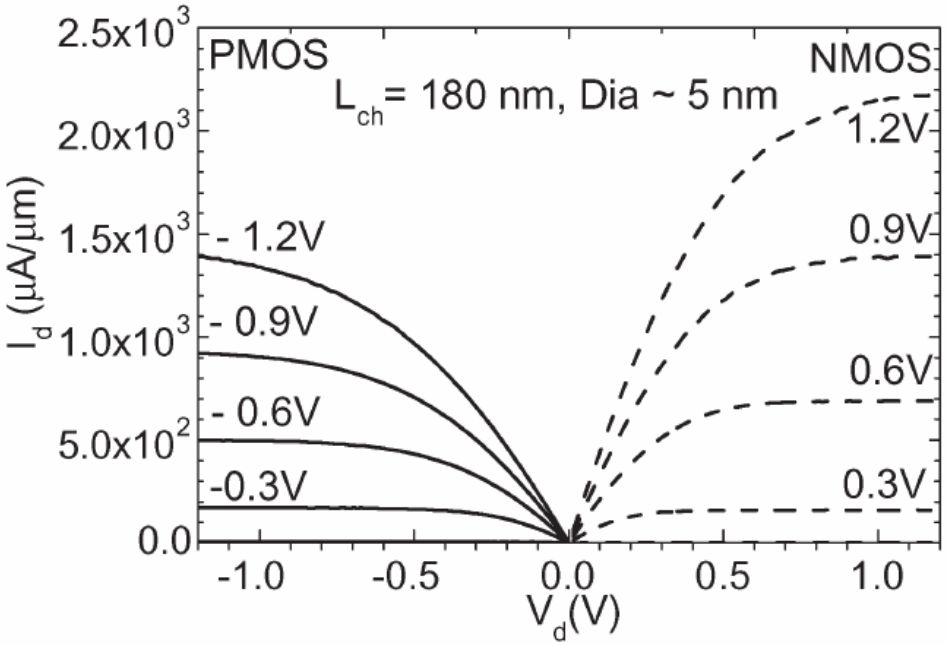


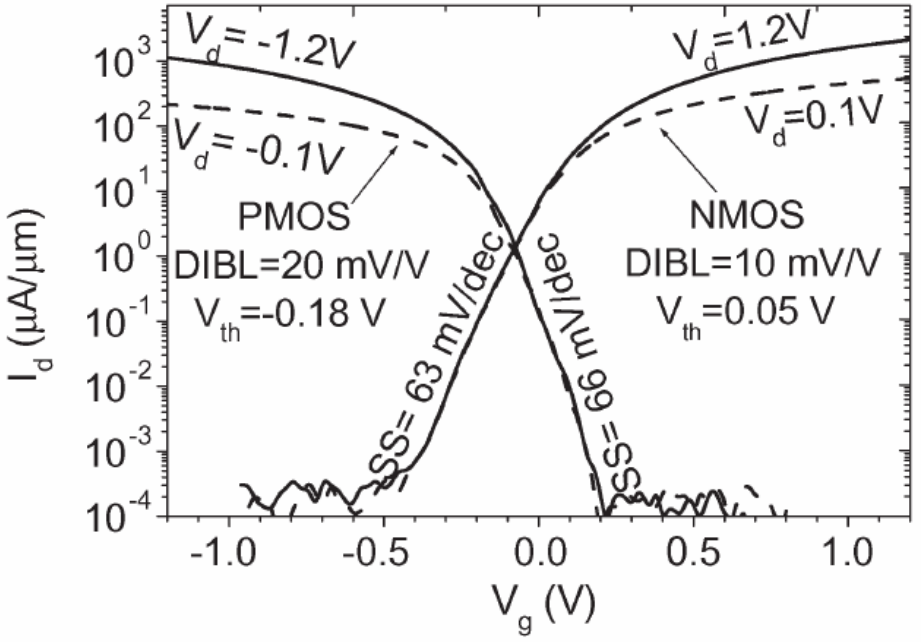
FinFET **Trigate** **Ω gate nanowire**

Fu-Liang Yang, Di-Hong Lee, Hou-Yu Chen, Chang-Yun Chang, Sheng-Da Liu, Cheng-Chuan Huang, Tang-Xuan Chung, Hung-Wei Chen, Chien-Chao Huang, Yi-Hsuan Liu, Chung-Cheng Wu, Chi-Chun Chen, Shih-Chang Chen, Ying-Tsung Chen, Ying-Ho Chen, Chih-Jian Chen, Bor-Wen Chan, Peng-Fu Hsu, Jyu-Horng Shieh, Han-Jan Tao, Yee-Chia Yeo, Yiming Li, Jam-Wem Lee, Pu Chen, Mong-Song Liang, Chenming Hu, "5nm-gate nanowire FinFET" , Symposium on VLSI Technology. Digest of Technical Papers, pp. 196-7, 2004

Nanowire FET
IEEE EDL 2006

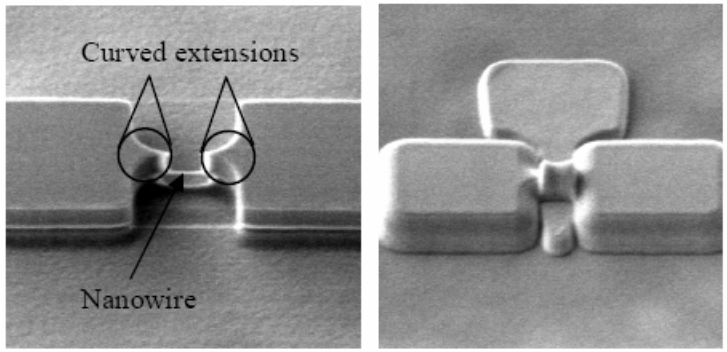






"High-performance fully depleted silicon nanowire (diameter /spl les/ 5 nm) gate-all-around CMOS devices", Singh, N.; Agarwal, A.; Bera, L.K.; Liow, T.Y.; Yang, R.; Rustagi, S.C.; Tung, C.H.; Kumar, R.; Lo, G.Q.; Balasubramanian, N.; Kwong, D.-L., IEEE Electron Device Letters, Vol. 27, no. 5, pp. 383- 386, 2006

Nanowire FET IEDM 2006



Quantum effect

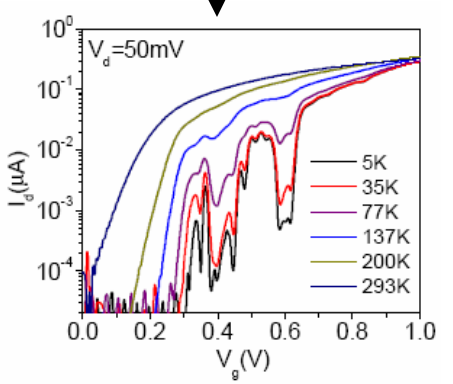


Fig14. I_d-V_g plots with temp for a 6 nm diameter nanowire at V_d=0.05V (linear region).

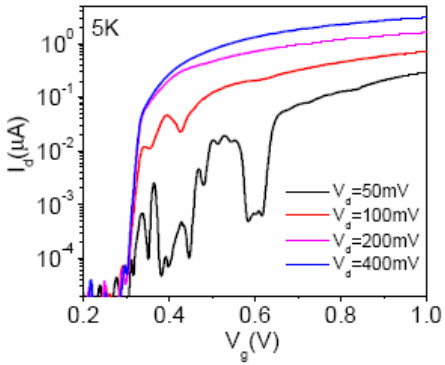


Fig15. I_d-V_g plots with temp for a 6 nm diameter nanowire at 5°K at different drain voltages.

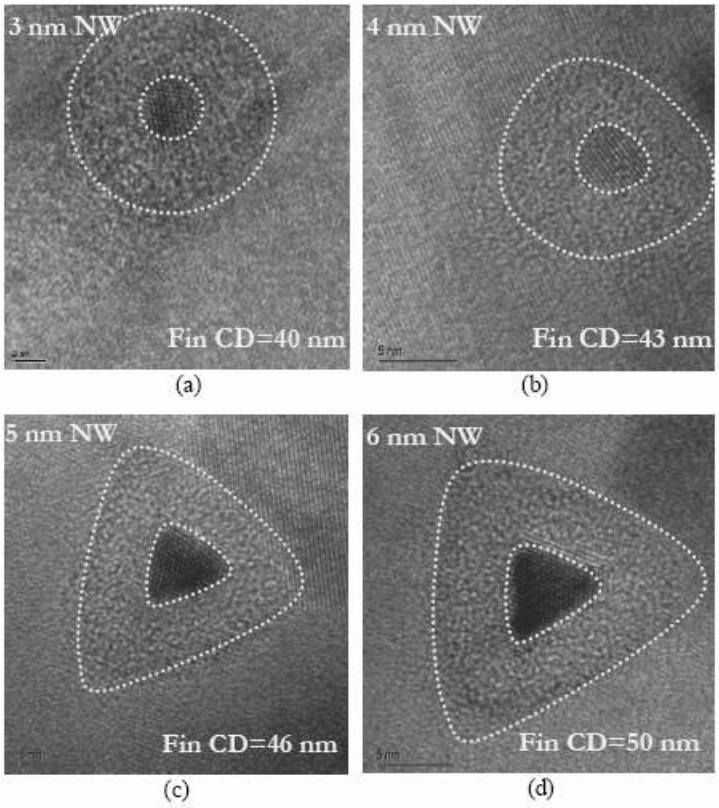


Fig. 2 TEM micrographs of the channel cross-section showing 3 to 6 nm thick SiNW surrounded by 4 nm oxide followed by poly silicon. TEM is done after full process. (a) 3 nm, (b) 4 nm, (c) 5 nm, and (d) 6 nm.

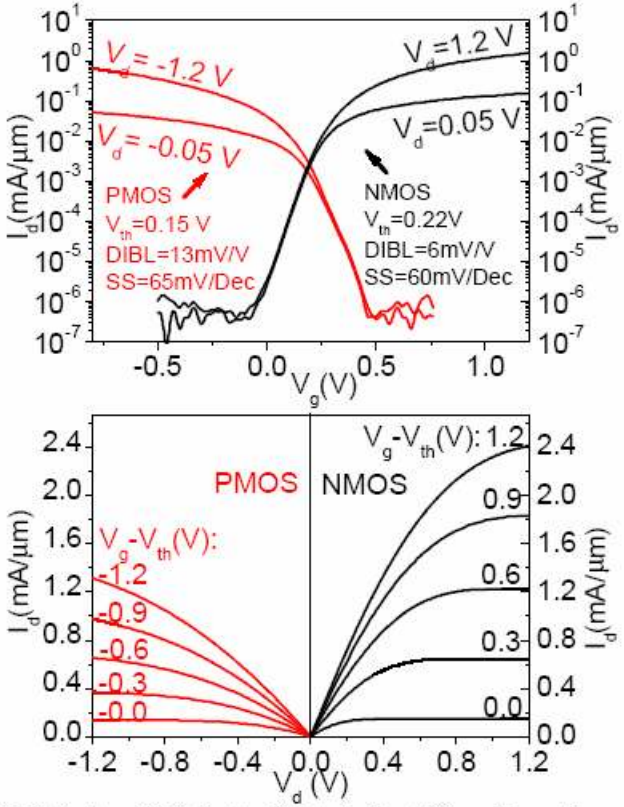


Fig. 3 I_d-V_g (top) and I_d-V_d (bottom) plots for Lg=350 nm. Current is normalized to diameter (3 nm). The channel body consists of thicker curved extension regions caused by the corner rounding in lithography on both sides of the 200 nm long nanowire (Fig. 1(a)).

Ultra-Narrow Silicon Nanowire Gate-All-Around CMOS Devices: Impact of Diameter, Channel-Orientation and Low Temperature on Device Performance

N. Singh, F. Y. Lim, W. W. Fang, S. C. Rustagi, L. K. Bera, A. Agarwal, C. H. Tung, K. M. Hoe, S. R. Omampuliyur, D. Tripathi1, A. O. Adeyeye1, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, IEDM 2006