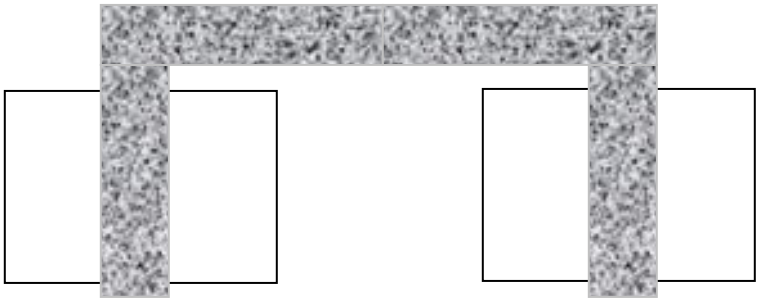
# Solutions UE 4008 Autumn 2009

## Q 1

a) With the aid of diagrams describe how certain elements of a MOS transistor have changed in the shrink from processes with minimum dimensions of about 1.0μm to processes with dimensions in the region of 45-60nm. Give a very brief explanation for the technological reasons for these changes. (Hint: concentrate on the "Gate Stack" and substrate.)

Diagram (preferred of the entire gate stack plus substrate showing change areas between older and modern technologies.
In older processes N+ doped polysilicon was used as the gate electrode material for both N and P Channel devices. With small geometry processes this has switched to N doped polysilicon over the N channel devices and P doped polysilicon over the P channel devices. This change adjusts the work function difference between the gate electrode material and the underlying silicon in the channel region, this allows for better control over the threshold voltage. To prevent formation of a diode contact in areas where P and N channel gates are connected and to reduce the polysilicon sheet resistance the polysilicon is combined with a refractory metal such as titanium to create a silicide which effectively shorts out the pn junction that would be formed where the P doped polysilicon meets the n-doped polysilicon.



In processes below the 90nm node nickel silicide is the preferred material for the gate electrode. Using N doped polysilicon over the N-channed transistors and P-doped over the P-Channels also allows reduction of the threshold voltages in line with scaling of the power supply voltages.

Gate dielectric

As Device geometries shrink all of the dimensions of the films are scaled down as well including film thickness and junction depths. It is necessary as well to reduce the power supply voltages. This in turn necessitates the reduction of the Vt. To facilitate this the gate dielectric thickness is made thinner. The traditional material of the gate dielectric has been silicon dioxide because of the exceptional properties of the material for this role. But in processes below 180nm and approaching 100nm the oxide thickness is approaching 1nm this represents a thickness of about 3 atomic layers, difficult to control and the gate leakage current increases. To counteract this materials with higher dielectric constants are being used. The dielectric constant of silicon dioxide is 3.9, materials such as $HfO_2$ with a dielectric constant of 25 are being used. This enables thicker actual films to be used but with equivalent oxide thickness in the 1nm region. Non-silicon dioxide materials such as $HfO_2$ are being used from the 45nm node on. In scaling from 90nm to 65nm the gate oxide thickness was not scaled down because of leakage problems

Substrate material

Increasingly strained layers are being used in the substrate material to improve the carrier mobility in the channel region. The strain can be induced in a number of ways; By epitaxially growing a layer of silicon germanium on top of the silicon substrate and then another thin layer of silicon on top of the SiGe. The different size of the germanium atom in the crystal induces strain in the top silicon layer, this in turn improves the carrier mobility in the channel region. This is particularly used to increase the mobility in PMOS transistors. In NMOS transistors the mobility is optimised by thermomechanical design of the sidewall spacers and a strain inducing silicon nitride film.

Diagram here of the strained region.

Many modern process are now also moving to SOI silicon to improve (reduce) substrate capacitance.. SOI Substrates consist of a thin layer of silicon on top of a buried oxide layer (BOX) which in turn sits on a carrier wafer. SOI offers reduced substrate capacitance, better isolation and improved speed of operation performance.

Additional items

Sidewall spacers, these allow for silicidation of the gate electrode and the contact/S/D areas without shorting out the gates to the source and drain.

The Source drains are generally engineered to have high doping at the surface and lower doping through the full S/D region.

The metallization has moved from aluminium alloys to damascene copper with low k dielectric films between the copper layers.

b) In the shrink from 65nm to 45nm a company changes the gate dielectric from to hafnium oxide with a dielectric constant of 25 if the resultant gate capacitance is $3.0 \times 10^{-6}$ F/cm$^2$ what is the actual new dielectric thickness and the silicon dioxide equivalent?

Given:

The permittivity of free space is 8.86 X $10^{-14}$ F/cm
The dielectric constant of silicon dioxide is 3.9

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$\varepsilon_{ox} = k\varepsilon_0$$

$$C_{diel} = \frac{k_{diel} \times \varepsilon_0}{t_{diel}}$$

$$3.0 \times 10^{-6} = \frac{25 \times 8.86 \times 10^{-14}}{t_{diel}}$$

$$t_{Haf} = \frac{25 \times 8.86 \times 10^{-14}}{3.0 \times 10^{-6}}$$

$$t_{Haf} = 7.22 \times 10^{-7} cm$$

$$t_{Haf} = 7.22 nm$$

$$t_{ox} = \frac{3.9 \times 8.86 \times 10^{-14}}{3.0 \times 10^{-6}}$$

$$t_{ox} = 1.15 \times 10^{-7} cm$$

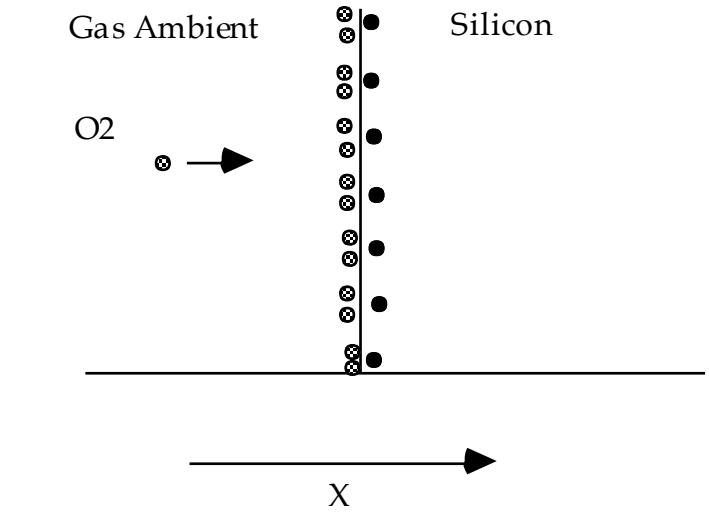
$$t_{ox} = 1.15 nm$$

**Q 2**

a) Describe a physical model for the thermal oxidation of silicon.

**Thermal Oxidation Understanding**

Initially



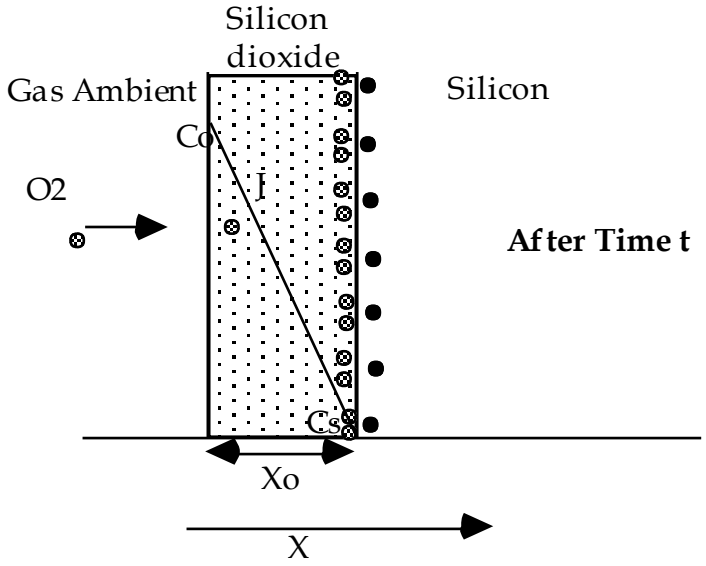




Diagram 1
Reaction controlled
How fast the chemical reaction between the oxidizing species and the silicon can take place
Growth is linear

Diagram 2
Oxide on the surface

Oxidizing species must diffuse through the oxide
As the oxide gets thicker this takes longer
Growth rate becomes dominated by the diffusion time
Growth rate parabolic

b) Describe what happens to dopant in the silicon during the thermal oxidation cycle if:
   i) The segregation co-efficient is less than 1,
   ii) If the segregation coefficient is greater than 1.

**Dopant Segregation**

**Redistribution of Impurities During Thermal Oxidation**

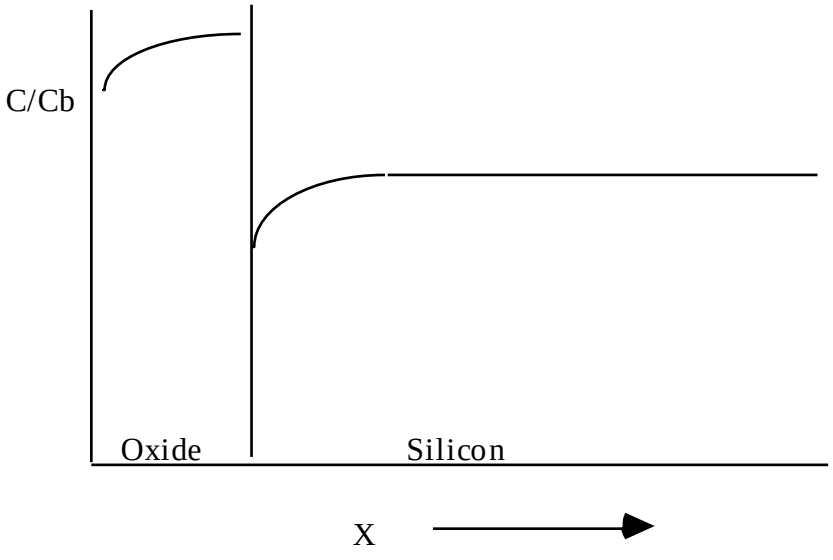
Because most impurities diffuse much slower in silicon dioxide than in silicon we expect that an oxide grown on the surface will effectively seal the impurities in the silicon.

The situation is much more complex!! With any two phases in contact, any impurity will be redistributed between the two phases, until equilibrium is reached. In equilibrium the ratio of the concentrations will be constant.

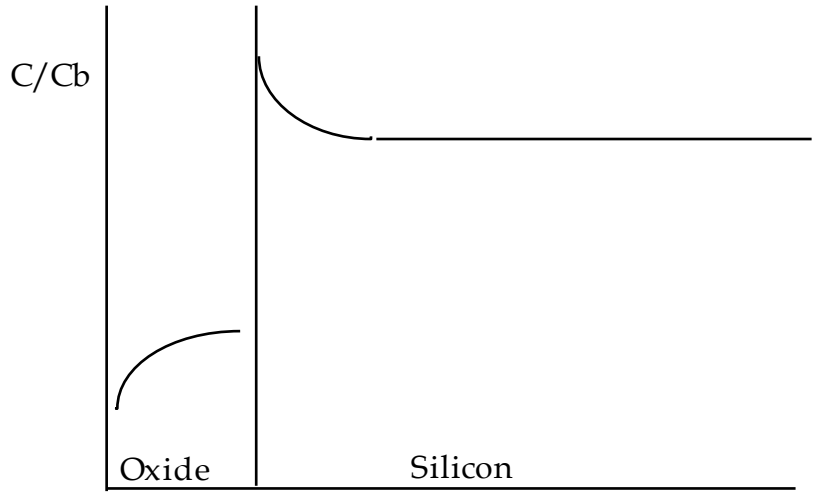
The ratio of the equilibrium concentrations in the silicon and silicon dioxide is denoted by the term segregation coefficient and is defined by :-

$$M = \frac{\text{Equilibrium conc. of impurity in silicon}}{\text{Equilibrium conc. of impurity in silicon dioxide}}$$

When oxide takes up the impurity M<1



For M>1




One interesting feature is that this redistribution is independent of oxidation time.

| | |
|---|---|
| Boron Segregation Coefficient | 0.3 |
| Phosphorous Segregation Coefficient | 10.0 |

**Common Terms (colloquial)**
Boron "suck-out"
Phosphorus "Pile-up" or "Snowplough Effect"

c) A silicon <100> wafer, which had been patterned for ion implant with 50nm of oxide in the windows to be implanted and 1.0μm in the other areas to protect against the implant, is put through a thermal oxide process at 1000°C in pyrogenic steam for 3 hours, what is the final oxide thickness in:
   i) The areas which had 50nm on the surface prior to oxidation?
   ii) The areas which had 1.0μm on the surface prior to oxidation?

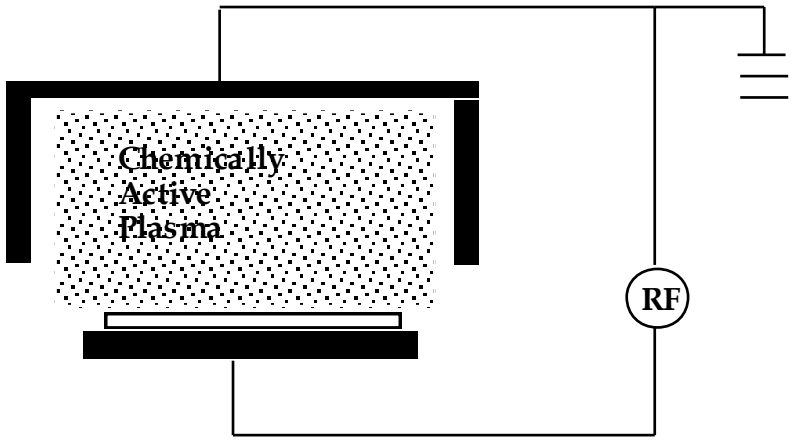
From the supplied curve for Oxygen Growth in Pyrogenic Steam
50nm-500A=.05μm
It would take 2min to grow this thickness at 1000°C in steam
New oxidation time is 180min additional 2 minutes is negligible final thickness read from curve is 0.82μm or 820nm

The areas with 1.0μm oxide, this would take 250 minutes to grow at 1000°C, this plus the new time of 180 minutes would give an equivalent total of 430 minutes and a final oxide thickness of 1.4μm

**Q 3**

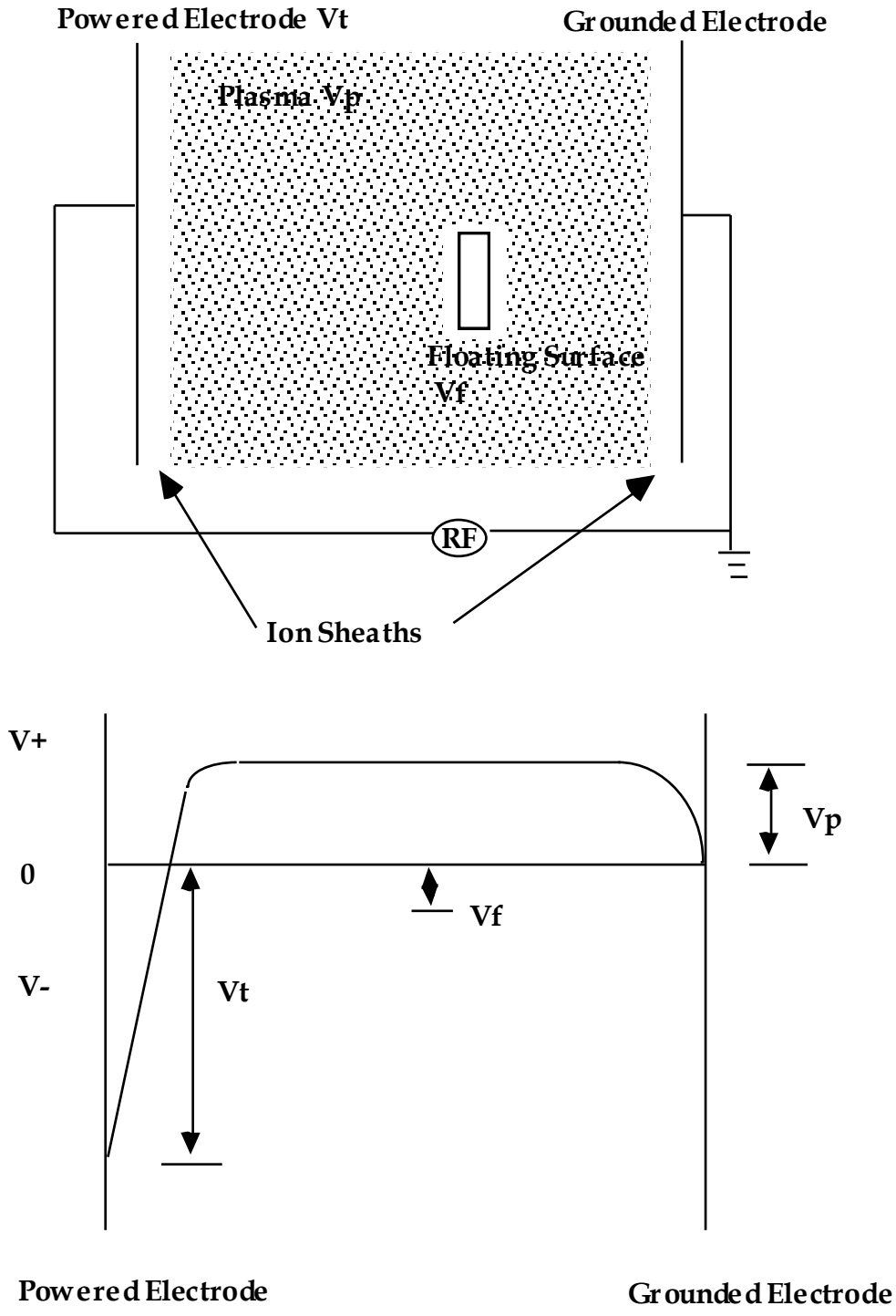
a) Describe the Reactive Ion Etch process, outlining parameters that effect the process and describing the equipment used

Reactive ion etch is a dry etch system. The physical arrangement is a parallel plate electrode system connected to an RF Power Supply. The wafer sits on the lower electrode that is the powered electrode, the top electrode is grounded. The top electrode is often called a showerhead as it is manufactured so that the etch gases can enter the chamber through the top electrode.
The etch mechanism is a combination of physical and chemical etching with the physical etch being the more dominant, giving an anisotropic etch profile. The fact that the wafers sit on the powered electrode means that there is a high DC potential from the plasma cloud to the surface of the wafer, increasing the physical element of the etch. Reactive gas species are used in the etching the exact gas selection is dependant on the material to be etched.




**REACTIVE ION ETCH**

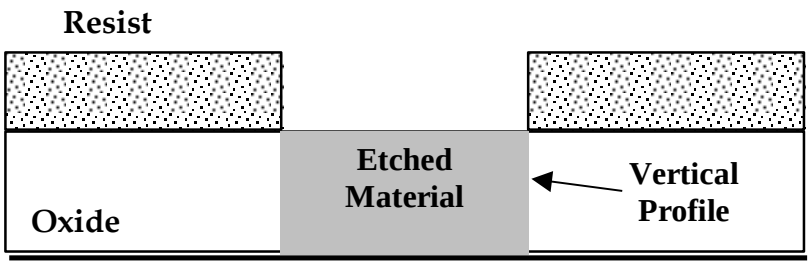
*Reactive Ion Etch (RIE)*
Wafer on the powered electrode
Pressure 10mTorr – 100 mTorr
DC Voltage Drop ≈ 100 700V
Uses chemically reactive gases




**Potential diagrams showing the potential difference between the plasma cloud and the electrodes of a dry etch system**

(not essential)

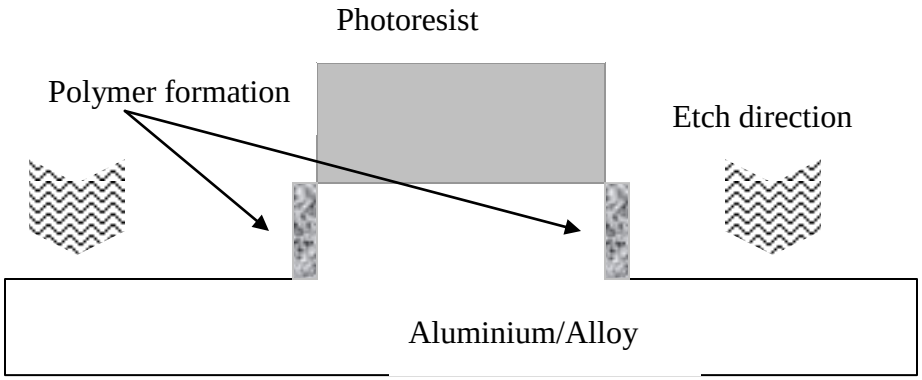
The etch profile of an RIE etch sample can be controlled by controlling the pressure, gas mixture, and power of the etch, but essentially an RIE profile is very anisotropic that is there is very little sideways etch or undercut of the masking material.




**Anisotropic etch profile typical of an RIE etch**

b) Describe how polymer formation in RIE can assist the anisotropic etch of aluminium alloys, outline problem(s) associated with this etch.

During the RIE etch aluminium and aluminium alloys with Cl2 and BCl3 a polymer is formed down the vertical sidewall of the etched area. This provides a degree of passivation of the edge and prevents sideways etch of the material and greatly assists in having a very anisotropic profile for the etch, (diagram)




As described above the formation of the polymer is useful in achieving the anisotropic profile but contained in the polymer is a certain amount of chlorine from the etch gases. When the vacuum system is vented up to take the wafers out of the etch system there will be a certain amount of water vapour in the lab environment. This water combines with the chlorine to form hydrochloric acid (HCl) and this essentially begins to "wet etch" the Al or alloy. The way to prevent is to , immediately on bringing to atmosphere ash or wet resist strip, this will also remove the polymer and stop the attack of the HCl on the metal.
Most modern RIE metal etch systems have a separate chamber where this can be done in an oxygen plasma prior to bringing the wafers up to atmosphere.

a) Using the linear etch model for a silicon etch with photoresist as a masking material, How deep is the silicon etched in the vertical direction well away from the mask edge, and in a lateral direction under the mask edge, if the etch time is 5 minutes?

Given:

Etch Rate = **R**

$$R = \frac{\left(S_c K_f F_c + K_i F_i\right)}{N}$$

$S_c$ = Sticking coefficient (.01), $K_f = (.02)$ and $K_i = (1)$ are the relative rate constantsfor the two processes

$F_c = (2.5 \times 10^{18}$ atoms $cm^{-2}s^{-1})$ and $F_i = (1 \times 10^{16}$ atoms $cm^{-2}s^{-1})$ are the chemical and ion fluxes,

$N$ is the density $= (5 \times 10^{22}$ atoms$/cm^3)$

**Question 4:**

a) Describe in terms movement of holes and electrons the operation of an NMOS transistor as the gate voltage is swept from 0V to a voltage greater than the threshold voltage. Assume the source is grounded and there is a small positive voltage on the drain. What effect will the application of a reverse bias to the substrate or bulk have on the device?

Diagram of a cross section of a MOS device, showing SD, Gate oxide, Gate electrode, and electrical connections to the S, D, and Gate. Initially show 0V on the gate and a small! 0.1V on the Drain, show the Source grounded.

Description, with 0V on the gate and a small positive voltage on the drain there is no current flowing. Even though there is a potential difference between the S and drain because the positive is applied to the N side of the PN junction diode, this is a reverse biased diode and no current will cross.

If instead of 0V on the gate the voltage applied is increased in the positive direction, no current flows in the gate as the gate is sitting on the gate oxide which is a good insulator and prevents current flow from the gate to the silicon. But if there is a positive voltage with no current flow there will be an associated electric field, this electric field spreads into the channel region of the device. The channel region of the device between the S and D is P type, that is a large number of holes as majority carriers and a smaller number of electrons as minority carriers. By definition these carriers can move under the influence of an electric field, like charges repel each other and unlike charges attract. So under the influence of the gate induced electric field the holes start to move away from the area immediately under the gate oxide, this is known as depletion, the region starts to be come depleted of majority carriers. If the voltage applied to the gate is further increased, the electric field will increase and push the majority carriers further away, at some point not alone are the majority carriers pushed away but minority carriers are pulled into the region. If the voltage on the gate becomes sufficiently high a layer of minority carriers or in this case is formed in the channel region under the gate. This condition is known as inversion, in a region where you expect to find a large number of holes there are a large number of electrons, the type has been inverted.

At this point the conditions for a reverse biased diode are no longer being met, (large no. holes on one side large no of electrons on the other), now there are electrons for conduction in the N Drain region in the channel under the gate and in the source region, this is now like a resistor and the carriers are free to move between s and d under the influence of the potential difference between the source and drain. The point at which the channel is formed or the surface type is inverted is known as the threshold voltage of the device or the turn point of the device

b) By how much will the threshold voltage shift in an NMOS transistor if a 1.0V reverse bias is applied to the substrate at a measurement temperature of 27°C?

Given:

Substrate doping =1 x $10^{15}$ atoms $cm^{-3}$

$\varepsilon_o$ = 8.86 x $10^{-14}$ F $cm^{-1}$

$k_s$ = 11.7

$n_i$ = 1.45 x $10^{10} cm^{-3}$

q = 1.602 x $10^{-19}$ Joule

$C_{ox}$ = 1.4 x $10^{-8}$ F $cm^{-2}$

k = 1.38 x $10^{-23}$ $JK^{-1}$ (Boltzmann's constant)

$$\Delta V_t = \frac{\sqrt{2k_s \varepsilon_o q N_B}}{C_{ox}} \left( \sqrt{2\Psi_p + V_{BS}} - \sqrt{2\Psi_p} \right)$$

$$\psi_p = \frac{kT}{q} \ln \frac{N_B}{n_i}$$

$$\psi_p = 0.288$$

$$\Delta V_t = \frac{\sqrt{3.32 \times 10^{-16}}}{1.4 \times 10^{-8}} (0.497)$$

$$\Delta V$$

=0.65V

Well away from the mask edge there is both chemical and physical etchinig, close under the mask edge there is no ion bombardment or physical etch so there is only the chemical etch.

Vertical Etch well away from mask edge

$$(R) = \frac{0.01 \times 0.02 \times 2.5 \times 10^{18} + 1 \times 1 \times 10^{16}}{5 \times 10^{22}}$$

$$R = cm.s^{-1}$$

$$R = 2.1 \times 10^{-7}\, cm.s^{-1}$$

For a 5 min etch time (300 sec)
Etch depth is 6.3 x $10^{-5}$ cm or 0.63μm for a location well away from the mask edge

At the mask edge, under the mask there is no physical etch component as the ions cannot bombard under the masking material. There is only a chemical component.

$$R = 1.0 \times 10^{-8}\, cm.s^{-1}$$

For a 10min etch time (300 sec)
Lateral etch distance is 3.0 x $10^{-6}$ cm or 0.03μm