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THE NATIONAL UNIVERSITY OF IRELAND CORK

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UNIVERSITY COLLEGE CORK

Summer 2011

FOURTH ENGINEERING (ELECTRICAL & ELECTRONIC)

Digital Integrated Circuit Design UE4001

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Answer Question 1 and 4 of the remaining 5 questions
1.5 HOURS

Approved Calculator Allowed

Questions follow overleaf

Question 1) **(20 marks)**

a) Describe the General-Purpose-IC and Application Specific Integrated circuit. Define Logic Synthesis and RTL modelling.

b) Define decomposition, pipelining and replication in the context of architectural design. Present the performance implications of each.

c) Define synchronous and asynchronous clocking. Give some pros and cons for the synchronous clocking.

d) Define clock skew and clock jitter. How much clock skew does a circuit tolerate?

e) Present one method on how to implement clock gating properly. What is metastability?

Question 2) **(20 Marks)**

a) Given the following equation, present an architecture which would implement it:

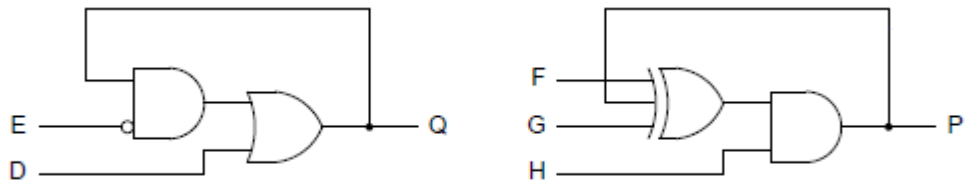
$$y(k) = \sum_{n=0}^{N=3} b_n x(k-n)$$

Analyse the architecture by giving the following: longest path delay, data throughput, latency, circuit size, area by time product.

b) For the same circuit use pipelining to improve its performance. Discuss the new architecture through the same parameters as above (longest path delay, data throughput, latency, circuit size, area by time product)

Question 3) **(20 Marks)**

a) In the Figure below two feedback circuits each built from a few logic gates are presented. Establish their respective truth tables and briefly describe their behaviour.



b) Consider the truth table below and assume all of x, y, z are available in complemented and non-complemented form. Is it possible to implement this function in a single gate in static CMOS technology? How many gate equivalents would it take to implement your solution?

	f	yz 00	01	11	10
x	0	1	1	0	0
	1	0	1	0	1

c) Design a transistor-optimised 3 input minority gate.

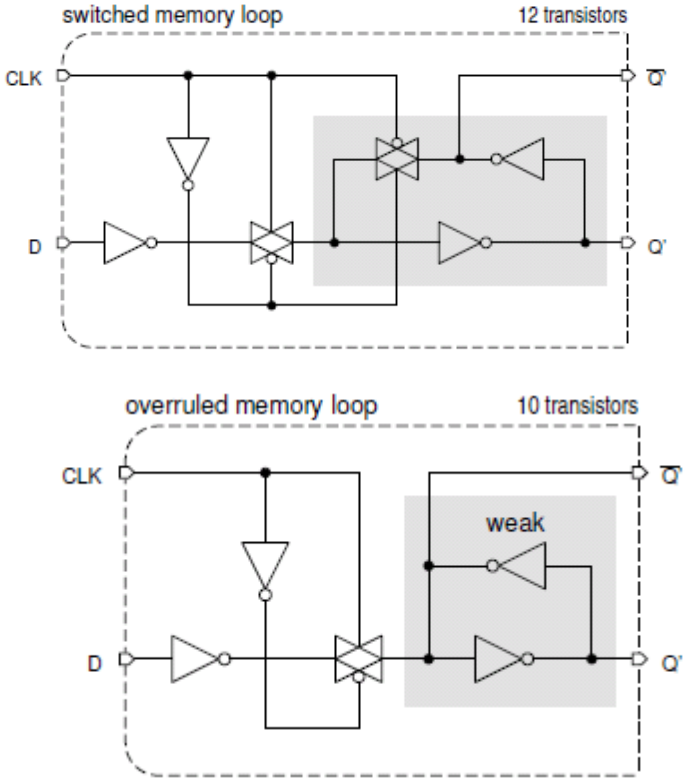
Question 4) **(20 Marks)**

a) In the context of combinational digital circuits, a flip-flop and a latch, define using some waveforms the following timing quantities: contamination delay, propagation delay, fall time, high time, low time, hold time.

b) Consider two flip-flops with combinational logic in between. Derive a lower bound for the clock skew (setup condition for the circuit). Derive an upper bound for the clock skew (hold condition for the circuit)

Question 5) **(20 Marks)**

a) Figure below presents two schematics of a latch. Compare the two architectures by presenting some pros and cons of the overruled memory loops architectures.



b) Present a RAM overall organisation. Give the description of an SRAM cell and one DRAM cell. Present some differences between SRAM and DRAM memory.

Question 6) **(35 Marks)**

a) In the context of CMOS digital circuits, present and derive the expression for the average energy dissipated per computation cycle.

b) Present some techniques to improve energy efficiency, based on Dynamic voltage and frequency scaling, dynamic dissipation and leakage reduction techniques.