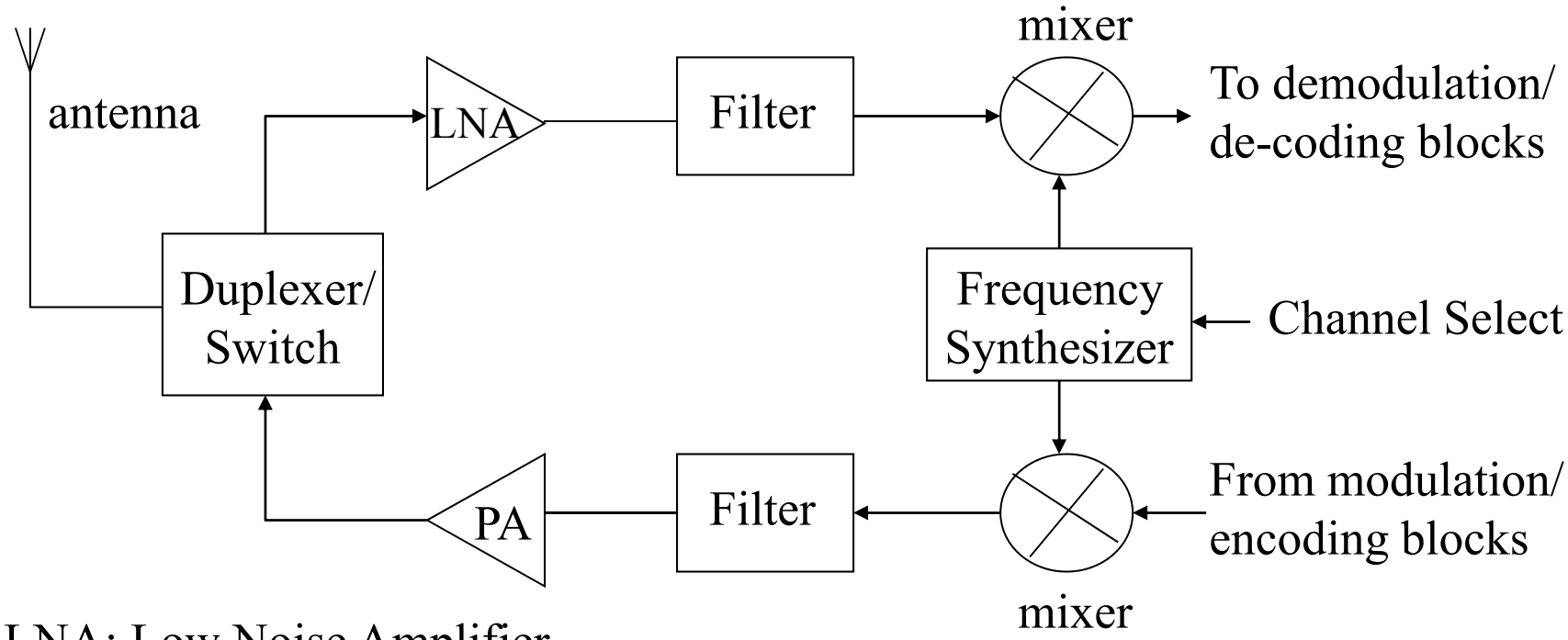
EE4011 RF ICs

Introduction to Phase-Locked-Loops (PLLs)

A Generic RF Front-End

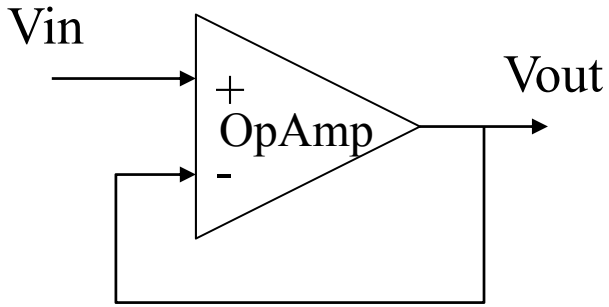


LNA: Low Noise Amplifier
PA: Power Amplifier

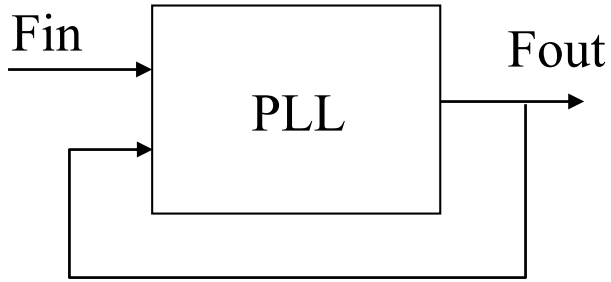
The front-end of a typical RF system is shown above. A frequency synthesizer is frequently used to select the frequency of operation (the channel). It supplies a local oscillator signal which can be varied over a wide frequency range. Mixers are used to down-convert the high frequency received signals to lower intermediate frequencies and vice-versa.

Phase Locked Loops (PLL)

A phase locked loop is a feedback system which uses phase (or more precisely excess phase) to "lock" the frequency of its' output with that of an input (reference) signal. In many ways, it is a similar system to an op-amp configured with negative feedback except that the op-amp uses voltage as the feedback and control quantity whereas the PLL uses phase.

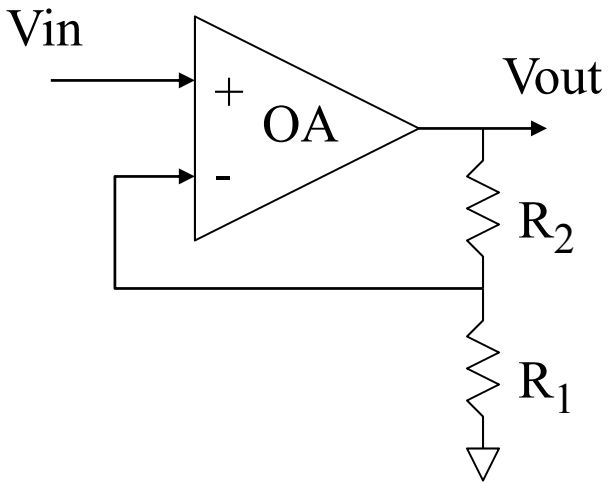


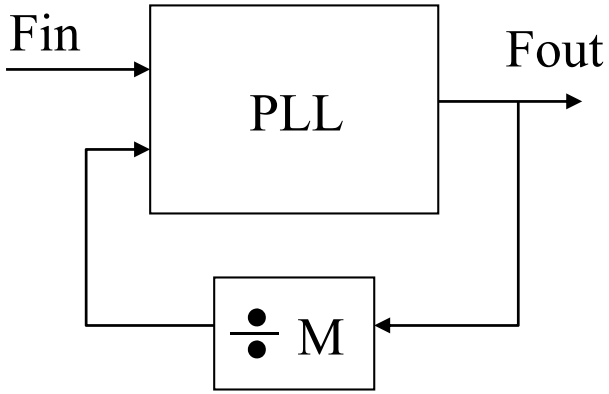
$$V_{out} = V_{in}$$



$$F_{out} = F_{in}$$

PLLs as Frequency Synthesizers



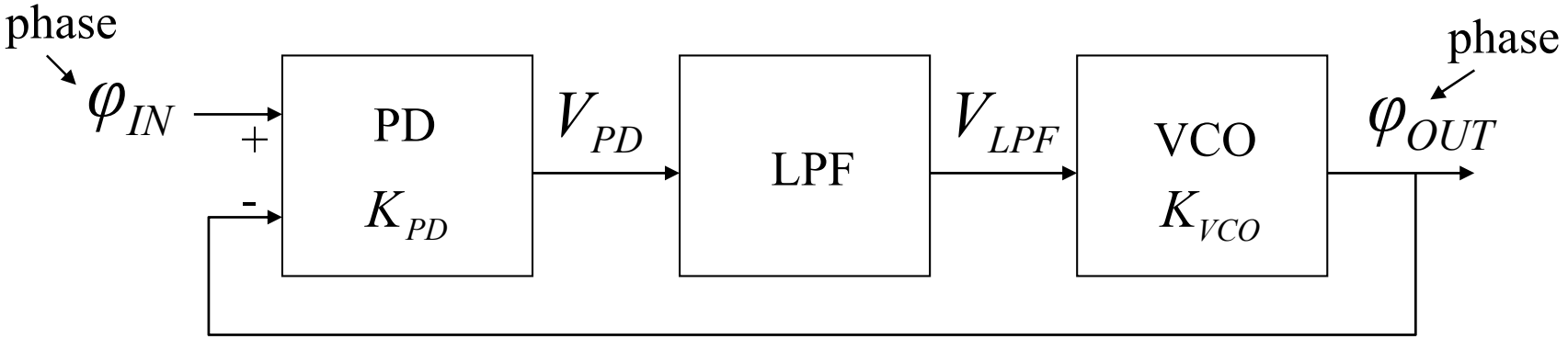


$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) V_{in}$$

$$F_{out} = M F_{in}$$

In an op-amp configuration, a voltage divider can be used to make the output voltage a multiple of the input voltage. In PLLs, a ***frequency divider*** in the feedback circuit causes the output frequency to be a multiple of the input frequency. A frequency synthesizer is formed by using a stable low-frequency reference for the input while different output frequencies can be obtained by changing the feedback divider factor, M, in a programmable divider. M is then the "channel select" control.

Type I PLL



A Type I PLL consists of a phase detector (PD), a low-pass filter (LPF), and a voltage controlled oscillator as shown. The phase detector generates an output voltage which is linearly proportional to the phase difference between the two inputs where K_{PD} is the "gain" of the phase detector in V/rad:

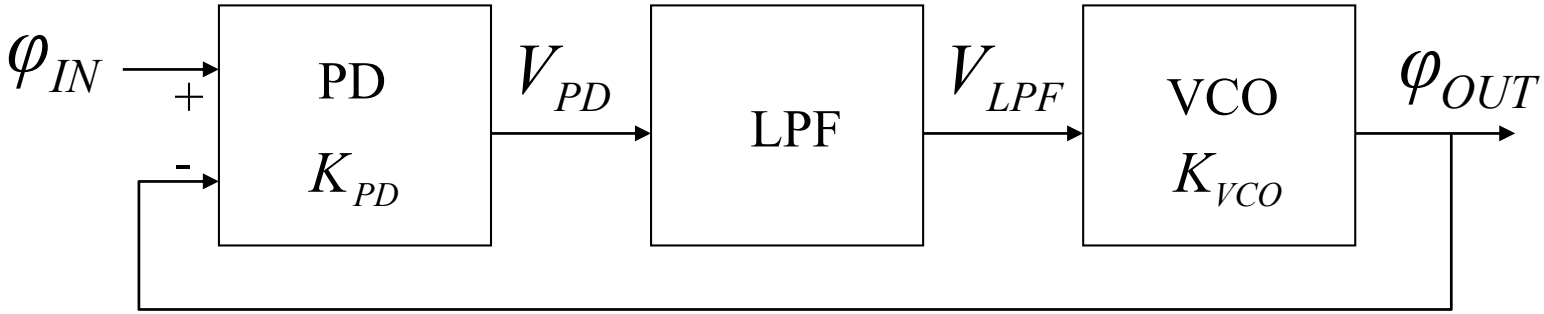
$$V_{PD} = K_{PD}\left(\varphi_{in} - \varphi_{out}\right)$$

The output from the phase detector is filtered by means of a low-pass filter and the VCO generates a waveform whose instantaneous frequency is proportional to this:

$$\omega_{out} = \omega_{fr} + K_{VCO}V_{LPF}$$

NB: The "control quantity" is phase.

Type I PLL in Steady State - 1



If the input waveform has a constant frequency (and excess phase), then the loop will eventually reach a steady state condition where the output waveform will also have a constant frequency (and excess phase) and the voltages V_{PD} and V_{LPF} will be constant. In this case:

$$\varphi_{in} = \omega_{in} t + \varphi_1 \quad \text{and} \quad \varphi_{out} = \omega_{out} t + \varphi_2$$

$$V_{PD} = K_{PD}\left(\varphi_{in} - \varphi_{out}\right) = K_{PD}\left(\omega_{in} t + \varphi_1 - \omega_{out} t - \varphi_2\right)$$

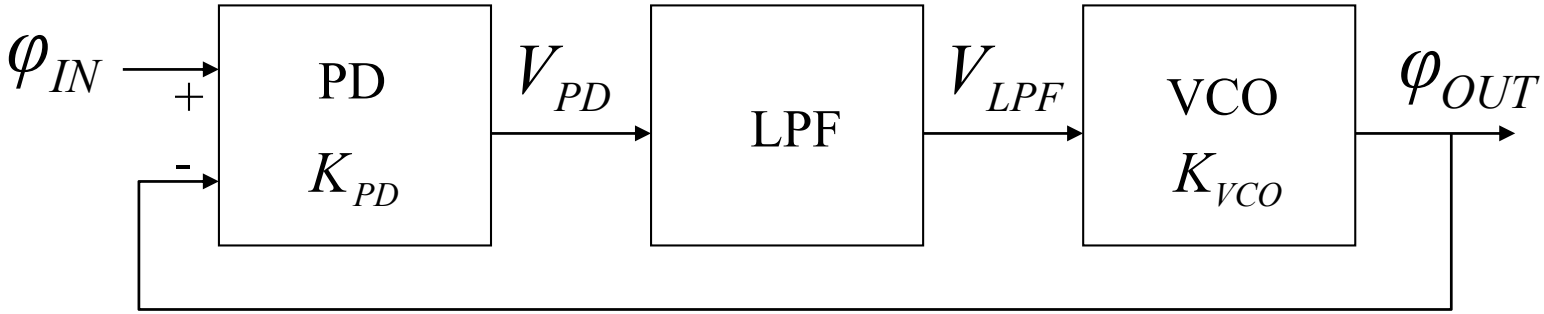
$$V_{PD} = K_{PD}\left(\left(\omega_{in} - \omega_{out}\right)t + \left(\varphi_1 - \varphi_2\right)\right) = K_{PD}\left(\left(\omega_{in} - \omega_{out}\right)t + \Delta\varphi\right)$$

In steady state, V_{LPF} is the same as V_{PD} so:

$$V_{LPF} = V_{PD} = K_{PD}\left(\left(\omega_{in} - \omega_{out}\right)t + \Delta\varphi\right)$$

$\Delta\phi$ is the phase difference between the input and output waveforms

Type I PLL in Steady State - 2



In steady state the output voltage of the LPF is constant i.e. $dV_{LPF}/dt = 0$:

$$\frac{dV_{LPF}}{dt} = \frac{d}{dt}\left[K_{PD}\left(\left(\omega_{in} - \omega_{out}\right)t + \Delta\varphi\right)\right] = K_{PD}\left(\omega_{in} - \omega_{out}\right)$$

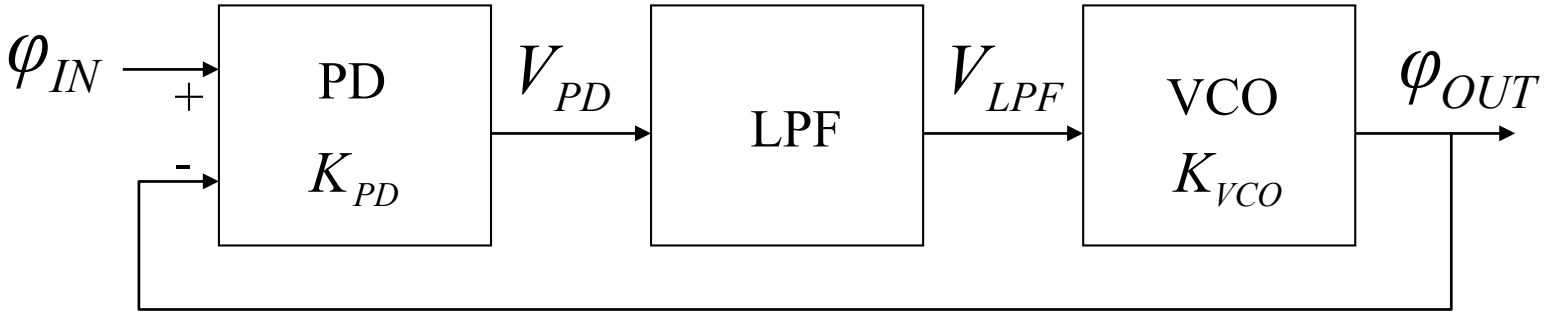
$$\frac{dV_{LPF}}{dt} = 0 \Rightarrow \omega_{out} = \omega_{in}$$

Therefore, this system which is using phase as the feedback quantity, causes the output frequency to be *exactly* the same as the input frequency in steady state.

In steady state, the input voltage to the VCO is determined by K_{PD} and $\Delta\phi$:

$$V_{LPF} = V_{PD} = K_{PD}\left(\left(\omega_{in} - \omega_{out}\right)t + \Delta\varphi\right) = K_{PD}\Delta\varphi$$

Type I PLL in Steady State - 3



In steady state:

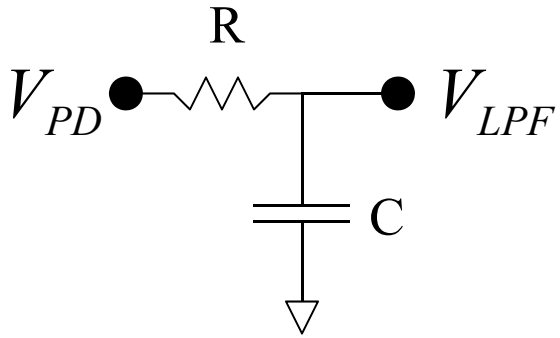
$$\omega_{out} = \omega_{fr} + K_{VCO}V_{LPF} = \omega_{fr} + K_{VCO}K_{PD}\Delta\varphi$$

$$\Rightarrow \Delta\varphi = \frac{\omega_{out} - \omega_{fr}}{K_{VCO}K_{PD}} = \frac{\omega_{in} - \omega_{fr}}{K_{VCO}K_{PD}}$$

In steady state, the output frequency is the same as the input frequency but there is a difference between the input and output phases which depends on the input frequency, the oscillator free-running frequency and the PLL gain $K_{VCO}K_{PD}$. The phase difference $\Delta\phi$ is sometimes referred to as "sustaining" the output frequency.
This is an interesting control system: it uses phase as the feedback quantity but it is frequency (i.e. the derivative of phase) which is being matched exactly.

Transfer Function of A Simple LPF

The simplest low-pass filter is an RC circuit:



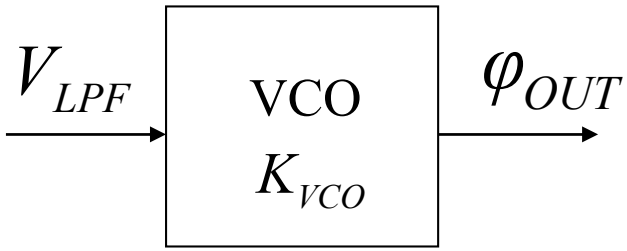
The cut-off frequency of the filter (in rad/s) is:

$$\omega_{LPF} = \frac{1}{RC}$$

In the s-domain:

$$\frac{V_{LPF}(s)}{V_{PD}(s)} = \frac{\frac{1}{sC}}{\frac{1}{sC} + R} = \frac{1}{1 + sRC} = \frac{1}{1 + \frac{s}{\omega_{LPF}}}$$

Transfer Function of the VCO



$$\varphi_{out} = \int \omega_{out} dt = \int_0^t \left(\omega_{fr} + K_{VCO} V_{LPF}\right) dt = \omega_{fr} t + K_{VCO} \int_0^t V_{LPF} dt$$

Considering only the *excess* phase:

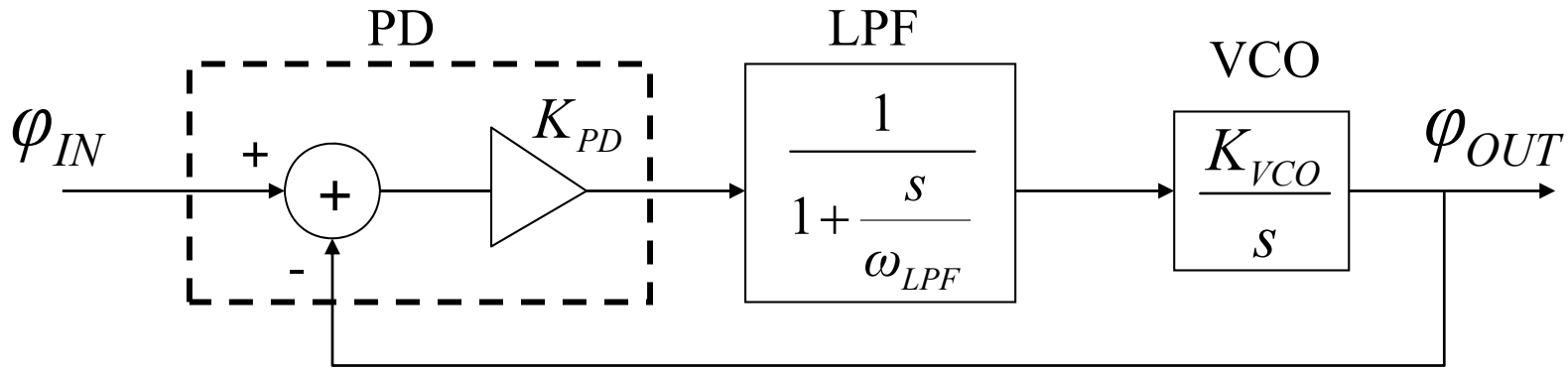
$$\varphi_{out} = K_{VCO} \int_0^t V_{LPF} dt$$

In the s-domain, integration corresponds to 1/s so:

$$\varphi_{out}(s) = \frac{K_{VCO}}{s} V_{LPF}(s) \Rightarrow \frac{\varphi_{out}(s)}{V_{LPF}(s)} = \frac{K_{VCO}}{s}$$

Type I PLL – Open Loop Transfer Function

The ideal phase detector can be considered to perform a “subtract” followed by a gain giving an overall system:



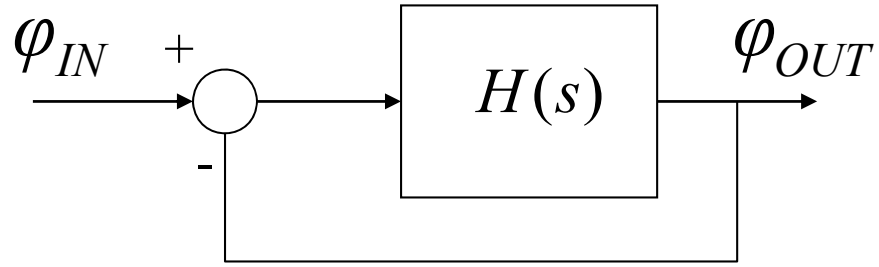
The Open Loop Transfer Function is:

$$H(s)\Big|_{OPEN} = \frac{\varphi_{OUT}(s)}{\varphi_{IN}(s)}\Bigg|_{OPEN} = K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s} = \frac{K_{PD}K_{VCO}}{s+\frac{s^2}{\omega_{LPF}}}$$

The open loop transfer function has a pole at s = 0 and another pole at s = $-\omega_{LPF}$

The single pole at the origin gives rise to the label “ Type I ”.

Closed Loop Transfer Function



$$\varphi_{OUT}(s) = H(s)\left(\varphi_{IN}(s) - \varphi_{OUT}(s)\right) \Rightarrow \varphi_{OUT}(s)\left(1 + H(s)\right) = H(s)\varphi_{IN}(s)$$

$$\Rightarrow \frac{\varphi_{OUT}(s)}{\varphi_{IN}(s)} = \frac{H(s)}{1 + H(s)} = \frac{1}{\frac{1}{H(s)} + 1}$$

Putting in the open loop H(s) from the previous slide and re-arranging gives:

$$H(s)\Big|_{CLOSED} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}$$

Type I PLL – A Second-Order System

The transfer function of a Type I PLL can be put in the form of the well-known second-order system:

$$H(s)\Big|_{CLOSED} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}} = \frac{K_{PD}K_{VCO}\omega_{LPF}}{s^2 + \omega_{LPF}s + K_{PD}K_{VCO}\omega_{LPF}} \equiv \frac{\omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2}$$

The natural frequency, damping factor and poles as related to the PLL characteristics as follows:

$$\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}} \qquad 2\varsigma\omega_n = \omega_{LPF} \Rightarrow \varsigma = \frac{1}{2}\frac{\omega_{LPF}}{\omega_n} = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$$

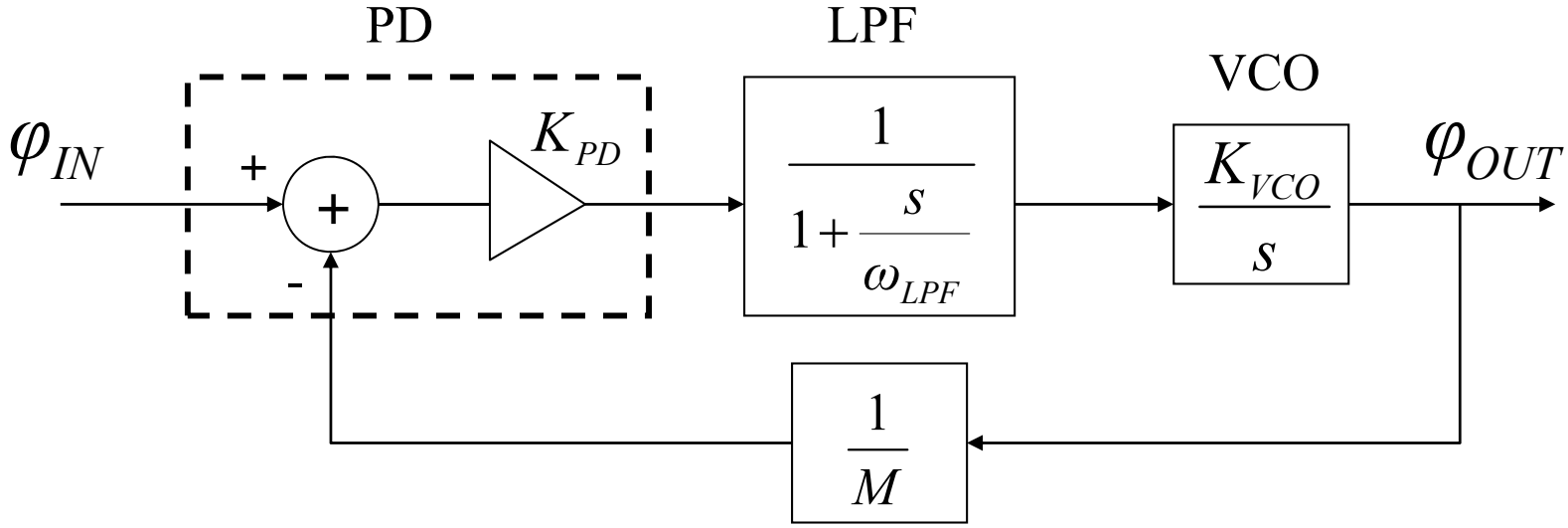
$$s_{1,2} = (-\varsigma \pm \sqrt{\varsigma^2 - 1})\omega_n$$

If $\zeta > 1$ both poles are real and the system is overdamped.

If $\zeta < 1$ the poles are complex and the response to a step change contains a sinusoid with frequency $\omega_n\sqrt{1-\varsigma^2}$ which decays with a time constant $(\varsigma\omega_n)^{-1}$.

$$\tau = \frac{1}{\varsigma\omega_n} = \frac{2}{\omega_{LPF}} = 2RC$$

Basic PLL Frequency Synthesizer

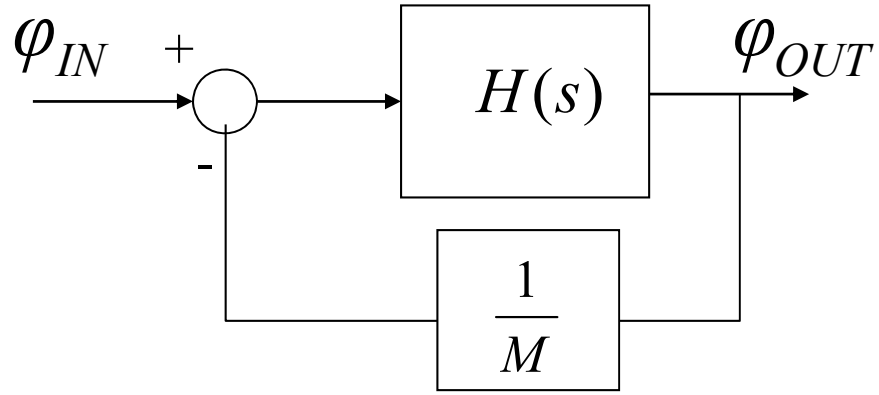


By dividing the frequency/phase by an integer M in the feedback path a general purpose frequency synthesizer is achieved allowing the output frequency to be modified by changing the feedback divide ratio:

$$\omega_{OUT} = M\omega_{IN}$$ In steady state

M is an integer so the frequency resolution of the synthesizer (the change of frequency if M changes by 1) is equal to the input frequency. Therefore the input frequency has to be set at the desired channel spacing in a communication system (e.g. 200kHz in GSM): $\Delta\omega_{OUT} = \omega_{IN}$

Closed Loop Transfer Function with Divider



$$\varphi_{OUT}(s) = H(s)\left(\varphi_{IN}(s) - \frac{\varphi_{OUT}(s)}{M}\right) \Rightarrow \varphi_{OUT}(s)\left(1 + \frac{H(s)}{M}\right) = H(s)\varphi_{IN}(s)$$

$$\Rightarrow \frac{\varphi_{OUT}(s)}{\varphi_{IN}(s)} = \frac{H(s)}{1 + \frac{H(s)}{M}} = \frac{1}{\frac{1}{H(s)} + \frac{1}{M}} = \frac{1}{s + \frac{s^2}{\omega_{LPF}}} = \frac{K_{PD}K_{VCO}}{s + \frac{s^2}{\omega_{LPF}} + \frac{K_{PD}K_{VCO}}{M}}$$

$$= \frac{K_{PD}K_{VCO}\omega_{LPF}}{s^2 + \omega_{LPF}s + \frac{K_{PD}K_{VCO}\omega_{LPF}}{M}}$$

Loop Constants with Divider

$$H(s)\Big|_{CLOSED} = \frac{K_{PD}K_{VCO}\omega_{LPF}}{s^2 + \omega_{LPF}s + \frac{K_{PD}K_{VCO}\omega_{LPF}}{M}} \equiv \frac{K_{PD}K_{VCO}\omega_{LPF}}{s^2 + 2\varsigma\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}\omega_{LPF}}{M}}$$

$$2\varsigma\omega_n = \omega_{LPF} \Rightarrow \varsigma = \frac{1}{2}\frac{\omega_{LPF}}{\omega_n} = \frac{1}{2}\sqrt{\frac{M\omega_{LPF}}{K_{PD}K_{VCO}}}$$

The loop dynamics change when the divider ratio changes so it's important to make sure that the PLL has good performance for all divider ratios to be used.
The product $K_{PD}K_{VCO}$ is often called the PLL or loop gain and just called K. The damping factor and the loop gain are not independent – if K is increased the damping factor decreases. Usually the damping factor is > 0.5 and sometimes it is set to $\sqrt{2}/2$ to provide an optimally flat frequency response.

Some Limitations of Type 1 PLL

If the synthesizer is required to have a very small output frequency step then the input frequency has to be very small. Usually, to give good stability, the cut-off frequency of the LPF is chosen to be 10%-20% of the input frequency. This causes the settling time constant of the filter to be relatively high making the switching from one frequency to another relatively slow.

The phase offset between the output and the input is frequency dependent. If this phase offset has to be small then $K_{PD}K_{VCO}$ can be increased but increasing $K_{PD}K_{VCO}$ gives a smaller damping factor and may cause instability.

Another limitation of Type 1 PLLs is that the "frequency acquisition range" can be fairly small – in the range of the cut-off frequency of the LPF i.e. if there is a large frequency step at the input or if the input frequency is substantially different from the VCO free-running frequency, then the loop may fail to lock.