Solutions UE4010 Summer 2006 Part A

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an NMOS in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.
In each question, capacitances other than those mentioned may be ignored.

Question 1

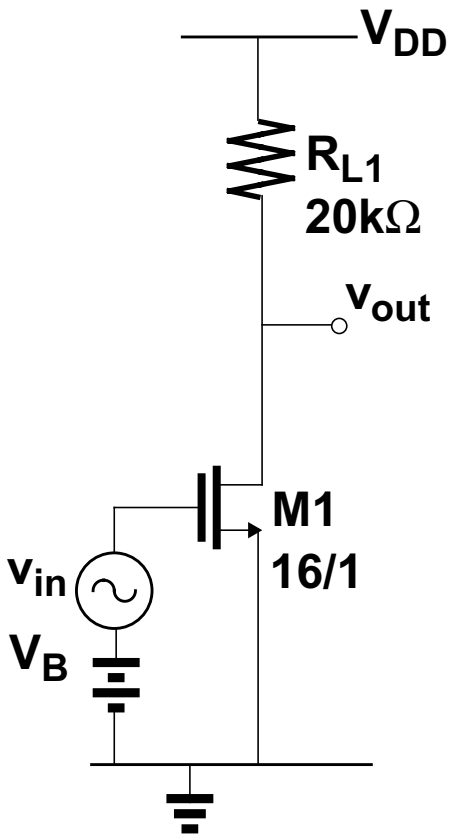

Figure 1a

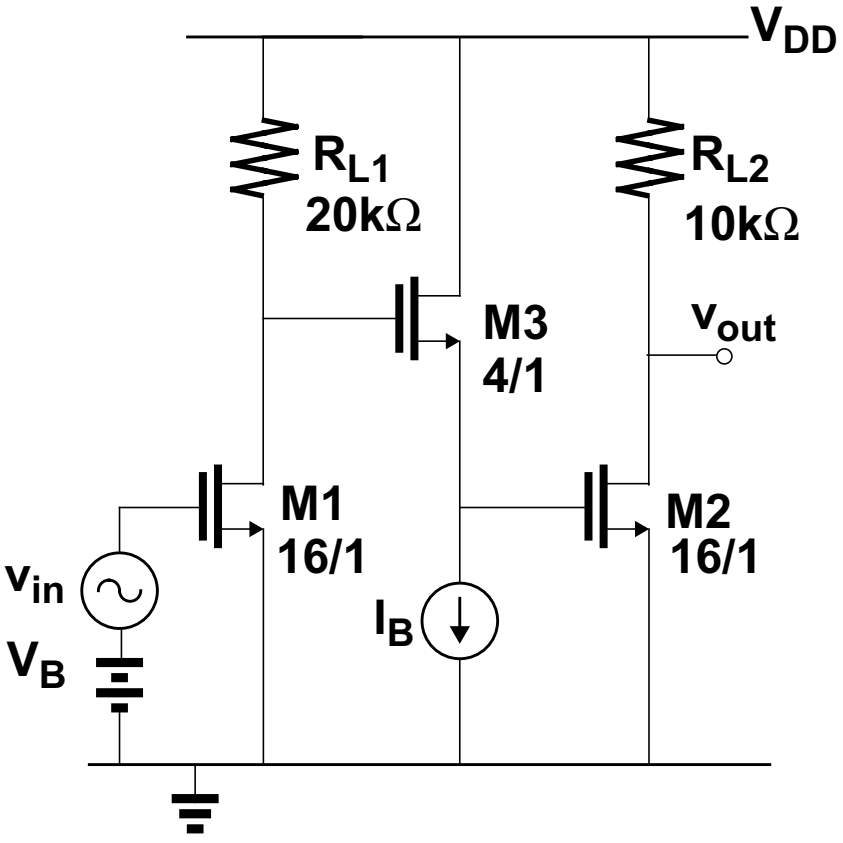

Figure 1b

Assume all transistors in the circuits shown in Figure 1a and 1b are biased in saturation.

(i) Draw the small-signal equivalent circuit for the common-source stage shown in Figure 1a.

(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) of this circuit in terms of the small-signal transistor parameters and R_{L1}.

(iii) Calculate the small-signal voltage gain (v_{out}/v_{in}) in dB if
V_{DD}=5V, V_B = 1V, V_{tn} = 0.75V, K_n'=200μA/V^2.
Assume $R_L << 1/g_{ds1}$. Transistor dimensions in microns, and resistor values are as shown in Figure 1a.

(iv) The stage shown in Figure 1a is cascaded with a similar stage, as shown in Figure 1b.
What value of I_B is required so that M2 has the same gate bias voltage as M1?
Calculate the small-signal voltage gain (v_{out}/v_{in}) in dB of the circuit in Figure 1b.
Assume the source-follower stage has unity gain.

(i) Draw the small-signal equivalent circuit for the CMOS common-source stage shown in Figure 1a.

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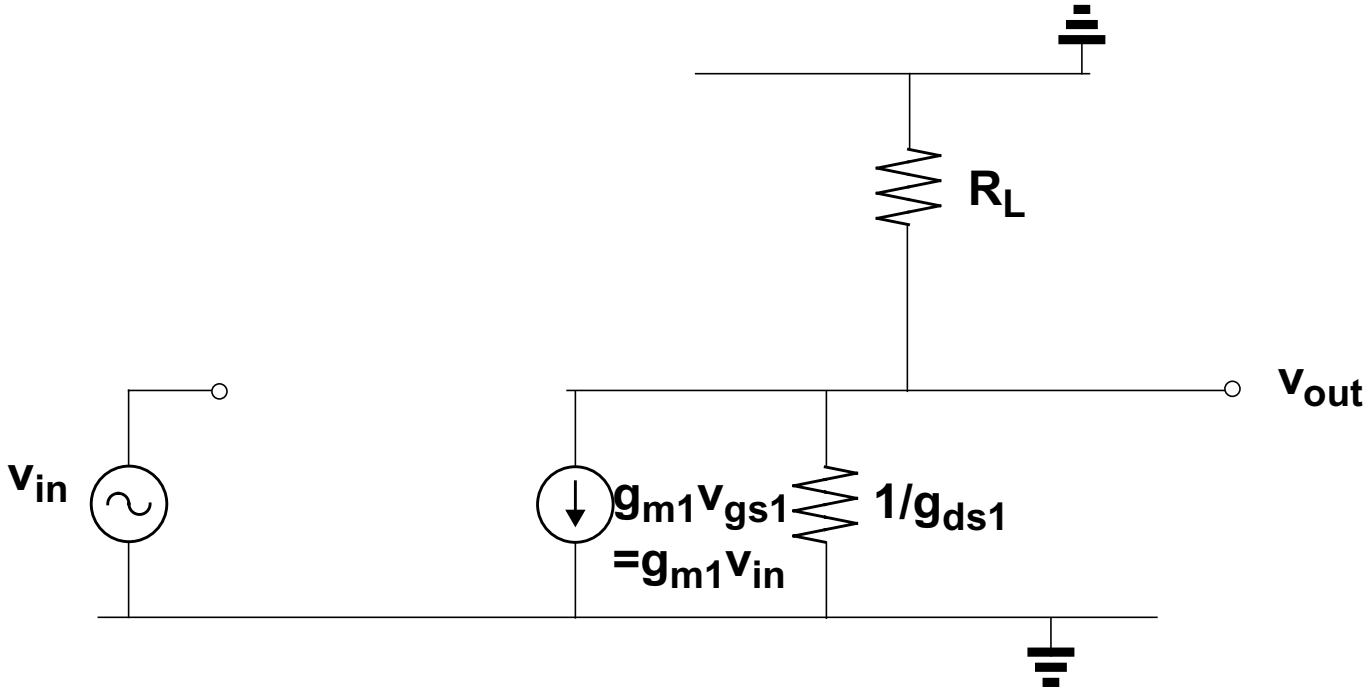

(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) of this circuit in terms of the small-signal transistor parameters and R_{L1}.

KCL at output node

$$g_{m1}v_{in} + v_{out}g_{ds1} + \frac{v_{out}}{R_L} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + \frac{1}{R_L}}$$

(iii) Calculate the small-signal voltage gain (v_{out}/v_{in}) in dB if
V_{DD}=5V, V_B = 1V, V_{tn} = 0.75V, K_n =200μA/V^2.
Assume $R_L << 1/g_{ds1}$. Transistor dimensions in microns, and resistor values are as shown in Figure 1a.

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$$I_{D1} = \frac{K'_n}{2}\frac{W}{L}(V_{GS1}-V_{tn})^2 = \frac{200\mu A/V^2}{2}\cdot\frac{16}{1}\cdot(1-0.75)^2 = 100\mu A$$

$$g_{m1} = \sqrt{2K'_n\frac{W}{L}I_{D1}} = \sqrt{2\times 200\mu A/V^2\times\frac{16}{1}\times 100\mu A} = 800\mu A/V$$

$$\frac{v_{out}}{v_{in}} \approx -g_{m1}R_{L1} = -800\mu A/V\times 20k\Omega = -16$$

$$20\log\left|\frac{v_{out}}{v_{in}}\right| = 24dB$$

(iv) The stage shown in Figure 1a is cascaded with a similar stage, as shown in Figure 1b.
What value of I_B is required so that M2 has the same gate bias voltage as M1?
Calculate the small-signal voltage gain (v_{out}/v_{in}) in dB of the circuit in Figure 1b.
Assume the source-follower stage has unity gain.

Output voltage of first stage is biased at

$$V_{OUT} = V_{DD} - I_{D1}R_L = 5V - 100\mu A\times 20k\Omega = 3V$$

Gate of M3 needs to be at 1V => source follower stage must levelshift down 2V so needs a V_{GS}-V_t of 1.25V

$$I_{D3} = \frac{K'_n}{2}\frac{W}{L}(V_{GS3}-V_{tn})^2 = \frac{200\mu A/V^2}{2}\cdot\frac{4}{1}\cdot 1.25^2 = 625\mu A$$

Total gain

$$\frac{v_{out}}{v_{in}} \approx -g_{m1}R_{L1}\times g_{m3}R_{L3} = -16\times -(800\mu A/V\times 10k\Omega) = 128$$

$$20\log\left|\frac{v_{out}}{v_{in}}\right| = 42dB$$

Question 2

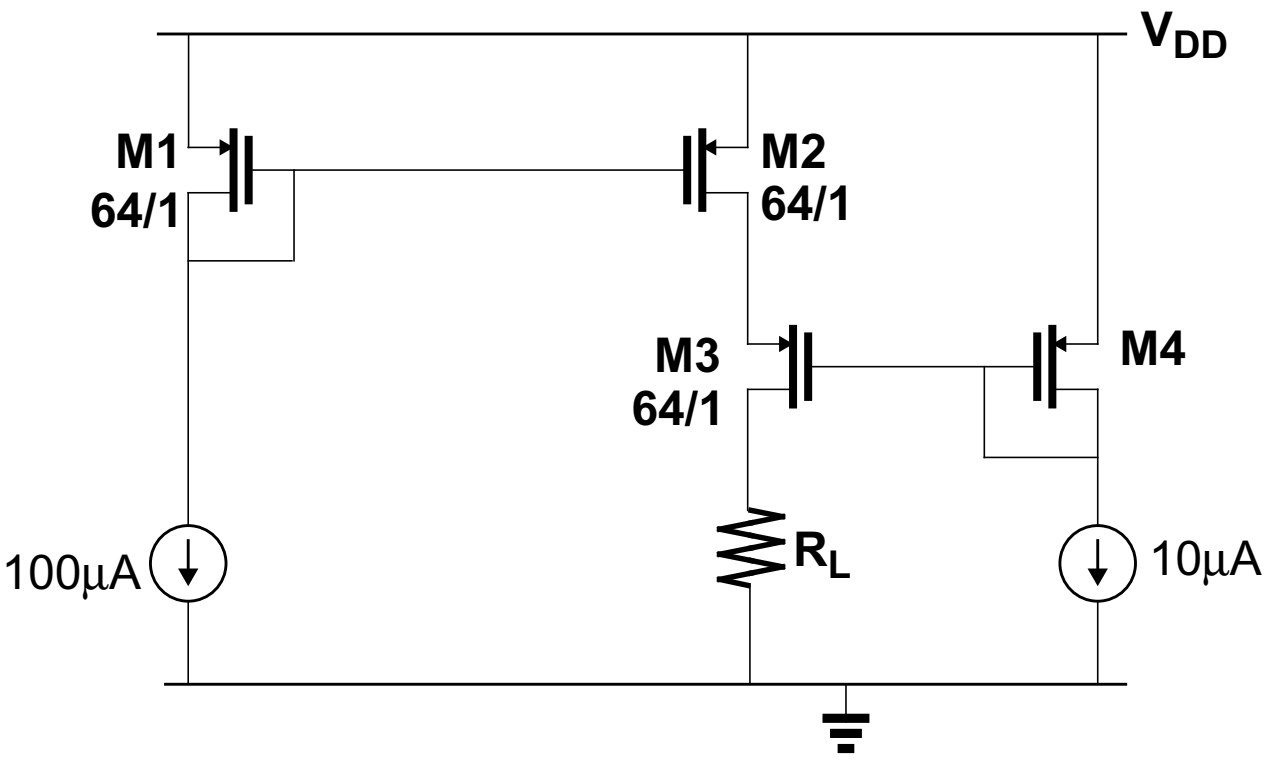


Figure 2

Figure 2 shows a PMOS current mirror (M1, M2) with cascoded output. The bias voltage for the cascode is generated by the diode-connected PMOS M4, which is biased by a current source as shown.

For this question K_p'=50µA/V^2, V_{tp}= -750mV, V_{DD}=3V.

The device sizes of M1, M2 and M3 in microns are as indicated in Figure 2.

(i) What is the maximum voltage at the drain of M2 such that M2 is just biased in saturation?
If M4 has L=10µm, what is the required value of W for M4 such that M2 is just biased in saturation, assuming M3 is in saturation?

(ii) What is then the maximum value of R_L such that M3 is also biased in saturation?

(iii) Given the bias conditions established in (i) and (ii), estimate the percentage inaccuracy of the current mirror due to the finite output conductance of M1 and M2.
For this calculation take λ_p=0.04V^{-1}.

(iv) Estimate the 3 sigma percentage inaccuracy of the current mirror due to transistor V_{tp} mismatch.
Note: Assume the mismatch is normally distributed and that the 1 sigma V_{tp} mismatch of a transistor pair (in mV) is given by

$$\sigma_{\Delta V_{tp}} = \frac{A_{V_{tp}}}{\sqrt{WL}}$$

Take A_{Vtp}= 10mVµm.

(i) What is the maximum voltage at the drain of M2 such that M2 is just biased in saturation?
If M4 has L=10μm, what is the required value of W for M4 such that M2 is just biased in saturation, assuming M3 is in saturation?

For M1,M2

$$\left|\left|V_{GS}\right| - \left|V_t\right|\right| = \sqrt{\frac{2I_D}{K_p' \frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{50\mu A/V^2 \frac{64}{1}}} = 250mV$$

This is the minimum source drain voltage required for M2 to be in saturation.

The maximum voltage at the drain of M2 is then given by V_{DD} minus this voltage

$$V_{D2max} = V_{DD} - 0.25V = \underline{\underline{2.75V}}$$

For M4

As M3 has same dimensions, same current as M1, M2, it has the same V_{GS}

$$\left|V_{GS3}\right| = \left|V_{GS1}\right| = (\left|V_{GS1}\right| - \left|V_t\right|) + \left|V_t\right| = 0.25V + 0.75V = 1V$$

$$\left|V_{GS4}\right| = \left|V_{GS3}\right| + \left|V_{DS2min}\right|$$

$$= 1 + 0.25V$$

$$= 1.25V$$

$$\left|I_{D4}\right| = \frac{K_p'}{2}\frac{W}{L}(\left|V_{GS4}\right| - \left|V_t\right|)^2 \Rightarrow W = \frac{2\left|I_{D4}\right|}{K_p' \frac{1}{L}(\left|V_{GS4}\right| - \left|V_t\right|)^2}$$

$$W = \frac{2 \cdot 10\mu A}{50\mu A/V^2 \frac{1}{10}(1.25 - 0.75)^2} = 16$$

(ii) What is then the maximum value of R_L such that M3 is also biased in saturation?

Maximum voltage at drain of M3

$$V_{D3max} = V_{D2max} - (|V_{GS3}| - |V_t|) = 2.75V - 0.25V = 2.5V$$

Maximum value of R_L is then given by

$$R_{Lmax} = \frac{V_{D3max}}{I_{D3}} = \frac{2.5}{100\mu A} = 25k\Omega$$

(iii) Given the bias conditions established in (i) and (ii), estimate the percentage inaccuracy of the current mirror due to the finite output conductance of M1 and M2.
For this calculation take $\lambda_p=0.04V^{-1}$.

$$I_{D1} = \frac{K'_p}{2}\frac{W}{L}(|V_{GS1}| - |V_{tp}|)^2(1 + \lambda_p|V_{DS1}|)$$

$$I_{D2} = \frac{K'_p}{2}\frac{W}{L}(|V_{GS2}| - |V_{tp}|)^2(1 + \lambda_p|V_{DS2}|)$$

$$\frac{I_{D2}}{I_{D1}} = \frac{1 + \lambda_p|V_{DS2}|}{1 + \lambda_p|V_{DS1}|} = \frac{1 + 0.04 \cdot 0.25}{1 + 0.04 \cdot 1.00} = 0.971$$

Percentage inaccuracy = -2.9%

(iv) Estimate the 3 sigma percentage inaccuracy of the current mirror due to transistor V_{tp} mismatch.
Note: Assume the mismatch is normally distributed and that the 1 sigma V_{tp} mismatch of a transistor pair (in mV) is given by

$$\sigma_{\Delta V_{tp}} = \frac{A_{V_{tp}}}{\sqrt{WL}}$$

Take A_{Vtp}= 10mVμm.

$$\sigma_{Vtp} = \frac{A_{Vtp}}{\sqrt{WL}} = \frac{10mV\mu m}{\sqrt{64\mu m \cdot 1\mu m}} = 1.25mV$$

This is the 1σ mismatch in V_{tp} of M1 and M2

This value is small compared to the overdrive voltage $|V_{GS}|-|V_{tp}|$

=> Use small-signal analysis to calculate inaccuracy

$$g_m = \frac{2I_D}{|V_{GS}| - |V_{tp}|} = \frac{2 \times 100\mu A}{0.25V} = 0.8mA/V = 0.8\mu A/mV$$

$$\sigma_{I_D} = g_m \sigma_{Vt} = 1.25mV \cdot 0.8\mu A/mV = 1\mu A$$

i.e. 1σ sigma mismatch in drain currents of 1%

3σ percentage mismatch is +/-6%

Question 3

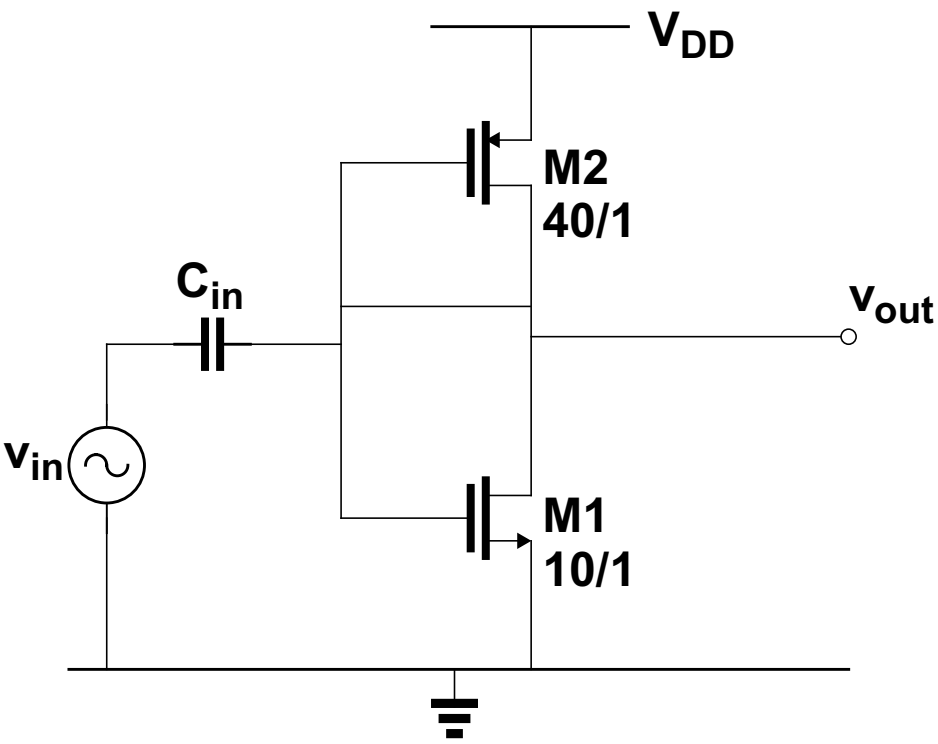


Figure 3

For the questions below you may assume $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$ and that all devices are biased in saturation.
Transistor dimensions in microns are as shown in Figure 3.

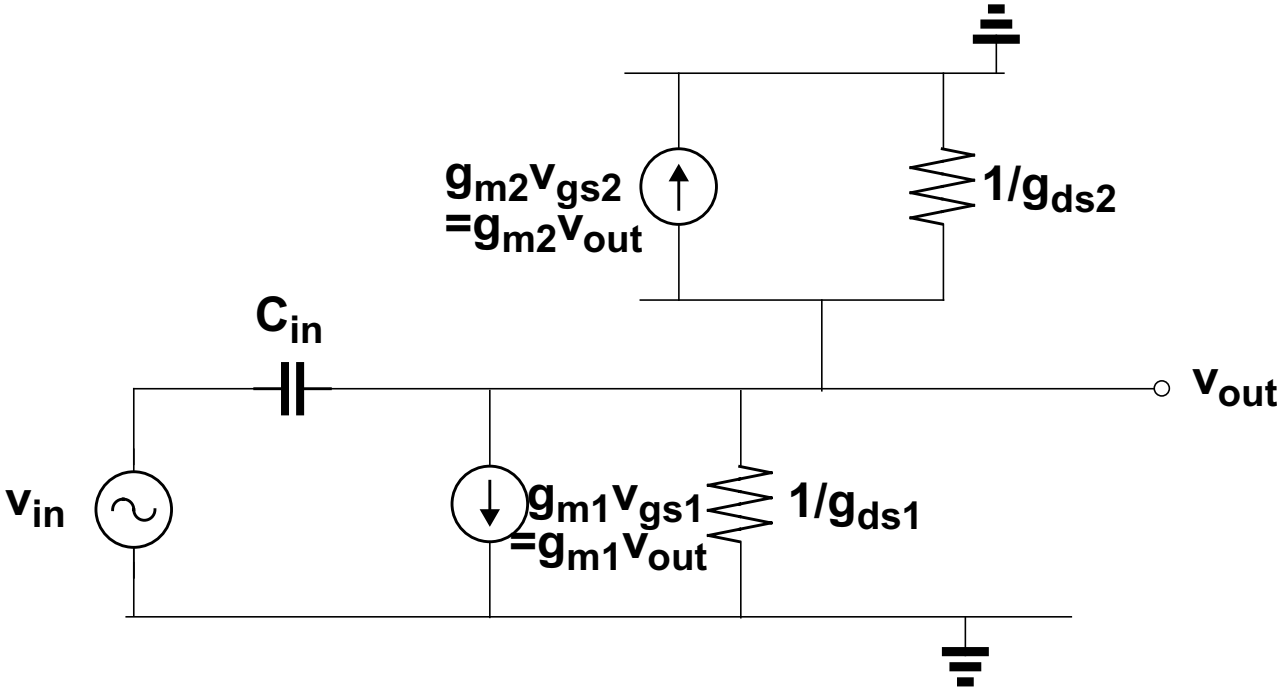
(i) Figure 3 shows a CMOS inverter stage. The input signal v_{in} is capacitively coupled into the stage through the capacitor C_{in}.
Draw the small-signal model for this circuit.

(ii) Ignoring all capacitances except C_{in}, derive an expression for the high-frequency transfer function of the small-signal voltage gain (v_{out}/v_{in}) of the circuit shown in Figure 3.

(iii) Calculate the break frequencies (i.e. pole and/or zero frequencies) if
V_{DD} = 3V, V_{tn} = $|V_{tp}|$ = 0.7V, K_n'=200μA/V^2,K_p'=50μA/V^2,C_{in}= 1nF.

(iv) Draw a Bode diagram of the gain response.
What is the value of gain at frequencies well above the break frequencies?

(i) Figure 3 shows a CMOS inverter stage. The input signal v_{in} is capacitively coupled into the stage through the capacitor C_{in}.
Draw the small-signal model for this circuit.



(ii) Ignoring all capacitances except C_{in}, derive an expression for the high-frequency transfer function of the small-signal voltage gain (v_{out}/v_{in}) of the circuit shown in Figure 3.

KCL at output node

$$g_{m1}v_{out} + g_{m2}v_{out} + v_{out}g_{ds1} + v_{out}g_{ds2} + (v_{out} - v_{in})sC_{in} = 0$$

$$\frac{v_{out}}{v_{in}} = \frac{sC_{in}}{g_{m1} + g_{m2} + g_{ds1} + g_{ds2} + sC_{in}}$$

$$\frac{v_{out}}{v_{in}} = \frac{sC_{in}}{(g_{m1} + g_{m2} + g_{ds1} + g_{ds2})\left(1 + \dfrac{sC_{in}}{g_{m1} + g_{m2} + g_{ds1} + g_{ds2}}\right)}$$

$$\frac{v_{out}}{v_{in}} \approx \frac{sC_{in}}{(g_{m1} + g_{m2})\left(1 + \dfrac{sC_{in}}{g_{m1} + g_{m2}}\right)}$$

Alternatively use $1/g_m$ approx. for diode connected M2 and get simpler derivation

(iii) Calculate the break frequencies (i.e. pole and/or zero frequencies) if V_{DD} = 3V, $V_{tn} = |V_{tp}|$ = 0.7V, K_n'=200μA/V^2,K_p'=50μA/V^2,C_{in}= 1nF.

The high-frequency transfer function shows a zero at dc and a high frequency pole

Zero frequency is at dc.

Pole frequency given by

$$|\omega_p| = \frac{g_{m1} + g_{m2}}{C_{in}}$$

Claculate g_{m1},g_{m2}
$I_{D1}=|I_{D2}|$=>

$$\frac{K_n'}{2}\frac{W_1}{L_1}(V_{GS1}-V_{tn})^2 = \frac{K_p'}{2}\frac{W_2}{L_2}(|V_{GS2}|-|V_{tp}|)^2$$

With the values given this reduces to

$$(V_{GS1}-V_{tn}) = (|V_{GS2}|-|V_{tp}|)$$

With V_{DD}=3V, and $|V_{tp}| = V_{tn}$, this gives $V_{GS1}=|V_{GS2}|$=1.5V

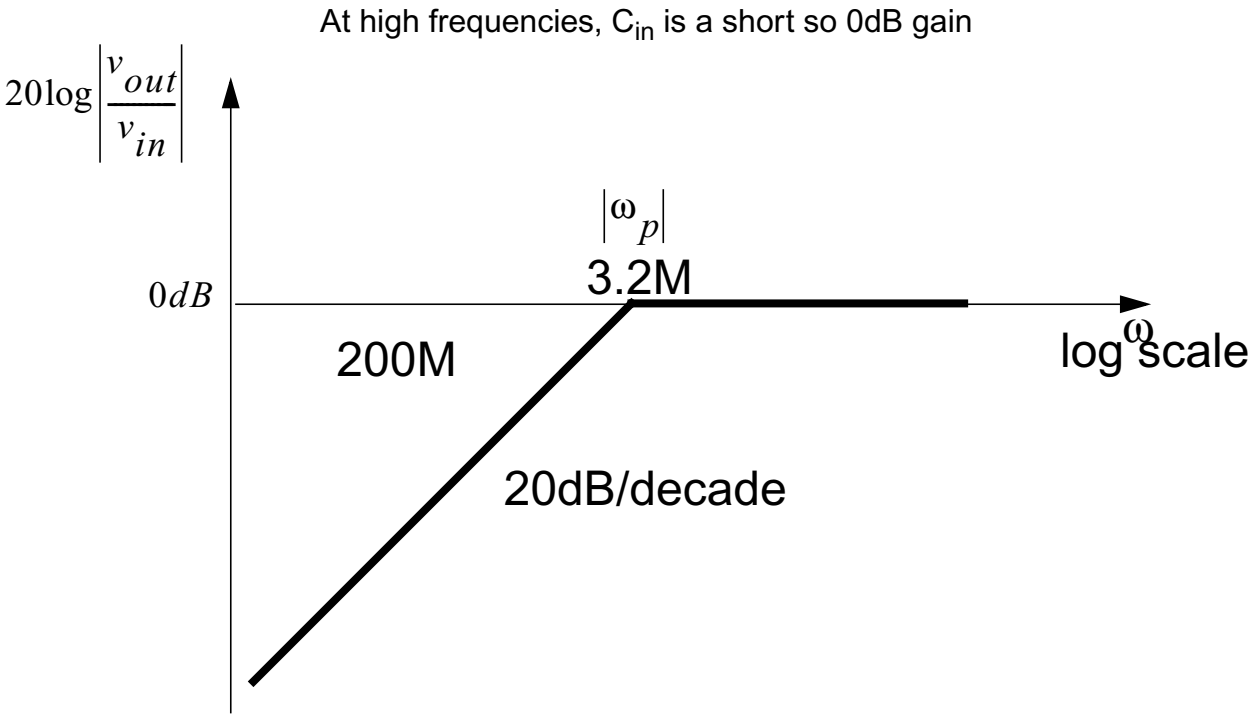
$$I_{D1} = \frac{K_n'}{2}\frac{W}{L}(V_{GS1}-V_{tn})^2 = \frac{200\mu A/V^2}{2}\cdot\frac{10}{1}\cdot(1.5-0.7)^2 = 640\mu A$$

=> 640μA through M1, M2.

$$g_{m1} = \frac{2I_D}{V_{GS}-V_t} = \frac{2\times 640\mu A}{0.8V} = 1.6mA/V = g_{m1}$$

$$|\omega_p| = \frac{g_{m1} + g_{m2}}{C_{in}} = \frac{1.6mA/V + 1.6mA/V}{1nF} = 3.2Mrad/s$$

(iv) Draw a Bode diagram of the gain response.
What is the value of gain at frequencies well above the break frequencies.



Question 4

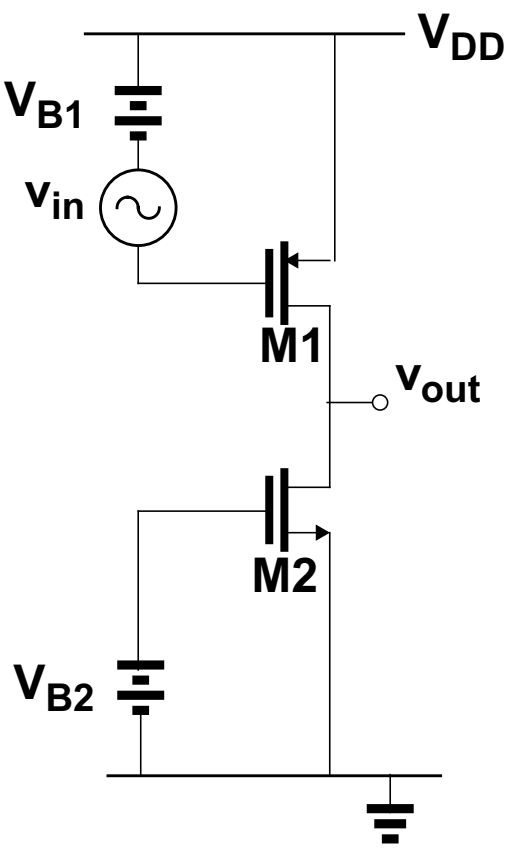


Figure 4a

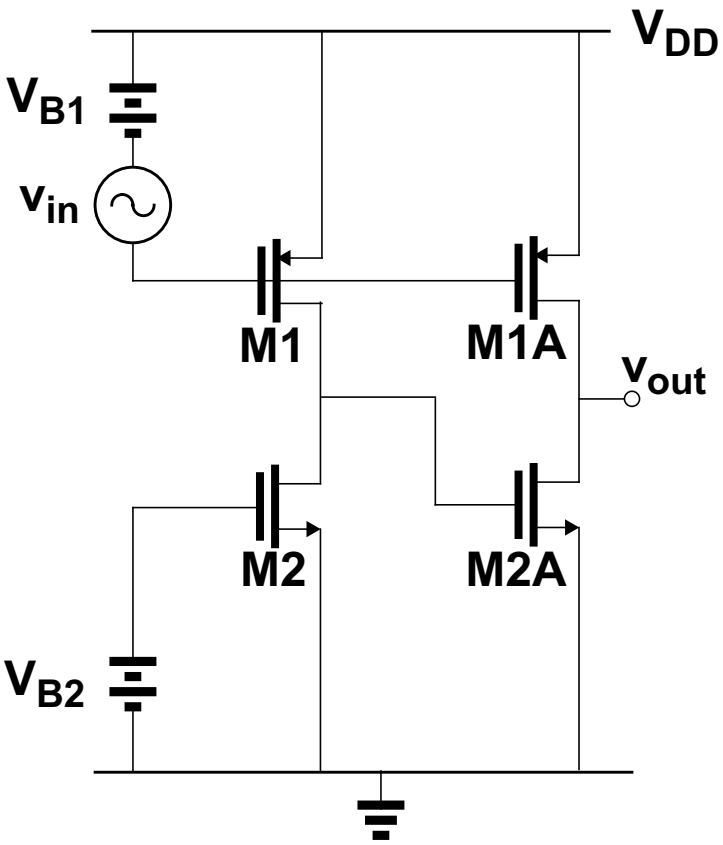


Figure 4b

For the circuits shown in Figure 4a and 4b, assume all transistors are operating in saturation.
Only thermal noise sources need be considered.

Take Boltzmann's constant $k=13.8X10^{-24}J/^oK$, temperature $T=300^oK$.

(i) Draw the small-signal model for the circuit shown in Figure 4a.
What is the low-frequency small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters of M1 and M2?

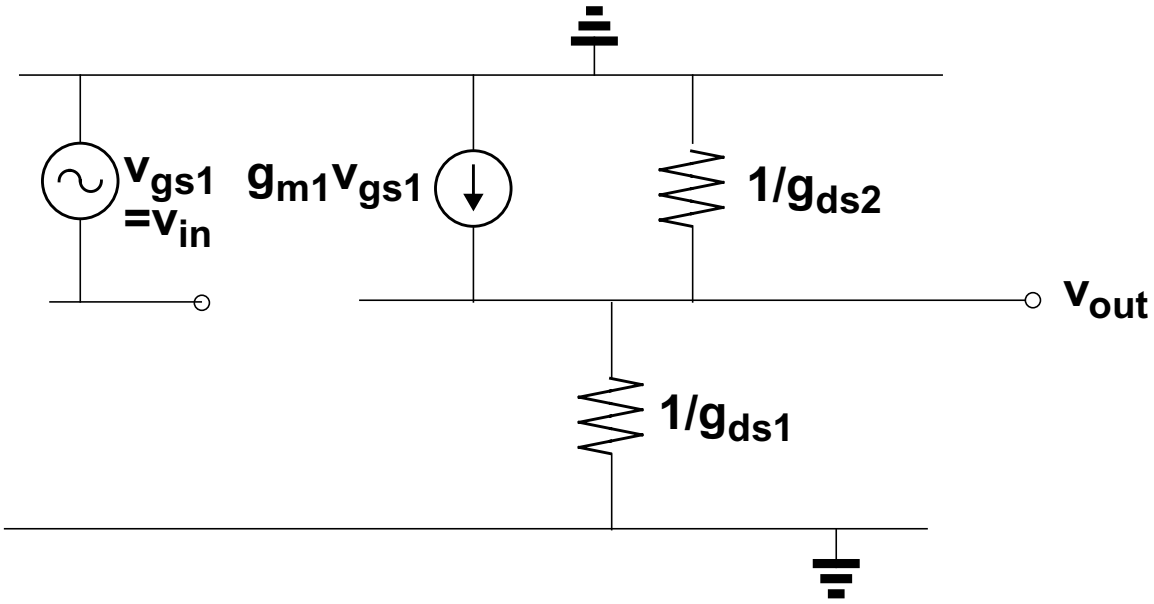
(ii) What is the input-referred noise voltage density in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T?

(iii) Calculate the input-referred noise voltage density if $g_{m1}=100\mu A/V$, $g_{m2}=40\mu A/V$, $g_{ds1}=g_{ds2}=2\mu A/V$.
What is the noise voltage density at the output?
(Note: the units $\mu A/V$ are equivalent to μS).

(iv) The gain stage shown in Figure 4a is cascaded with an identcal gain stage, with identical transistor dimensions and biasing conditions, as shown in Figure 4b. Calculate the input-referred noise voltage density of this circuit.
What is the total input-referred noise in a bandwidth of 1MHz to 10MHz?

Solution

(i) Draw the small-signal model for the circuit shown in Figure 4a.
What is the low-frequency small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters of M1 and M2?

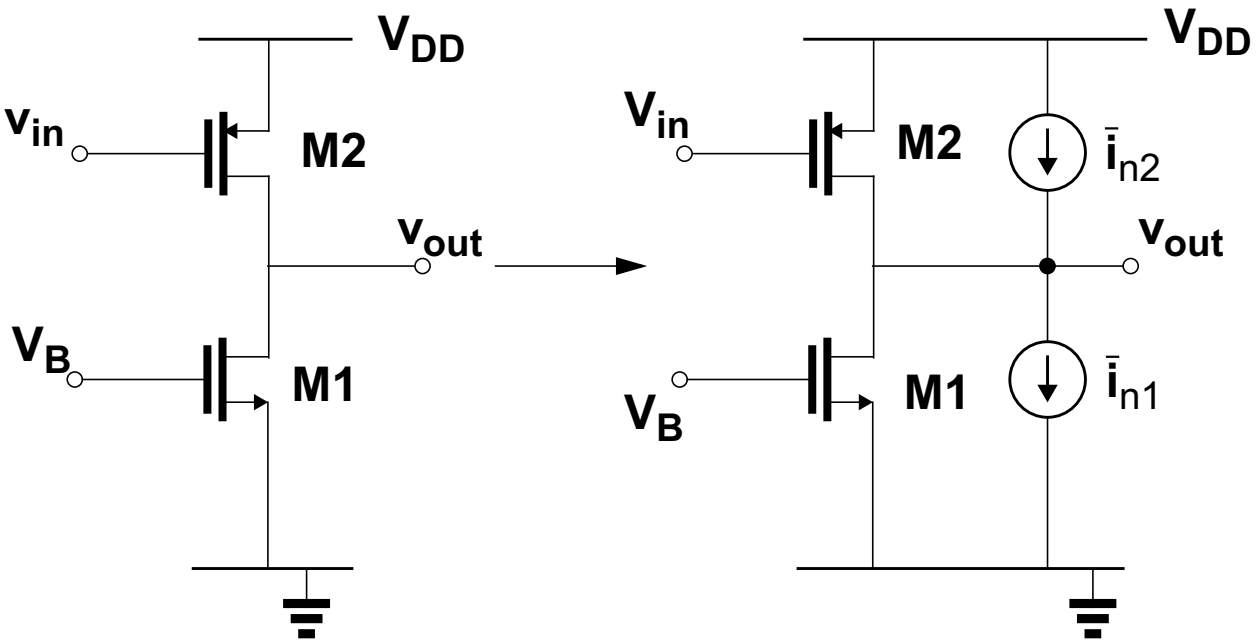


Current at output node

$$g_{m1}v_{in} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

(ii) What is the input-referred noise voltage density in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T?



Noise current of MOS: $\overline{i_n^2} = 4kT\left(\frac{2}{3}g_m\right)$

Noise sources uncorrelated => total noise is the sum of squares

$$\overline{i_{nt}^2} = i_{n1}^2 + i_{n2}^2 \quad \text{or} \quad \overline{i_{nt}} = \sqrt{i_{n1}^2 + i_{n2}^2} \quad \text{rms value}$$

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}}{g_{m1}} \quad \text{rms noise} \quad V/\sqrt{Hz}$$

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \sqrt{4kT \cdot \frac{2}{3}\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2}\right)}$$

(iii) Calculate the input-referred noise voltage density if g_{m1}=100μA/V, g_{m2}=40μA/V,g_{ds1}=g_{ds2}=2μA/V. What is the noise voltage density at the output?
(Note: the units μA/V are equivalent to μS).

Noise density at input

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \sqrt{4kT \cdot \frac{2}{3}\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2}\right)} = \sqrt{4kT \cdot \frac{2}{3}\left(\frac{1}{100\mu A/V} + \frac{40\mu A/V}{(100\mu A/V)^2}\right)} = 12.4nV/(\sqrt{Hz})$$

To get voltage noise at output multiply input-referred noise by gain of circuit

$$\overline{v_{no}} = \overline{v_{ni}}\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

$$Gain = \frac{g_{m1}}{g_{ds1} + g_{ds2}} = \frac{100\mu A/V}{2\mu A/V + 2\mu A/V} = 25$$

$$\overline{v_{no}} = 12.4nV/(\sqrt{Hz}) \times 20 = 311nV/(\sqrt{Hz})$$

(iv) The gain stage shown in Figure 4a is cascaded with an identcal gain stage, with identical transistor dimensions and biasing conditions, as shown in Figure 4b. Calculate the input-referred noise voltage density of this circuit. What is the total input-referred noise in a bandwidth of 1MHz to 10MHz?

Input Noise density of second stage is divided by gain of second stage and added quadratically to noise of first stage

$$\overline{v_{nitot}} = \sqrt{v_{ni1}^2 + \left(\frac{v_{ni2}}{Gain}\right)^2} = \sqrt{12.4^2 + \left(\frac{12.4}{20}\right)^2} \approx 12.4nV/(\sqrt{Hz})$$

Alternatively point out that noise of second stage divided by gain of first stage makes it negligible.

$$\overline{v_{nitot1to10MHz}} = v_{nitot}\sqrt{9MHz} = (12.4nV/(\sqrt{Hz}))\sqrt{9MHz} \approx 37.2\mu V$$