Solutions UE4010 Autumn 2004 Part A

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an nmos in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.

Question 1

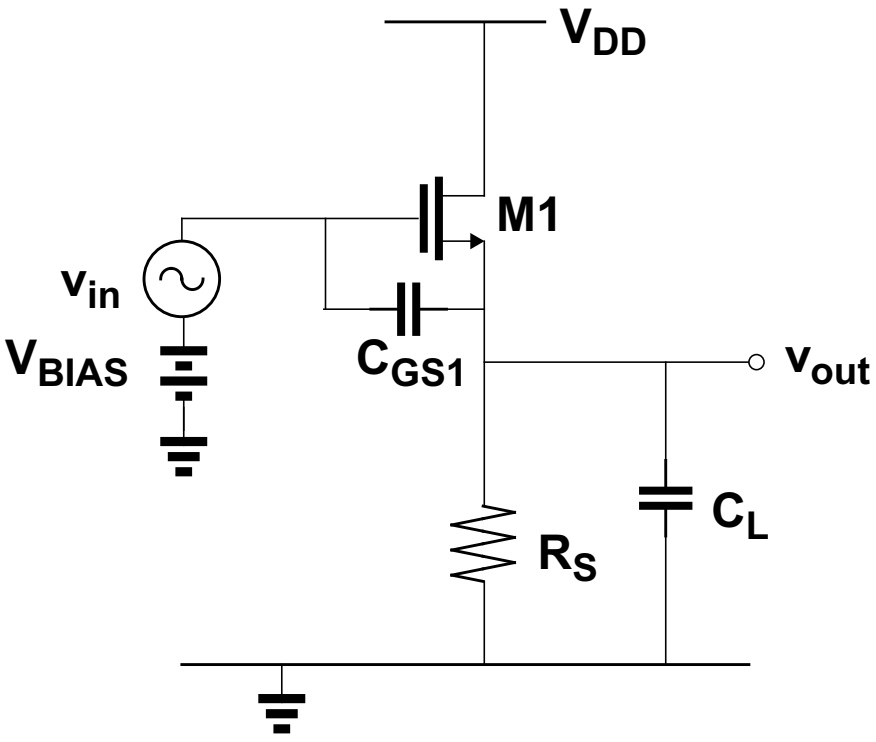
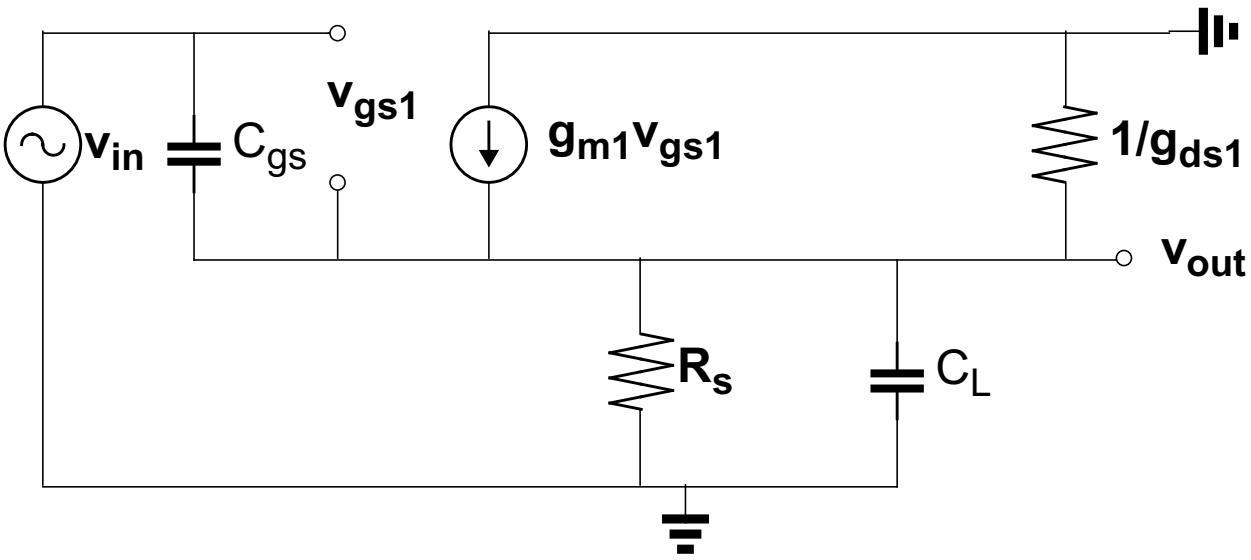


Figure 1

Figure 1 shows a source follower driving a resistive load. Assume M1 is in saturation and $g_{m1} >> g_{ds1}$.

(i) Draw the small-signal equivalent circuit for the source follower stage shown in Figure 1.
(ii) Ignoring all capacitances except C_{GS1} and C_L derive an expression for the high frequency transfer function.
(iii) Calculate the dc gain, pole and zero frequencies if V_{BIAS}=1.5V, K_n'=200μA/V^2, V_{tn}=0.75V, I_{D1}=100μA, W_1=16μm, L_1=1μm, C_{GS1}=1pF, C_L=9pF.
(iv) Draw a Bode diagram of the gain. On the diagram indicate the pole and zero frequencies, the value of the dc gain, and the value of the gain at frequencies well above the pole and zero frequencies.

(i) Draw the small signal equivalent circuit



(ii) Ignoring all capacitances except Cgs and CL derive an expression for the high frequency transfer function

KCL at output node

$$(v_{in}-v_{out})sC_{gs1}+g_{m1}(v_{in}-v_{out})-(v_{out}g_{ds1})-\frac{v_{out}}{R_s}-v_{out}sC_L=0$$

$$(g_{m1}+sC_{gs1})v_{in}=\left(g_{m1}+g_{ds1}+\frac{1}{R_s}+sC_{gs1}+sC_L\right)v_{out}$$

$$\frac{v_{out}}{v_{in}}=\frac{g_{m1}+sC_{gs1}}{g_{m1}+g_{ds1}+\frac{1}{R_s}+sC_{gs1}+sC_L}$$

$$\frac{v_{out}}{v_{in}}=\frac{g_{m1}}{g_{m1}+g_{ds1}+\frac{1}{R_s}}\frac{\left(1+\frac{sC_{gs1}}{g_{m1}}\right)}{\left(1+\frac{s(C_{gs1}+C_L)}{g_{m1}+g_{ds1}+\frac{1}{R_s}}\right)}$$

(iii) Calculate the dc gain, pole and zero frequencies if V_{BIAS}=1.5V, V_{tn}=0.75V, I_{D1}=100μA,

W_1=16µm, L_1=µm, C_{GS1}=1pF, C_L=9pF.

Bias conditions:

$$V_{GS1} - V_t = \sqrt{\frac{2I_{D1}}{K_n' \frac{W_1}{L_1}}} = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V^2 \frac{16}{1}}} = 250mV$$

$$V_{GS1} = V_{GS1} - V_t + V_t = 250mV + 750mV = 1V$$

$$I_D R_S = V_{BIAS} - V_{GS1} = 1.5V - 1V = 0.5V$$

$$R_S = \frac{0.5V}{100\mu A} = 5k\Omega$$

$$g_{m1} = \frac{2I_D}{(V_{GS1} - V_t)} = \frac{2 \times 100\mu A}{1 - 0.75} = 800\mu A/V$$

DC gain given by

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1} + \frac{1}{R_s}} \approx \frac{g_{m1}}{g_{m1} + \frac{1}{R_s}} = \frac{800\mu A/V}{800\mu A/V + \frac{1}{5k\Omega}} = 0.8$$

$$20\log\left|\frac{v_{out}}{v_{in}}\right| = -2dB$$

Pole frequency given by

$$|\omega_p| = \frac{g_{m1} + g_{ds1} + \frac{1}{R_s}}{(C_{gs1} + C_L)} \approx \frac{g_{m1} + \frac{1}{R_s}}{(C_{gs1} + C_L)}$$

$$|\omega_p| \approx \frac{800\mu A/V + \frac{1}{5k\Omega}}{1pF + 9pF} = 100Mrad/s$$

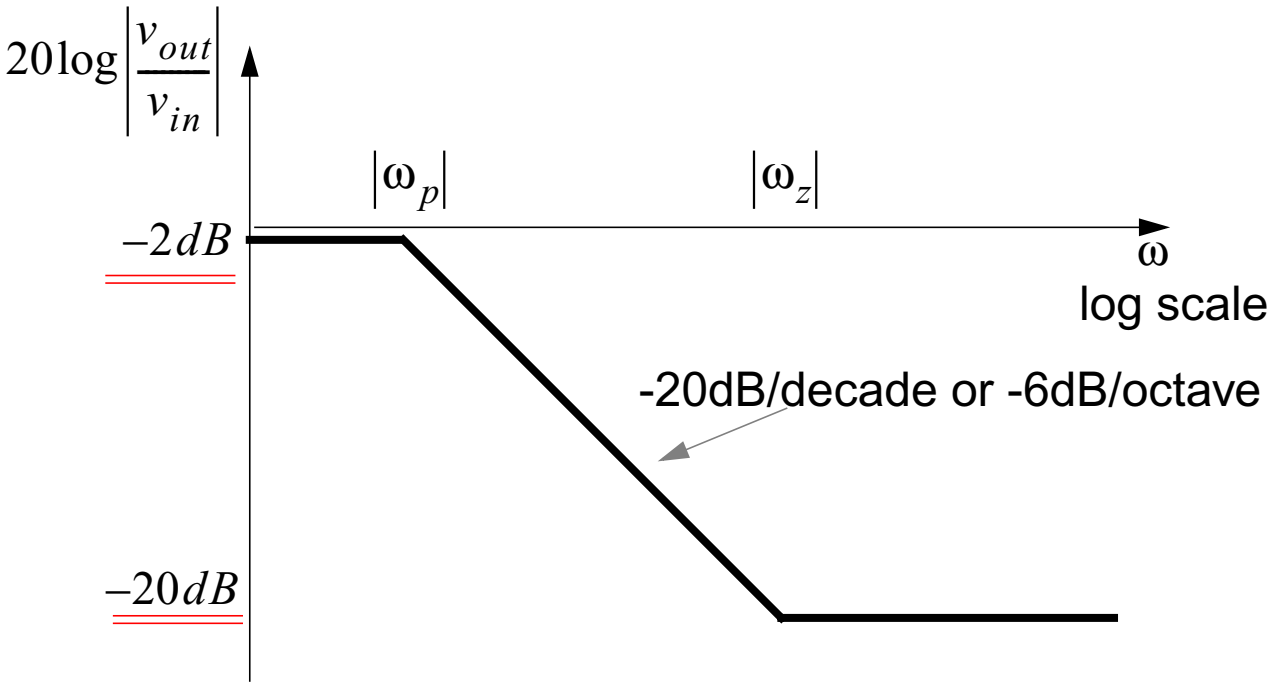
Zero frequency given by

$$|\omega_z| = \frac{g_{mn}}{C_{gs1}} = \frac{800\mu A/V}{1pF} = 800Mrad/s$$

(iv) Draw a Bode diagram of the gain. Indicate the dc gain and the gain at frequencies well above the pole and zero frequencies..

DC gain is -2dB

HF gain is 18dB down (since zero is 3 octaves above pole).



Question 2

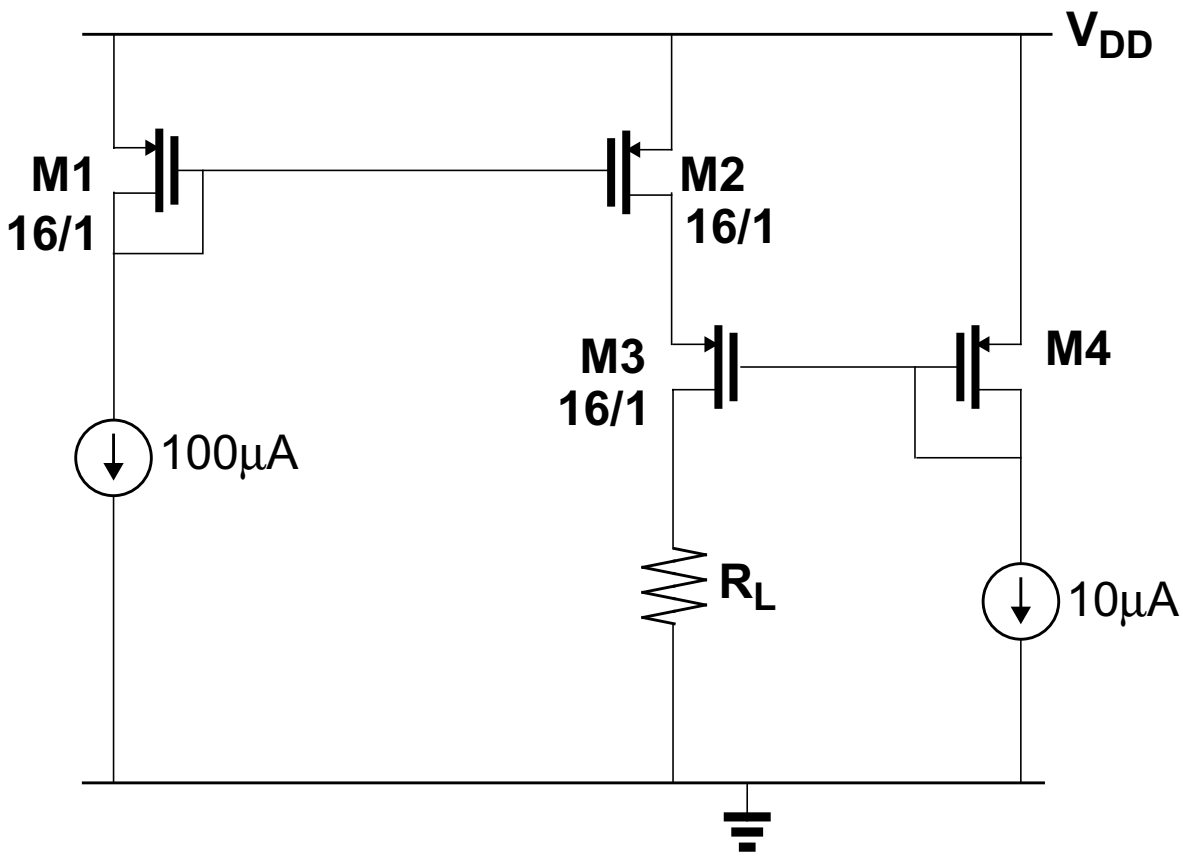


Figure 2

Figure 2 shows a pmos current mirror (M1, M2) with cascoded output. The bias voltage for the cascode is generated by the pmos diode M4.

For this question K_p'=50µA/V^2, V_{tp}= -750mV, V_{DD}=3V.

The device sizes of M1, M2 and M3 in microns are as indicated in Figure 2.

All devices are biased in saturation. For dc biasing calculations take λ=0.

(i) What is the maximum voltage at the drain of M2 such that M2 is just biased in saturation? If M4 has L=10, what is the required value of W for M4 such that M2 is just biased in saturation?

(ii) What is then the maximum value of R_L such that M3 is also biased in saturation?

(iii) Given the bias conditions established in (i) and (ii), estimate the percentage inaccuracy of the current mirror due to the finite output conductance of M1 and M2. For this calculation take λ_p=0.04V^{-1}.

(iv) Estimate the 3 sigma percentage inaccuracy of the current mirror due to transistor V_t mismatch. Note: Assume the mismatch is normally distributed and that the 1 sigma V_t mismatch of a transistor pair (in mV) is given by

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{WL}}$$

Take A_{Vt} = 10mVµm.

(i) What is the maximum voltage at the drain of M2 such that M2 is just biased in saturation?
If M4 has L=10, what is the required value of W for M4 such that M2 is just biased in saturation?

For M1

$$|V_{GS1} - V_t| = \sqrt{\frac{2I_{D1}}{K_p' \frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{50\mu A/V^2 \frac{16}{1}}} = 500mV$$

This is the minimum source drain voltage required for M2 to be in saturation.

$$V_{D4max} = V_{DD} - |V_{GS1} - V_t| = 3 - 0.5 = \underline{2.5V}$$

As M3 has same dimensions, same current as M1 it has the same V_{GS}

For M4

$$\begin{aligned} |V_{GS4}| - |V_t| &= |V_{GS3}| + |V_{DS1}| - |V_t| \\ &= |V_{GS3} - V_t| + |V_t| + |V_{DS1}| - |V_t| \\ &= 500mV + 500mV \\ &= 1V \end{aligned}$$

$$I_{D4} = \frac{K_P'}{2}\frac{W}{L}(V_{GS4} - V_t)^2 \Rightarrow W = \frac{2I_{D4}}{K_P' \frac{1}{L}(V_{GS4} - V_t)^2}$$

$$W = \frac{2 \cdot 10\mu A}{50\mu A/V^2 \frac{1}{10}(1)^2} = \underline{4}$$

(ii) What is then the maximum value of R_L such that M3 is also biased in saturation?

Maximum voltage at drain of M3

$$V_{D3max} = V_{DD} - |V_{GS2} - V_t| - |V_{GS3} - V_t| = 3 - 0.5 - 0.5 = 2V$$

Maximum value of R_L is then given by

$$R_{Lmax} = \frac{V_{D3max}}{I_{D3}} = \frac{2V}{100\mu A} = \underline{20k\Omega}$$

(iii) Estimate the percentage inaccuracy of the current mirror due to the finite output conductance of M1 and M2?

$$I_{D1} = \frac{K'_p}{2}\frac{W}{L}\left(|V_{GS2}| - |V_{tp}|\right)^2\left(1 + \lambda_p|V_{DS1}|\right)$$

$$I_{D2} = \frac{K'_p}{2}\frac{W}{L}\left(|V_{GS2}| - |V_{tp}|\right)^2\left(1 + \lambda_p|V_{DS1}|\right)$$

$$\frac{I_{D2}}{I_{D1}} = \frac{1 + \lambda_p|V_{DS2}|}{1 + \lambda_p|V_{DS1}|} = \frac{1 + 0.04 \cdot 0.5}{1 + 0.04 \cdot 1.25} = 0.976$$

Percentage inaccuracy = -2.4%

(iv) Estimate the 3 sigma percentage inaccuracy of the current mirror due to transistor V_t mismatch.
Note: The 1 sigma V_t mismatch of a transistor pair in mV is given by

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{WL}}$$

Take A_{Vt} = 10mVμm.

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{WL}} = \frac{10mV\mu m}{\sqrt{16\mu m \cdot 1\mu m}} = 2.5mV$$

This is the 1σ mismatch in V_t of M1 and M2

This value is small compared to the overdrive voltage V_{GS}-V_t

=> Use small-signal analysis to calculate inaccuracy

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2 \times 100\mu A}{0.5V} = 0.4mA/V = 0.4\mu A/mV$$

$$\sigma_{I_D} = g_m \sigma_{Vt} = 2.5mV \cdot 0.4\mu A/mV = 1\mu A$$

i.e. 1σ sigma mismatch in drain currents of 1%

3σ percentage mismatch is +/-3%

Question 3

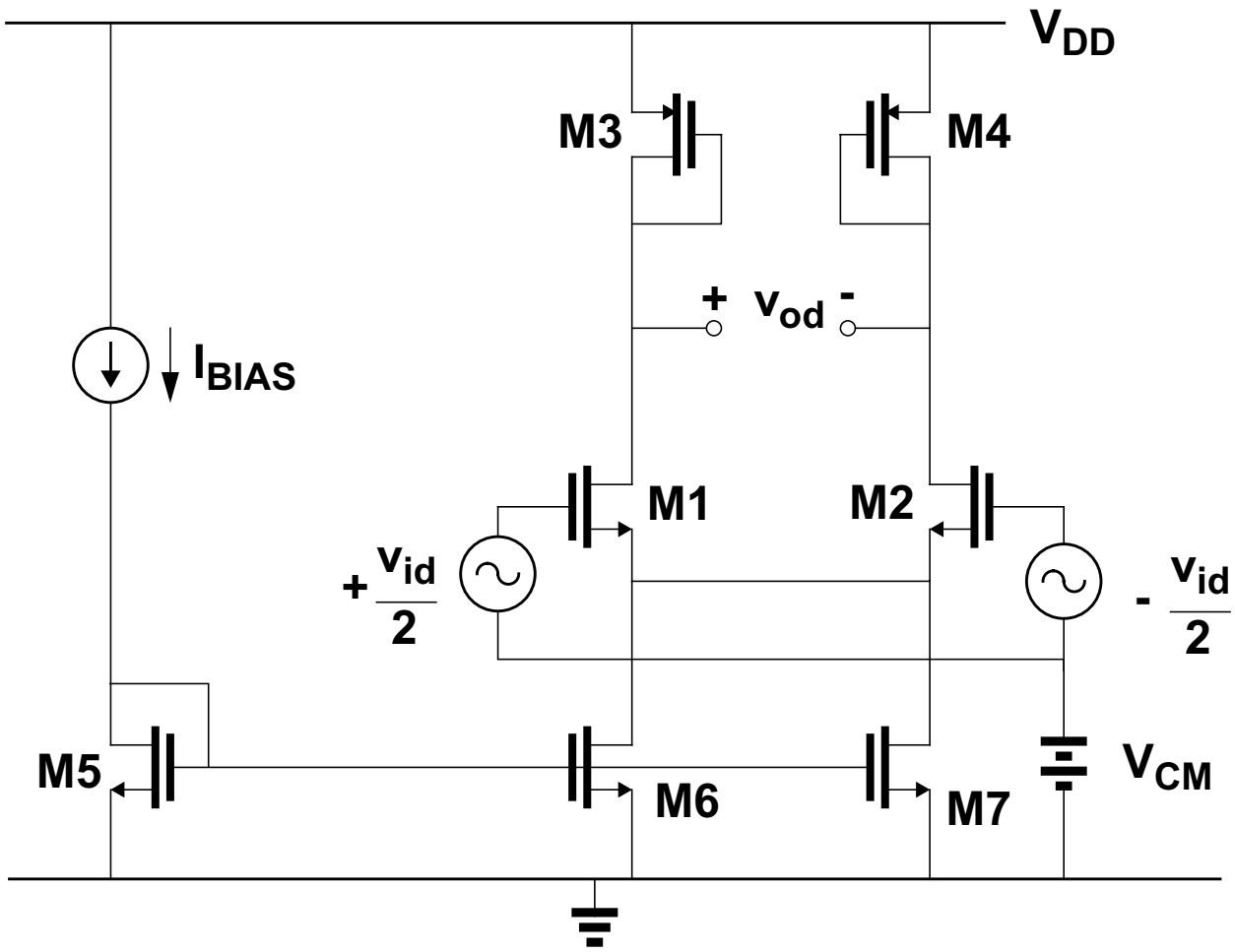


Figure 3

Figure 3 shows a differential amplifier with pmos diode loads.

V_{DD}=5V, I_{BIAS} = 100µA,K_n'=200µA/V^2, K_p'=50µA/V^2,V_{tn}=0.7V, V_{tp}=-0.7V

All transistors have W/L = 12.5µm/2µm.

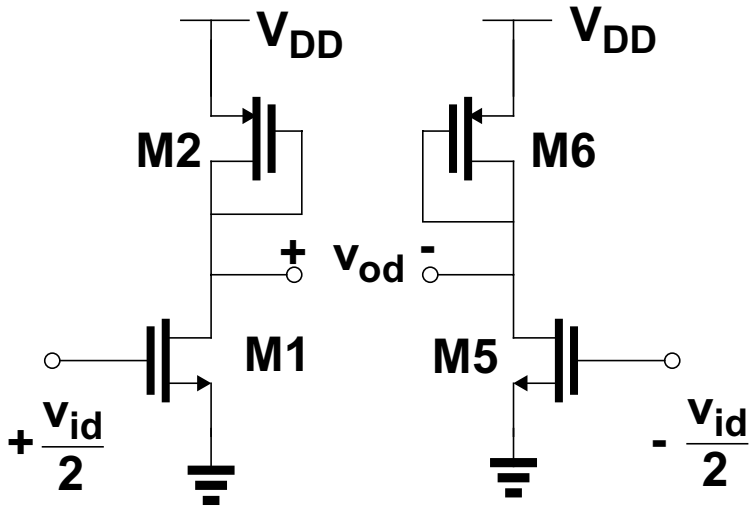
Assume g_{mn} >> g_{dsn}, g_{mp} >> g_{dsp}.

You may assume the common source of M1,M2 is at ac ground.

(i) What is the small-signal low-frequency differential gain (v_{od}/v_{id}) of this amplifier in terms of the small-signal parameters?
(ii) What is the common-mode input range of this amplifier?
(iii) Calculate the value of low-frequency small-signal gain. Assume all transistors are in saturation.
(iv) What is value of the low-frequency small-signal gain if the current I_{BIAS} is doubled, assuming all transistors stay in saturation?

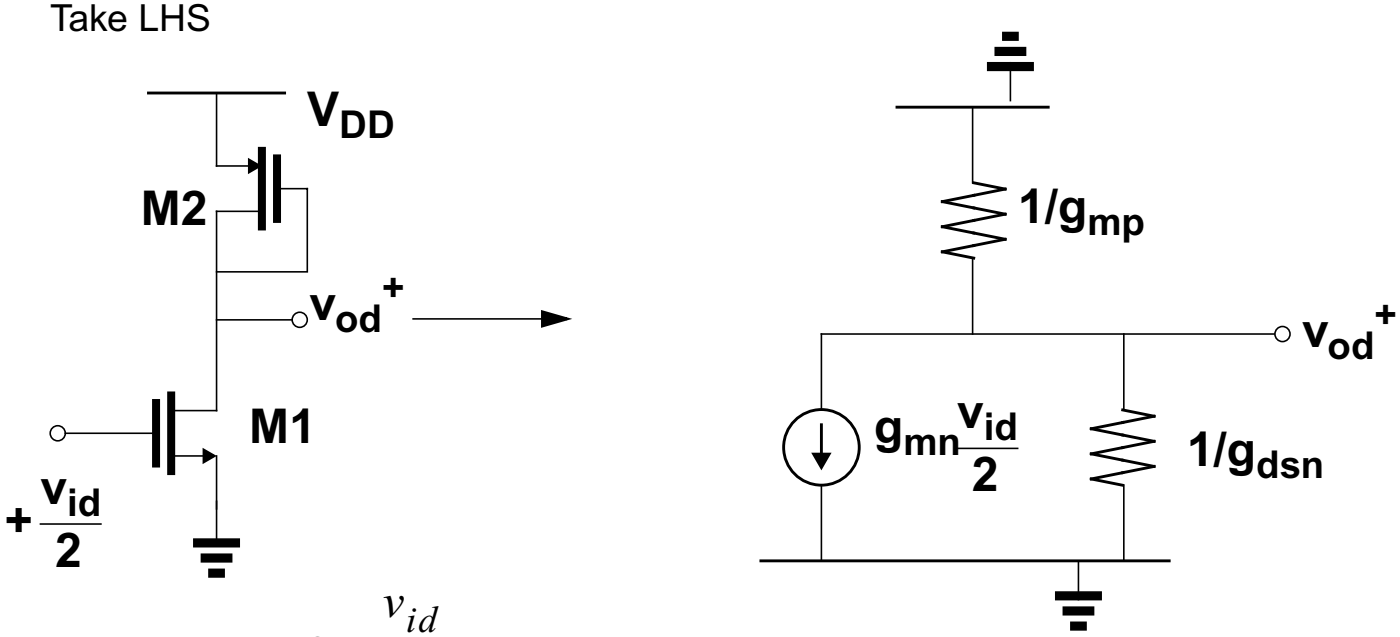
(i) Figure 3 shows a differential amplifier with pmos diode loads. What is the small-signal differential gain (v_{od}/v_{id}) of this amplifier ?.

Note that the question does not ask for a derivation. It has been shown in the course that the gain of such circuits can be given by inspection. Deriving the gain by the analyses given in the notes as shown below, is of course also good



circuit is symmetrical
=> We can split it into two identical halves

Take LHS



$$v_{od}^{+} = -\frac{g_{mn}\frac{v_{id}}{2}}{g_{dsn}+g_{mp}}$$

Alternatively give this answer directly by observation

$$v_{od} = v_{od}^{+} - v_{od}^{-} = -\frac{g_{mn}\frac{v_{id}}{2}}{g_{dsn}+g_{mp}} - \left(-\frac{g_{mn}-\frac{v_{id}}{2}}{g_{dsn}+g_{mp}}\right)$$

$$v_{od} = -\frac{g_{mn}}{g_{dsn}+g_{mp}}v_{id} \qquad A_{dm} = \frac{v_{od}}{v_{id}} = -\frac{g_{mn}}{g_{dsn}+g_{mp}} \approx -\frac{g_{mn}}{g_{mp}}$$

(ii) What is the common-mode input range of this amplifier?

1. Lower limit on V_{CM}: is given by the requirement that M6 stay in saturation

In quiescent state, amplifier is symmetrical. Look at biasing of left-hand side.

$$V_{CM} \geq V_{GS1} + (V_{GS6} - V_t)$$

$$V_{GS} - V_t = \sqrt{\frac{2I_D}{K_n' \frac{W}{L}}}$$

M1: $$V_{GS1} - V_t = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V \cdot \frac{12.5}{2}}} = 400mV$$

$$V_{GS1} = 400mV + V_t = 1.1V$$

M6: $$V_{GS6} - V_t = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V \cdot \frac{12.5}{2}}} = 400mV$$

$$V_{CM} \geq 1.1V + 0.4V$$

$$V_{CM} \geq 1.5V$$

2. Upper limit on V_{CM}: is given by the requirement that M1 be in saturation

$$V_{DS1} \geq V_{GS1} - V_{tn}$$

$$V_{DD} - |V_{GS3}| - V_{S1} \geq V_{CM} - V_{S1} - V_{tn}$$

$$V_{CM} \leq V_{DD} - |V_{GS3}| + V_{tn}$$

M3

$$|V_{GS3} - V_{tp}| = \sqrt{\frac{2 \cdot 100\mu A}{50\mu A/V \cdot \frac{12.5}{2}}} = 800mV$$

$$|V_{GS3}| = 800mV + |V_{tp}| = 1.5V$$

$$V_{CM} \leq V_{DD} - |V_{GS3}| + V_{tn}$$

$$V_{CM} \leq 5 - 1.5V + 0.7V$$

$$V_{CM} \leq 4.2V$$

Common-mode input range given by

$$1.5V \leq V_{CM} \leq 4.2V$$

(iii) Calculate the low-frequency small-signal gain.

$$Gain = \frac{v_{out}}{v_{id}} = -\frac{g_{mn}}{g_{mp}}$$

$$g_{mn} = \frac{2I_D}{(V_{GS1} - V_{tn})}$$

$$g_{mp} = \frac{2I_D}{(|V_{GS3}| - |V_{tp}|)}$$

$$Gain = \frac{v_{out}}{v_{id}} = -\frac{g_{mn}}{g_{mp}} = -\frac{|V_{GS3}| - |V_{tp}|}{V_{GS1} - V_{tn}} = -\frac{0.8}{0.4} = -2$$

(iv) What is value of the low-frequency small-signal gain if the current I_{BIAS} is doubled, assuming all transistors stay in saturation?

If I_{BIAS} is doubled, $|V_{GS}|-|V_t|$ will increase by sqrt 2 for both M1 and M3, so the overall gain will remain unchanged.

Question 4

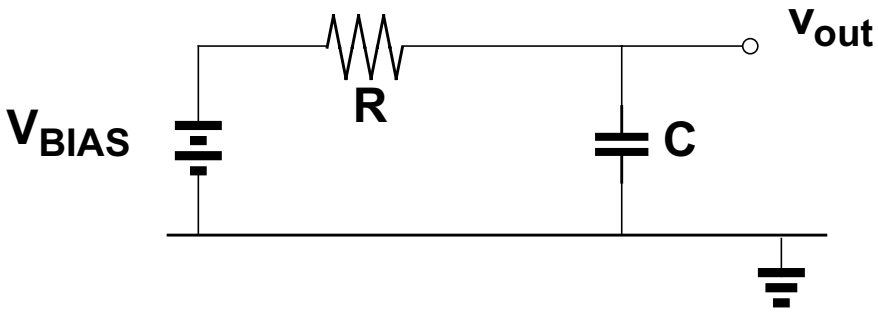


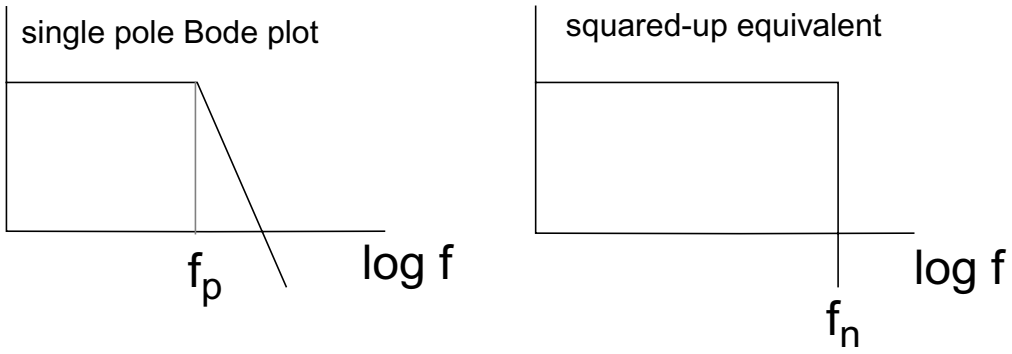
Figure 4

For numerical calculations take Boltzmann's constant k=1.38X10^{-23}J/^{o}K, temperature T=300^{o}K.

(i) Show that the total integrated thermal noise voltage at node v_{out} in Figure 4 is

$$v_{nout}^2 = \frac{kT}{C}$$

where k is Boltzmann's constant, and T is the temperature.
You may assume the following:



For the area underneath the curves to be the same then $f_n=(\pi/2)*f_p$

(ii) If R= 1kΩ and C=1pF calculate the total thermal noise in V_{rms} at node v_{out} in Figure 4?

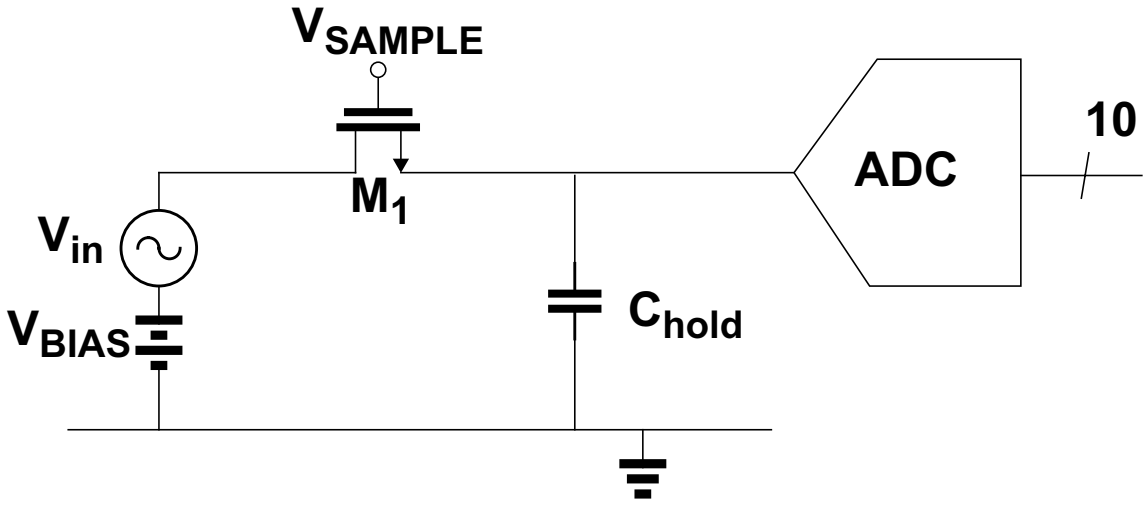


Figure 5

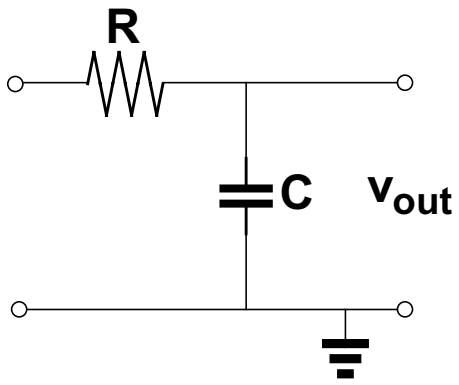
(iii) Figure 5 shows a sampling circuit preceding a 10-bit A/D converter. The sampling switch M1 is turned on.If the A/D converter has an input range of 1Vrms, and the noise budget for the sampling circuit is 0.1 LSB, what is the minimum value required for C_{hold}?

(iv) If a 12-bit A/D converter is used with the same input range, and the noise budget for the sampling circuit is kept at 0.1LSB, what is the new minimum value required for C_{hold}?

(i) Show that the total integrated thermal noise voltage at node v_{out} in Figure 4 is

$$v_{nout}^2 = \frac{kT}{C}$$

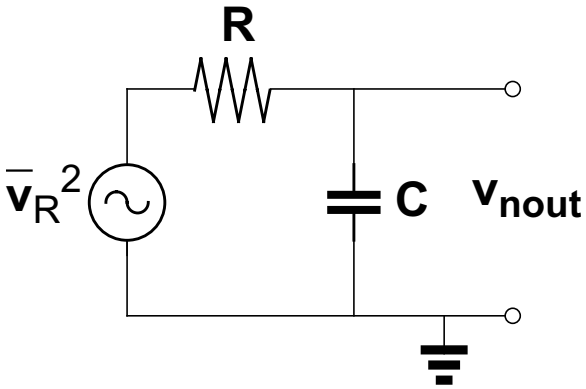
where k is Boltzmann's constant, and T is the temperature.



The resistor R generates a noise voltage $v_r^2 = 4kTR$

The noise from the resistor is filtered by the pole formed by R,C

Pole frequency: $f_o = \frac{1}{2\pi RC}$



Total output noise noise power:

$$v_{nout}^2 = v_r^2 \cdot \frac{\pi}{2} \cdot f_o = 4kTR \cdot \frac{\pi}{2} \cdot \frac{1}{2\pi RC} = \frac{kT}{C}$$

(ii) If R= 1kΩ and C=1pF what is the total thermal noise in Vrms at node v_{out} in Figure 4?

$$v_{nout} = \sqrt{\frac{kT}{C}} = \sqrt{\frac{1.38\times10^{-23}\,300}{1\,pF}} = 64\mu V_{rms}$$

(iii) Figure 5 shows a sampling circuit preceding a 10-bit ADC. The sampling switch M1 is turned on. If the A/D converter has an input range of 1Vrms, and the noise budget for the sampling circuit is 0.1 LSB, what is the minimum value required for C_{hold}?

10-bit ADC full-scale input range = 1Vrms

ADC LSB = $1V/2^{10}$ =1mVrms

The sample-and-hold circuit is a first-order circuit => noise is

$$\overline{v_n^2} = \frac{kT}{C}$$

For error budget want $\overline{v}_n$ < LSB/10 = 0.1mV

$$\sqrt{\frac{kT}{C}} < 0.1mV \Rightarrow C > \frac{kT}{(0.1mV)^2} \Rightarrow C > \frac{1.38\times10^{-23}\times 300}{(0.1mV)^2} = 0.41\,pF$$

(iv) If a 12-bit ADC is used, and the noise budget for the sampling circuit is kept at 0.1LSB, what is the new minimum value required for C_{hold}?

12-bit ADC full-scale input range = 1Vrms

ADC LSB = $1V/2^{10}$ =0.25mV

The sample-and-hold circuit is a first-order circuit => noise is

$$\overline{v_n^2} = \frac{kT}{C}$$

For error budget want $\overline{v}_n$ < LSB/10 = 0.025mV

$$\sqrt{\frac{kT}{C}} < 0.1mV \Rightarrow C > \frac{kT}{(0.025mV)^2} \Rightarrow C > \frac{1.38\times10^{-23}\times 300}{(0.025mV)^2} = 6.6\,pF$$