Part A

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an nmos in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda V_{DS})$$

Question 1

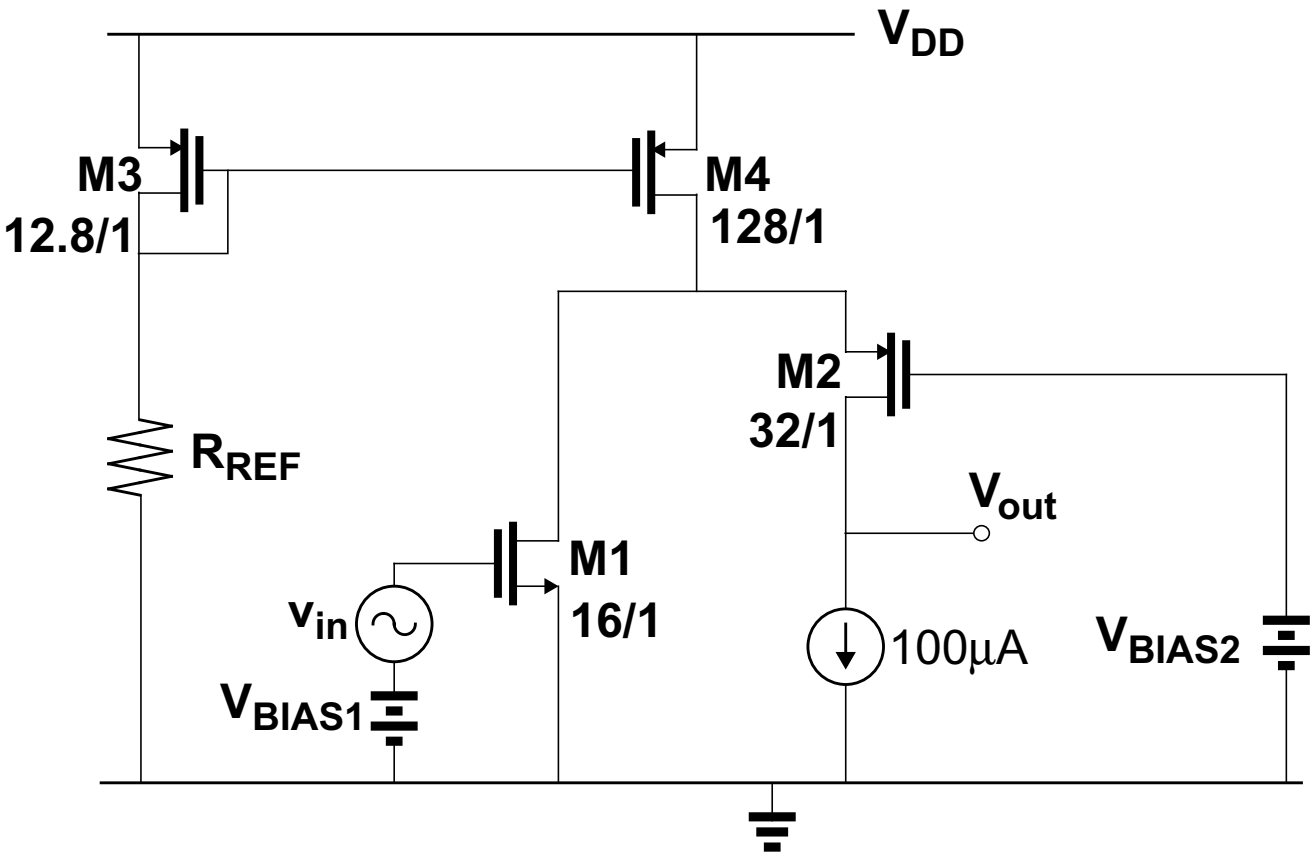


Figure 1

Figure 1 shows a folded-cascode gain stage with an ideal current source load. The bias current for the stage is provided by the current mirror and resistor R_{REF}.

$K_n'=200\mu A/V^2$, $K_p'=50\mu A/V^2$, $V_{tn}=|V_{tp}|=750mV$. $V_{DD}=3V$.
The device sizes in microns are as indicated in Figure 1.
Assume all devices are biased in saturation. For dc biasing calculations take $\lambda=0$.

(i) M1 has the same quiescent bias current as M2. What is the value of V_{BIAS1}? What are the drain currents of M3 and M4?
(ii) What value of R_{REF} is required to generate the total bias current for the folded cascode stage?
(iii) What is the maximum value of V_{BIAS2} such that M4 is in saturation?
(iv) Draw the small-signal model of the folded-cascode gain stage shown in Figure 1.
(v) Derive an expression for the output resistance i.e. the resistance looking into the output node.

(i) M1 has the same quiescent bias current as M2. What is the value of V_{BIAS1}? What are the drain currents of M3 and M4?

Bias current of M2 is 100μA

$$I_{D1} = \frac{K_n'}{2}\frac{W}{L}(V_{GS1} - V_t)^2 \Rightarrow V_{GS1} - V_t = \sqrt{\frac{2I_{D1}}{K_n'\frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V^2 \frac{16}{1}}}$$

$$V_{GS1} - V_t = 250mV$$

$$V_{BIAS1} = V_{GS1} - V_t + V_t = 250mV + 750mV = \underline{\underline{1V}}$$

I_{D4} = Total bias current is 200μA.

Current mirror is 1:10 so 20μA through I_{D3}.

(ii) What value of R_{REF} is required to generate the total bias current for the folded cascode stage?

Total bias current is 200μA. Current mirror is 1:10 so 20μA through R_{REF}.

$$|V_{GS3} - V_t| = \sqrt{\frac{2I_{D3}}{K_p'\frac{W}{L}}} = \sqrt{\frac{2 \cdot 20\mu A}{50\mu A/V^2 \frac{12.8}{1}}} = 250mV$$

$$|V_{GS3}| = 250mV + |V_t| = 1V$$

$$I_{D3} = \frac{V_{DD} - |V_{GS3}|}{R_{REF}} \Rightarrow R_{REF} = \frac{V_{DD} - |V_{GS3}|}{I_{D3}} = \frac{3V - 1V}{20\mu A} = \underline{\underline{100k\Omega}}$$

(iii) What is the maximum value of V_{BIAS2} such that M4 is in saturation?

First calculate $|V_{GS2}|$

$$|V_{GS2}| - |V_t| = \sqrt{\frac{2I_{D2}}{K_p' \frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{50\mu A/V^2 \frac{32}{1}}} = 354mV$$

$$|V_{GS2}| = 354mV + |V_t| = 1.104V$$

Maximum value of VBIAS2 is value such that M4 is just in saturation

$$V_{DD} - (V_{BIAS2} + |V_{GS2}|) > |V_{GS4} - V_t|$$

$$|V_{GS4} - V_t| = |V_{GS3} - V_t| = 250mV$$

$$V_{BIAS2} < V_{DD} - |V_{GS2}| - |V_{GS4} - V_t|$$

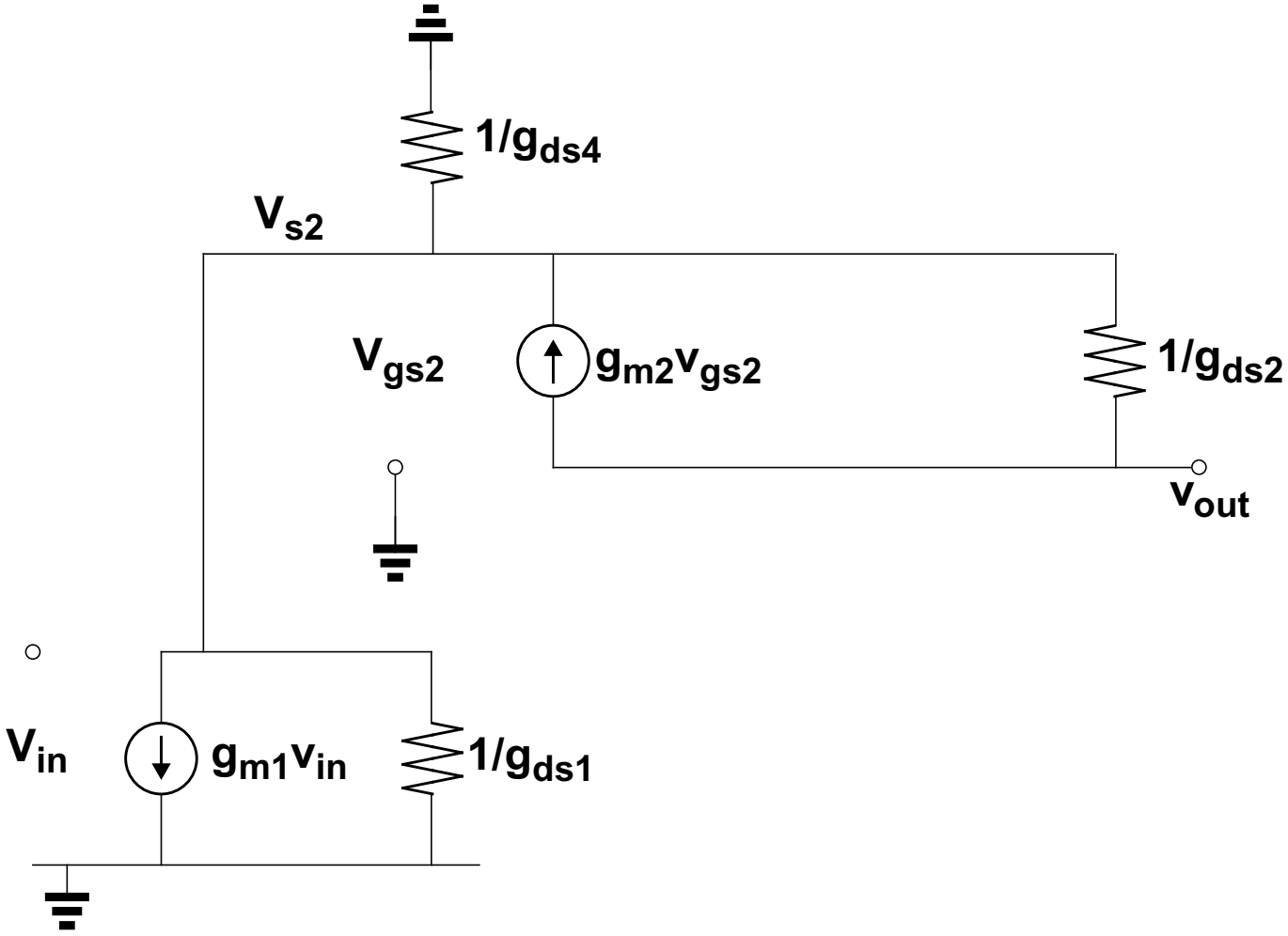
$$V_{BIAS2} < 3V - 1.104V - 250mV$$

$$V_{BIAS2} < 3V - 1.104V - 250mV$$

$$V_{BIAS2} < \underline{\underline{1.646}}$$

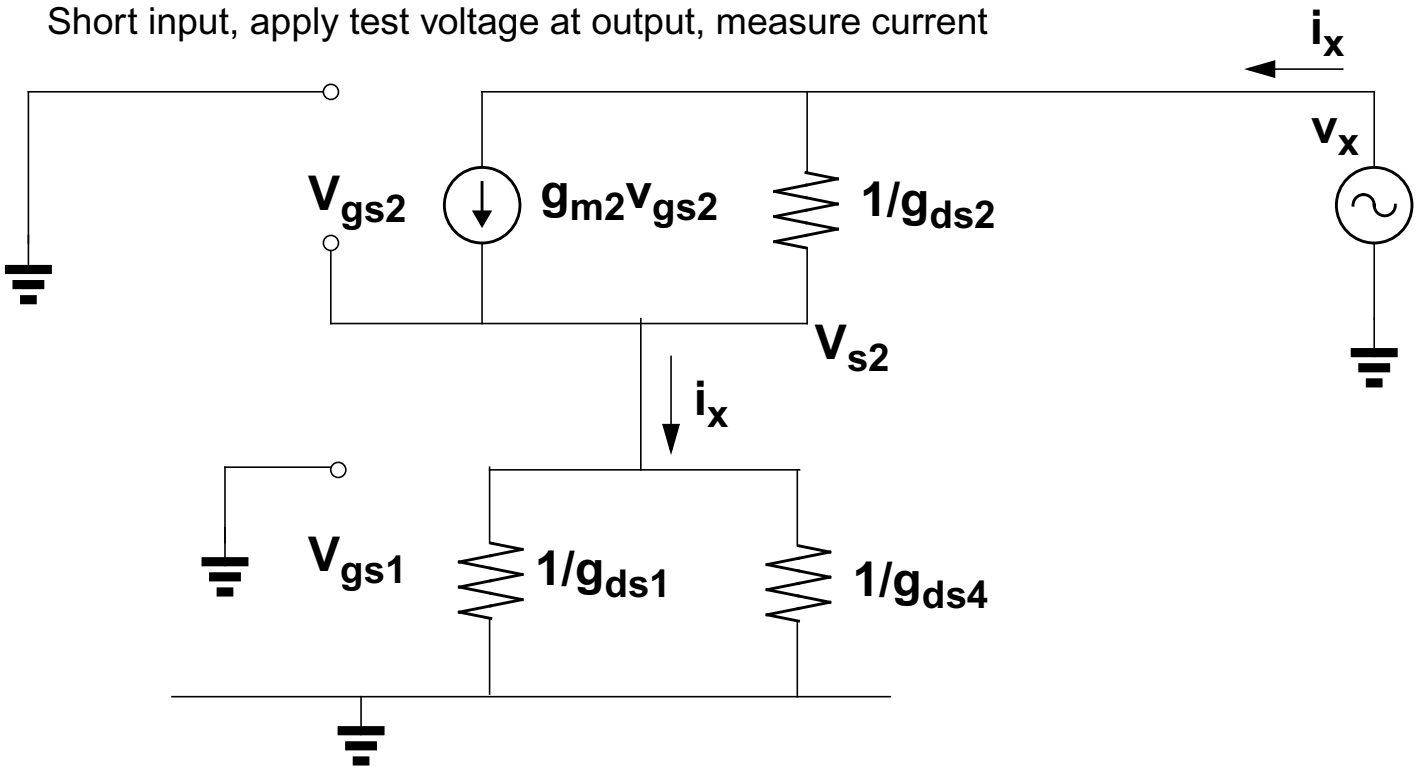
(iv) Draw the small-signal model of the folded-cascode gain stage.

Small-signal equivalent circuit:



(v) Derive an expression for the output resistance

Short input, apply test voltage at output, measure current



$$v_{gs1} = 0 \Rightarrow g_{m1}v_{gs1} = 0$$

$$v_{gs2} = -v_{s2}$$

$$i_x = g_{m2}v_{gs2} + (v_x - v_{s2})g_{ds2}$$

$$i_x = -g_{m2}v_{s2} + v_x g_{ds2} - v_{s2}g_{ds2}$$

Since $v_{s2} = \dfrac{i_x}{g_{ds1} + g_{ds4}}$

$$i_x = -g_{m2}\left(\frac{i_x}{g_{ds1} + g_{ds4}}\right) + v_x g_{ds2} - \left(\frac{i_x}{g_{ds1} + g_{ds4}}\right)g_{ds2}$$

$$r_{out} = \frac{v_x}{i_x} = \frac{1}{g_{ds2}}\left(1 + \frac{g_{m2}}{g_{ds1} + g_{ds4}} + \frac{g_{ds2}}{g_{ds1} + g_{ds4}}\right)$$

May simplify if wish to: $g_{m2} >> g_{ds1}, g_{ds4}$

$$r_{out} = \frac{v_x}{i_x} \approx \frac{g_{m2}}{g_{ds2}}\left(\frac{1}{g_{ds1} + g_{ds4}}\right)$$

Question 2

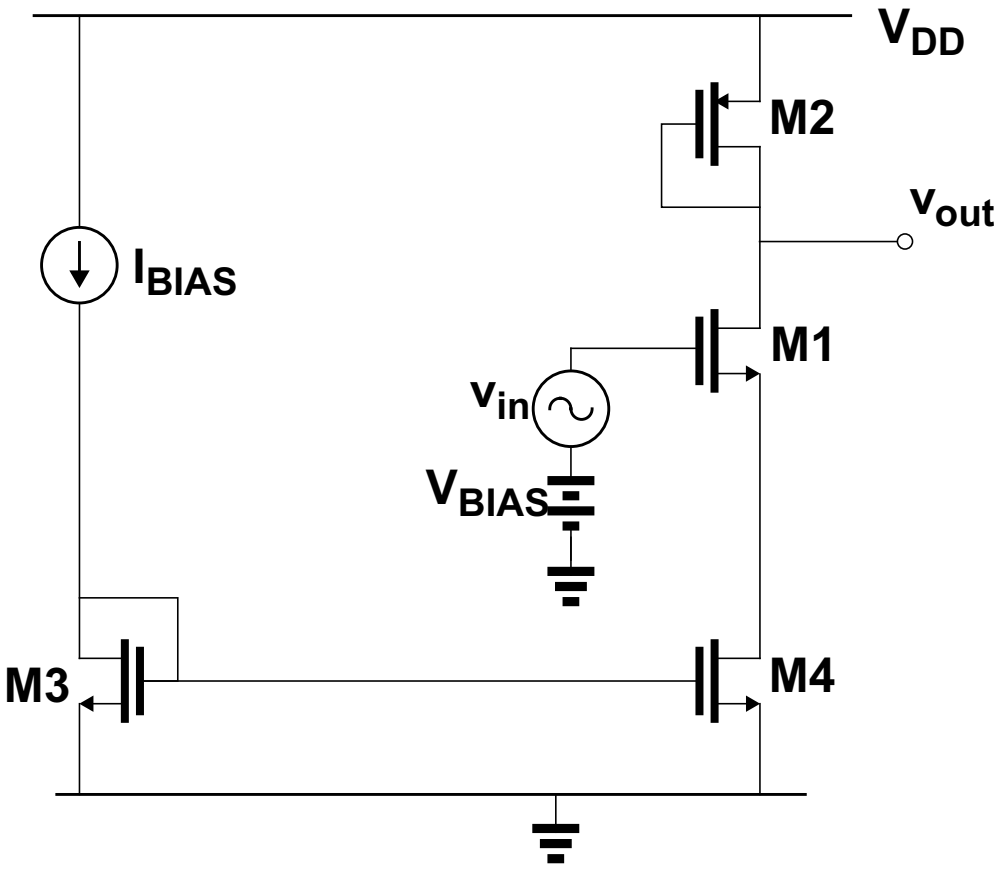


Figure 2

For each part of this question assume all nmos transistors have equal transconductances g_{mn} and output conductances g_{dsn}, and similarily that all pmos transistors have equal transconductances g_{mp} and output conductances g_{dsp}.
Assume g_{mn},g_{mp}>>g_{dsn},g_{dsp}. Ignore all capacitances.

(i) Figure 2 shows a gain stage with a diode load biased by a current mirror. Draw the small signal model for this circuit.
(ii) Show that the small signal voltage gain (v_{out}/v_{in}) is approximately given by

$$\frac{v_{out}}{v_{in}} = -\frac{g_{dsn}}{g_{mp}}$$

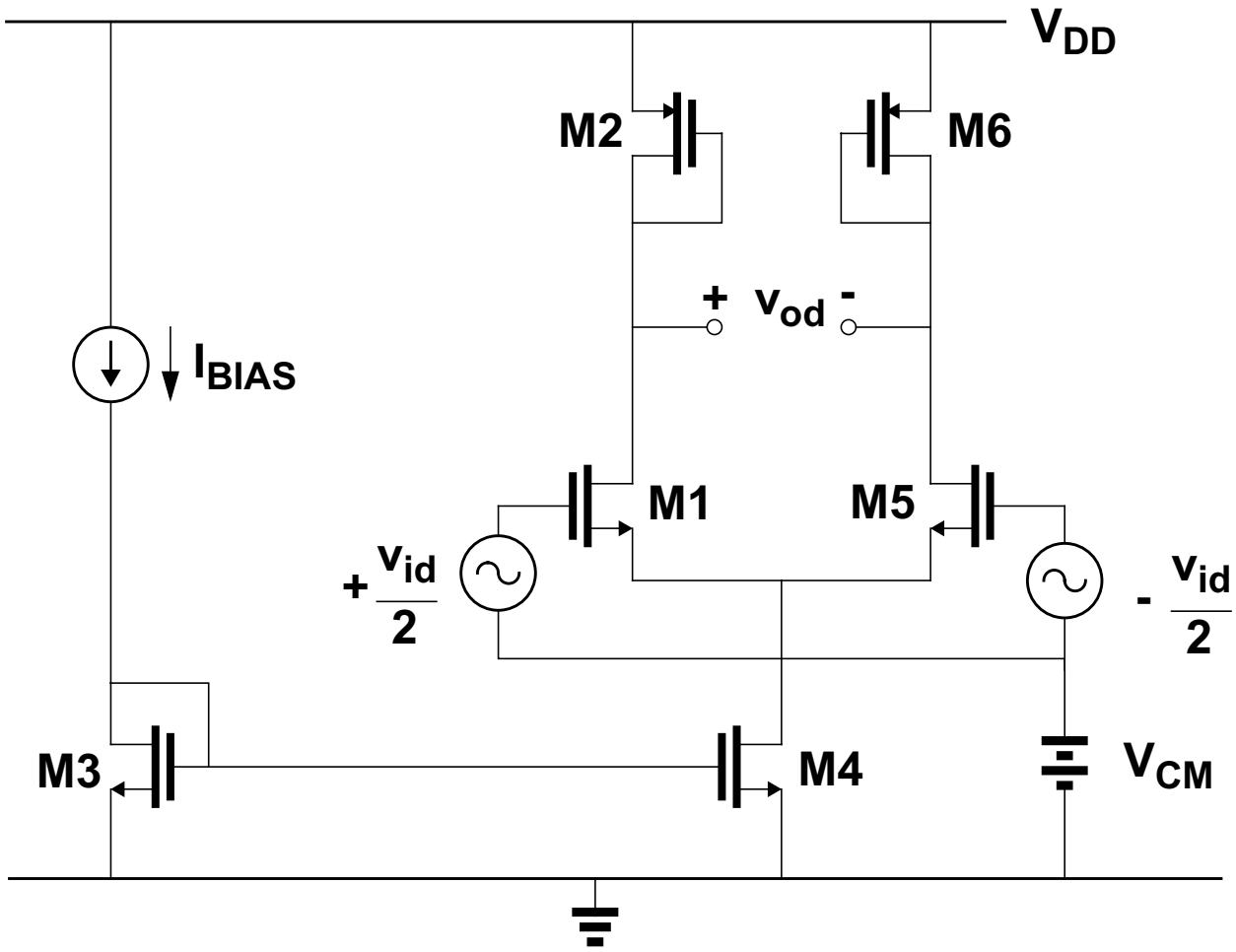


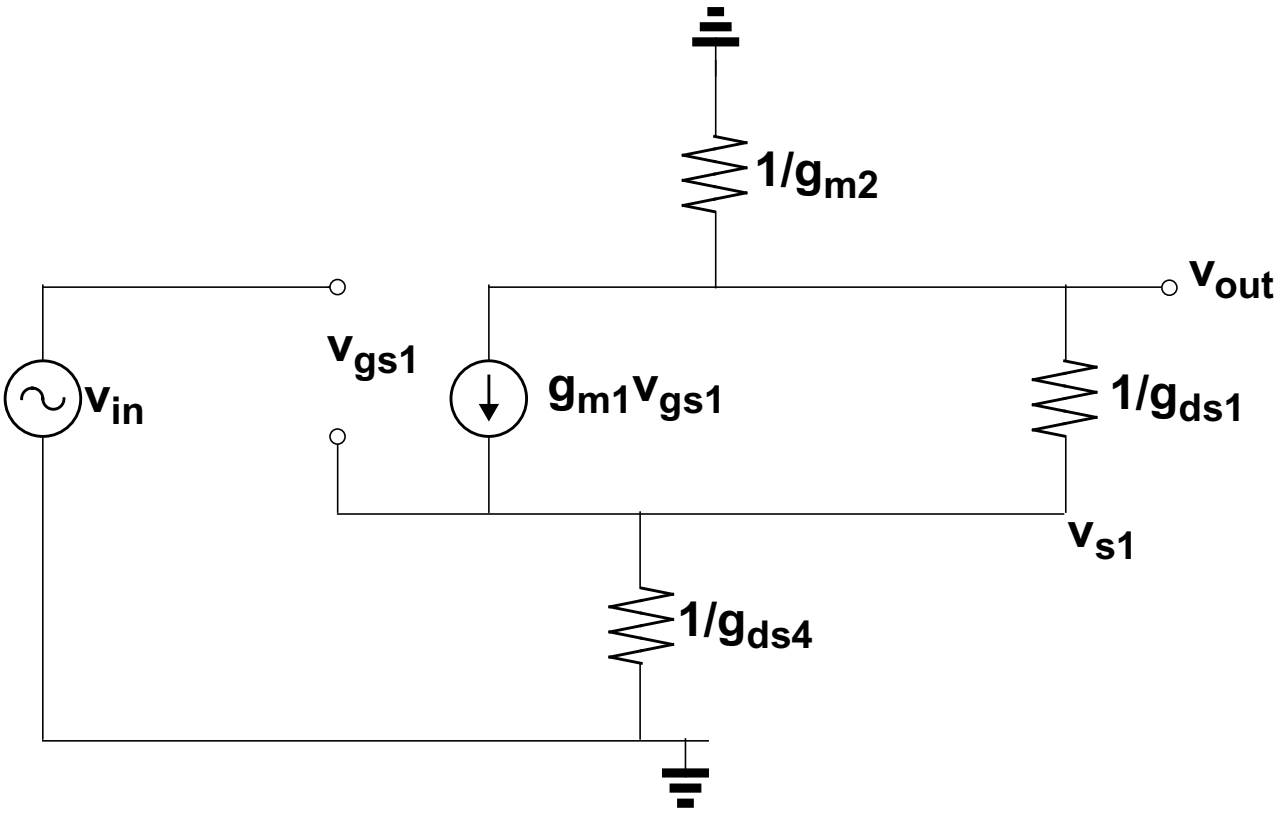
Figure 3

(iii) Figure 3 shows a differential amplifier with pmos diode loads. What is the small-signal differential gain (v_{od}/v_{id}) of this amplifier ?
You may assume the common source of M1,M5 is at ac ground.

(iv) What is the common-mode gain of the differential amplifier shown in Figure 3?

(v) What is the common-mode rejection ratio (i.e. the ratio of the differential gain to the common-mode gain) of the differential amplifier shown in Figure 3?
Calculate the common-mode rejection ratio in dB if
I_{BIAS} = 100μA,K_n'=200μA/V^2, K_p'=50μA/V^2, $\lambda_n=\lambda_p$=0.04/L V^{-1} (L in μm)
All nmos transistors have W/L = 10μm/2μm. All pmos transistors have W/L = 40μm/2μm.

(i) Figure 2 shows a gain stage with a diode load biased by a current mirror. Draw the small signal model for this circuit.



(ii) Show that the small signal voltage gain (v_{out}/v_{in}) is approximately given by

$$\frac{v_{out}}{v_{in}} = \frac{-g_{dsn}}{g_{mp}}$$

KCL at output node

$$v_{out}g_{m2} + g_{m1}v_{gs1} + (v_{out} - v_{s1})g_{ds1} = 0$$
$$v_{out}g_{m2} + g_{m1}(v_{in} - v_{s1}) + (v_{out} - v_{s1})g_{ds1} = 0$$

Current through $1/g_{m2}$ = current through $1/g_{ds4}$

$$-v_{out}g_{m2} = v_{s1}g_{ds4}$$

$$v_{s1} = -\frac{g_{m2}}{g_{ds4}}v_{out}$$

Substitute for v_{s1}

$$v_{out}g_{m2} + g_{m1}\left(v_{in} + \frac{g_{m2}}{g_{ds4}}v_{out}\right) + \left(v_{out} + \frac{g_{m2}}{g_{ds4}}v_{out}\right)g_{ds1} = 0$$

$$g_{m1}v_{in} = -\left(g_{m2} + g_{m1}\frac{g_{m2}}{g_{ds4}} + g_{ds1} + g_{ds1}\frac{g_{m2}}{g_{ds4}}\right)v_{out}$$

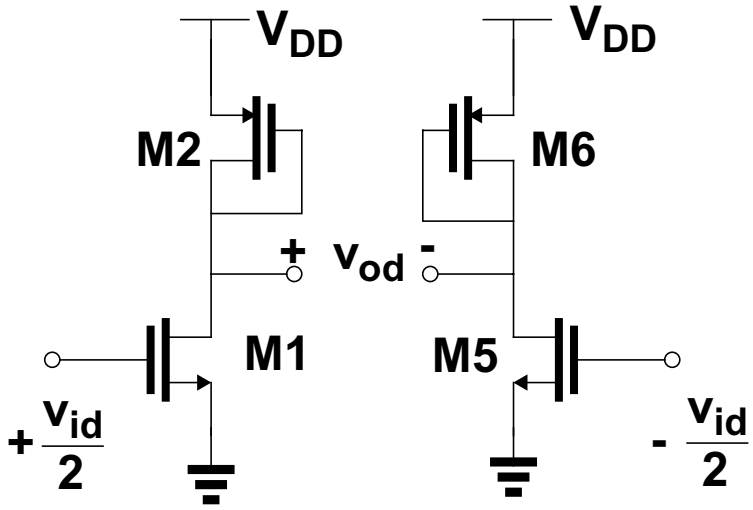
$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{m1}\frac{g_{m2}}{g_{ds4}} + g_{ds1} + \frac{g_{m2}}{g_{ds4}}g_{ds1}}$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{mn}}{g_{mp} + g_{mn}\frac{g_{mp}}{g_{dsn}} + g_{dsn} + \frac{g_{mp}}{g_{dsn}}g_{dsn}}$$

Using $g_m >> g_{ds}$ this simplifies to

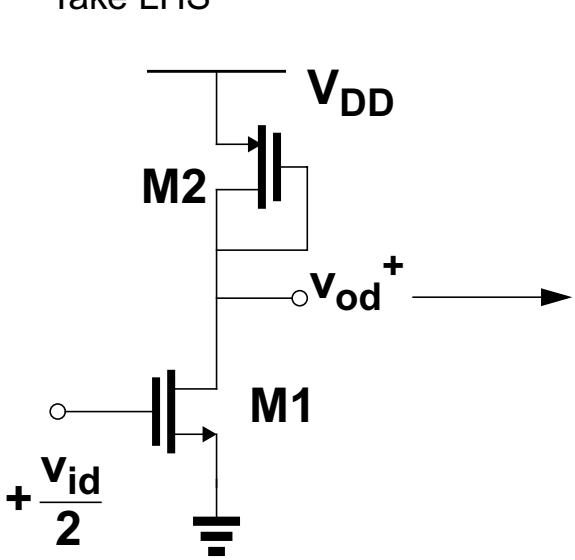
$$\frac{v_{out}}{v_{in}} = -\frac{g_{mn}}{g_{mn}\frac{g_{mp}}{g_{dsn}}} = -\frac{g_{dsn}}{g_{mp}}$$

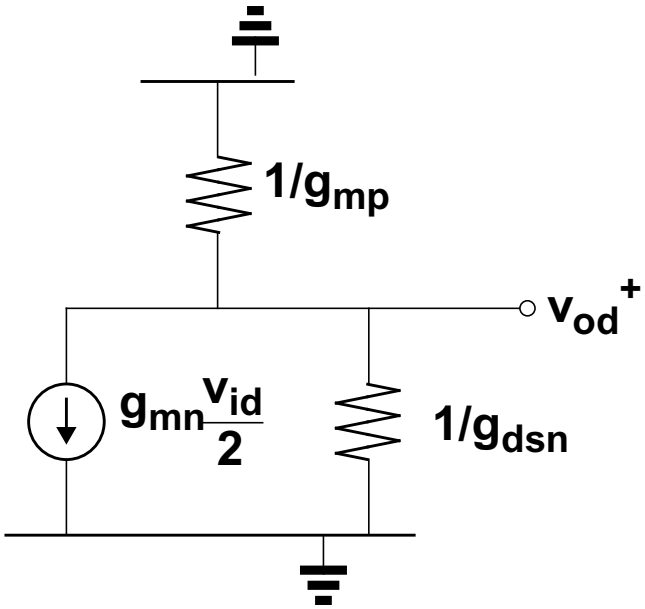
(iii) Figure 3 shows a differential amplifier with pmos diode loads. What is the small-signal differential gain (v_{od}/v_{id}) of this amplifier ?
You may assume the common source of M1,M5 is at ac ground.



circuit is symmetrical
=> We can split it into two identical halves

Take LHS





$$v_{od}^{+} = -\frac{g_{mn}\frac{v_{id}}{2}}{g_{dsn}+g_{mp}}$$

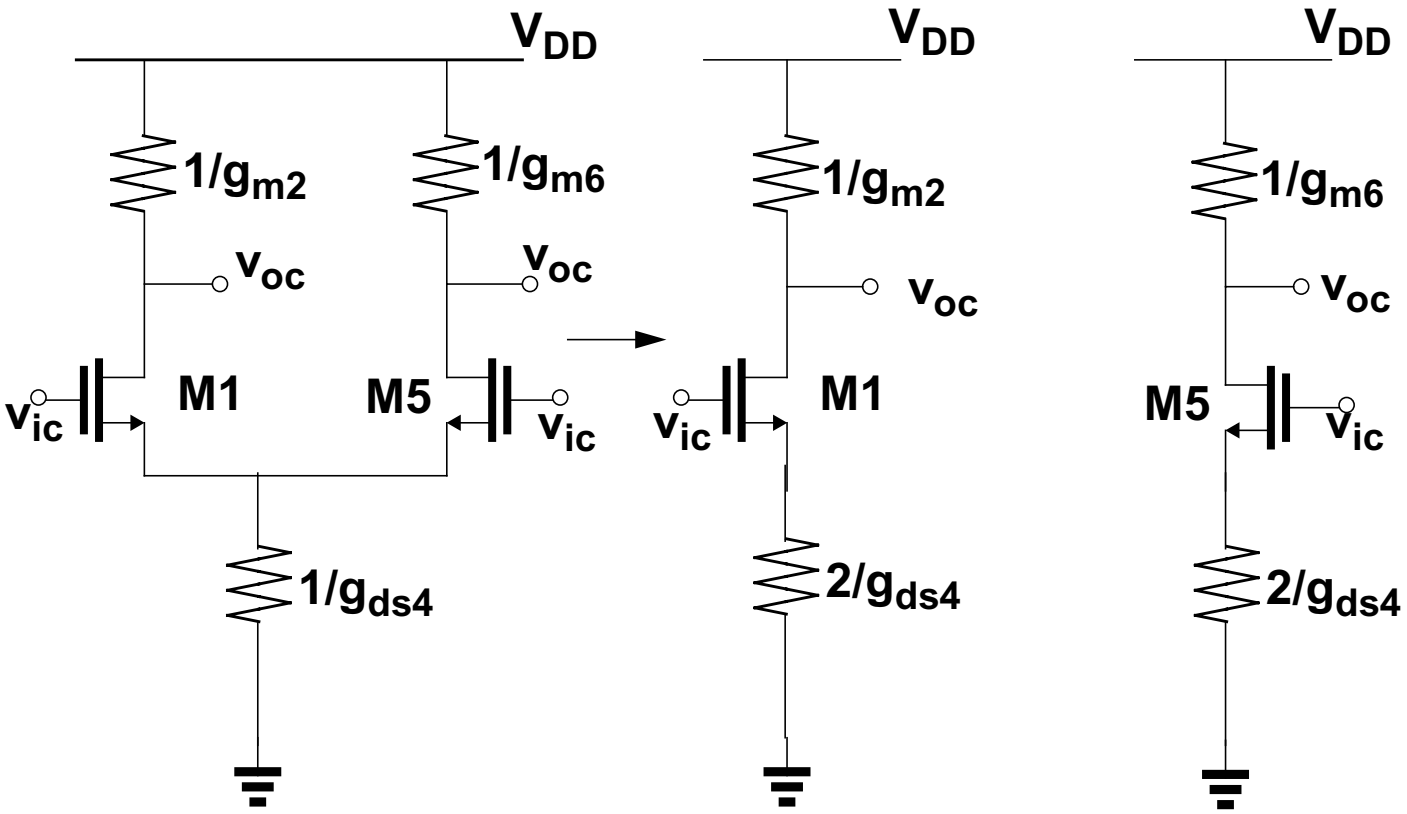
Alternatively give this answer directly by observation

$$v_{od} = v_{od}^{+} - v_{od}^{-} = -\frac{g_{mn}\frac{v_{id}}{2}}{g_{dsn}+g_{mp}} - \left(-\frac{g_{mn}-\frac{v_{id}}{2}}{g_{dsn}+g_{mp}}\right)$$

$$v_{od} = -\frac{g_{mn}}{g_{dsn}+g_{mp}} v_{id} \qquad A_{dm} = \frac{v_{od}}{v_{id}} = -\frac{g_{mn}}{g_{dsn}+g_{mp}} \approx -\frac{g_{mn}}{g_{mp}}$$

(iv) What is the common-mode gain of the differential amplifier shown in Figure 3?

Apply a small common mode voltage signal to both inputs and calculate output voltage change.



Equivalent circuit for tail current source

Split into identical half circuits
Current halved => conductance halved.

Use result from (ii) directly

$$A_{cm} = \frac{v_{oc}}{v_{ic}} = -\frac{\frac{g_{ds4}}{2}}{g_{m2}} = -\frac{\frac{g_{dsn}}{2}}{g_{mp}}$$

(v) What is the common-mode rejection ratio (i.e. the ratio of the differential gain to the common-mode gain) of the differential amplifier shown in Figure 3?
Calculate the common-mode rejection ratio in dB if
I_{BIAS} = 100μA,K_n'=200μA/V^2, K_p'=50μA/V^2, $\lambda_n=\lambda_p$=0.04/L V^{-1} (L in μm).
All nmos transistors have W/L = 10μm/2μm. All pmos transistors have W/L = 40μm/2μm.

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\frac{-\frac{g_{mn}}{g_{mp}}}{-\frac{g_{dsn}}{2g_{mp}}}\right| = \frac{2g_{mn}}{g_{dsn}}$$

$I_{D1} = I_{BIAS}/2 = 50\mu A$.

$$g_{mn} = \sqrt{2K_n'\frac{W}{L}I_{D1}} = \sqrt{2\cdot 200\mu A/V^2\frac{10}{2}50\mu A} = 316\mu A/V$$

$$g_{dsn} = \lambda I_{D1} = \frac{0.04}{L}I_{D1} = \frac{0.04}{2}50\mu A = 1\mu A/V$$

$$CMRR_{dB} = 20\log\left|\frac{A_{dm}}{A_{cm}}\right| = 20\log\frac{2g_{mn}}{g_{dsn}} = 20\log\frac{2(316\mu A/V)}{1\mu A/V} = \underline{\underline{56dB}}$$

Question 3

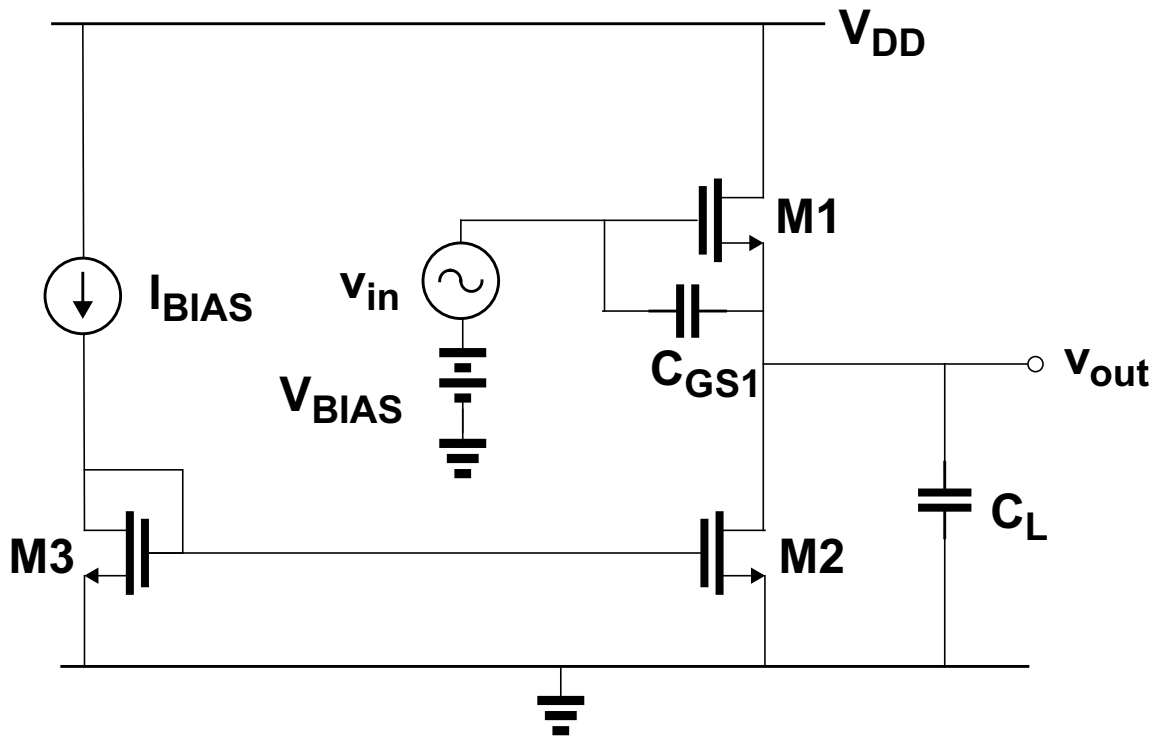
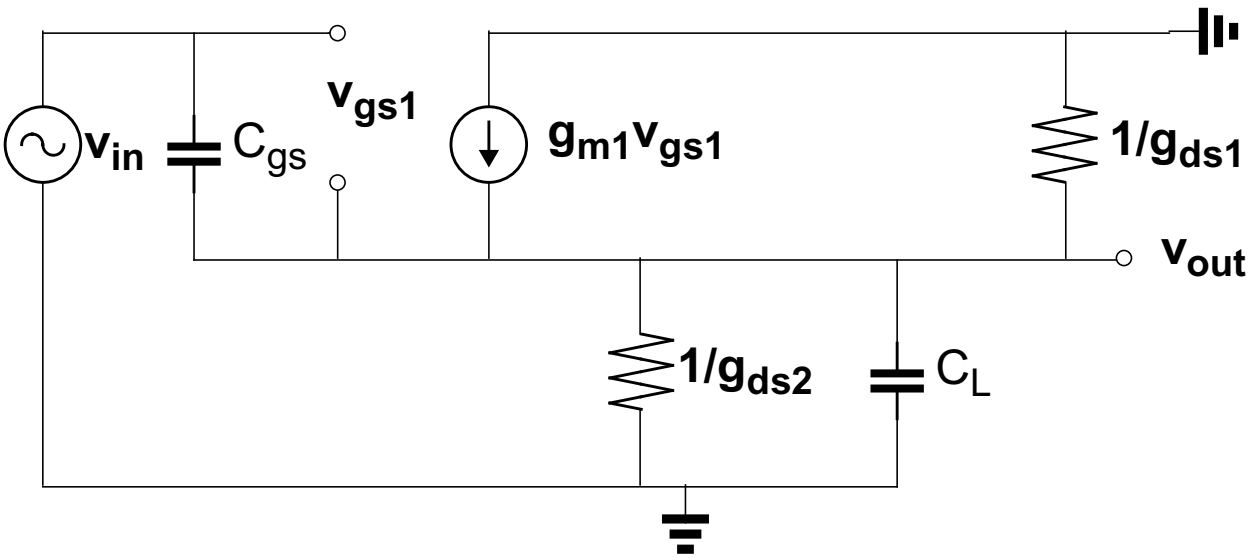


Figure 4

Figure 4 shows a source follower stage biased by a current mirror.
All transistors have equal dimensions, transconductances g_{mn} and output conductances g_{dsn}.
Assume $g_{mn} >> g_{dsn}$.

(i) Draw the small signal equivalent circuit for the source follower stage shown in Figure 4.
(ii) Derive an expression for the low-frequency small signal voltage gain (v_{out}/v_{in}).
(iii) Ignoring all capacitances except C_{GS1} and C_L derive an expression for the high frequency transfer function.
(iv) Calculate the pole and zero frequencies if V_{GS1}=1V, V_{tn}=0.75V, I_{BIAS}=100μA, C_{GS1}=1pF, C_L=9pF.
(v) Draw a Bode diagram of the gain. Indicate the dc gain and the gain at frequencies well above the pole and zero frequencies.

(i) Draw the small signal equivalent circuit



(ii) Derive an expression for the low-frequency small signal voltage gain (v_{out}/v_{in})

KCL at output node

$$g_{m1}v_{gs1} - v_{out}g_{ds1} - v_{out}g_{ds2} = 0$$

$$g_{m1}(v_{in} - v_{out}) - v_{out}g_{ds1} - v_{out}g_{ds2} = 0$$

$$g_{m1}v_{in} = (g_{m1} + g_{ds1} + g_{ds2})v_{out}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1} + g_{ds2}}$$

Using $g_{ds1}=g_{ds2}=g_{dsn}$, $g_{m1}=g_{m2}=g_{mn}$

$$\frac{v_{out}}{v_{in}} = \frac{g_{mn}}{g_{mn} + 2g_{dsn}} \approx 1$$

(iii) Ignoring all capacitances except Cgs and CL derive an expression for the high frequency transfer function

KCL at output node

$$(v_{in}-v_{out})sC_{gs1}+g_{m1}(v_{in}-v_{out})-(v_{out}g_{ds1})-(v_{out}g_{ds2}+v_{out}sC_L)=0$$

$$(g_{m1}+sC_{gs1})v_{in}=(g_{m1}+g_{ds1}+g_{ds2}+sC_{gs1}+sC_L)v_{out}$$

$$\frac{v_{out}}{v_{in}}=\frac{g_{m1}+sC_{gs1}}{g_{m1}+g_{ds1}+g_{ds2}+sC_{gs1}+sC_L}$$

Using $g_{ds1}=g_{ds2}=g_{dsn}$, $g_{m1}=g_{m2}=g_{mn}$

$$\frac{v_{out}}{v_{in}}=\frac{g_{mn}+sC_{gs1}}{g_{mn}+2g_{dsn}+sC_{gs1}+sC_L}$$

$$\frac{v_{out}}{v_{in}}=\frac{g_{mn}}{g_{mn}+2g_{dsn}}\frac{\left(1+\frac{sC_{gs1}}{g_{mn}}\right)}{\left(1+\frac{s(C_{gs1}+C_L)}{g_{mn}+2g_{dsn}}\right)}$$

(iv) Calculate the pole and zero frequencies if V_{BIAS}=1V, V_t=0.75V, I_{BIAS}=100μA, C_{gs1}=1pF, C_L=9pF.

Pole frequency given by

$$|\omega_p| = \frac{g_{mn} + 2g_{dsn}}{(C_{gs1} + C_L)} \approx \frac{g_{mn}}{(C_{gs1} + C_L)}$$

$$g_{mn} = \frac{2I_D}{(V_{GS} - V_t)} = \frac{2 \times 100\mu A}{1 - 0.75} = 800\mu A/V$$

$$|\omega_p| \approx \frac{800\mu A/V}{1pF + 9pF} = 80Mrad/s$$

$$|\omega_z| = \frac{g_{mn}}{C_{gs1}} = \frac{800\mu A/V}{1pF} = 800Mrad/s$$

(v) Draw a Bode diagram of the gain. Indicate the dc gain and the gain at frequencies well above the pole and zero frequencies..

Zero frequency given by

$$|\omega_z| = \frac{g_{mn}}{C_{gs1}}$$

Pole frequency given by

$$|\omega_p| = \frac{g_{mn} + 2g_{dsn}}{(C_{gs1} + C_L)}$$