UE4010 Autumn 2004 Part A

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an nmos in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.

Question 1

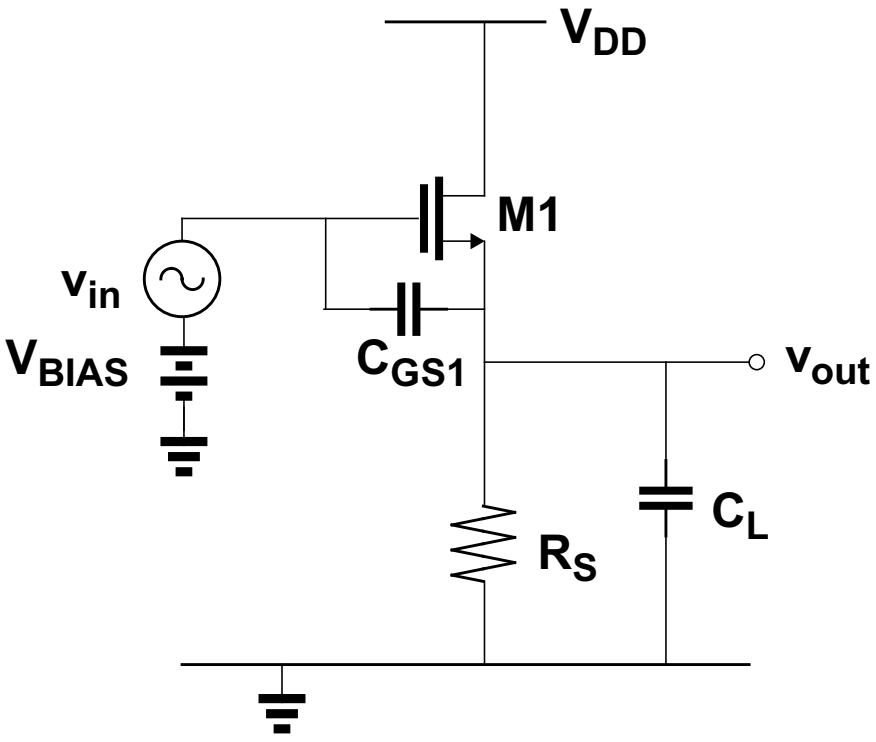


Figure 1

Figure 1 shows a source follower driving a resistive load. Assume M1 is in saturation and $g_{m1} >> g_{ds1}$.

(i) Draw the small-signal equivalent circuit for the source follower stage shown in Figure 1.
(ii) Ignoring all capacitances except C_{GS1} and C_L derive an expression for the high frequency transfer function.
(iii) Calculate the dc gain, pole and zero frequencies if V_{BIAS}=1.5V, K_n'=200μA/V^2, V_{tn}=0.75V, I_{D1}=100μA, W_1=16μm, L_1=1μm, C_{GS1}=1pF, C_L=9pF.
(iv) Draw a Bode diagram of the gain. On the diagram indicate the pole and zero frequencies, the value of the dc gain, and the value of the gain at frequencies well above the pole and zero frequencies.

Question 2

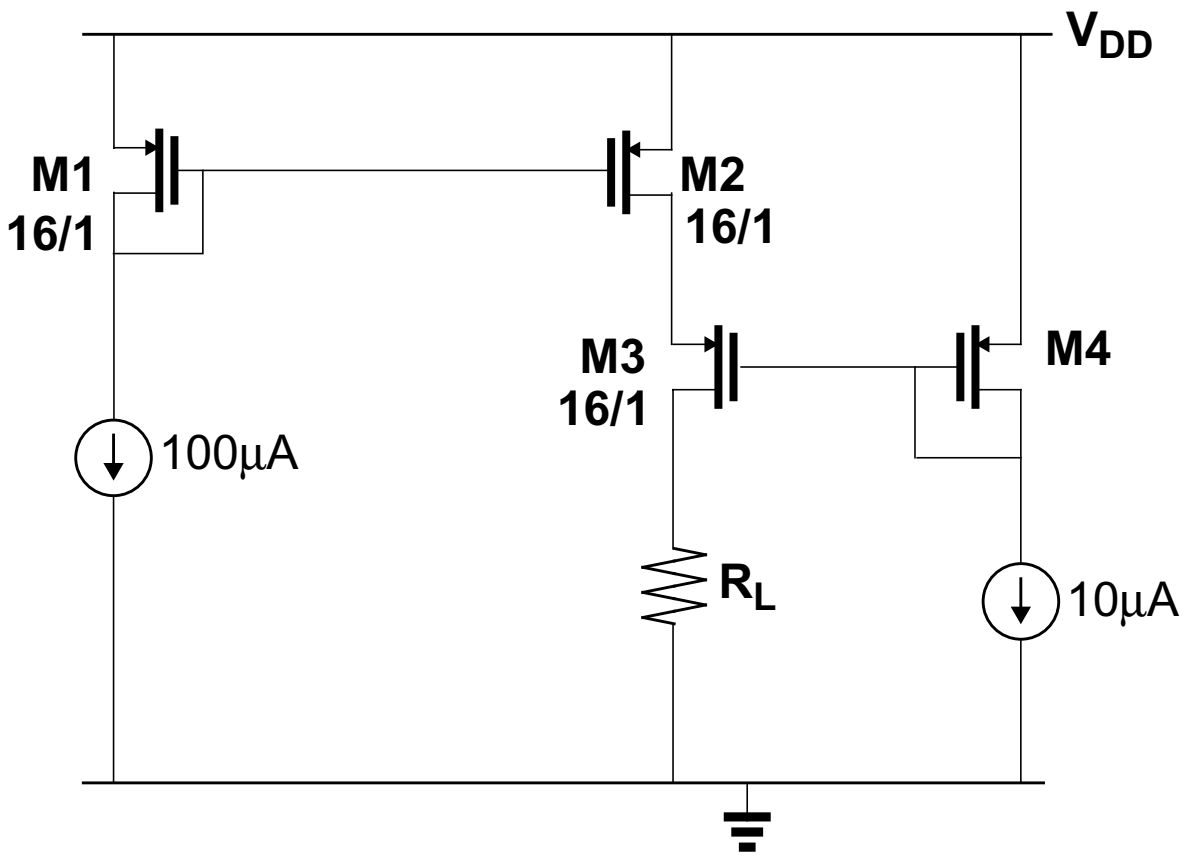


Figure 2

Figure 2 shows a pmos current mirror (M1, M2) with cascoded output. The bias voltage for the cascode is generated by the pmos diode M4.

For this question K_p'=50µA/V^2, V_{tp}= -750mV, V_{DD}=3V.

The device sizes of M1, M2 and M3 in microns are as indicated in Figure 2.

All devices are biased in saturation. For dc biasing calculations take λ=0.

(i) What is the maximum voltage at the drain of M2 such that M2 is just biased in saturation? If M4 has L=10, what is the required value of W for M4 such that M2 is just biased in saturation?

(ii) What is then the maximum value of R_L such that M3 is also biased in saturation?

(iii) Given the bias conditions established in (i) and (ii), estimate the percentage inaccuracy of the current mirror due to the finite output conductance of M1 and M2. For this calculation take λ_p=0.04V^{-1}.

(iv) Estimate the 3 sigma percentage inaccuracy of the current mirror due to transistor V_t mismatch. Note: Assume the mismatch is normally distributed and that the 1 sigma V_t mismatch of a transistor pair (in mV) is given by

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{WL}}$$

Take A_{Vt} = 10mVµm.

Question 3

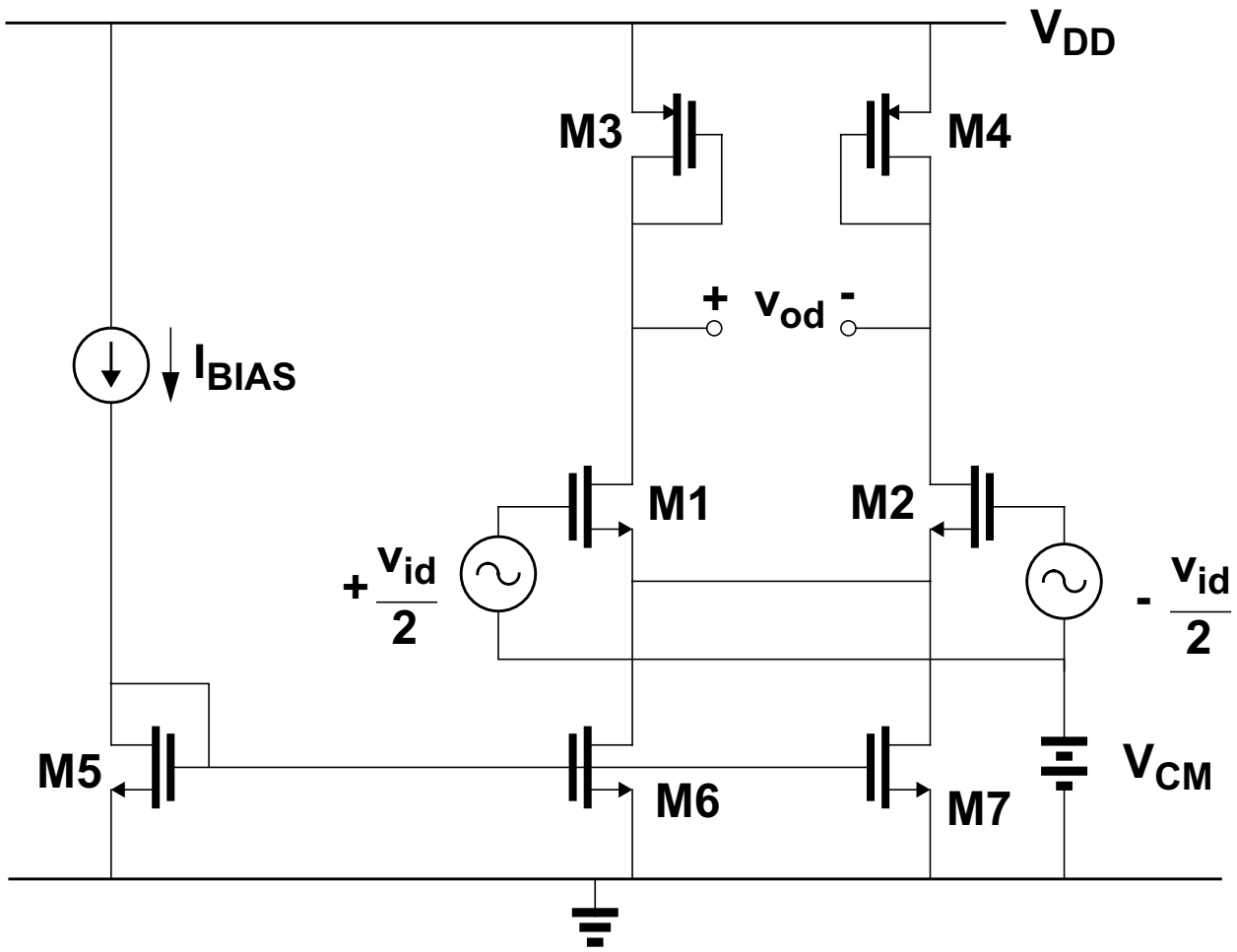


Figure 3

Figure 3 shows a differential amplifier with pmos diode loads.

V_{DD}=5V, I_{BIAS} = 100µA,K_n'=200µA/V^2, K_p'=50µA/V^2,V_{tn}=0.7V, V_{tp}=-0.7V

All transistors have W/L = 12.5µm/2µm.

Assume g_{mn} >> g_{dsn}, g_{mp} >> g_{dsp}.

You may assume the common source of M1,M2 is at ac ground.

(i) What is the small-signal low-frequency differential gain (v_{od}/v_{id}) of this amplifier in terms of the small-signal parameters?
(ii) What is the common-mode input range of this amplifier?
(iii) Calculate the value of low-frequency small-signal gain. Assume all transistors are in saturation.
(iv) What is value of the low-frequency small-signal gain if the current I_{BIAS} is doubled, assuming all transistors stay in saturation?

Question 4

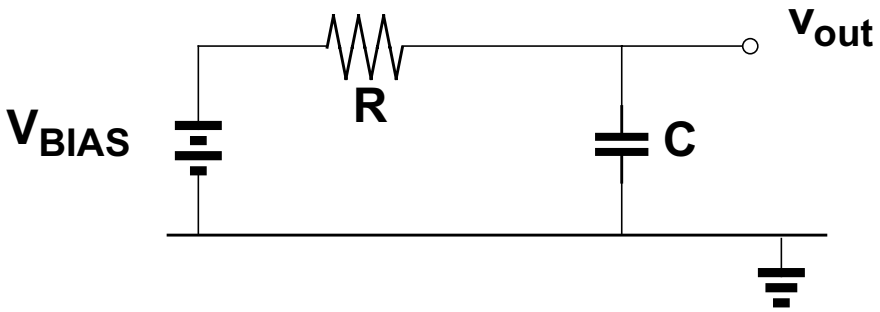


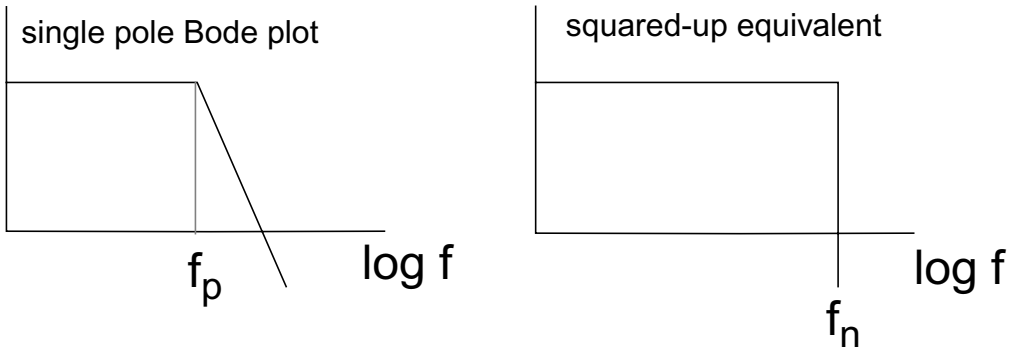
Figure 4

For numerical calculations take Boltzmann's constant k=1.38X10^{-23}J/^{o}K, temperature T=300^{o}K.

(i) Show that the total integrated thermal noise voltage at node v_{out} in Figure 4 is

$$v_{nout}^2 = \frac{kT}{C}$$

where k is Boltzmann's constant, and T is the temperature.
You may assume the following:



For the area underneath the curves to be the same then $f_n=(\pi/2)*f_p$

(ii) If R= 1kΩ and C=1pF calculate the total thermal noise in V_{rms} at node v_{out} in Figure 4?

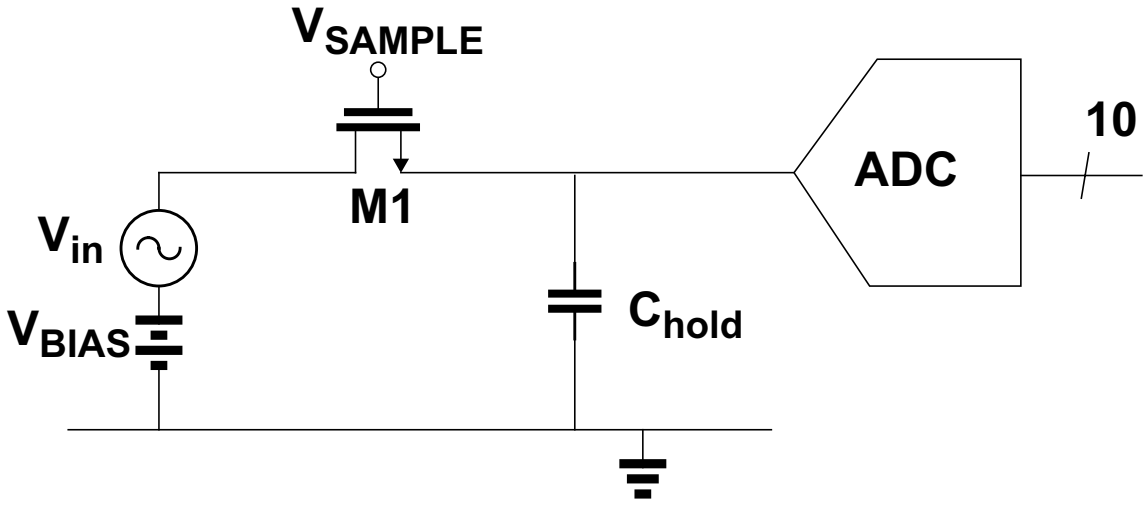


Figure 5

(iii) Figure 5 shows a sampling circuit preceding a 10-bit A/D converter. The sampling switch M1 is turned on.If the A/D converter has an input range of 1Vrms, and the noise budget for the sampling circuit is 0.1 LSB, what is the minimum value required for C_{hold}?

(iv) If a 12-bit A/D converter is used with the same input range, and the noise budget for the sampling circuit is kept at 0.1LSB, what is the new minimum value required for C_{hold}?