Part A

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an nmos in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For d.c. biasing calculations you may take $\lambda=0$

Question 1

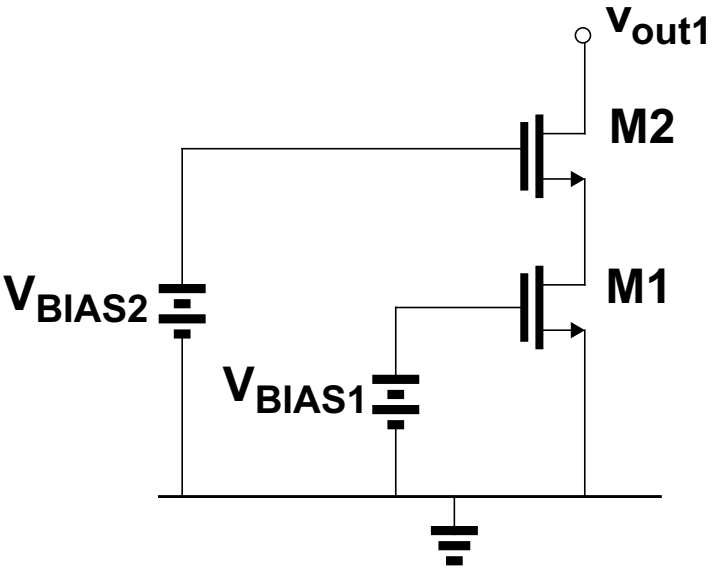


Figure 1a

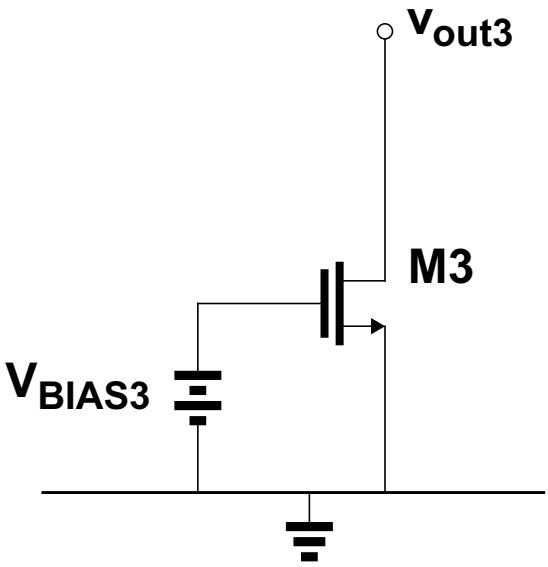


Figure 1b

(i) Draw the small-signal model of the cascode stage shown in Figure 1a.

(ii) Derive an expression for the output resistance r_{out1} of the cascode stage i.e. the resistance looking into the output node v_{out1} and show that this can be simplified to

$$r_{out1} = \frac{g_{m2}}{g_{ds2}} \cdot \frac{1}{g_{ds1}}$$

assuming $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$

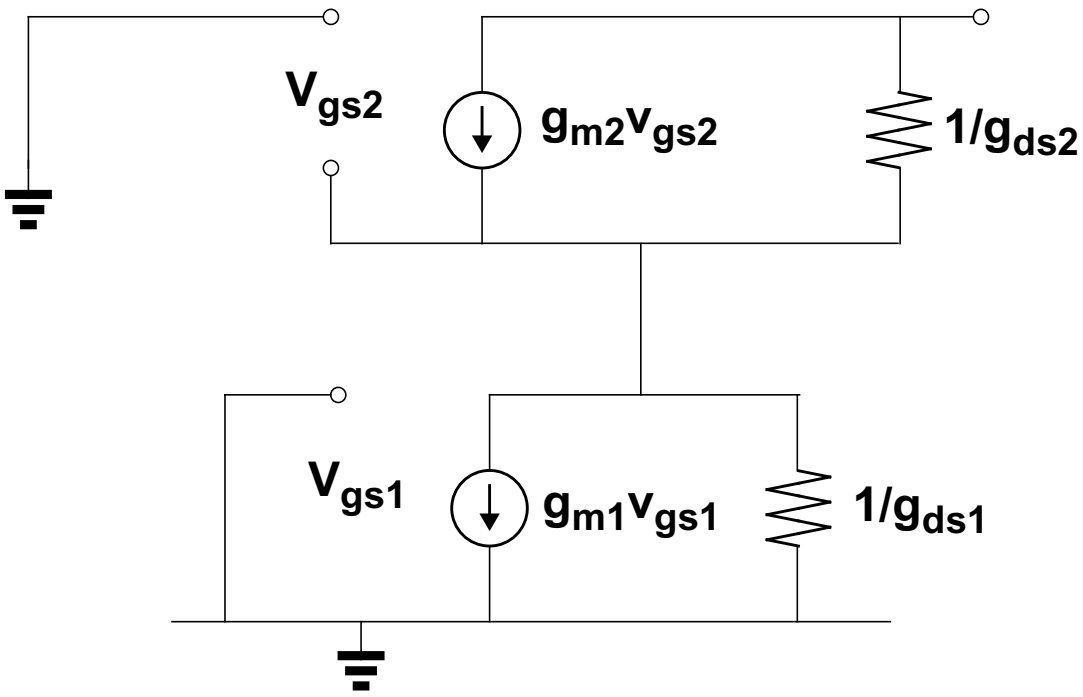
(iii) $W_1=W_2=8\mu m$, $L_1=L_2=1\mu m$, $K_n'=200\mu A/V^2$, $V_{tn}=0.75V$ and V_{BIAS1} is set so that $I_{D1}=200\mu A$ in saturation.
What is the minimum value of voltage at the drain of M1 such that M1 is in saturation?
What is the value of V_{BIAS2} required to achieve this biasing condition?
What is the headroom (i.e. the minimum voltage at the output such that all devices are in saturation) required by the cascode stage?

(iv) Figure 1b shows a simple transistor stage. If this stage is implemented in the same technology with the same bias current, transistor width and voltage headroom as the cascode stage, what is the maximum value of L3 such that M3 is in saturation?

(v) Calculate the approximate output resistances of the configurations shown in Figure 1a and 1b for the bias conditions and dimensions used in (iii) and (iv).
Take $\lambda_n=0.04/L\ V^{-1}$ (L in μm) for this calculation.

Solution

(i) Draw the small-signal model of the cascode stage shown in Figure 1a.

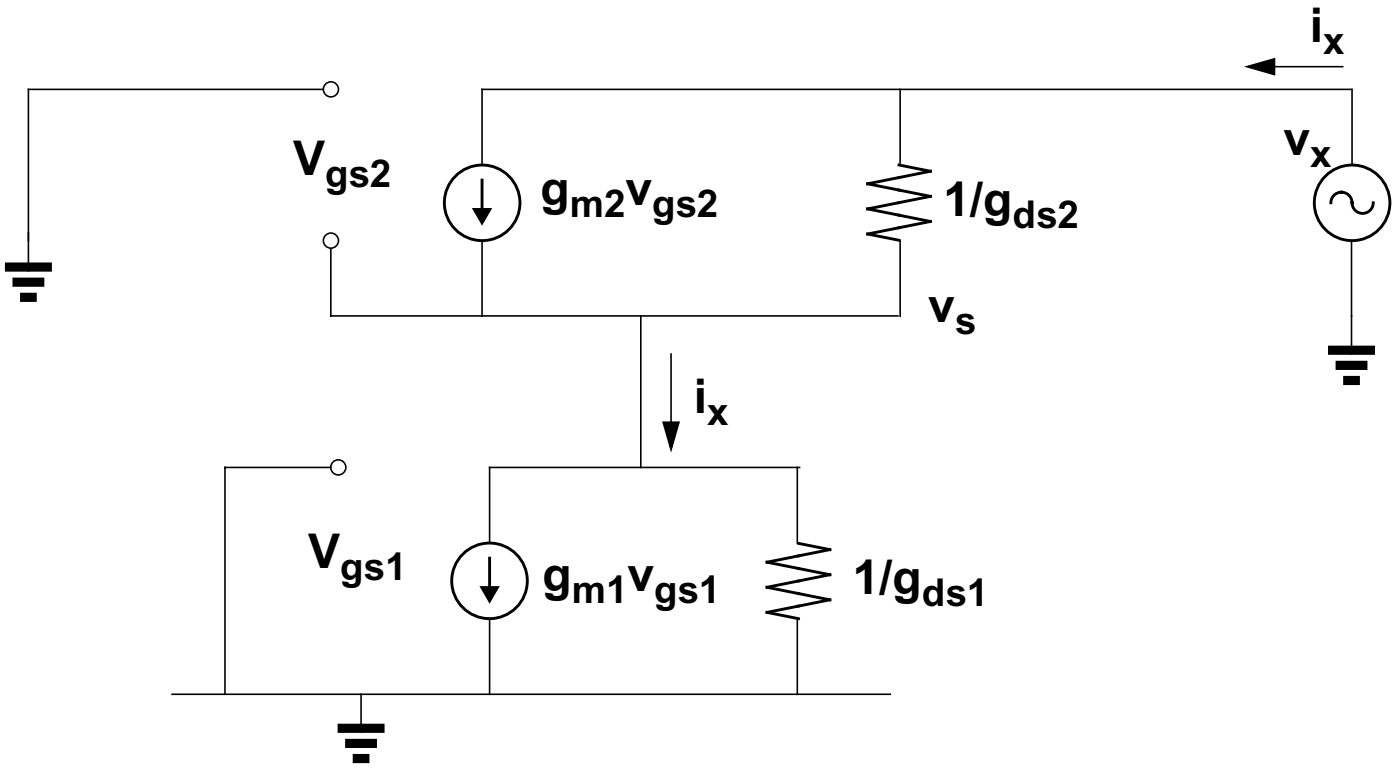


(ii) Derive an expression for the output resistance r_{out1} of the cascode stage i.e. the resistance looking into the output node v_{out1} and show that this can be simplified to

$$r_{out1} = \frac{g_{m2}}{g_{ds2}} \cdot \frac{1}{g_{ds1}}$$

assuming $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$

To derive the output resistance put a test voltage at the output node and calculate the small-signal current into the circuit.



Note: $v_{gs1} = 0 \Rightarrow g_{m1} v_{gs1} = 0$

$$i_x = g_{m2} v_{gs2} + (v_x - v_s) g_{ds2}$$

Since $v_{gs2} = -v_s$ and $v_s = \frac{i_x}{g_{ds1}}$

$$i_x = -(g_{m2}) \frac{i_x}{g_{ds1}} + \left(v_x - \frac{i_x}{g_{ds1}} \right) g_{ds2}$$

$$r_{out} = \frac{v_x}{i_x} = \frac{1 + \frac{g_{m2}}{g_{ds1}} + \frac{g_{ds2}}{g_{ds1}}}{g_{ds2}}$$

Since $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$ this can be reduced to

$$r_{out} = \frac{g_{m2}}{g_{ds2}} \cdot \frac{1}{g_{ds1}}$$

(iii) $W_1=W_2=8\mu m$, $L_1=L_2=1\mu m$, $K_n'=200\mu A/V^2$, $V_{tn}=0.75V$ and V_{BIAS1} is set so that $I_{D1}=200\mu A$ in saturation.
What is the minimum value of voltage at the drain of M1 such that M1 is in saturation?
What is the value of V_{BIAS2} required to achieve this biasing condition?
What is the headroom (i.e. the minimum voltage at the output such that all devices are in saturation) required by the cascode stage?

For M1 to be in saturation then

$$V_{DS1} \geq V_{GS1} - V_t$$

$$\left|V_{GS1} - V_t\right| = \sqrt{\frac{2I_{D1}}{K_n' \frac{W_1}{L_1}}} = \sqrt{\frac{2 \cdot 200\mu A}{200\mu A/V^2 \frac{8}{1}}} = 500mV$$

$$(V_{DS1})_{min} = V_{GS1} - V_T = 0.5V$$

As

$$\left|V_{GS2} - V_t\right| = \sqrt{\frac{2I_{D2}}{K_n' \frac{W_2}{L_2}}} = \sqrt{\frac{2 \cdot 200\mu A}{200\mu A/V^2 \frac{8}{1}}} = 500mV$$

$$V_{BIAS2} = V_{GS2} + (V_{DS1})_{min}$$

$$V_{BIAS2} = (V_{GS2} - V_t) + V_t + (V_{DS1})_{min} = 0.5V + 0.75V + 0.5V = \underline{1.75V}$$

$$V_{DS2} \geq V_{GS2} - V_t$$

so minimum voltage at the output for both transistors to be in saturation is given by

$$V_{outmin} = (V_{DS1})_{min} + (V_{DS2})_{min} = 1V$$

(iv) Figure 1b shows a simple transistor stage. If this stage is implemented in the same technolgy as the cascode stage, with the same bias current, transistor width and voltage headroom requirement as the cascode stage what is the maximum value of L3 such that M3 is in saturation?

$$(V_{GS1}-V_t) = \sqrt{\frac{2I_{D1}}{K_n \frac{W_1}{L_1}}} \qquad (V_{GS3}-V_t) = \sqrt{\frac{2I_{D3}}{K_n \frac{W_3}{L_1}}}$$

As $V_{GS3}-V_t = 2*(V_{GS}1-V_t)$, $I_{D1}=I_{D3}$, $W_1=W_3$, can divide these expressions to get

$$2 = \sqrt{\frac{L_3}{L_1}} \Rightarrow L_3 = 4 \times L_1 = 4\mu m$$

(v) Calculate the approximate output resistances of the configurations shown in Figure 1a and 1b for the bias conditions given. Take $\lambda_n=0.04/L\ V^{-1}$ (L in μm) for this calculation.

$$g_{m2} = \frac{2I_{D2}}{(V_{GS}-V_t)} = \frac{2 \times 200\mu A}{0.5} = 800\mu A/V$$

$$g_{ds1} = \lambda I_{D1} = \frac{0.04}{L_1} I_{D1} = \frac{0.04}{1} 200\mu A = 8\mu A/V$$

$$g_{ds3} = \lambda I_{D3} = \frac{0.04}{L_3} I_{D3} = \frac{0.04}{4} 200\mu A = 2\mu A/V$$

$$r_{out1} = \frac{g_{m2}}{g_{ds2}} \cdot \frac{1}{g_{ds1}} = \frac{800\mu A/V}{8\mu A/V} \cdot \frac{1}{8\mu A/V} = 12.5M\Omega$$

$$r_{out2} = \frac{1}{g_{ds3}} = \frac{1}{2\mu A/V} = 500k\Omega$$

Question 2

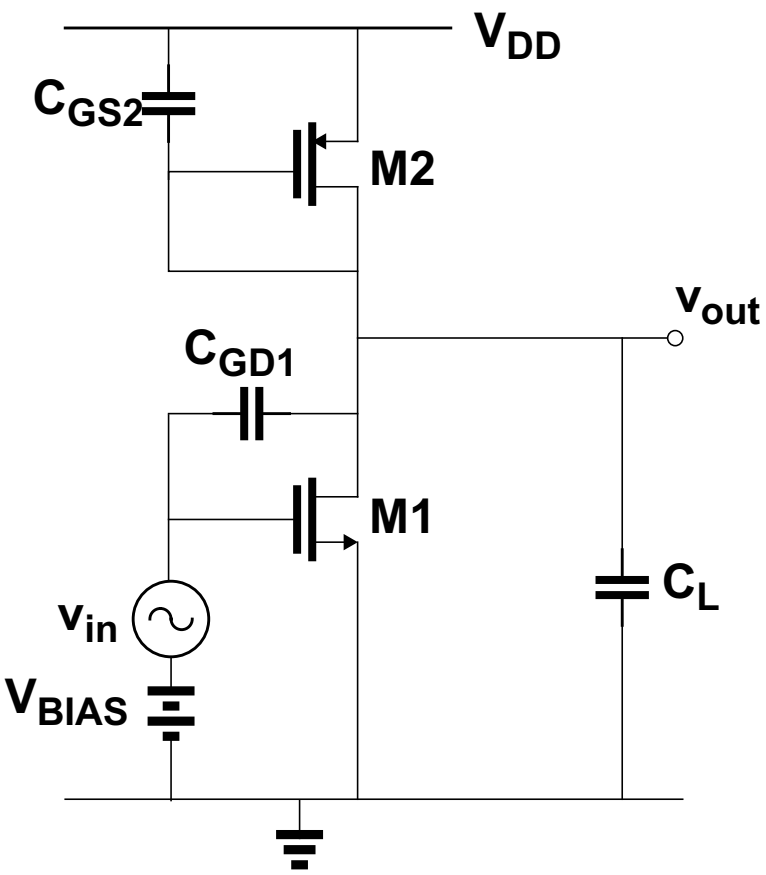
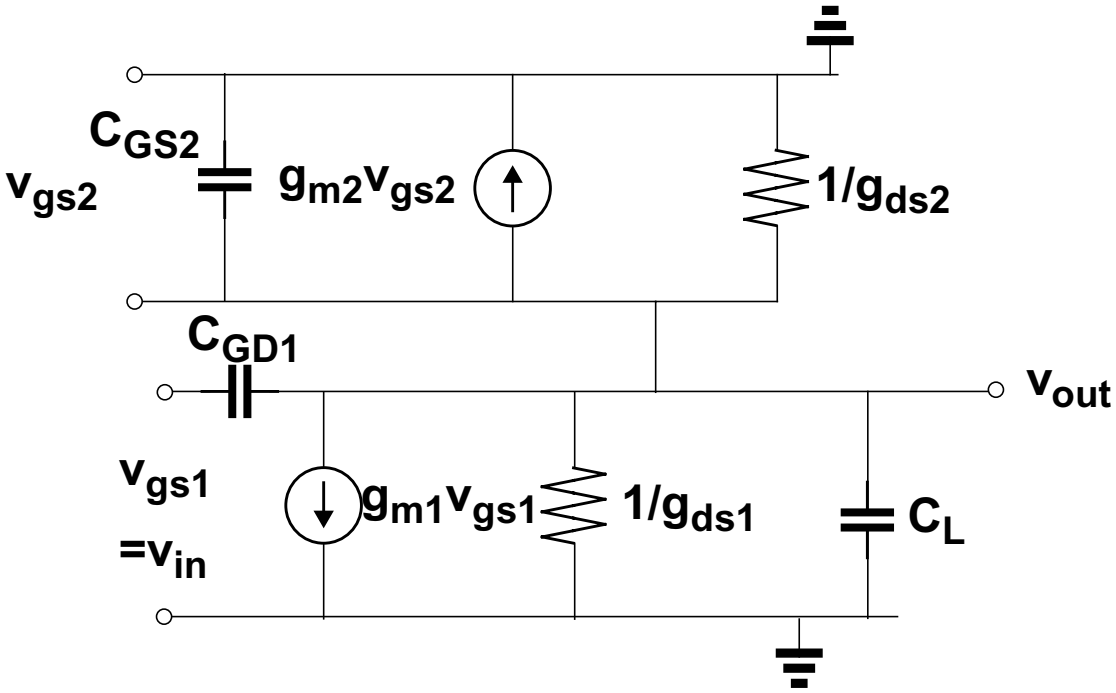


Figure 2

For the questions below you may assume g_{m1},g_{m2}>>g_{ds1},g_{ds2} and that all devices are biased in saturation.

(i) Figure 2 shows a gain stage with a diode-connected load. Draw the small-signal model for this circuit.
(ii) Derive an expression for the low-frequency small signal voltage gain (v_{out}/v_{in}).
(iii) Ignoring all capacitances except C_{GD1}, C_{GS2} and C_L derive an expression for the high-frequency transfer function.
(iv) Calculate the low-frequency gain (v_{out}/v_{in}) and the pole and zero frequencies if V_{GS1}=1V,V_{GS2}=1.75V, V_{tn}=|V_{tp}|=0.75V, I_{D1}=250μA, C_{GD1}=0.1pF, C_{GS2}=1pF, C_L=1.5pF.
(v) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the pole and zero frequencies.

(i) Figure 2 shows a gain stage with a diode-connected load. Draw the small-signal model for this circuit.



(ii) Derive an expression for the low-frequency small signal voltage gain (v_{out}/v_{in}).

Current at outout node

$$g_{m1}v_{gs1} + g_{m2}v_{gs2} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$g_{m1}v_{in} + g_{m2}v_{out} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \cong -\frac{g_{m1}}{g_{m2}}$$

Alternatively recognise that the current of the current-source $g_{m2}v_{gs2}$ is determined by voltage across its terminals i.e. is equivalent to a resistance $1/g_{m2}$.

Since $1/g_{m2} << 1/g_{ds2}$, $1/g_{m2} << 1/g_{ds1,}$ can write directly

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2}}$$

(iii) Ignoring all capacitances except C_{GD1}, C_{GS2} and C_L derive an expression for the high-frequency transfer function.

KCL at outout node

$$g_{m1}v_{gs1} + g_{m2}v_{gs2} + v_{out}g_{ds1} + v_{out}g_{ds2} + v_{out}s(C_L + C_{GS2}) - (v_{in} - v_{out})sC_{GD1} = 0$$

$$g_{m1}v_{in1} + g_{m2}v_{out} + v_{out}g_{ds1} + v_{out}g_{ds2} + v_{out}s(C_L + C_{GS2}) - (v_{in} - v_{out})sC_{GD1} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} - sC_{GD1}}{g_{m2} + g_{ds1} + g_{ds2} + s(C_L + C_{GS2})}$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}\left(1 - \frac{sC_{GD1}}{g_{m1}}\right)}{g_{m2} + g_{ds1} + g_{ds2}\left(1 + \frac{s(C_{GS2} + C_L)}{g_{m2} + g_{ds1} + g_{ds2}}\right)}$$

$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}\left(1 - \frac{sC_{GD1}}{g_{m1}}\right)}{g_{m2}\left(1 + \frac{s(C_{GS2} + C_L)}{g_{m2}}\right)}$$

Alternatively use $1/g_{m2}$ approx. for diode connected M2 and get simpler derivation.

(iv) Calculate the low-frequency gain (v_{out}/v_{in}) and the pole and zero frequencies if V_{GS1}=1V,V_{GS2}=1.75V, V_{tn}=|V_{tp}|=0.75V, I_{D1}=250μA, C_{GD1}=0.1pF, C_{GS2}=1pF, C_L=1.5pF.

$$g_{m1} = \frac{2I_{D1}}{(V_{GS1}-V_{tn})} = \frac{2\times 250\mu A}{1-0.75} = 2000\mu A/V$$

$$g_{m2} = \frac{2|I_{D2}|}{(|V_{GS2}|-V_{tp})} = \frac{2\times 250\mu A}{1.75-0.75} = 500\mu A/V$$

Low-frequency gain given by

$$\frac{v_{out}}{v_{in}} \cong -\frac{g_{m1}}{g_{m2}} = \frac{2000\mu A/V}{500\mu A/V} = -4$$

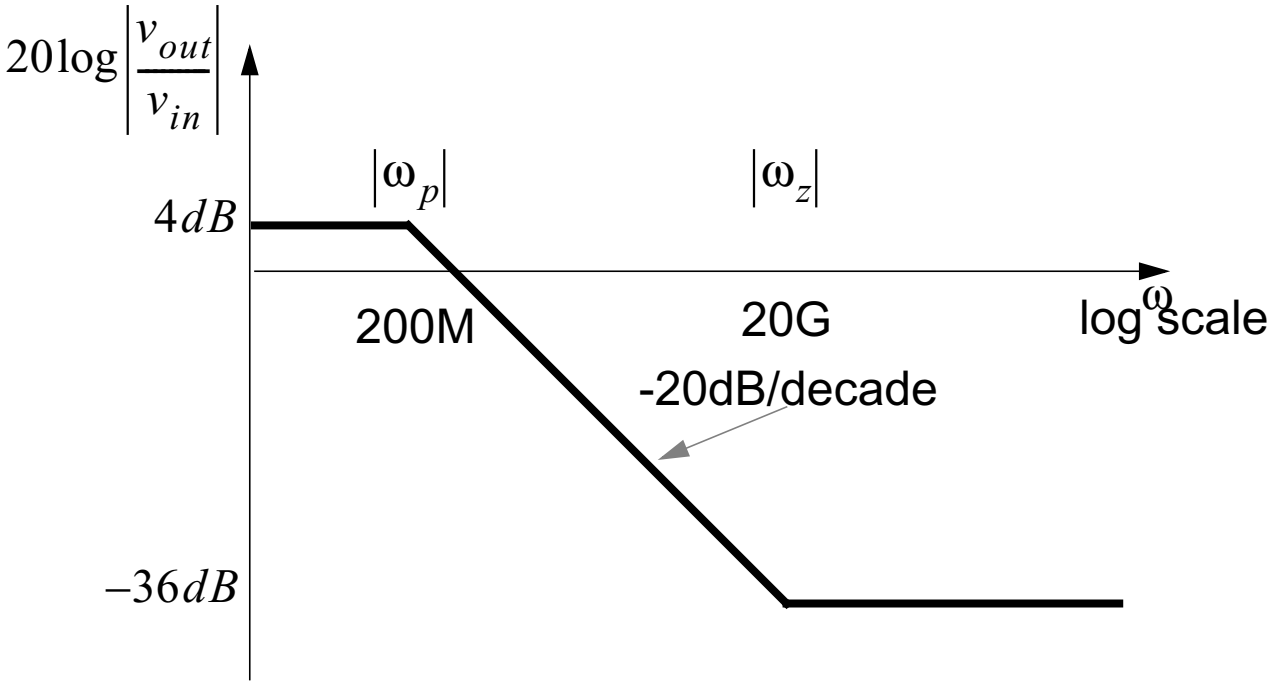
Zero frequency given by

$$|\omega_z| = \frac{g_{m1}}{C_{GD1}} = \frac{2000\mu A/V}{0.1\,pF} = 20\,Grad/s$$

Pole frequency given by

$$|\omega_p| = \frac{g_{m2}}{C_{GS2}+C_L} = \frac{500\mu A/V}{1\,pF+1.5\,pF} = 200\,Mrad/s$$

(v) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the pole and zero frequencies.



Question 3

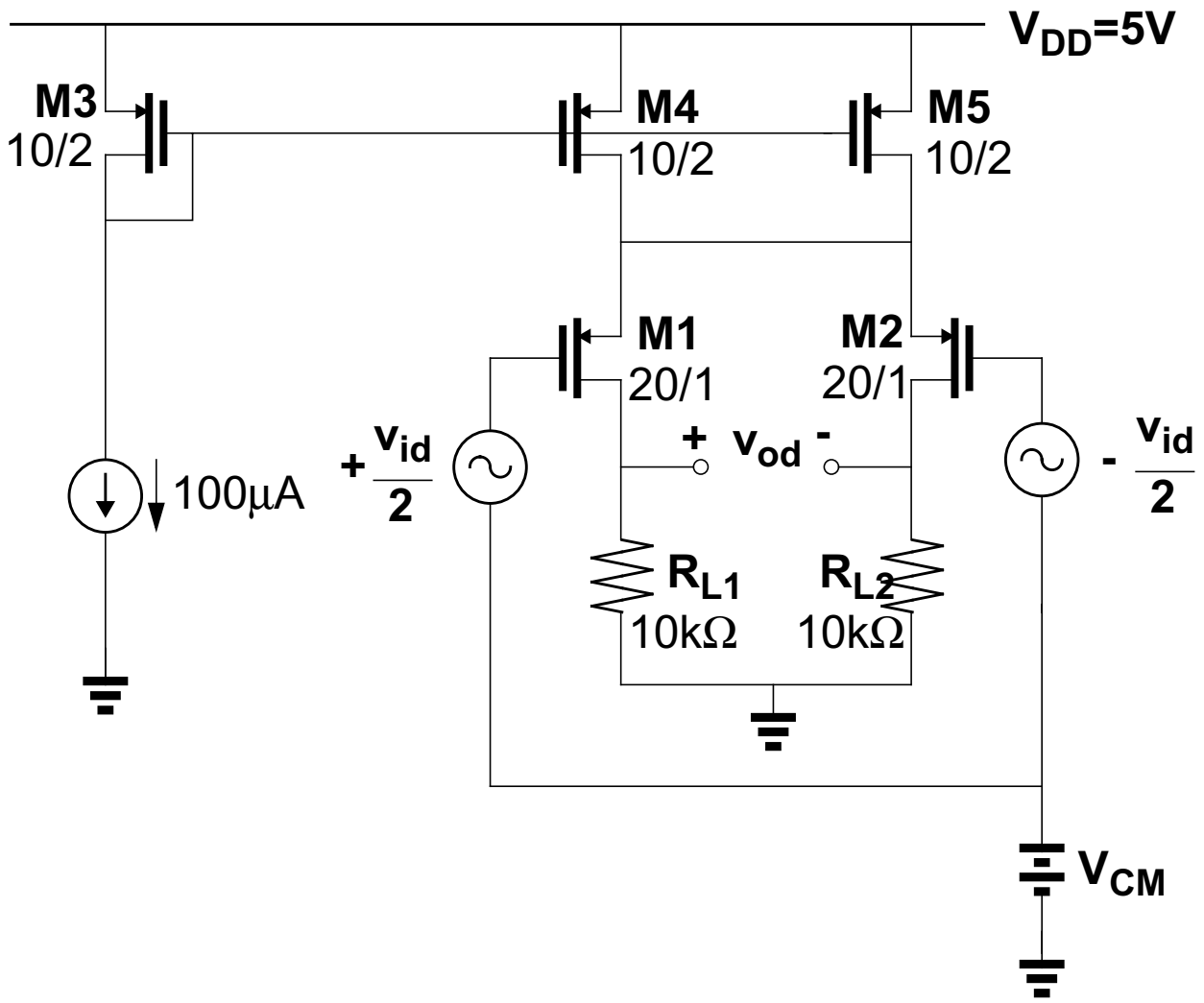


Figure 3

Figure 3 shows a pmos differential pair biased by a common-mode voltage V_{CM}.

For the calculations below use K_p'=50µA/V^2, $|V_{tp}|$=0.8V.

(i) What is the maximum value of V_{CM} such that all devices are still biased in saturation?
(ii) What is the minimum value of V_{CM} such that all devices are still biased in saturation?
(iii) A differential small-signal v_{id} is applied at the inputs. Give an expression for the low-frequency small signal voltage gain (v_{od}/v_{id}).
(iv) Calculate the low-frequency small signal voltage gain. Assume all devices are biased in saturation and $1/g_{ds1}, 1/g_{ds2} >> R_{L1}, R_{L2}$.
(v) A small signal sine wave with a differential peak-peak voltage of 40mV is applied to the inputs. The common-mode voltage $V_{CM}=V_{DD}/2$. What is the maximum value of gain that can be achieved by increasing the load resistance (R_L and R_{L2})?

(i) What is the maximum value of V_{CM} such that all devices are still biased in saturation.

For M4 in saturation

$$V_{CM} \le V_{DD} - |V_{GT4}| - |V_{GS3}|$$

M4 $$|V_{GS4} - V_{tp}| = \sqrt{\frac{2 \cdot 100\mu A}{50\mu A/V \cdot \frac{10}{2}}} = 894mV$$

M1 $$|V_{GS1} - V_{tp}| = \sqrt{\frac{2 \cdot 100\mu A}{50\mu A/V \cdot \frac{20}{1}}} = 447mV \Rightarrow |V_{GS3}| = 1.247V$$

$$V_{CM} \le 5 - 0.894V - 1.247 = 2.859V$$

(ii) What is the minimum value of V_{CM} such that all devices are still biased in saturation.

For M1 in saturation

$$V_{CM} + |V_{GS1}| - |V_{GT1}| \ge IR_L$$

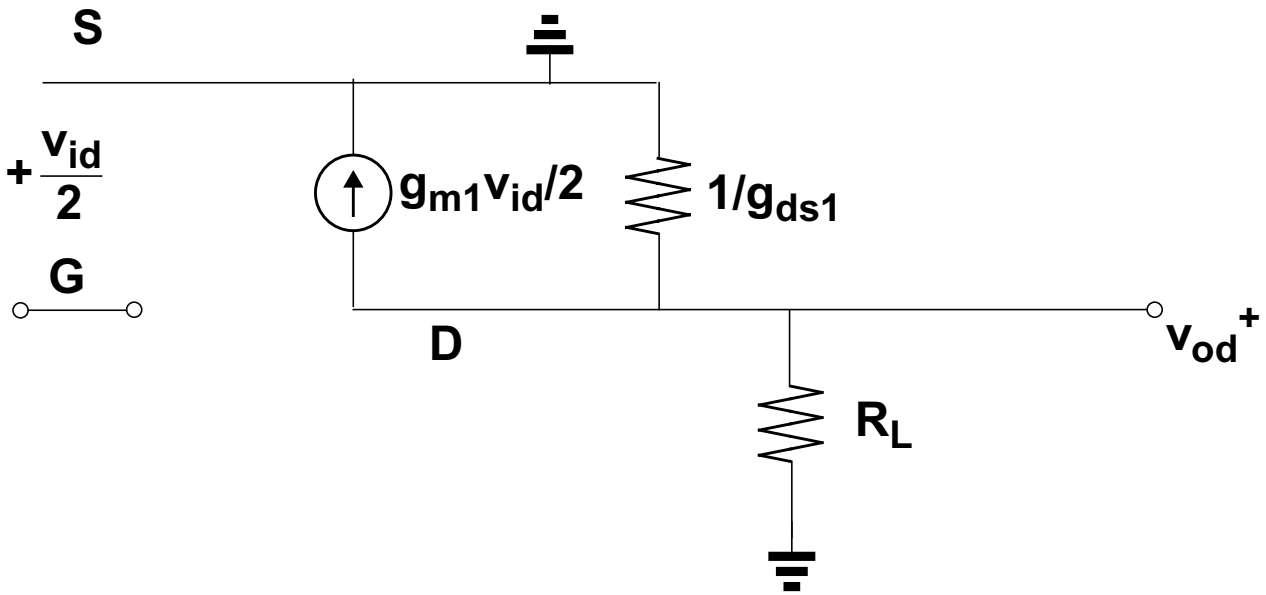
$$V_{CM} \ge |V_{tp}| + IR_L$$

$$V_{CM} \ge 0.8 + 100\mu A \times 10k\Omega$$

$$V_{CM} \ge 1.8V$$

(iii) A differential small-signal v_{id} is applied at the inputs. Give an expression for the low-frequency small signal voltage gain (v_{od}/v_{id}).

Common source of M1,M2 is at ac ground.
Use half-circuit method:



$$v_{od}^{+} = -\frac{g_{m1}\frac{v_{id}}{2}}{g_{ds1}+\frac{1}{R_L}}$$

$$v_{od} = v_{od}^{+} - v_{od}^{-} = -\frac{g_{m1}\frac{v_{id}}{2}}{g_{ds1}+\frac{1}{R_L}} - \left(-\frac{g_{m2}-\frac{v_{id}}{2}}{g_{ds2}+\frac{1}{R_L}}\right)$$

Assume M1=M2

$$v_{od} = -\frac{g_m}{g_{ds}+\frac{1}{R_L}}v_{id} \qquad \frac{v_{od}}{v_{id}} = -\frac{g_m}{g_{ds}+\frac{1}{R_L}}$$

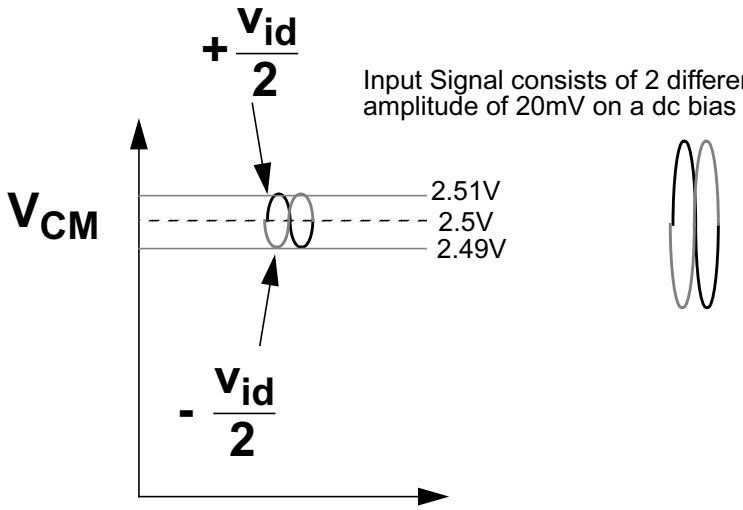
Alternatively write this answer directly by observation.

(iv) Calculate the low-frequency small signal voltage gain. Assume all devices are biased in saturation and $1/g_{ds1} >> R_L$.

$$g_{m1} = \frac{2I_D}{|V_{GS1} - V_{tp}|} = \frac{2 \times 100\mu A}{0.447} = 447\mu A/V$$

$$\frac{v_{od}}{v_{id}} = -\frac{g_{m1}}{g_{ds1} + \frac{1}{R_L}} \approx -g_{m1}R_L = -(447\mu A/V \times 10k\Omega) = -4.47$$

(v) A small signal sine wave with a differential peak-peak voltage of 40mV is applied to the inputs. The common-mode voltage $V_{CM}=V_{DD}/2$. What is the maximum value of gain that can be achieved by increasing R_L?



Input Signal consists of 2 differential signals each with peak-peak amplitude of 20mV on a dc bias voltage of 2.5V ($V_{DD}/2$)

Max gain is when dc voltage at output plus the positive peak of the amplified signal forces M1 out of saturation

This occurs when input voltage is VCM - vin

$$V_{out(peak)} \le V_{CM} - v_{in} + \left|V_{GS1}\right| - \left|V_{GT1}\right|$$

$$V_{out(peak)} \le 2.49 - 0.8 \;=\; 1.69V$$

The voltage at the output is the sum of the dc voltage and amplified ac input signal

$$V_{out(peak)} \;=\; IR_L - g_{m1}R_L v_{in}$$

$$V_{out(peak)} \;=\; R_L(I - g_{m1}v_{in})$$

$$R_L(I - g_{m1}v_{in}) \le 1.69V$$

$$R_L(100\mu A - 447\mu A/V \times -5mV) \le 1.69V$$

$$R_L \le 17.3k\Omega$$