OLLSCOIL NA hÉIREANN
THE NATIONAL UNIVERSITY OF IRELAND

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

Summer 2009
2009 Engineering (Electrical & Electronic) Examination

Microelectronics (UE4010)

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Time allowed **1 ½ Hours**
Answer three out of four questions

Approved calculator permitted.

Question 1:

a) With the aid of diagrams describe how certain elements of a MOS transistor have changed in the shrink from processes with minimum dimensions of about 1.0μm to processes with dimensions in the region of 45-65nm. Give a very brief explanation for the technological reasons for these changes. (Hint: concentrate on the "Gate Stack" and substrate.)
b) In the shrink from 65nm to 45nm a company changes the gate dielectric to hafnium oxide with a dielectric constant of 25, if the resultant gate capacitance is 3.0 X 10^{-6} F/cm^2 what is the actual new dielectric thickness and the silicon dioxide equivalent?

Given:
The permittivity of free space is 8.86 X 10^{-14} F/cm
The dielectric constant of silicon dioxide is 3.9

Question 2:

a) Describe a physical model for the thermal oxidation of silicon.
b) Why typically does a thermal oxidation finish with a nitrogen anneal cycle? Relate this practice to the electrical parameters of a MOS device.
c) Describe what happens to boron contained in the silicon during thermal oxidation.
d) A silicon <100> wafer, which had been patterned for ion implant with 90nm of oxide in the windows to be implanted and 0.5μm in the other areas to protect against the implant, is put through a thermal oxide process at 1000°C in pyrogenic steam for 1 hour 40minutes, what is the final oxide thickness in:
    i) The areas which had 90nm on the surface prior to oxidation?
    ii) The areas which had 0.5μm on the surface prior to oxidation?

Question 3

a) In relation to a high energy beam of ions striking the surface of crystalline silicon explain the following terms
    (i) Range
    (ii) Projected range
    (iii) Straggle
b) Explain the function(s) of the high temperature heat treatment given to wafers following ion implantation
c) What energy is needed to place the peak of a phosphorus implant at the silicon/oxide interface if the oxide thickness is 0.07μm, and what thickness of oxide is needed to protect other parts of the silicon from this implant? The implant dose is 1X 10^{16}/$cm^2$and the background concentration is 1 10^{15}/cm^3.

Given:

$C_{(x)} = C_p.\exp[-(x-R_p)^2/2\Delta R_p^2]$

Projected Range and Projected Standard Deviation Graphs attached.

Question 4

a) Describe how parasitic or field devices can be formed in a CMOS process; what measures can be taken to prevent the turn on of these devices, use diagrams to illustrate the answer.

b) What can an analogue designer do to increase or decrease the current flow in an NMOS transistor in a mature CMOS process?

c) In an NMOS process with a minimum allowed drawn gate length of 2.0μm, a threshold voltage of 0.8V and a power supply voltage of 10V. What is the smallest device that can be used to deliver a current of 10mA between the source and drain?