

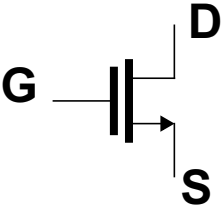
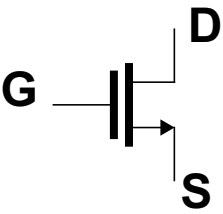
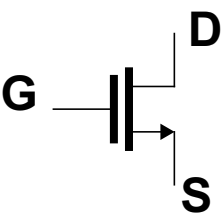
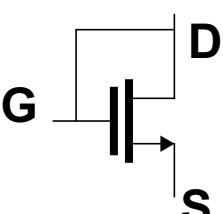
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# **UE4002 Analog IC Design**

**Problem solutions, supplementary notes**

## Problems P39: NMOS Operating regions

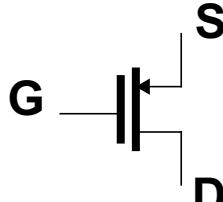
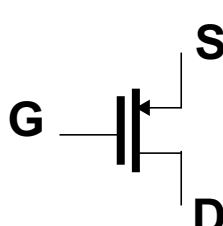
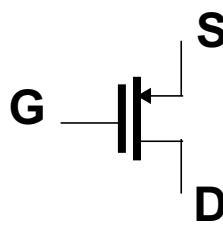
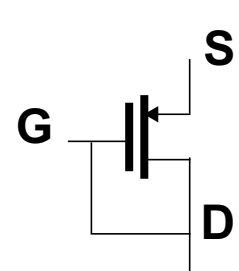
1. What is the operating region of the following nmos transistors?  
Take  $V_t = 1V$  and assume the bulk is tied to the source.

- (i)
- 
- $V_G = 2V$   
 $V_S = 0V$   
 $V_D = 3V$
- $V_{GS} = 2V$   
 $V_{GS} > V_t \Rightarrow \text{ON}$   
 $V_{GS} - V_t = 1V$   
 $V_{DS} = 3V$   
 $V_{DS} > V_{GS} - V_t \Rightarrow \text{Sat.}$
- (ii)
- 
- $V_G = 2V$   
 $V_S = 0V$   
 $V_D = 0.5V$
- $V_{GS} = 2V \Rightarrow \text{ON}$   
 $V_{GS} - V_t = 1V$   
 $V_{DS} = 0.5V \Rightarrow \text{Linear}$
- (iii)
- 
- $V_G = 0.5V$   
 $V_S = 0V$   
 $V_D = 3V$
- $V_{GS} = 0.5V$   
 $V_{GS} < V_t \Rightarrow \text{OFF}$
- (iv)
- 
- $V_S = 0V$   
 $V_D = 2V$
- $V_D = V_G$   
 $V_{GS} = V_{DS} = 2V \Rightarrow \text{ON}$   
 $V_{DS} > V_{GS} - V_t \Rightarrow \text{Sat.}$

**NMOS diode: If ON, then in saturation.**

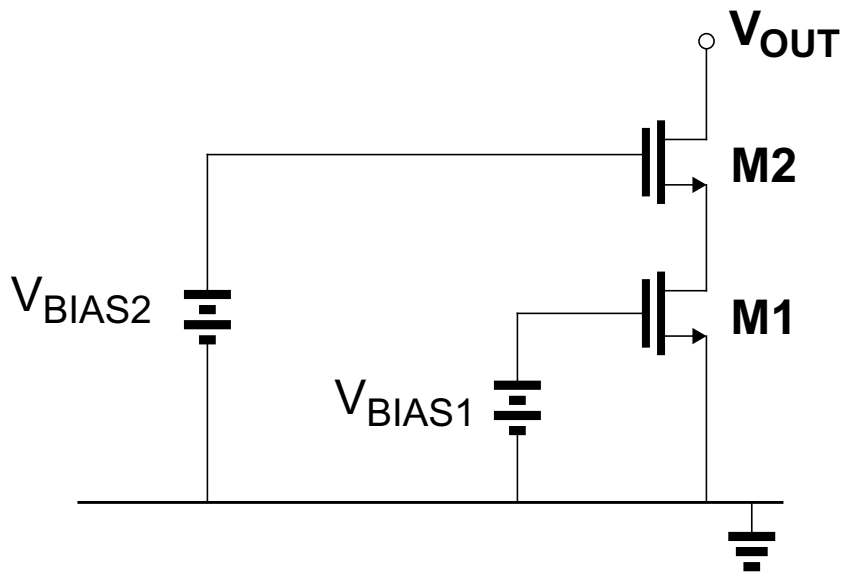
## Problems P40: PMOS Operating regions

1. What is the operating region of the following pmos transistors?  
Take  $V_t = -1V$  and assume the bulk is tied to the source.

(i)		$V_G = 3V$ $V_S = 5V$ $V_D = 3V$	$V_{GS} = -2V$ $V_{GS} < V_t \Rightarrow \text{ON}$ $V_{GS} - V_t = -1V$ $V_{DS} = -2V$ $V_{DS} < V_{GS} - V_t \Rightarrow \text{Sat.}$
(ii)		$V_G = 3V$ $V_S = 5V$ $V_D = 4.5V$	$V_{GS} = -2V \Rightarrow \text{ON}$ $V_{GS} - V_t = -1V$ $V_{DS} = -0.5V$ $V_{DS} > V_{GS} - V_t \Rightarrow \text{Linear}$
(iii)		$V_G = 4.5V$ $V_S = 5V$ $V_D = 3V$	$V_{GS} = -0.5V$ $V_{GS} > V_t \Rightarrow \text{OFF}$
(iv)		$V_S = 5V$ $V_D = 3V$	$V_D = V_G$ $V_{GS} = V_{DS} = -2V \Rightarrow \text{ON}$ $V_{DS} < V_{GS} - V_t \Rightarrow \text{Sat.}$

**PMOS diode: If ON, then in saturation.**

## Problem P.55 DC Biasing (2)



The body effect may be ignored.

- (i) The circuit shown is to be biased for optimal low-voltage operation.

If

$$V_{BIAS1} = 1.2V$$

$$V_T = 0.8V$$

$$(W/L)_{M2} = (W/L)_{M1}$$

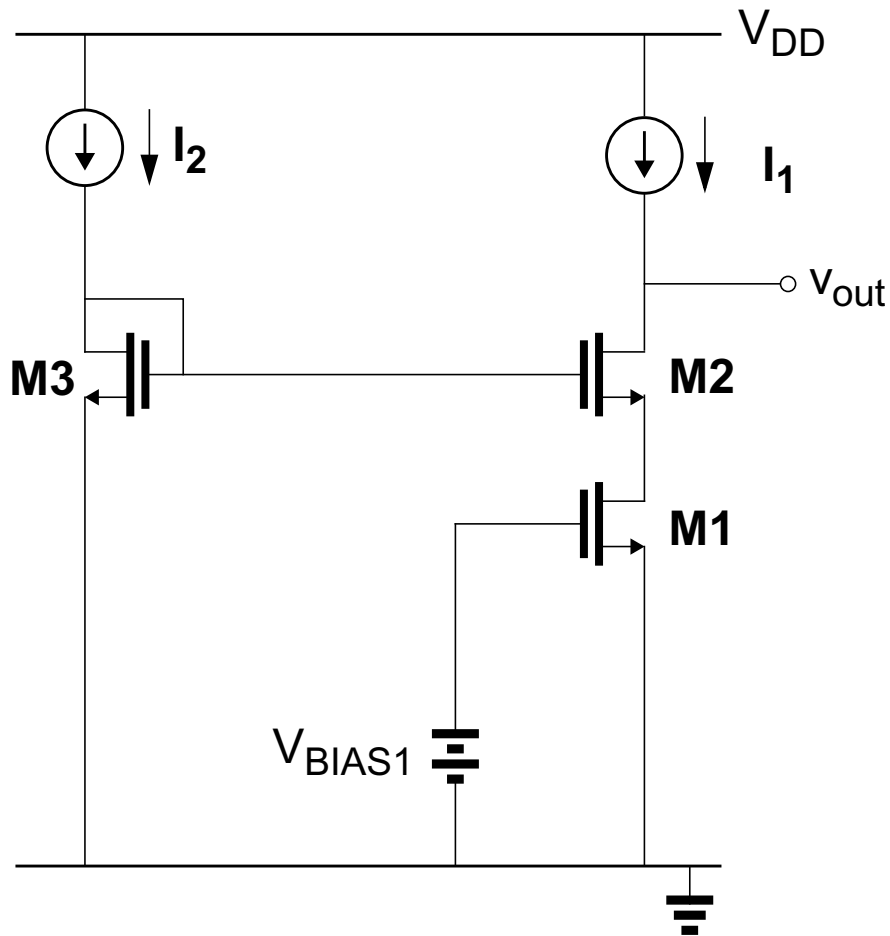
calculate the minimum value of the voltage at the output node (i.e. at the drain of M2) for both M1 and M2 to be in saturation and the value of  $V_{BIAS2}$  necessary to achieve this.

Neglect  $\lambda$  for this calculation.

- (ii) Repeat the calculations if the aspect ratio of M2 is four times that of M1

$$\text{i.e. } (W/L)_{M2} = 4 * (W/L)_{M1}$$

### Problem P.56: DC Biasing (3)



The body effect may be ignored.

- (i) The circuit shown is to be biased for optimal low-voltage operation.

If

$$V_{BIAS1} = 1.25V, V_T = 1V, I_1 = 100\mu A$$

$$(W/L)_{M1} = (W/L)_{M2} = (W/L)_{M3} = 16\mu m / 1\mu m$$

calculate the minimum value of the voltage at the output node (i.e. at the drain of M2) for both M1 and M2 to be in saturation and the value of  $I_2$  necessary to achieve this.

Neglect  $\lambda$  for this calculation.

- (i) For low power  $I_2$  is changed to  $40\mu A$ .

What value of  $(W/L)_{M3}$  is required to preserve the bias conditions of M1 and M2.

---

## Solution (Problem P.55) DC Biasing (2)

(i) For M1 to be in saturation then

$$V_{DS1} \geq V_{GS1} - V_t$$

$$(V_{DS1})_{min} = V_{GS1} - V_t = 1.2V - 0.8V = 0.4V$$

If M2 is in saturation its drain current is given by

$$I_{D2} = \frac{K'_n W}{2 L} (V_{GS2} - V_t)^2$$

Since M2 has same drain current, W/L and  $V_t$  as M1 it will also have the same  $V_{GS}$

$$(V_{DS2})_{min} = V_{GS2} - V_t = 0.4V$$

so minimum voltage at the output for both transistors to be in saturation is given by

$$V_{out} = (V_{DS1})_{min} + (V_{DS2})_{min} = 0.8V$$

The bias voltage  $V_{BIAS2}$  necessary to achieve this is given by

$$V_{BIAS2} = V_{GS2} + (V_{DS1})_{min} = 1.2V + 0.4V = 1.6V$$

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## Solution (Problem P.55) DC Biasing (2) cont.

(ii)

Since  $I_{D1} = I_{D2}$  then

$$\frac{K'_n}{2} \left( \frac{W}{L} \right) (V_{GS1} - V_t)^2 = \frac{K'_n}{2} 4 \left( \frac{W}{L} \right) (V_{GS2} - V_t)^2$$

$$V_{GS2} - V_t = \frac{V_{GS1} - V_t}{2} = 0.2V$$

$$V_{GS2} = 1V$$

$$(V_{DS2})_{min} = 0.2V$$

so minimum voltage at the output for both transistors to be in saturation is given by

$$V_{out} = (V_{DS1})_{min} + (V_{DS2})_{min} = 0.6V$$

The bias voltage  $V_{BIAS2}$  necessary to achieve this is given by

$$V_{BIAS2} = V_{GS2} + (V_{DS1})_{min} = 1.0V + 0.4V = 1.4V$$

## Solution (Problem P.56) DC Biasing (3)

(i) For M1 to be in saturation then

$$V_{DS1} \geq V_{GS1} - V_t$$

$$(V_{DS1})_{min} = V_{GS1} - V_t = 1.25V - 1V = 0.25V$$

If M2 is in saturation its drain current is given by

$$I_{D2} = \frac{K'_n W}{2L} (V_{GS2} - V_t)^2$$

Since M2 has same drain current, W/L and  $V_t$  as M1 it will also have the same  $V_{GS}$

$$(V_{DS2})_{min} = V_{GS2} - V_t = 0.25V$$

so minimum voltage at the output for both transistors to be in saturation is given by

$$V_{out} = (V_{DS1})_{min} + (V_{DS2})_{min} = 0.5V$$

The bias voltage  $V_{GS3}$  necessary to achieve this is given by

$$V_{GS3} = V_{GS2} + (V_{DS1})_{min} = 1.25V + 0.25V = 1.5V$$

$$I_{D1} = \frac{K'_n \left(\frac{W}{L}\right)}{2} (V_{GS1} - V_t)^2$$

$$I_{D3} = \frac{K'_n \left(\frac{W}{L}\right)}{2} (V_{GS3} - V_t)^2$$

$$\frac{I_{D1}}{I_{D3}} = \frac{(V_{GS1} - V_t)^2}{(V_{GS3} - V_t)^2}$$

$$I_{D3} = I_{D1} \frac{(V_{GS3} - V_t)^2}{(V_{GS1} - V_t)^2} = 100\mu A \frac{(0.5)^2}{(0.25)^2} = 400\mu A$$



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## Solution (Problem P.56) DC Biasing (3) cont.

(ii)

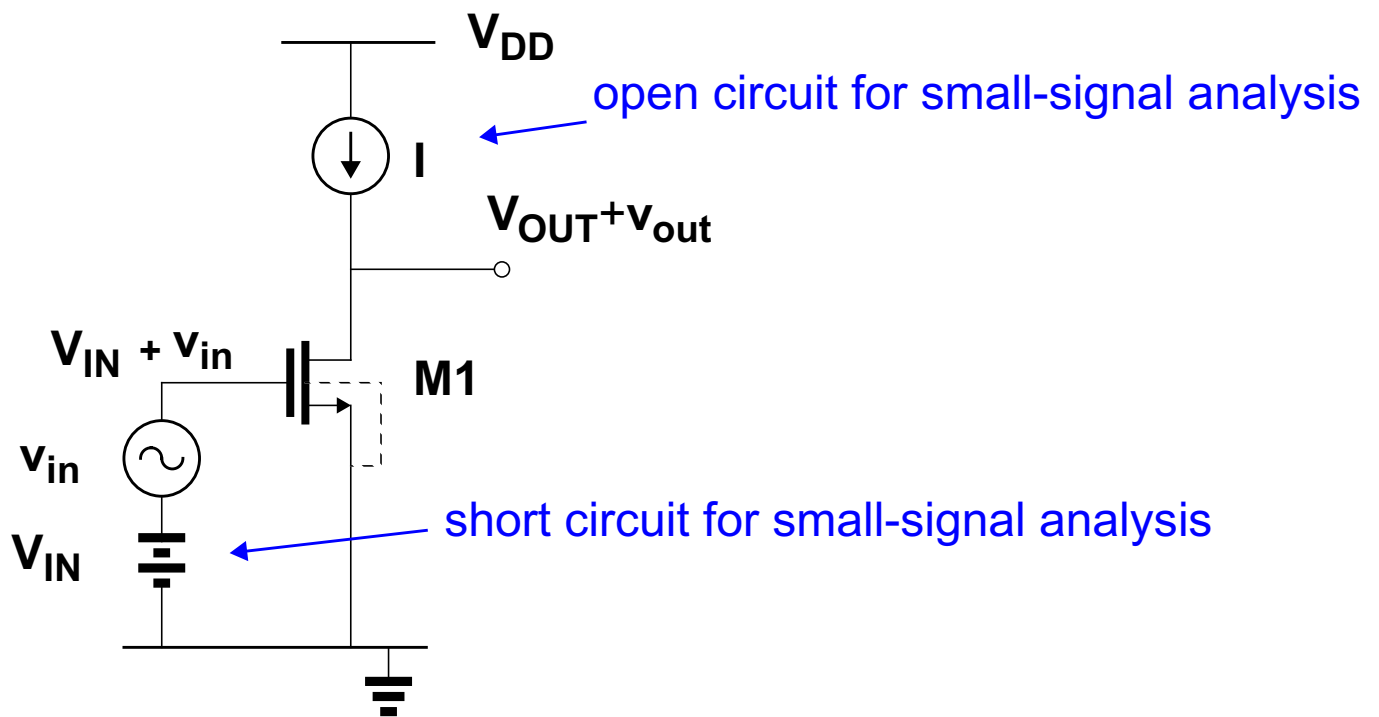
Need same  $V_{GS3} - V_t$

$$I_{D3} = \frac{K'_n}{2} \left( \frac{W}{L} \right)_3 (V_{GS3} - V_t)^2$$

If  $I_{D3}$  is reduced by a factor 10, then  $W/L$  also needs to be reduced by ten

$$\left( \frac{W}{L} \right)_{M3} = 1.6$$

## Problem P.72: Small-signal model



- (i) Draw the small-signal equivalent circuit
- (ii) What is the small-signal gain in terms of the small-signal parameters of M1
- (iii) Explain the result in terms of the large-signal behavior assuming M1 is in saturation
- (iv) What is the small signal gain if  $I=100\mu\text{A}$ ,  $\lambda=0.1$ ,  $V_{GS}-V_t=200\text{mV}$

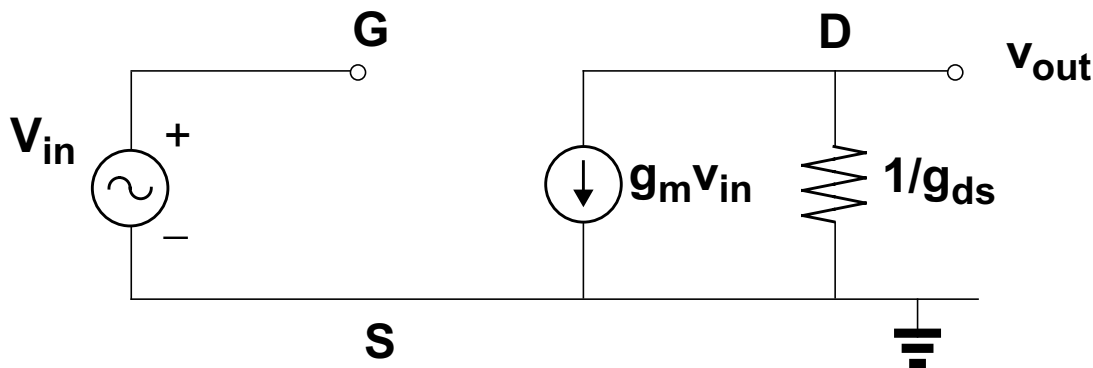
## Solution Problem P.72: Small-signal model.

Body and source tied together

$$\Rightarrow v_{bs} = 0$$

$\Rightarrow$  can ignore  $g_{mb}$

(i) Equivalent small-signal circuit



(ii) Small-signal voltage gain

Use KCL at output node

$$g_m v_{in} + v_{out} g_{ds} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_m}{g_{ds}}$$

(iii) In terms of small-signal parameters

$$I_D = \frac{K'_n W}{2 L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$

Small increase in  $V_{GS}$

$I_D$  is fixed by the ideal DC current source

$\Rightarrow V_{DS}$  must decrease to restore equilibrium

Also:  $V_{DS}$  must decrease much more than the increase in  $V_{GS}$

$\Rightarrow$  Gain

Q. What happens if current source is not ideal?

---

(iv) What is the small signal gain if  $I=100\mu A$ ,  $\lambda=0.1$ ,  $V_{GS}-V_t=200mV$

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2 \times 100\mu A}{200mV} = 1mA/V$$

$$g_{ds} = \lambda I_D = 0.1V^{-1} 100\mu A = 10\mu A/V$$

$$\left| \frac{v_{out}}{v_{in}} \right| = \frac{1000\mu A/V}{10\mu A/V} = 100$$

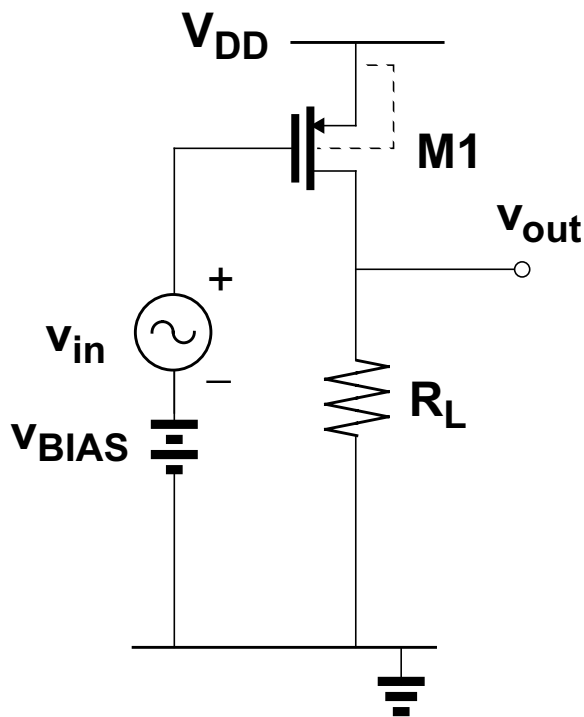
Note: gain usually expressed in dB

$$A = 20\log \left| \frac{v_{out}}{v_{in}} \right| = 40dB$$

Note:

$$\left. \begin{array}{l} g_m = \frac{2I_D}{V_{GS} - V_t} \\ g_{ds} = \lambda I_D \end{array} \right\} \frac{g_m}{g_{ds}} = \frac{2}{\lambda(V_{GS} - V_t)} \gg 1 \Rightarrow g_m \gg g_{ds}$$

## Problem: PMOS common-source stage with resistive load



$$V_{BIAS}=3.5V, V_t=1V, \lambda=0.05V^{-1}, I_{D1}=100\mu A, V_{DD}=5V$$

- Draw the small signal model for the circuit shown.
- What is the low-frequency small signal voltage gain ( $v_{out}/v_{in}$ ) in terms of the small-signal parameters and  $R_L$ ?
- What is the value of  $g_{m1}$ ?  
What is the value of  $g_{ds1}$ ?
- What is the largest value of  $R$  such that M1 is operating in the saturated region?
- What value of  $R$  gives the largest small-signal gain?  
What is the largest small-signal gain?

*The ratio  $g_m/g_{ds}$  is the intrinsic gain of the transistor.*

*Actual gain of a stage will be lower due to non-ideal current source.*

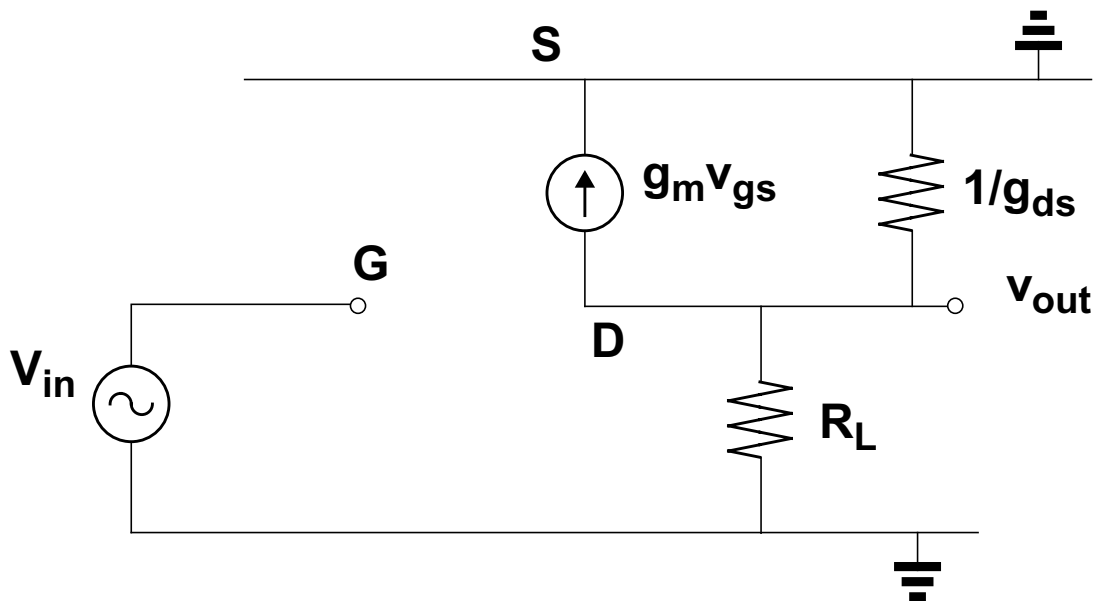
*Additional points:*

*Gain is inversely proportional to sqrt of drain current. Does this make sense?*

*What is (and what defines) DC voltage at output node?*

## Solution Prob. P83 (PMOS common-source with resistive load):

(i) Equivalent small-signal circuit



(ii) Small-signal voltage gain

Use KCL at output node

$$g_m v_{gs} + \frac{v_{out}}{R_L} + v_{out} g_{ds} = 0$$

$$g_m v_{in} = -v_{out} \left( \frac{1}{R_L} + g_{ds} \right)$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_m}{g_{ds} + \frac{1}{R_L}}$$

*N.B. Small-signal model for PMOS is the same as for NMOS in the sense that the direction of the current source  $g_m v_{gs}$  is from drain to source*

(iii) What is the value of  $g_{m1}$ ? What is the value of  $g_{ds1}$ ?

$$g_m = \frac{2I_D}{|V_{GS}| - |V_t|} = \frac{2 \times 100\mu A}{1.5V - 1V} = 400\mu A/V$$

$$g_{ds} = \lambda I_D = 0.05V^{-1} 100\mu A = 5\mu A/V$$

(iv) What is largest value of  $R_L$  such that M1 is in saturation?

Minimum  $|V_{DS}|$  for M1 in saturation =  $|V_{GS}| - |V_t| = 0.5V$

=> Maximum voltage at  $v_{out} = V_{DD} - 0.5V = 4.5V$

=> Maximum value of  $R_L$  given by

$$R_{L(max)} = \frac{v_{out(max)}}{I_D} = \frac{4.5V}{100\mu A} = 45k\Omega$$

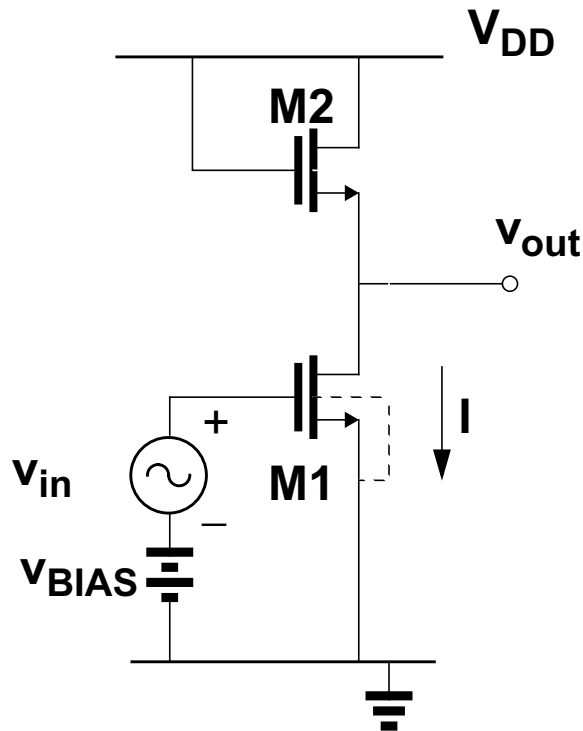
(v) What is the largest small-signal gain?

$$Gain_{max} = -\frac{g_m}{g_{ds} + \frac{1}{R_L}} = -\frac{400\mu A/V}{5\mu A/V + \frac{1}{45k\Omega}} = -14.7$$

In dB:

$$Gain_{max} = 20\log\left|\frac{v_{out}}{v_{in}}\right| = 23dB$$

## Problem P93: - Common source stage with NMOS Diode Load



Assume M1 is biased in saturation.

- (i) Draw the small signal model for the circuit shown.
- (ii) What is the low-frequency small signal voltage gain ( $v_{out}/v_{in}$ ) in terms of the small-signal parameters?

Assume that  $g_{m1} \gg g_{ds1}, g_{ds2}$  and that  $g_{m2} \gg g_{ds1}, g_{ds2}$

- (iii) Calculate the gain if

$$W1=25, L1=1$$

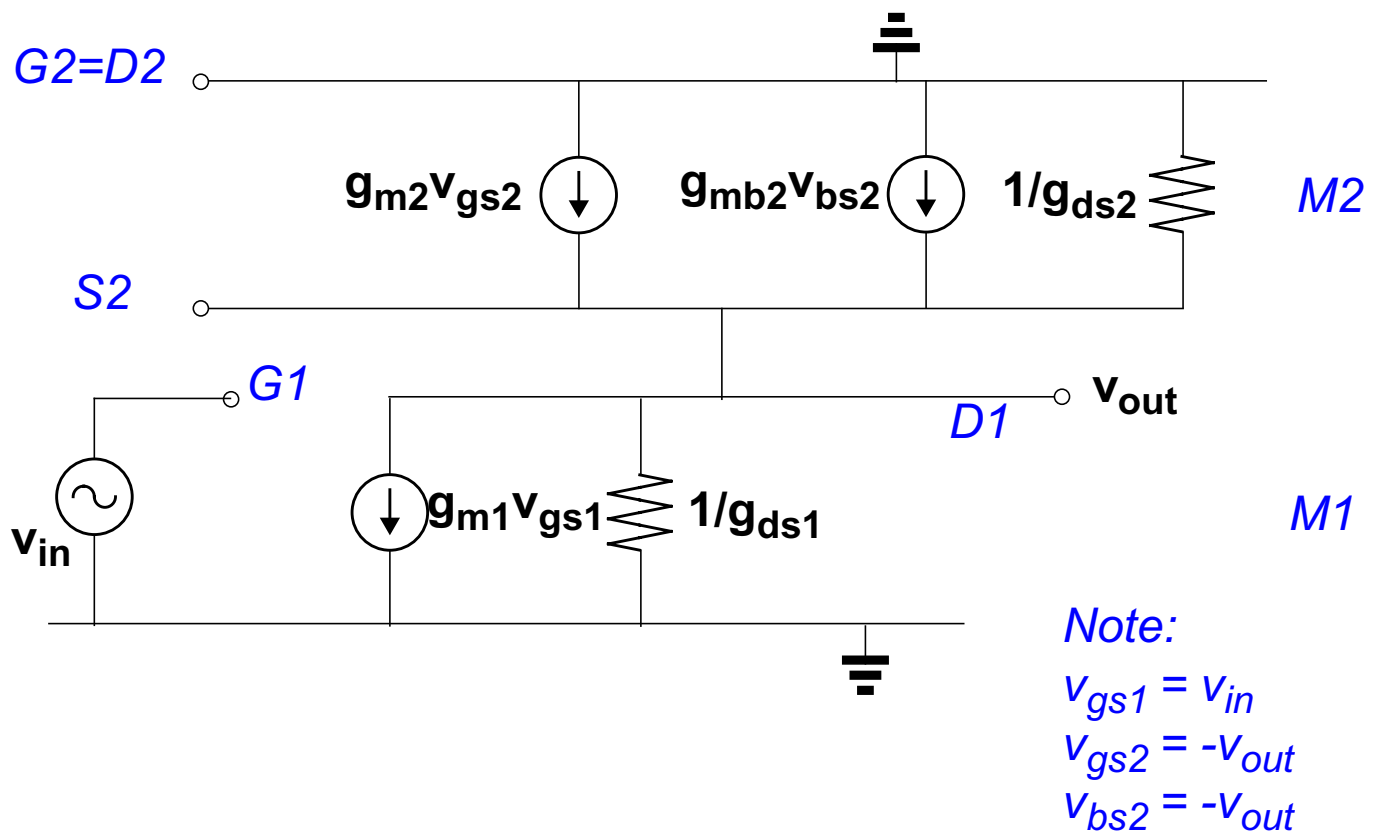
$$W2=1, L2=1$$

$$\eta=0.3$$



## Solution Prob. P93 (NMOS common-source stage with NMOS diode load):

(i) Equivalent small-signal circuit



(ii) Small-signal voltage gain

Use KCL at output node

$$g_{m1}v_{gs1} + v_{out}g_{ds1} - g_{m2}v_{gs2} - g_{mb2}v_{bs2} + v_{out}g_{ds2} = 0$$

$$g_{m1}v_{in} + v_{out}g_{ds1} + g_{m2}v_{out} + g_{mb2}v_{out} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{mb2} + g_{ds1} + g_{ds2}} \cong -\frac{g_{m1}}{g_{m2} + g_{mb2}}$$

*Alternatively recognise that current-sources  $g_{m2}v_{gs2}$  and  $g_{m2}v_{bs2}$  are equivalent to resistances  $1/g_{m2}$ ,  $1/g_{mb2}$  respectively.*

(iii) Calculate the gain if

$W_1=25, L_1=1$

$W_2=1, L_2=1$

$\eta=0.3$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{mb2}}$$

$$= -\frac{g_{m1}}{g_{m2}(1 + \eta)} \quad \text{since } g_{mb2} = \eta g_{m2}$$

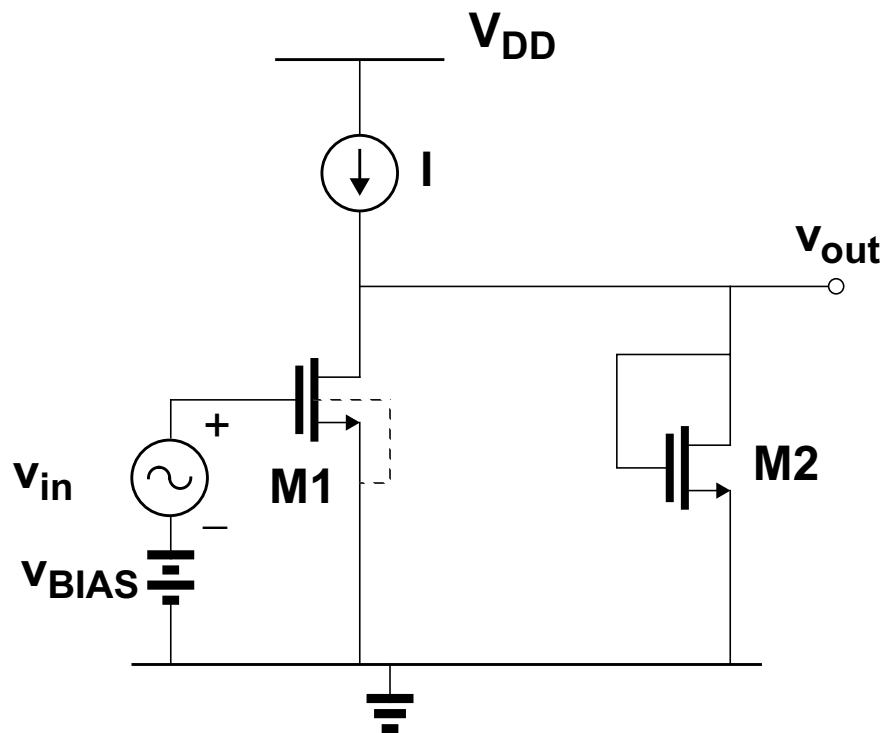
$$= -\sqrt{\frac{2K'_n \frac{W_1}{L_1} I_{D1}}{2K'_n \frac{W_2}{L_2} I_{D2}}} \cdot \frac{1}{1 + \eta}$$

$$= -\sqrt{\frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}}} \cdot \frac{1}{1 + \eta}$$

$$= -\sqrt{\frac{25}{1}} \cdot \frac{1}{1 + 0.3} = 3.8 \Leftrightarrow 11.7dB$$

*Note: Variation in gain over process is much less than for common-source NMOS with PMOS diode load.*

To eliminate the body effect on the load transistor, use a 'folded' load.

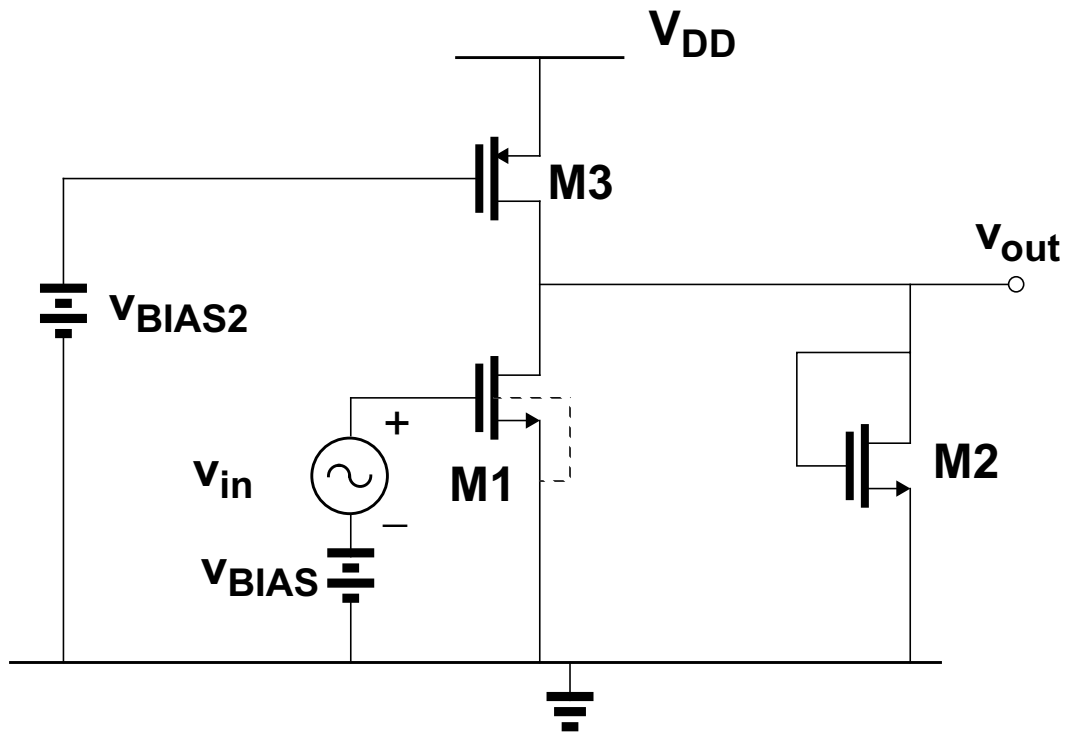


$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \cong -\frac{g_{m1}}{g_{m2}}$$

Looked at from another perspective:

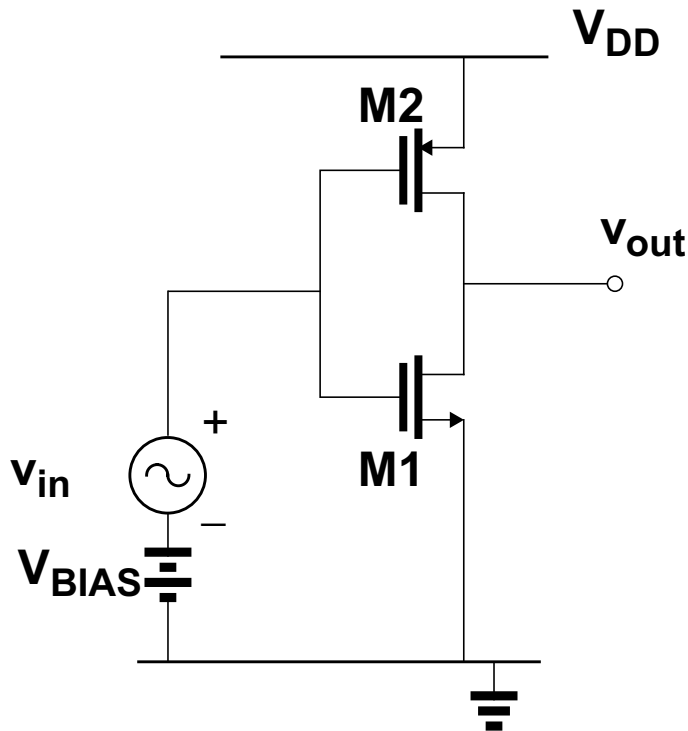
A change in input voltage causes a change in the drain current of M1. Because  $I$  is clamped this produces an equal change in M2, which is converted to a voltage by the impedance of M2

## Practical implementation of the 'folded' load - PMOS supplies current



$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2} + g_{ds3}} \cong -\frac{g_{m1}}{g_{m2}}$$

## Problem: CS stage (CMOS Inverter)



Assume M1 and M2 are biased in saturation.

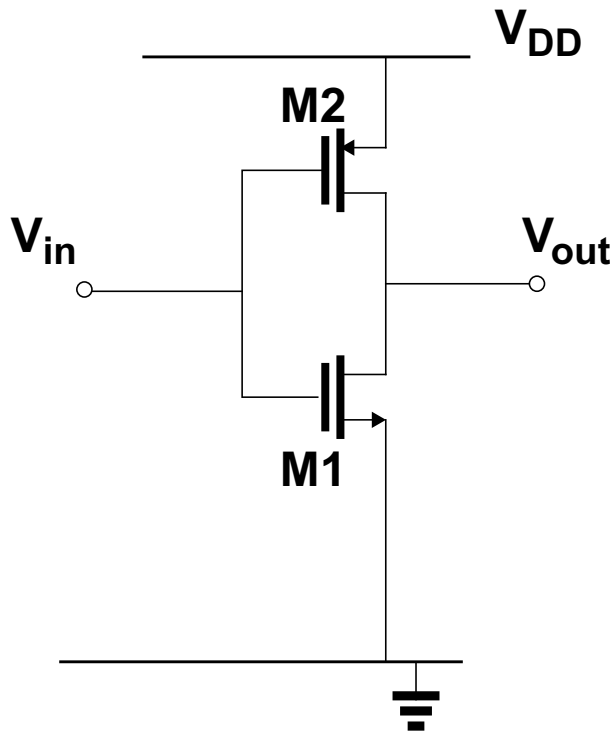
- (i) Draw the small signal model for the circuit shown.
- (ii) Derive an expression for the low-frequency small signal voltage gain ( $v_{out}/v_{in}$ ) in terms of the small-signal parameters?

Assume that  $g_{m1} \gg g_{ds1}, g_{ds2}$  and that  $g_{m2} \gg g_{ds1}, g_{ds2}$

- (iii) Calculate the gain if

$$\begin{aligned} V_{DD} &= 3, V_{BIAS} = 1.5, |V_t| = 1 \\ I_D &= 100 \mu A, \lambda_p = \lambda_n = 0.05 V^{-1} \\ W_1 &= 10, L_1 = 1 \\ W_2 &= 40, L_2 = 1 \end{aligned}$$

## Problem P104 CS stage (CMOS Inverter)



How does this stage work?

Assume both devices are in saturation, and so obey the equation

$$|I_D| = \frac{K'}{2} \frac{W}{L} (|V_{GS}| - |V_t|)^2 (1 + \lambda |V_{DS}|)$$

Small increase in  $V_{in} \Rightarrow V_{GS}$  M1 increases

$\Rightarrow$  M1 'wants' more drain current from M2

$\Rightarrow V_{out}$  goes down to pull more current from M2 (by increasing  $|V_{DS2}|$ )

At the same time  $|V_{GS}|$  M2 decreases

$\Rightarrow$  M2 'wants' less drain current from M1

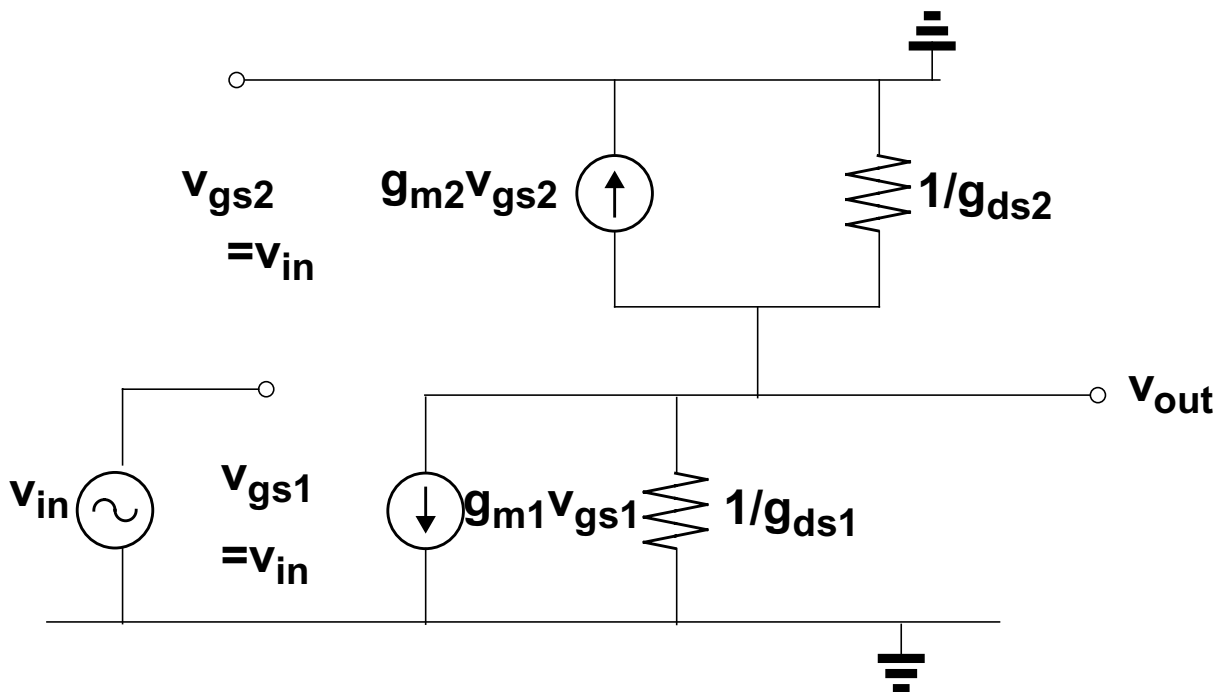
$\Rightarrow V_{out}$  goes down to cut off current from M1 (by decreasing  $|V_{DS1}|$ )

$V_{out}$  drops until equilibrium is restored.

Note: gain is higher than circuit on P.98 because M2 contributes.

## Solution

(i) Draw the small signal model for the circuit shown.



(ii) Derive an expression for the low-frequency small signal voltage gain ( $v_{out}/v_{in}$ ) in terms of the small-signal parameters?

Sum current at output node

$$g_{m1}v_{gs1} + g_{m2}v_{gs2} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$g_{m1}v_{in} + g_{m2}v_{in} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}}$$

(iii) Calculate the gain if

$$\begin{aligned}V_{DD} &= 3, V_{BIAS} = 1.5, |V_t| = 1 \\I_D &= 100\mu A, \lambda_p = \lambda_n = 0.05V^{-1} \\W_1 &= 10, L_1 = 1 \\W_2 &= 40, L_2 = 1\end{aligned}$$

$$I_{D1} = I_{D2} = 100\mu A,$$

$$V_{GS1} - V_{t1} = |V_{GS2}| - |V_{t2}| = 0.5V$$

$$g_{m1} = g_{m2} = \frac{2I_D}{V_{GS} - V_t} = \frac{2 \times 100\mu A}{0.5V} = 400\mu A/V$$

$$\lambda_1 = \lambda_2 = 0.05V^{-1}$$

$$g_{ds1} = g_{ds2} = \lambda I_D = 0.05V^{-1} \times 100\mu A = 5\mu A/V$$

$$Gain = \frac{v_{out}}{v_{in}} = -\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}} = -\frac{800}{10} = 80$$

$$dBGain = 20\log\left|\frac{v_{out}}{v_{in}}\right| = 38dB$$



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## y-parameters summary

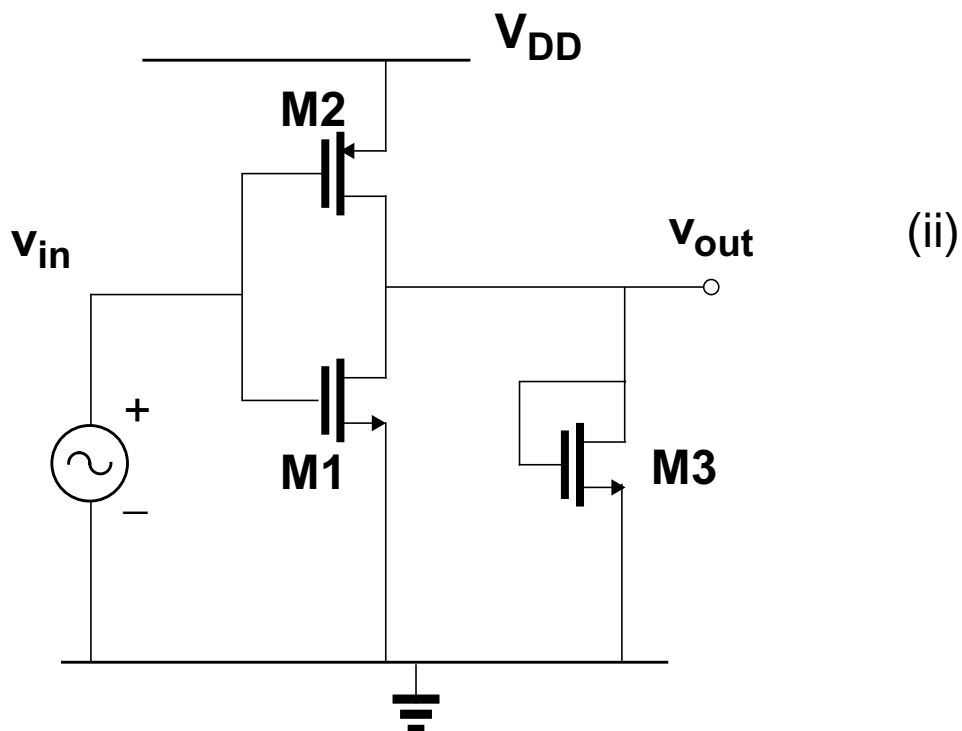
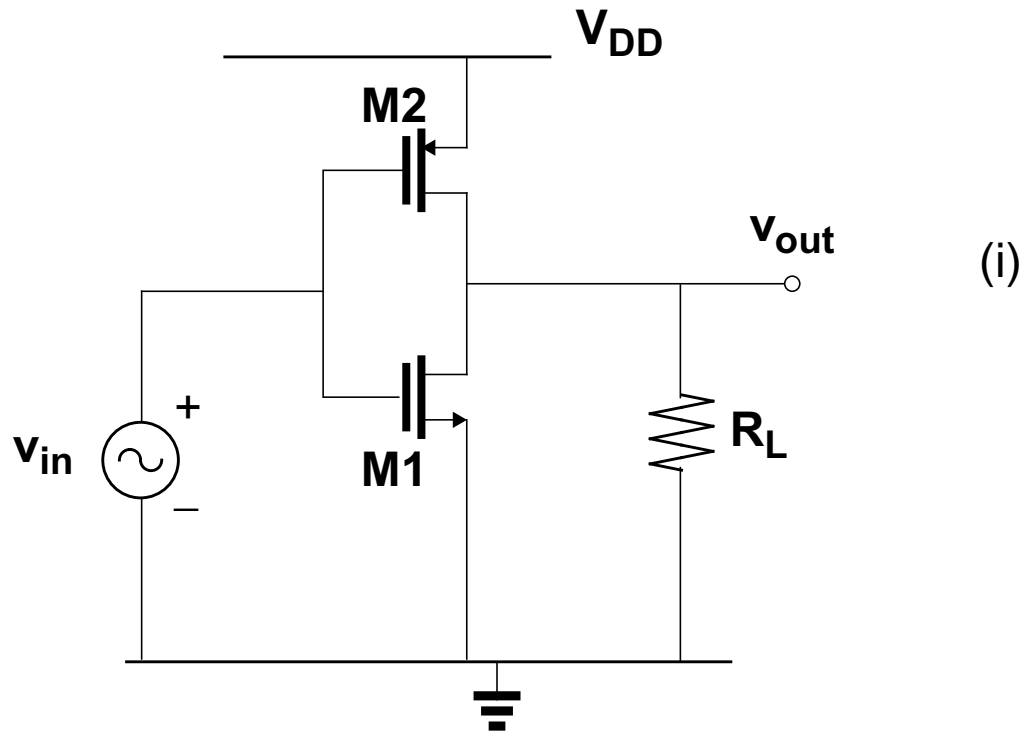
Razavi Chap. 3

**Lemma:** *In a linear circuit, the voltage gain is equal to  $-G_m R_{out}$ , where  $G_m$  denotes the transconductance of the circuit when the output is shorted to ground, and  $R_{out}$  represents the output resistance of the circuit when the input voltage is set to zero.*

In the notes we more often use  $G_{out}$ . When a load with conductance  $G_L$  is added we simply add its conductance to  $G_{out}$ , so the voltage gain is equal to  $-G_m/(G_{out}+G_L)$  or **transconductance of the circuit divided by the total conductance at the output node**.

This is a very useful concept in circuits where it is easy to determine  $G_m$  and  $G_{out}$  by inspection e.g. common-source stage, cascode stage, differential pair.

## Problem P109: CMOS Inverter & y-parameters



Use y-parameters to calculate the small-signal gain of a CMOS inverter (both devices are in saturation) with

- (i) resistive load
- (ii) nmos diode load

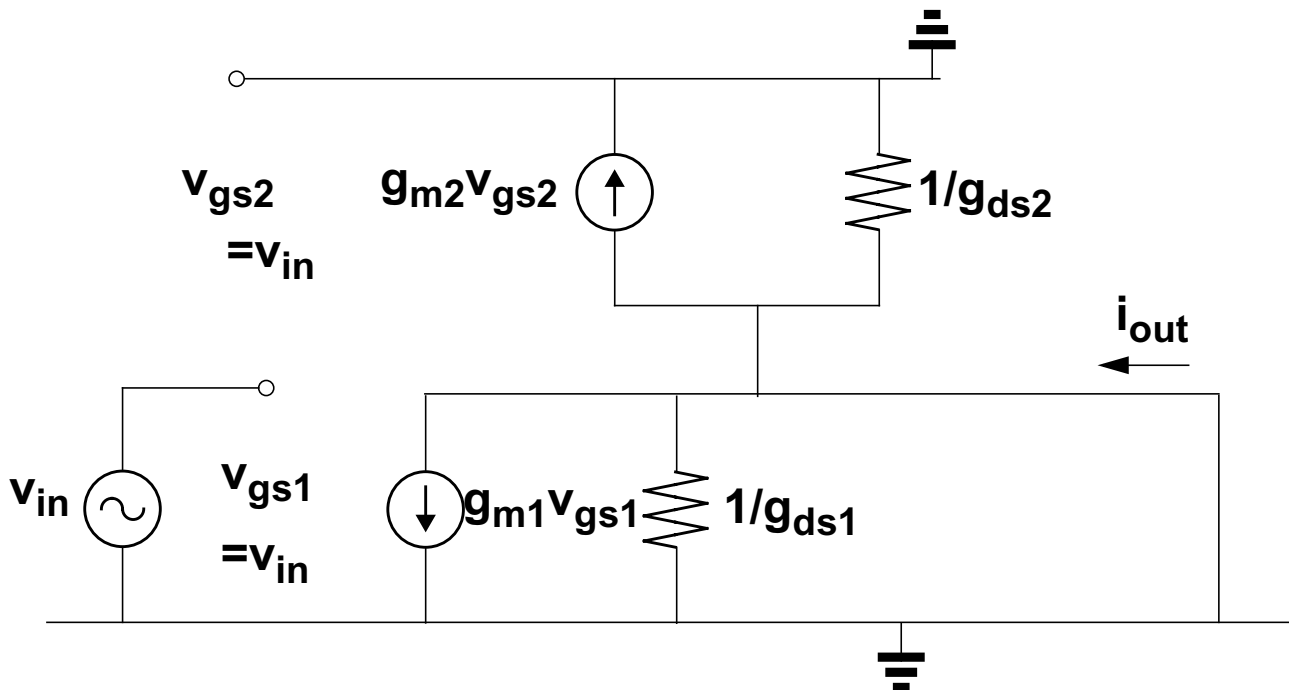
## Problem P. 109 CMOS Inverter & y-parameters.

First derive expressions for  $G_m$  and  $R_{out}/G_{out}$ .

**$G_m$**

For  $G_m$ , small-signal circuit as previously, with output shorted to ground.

Calculate  $i_{out}/v_{in}$ .



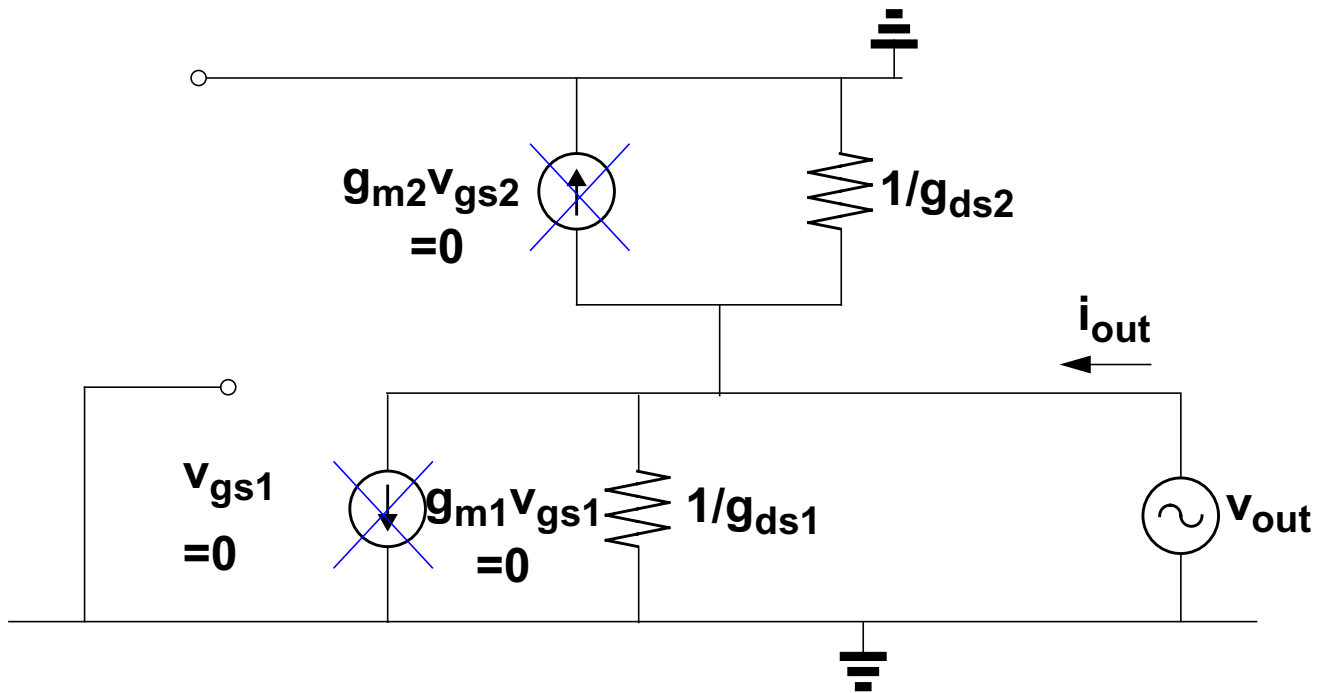
$$i_{out} = g_{m1}v_{in} + g_{m2}v_{in}$$

$$G_m \equiv \frac{i_{out}}{v_{in}} = g_{m1} + g_{m2}$$

## **G<sub>out</sub>**

For G<sub>out</sub>, short input to ground.

Apply voltage at output and calculate i<sub>out</sub>/v<sub>in</sub>



$$i_{out} = v_{out}g_{ds1} + v_{out}g_{ds2}$$

$$G_{out} \equiv \frac{i_{out}}{v_{out}} = g_{ds1} + g_{ds2}$$

$$Gain_{unloaded} \equiv \frac{G_m}{G_{out}} = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}}$$

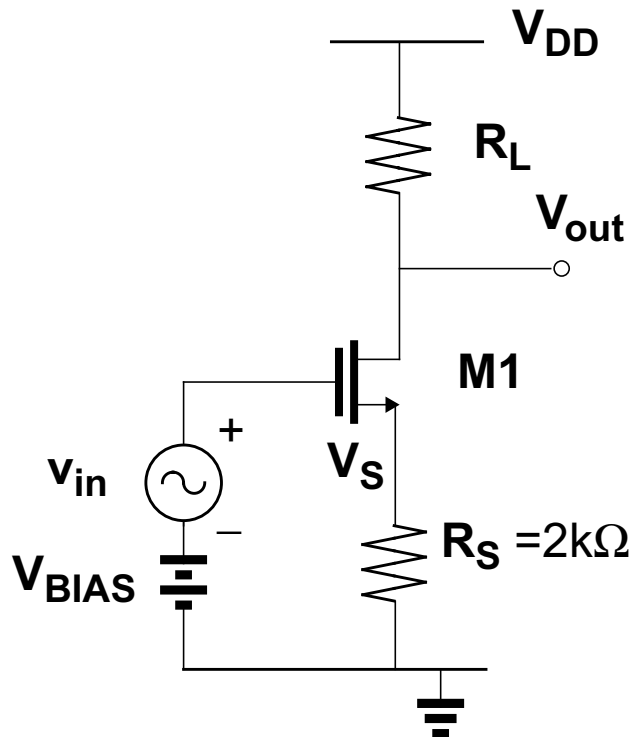
(i) With R<sub>L</sub> connected:

$$Gain_{R_L} \equiv \frac{G_m}{G_{out} + G_L} = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2} + \frac{1}{R_L}}$$

(ii) With nmos diode connected:

$$Gain_{nd} \equiv \frac{G_m}{G_{out} + G_L} = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2} + g_{m3}}$$

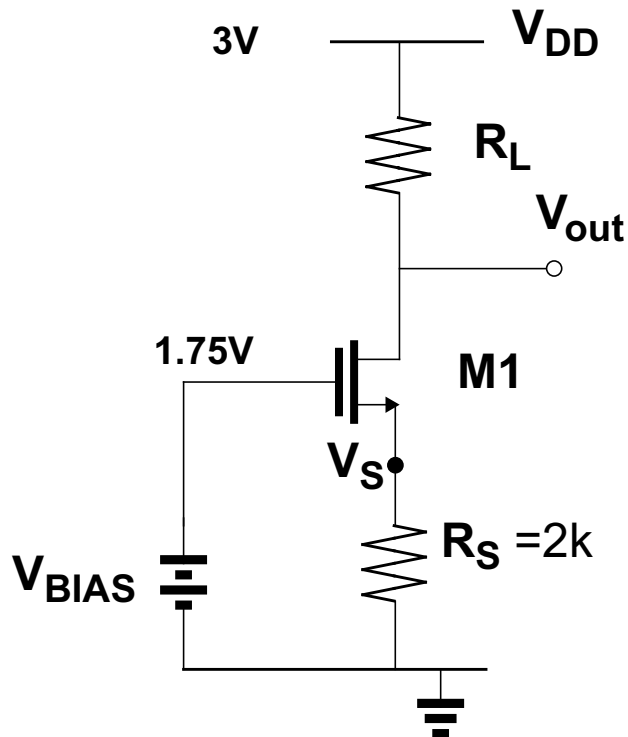
## Problem: CS stage with resistive degeneration



Assume M1 is in saturation, ignore the body effect, take  $g_m \gg g_{ds}$   
Assume the stage is biased such that  $g_m R_S = 2$   
 $V_{\text{DD}} = 3\text{V}$ ,  $V_{\text{BIAS}} = 1.75\text{V}$ ,  $V_t = 1\text{V}$ .

- (i) Calculate the value of the stage transconductance  $G_m$
- (ii) What is the largest value of  $R_L$  such that M1 is in saturation  
(Take  $\lambda = 0$  for this calculation)
- (iii) What is the value of the small-signal gain for this  $R_L$ ?

## Solution Problem P120 Resistive degeneration



(i) 
$$G_m = \frac{g_m}{1 + g_m R_s}$$

$$g_m = \frac{2I_D}{V_{GS} - V_t}$$

Need to find values for  $I_D$ ,  $V_{GS} - V_t$

$$g_m R_s = \frac{2I_D R_s}{V_{GS} - V_t} = 2 \Rightarrow V_{GS} - V_t = I_D R_s$$

i.e. overdrive voltage of M1 = voltage across  $R_s$

$$V_{BIAS} = V_t + (V_{GS} - V_t) + I_D R_s$$

$$V_{BIAS} - V_t = 2(V_{GS} - V_t)$$

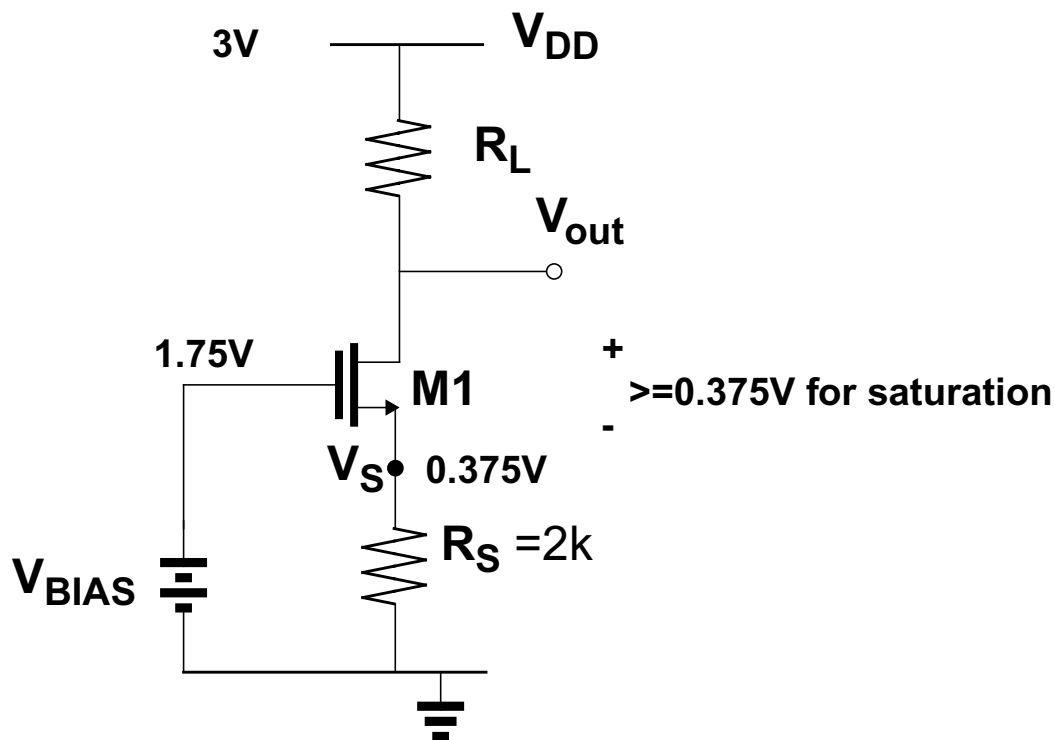
$$V_{GS} - V_t = \frac{1.75 - 1}{2} = 0.375 V$$

$$I_D R_s = 0.375 V \Rightarrow I_D = \frac{0.375 V}{2 k\Omega} = 187.5 \mu A$$

---

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2 \times 187.5 \mu A}{0.375 V} = 1 mA/V$$

$$G_m = \frac{g_m}{1 + g_m R_s} = \frac{1 mA/V}{1 + 2} = 333 \mu A/V$$



(ii) For M1 to be in saturation

$$V_{DS} \geq V_{GS} - V_t \Rightarrow V_{DS} \geq 0.375V \Rightarrow V_{out} \geq 0.75V$$

$$V_{DD} - I_D R_L \geq 0.75V$$

$$R_L \leq \frac{3 - 0.75V}{187.5\mu A}$$

$$R_L \leq 12k\Omega \quad \Rightarrow \quad R_{Lmax} = 12k\Omega$$

(iii)

$$\begin{aligned} Gain_{max} &= -G_m R_L = -\frac{g_m R_L}{1 + g_m R_S} \\ &= -\frac{1mA/V \times 12k\Omega}{1 + 2} = -4 \end{aligned}$$

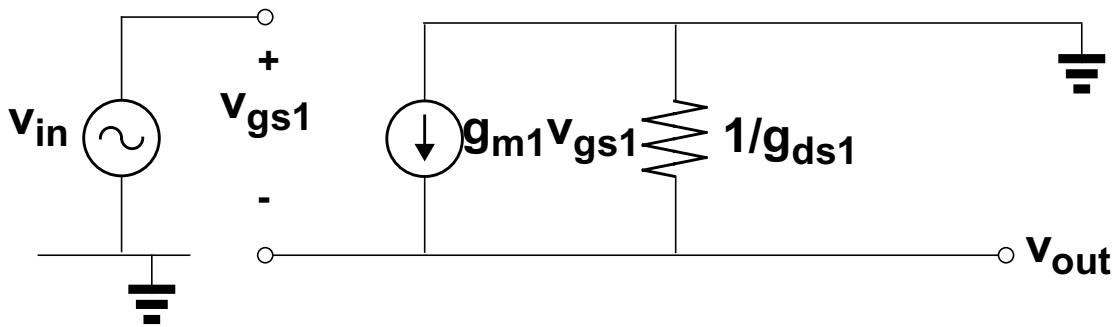
In dB

$$Gain = 12dB$$



## Solution Problem P. 130: Source Follower

(i) Draw the small-signal model for the circuit shown in Fig.1.



(ii) What is the small-signal low-frequency gain of the circuit in terms of  $g_m$  and  $g_{ds}$ ?

Sum current at output node

$$g_{m1}v_{gs1} - v_{out}g_{ds1} = 0$$

$$g_{m1}(v_{in} - v_{out}) = v_{out}g_{ds1}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1}} \approx 1$$

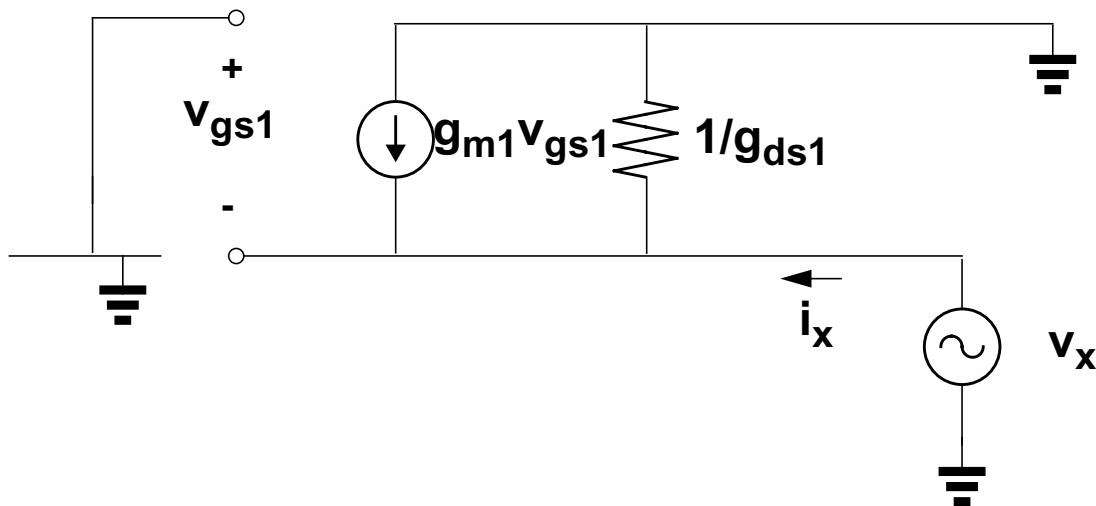
(iii) If  $I_B = 200\mu A$ ,  $V_{GS} = 1.5V$ ,  $V_t = 1V$ , calculate the small-signal low-frequency gain. Take  $\lambda = 0.02V^{-1}$ .

$$g_{m1} = \frac{2I_B}{V_{GS} - V_t} = \frac{2 \times 200\mu A}{0.5V} = 800\mu A/V$$

$$g_{ds1} = \lambda I_B = 0.02V^{-1} \times 200\mu A = 4\mu A/V$$

$$Gain = \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1}} = \frac{800}{800 + 4} \approx 1$$

(iv) What is the conductance/resistance at the output node?  
 To measure the small-signal output resistance:  
 Short the input.  
 Apply a test voltage at the output.  
 Measure the current through the test voltage.  
 Calculate ratio of voltage to current



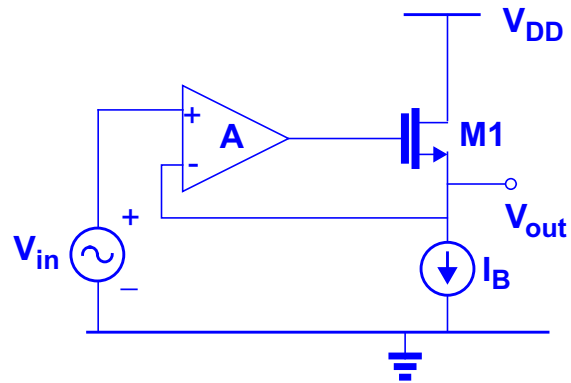
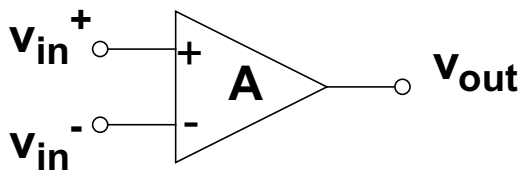
$$i_x = v_x g_{ds1} - g_{m1} v_{gs1}$$

$$= v_x g_{ds1} + g_{m1} v_x$$

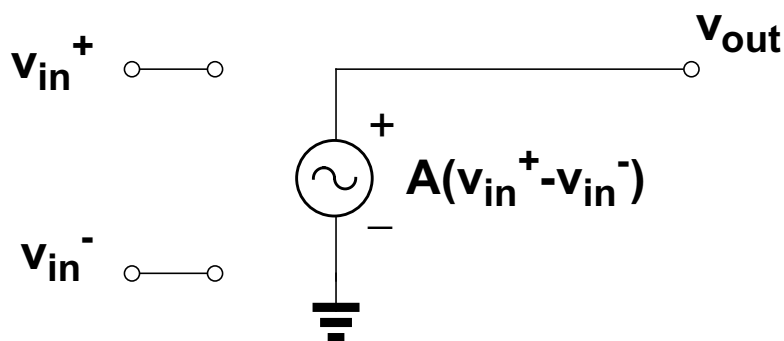
$$r_{out} = \frac{v_x}{i_x} = \frac{1}{g_{m1} + g_{ds1}} \approx \frac{1}{g_{m1}}$$

(v) In Fig.2 an ideal amplifier has been added to reduce the output resistance. Draw the small-signal model.

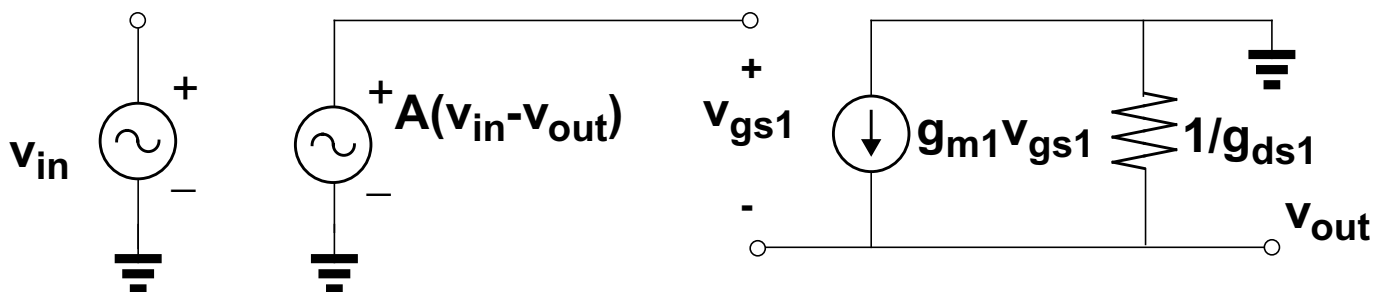
### Differential-to-single-ended opamp



### Small-signal model of opamp:



### Small-signal model of Fig. 2:



### Gain:

$$g_{m1}v_{gs1} - v_{out}g_{ds1} = 0$$

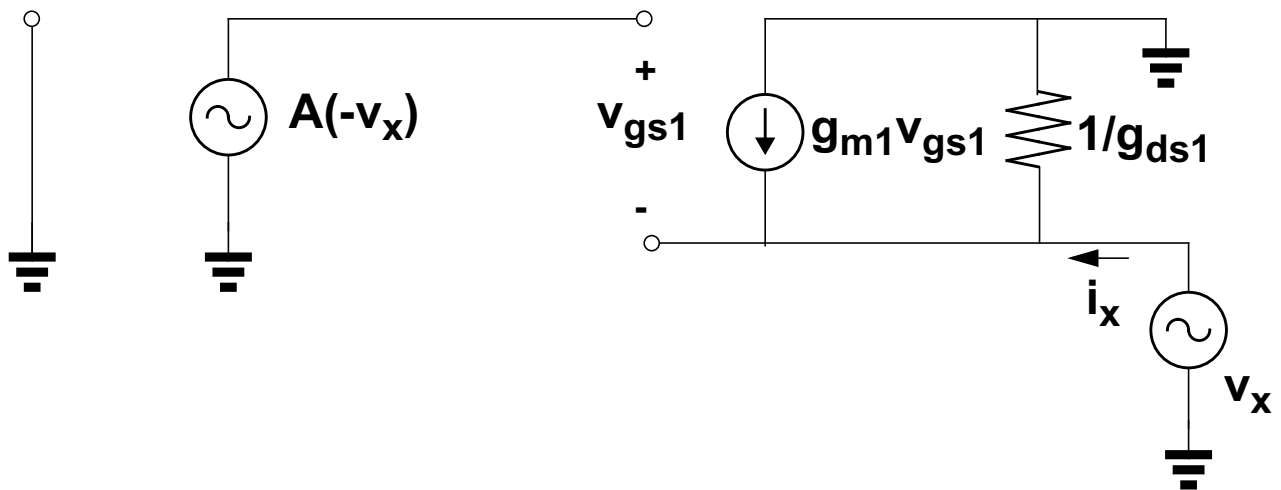
$$g_{m1}(A(v_{in} - v_{out}) - v_{out}) - v_{out}g_{ds1} = 0$$

$$g_{m1}Av_{in} = g_{m1}Av_{out} + g_{m1}v_{out} + v_{out}g_{ds1}$$

$$\frac{v_{out}}{v_{in}} = \frac{Ag_{m1}}{Ag_{m1} + g_{m1} + g_{ds1}} \approx 1$$

(vi) What is the impedance at the output node in terms of  $A$ ,  $g_m$  and  $g_{ds}$ ?  
 (To simplify the analysis assume  $g_m \gg g_{ds}$ )

**Short input, apply test voltage at output and measure current into circuit**

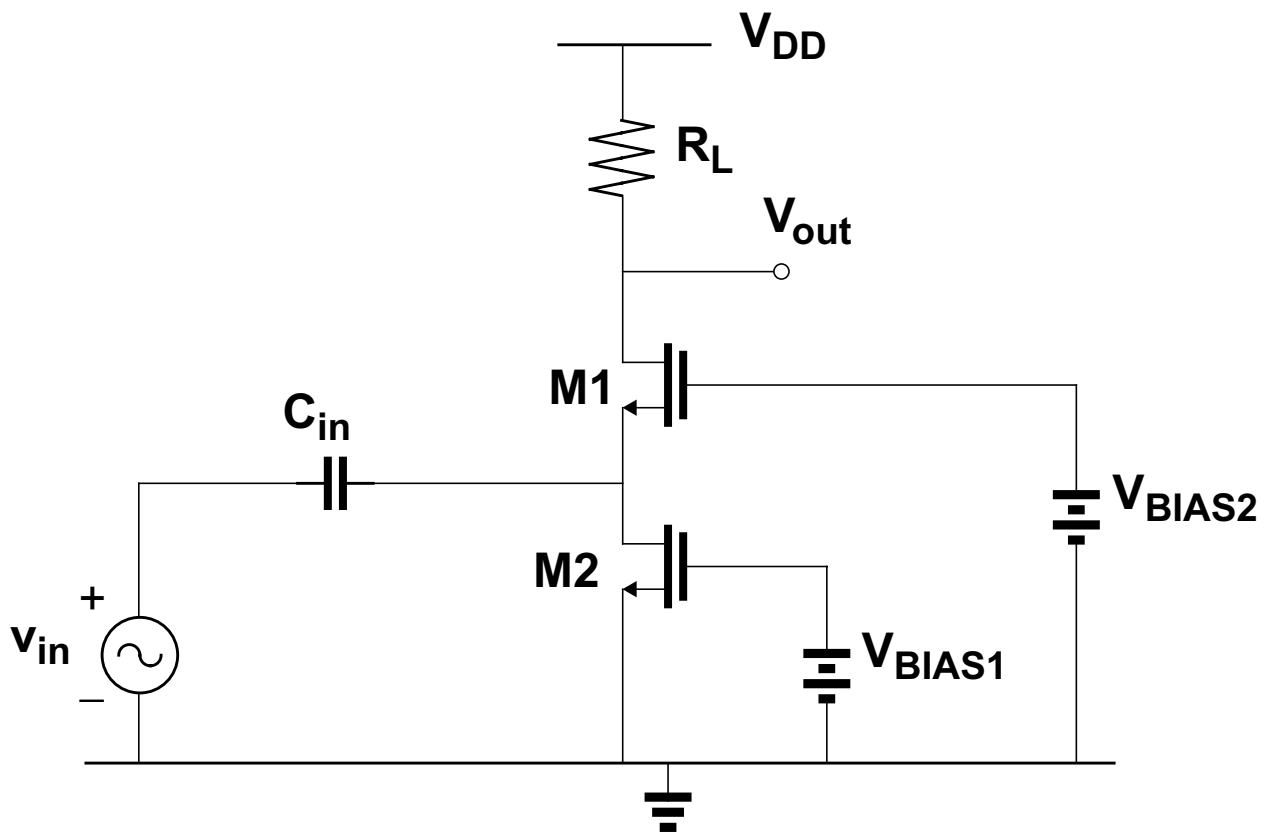


$$i_x = v_x g_{ds1} - g_{m1} v_{gs1}$$

$$= v_x g_{ds1} - g_{m1} (-A v_x - v_x)$$

$$r_{out} = \frac{v_x}{i_x} = \frac{1}{A g_{m1} + g_{m1} + g_{ds1}} \approx \frac{1}{(A + 1) g_{m1}}$$

## Problem: Common-gate stage



$V_{DD}=3.3\text{V}$ ,  $V_t=0.6\text{V}$ ,  $I_{D1}=1\text{mA}$

It is required for an input stage to a system to have an input resistance of  $200\Omega \pm 10\%$  and a gain of about 20dB.

Assume the input signal couples through  $C_{in}$  without loss.

- (i) Suggest values for  $g_{m1}$  and  $R_L$  to meet this specification.
- (ii) Assuming M1 and M2 have the same  $W/L$  and M2 is just in saturation, what is the range of allowed voltages for  $V_{BIAS2}$ ?

---

## Solution Common-gate stage problem

(i)

Assume body effect can be ignored.

From analysis in notes:

$$R_{in} = \frac{v_x}{i_x} \approx \frac{1}{g_m} + \frac{R_L}{\frac{g_m}{g_{ds}}}$$

Assume  $1/g_m$  term dominates

$$R_{in} = \frac{v_x}{i_x} \approx \frac{1}{g_m} \Rightarrow g_m = \frac{1}{R_{in}} = \frac{1}{200\Omega}$$

$$Gain \approx g_m R_L = 10 \Rightarrow R_L = \frac{10}{g_m} = 2k\Omega$$

Note that this implies that  $g_m/g_{ds} > 100$  in order to meet the spec of  $R_{in}=200\Omega \pm 10\%$ .

May want to increase  $g_m$ , reduce  $R_L$  to meet spec more comfortably, target  $R_{in} = 200\Omega$ .

=> design iteration

## Solution

(ii)

What  $V_{GS}-V_t$  is required for each transistor?

For M1:

$$g_m = \frac{2I_D}{V_{GS} - V_t} \Rightarrow V_{GS} - V_t = \frac{2I_D}{g_m} = 2 \times 1mA \times 200\Omega = 400mV$$

M1 and M2 have same  $V_{GS}-V_t$

For M2 to be in saturation

$$V_{BIAS2} \geq V_{GS1} + (V_{GS2} - V_t)$$

$$V_{BIAS2} \geq V_t + (V_{GS1} - V_t) + (V_{GS2} - V_t)$$

$$V_{BIAS2} \geq 0.6V + 0.4V + 0.4V = 1.4V$$

For M1 to be in saturation

$$V_{out} \geq V_{BIAS2} - V_t \Rightarrow V_{BIAS2} \leq V_{out} + V_t$$

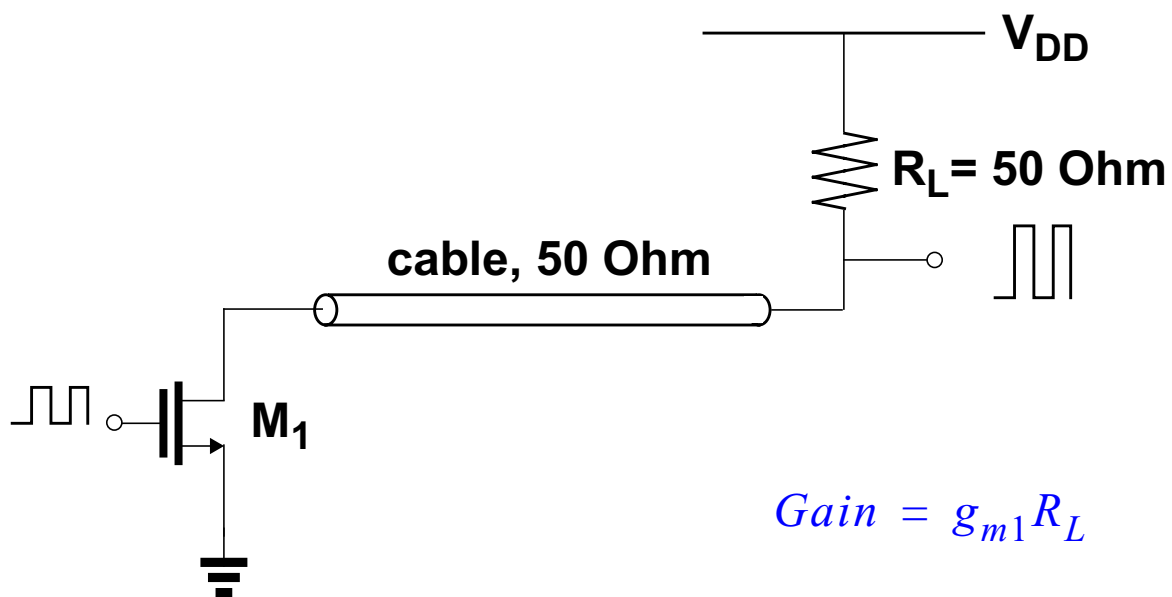
$$V_{out} = V_{DD} - I_D R_L = 3.3 - 1mA \times 2k\Omega = 1.3V$$

$$V_{BIAS2} \leq 1.3V + 0.6V = 1.9V$$

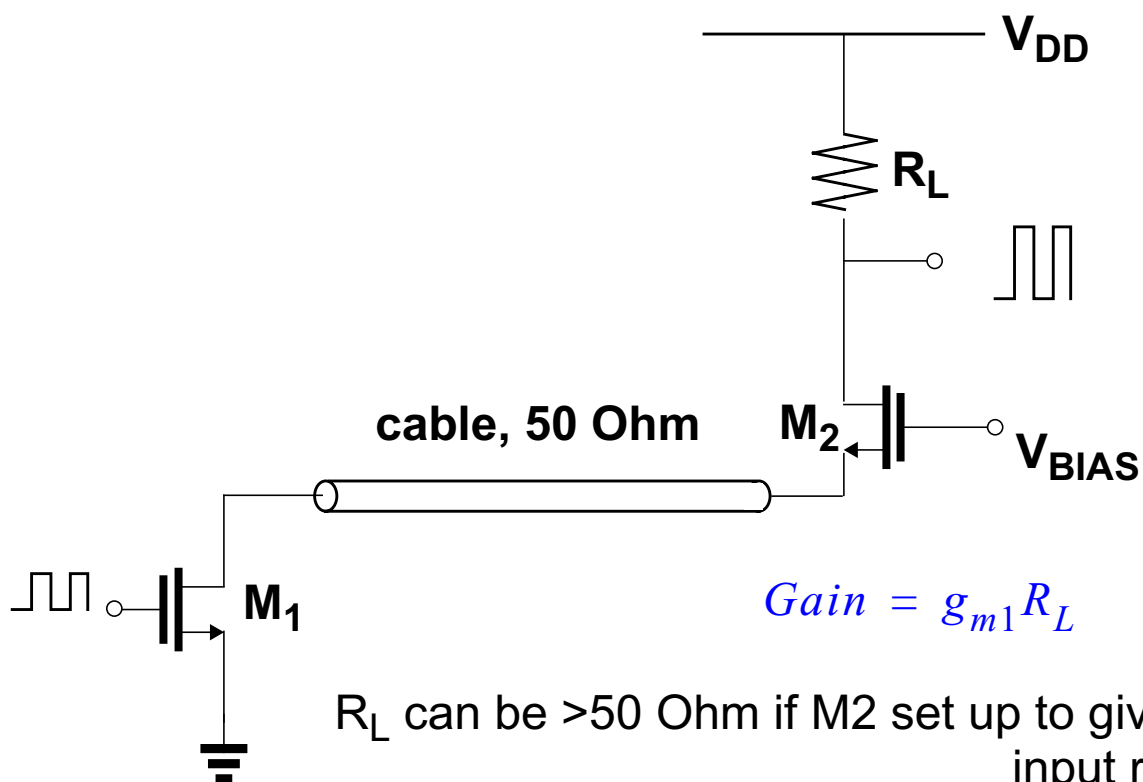
$$1.4V \leq V_{BIAS2} \leq 1.9V$$

So the optimum voltage for  $V_{BIAS2}$  is around 1.65V.  
A small signal of up to 250mV could then be handled

## Example from Ravavi



$R_L$  must be  $\sim 50 \text{ Ohm}$  to prevent reflections

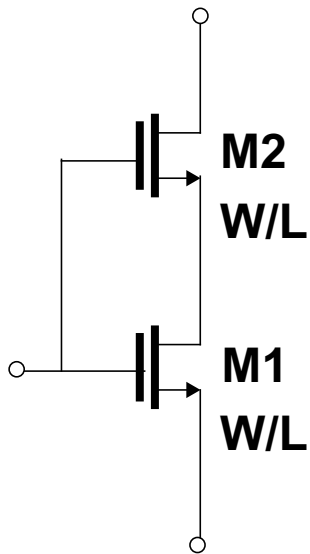


$R_L$  can be  $> 50 \text{ Ohm}$  if  $M_2$  set up to give 50 Ohm input resistance

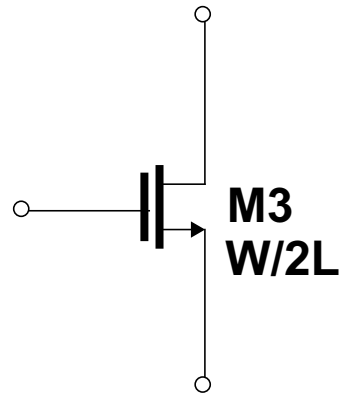


## Problem P.140 : Cascode v. common source

Redraw



as



(i) Compare output resistances

Cascode:

$$r_{outcas} = \frac{g_{m2}}{g_{ds2}} \cdot \frac{1}{g_{ds1}}$$

Common source:  $r_{outcs} = \frac{1}{g_{ds3}}$

Given that  $g_{ds} = \lambda I_D$  and  $\lambda \propto \frac{1}{L}$

then  $g_{ds3} = \frac{g_{ds1}}{2}$

and  $r_{outcs} = \frac{2}{g_{ds1}}$

=> Common source:

$$r_{outcs} = 2 \frac{1}{g_{ds1}}$$

Since  $\frac{g_{m2}}{g_{ds2}} \gg 2$  the  $r_{out}$  of the cascode is much higher.

(ii) Compare gains

Cascode:  $Gain_{cas} = -g_{m1} r_{outcas} = -g_{m1} \cdot \frac{g_{m2}}{g_{ds2}} \cdot \frac{1}{g_{ds1}} = \frac{g_{m1}}{g_{ds1}} \cdot \frac{g_{m2}}{g_{ds2}}$

Common source:  $Gain_{cs} = -g_{m3} r_{out3}$

Given that  $g_{m3} = \sqrt{2K'_n \frac{W}{2L} I_D}$

then  $g_{m3} = \frac{g_{m1}}{\sqrt{2}}$

=> Common source:  $Gain_{cs} = -\frac{g_{m1}}{\sqrt{2}} \frac{2}{g_{ds1}} = -\frac{2}{\sqrt{2}} \frac{g_{m1}}{g_{ds1}}$

Since  $\frac{g_{m2}}{g_{ds2}} \gg \frac{2}{\sqrt{2}}$  the gain of cascode is much higher

### (iii) Compare required voltage headroom

Cascode:

The minimum output voltage if the cascode is optimally biased is

$$V_{outcas} \geq 2V_{GT1}$$

$$\text{where } V_{GT} \equiv V_{GS} - V_t$$

Common source:

$$V_{outcs} \geq V_{GT3}$$

$$\text{Since } I_D = \frac{K_n'}{2} \frac{W}{L} (V_{GT3})^2$$

$$\text{then } V_{GT3} = \sqrt{\frac{2I_D}{K_n' \frac{W}{L}}} = \sqrt{2} \sqrt{\frac{2I_D}{K_n' \frac{W}{L}}}$$

$$V_{outcs} \geq V_{GT3} = \sqrt{2} V_{GT1}$$

=> common source stage requires less headroom

---

Note: It can be argued that a fairer comparison would be if we were to dimension M3 to have the same voltage headroom requirement as the cascode stage, i.e. by making  $M3=W/4L$ .

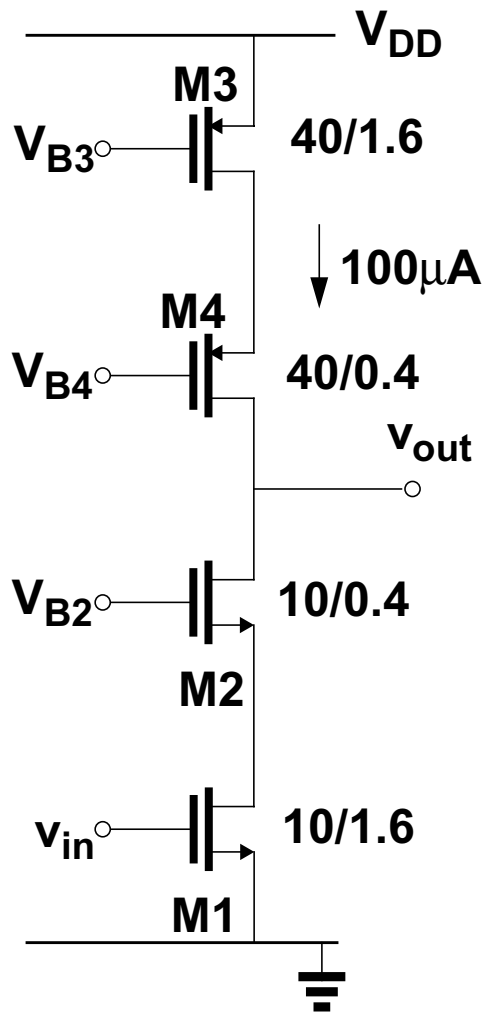
Then for the common source stage:

$$r_{outcs} = \frac{4}{g_{ds1}}$$

$$Gain_{cs} = -2 \frac{g_{m1}}{g_{ds1}}$$

i.e. still much poorer performance w.r.t. cascode

## Problem P. 144 Cascode gain stage with cascode load



From P.134: 
$$Gain = -\frac{g_{m1}}{\frac{g_{ds1}}{g_{m2}/g_{ds2}} + \frac{g_{ds3}}{g_{m4}/g_{ds4}}}$$

Given:  $K_n', K_p', \lambda_n, \lambda_p, I$

Use: 
$$g_{mn} = \sqrt{2K_n' \frac{W}{L} I} \quad g_{dsn} = \lambda_n I$$

$$g_{mp} = \sqrt{2K_p' \frac{W}{L} I} \quad g_{dsp} = \lambda_p I$$

$$g_{m1} = \sqrt{2 \cdot 200\mu A/V^2 \cdot \frac{10}{1.6} \cdot 100\mu A} = 500\mu A/V$$

$$g_{m2} = \sqrt{2 \cdot 200\mu A/V^2 \cdot \frac{10}{0.4} \cdot 100\mu A} = 1mA/V$$

$$g_{m3} = \sqrt{2 \cdot 50\mu A/V^2 \cdot \frac{40}{1.6} \cdot 100\mu A} = 500\mu A/V$$

$$g_{m4} = \sqrt{2 \cdot 50\mu A/V^2 \cdot \frac{40}{0.4} \cdot 100\mu A} = 1mA/V$$

$$g_{ds1} = \frac{0.04V^{-1}}{1.6} \cdot 100\mu A = 2.5\mu A/V$$

$$g_{ds2} = \frac{0.04V^{-1}}{0.4} \cdot 100\mu A = 10\mu A/V$$

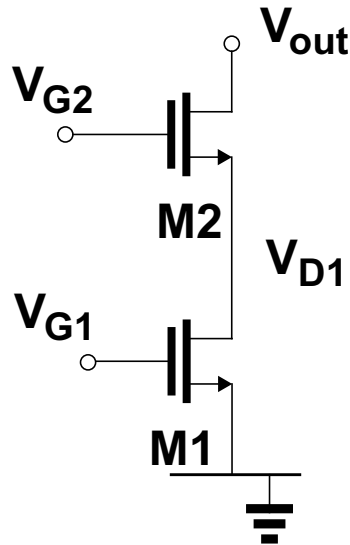
$$g_{ds3} = \frac{0.04V^{-1}}{1.6} \cdot 100\mu A = 2.5\mu A/V$$

$$g_{ds4} = \frac{0.04V^{-1}}{0.4} \cdot 100\mu A = 10\mu A/V$$

$$\begin{aligned} Gain &= -\frac{g_{m1}}{\frac{g_{ds1}}{g_{m2}/g_{ds2}} + \frac{g_{ds3}}{g_{m4}/g_{ds4}}} = -\frac{500}{\frac{2.5}{1000/10} + \frac{2.5}{1000/10}} \\ &= -10000 \end{aligned}$$

$$\text{In dB: } Gain = 80dB$$

## Cascode output resistance - DC point of view



The cascode provides extra gain by increasing the output resistance of the common source stage i.e. the change in output current for a given change in output voltage is reduced.

Looked at from the DC point of view: if the DC voltage at the output increases, then the output current will increase due to the finite output conductance of the transistors.

This current will be provided by M1.

As M1 obeys the equation

$$I_D = \frac{K'_n W}{2L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$

and its  $V_{GS}$  is fixed, then  $V_{D1}$  will increase.

The increase in  $V_{D1}$  reduces  $V_{GS}$  of M2, so that M2 will obey the current equation with a relatively large increase in its  $V_{DS}$ .

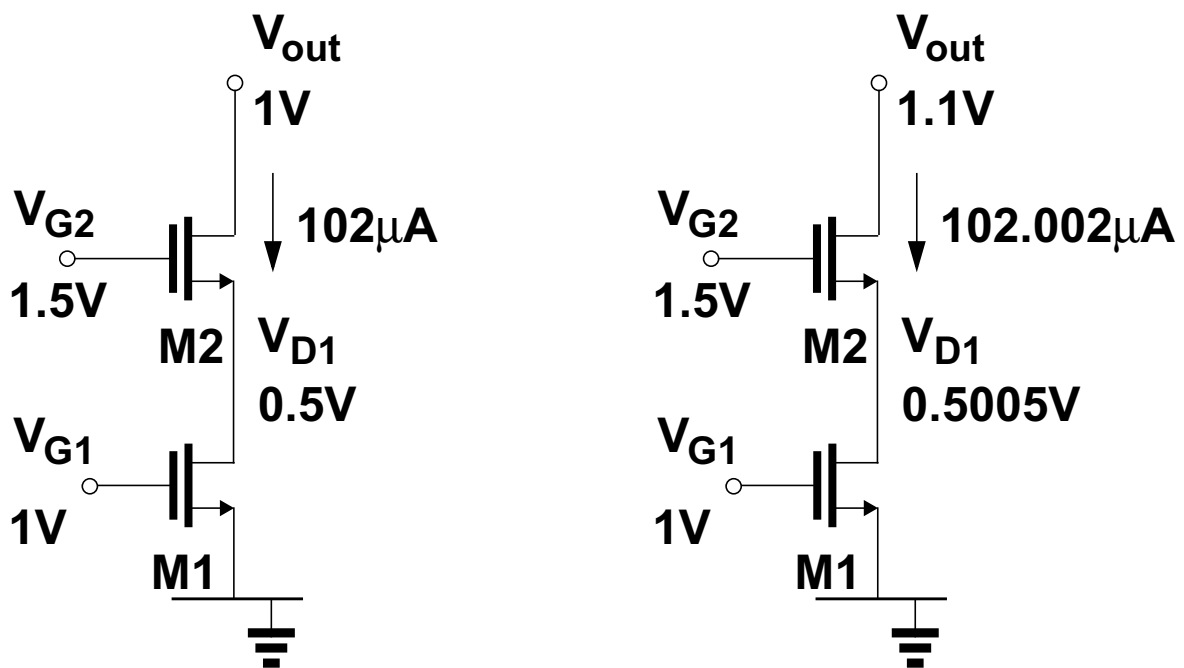
The overall result is that the increase in  $V_{out}$  falls largely over M2, and only a small proportion of the increase falls over M1.

So the current out of M1 increases much less than would be the case without the cascode (basically a factor defined by the ratio of the transconductance of M2 to its output conductance).

Simulation results are given below for 2 output voltages of 1V and 1.1V using the model

$$I_D = \frac{K_n'}{2} \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$

with  $K_n' = 200 \mu\text{A}/\text{V}^2$ ,  $W/L = 16/1$ ,  $V_t = 0.75\text{V}$ ,  $\lambda = 0.04$ .



It can be seen that the voltage at the drain of M1 increases by 0.5mV, and the output current by just 2nA. Without the cascode this would have been 0.4μA.

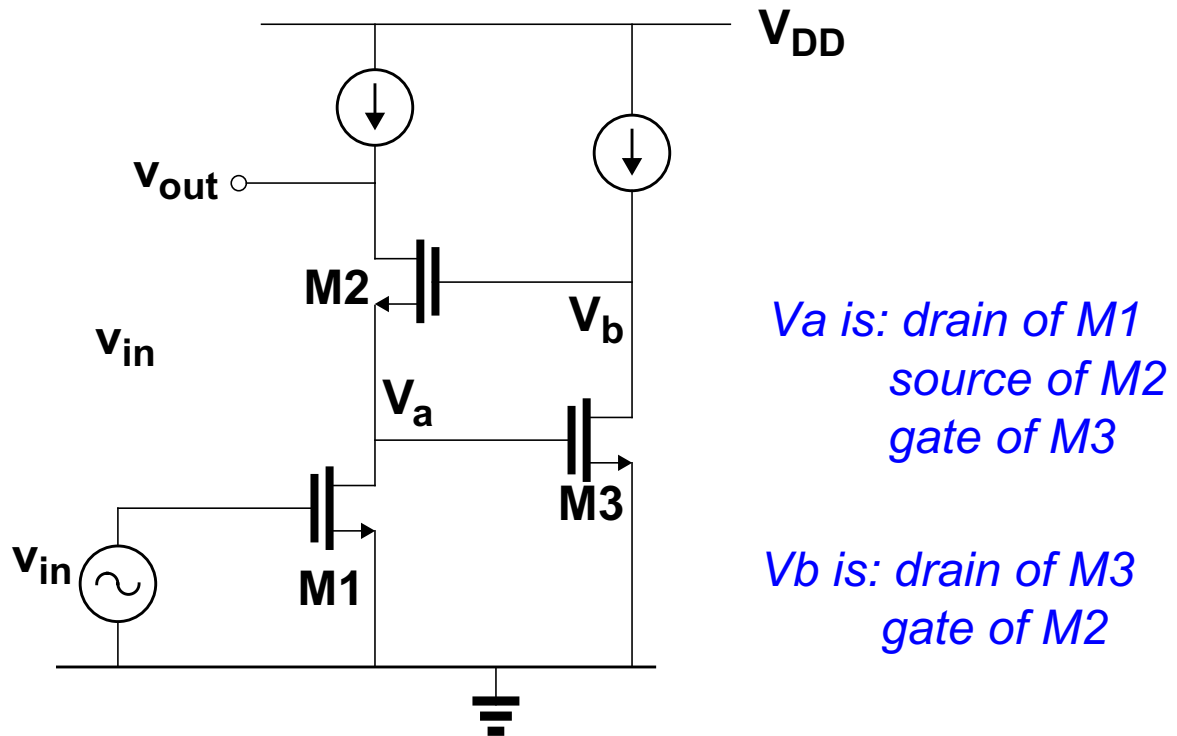


### Problem P150: regulated cascode:

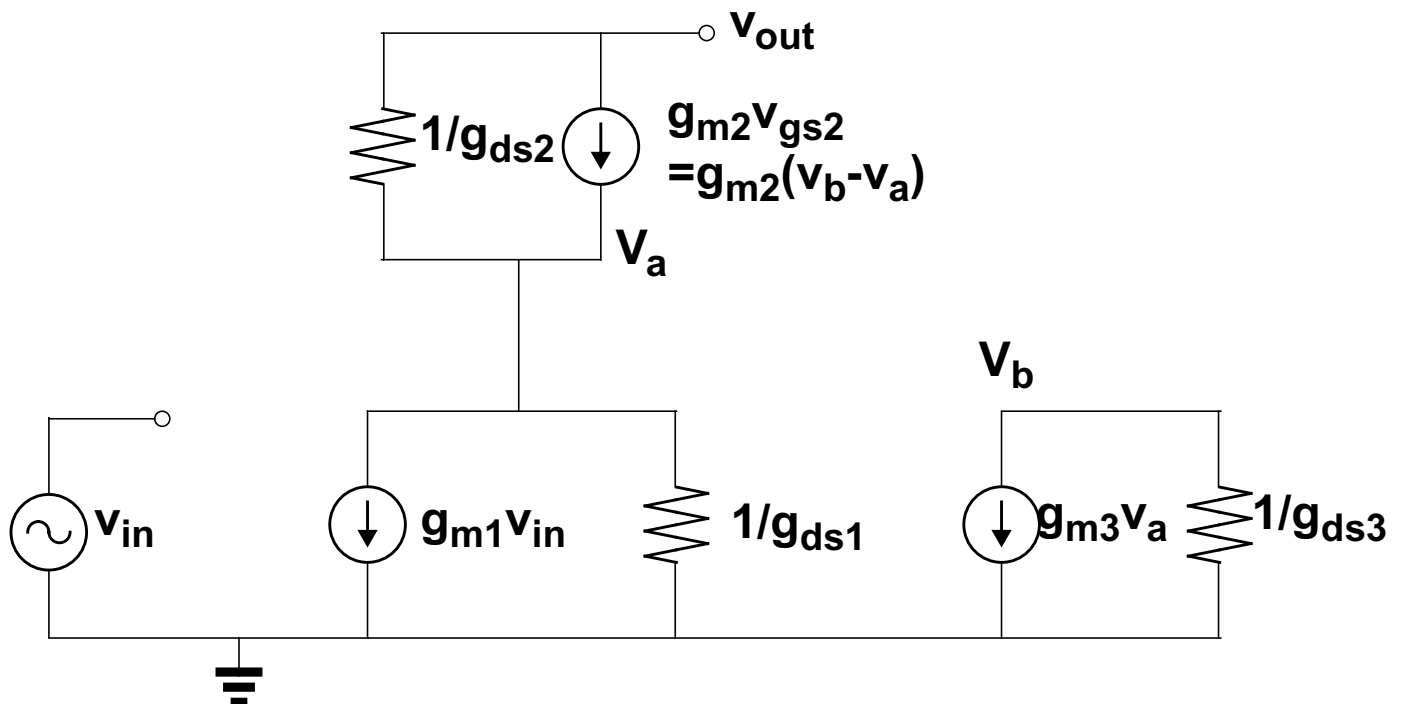
What is voltage gain of stage shown below?

Assume all transistors are biased in saturation.

Ignore body effect.?



Small-signal model



## Small-signal voltage gain

KCL at output node (drain of M2):

$$(v_{out} - v_a)g_{ds2} + g_{m2}(v_b - v_a) = 0 \quad [1]$$

i.e. because there is no current flowing into  $v_{out}$  (biased by ideal DC current source), then the two currents must be equal

KCL at node  $v_a$  (source of M2):

$$(v_{out} - v_a)g_{ds2} + g_{m2}(v_b - v_a) = g_{m1}v_{in} + v_ag_{ds1}$$

$$0 = g_{m1}v_{in} + v_ag_{ds1}$$

$$v_a = -\frac{g_{m1}}{g_{ds1}}v_{in}$$

KCL at node  $v_b$  (gate of M2):

$$g_{m3}v_a = -v_bg_{ds3}$$

$$v_b = -\frac{g_{m3}}{g_{ds3}}v_a$$

$$v_b = \frac{g_{m3}g_{m1}}{g_{ds3}g_{ds1}}v_{in}$$

Substitute for  $v_b, v_a$  in [1]

$$v_{out}g_{ds2} + \frac{g_{m1}}{g_{ds1}}g_{ds2}v_{in} + g_{m2}\left(\frac{g_{m3}g_{m1}}{g_{ds3}g_{ds1}}\right)v_{in} + g_{m2}\left(\frac{g_{m1}}{g_{ds1}}\right)v_{in} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{1}{g_{ds2}}\left(g_{m2}\left(\frac{g_{m3}g_{m1}}{g_{ds3}g_{ds1}}\right) + g_{m2}\left(\frac{g_{m1}}{g_{ds1}}\right) + g_{ds2}\frac{g_{m1}}{g_{ds1}}\right)$$

$$\frac{v_{out}}{v_{in}} = -\left(\frac{g_{m3}g_{m2}g_{m1}}{g_{ds3}g_{ds2}g_{ds1}} + \frac{g_{m2}g_{m1}}{g_{ds2}g_{ds1}} + \frac{g_{m1}}{g_{ds1}}\right) \approx -\frac{g_{m2}g_{m3}g_{m1}}{g_{ds2}g_{ds3}g_{ds1}}$$

This technique is known as ‘gain-boosting’

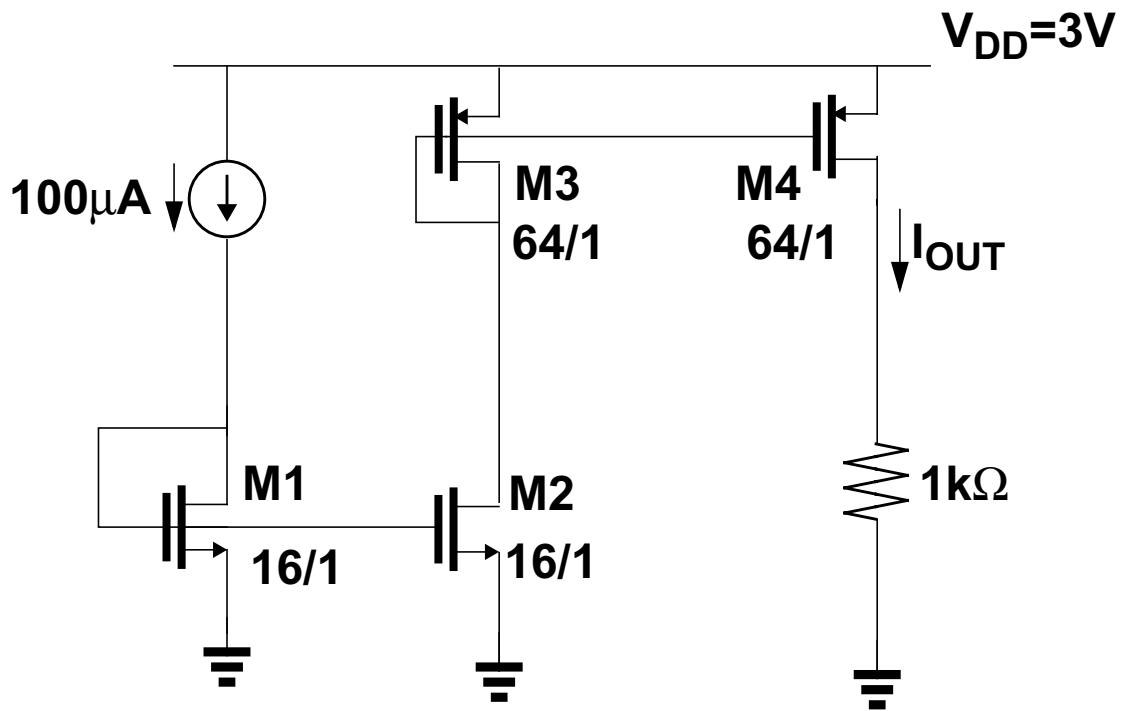
### Problem P174: Current source inaccuracy due to $V_t$ mismatch

Estimate the nominal value and the  $3\sigma$  spread of the current  $I_{OUT}$  in the circuit below.

$$A_{V_t} = 10 \text{ mV}/\mu\text{m}$$

$$K_n' = 200 \mu\text{A}/\text{V}^2, K_p' = 50 \mu\text{A}/\text{V}^2, V_t = 0.75 \text{ V}$$

Assume all errors have a normal distribution and are uncorrelated.



## Problem P.174 Current mirror spread

*Need  $\sigma_{V_t}$  and  $g_m$*

Taking  $\lambda = 0$  initially *i.e. neglecting output conductance*

For nmos mirror

$$\sigma_{V_{tn}} = \frac{A_{V_{tn}}}{\sqrt{WL}} = \frac{10mV\mu m}{\sqrt{16\mu m \cdot 1\mu m}} = 2.5mV$$

$$V_{GS1} - V_{tn} = \sqrt{\frac{2I_D}{K'_n \frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V^2 \frac{16}{1}}} = 0.25V$$

$$g_{mn} = \frac{2I_D}{V_{GS} - V_{tn}} = \frac{2 \times 100\mu A}{0.25V} = 800\mu A/V$$

$$\sigma_{I_{Dn}} = g_{mn} \sigma_{V_{tn}} = 800\mu A/V \times 2.5mV = 2\mu A$$

For pmos mirror

$$\sigma_{V_{tp}} = \frac{A_{V_{tp}}}{\sqrt{WL}} = \frac{10mV\mu m}{\sqrt{64\mu m \cdot 1\mu m}} = 1.25mV$$

$$|V_{GS3} - V_{tp}| = \sqrt{\frac{2I_D}{K'_n \frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{50\mu A/V^2 \frac{64}{1}}} = 0.25V$$

$$g_{mp} = \frac{2I_D}{V_{GS} - V_{tp}} = \frac{2 \times 100\mu A}{0.25V} = 800\mu A/V$$

$$\sigma_{I_{Dp}} = g_{mp} \sigma_{V_{tp}} = 800\mu A/V \times 1.25mV = 1\mu A$$

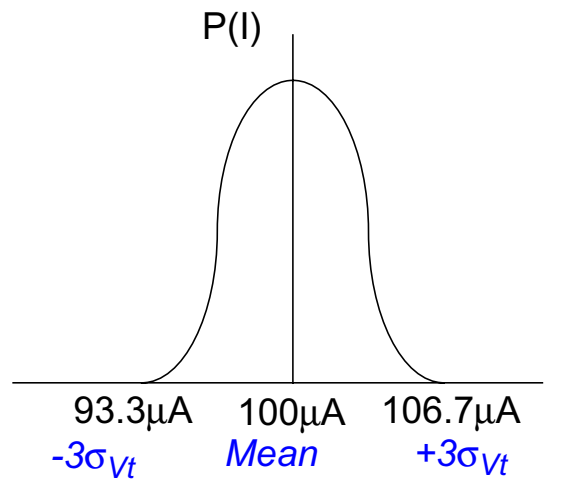
$$\sigma_{I_{OUT}} = \sqrt{\sigma_{I_{Dn}}^2 + \sigma_{I_{Dp}}^2}$$

*Mismatches are uncorrelated => add quadratically*

$$\sigma_{I_{OUT}} = \sqrt{2^2 + 1^2} = 2.236\mu A$$

This is the total  $1\sigma$  sigma mismatch between  $I_{IN}$  and  $I_{OUT}$

If we specify for  $3\sigma$  sigma mismatch then we specify  $100\mu A \pm 6.7\mu A$



*i.e. if this circuit was fabricated in this process and the output current was measured on say millions of samples from many batches over time, then the output current would have a mean value of  $100\mu A$ , and be between  $93.3\mu A$  and  $106.7\mu A$  on 99.7% of the samples*

*Q: How to reduce the spread*

The above analysis ignored the static error.

To calculate the mean output current, the finite output conductance must be taken into account

Taking  $\lambda = 0.04V^{-1}$

*nmos mirror:*

$$V_{GS1} = V_{DS1} = 1.0V$$

$$|V_{GS3}| = |V_{DS3}| = 1.0V$$

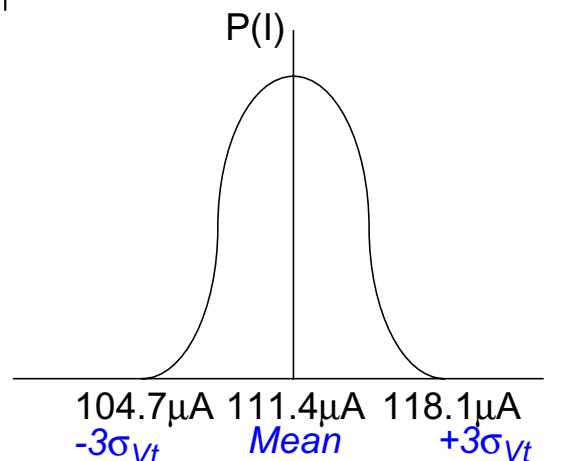
$$V_{DS2} = V_{DD} - |V_{GS3}| = 2V$$

$$\frac{I_{D2}}{I_{D1}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} = \frac{1 + 0.04 \times 2}{1 + 0.04 \times 1} \Rightarrow I_{D2} = 103.8\mu A$$

*pmos mirror:*

$$V_{DS4} = V_{DD} - I_{OUT} \times 1k\Omega \approx 2.9V$$

$$\frac{I_{D4}}{I_{D3}} = \frac{1 + \lambda |V_{DS4}|}{1 + \lambda |V_{DS3}|} = \frac{1 + 0.04 \times 2.9}{1 + 0.04 \times 1} \Rightarrow I_{D4} = 1.07 I_{D3} = 111.4\mu A$$



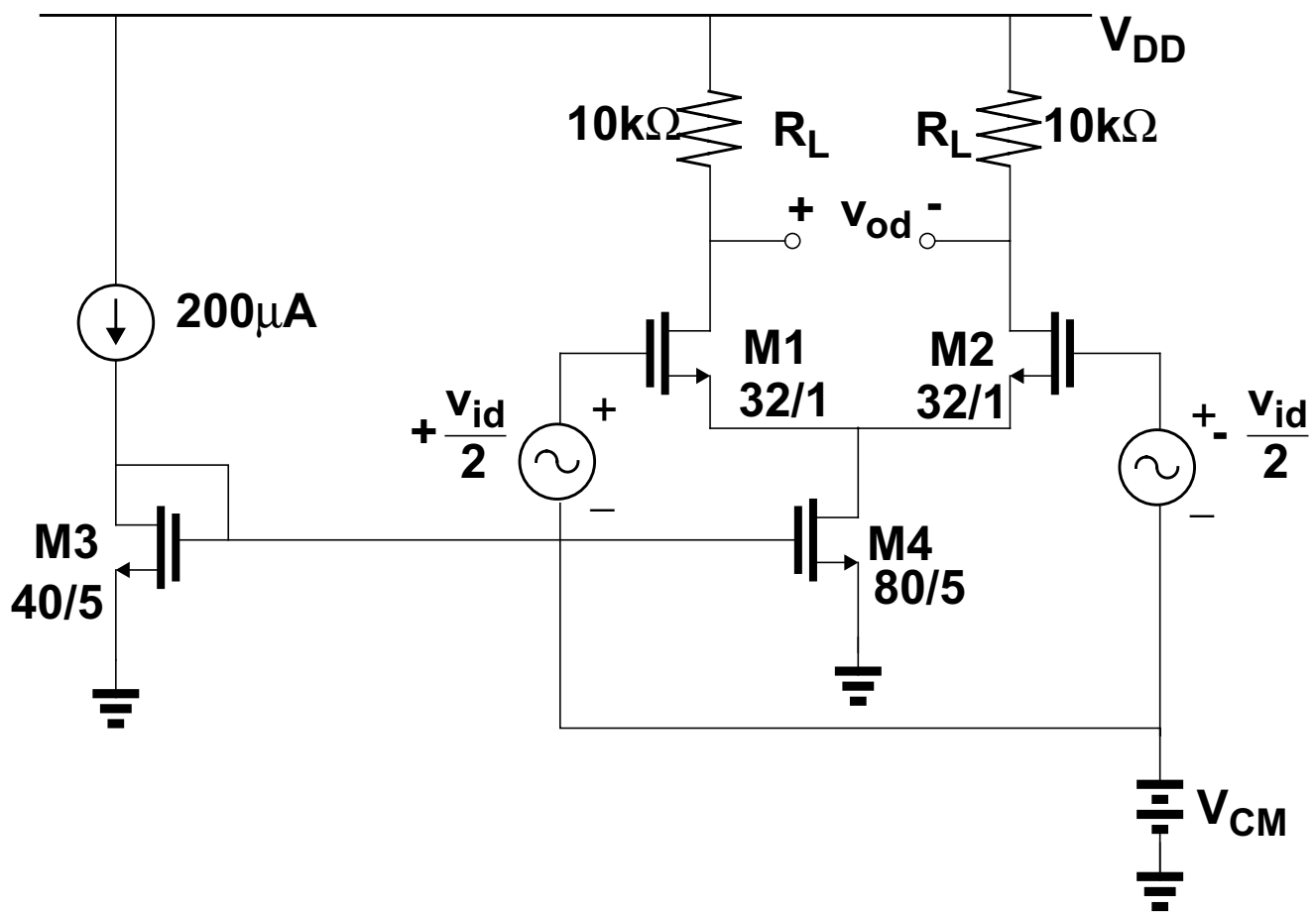
Note: there are still a number of approximations in this answer.

*e.g. gm slightly different to initial calculation, resistor variation.*

For fully accurate yield prediction, use Monte Carlo simulations

*Q: How to reduce the static error*

## Problem P192 - Diff. amp. common-mode input range, CMRR



- (i) What is the allowed range of the common-mode input voltage (i.e. the range in the quiescent state such that all transistors remain in saturation)?
- (ii) What is the value of the differential gain?
- (iii) What is the value of the common-mode gain?
- (iv) What is the CMRR?

$$V_{DD} = 3.3\text{V}$$

$$V_t = 1\text{V}, \lambda_n = 0.04/\text{L V}^{-1}$$

$$K_n' = 200\mu\text{A/V}$$

## Problem P. 192 (Common-Mode Input Range)

(i) Common-mode input voltage range

### 1. Lower limit on $V_{CM}$ :

The common-mode voltage is bound on the lower side by the voltage at the common-source node falling with the common-mode voltage and pushing M4 out of saturation.

$$\text{M4: } V_{GS4} - V_t = \sqrt{\frac{2 \cdot 400\mu A}{200\mu A/V \cdot \frac{80}{5}}} = 500mV$$

=> Voltage at drain of M4 must be greater than 0.5V.

$$\text{M1: } V_{GS1} - V_t = \sqrt{\frac{2 \cdot 200\mu A}{200\mu A/V \cdot \frac{32}{1}}} = 250mV$$

$$V_{GS1} = 250mV + V_t = 1.25V$$

So minimum common-mode voltage given by

$$V_{CMmin} = V_{D4min} + V_{GS1}$$

$$V_{CMmin} = 0.5V + 1.25V = 1.75V$$



---

### 1. Upper limit on $V_{CM}$ :

The common-mode voltage is bound on the upper side by the voltage at the common-source node rising with the common-mode voltage and pushing M1,M2 out of saturation.

$$V_{D1} = V_{DD} - I_D R_L = 3.3V - 200\mu A \times 10k\Omega = 1.3V$$

$$V_{DS1} \geq V_{GS1} - V_t$$

$$V_{S1} \leq V_{D1} - (V_{GS1} - V_t)$$

$$V_{S1} \leq 1.3V - 0.25V = 1.05V$$

So maximum common-mode voltage given by

$$V_{CM} \leq V_{S1min} + V_{GS1}$$

$$V_{CM} \leq 1.05V + 1.25V = 2.3V$$

$$V_{CMmax} = 2.3V$$

Common-mode input range given by

$$V_{CMmin} \leq V_{CM} \leq V_{CMmax}$$

$$1.75V \leq V_{CM} \leq 2.3V$$

*Comment: This is quite a narrow input range, as full signal swing must be allowed for.*

*Also need to allow margin for PVT spread etc.*

## (ii) Differential Gain

$$A_{dm} = -\frac{g_{m1}}{g_{ds1} + \frac{1}{R_L}}$$

$$g_{m1} = \sqrt{2K'_n \frac{W_1}{L_1} I_{D1}} = \sqrt{2 \times 200 \mu A/V \times \frac{32}{1} \times 200 \mu A} = 1.6 mA/V$$

$$g_{ds1} = \lambda I_{D1} = \frac{0.04}{1} \times 200 \mu A = 8 \mu A/V$$

$$\frac{1}{g_{ds1}} = 125 k\Omega \Rightarrow \frac{1}{g_{ds1}} \gg R_L$$

$$A_{dm} \approx -g_{m1} R_L = 1.6 mA/V \times 10 k\Omega = -16 \equiv 24 dB$$

## (iii) Common-mode Gain

$$A_{cm} = -\frac{R_L}{2R_{cur}}$$

$R_{cur}$  is output resistance of M4 *tail current source*

$$g_{ds4} = \lambda I_{D4} = \frac{0.04}{5} \times 400 \mu A = 3.2 \mu A/V$$

$$\frac{1}{g_{ds4}} = 312.5 k\Omega \equiv R_{cur}$$

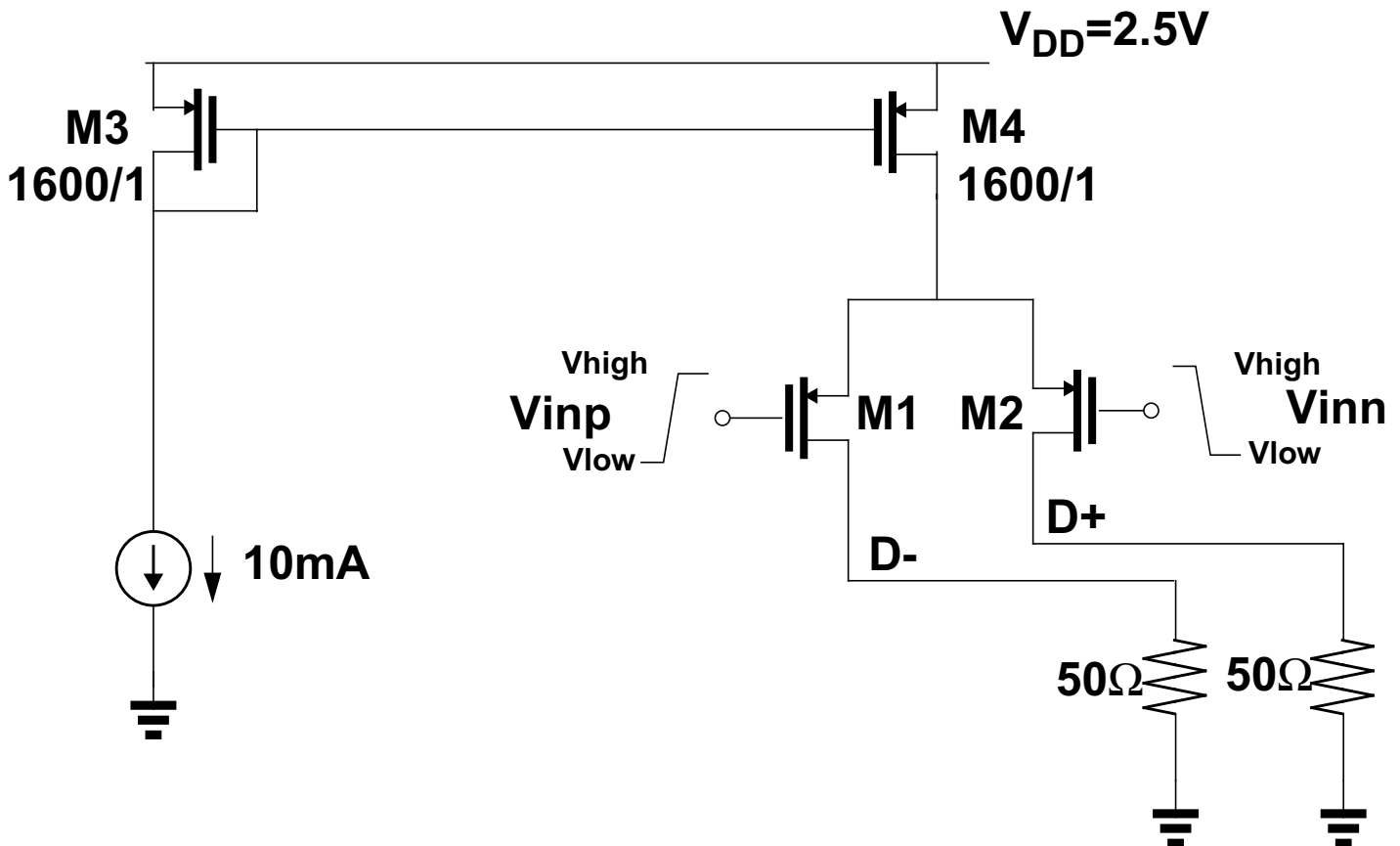
$$A_{cm} = -\frac{10 k\Omega}{2 \times 312.5 k\Omega} = -16 e^{-3} \equiv -36 dB$$

## (iv) Common-mode rejection ratio

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right| = \left| \frac{-16}{-16 e^{-3}} \right| = 1000 \equiv 60 dB$$



## Problem: (supplement to P 177) **SKIPPED**



For an interconnectivity application a differential signal current is sourced into a differential cable (D+, D-) terminated in  $50\Omega$ . The signal current is set up by the mirror M3:M4, and is switched into the positive or negative output lines by the switches M1,M2 which are driven by differential logic signals  $V_{inp}$  and  $V_{inn}$ . The low logic level ( $V_{low}$ ) is 0V.

Take  $K_p' = 50\mu A/V^2$ ,  $V_{tp} = -0.75V$ .

- What are the dimensions of the switches for optimal mirroring accuracy?
- What is the minimum logic high level ( $V_{high}$ ) such that the 'off' switch is completely turned off?

---

**Problem Solution: (supplement to P 177) SKIPPED**

(i) What are the dimensions of the switches for optimal mirroring accuracy?

$$\text{M3: } |V_{GS3}| - |V_t| = \sqrt{\frac{2 \cdot 10mA}{50\mu A/V \cdot \frac{1600}{1}}} = 500mV$$

$$|V_{GS3}| = 500mV + |V_{tp}| = 500mV + 750mV = 1.25V$$

$$V_{D3} = V_{DD} - |V_{GS3}| = 2.5V - 1.25V = 1.25V$$

For optimal mirroring accuracy the drain of M4 should be at 1.25V  
Voltage at drain of M4 is set by  $V_{GS}$  across M1 or M2

For example if M1 on:

$$V_{D4} = V_{low} + V_{GS1} = 1.25V \Rightarrow V_{GS1} = 1.25V$$

So W/L of M1,M2 should be same as M3,M4 i.e. 1600/1.

*would probably use min. L to reduce capacitive load  
would also reduce  $I_{D3}$  to  $\ll 10mA$*

(ii) What is the minimum logic high level ( $V_{high}$ ) such that the 'off' switch is completely turned off?

For all current to be flowing in M1 or in M2 then

$$\sqrt{\frac{2I_S}{K'_p \frac{W}{L}}} < v_{id} < -\sqrt{\frac{2I_S}{K'_p \frac{W}{L}}}$$

$$\sqrt{\frac{2 \cdot 10mA}{50\mu A/V \cdot \frac{1600}{1}}} < V_{inp} - V_{inn} < -\sqrt{\frac{2 \cdot 10mA}{50\mu A/V \cdot \frac{1600}{1}}}$$

$$500mV < V_{inp} - V_{inn} < -500mV$$

For example if all current to be flowing in M1 then

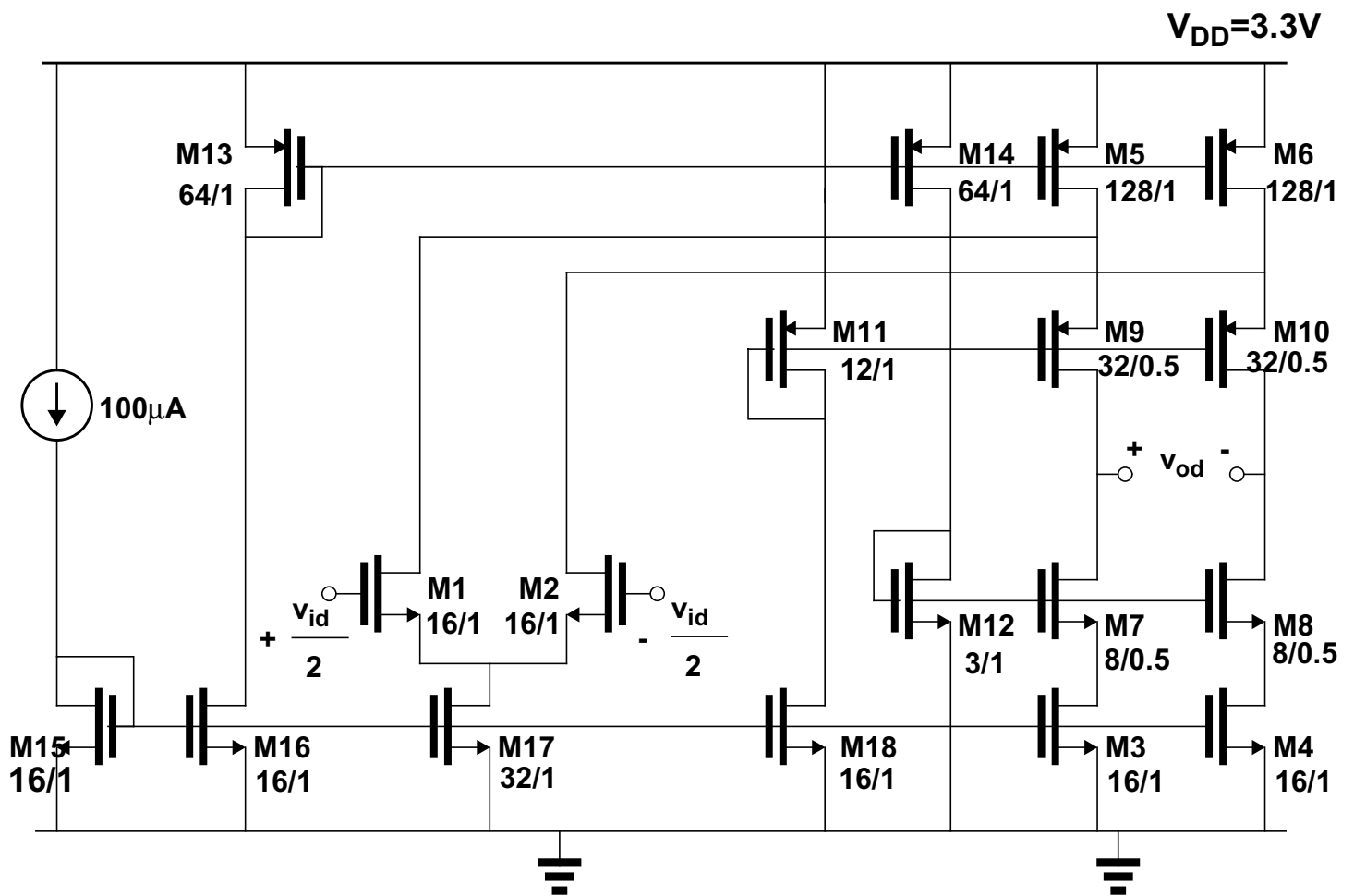
$$V_{inp} - V_{inn} < -500mV$$

$$V_{low} - V_{high} < -500mV$$

$$V_{high} > 500mV$$

*Above analysis is a bit clumsy - basically just need the logic swing to be  $= V_{GS} - V_t$  for a current of 10mA.  
Also: Want low swing to minimize disturbances at common-source node.*

## Problem P207: Folded Cascode differential amplifier.



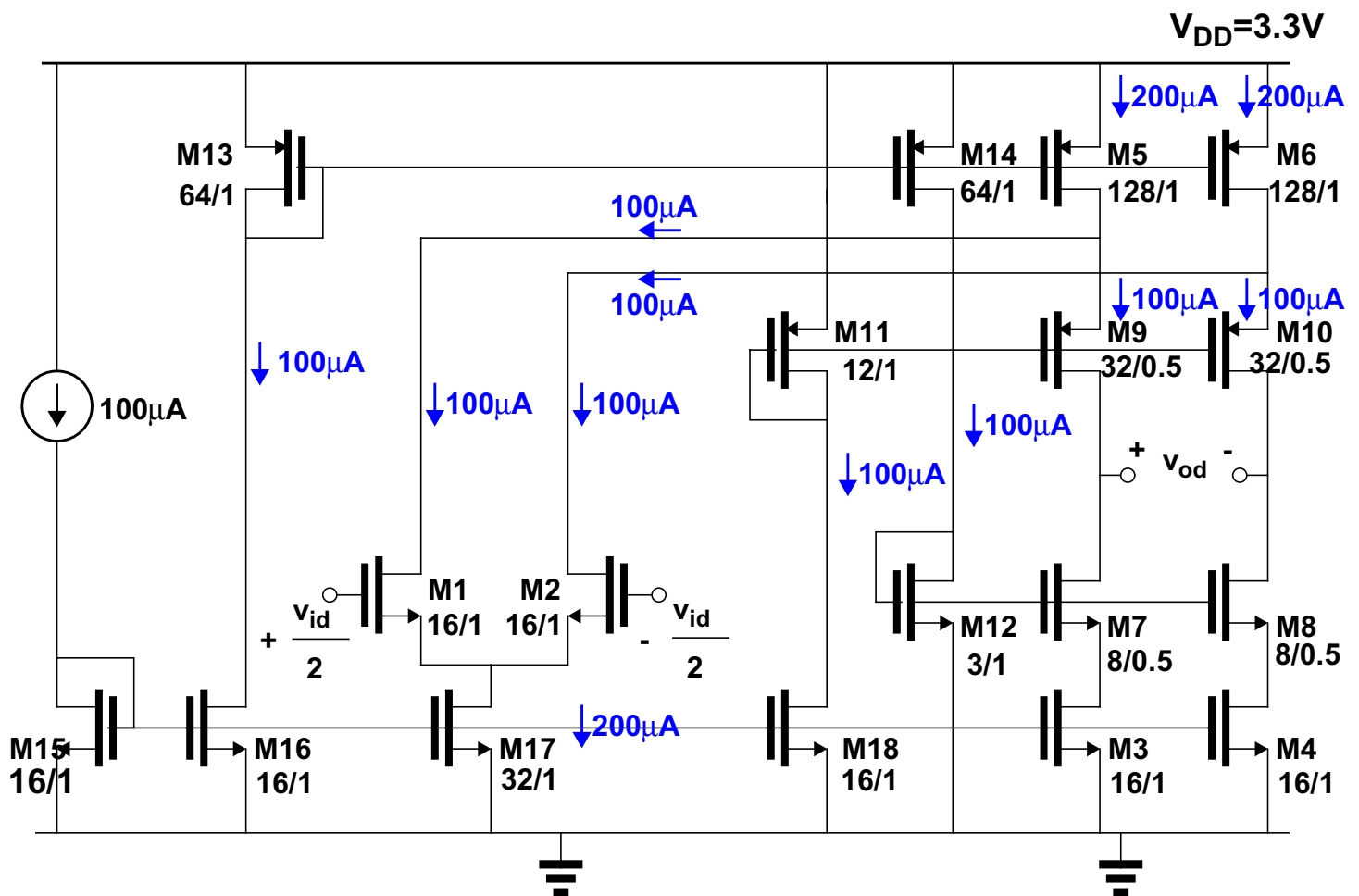
Calculate the small-signal gain of the folded-cascode amplifier shown.

Dimensions are as shown.

Assume all transistors are in saturation.

$K_n' = 200\mu A/V^2$ ,  $K_p' = 50\mu A/V^2$ ,  $V_t = 0.75V$ ,  $\lambda = 0.04/L V^{-1}$

## Branch Currents



The input bias current is mirrored via M15 to the p-side mirror (through M16), to the differential pair (through M17), to the output stage (through M3, M4), and to the p cascode generation diode (through M18).

The p-bias current from M16 is mirrored via M13 to the output stage (through M5, M6) and to the n cascode generation diode (through M14).



## Voltage requirements

All transistors except M11,M12 are dimensioned for  $V_{GS}-V_t=250mV$ ,  
i.e.  $V_{GS}=1V$

$$M3,M4: V_{GS} - V_t = \sqrt{\frac{2I_D}{K'_n \frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V^2 \frac{16}{1}}} = 250mV$$

$$M9,M10: |V_{GS}| - |V_t| = \sqrt{\frac{2I_D}{K'_p \frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{50\mu A/V^2 \frac{32}{0.5}}} = 250mV$$

$$M5,M6: |V_{GS}| - |V_t| = \sqrt{\frac{2I_D}{K'_p \frac{W}{L}}} = \sqrt{\frac{2 \cdot 200\mu A}{50\mu A/V^2 \frac{128}{1}}} = 250mV$$

M12 sets up the cascode voltage on the NMOS output side.  
From the notes the W/L needs to be at least 4/1.  
A safety margin is taken here and 3/1 is used.

$$M12: V_{GS} - V_t = \sqrt{\frac{2I_D}{K'_n \frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{100\mu A/V^2 \frac{3}{1}}} = 577mV$$

The voltage at the source of M7 is

$$V_{S7} = (V_t + 577mV) - (V_t + 250mV) = 327mV$$

i.e. 77mV above the minimum required.

Similarly M11 sets up the cascode voltage on the PMOS output side. From the notes the W/L needs to be at least 16/1. A safety margin is taken here and 12/1 is used.

$$\text{M12: } |V_{GS}| - |V_t| = \sqrt{\frac{2I_D}{K'_p \frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{50\mu A/V^2 \frac{12}{1}}} = 577mV$$

The voltage at the source of M9 is

$$V_{S9} = V_{DD} - ((|V_t| + 577mV) + (|V_t| + 250mV))$$

$$V_{S9} = V_{DD} - 327mV$$

i.e. 77mV above the minimum required.

The common-mode input voltage needs to be greater than 1.25V so that M17 is in saturation.

The maximum common mode input voltage is given by the requirement that the input pair is in saturation i.e.

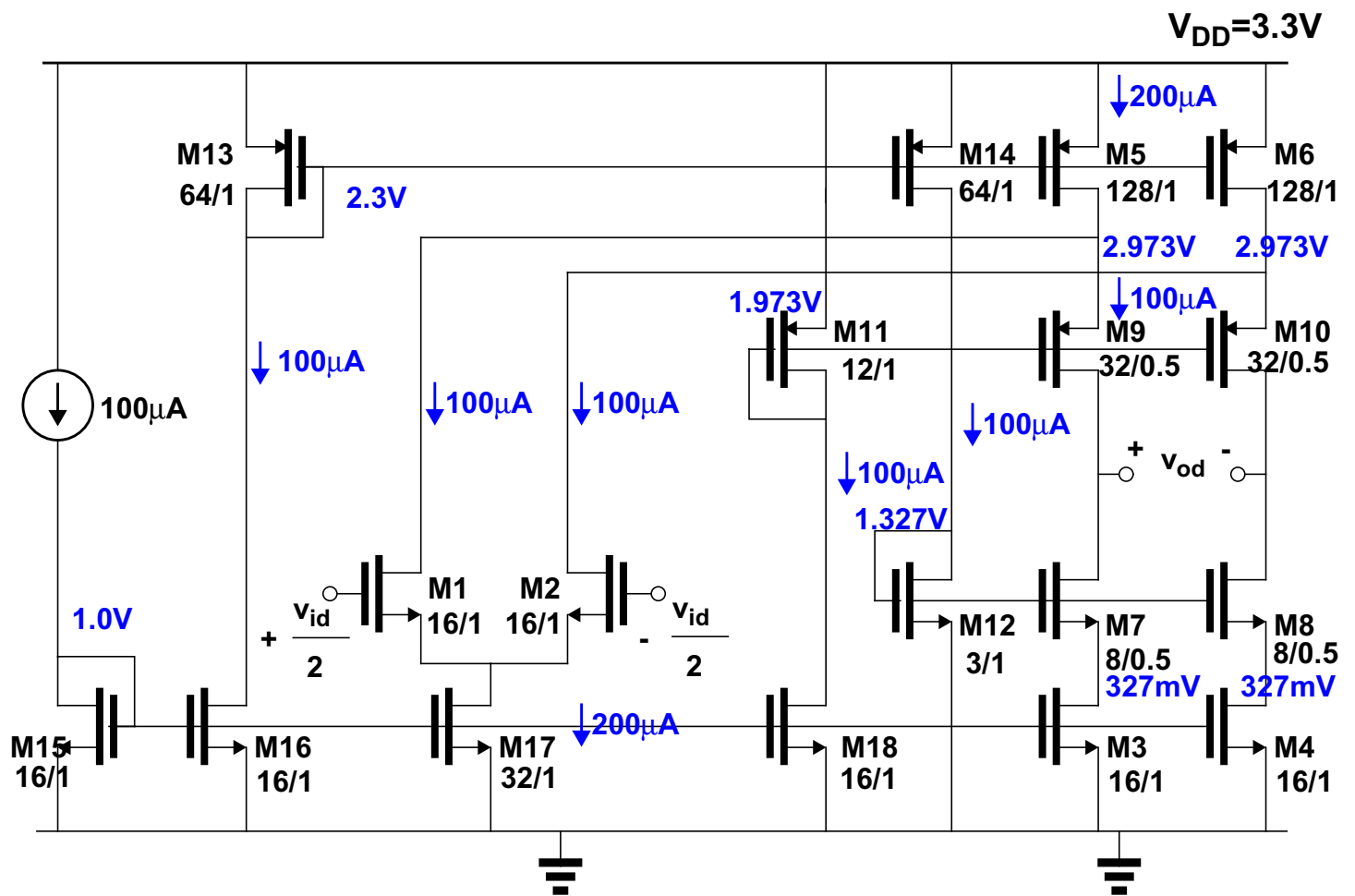
$$V_{CM} - |V_t| < V_{DD} - 327mV$$

$$V_{CM} < V_{DD} - 327mV + |V_t|$$

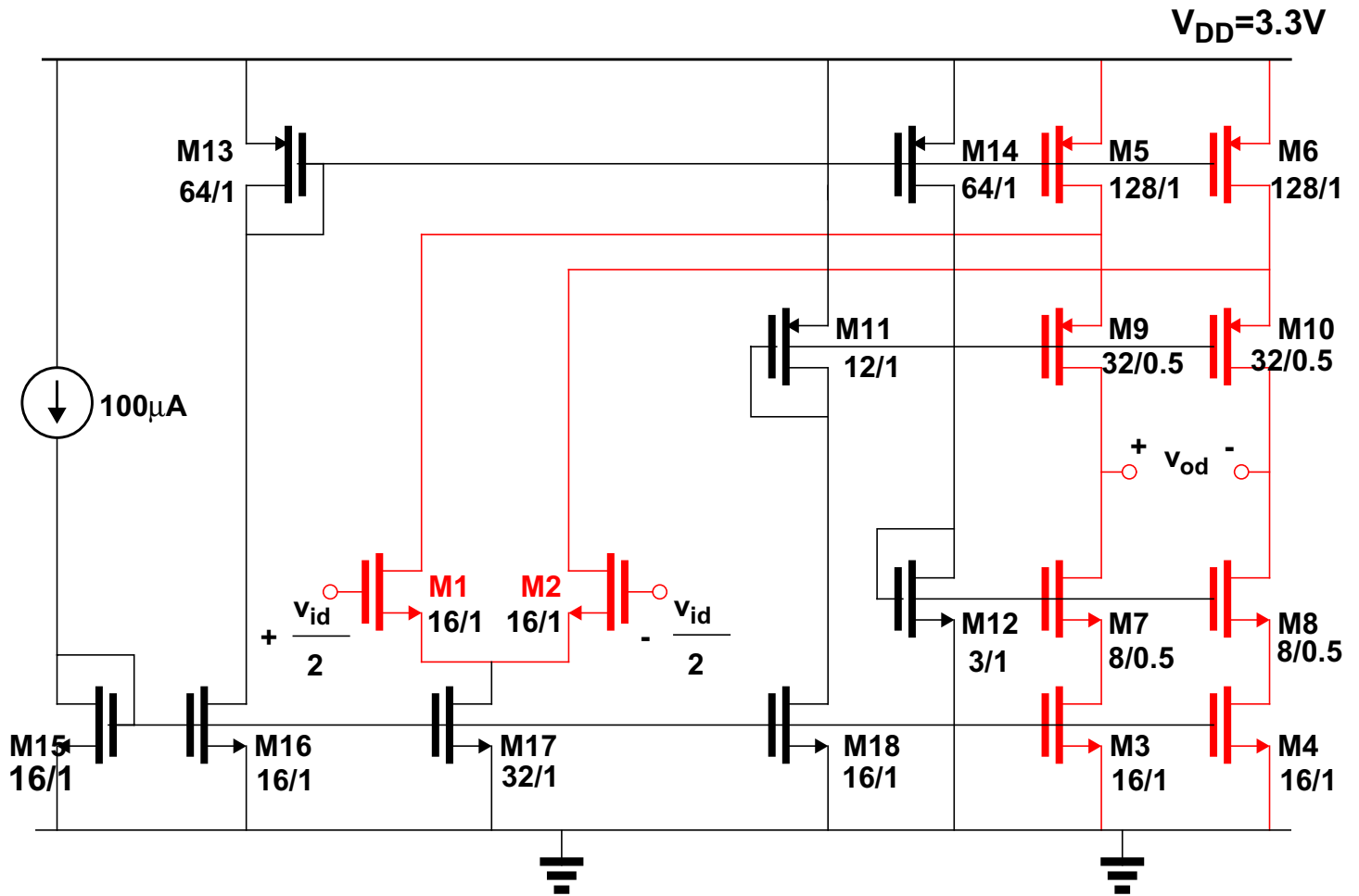
$$V_{CM} < 3.3V - 327mV + 0.75V$$

$$V_{CM} < 3.723V$$

# DC Bias Voltages



## Signal path



## Gain

$$\frac{v_{od}}{v_{id}} = - \frac{g_{m1}}{\frac{g_{ds3}}{g_{m7}/g_{ds7}} + \frac{g_{ds1} + g_{ds5}}{g_{m9}/g_{ds9}}}$$

**Use:**  $g_{mn} = \sqrt{2K'_n \frac{W}{L} I}$

$$g_{dsn} = \lambda_n I$$

$$g_{mp} = \sqrt{2K'_p \frac{W}{L} I}$$

$$g_{dsp} = \lambda_p I$$

$$g_{m1} = \sqrt{2 \cdot 200\mu A/V^2 \cdot \frac{16}{1} \cdot 100\mu A} = 800\mu A/V$$

$$g_{m7} = \sqrt{2 \cdot 200\mu A/V^2 \cdot \frac{8}{0.5} \cdot 100\mu A} = 800\mu A/V$$

$$g_{m9} = \sqrt{2 \cdot 50\mu A/V^2 \cdot \frac{32}{0.5} \cdot 100\mu A} = 800\mu A/V$$

$$g_{ds1} = \frac{0.04V^{-1}}{1} \cdot 100\mu A = 4\mu A/V$$

$$g_{ds3} = \frac{0.04V^{-1}}{1} \cdot 100\mu A = 4\mu A/V$$

$$g_{ds5} = \frac{0.04V^{-1}}{1} \cdot 200\mu A = 8\mu A/V$$

$$g_{ds7} = \frac{0.04V^{-1}}{0.5} \cdot 100\mu A = 8\mu A/V$$

$$g_{ds9} = \frac{0.04V^{-1}}{0.5} \cdot 100\mu A = 8\mu A/V$$

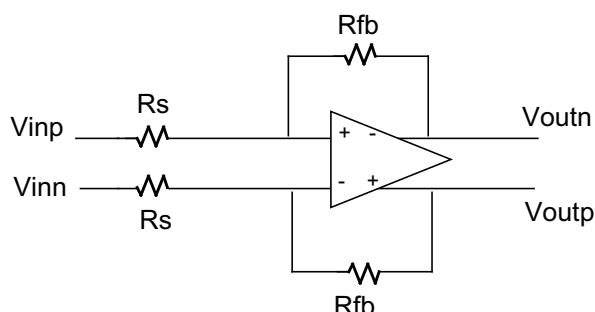
$$Gain = -\frac{g_{m1}}{\frac{g_{ds3}}{g_{m7}/g_{ds7}} + \frac{g_{ds1} + g_{ds5}}{g_{m9}/g_{ds9}}} = -\frac{800}{\frac{4}{800/8} + \frac{4+8}{800/8}}$$

$$= -5000$$

$$\text{In dB: } Gain = 74dB$$

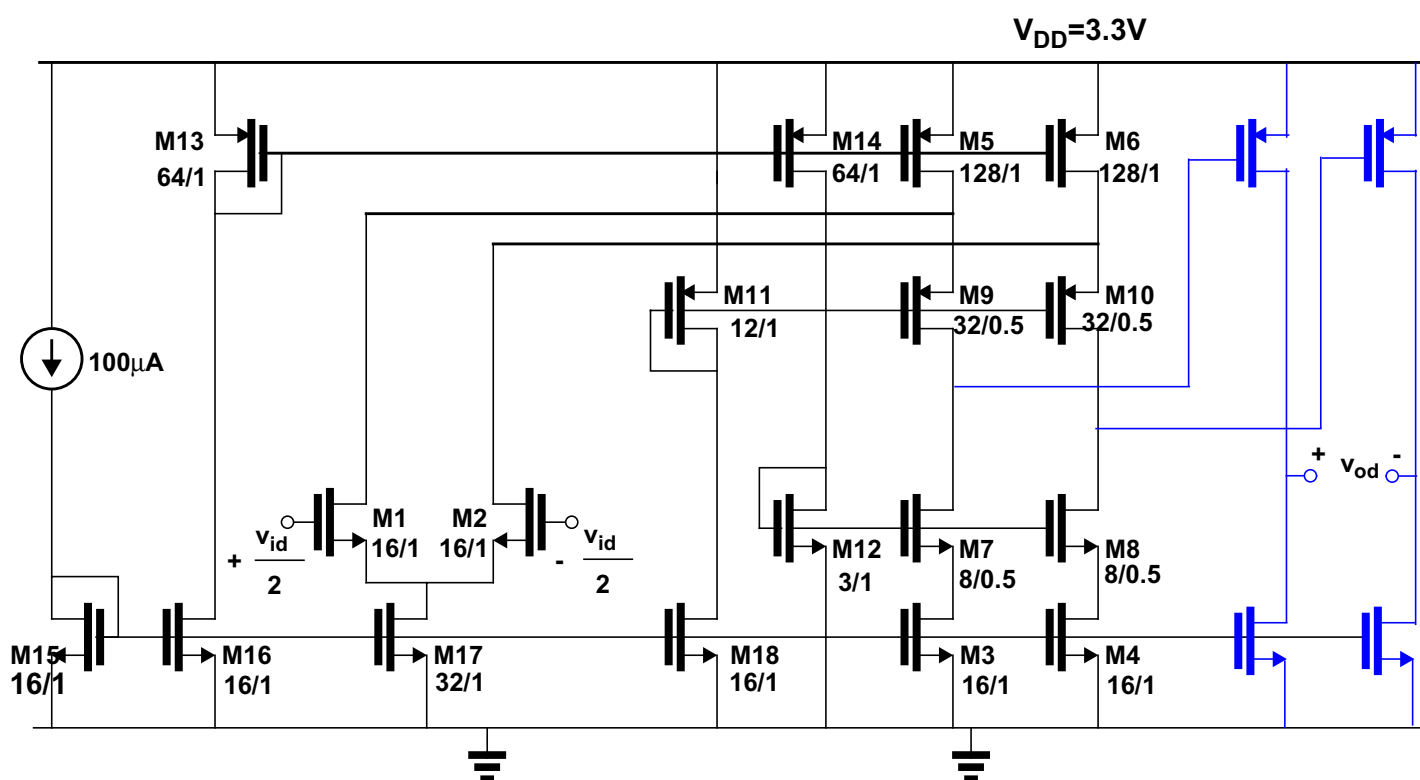
## Note on output stage:

Many opamp applications require driving a resistive load e.g. gain stages, filters.



$$\frac{V_{out}}{V_{in}} \equiv \frac{V_{outp} - V_{outn}}{V_{inp} - V_{inn}} \cong -\frac{R_{fb}}{R_s}$$

If the previous opamp were used in this configuration its gain would reduce to  $\sim g_{m1} R_{fb}$ . An extra buffer stage (e.g. common-source stage) is required to drive the resistive load:



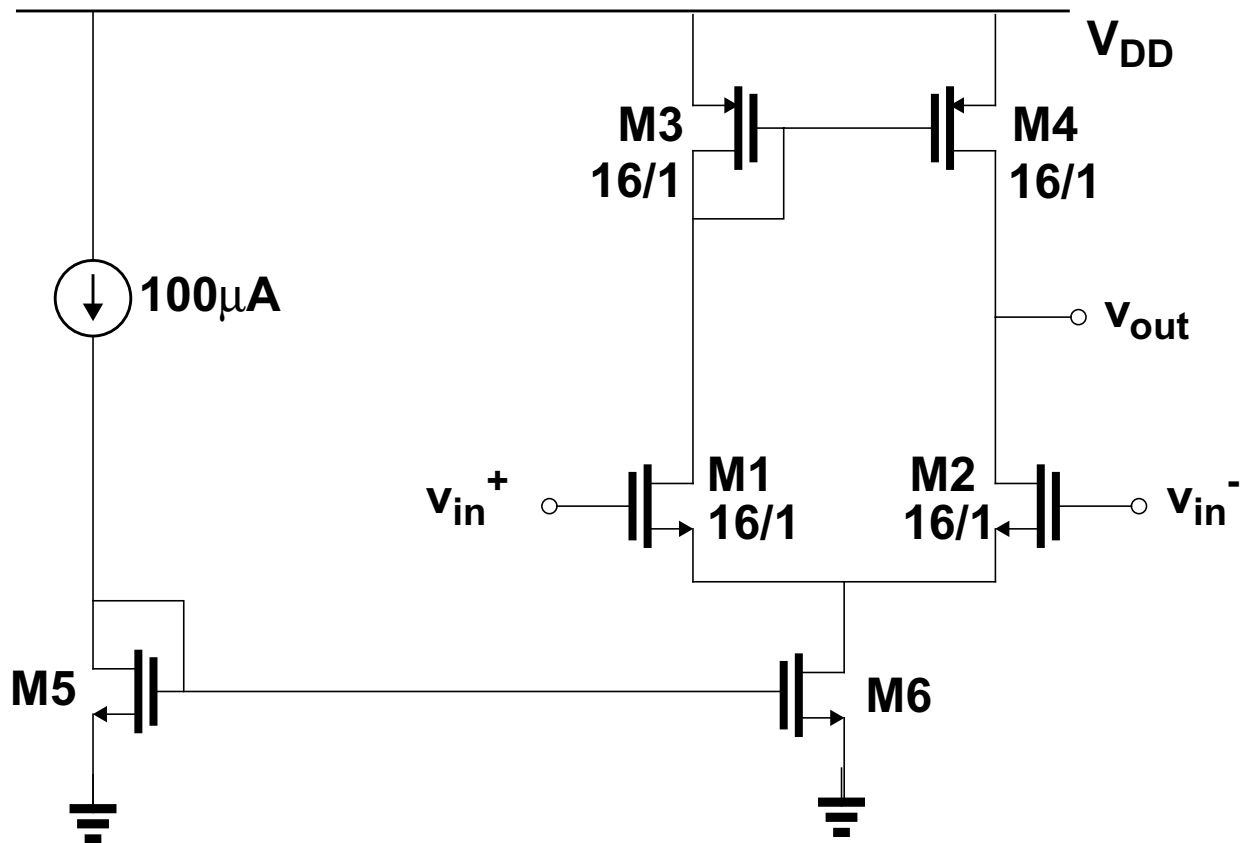
Notes:

Compensation for stability not shown.

CMFB not shown.

Opamp as drawn has positive gain

## Problem (supplement to P 206)



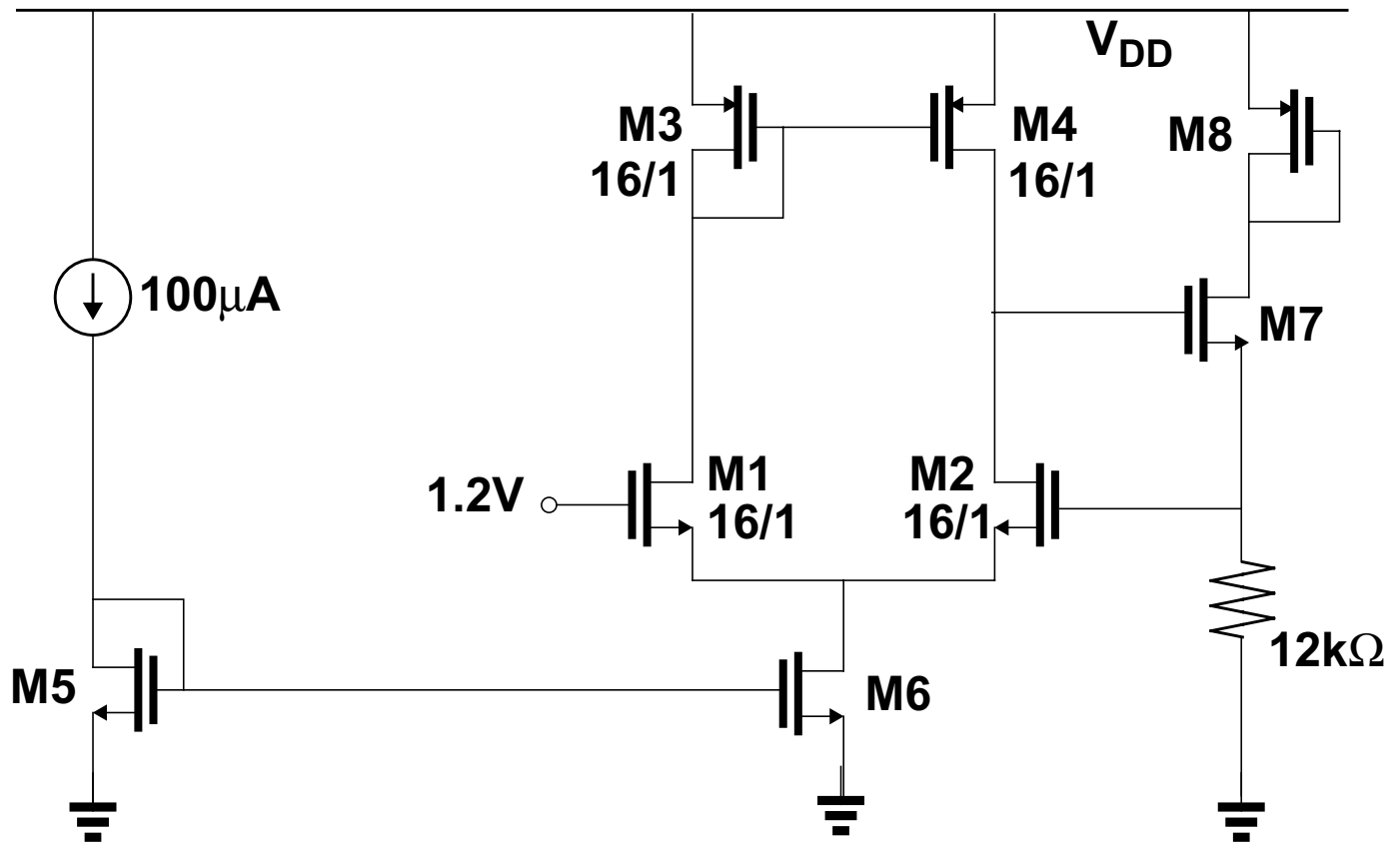
The opamp shown is to be used in the current reference circuit of P147. Each input transistor is to have a drain current of  $100\mu\text{A}$ . Body effect may be ignored.

Use  $V_{tn}=|V_{tp}|=0.7\text{V}$ ,  $K_n'=200\mu\text{A/V}^2$ ,  $K_p'=50\mu\text{A/V}^2$

$\lambda_n=\lambda_p=0.04/\text{L V}^{-1}$

- Draw the full circuit
- What  $W/L$  is required for the mirror transistors M5, M6?
- What  $W/L$  is required for the source follower?
- What is the open-loop gain of the circuit?
- What is the effect on the circuit if the reference resistor is reduced from  $12\text{k}\Omega$  to  $3\text{k}\Omega$ ?

(i) Draw the full circuit



N.B Assume stability has been taken care of!

(ii) What W/L is required for the mirror transistors M5, M6?

$$M1: V_{GS1} - V_t = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V \cdot \frac{16}{1}}} = 250mV$$

$$V_{GS1} = 250mV + V_t = 250mV + 700mV = 950mV$$

So the drain of M6 is at 1.2V-950mV=250mV

=>  $V_{GS} - V_t$  of M6 is max 250mV

M6 is to carry twice the current of M1, so will need 2XW/L of M5

=> W/L min for M5 = 32/1 (use higher L for good current mirror)



(iii) What W/L is required for the source follower?

The first requirement is that M4 is in saturation.

If the amplifier is to be dimensioned optimally to give exactly 1.2V at the gate of M2, then it needs to be symmetrical

=> voltage at the drain of M3 should be equal to voltage at drain of M4.

$$\text{M3: } |V_{GS3}| - |V_t| = \sqrt{\frac{2 \cdot 100\mu A}{50\mu A/V \cdot \frac{16}{1}}} = 500mV$$

$$|V_{GS3}| = 500mV + |V_t| = 500mV + 700mV = 1.2V$$

$$V_{D3} = V_{DD} - |V_{GS3}| = 3.3V - 1.2V = 2.1V$$

For the drain of M4 to be at 2.1V then  $V_{GS7}$  needs to be 0.9V

=>  $V_{GS} - V_t$  of M7 = 200mV

$$\frac{W}{L} = \frac{2I_{D7}}{K'_n(V_{GS7} - V_t)^2} = \frac{2 \cdot 100\mu A}{200\mu A/V \cdot 0.2V^2} = \frac{25}{1}$$

N.B. M8 will also need to be dimensioned such that M7 is in saturation.

(iv) What is the open-loop gain of the circuit?

Loop Gain = Gain of diff. amp X gain of source follower

$$A_{diffamp} = -\frac{g_{m2}}{g_{ds2} + g_{ds4}}$$

$$g_{m2} = \frac{2I_{D2}}{V_{GS2} - V_t} = \frac{2 \times 100\mu A}{0.25} = 0.8mA/V$$

$$g_{ds2} = \lambda I_{D2} = \frac{0.04}{1} \times 100\mu A = 4\mu A/V$$

$$A_{diffamp} = -\frac{g_{m2}}{g_{ds2} + g_{ds4}} = -\frac{0.8mA/V}{4\mu A/V + 4\mu A/V} = -100 = 40dB$$

$$A_{sf} = -\frac{g_{m7}R_L}{1 + g_{m7}R_L}$$

$$g_{m7} = \frac{2I_{D7}}{V_{GS7} - V_t} = \frac{2 \times 100\mu A}{0.2} = 1mA/V$$

$$A_{sf} = \frac{g_{m7}R_L}{1 + g_{m7}R_L} = \frac{1mA/V \times 12k\Omega}{1 + 1mA/V \times 12k\Omega} = 0.92 = -0.7dB$$

$$A_{loop} = 40dB - 0.7dB = 39.3dB$$

(v) What is the effect on the circuit if the reference resistor is reduced from 12kΩ to 3kΩ?

This will increase  $V_{GS7} - V_{GS} - V_t$  of M7 will double

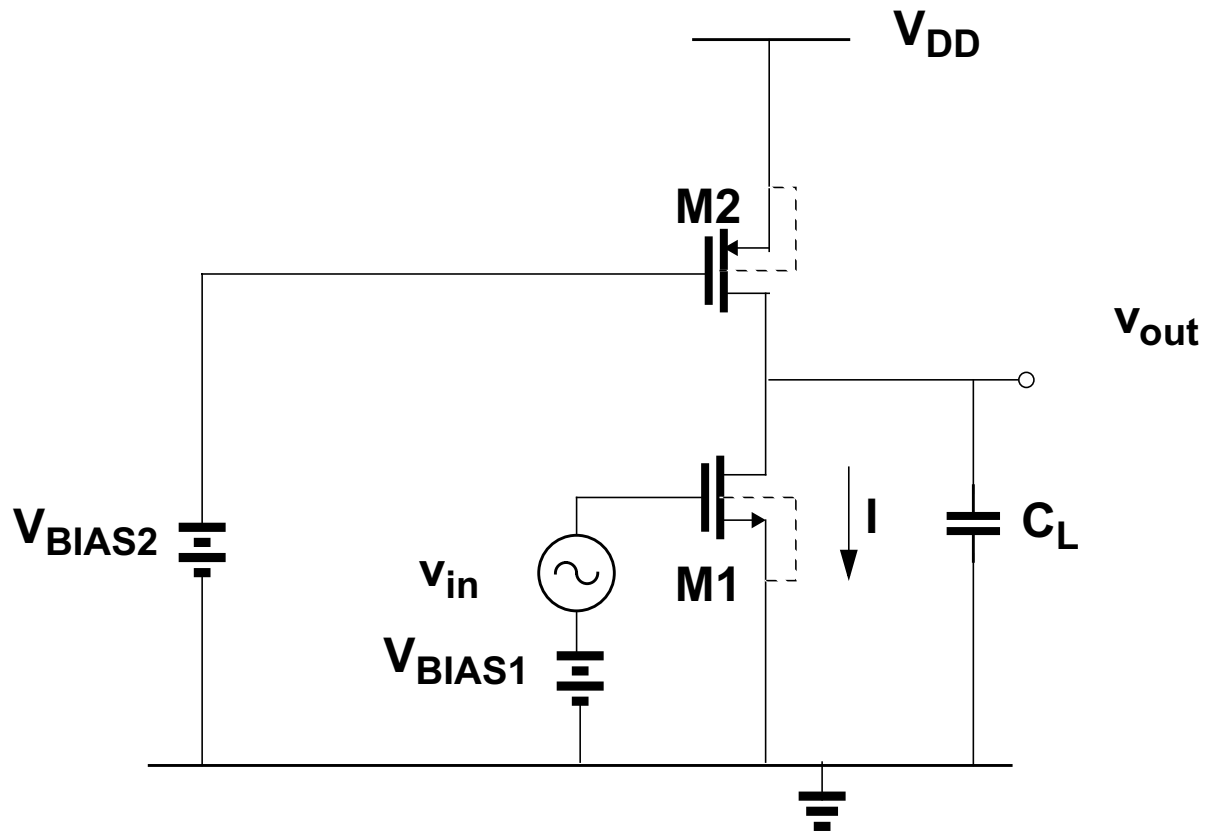
As long as the opamp still has a high gain i.e. if M4 is still in saturation (it is), then there will still be about 1.2V at the gate of M2.

However the extra 200mV  $V_{GS7}$  will introduce an offset.

Approx. 200mV divided by the Loop Gain will appear at the gate of M2 (about 2mV), so an error of about 0.17% in the output current.

Alternatively increase W/L M7 by 4.

## Problem P236. CS stage with active load, h.f. analysis



$$V_{BIAS1}=1.3, V_{BIAS2}=1.7, V_{DD}=3$$

$$V_{tn}=0.8V, V_{tp}=-0.8V,$$

$$\lambda_p=0.04/L \text{ V}^{-1}, \lambda_n=0.04/L \text{ V}^{-1}$$

$$K_n'=160\mu\text{A/V}, K_p'=40\mu\text{A/V}$$

$$W_1=10, L_1=1, W_2=40, L_2=1$$

$$C_L=1\text{pF}$$

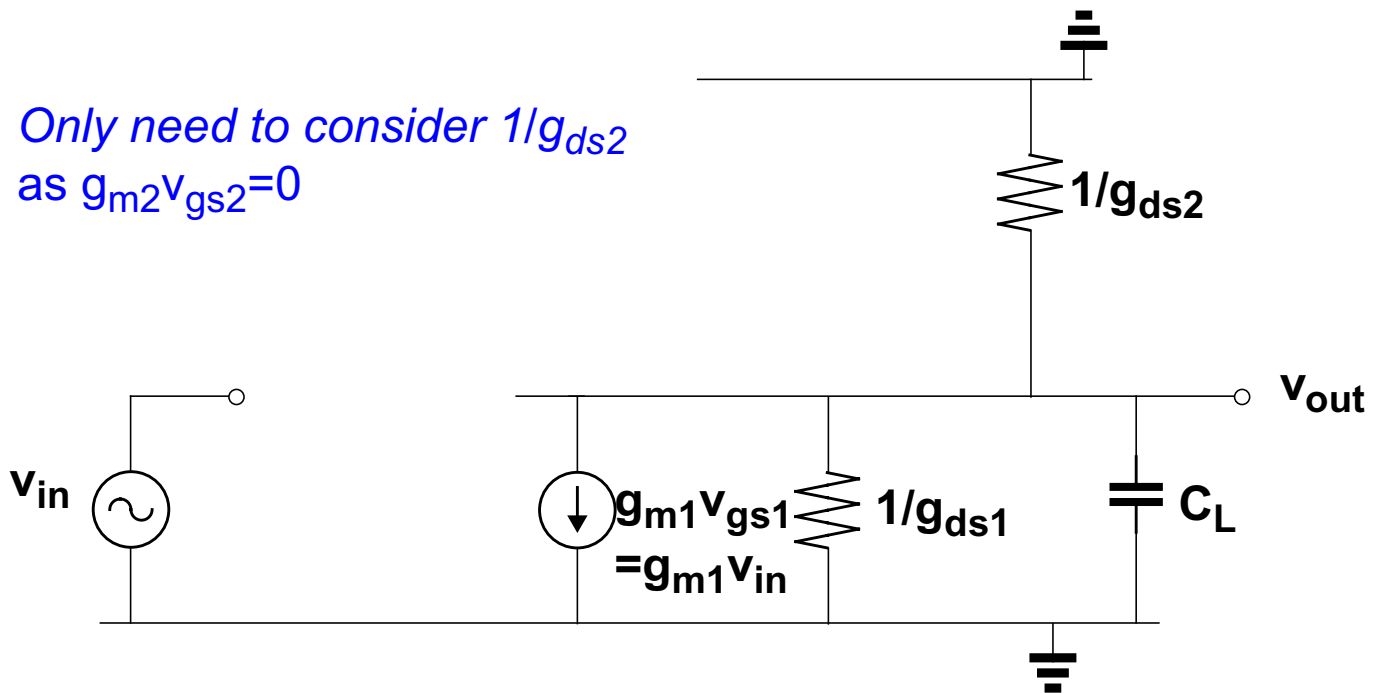
Assume all transistors are in saturation.

Ignore all capacitances except  $C_L$

- (i) Draw the small-signal model
- (ii) Derive an expression for the gain in terms of the small-signal parameters and the load capacitance
- (iii) What is the pole frequency?
- (iv) What is the GBW?
- (v) What is the effect on the gain, pole frequency and GBW if the bias current is doubled?

## Solution Common Source HF Problem P236

(i) Draw the small-signal model



(ii) Derive an expression for the gain in terms of the small-signal parameters and the load capacitance

KCL at output node

$$g_{m1}v_{in} + v_{out}g_{ds1} + v_{out}g_{ds2} + v_{out}sC_L = 0$$

$$g_{m1}v_{in} = -(g_{ds1} + g_{ds2} + sC_L)v_{out}$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2} + sC_L}$$

$$\frac{v_{out}}{v_{in}} = \underbrace{-\frac{g_{m1}}{g_{ds1} + g_{ds2}}}_{\text{LF gain}} \cdot \underbrace{\frac{1}{\left(1 + \frac{sC_L}{g_{ds1} + g_{ds2}}\right)}}_{-1/\text{pole freq.}}$$

(iii) What is the pole frequency?

$$|\omega_p| = \frac{g_{ds1} + g_{ds2}}{C_L}$$

$$g_{ds1} = \lambda_n I_D$$

$$I_{D1} = \frac{K'_n W}{2L} (V_{GS1} - V_t)^2 = \frac{160 \mu A/V^2}{2} \frac{10}{1} (1.3 - 0.8)^2 = 200 \mu A$$

$$g_{ds1} = \lambda_n I_D = 0.04 V^{-1} \times 200 \mu A = 8 \mu A/V$$

$$g_{ds2} = \lambda_p I_D = 0.04 V^{-1} \times 200 \mu A = 8 \mu A/V$$

$$|\omega_p| = \frac{g_{ds1} + g_{ds2}}{C_L} = \frac{8 \mu A/V + 8 \mu A/V}{1 pF} = 16 Mrad/s$$

(iv) What is the GBW

$$GBW = A_o |\omega_p|$$

$$A_o = \frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

$$|\omega_p| = \frac{g_{ds1} + g_{ds2}}{C_L}$$

$$GBW = A_o |\omega_p| = \frac{g_{m1}}{g_{ds1} + g_{ds2}} \cdot \frac{g_{ds1} + g_{ds2}}{C_L} = \frac{g_{m1}}{C_L}$$

$$g_{m1} = \sqrt{2 K'_n \frac{W}{L} I_D} = \sqrt{2 \times 160 \mu A/V \times \frac{10}{1} \times 200 \mu A} = 800 \mu A/V$$

Alternatively

$$g_{m1} = \frac{2I_D}{(V_{GS1} - V_{tn})} = \frac{2 \times 100 \mu A}{0.25} = 800 \mu A/V$$

$$GBW = \frac{g_{m1}}{C_L} = \frac{800 \mu A/V}{1 pF} = 800 Mrad/s$$

(v) What is the effect on the gain, pole frequency and GBW if the bias current is doubled?

*Note: for bias current to be doubled, assume bias voltages changed.*

$$A_o = \frac{g_{m1}}{g_{ds1} + g_{ds2}} \quad \left. \begin{array}{l} g_{m1} \propto \sqrt{I_D} \\ g_{ds} \propto I_D \end{array} \right\} \Rightarrow A_o \propto \frac{1}{\sqrt{I_D}}$$

i.e goes down by  $\sqrt{2}$

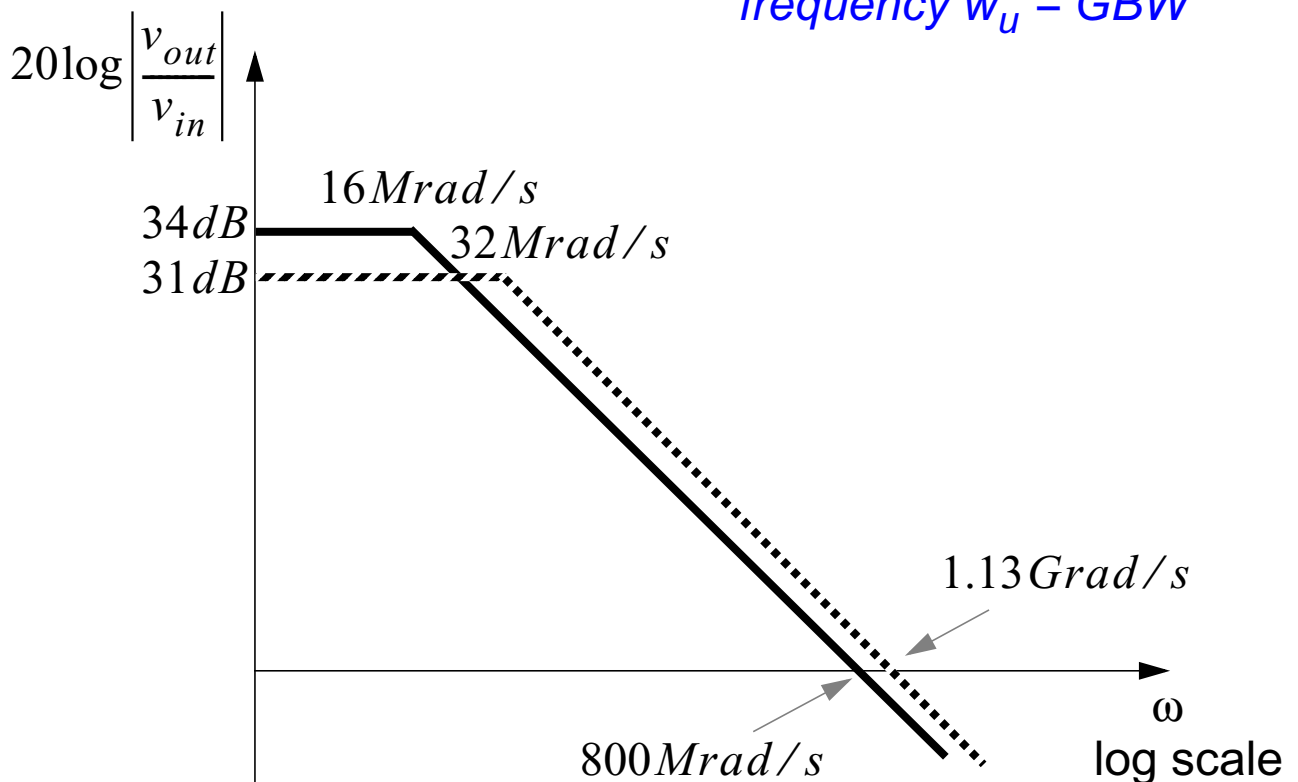
$$|\omega_p| = \frac{g_{ds1} + g_{ds2}}{C_L} \Rightarrow \omega_p \propto I_D$$

i.e goes up by 2

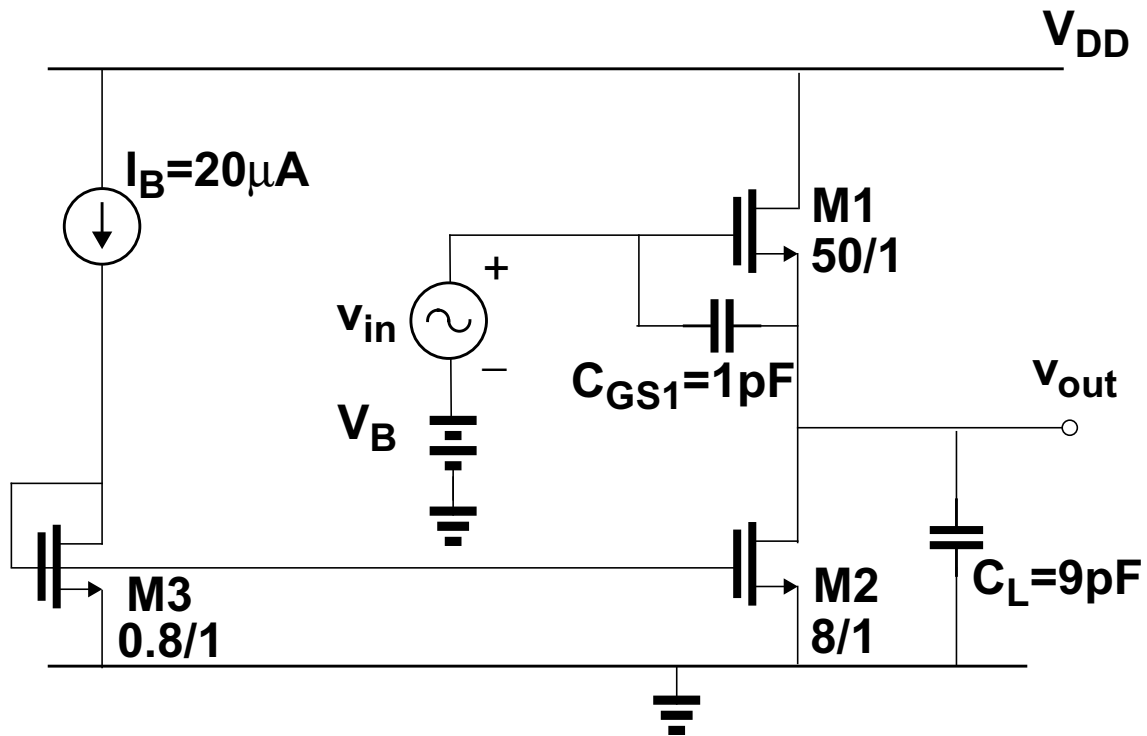
$$GBW = \frac{g_{m1}}{C_L} \Rightarrow GBW \propto \sqrt{I_D}$$

i.e goes up by  $\sqrt{2}$

*Note: Unity gain frequency  $\omega_u = GBW$*



## Problem P237: Source follower stage, h.f. analysis



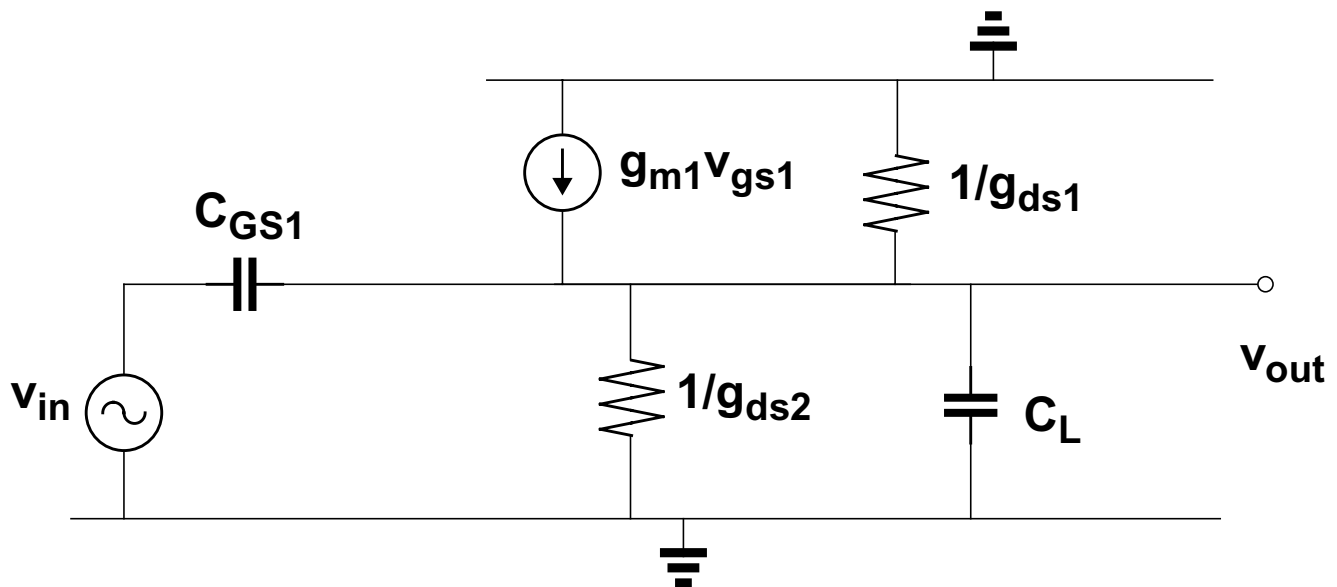
Take  $K_n' = 200 \mu\text{A}/\text{V}^2$ .

Assume all transistors are in saturation and  $g_{m1}, g_{m2} \gg g_{ds1}, g_{ds2}$ .

- Draw the small-signal equivalent circuit for the source follower stage shown.
- Derive an expression for the high-frequency transfer function.
- Calculate the dc gain in dB, and the break frequencies (i.e. pole and/or zero frequencies).
- Draw a Bode diagram of the gain response.

What is the value of gain at frequencies well above the break frequencies?

- (i) Draw the small-signal equivalent circuit for the source follower stage shown in Figure 3.



- (ii) Derive an expression for the high frequency transfer function.

$$v_{gs1} = v_{in} - v_{out}$$

KCL at output node

$$(v_{in} - v_{out})sC_{gs1} + g_{m1}(v_{in} - v_{out}) - (v_{out}g_{ds1}) - (v_{out}g_{ds2}) - v_{out}sC_L = 0$$

$$(g_{m1} + sC_{gs1})v_{in} = (g_{m1} + g_{ds1} + g_{ds2} + sC_{gs1} + sC_L)v_{out}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1} + sC_{gs1}}{g_{m1} + g_{ds1} + g_{ds2} + sC_{gs1} + sC_L}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1} + g_{ds2}} \frac{\left(1 + \frac{sC_{gs1}}{g_{m1}}\right)}{\left(1 + \frac{s(C_{gs1} + C_L)}{g_{m1} + g_{ds1} + g_{ds2}}\right)}$$



(iii) Calculate the dc gain in dB, and the break frequencies (i.e. pole and/or zero frequencies).

DC gain given by

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1} + g_{ds2}} \approx 1 = \underline{\underline{0dB}}$$

Pole frequency given by

$$|\omega_p| = \frac{g_{m1} + g_{ds1} + g_{ds2}}{(C_{gs1} + C_L)} \approx \frac{g_{m1}}{(C_{gs1} + C_L)}$$

$$W_3/L_3 = 10W_2/L_2 \Rightarrow I_{D2} = 10I_{D1}$$

$$g_{m1} = \sqrt{2K'_p \frac{W}{L} I_D} = \sqrt{2 \times 200\mu A/V \times \frac{50}{1} \times 200\mu A} = 2000\mu A/V$$

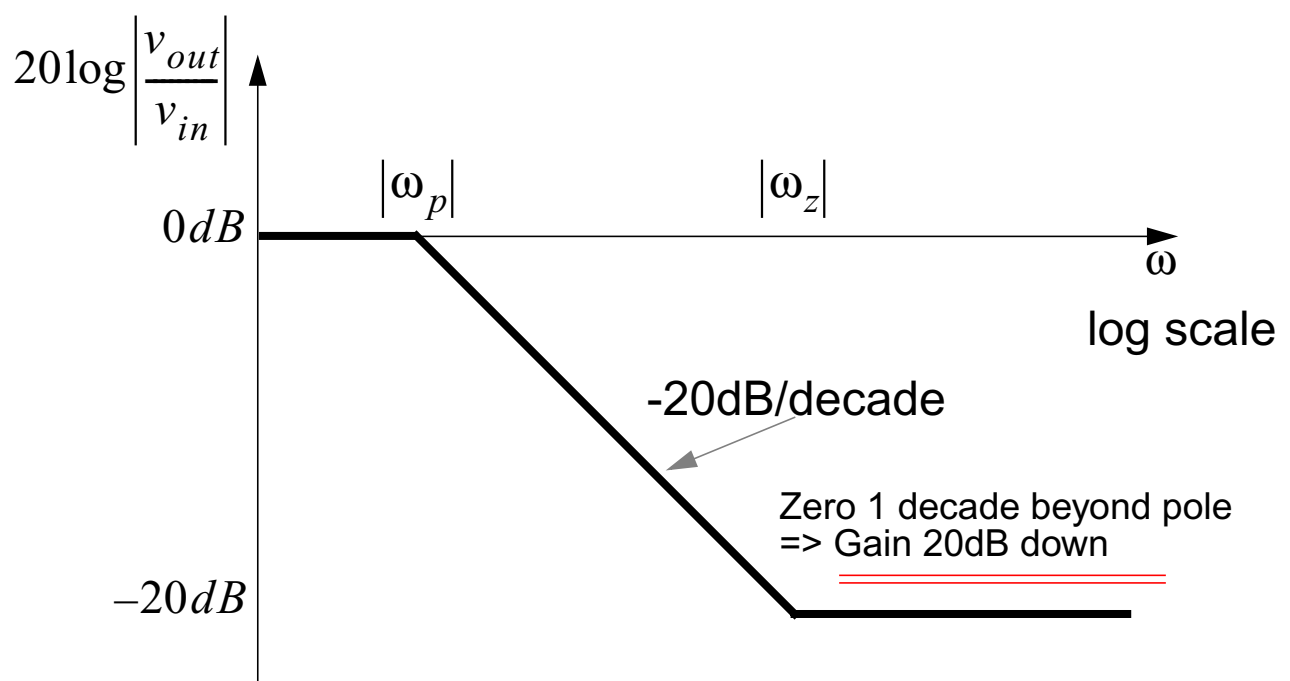
$$|\omega_p| \approx \frac{2000\mu A/V}{1pF + 9pF} = \underline{\underline{200Mrad/s}}$$

Zero frequency given by

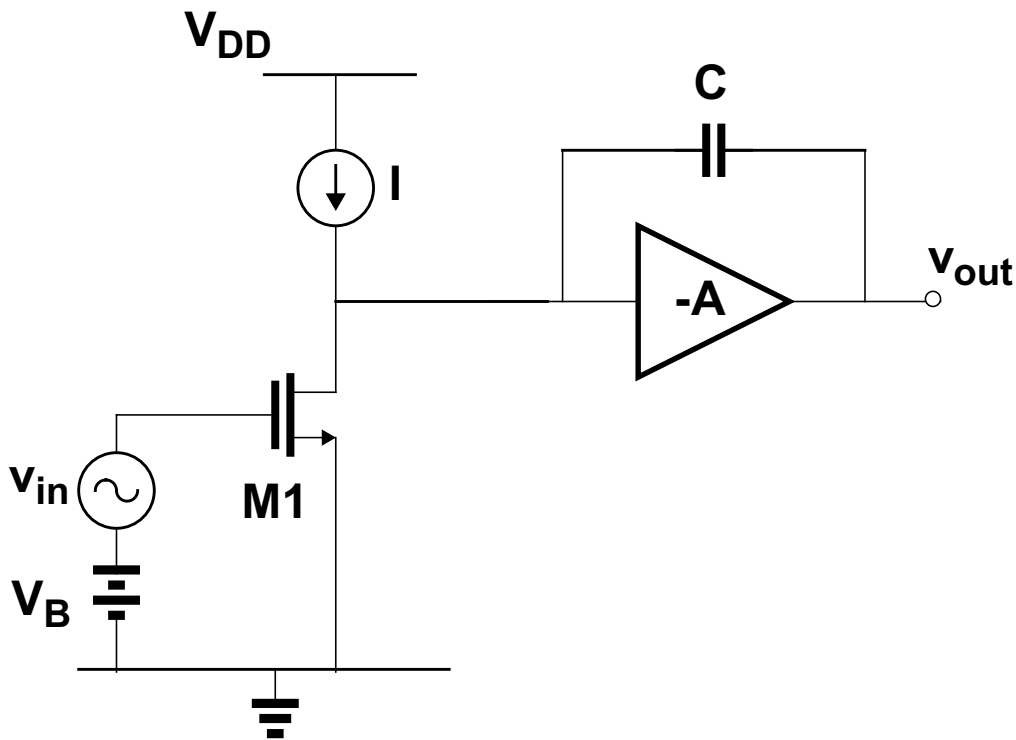
$$|\omega_z| = \frac{g_{m1}}{C_{gs1}} = \frac{2000\mu A/V}{1pF} = \underline{\underline{2Grad/s}}$$

(iv) Draw a Bode diagram of the gain response.

What is the value of gain at frequencies well above the break frequencies?



## Problem P241: Miller capacitance.



A gain stage is cascaded with an ideal amplifier with gain  $-A$ . Assume M1 is in saturation.

- Write an expression for the small-signal low-frequency voltage gain ( $v_{out}/v_{in}$ ) of this circuit.
- Write an expression for the frequency of the dominant pole
- Calculate the small-signal voltage gain, and the pole frequency if  
 $W/L$  of M1 = 25/1,  $V_B = 1V$ ,  $V_{tn} = 0.75V$ ,  $K_n' = 200\mu A/V^2$ ,  $\lambda_n = 0.04V^{-1}$   
 $A = -100$ ,  $C = 1pF$ .

---

**Problem: Miller capacitance.**

- (i) Write an expression for the small-signal low-frequency voltage gain ( $v_{out}/v_{in}$ ) of this circuit.

Gain is the product of the gain of the common-source stage and the gain of the ideal amplifier

$$Gain = -\frac{g_{m1}}{g_{ds1}} \cdot -A = A \frac{g_{m1}}{g_{ds1}}$$

- (ii) Write an expression for the frequency of the dominant pole

Assuming an ideal amplifier (i.e. with low output impedance), the dominant pole is at the output of the common-mode stage

The pole frequency is given by conductance at the output of the gain stage divided by the capacitance seen at this node.

The conductance is equal to  $g_{ds1}$

The capacitance seen at this node is  $(1 + A)C$

(from the Miller approximation)

The pole frequency is then given by

$$|\omega_p| = \frac{g_{ds1}}{(1 + A)C_1}$$

(iii) Calculate the small-signal voltage gain, and the pole frequency if

$W/L$  of  $M1 = 25/1$ ,  $V_B = 1V$ ,  $V_{tn} = 0.75V$ ,  $K_n' = 200\mu A/V^2$ ,  $\lambda_n = 0.04V^{-1}$   
 $A = -100$ ,  $C = 1pF$ .

$$I_{D1} = \frac{K_n' W}{2L} (V_{GS1} - V_t)^2 = \frac{200\mu A/V^2}{2} \frac{25}{1} (1 - 0.75)^2 = 156\mu A$$

$$g_{m1} = \frac{2I_{D1}}{(V_{GS1} - V_{tn})} = \frac{2 \times 156\mu A}{1 - 0.75} = 1250\mu A/V$$

$$g_{ds1} = \lambda I_{D1} = 0.04V^{-1} \times 156\mu A = 6.25\mu A/V$$

Low-frequency gain given by

$$\frac{v_{out}}{v_{in}} \cong A \frac{g_{m1}}{g_{ds1}} = 100 \frac{1248\mu A/V}{6.2\mu A/V} = 20^3 = 86dB$$

Pole frequency given by

$$|\omega_p| = \frac{g_{ds1}}{(1 + A)C_1} = \frac{6.25\mu A/V}{(1 + 100)100pF} = 619rad/s$$



---

### Problem P. 264 - Stability and feedback factor

An amplifier has the following 3 pole transfer function

$$A(s) = \frac{A_o}{\left(1 - \frac{s}{\omega_{p1}}\right)\left(1 - \frac{s}{\omega_{p2}}\right)\left(1 - \frac{s}{\omega_{p3}}\right)}$$

$$A_o = 10^4 \text{ (80dB)}$$

$$\omega_{p1} = 1 \text{ Mrad/s}$$

$$\omega_{p2} = 100 \text{ Mrad/s}$$

$$\omega_{p3} = 1 \text{ Grad/s}$$

(i) Draw the Bode diagram for the gain

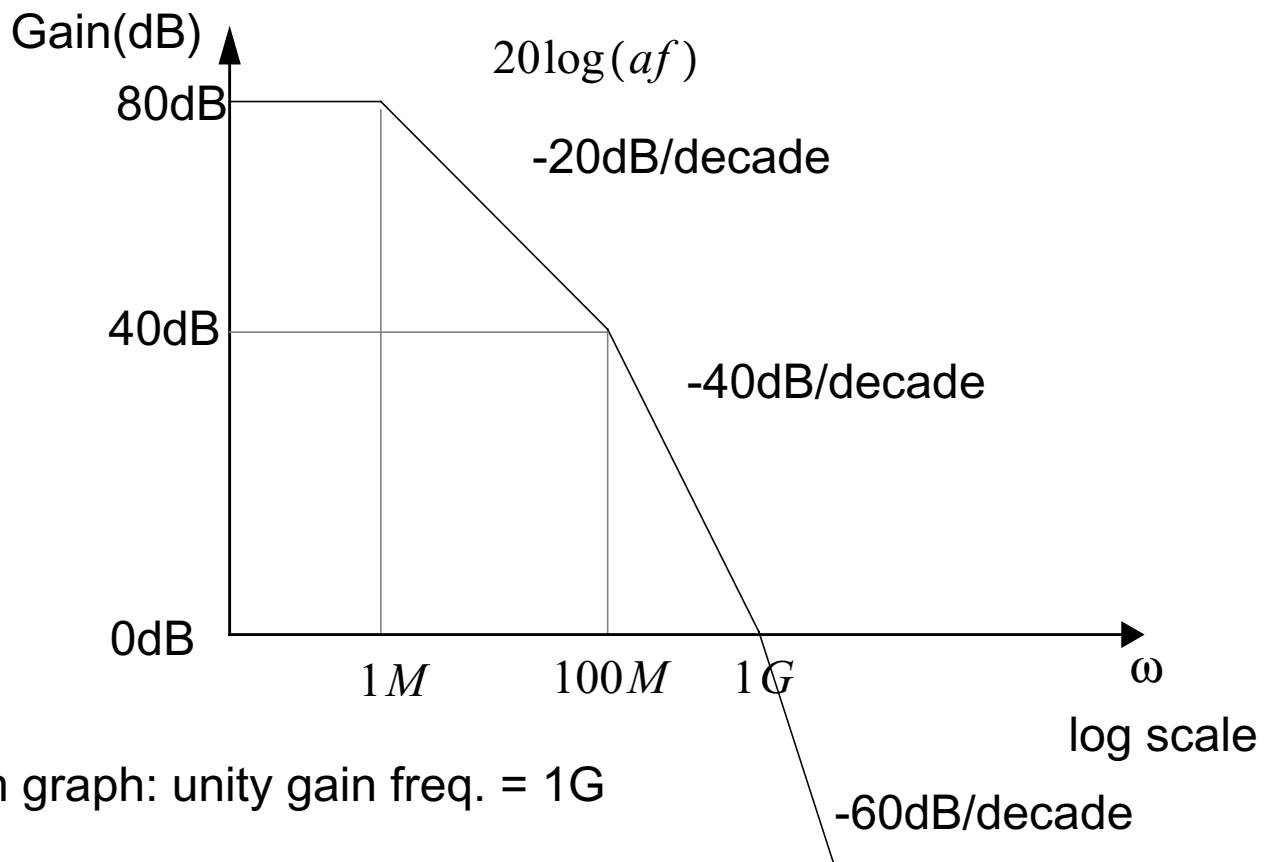
(ii) If this amplifier is used in a unity gain feedback configuration, what is the phase margin?

(iii) If the feedback factor is reduced to 0.1 what is the phase margin?

## Problem P. 255 Feedback and stability

(i) Bode diagram for the gain

If feedback factor  $f=1$  then loop gain = open loop gain



From graph: unity gain freq. = 1G

(ii) If this amplifier is used in a unity gain feedback configuration, what is the phase margin?

If feedback factor  $f=1$  then loop gain = open loop gain

Phase Margin:

Difference between the phase shift at unity gain frequency and  $180^\circ$

$$Phase_{\omega = \omega_u} = -\operatorname{atan}\left(\frac{\omega_u}{\omega_{p1}}\right) - \operatorname{atan}\left(\frac{\omega_u}{\omega_{p2}}\right) - \operatorname{atan}\left(\frac{\omega_u}{\omega_{p3}}\right)$$

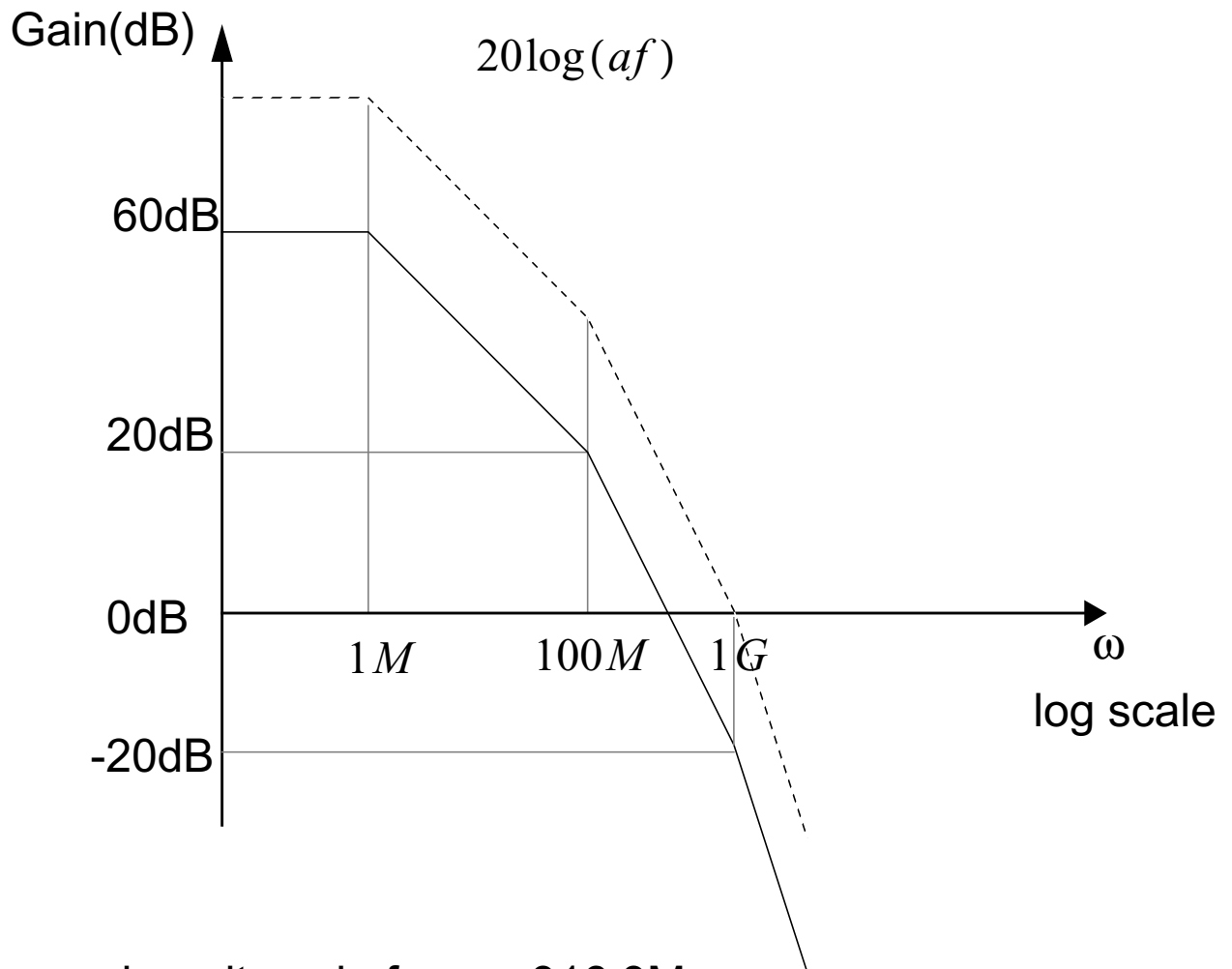
$$Phase_{\omega = \omega_u} = -\operatorname{atan}\left(\frac{1G}{1M}\right) - \operatorname{atan}\left(\frac{1G}{100M}\right) - \operatorname{atan}\left(\frac{1G}{1G}\right)$$

$$Phase_{\omega = \omega_u} = -90 - 84 - 45 = -219$$

$$PM = -39 \quad \Rightarrow \text{Unstable}$$

(iii) If the feedback factor is reduced to 0.1 what is the phase margin?

Reduce feedback factor to 0.1 i.e. move  $af$  down 20dB



From graph: unity gain freq. =  $316.3M$

$$Phase_{\omega = \omega_u} = -\text{atan}\left(\frac{316M}{1M}\right) - \text{atan}\left(\frac{316M}{100M}\right) - \text{atan}\left(\frac{316M}{1G}\right)$$

$$Phase_{\omega = \omega_u} = -90 - 72.5 - 17.5 = 0 - 180$$

$$PM = 0$$

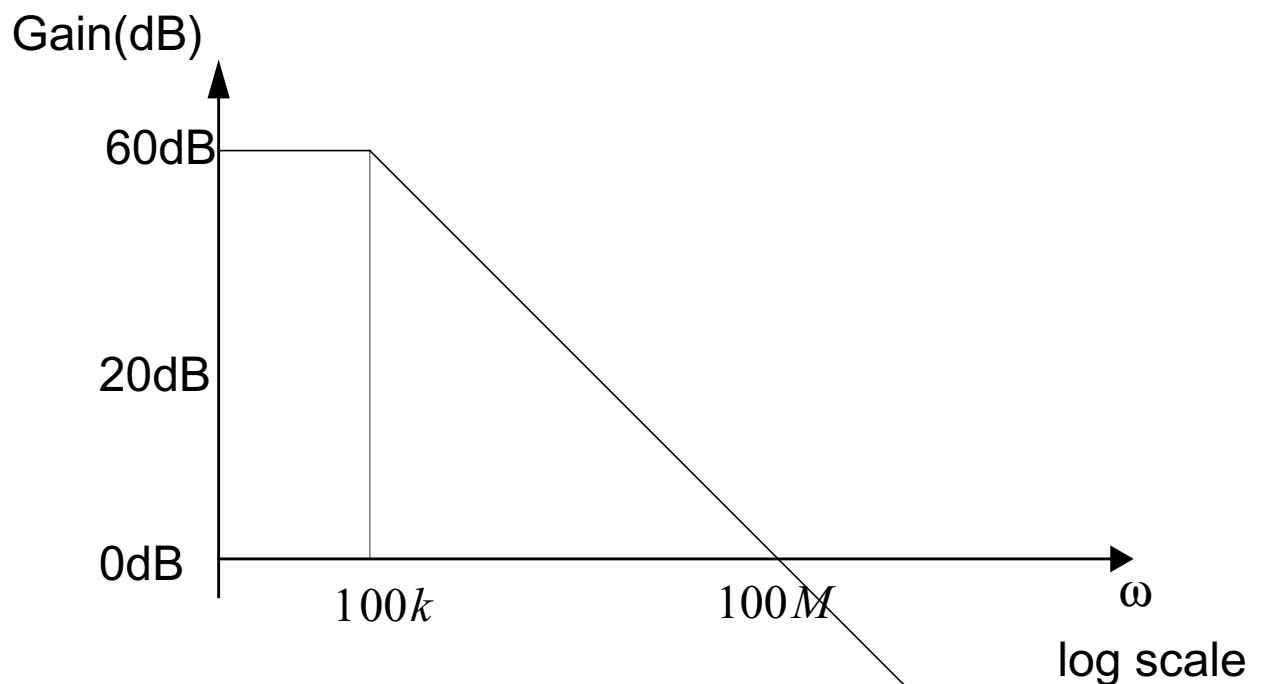
Marginally stable

Reduce  $f$  another 20dB: unity gain freq =  $100M \Rightarrow PM = 45^\circ$

Note: these are approximate values



Example: First order system, Gain = 60dB, BW = 100k, GBW = 100M



What is effect of second pole at GBW,  $0.5 \cdot \text{GBW}$ ,  $2 \cdot \text{GBW}$  if system is used in unity gain configuration?

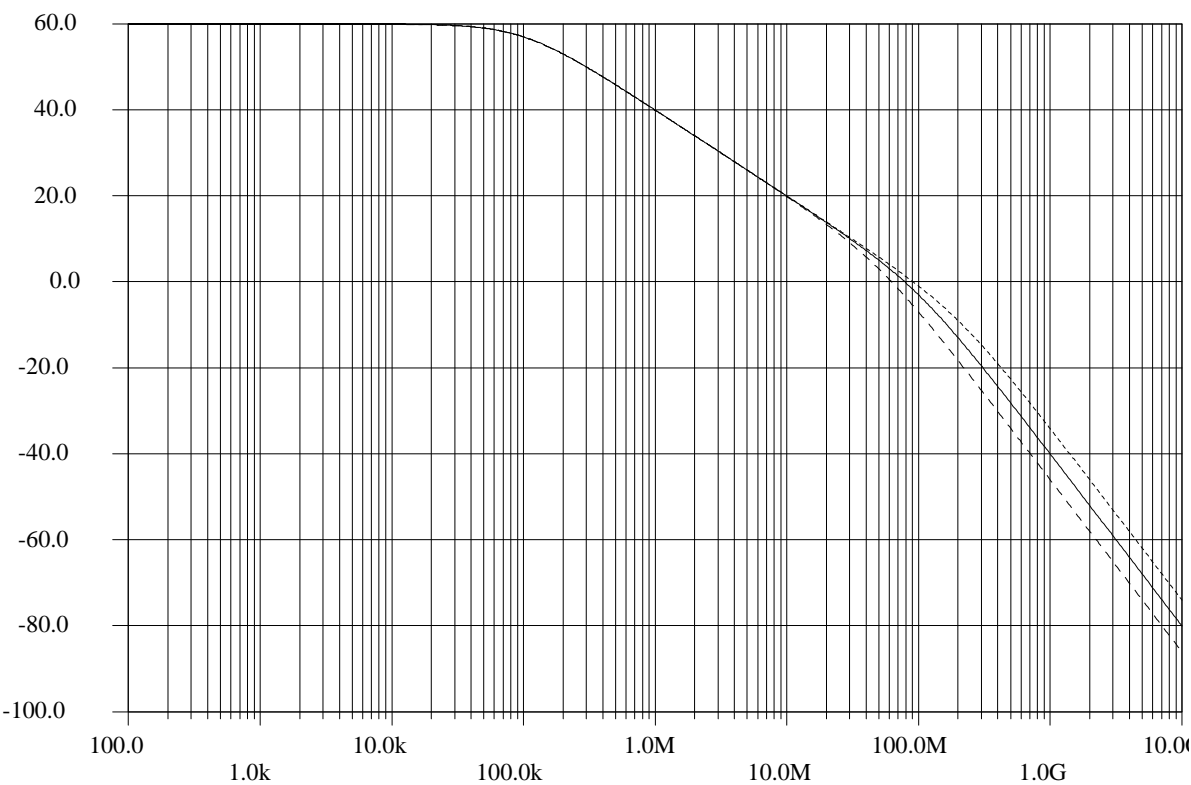
Note: Using the Bode approximation this would give us PM's of  $45^\circ$ ,  $26.6^\circ$  and  $63^\circ$  respectively.

The following plots give  $51.9^\circ$ ,  $38.7^\circ$  and  $65.5^\circ$  respectively due to the gain curve being 3dB lower at the second pole compared with the Bode approximation, i.e. the unity gain frequency occurs earlier.

# Open-loop response:

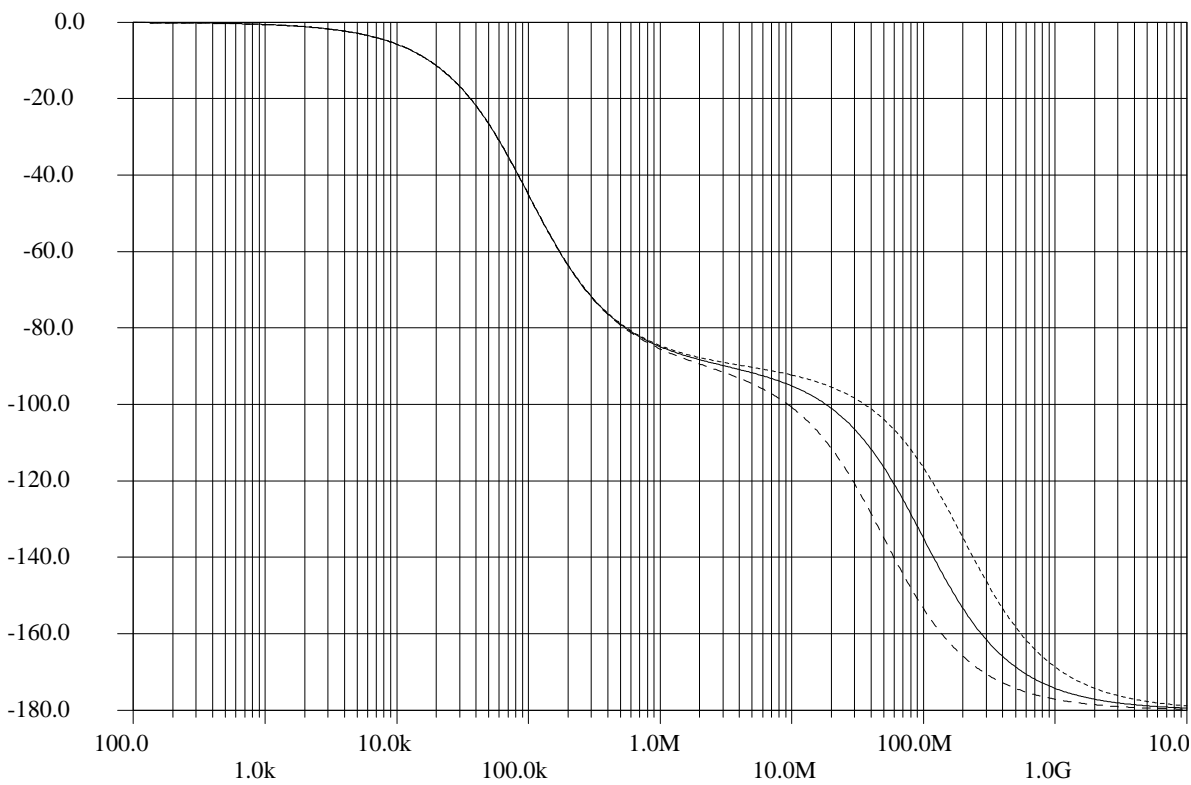
- y1-axis -  
DB(VN(OUT2P))

- Subvar -  
(0) ———  
WP2: 100.0M  
(1) - - - - -  
WP2: 50.0M  
(2) - - - - -  
WP2: 200.0M

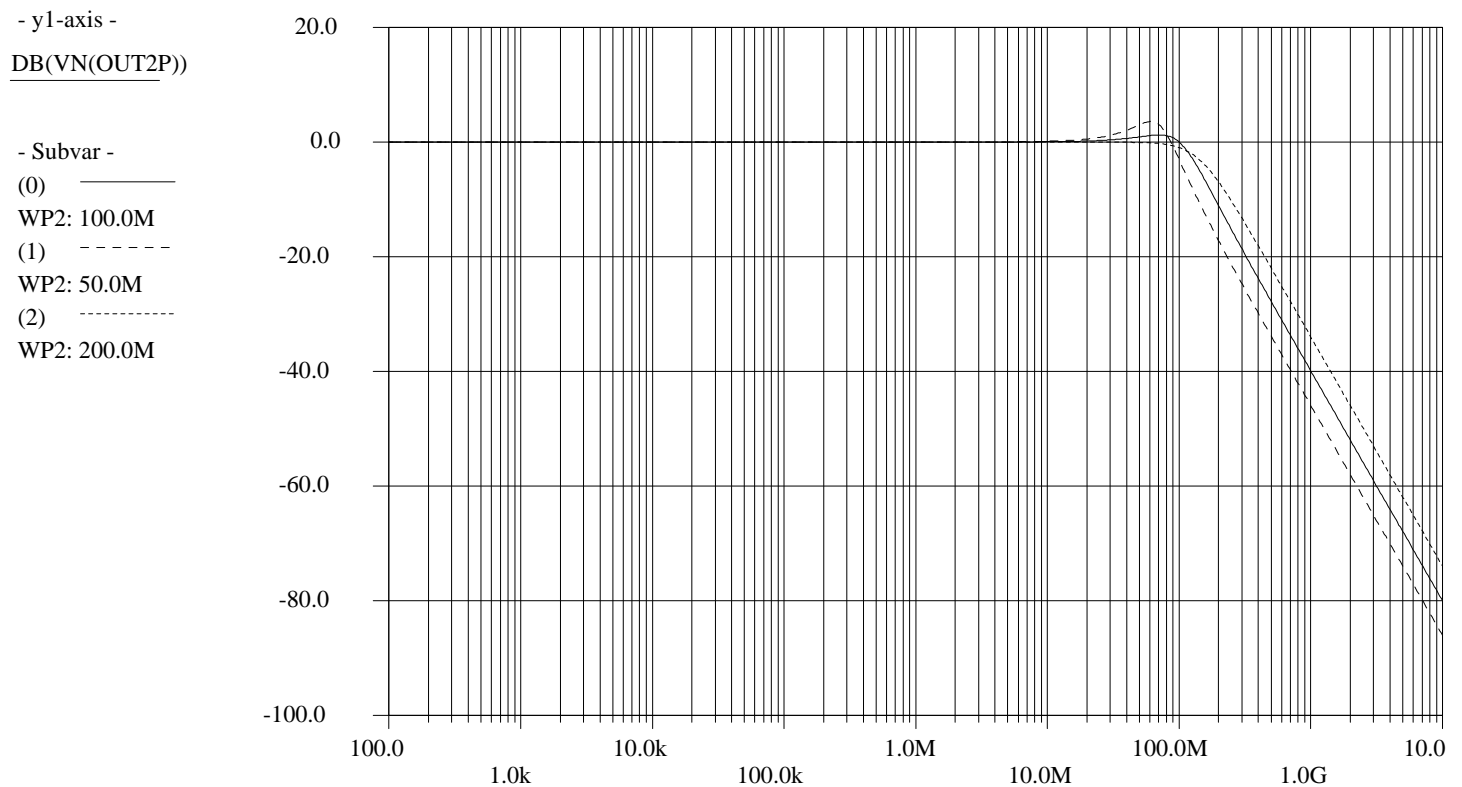


- y1-axis -  
PHA(VN(OUT2P))

- Subvar -  
(0) ———  
WP2: 100.0M  
(1) - - - - -  
WP2: 50.0M  
(2) - - - - -  
WP2: 200.0M

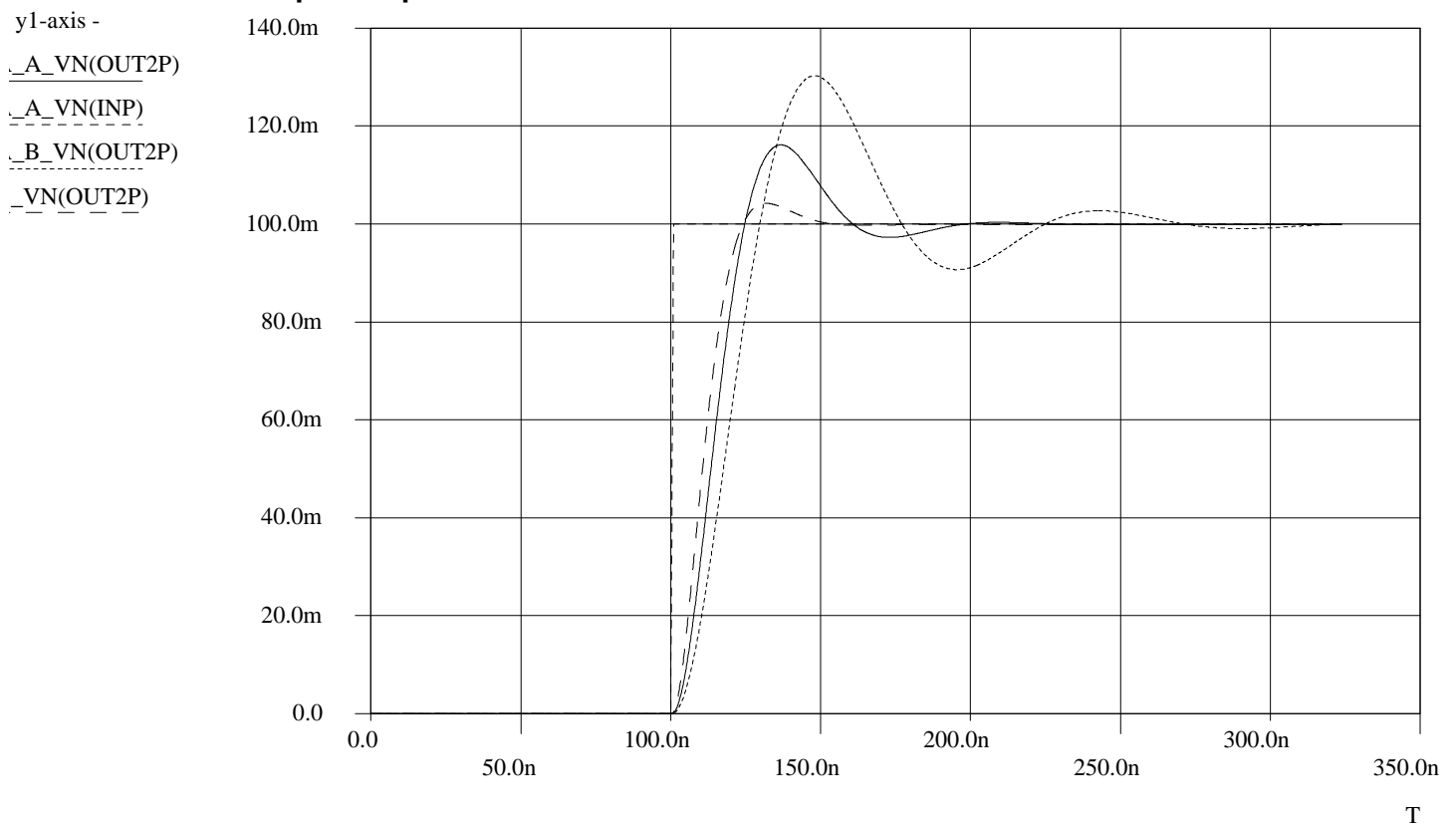


## Closed-loop response:



Note peaking in closed loop response

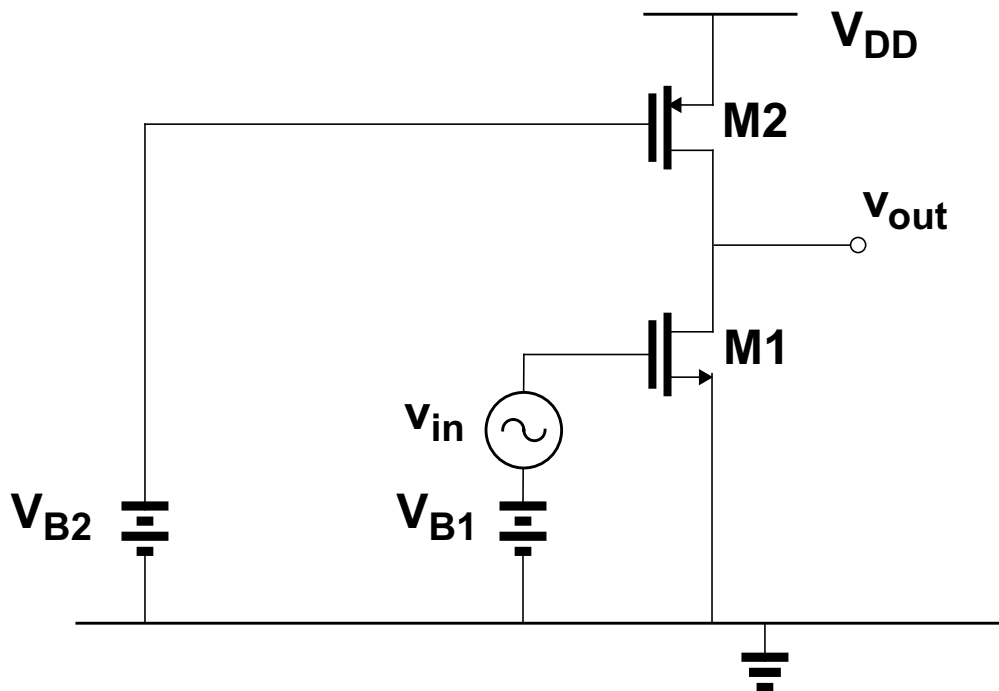
## Transient Step response:



Note overshoot in transient step response



## Problem P 321: CS with active load noise analysis



Assume M1 and M2 are operating in saturation. Only thermal noise sources need be considered.

For calculations take Boltzmann's constant  $k=1.38 \times 10^{-23} \text{ J/}^\circ\text{K}$ , temperature  $T=300^\circ\text{K}$ .

(i) Draw the small-signal model for the circuit shown.

What is the low-frequency small-signal voltage gain ( $v_{\text{out}}/v_{\text{in}}$ ) in terms of the small-signal parameters of M1 and M2?

(ii) What is the input-referred thermal noise voltage density of M1? What is the input-referred thermal noise voltage density of M2?

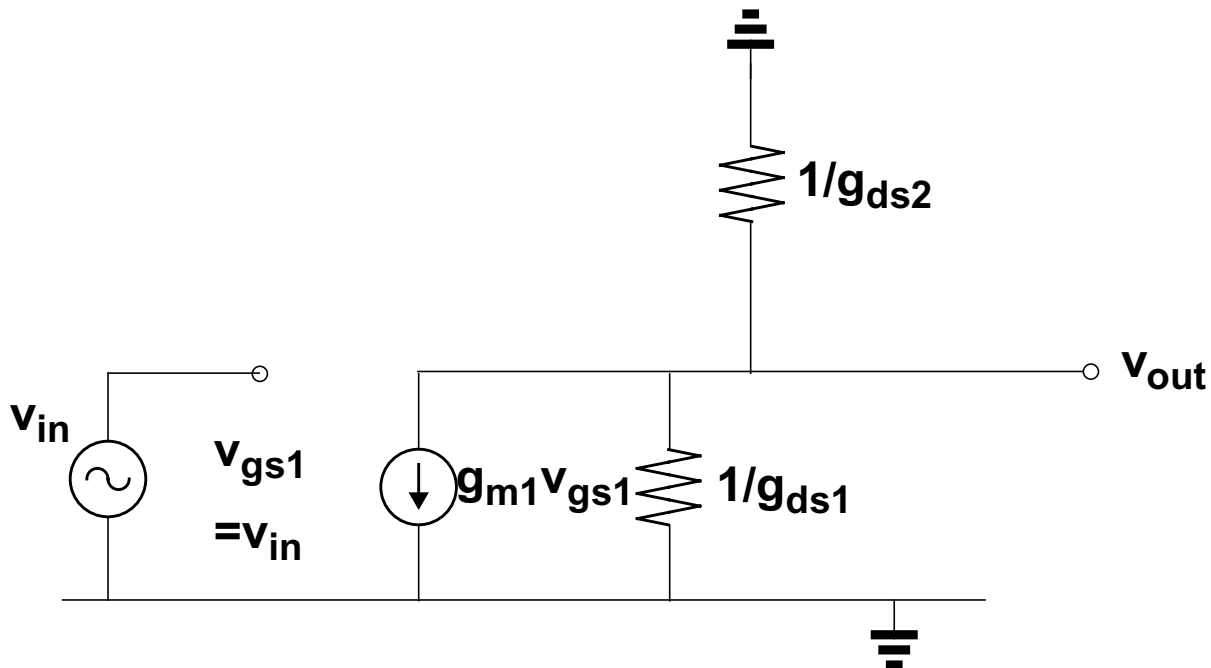
Answers should be in terms of the small-signal parameters of M1 and M2, Boltzmann's constant  $k$  and temperature  $T$ .

(iii) Calculate the input-referred thermal noise voltage density of M1 and the input-referred thermal noise voltage density of M2 if  $V_{B1}=1.0\text{V}$ ,  $V_{B2}=1.25\text{V}$ ,  $V_{DD}=3\text{V}$ ,  $V_{tn} = 0.75\text{V}$ ,  $V_{tp} = -0.75\text{V}$ ,  $\lambda_n=\lambda_p=0.04\text{V}^{-1}$ . The drain current of M1 is  $100\mu\text{A}$ . Which is the dominant noise source?

(iv) Calculate the total noise voltage at the output over a bandwidth of 1MHz. If the input signal  $v_{\text{in}}$  is a  $1\text{mV}_{\text{rms}}$  sine wave, calculate the signal-to-noise ratio in dB at the output over a bandwidth of 1MHz.

## Solution Problem P 321: CS with active load noise analysis

- (i) Draw the small-signal model for the circuit shown in Figure 4.  
What is the low-frequency small-signal voltage gain ( $v_{out}/v_{in}$ ) in terms of the small-signal parameters of M1 and M2?

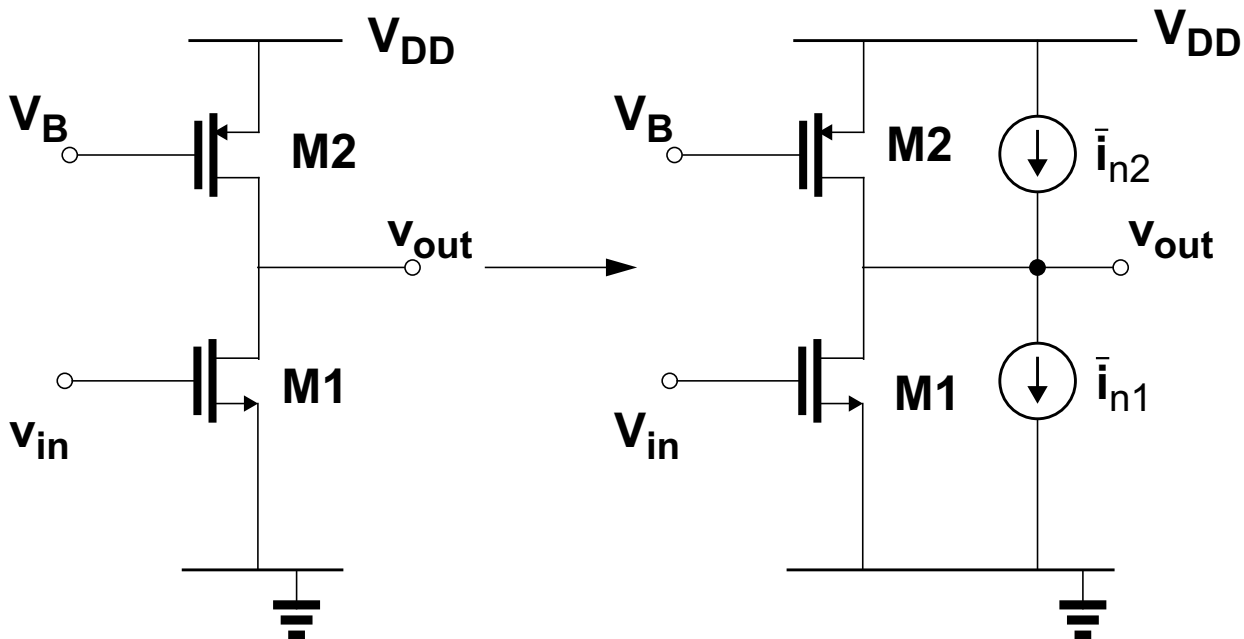


Current at output node

$$g_{m1}v_{in} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

- (ii) What is the input-referred thermal noise voltage density of M1?  
 What is the input-referred thermal noise voltage density of M2?  
 Answers should be in terms of the small-signal parameters of M1 and M2,  
 Boltzmann's constant  $k$  and temperature  $T$ .



Noise current of MOS:

$$\overline{i_n^2} = 4kT\left(\frac{2}{3}g_m\right)$$

Input-referred noise of M1

$$\overline{v_{niM1}} = \frac{\overline{i_{nM1}}}{g_{m1}} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right)}}{g_{m1}} = \sqrt{\frac{4kT\left(\frac{2}{3}\right)}{g_{m1}}} \quad \text{rms noise} \quad V / \sqrt{Hz}$$

Input-referred noise of M2

$$\overline{v_{niM2}} = \frac{\overline{i_{M2}}}{g_{m1}} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m2}\right)}}{g_{m1}} = \sqrt{4kT\left(\frac{2}{3}\frac{g_{m2}}{g_{m1}}\right)} \quad \text{rms noise} \quad V / \sqrt{Hz}$$

(iii) Calculate the input-referred thermal noise voltage density of M1 and the input-referred thermal noise voltage density of M2 if

$$V_{B1}=1.0V, V_{B2}=1.25V, V_{DD}=3V, V_{tn} = 0.75V, V_{tp} = -0.75V, \lambda_n=\lambda_p=0.04V^{-1}.$$

The drain current of M1 is  $100\mu A$ .

Which is the dominant noise source?

$g_m$  given by

$$g_m = \frac{2I_D}{(V_{GS}-V_T)}$$

$$g_{m1} = \frac{2 \cdot 100\mu A}{1V - 0.75V} = 800\mu A/V \quad g_{m2} = \frac{2 \cdot 100\mu A}{1.75V - 0.75V} = 200\mu A/V$$

Input-referred noise of M1

$$\overline{v_{niM1}} = \sqrt{\frac{4kT\left(\frac{2}{3}\right)}{g_{m1}}} = \sqrt{\frac{(4 \cdot 1.38 \times 10^{-23} \cdot 300)\left(\frac{2}{3}\right)}{800\mu A/V}} = \underline{\underline{3.71nV/\sqrt{Hz}}}$$

Input-referred noise of M2

$$\overline{v_{niM2}} = \sqrt{4kT\left(\frac{2}{3} \frac{g_{m2}}{g_{m1}}\right)} = \sqrt{(4 \cdot 1.38 \times 10^{-23} \cdot 300)\left(\frac{2}{3}\right) \cdot \frac{200\mu A/V}{800\mu A/V^2}} = \underline{\underline{1.86nV/\sqrt{Hz}}}$$

M1 is dominant noise source



(iv) Calculate the total noise voltage at the output over a bandwidth of 1MHz.

If the input signal  $v_{in}$  is a  $1mV_{rms}$  sine wave, calculate the signal-to-noise ratio in dB at the output over a bandwidth of 1MHz.

$$g_{ds1} = \lambda_n I_D = 0.04V^{-1} 100\mu A = 4\mu A/V$$

$$g_{ds2} = \lambda_n I_D = 0.04V^{-1} 100\mu A = 4\mu A/V$$

Gain of stage

$$Gain = -\left(\frac{g_{m1}}{g_{ds1} + g_{ds2}}\right) = -\frac{800\mu A/V}{8\mu A/V} = -100$$

Total input-referred noise

$$\overline{v_{nitot}} = \sqrt{\left[\frac{4kT\left(\frac{2}{3}\right)}{g_{m1}}\right]^2 + \left[4kT\left(\frac{2}{3}\frac{g_{m2}}{g_{m1}}\right)\right]^2}$$

$$\overline{v_{nitot}} = \sqrt{(3.71nV/\sqrt{Hz})^2 + (1.86nV/\sqrt{Hz})^2} = 4.15nV/\sqrt{Hz}$$

Total noise at output given by

$$\overline{v_{notot}} = \overline{v_{nitot}} \cdot \left(\frac{g_{m1}}{g_{ds1} + g_{ds2}}\right) \cdot \sqrt{BW} = 4.15nV/\sqrt{Hz} \cdot 100 \cdot \sqrt{1MHz} = \underline{\underline{415\mu V_{rms}}}$$

Output signal

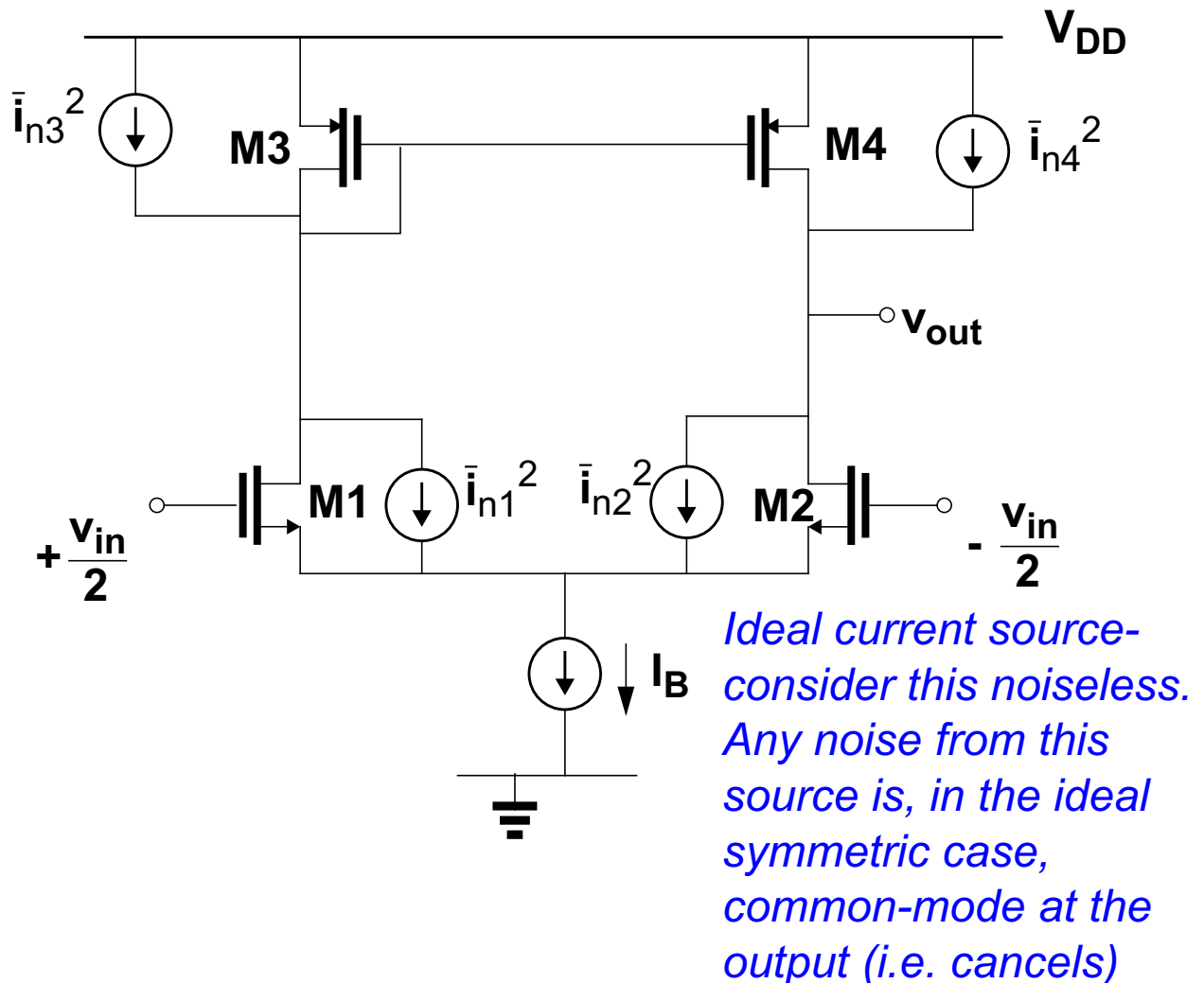
$$v_{out} = -\left(\frac{g_{m1}}{g_{ds1} + g_{ds2}}\right)v_{in} = -\frac{800\mu A/V}{8\mu A/V} \cdot 1mV_{rms} = 100mV_{rms}$$

Signal-to-Noise ratio given by

$$\frac{S}{N} = \frac{100mV}{415\mu V_{rms}} = 241 \quad \text{or } \underline{\underline{47.6 \text{ dB}}}$$

## Problem P. 322(Differential pair noise analysis).

- (i) What is the input-referred thermal noise voltage of the circuit shown in terms of the small signal parameters  $g_m$  and  $g_{ds}$ ?



Total noise current at output is square root of the individual noise currents

$$\overline{i_{nt}} = \sqrt{i_{n1}^2 + i_{n2}^2 + i_{n3}^2 + i_{n4}^2} = \sqrt{4kT\frac{2}{3}(2g_{mn} + 2g_{mp})}$$

where  $g_{mn}/g_{mp}$  are the transconductances of the nmos/pmos transistors

(Note that in calculating the total noise at the output, the noise currents of M1 and M3 are mirrored to the output node)

To refer this back to the input divide by  $g_{mn}$

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_{mn}} = \frac{\sqrt{4kT\frac{2}{3}(2g_{mn} + 2g_{mp})}}{g_{mn}} \quad V/\sqrt{Hz}$$

(ii) Calculate the total noise voltage at the output over a bandwidth of 20kHz.

Use  $g_{mn}=g_{mp}=100\mu A/V$ ,  $g_{dsn}=g_{dsp}=2\mu A/V$

Noise voltage at output is given by input-referred noise multiplied by voltage gain

$$\overline{v_{no}} = \overline{v_{ni}} \frac{g_{mn}}{g_{dsn} + g_{dsp}} = \frac{\sqrt{4kT\frac{2}{3}(2g_{mn} + 2g_{mp})}}{g_{mn}} \frac{g_{mn}}{(g_{dsn} + g_{dsp})}$$

$$= \frac{\sqrt{4kT\frac{2}{3}(2g_{mn} + 2g_{mp})}}{g_{dsn} + g_{dsp}}$$

*Note: This is equal to the total current noise at the output, divided by the output conductance*

$$= \frac{\sqrt{4 \times 1.38 \times 10^{-23} J/K \times 300 K \times \frac{2}{3} (2 \times 100 \mu A/V + 2 \times 100 \mu A/V)}}{2 \mu A/V + 2 \mu A/V}$$
$$= 525 nV / \sqrt{Hz}$$

Total integrated noise over a bandwidth of 20kHz:

$$\overline{v_{no-20kHz}} = 525 nV \cdot \sqrt{20 kHz} = 74.3 \mu V$$

(iii) Calculate the total noise voltage at the output if the output is loaded by a capacitor  $C_L = 1\text{pF}$

Capacitor  $C_L$  connected between the output node and ground  
=> pole at output node given by

$$|f_p| = \frac{g_{dsn} + g_{dsp}}{2\pi C_L}$$

Total noise voltage at the output is given by

$$\overline{v_{nototal}} = \overline{v_{no}} \sqrt{\frac{\pi}{2} f_p}$$

$$\overline{v_{nototal}} = \frac{\sqrt{4kT \frac{2}{3} (2g_{mn} + 2g_{mp})}}{(g_{dsn} + g_{dsp})} \cdot \sqrt{\frac{\pi}{2} \cdot \frac{(g_{dsn} + g_{dsp})}{2\pi C_L}}$$

$$\overline{v_{nototal}} = 525\text{nV} / \sqrt{\text{Hz}} \cdot \sqrt{\frac{2\mu\text{A}/V + 2\mu\text{A}/V}{4 \times 1\text{pF}}}$$

$$\overline{v_{nototal}} = 525\mu\text{V}$$

---

(iv) What is the SNR at the output if the input to the circuit is a differential sine wave of 10mV<sub>rms</sub>? Assume the frequency of the sine-wave is much less than the pole frequency.

The input signal is multiplied by the voltage gain of the circuit to give

Output signal

$$v_{out} = -\frac{g_{m1}}{g_{dsn} + g_{dsp}} v_{in} = -\frac{100\mu}{2\mu + 2\mu} \cdot 10mV_{rms} = 250mV_{rms}$$

Signal-to-Noise ratio at output given by

$$\frac{S}{N} = \frac{250mV}{525\mu V} = 476 \quad \text{or } 53.6\text{dB}$$

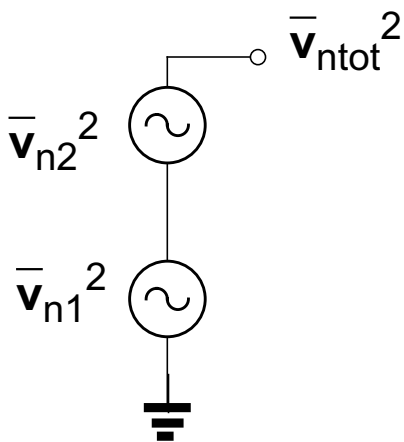
*Note: For optimum SNR, limit the bandwidth to that required for the signal, or employ extra filtering at the output.*

*Note: If the circuit is followed by an A/D converter, the total noise will be aliased into the digital signal.*

## Noise notes (1)

### Uncorrelated sources and dominant sources

For uncorrelated noise sources



$$\overline{v_{ntot}^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2}$$

$$\overline{v_{ntot}} = \sqrt{\overline{v_{n1}^2} + \overline{v_{n2}^2}}$$

i.e. r.m.s. sum

### Example

$$\overline{v_{n1}} = 10\mu V$$

$$\overline{v_{n2}} = 5\mu V$$

1. What is the total rms value?

$$\overline{v_{ntot}} = \sqrt{10^2 + 5^2} = 11.2\mu V$$

2. How to keep the total value below  $10\mu V$ ?

Either eliminate  $\overline{v_{n2}}$

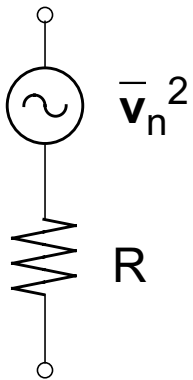
or reduce  $\overline{v_{n1}}$  to

$$\overline{v_{n1}} = \sqrt{10^2 - 5^2} = 8.7\mu V$$

i.e. concentrate on the largest or **dominant** noise source

## Noise notes (2)

### Resistor Noise



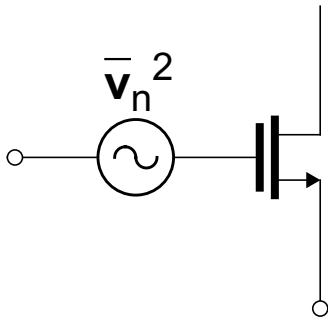
$$\overline{v_n} = \sqrt{4kTR} \quad V / \sqrt{Hz}$$

1k $\Omega$  resistor:  $\overline{V_n}=4nV/\sqrt{rt(Hz)}$  at 300°K

100k $\Omega$  resistor:  $\overline{V_n}=40nV/\sqrt{rt(Hz)}$  at 300°K

f

### MOS thermal noise

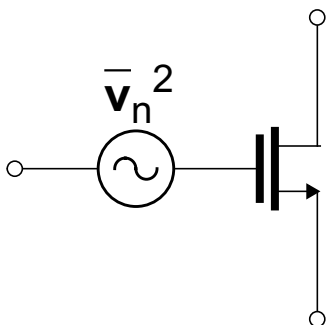


$$\overline{v_n^2} = 4kT \left( \frac{2}{3} \frac{1}{g_m} \right) \quad V^2 / Hz$$

$g_m = 100\mu A/V$ :  $\overline{V_n}=10.5nV/\sqrt{rt(Hz)}$  at 300°K

$g_m = 1000\mu A/V$ :  $\overline{V_n}=33nV/\sqrt{rt(Hz)}$  at 300°K

### MOS 1/f noise



$$\overline{v_n^2} = \frac{K}{C_{ox}WL} \frac{1}{f}$$

$$K=1 \times 10^{-25} \text{ V}^2\text{F}$$

$$C_{ox} = 3\text{fF}/\mu\text{m}^2$$

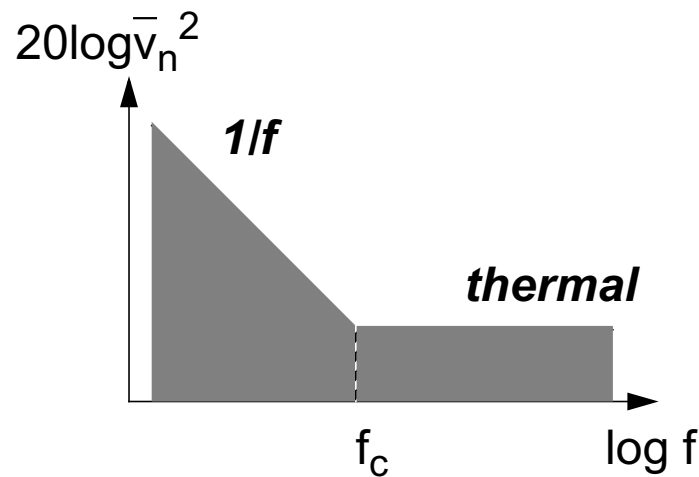
$$W = 20\mu\text{m}$$

$$L = 1\mu\text{m}$$

$$f = 1\text{kHz}$$

$$\overline{V_n}=40.8nV/\sqrt{rt(Hz)}$$

## Corner frequency



**$f_c$  = corner frequency**

Corner frequency for case  $g_m = 100\mu A/V$  above

$$4kT\left(\frac{2}{3}\frac{1}{g_m}\right) = \frac{K}{C_{ox}WL} \frac{1}{f_c} = (10.5nV/\sqrt{Hz})^2$$

$$f_c = \frac{K}{C_{ox}WL(10.5nV/\sqrt{Hz})^2} = 15kHz$$

Total noise at 15kHz = : 14.8nV/rt(Hz)



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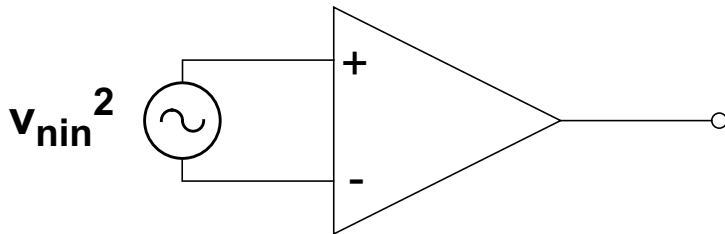
## Noise notes (3)

### Input-referred noise

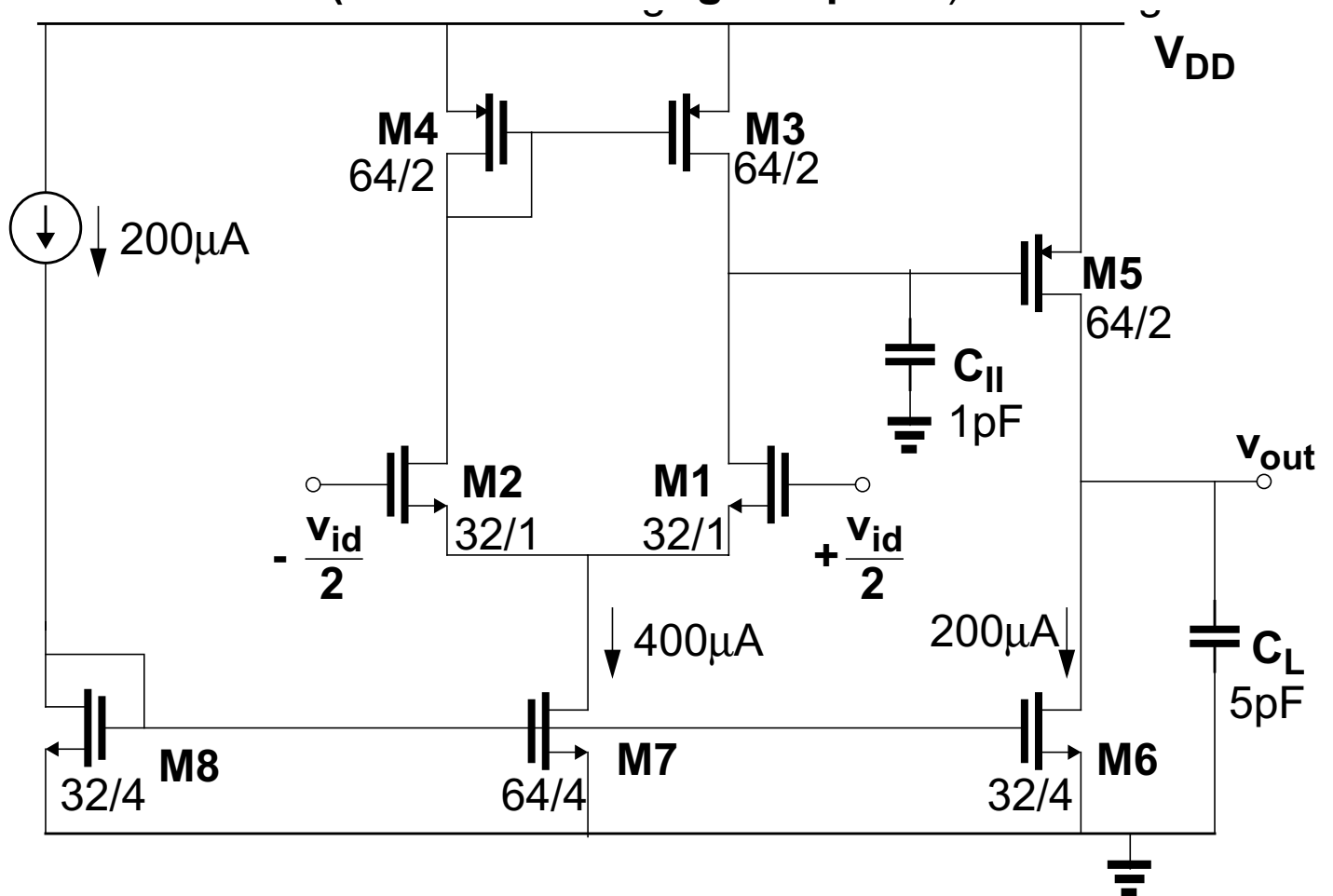
It is usual in the case of voltage amplifiers to refer all noise sources to the input of the amplifier, and quote the 'input-referred noise' of the amplifier.

This allows for easier comparison of noise performance.

To input-refer a noise source: divide the source by the gain from the input to the source.



### Problem P. 327: (Offset of two-stage amplifier)



$$g_{m1} = 1.6mA/V$$

$$g_{m5} = 800\mu A/V$$

**What is the input-referred offset of the amplifier shown?**

Take  $A_{Vt} = 10mV/\mu m$ .

Note: In the following  $\Delta V_t$ ,  $\Delta I$  refers to a 1 sigma mismatch in  $V_t$ 's  $I$ 's

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## Solution

### 1. Contribution of input pair.

Input pair have offset voltage given by

$$\Delta V_{t1} = \frac{A_{Vt}}{\sqrt{(WL)_1}} = \frac{10mV\mu m}{\sqrt{32 \times 1}} = 1.77mV$$

### 2. Contribution of mirror pair M3 M4.

Mirror pair have offset voltage given by

$$\Delta V_{t3} = \frac{A_{Vt}}{\sqrt{(WL)_3}} = \frac{10mV\mu m}{\sqrt{64 \times 2}} = 0.88mV$$

These cause a mismatch in drain currents  $\Delta I$  between M3 and M4

$$\Delta I = g_{m3} \Delta V_{t3}$$

To refer this to input divide by  $g_m$  of input pair

Input-referred offset voltage from mirror pair then given by

$$\Delta V_{t3inpref} = \frac{g_{m3} \Delta V_{t3}}{g_{m1}} = \frac{800\mu A/V}{1600\mu A/V} = 0.44mV$$

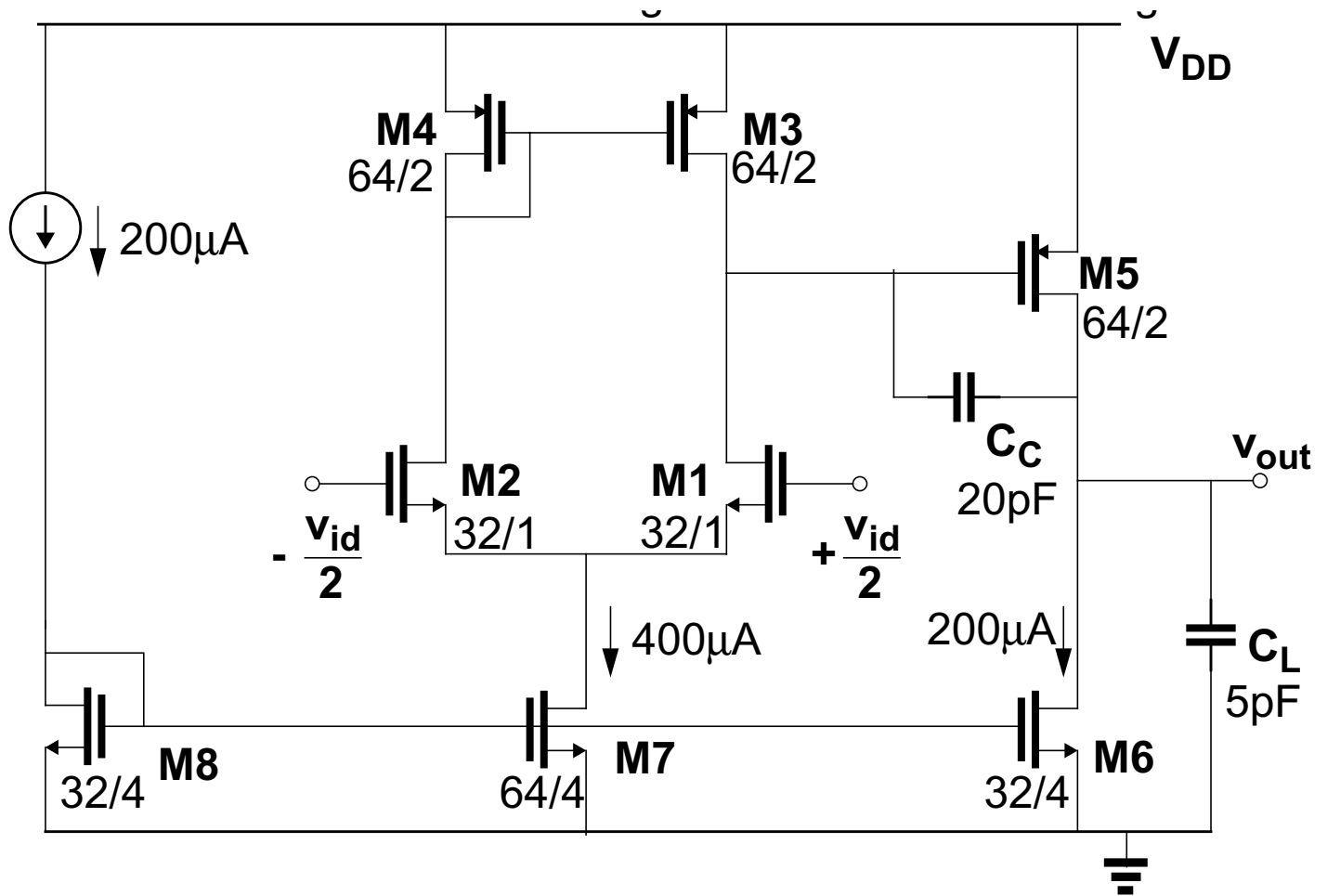
### 4. Total input referred offset

Sum contributions from input pair and mirror pair quadratically as offset is a random effect

$$\begin{aligned} V_{OSinpref} &= \sqrt{(\Delta V_{t1})^2 + (\Delta V_{t3inpref})^2} \\ &= \sqrt{1.77^2 + 0.44^2} = 1.82mV \end{aligned}$$

Conclusion: Offset of input pair is dominant. If it is required to reduce the overall offset the size of the input pair should be increased. In amplifier chains with large gain, offset cancellation may be required.

## Problem P. 331 (Slew Rate of two-stage amplifier)



**What is the slew rate of the amplifier shown?**

**Solution:**

**For  $C_{II}$ :** max. current available to charge/discharge  $C_C$  is  $400\mu A$

$$\text{Slew Rate} = \frac{400\mu A}{20pF} = 20\mu V/\mu s$$

**For  $C_L$ :**

Discharging  $C_L$  - max. current available to discharge  $C_L$  is the bias current of M6 =  $200\mu A$

$$\text{Slew Rate} = \frac{200\mu A}{5pF} = 40\mu V/\mu s$$

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Charging  $C_L$  - If a large positive step is applied to the input then all the  $400\mu A$  bias current will flow through M1 and none through M2, M4, M3.

=> the gate of M5 will be pulled low, increasing the  $|V_{GS}|$  of M5 and increasing the current through M5 far beyond the quiescent value of  $200\mu A$  giving a slew rate of much greater than that for the case of discharging  $C_L$

The overall slew rate of the amplifier is taken as the worst case value i.e.

$$\text{Slew Rate of amplifier} = 20\mu V/\mu s$$

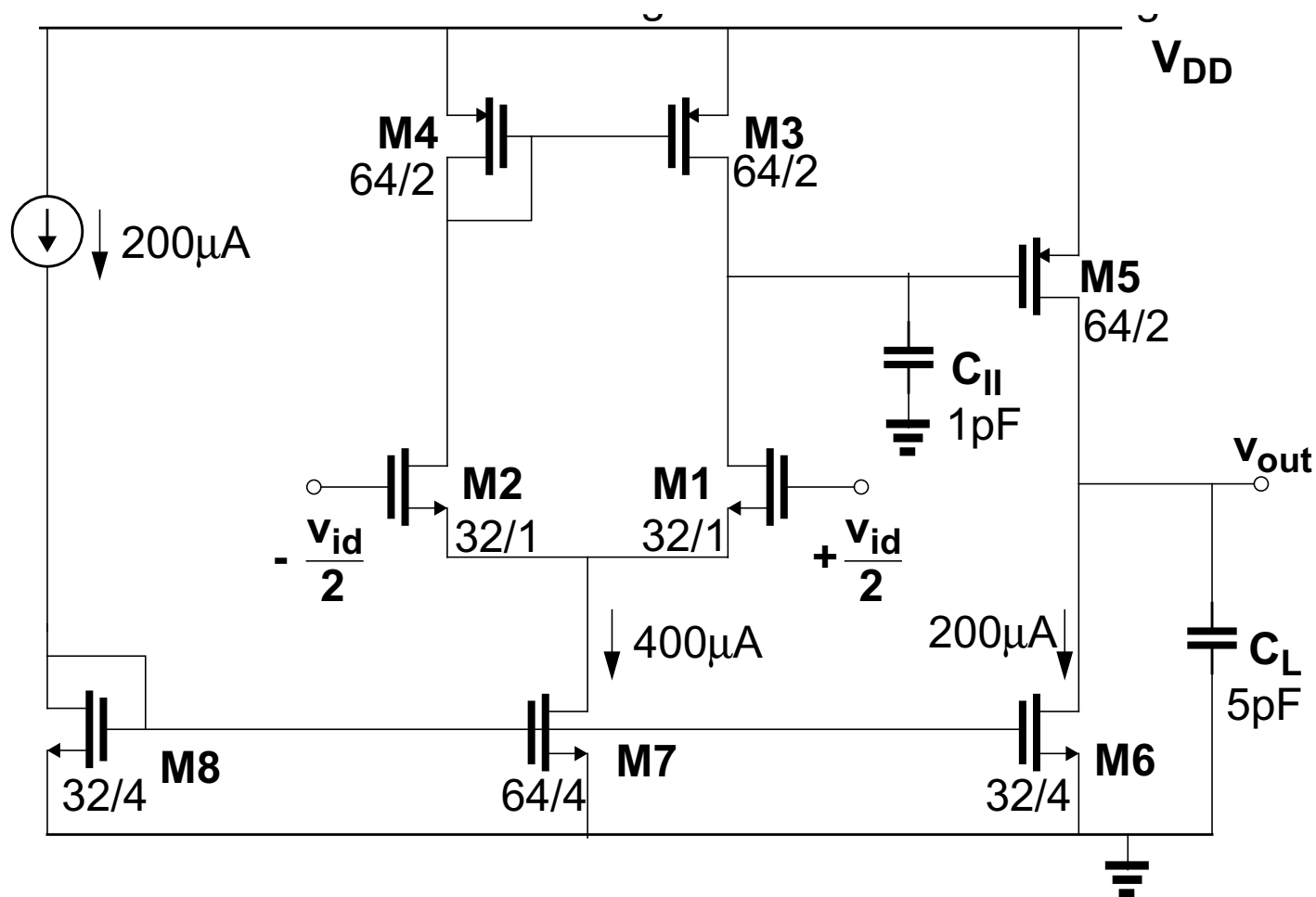
The significance of slew-rate is that even though the small-signal bandwidth may indicate a certain gain bandwidth, the slew-rate will often place a lower limit on the maximum frequency

$$GBW = \frac{g_{m1}}{C_C} = \frac{1.6mA/V}{20pF} = 80Mrad/s = 12.7MHz$$

For no slewing with 1Vpp sine wave at the output

$$f < \frac{I}{2\pi C_A} = \frac{400\mu A}{2\pi \times 20pF \times 0.5} = 6.4MHz$$

### Problem P. 334(Common-Mode Input Range)



**What is the Common-mode input range of the amplifier shown?**

Take  $V_{DD}=5V$ ,  $V_{tn}=V_{tp}=0.8V$

## 1. Lower limit on $V_{CM}$ :

$$V_{CM} \geq V_{GS1} + V_{SAT7}$$

$$V_{CM} \geq V_{GS1} + (V_{GS7} - V_t)$$

$$V_{GS} - V_t = \sqrt{\frac{2I_D}{K'_n \frac{W}{L}}}$$

$$\text{M1: } V_{GS1} - V_t = \sqrt{\frac{2 \cdot 200\mu A}{200\mu A/V \cdot \frac{32}{1}}} = 250mV$$

$$V_{GS1} = 250mV + V_t = 1.05V$$

$$\text{M7: } V_{GS7} - V_t = \sqrt{\frac{2 \cdot 400\mu A}{200\mu A/V \cdot \frac{64}{4}}} = 500mV$$

$$V_{CM} \geq 1.05V + 0.5V \Rightarrow V_{CM} \geq 1.55V$$

## 2. Upper limit:

$$V_{CM} \leq V_{DD} - |V_{GS4}| + V_{tn}$$

$$\text{M4 } |V_{GS4} - V_{tp}| = \sqrt{\frac{2 \cdot 200\mu A}{50\mu A/V \cdot \frac{64}{2}}} = 500mV$$

$$|V_{GS4}| = 500mV + |V_{tp}| = 1.30V$$

$$V_{CM} \leq V_{DD} - |V_{GS4}| + V_{tn}$$

$$V_{CM} \leq 5 - 1.30V + 0.8V$$

$$V_{CM} \leq 4.5V$$

**=>Common-mode input range given by**

$$1.55V \leq V_{CM} \leq 4.5V$$