Solutions UE4010 Autumn 2005 Part A

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an nmos in saturation:

$$I_D = \frac{K'_n}{2}\frac{W}{L}(V_{GS} - V_{tn})^2(1 + \lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n = \lambda_p = 0$.
In each question, capacitances other than those mentioned may be ignored.

Question 1

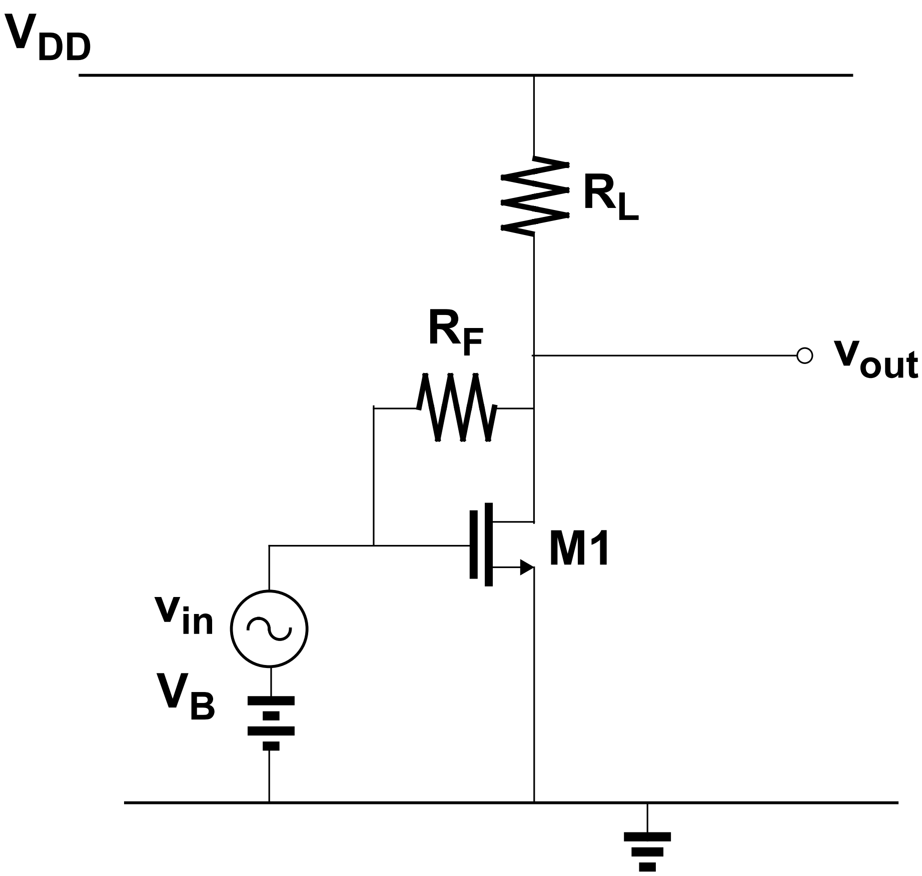

Figure 1

(i) Draw the small-signal equivalent circuit for the CMOS common-source stage shown in Figure 1.
(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal transistor parameters, R_F and R_L.
(iii) Calculate the small-signal gain in dB if
$V_B = 1.2V$, $V_{tn} = 0.7V$, $R_F = 5k\Omega$, $R_L = 20k\Omega$.
Assume R_L, R_F, << $1/g_{ds1}$, and that M1 is in saturation with a drain current of 200μA.
(iv) What is the value of the gain in dB if R_F is increased to 10kΩ?
What is the value of the gain in dB if R_F is increased to infinity?

(i) Draw the small-signal equivalent circuit for the CMOS inverter stage shown in Figure 1.

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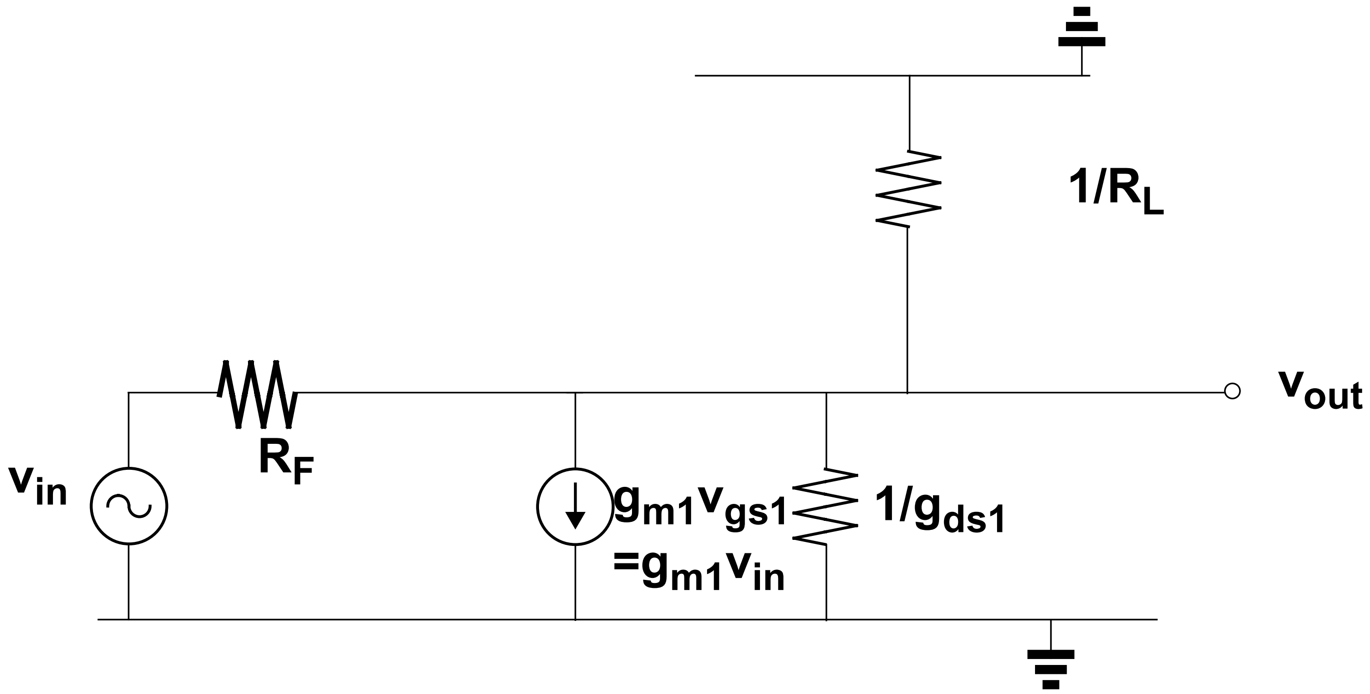

(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal transistor parameters, R_F and R_L.

KCL at output node

$$\frac{(v_{out}-v_{in})}{R_F} + g_{m1}v_{in} + v_{out}g_{ds1} + \frac{v_{out}}{R_L} = 0$$

$$\left(g_{m1} - \frac{1}{R_F}\right)v_{in} = -\left(g_{ds1} + \frac{1}{R_F} + \frac{1}{R_L}\right)v_{out}$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} - \frac{1}{R_F}}{g_{ds1} + \frac{1}{R_F} + \frac{1}{R_L}}$$

(iii) Calculate the small-signal gain in dB if
$V_B = 1.2V$, $V_{tn} = 0.7V$, $R_F = 5k\Omega$, $R_L = 20k\Omega$.
Assume R_L, R_F, << $1/g_{ds1}$, and that M1 is in saturation with a drain current of 200μA.

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$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} - \frac{1}{R_F}}{g_{ds1} + \frac{1}{R_F} + \frac{1}{R_L}}$$

$$g_{m1} = \frac{2I_D}{(V_{GS1} - V_{tn})} = \frac{2 \times 200\mu A}{1.2 - 0.7} = 800\mu A/V$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} - \frac{1}{R_F}}{g_{ds1} + \frac{1}{R_F} + \frac{1}{R_L}} \approx \frac{800\mu A/V - \frac{1}{5k\Omega}}{\frac{1}{5k\Omega} + \frac{1}{20k\Omega}} = 2.4$$

$$20\log\left|\frac{v_{out}}{v_{in}}\right| = 7.6dB$$

(iv) What is the value of the gain if R_F is increased to 10kΩ?
What is the value of the gain if R_F is increased to infinity?

R_F=10kΩ

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} - \frac{1}{R_F}}{g_{ds1} + \frac{1}{R_F} + \frac{1}{R_L}} \approx \frac{800\mu A/V - \frac{1}{10k\Omega}}{\frac{1}{10k\Omega} + \frac{1}{20k\Omega}} = 4.7 = 13.4dB$$

R_F=infinity

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} - \frac{1}{R_F}}{g_{ds1} + \frac{1}{R_F} + \frac{1}{R_L}} \approx \frac{800\mu A/V}{\frac{1}{20k\Omega}} = 16 = 24.1dB$$

Question 2

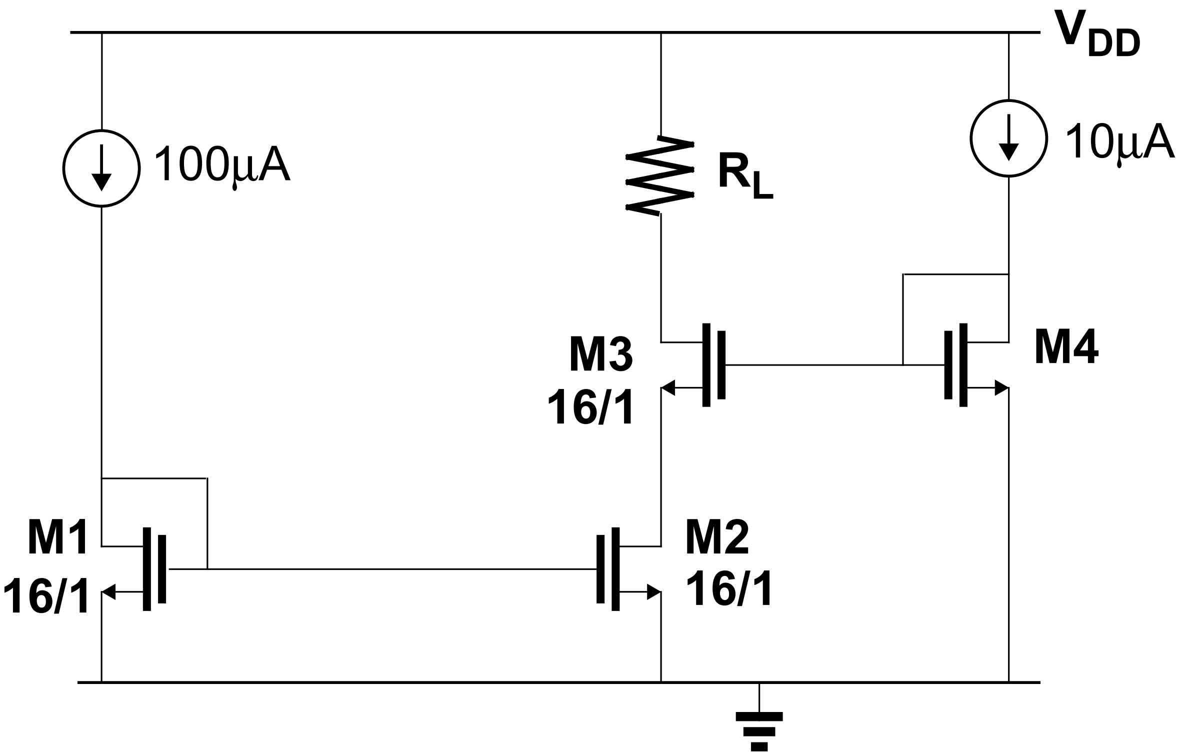


Figure 2

Figure 2 shows an nmos current mirror (M1, M2) with cascoded output. The bias voltage for the cascode is generated by the diode-connected nmos M4 which is biased by a current source as shown.

For this question $K_n' = 200\mu A/V^2$, $V_{tn} = 750mV$, $V_{DD} = 5V$.

The device sizes of M1, M2 and M3 in microns are as indicated in Figure 2.

All devices are biased in saturation.

(i) What is the maximum voltage at the drain of M2 such that M2 is just biased in saturation?
If M4 has L=10, what is the required value of W for M4 such that M2 is just biased in saturation, assuming M3 is in saturation?

(ii) What is then the maximum value of R_L such that M3 is also biased in saturation?

(iii) Given the bias conditions established in (i) and (ii), estimate the percentage inaccuracy of the current mirror due to the finite output conductance of M1 and M2.
For this calculation take $\lambda_n = 0.04V^{-1}$.

(iv) Estimate the 3 sigma percentage inaccuracy of the current mirror due to transistor V_{tn} mismatch.
Note: Assume the mismatch is normally distributed and that the 1 sigma V_{tn} mismatch of a transistor pair (in mV) is given by

$$\sigma_{Vtn} = \frac{A_{Vtn}}{\sqrt{WL}}$$

Take $A_{Vtn} = 10mV\mu m$.

(i) What is the maximum voltage at the drain of M2 such that M2 is just biased in saturation?
If M4 has L=10, what is the required value of W for M4 such that M2 is just biased in saturation, assuming M3 is in saturation?

For M1,M2

$$|V_{GS} - V_t| = \sqrt{\frac{2I_D}{K_n'\frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V^2\frac{16}{1}}} = 250mV$$

This is the minimum source drain voltage required for M2 to be in saturation.

$$V_{D2min} = \underline{\underline{0.25V}}$$

For M4

As M3 has same dimensions, same current as M1, M2 it has the same V_{GS}

$$V_{GS3} = V_{GS1} = (V_{GS1} - V_t) + V_t = 0.25V + 0.75V = 1V$$

$$V_{GS4} = V_{GS3} + V_{D2min}$$

$$= 1 + 0.25V$$

$$= 1.25V$$

$$I_{D4} = \frac{K_n'}{2}\frac{W}{L}(V_{GS4} - V_t)^2 \Rightarrow W = \frac{2I_{D4}}{K_n'\frac{1}{L}(V_{GS4} - V_t)^2}$$

$$\underline{\underline{W = \frac{2 \cdot 10\mu A}{200\mu A/V^2\frac{1}{10}(1)^2} = 1}}$$

(ii) What is then the maximum value of R_L such that M3 is also biased in saturation?

Maximum voltage at drain of M3

$$V_{D3max} = V_{D2max} + (V_{GS3} - V_t) = 0.25V + 0.25V = 0.5V$$

Maximum value of R_L is then given by

$$R_{Lmax} = \frac{V_{DD} - V_{D3max}}{I_{D3}} = \frac{5V - 0.5V}{100\mu A} = \underline{\underline{45k\Omega}}$$

(iii) Given the bias conditions established in (i) and (ii), estimate the percentage inaccuracy of the current mirror due to the finite output conductance of M1 and M2.
For this calculation take λ_n=0.04V^{-1}.

$$I_{D1} = \frac{K'_n}{2}\frac{W}{L}(V_{GS1} - V_{tn})^2(1 + \lambda_n V_{DS1})$$

$$I_{D2} = \frac{K'_n}{2}\frac{W}{L}(V_{GS2} - V_{tn})^2(1 + \lambda_n V_{DS2})$$

$$\frac{I_{D2}}{I_{D1}} = \frac{1 + \lambda_n |V_{DS2}|}{1 + \lambda_n |V_{DS1}|} = \frac{1 + 0.04 \cdot 0.25}{1 + 0.04 \cdot 1.00} = 0.962$$

Percentage inaccuracy = $\underline{\underline{-3.8\%}}$

(iv) Estimate the 3 sigma percentage inaccuracy of the current mirror due to transistor V_t mismatch.
Note: The 1 sigma V_t mismatch of a transistor pair in mV is given by

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{WL}}$$

Take $A_{Vt} = 10mV\mu m$.

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{WL}} = \frac{10mV\mu m}{\sqrt{16\mu m \cdot 1\mu m}} = 2.5mV$$

This is the 1σ mismatch in V_t of M1 and M2

This value is small compared to the overdrive voltage V_{GS}-V_t

=> Use small-signal analysis to calculate inaccuracy

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2 \times 100\mu A}{0.25V} = 0.8mA/V = 0.8\mu A/mV$$

$$\sigma_{I_D} = g_m \sigma_{Vt} = 2.5mV \cdot 0.8\mu A/mV = 2\mu A$$

i.e. 1σ sigma mismatch in drain currents of 2%

3σ percentage mismatch is +/-6%

Question 3

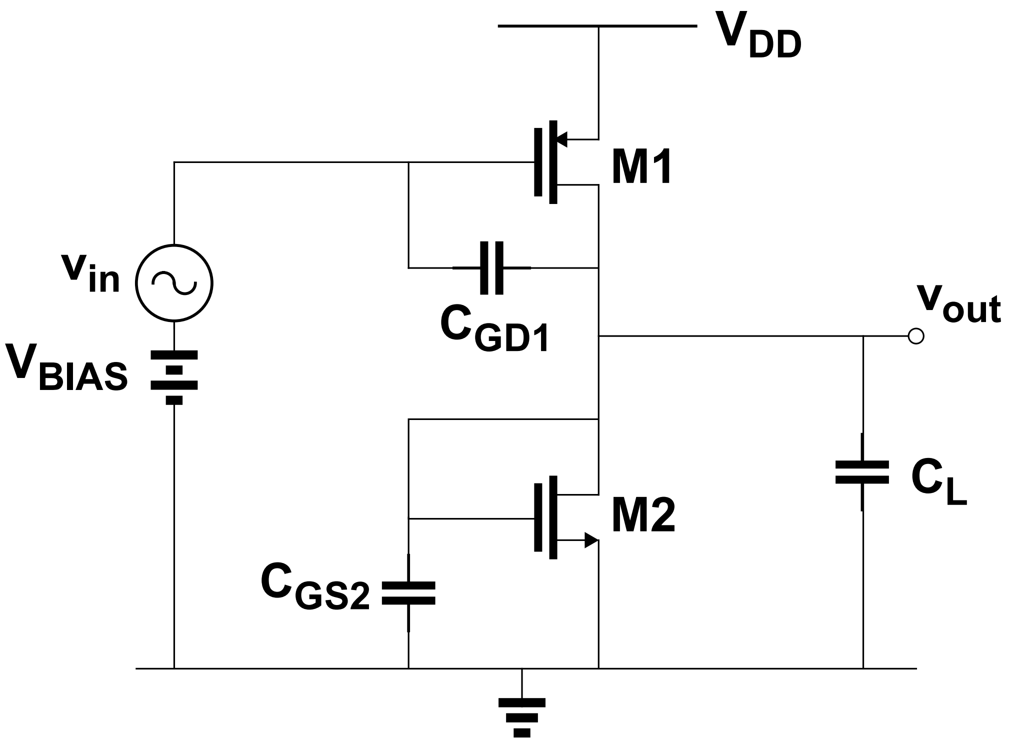


Figure 3

For the questions below you may assume $g_{m1},g_{m2} >> g_{ds1},g_{ds2}$ and that all devices are biased in saturation.

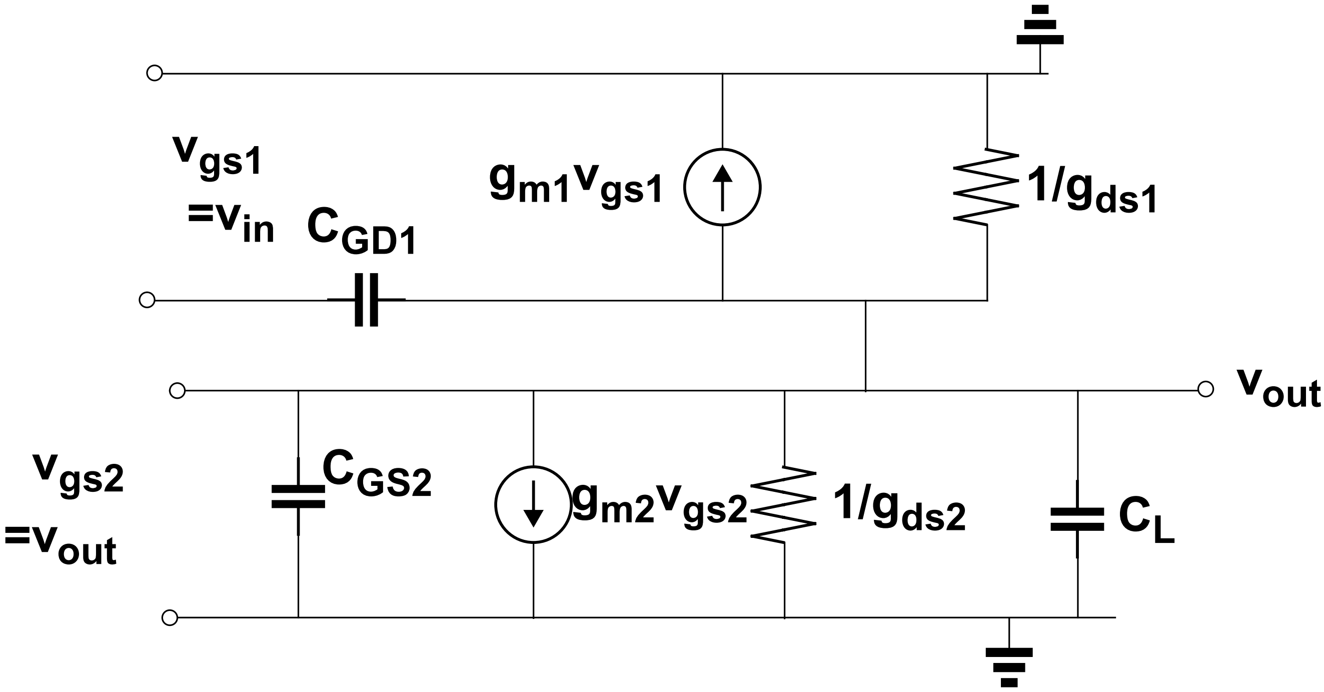
(i) Figure 3 shows a pmos common-source stage with a diode-connected nmos load. Draw the small-signal model for this circuit.

(ii) Ignoring all capacitances except C_{GD1}, C_{GS2} and C_L derive an expression for the high-frequency transfer function.

(iii) Calculate the low-frequency gain (v_{out}/v_{in}) in dB, and the pole and zero frequencies, if V_{GS1} = 1V, V_{GS2} = 1.75V, $V_{tn} = |V_{tp}|$ = 0.75V, $|I_{D1}|$ = 250μA, C_{GD1} = 0.1pF, C_{GS2} = 1pF, C_L= 1.5pF.

(iv) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the pole and zero frequencies.

(i) Figure 3 shows a pmos common-source stage with a diode-connected nmos load. Draw the small-signal model for this circuit.



(ii) Ignoring all capacitances except C_{GD1}, C_{GS2} and C_L derive an expression for the high-frequency transfer function.

KCL at output node

$$g_{m1}v_{gs1} + g_{m2}v_{gs2} + v_{out}g_{ds1} + v_{out}g_{ds2} + v_{out}s(C_L + C_{GS2}) - (v_{in} - v_{out})sC_{GD1} = 0$$

$$g_{m1}v_{in1} + g_{m2}v_{out} + v_{out}g_{ds1} + v_{out}g_{ds2} + v_{out}s(C_L + C_{GS2}) - (v_{in} - v_{out})sC_{GD1} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} - sC_{GD1}}{g_{m2} + g_{ds1} + g_{ds2} + s(C_L + C_{GS2})}$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}\left(1 - \frac{sC_{GD1}}{g_{m1}}\right)}{g_{m2} + g_{ds1} + g_{ds2}\left(1 + \frac{s(C_{GS2} + C_L)}{g_{m2} + g_{ds1} + g_{ds2}}\right)}$$

$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}\left(1 - \frac{sC_{GD1}}{g_{m1}}\right)}{g_{m2}\left(1 + \frac{s(C_{GS2} + C_L)}{g_{m2}}\right)}$$

Alternatively use $1/g_{m2}$ approx. for diode connected M2 and get simpler derivation

(iii) Calculate the low-frequency gain (v_{out}/v_{in}) in dB, and the pole and zero frequencies, if V_{GS1} = 1V, V_{GS2} = 1.75V, $V_{tn} = |V_{tp}|$ = 0.75V, $|I_{D1}|$ = 250µA, C_{GD1} = 0.1pF, C_{GS2} = 1pF, C_L= 1.5pF.

$$g_{m1} = \frac{2I_{D1}}{(V_{GS1}-V_{tn})} = \frac{2\times 250\mu A}{1-0.75} = 2000\mu A/V$$

$$g_{m2} = \frac{2|I_{D2}|}{(|V_{GS2}|-|V_{tp}|)} = \frac{2\times 250\mu A}{1.75-0.75} = 500\mu A/V$$

Low-frequency gain given by

$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}}{g_{m2}} = \frac{2000\mu A/V}{500\mu A/V} = -4 = 12dB$$

Zero frequency given by

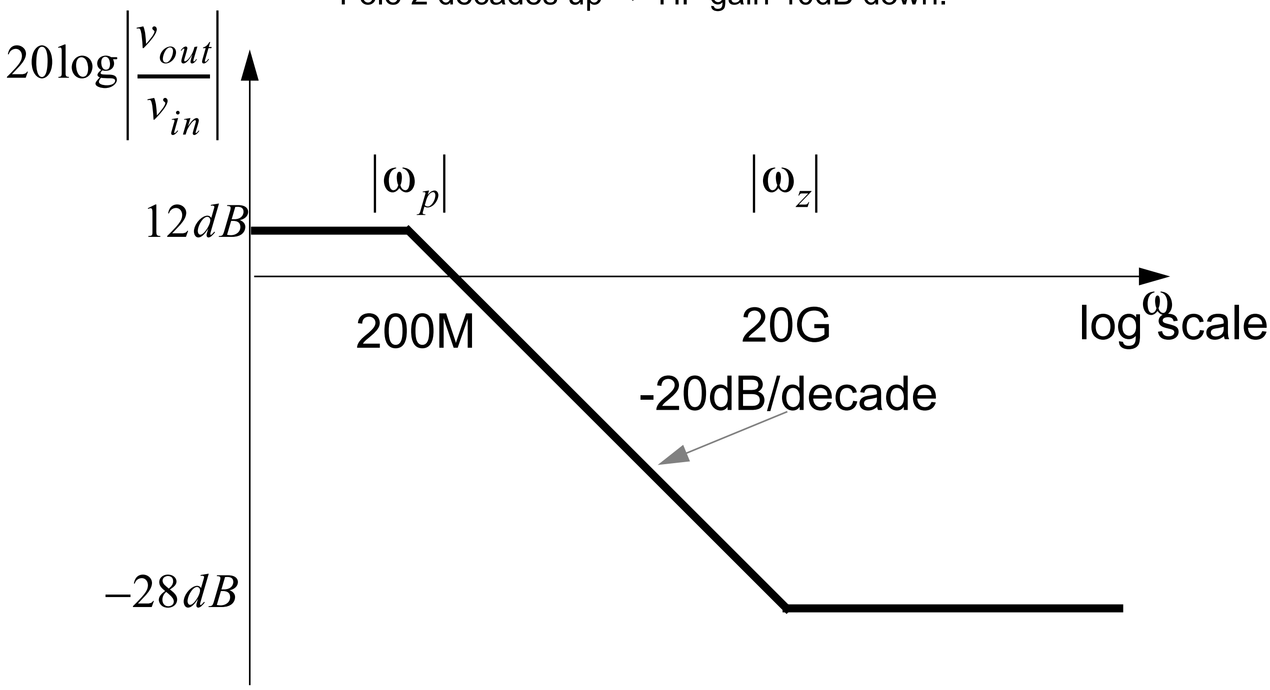
$$|\omega_z| = \frac{g_{m1}}{C_{GD1}} = \frac{2000\mu A/V}{0.1pF} = 20Grad/s$$

Pole frequency given by

$$|\omega_p| = \frac{g_{m2}}{C_{GS2}+C_L} = \frac{500\mu A/V}{1pF+1.5pF} = 200Mrad/s$$

(iv) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the pole and zero frequencies.

Pole 2 decades up => HF gain 40dB down.



Question 4

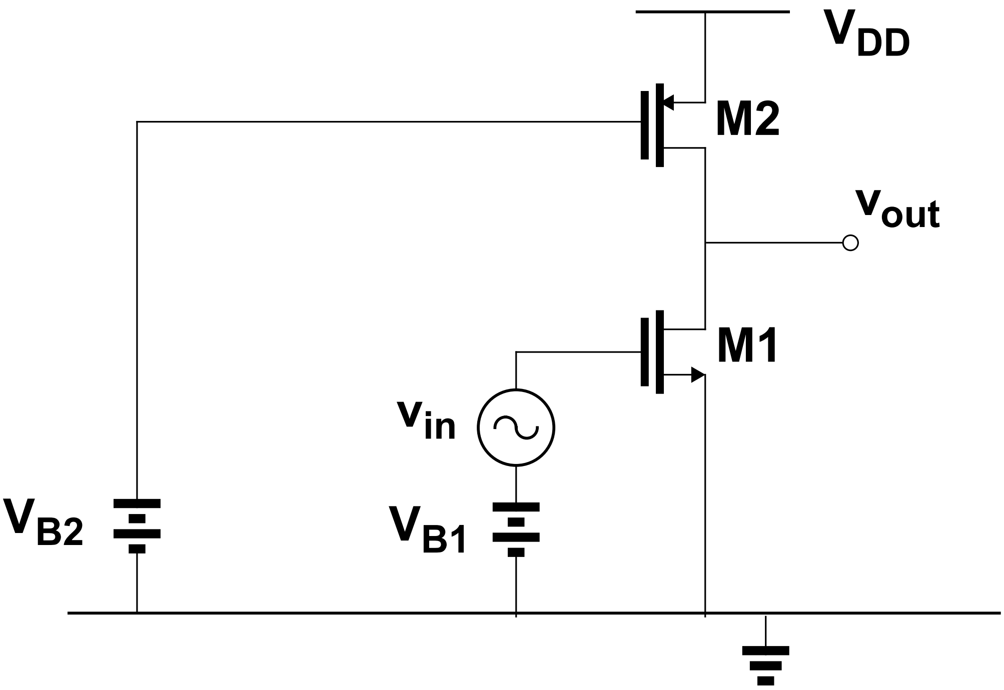


Figure 4

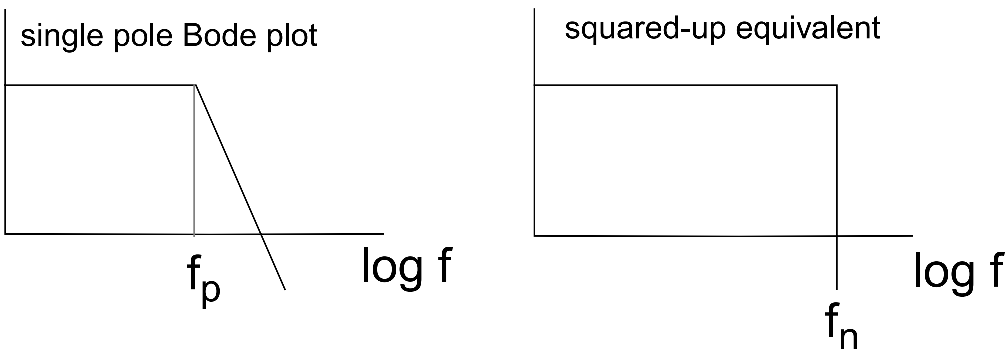
Assume M1 and M2 are operating in saturation. Only thermal noise sources need be considered.

(i) Draw the small-signal model for the circuit shown in Figure 4.
What is the low-frequency small-signal voltage gain (v_{out}/v_{in})?

(ii) What is the input-referred thermal noise voltage in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T?

(iii) If a capacitor C_L is connected between the output node and ground what is the total integrated thermal noise at the output node?

You may assume the following:



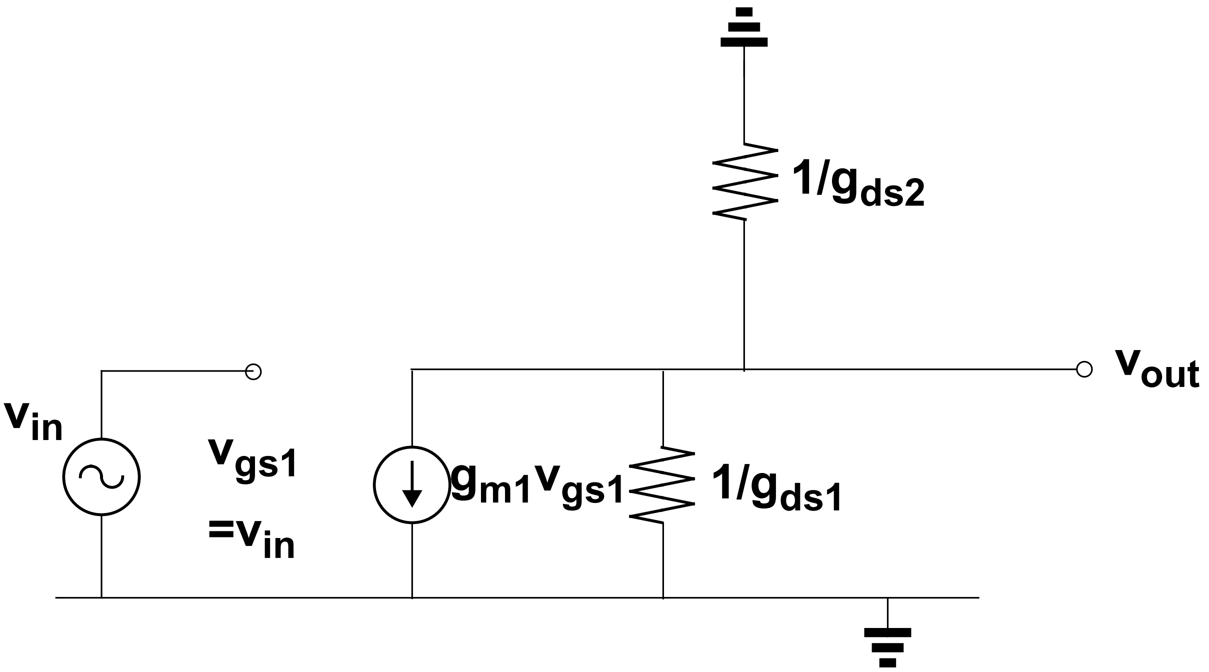
For the area underneath the curves to be the same then $f_n=(\pi/2)*f_p$

(iv) Using the result of (iii) calculate the signal-to noise ratio at the output if the input signal v_{in} is a $1mV_{rms}$ sine wave with a frequency much lower than the frequency of the pole at the output node.
For this calculation take V_{B1}=1.0V, V_{B2}=2.0V, V_{DD}=3V, V_{tn} = 0.75V, V_{tp} = -0.75V, $\lambda_n=\lambda_p=0.04V^{-1}$, C_L=10pF.
The drain current of M1 is 100µA.
Assume Boltzmann's constant $k=1.38X10^{-23}J/^oK$, temperature $T=300^oK$.

Solution

(i) Draw the small signal model for the circuit shown in Figure 3. Ignore all capacitances

What is the low-frequency small signal voltage gain (v_{out}/v_{in})?

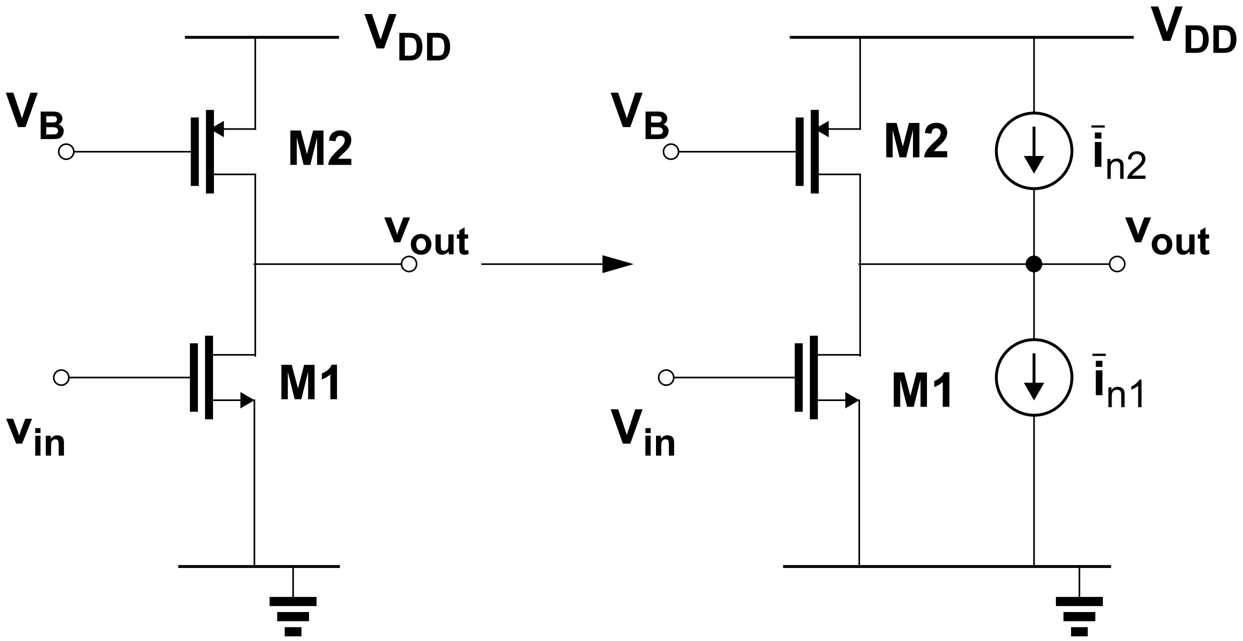


Current at output node

$$g_{m1}v_{in} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

(ii) What is the input-referred thermal noise voltage in terms of R_L, the small signal parameters of M1, Boltzmann's constant k and temperature T?



Noise current of MOS: $\overline{i_n^2} = 4kT\left(\frac{2}{3}g_m\right)$

Noise sources uncorrelated => total noise is the sum of squares

$$\overline{i_{nt}^2} = i_{n1}^2 + i_{n2}^2 \quad \text{or} \quad \overline{i_{nt}} = \sqrt{i_{n1} + i_{n2}} \quad \text{rms value}$$

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}}{g_{m1}} \quad \text{rms noise} \quad V/\sqrt{Hz}$$

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \sqrt{4kT \cdot \frac{2}{3}\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2}\right)}$$

(iii) If a capacitor C_L is connected between the output node and ground what is the total integrated thermal noise at the output node?

To get voltage noise at output multiply input-referred noise by gain of circuit

$$\overline{v_{no}} = \overline{v_{ni}} \frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

$$\overline{v_{no}} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}}{g_{ds1} + g_{ds2}}$$

To get total noise voltage at output need to integrate this over all frequencies

The circuit is first-order circuit with a pole at

$$\omega_o = -\frac{g_{ds1} + g_{ds2}}{C_L}$$

$$\overline{v_{nototal}^2} = \int_0^{\infty} \left(\frac{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}{(g_{ds1} + g_{ds2})^2} \cdot \frac{1}{1 + \frac{C_L^2}{(g_{ds1} + g_{ds2})^2} \cdot (2\pi f)^2} \right) df$$

This is equal to multiplying by the noise bandwidth

$$v_{nototal}^2 = v_{no}^2 \cdot \frac{\pi}{2} \cdot f_o = \frac{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}{(g_{ds1} + g_{ds2})^2} \cdot \frac{\pi}{2} \cdot \frac{g_{ds1} + g_{ds2}}{2\pi C_L}$$

$$= \left(\frac{\frac{2}{3}(g_{m1} + g_{m2})}{g_{ds1} + g_{ds2}} \cdot \frac{kT}{C_L} \right)$$

(iv) Using the result of (iii) calculate the signal-to noise ratio at the output if the input signal v_{in} is a $1mV_{rms}$ sine wave with a frequency much lower than the frequency of the pole at the output node.
For this calculation take V_{BIAS1}=1.0V, V_{BIAS2}=2.0V, V_{DD}=3V, V_{tn} = 0.75V, V_{tp} = -0.75V, $\lambda_n=\lambda_p=0.04V^{-1}$, C_L=10pF.
The drain current of M1 is 100μA.
Assume Boltzmann's constant $k=1.38X10^{-23}J/^oK$, temperature $T=300^oK$.

g_m given by

$$g_m = \frac{2I_D}{(V_{GS}-V_T)}$$

$$g_{m1} = \frac{2 \cdot 100\mu A}{1V - 0.75V} = 800\mu A/V \qquad g_{m2} = \frac{2 \cdot 100\mu A}{1V - 0.75V} = 800\mu A/V$$

$$g_{ds1} = \lambda_n I_D = 0.04V^{-1}100\mu A = 4\mu A/V$$

$$g_{ds2} = \lambda_n I_D = 0.04V^{-1}100\mu A = 4\mu A/V$$

Output signal

$$v_{out} = -\left(\frac{g_{m1}}{g_{ds1}+g_{ds2}}\right)v_{in} = -\frac{800\mu A/V}{8\mu A/V} \cdot 1mV_{rms} = 100mV_{rms}$$

Total output noise:

$$\overline{v_{nototal}} = \sqrt{\frac{\frac{2}{3}(g_{m1}+g_{m2})}{g_{ds1}+g_{ds2}} \cdot \frac{kT}{C_L}}$$

$$\overline{v_{nototal}} = \sqrt{\frac{2}{3}\left(\frac{800\mu A/V + 800\mu A/V}{4\mu A/V + 4\mu A/V}\right) \cdot \frac{1.38\times10^{-23}300}{10pF}} = 235\mu V_{rms}$$

Signal-to-Noise ratio given by

$$\frac{S}{N} = \frac{100mV}{235\mu V} = 426 \qquad \text{or 52.6 dB}$$