
UE4002 Analog IC Design

Kevin O'Sullivan
S3 Group

kevin.osullivan@s3group.com

Version History

Version	Date	Notes
1.0	16 Sep 2013	Initial Version
1.1	02 Apr 2014	Corrected some typos

Contents

1	Introduction	10
1.1	Analog Circuit Design	10
1.2	'Mixed-Signal' Circuit Design	11
1.3	Historical Overview.....	12
1.4	Analog design - levels of abstraction.....	14
1.5	Course Objective	15
1.6	Course Contents	16
1.7	Recommended books	18
1.8	General Course Items.....	19
2	Review of MOS Transistor basics	21
2.1	MOSFET switch.....	21
2.2	NMOS device structure.....	22
2.2.1	Backgate connection	23
2.3	PMOS device structure	24
2.4	CMOS technology	25
2.4.1	CMOS with DNW.....	26
2.5	MOSFET dimensions.....	27
2.6	MOSFET dimensions (scaling).....	28
2.7	MOSFET Symbols	29
2.8	MOSFET Operation (NMOS).....	30
2.9	Threshold voltage	32
2.10	Derivation of IV characteristic	33
2.11	MOS Operating Regions	38
2.12	Second-Order Effects	42
2.12.1	Body effect a.k.a. backgate effect	42
2.12.2	Channel Length modulation	44
2.12.3	Subthreshold Conduction	45
2.12.4	Velocity Saturation and other short-channel effects	46
2.13	Regions of Operation.....	47
2.14	Typical values (0.35um process)	49

3	Basic Circuit Techniques	58
3.1	Review of network elements and concepts	58
3.1.1	Resistance, Conductance	58
3.1.2	Ideal Independent Sources	61
3.1.3	Real Independent Sources	62
3.1.4	Dependent Sources.....	63
3.1.5	Kirchoff's current law	64
3.1.6	Kirchoff's voltage law	64
3.2	Small-signal analysis in transistor circuits (ac/incremental analysis).....	65
3.2.1	Notation	65
3.2.2	Linearisation	66
3.2.3	Small-signal equivalent circuits	67
3.3	MOS Small-signal parameters (NMOS)	68
3.3.1	Transconductance g_m	68
3.3.2	Output conductance g_{ds}	70
3.3.3	Back-gate (bulk) transconductance g_{mb}	71
3.4	Small Signal Model (Low-Frequency)	72
4	Single-stage amplifiers.....	74
4.1	Common source stage with Resistive Load	75
4.1.1	CS stage with resistor load - Large-signal behaviour	75
4.1.2	Gain of CS stage with resistive load.....	79
4.1.3	Gain of CS stage, R load, with output conductance.....	80
4.1.4	CS stage with Resistive Load: Small-signal analysis	81
4.2	Common source stage with Diode Load	85
4.2.1	CS stage with diode load -Large-signal behaviour.....	85
4.2.2	Diode-connected MOS (small-signal model).....	89
4.2.3	CS stage with Diode Load - small-signal analysis.....	90
4.3	Common source stage with active load	95
4.3.1	Common source stage with active load - Large signal behaviour	96
4.3.2	CS stage with active load - small-signal analysis	98
4.4	Two-port analysis and y-parameters	106
4.5	CS stage with Resistive degeneration	111
4.5.1	CS stage with Res. degeneration - Large-signal behaviour	111
4.5.2	CS stage with Res. degeneration - Large-signal behaviour: transconductance.....	113
4.5.3	CS with res. degeneration. Large-signal behaviour : gain.....	115
4.5.4	CS with res. degeneration: Small-signal gain.....	116
4.5.5	CS with res. degeneration: Transconductance G_m	117
4.5.6	CS with res. degeneration: Small-signal output resistance	118
4.6	Source Follower (common-drain) stage	122

4.6.1	Source Follower - Large-signal behaviour	122
4.6.2	Source follower: large signal behaviour analysis.....	124
4.6.3	Source Follower - Small-signal behaviour (gain).....	125
4.6.4	Source follower - output resistance R_{out}	127
4.6.5	Source follower - Transconductance G_m	128
4.7	Common Gate stage.....	130
4.7.1	Common gate small-signal voltage gain	131
4.7.2	Common gate - input resistance	132
4.7.3	Common gate - output resistance	133
4.8	Cascode Stage.....	135
4.8.1	Cascode Stage: Biasing requirements	136
4.8.2	Cascode Stage: Large signal behaviour	137
4.8.3	Cascode: Transconductance G_m	138
4.8.4	Cascode: Output Resistance R_{out}	139
4.8.5	Cascode: Small-signal voltage gain	140
4.8.6	Cascode gain stage with active load	144
4.8.7	Cascode gain stage with cascode load	145
4.9	Folded Cascode stage	147
4.9.1	Folded cascode stage: Small-signal equiv. circuit	148
4.10	Regulated cascodes	150
4.10.1	Regulated cascodes : output resistance	151
5	Current Mirrors and Current sources.....	153
5.1	Bias current provision on an IC	153
5.1.1	DC Current mirrors	153
5.1.2	Current sources and small-signal gain	154
5.1.3	Current-generation with low accuracy requirement:	155
5.1.4	Current-generation with high accuracy requirement:	156
5.2	Simple Current mirrors	157
5.2.1	Accuracy of Current mirrors	159
5.3	Cascode Current Mirror	162
5.3.1	Cascode Current Mirror - biasing	163
5.3.2	Cascode Current Mirror - output compliance	164
5.3.3	Low voltage cascode Current Mirror.....	166
5.4	Accuracy of Current mirrors - mismatch	167
5.4.1	Layout of current mirrors	168
5.4.2	Random errors due to processing.....	171
5.4.3	V_t variation	172
5.4.4	Mismatch in cascode current mirrors	175

6	Differential Amplifiers	177
6.1	Differential amplifiers - definitions	177
6.2	Differential Gain stage	181
6.2.1	Differential gain stage - Small-signal behaviour	182
6.2.2	Differential stage : Large signal transfer function	183
6.2.3	Differential Gain stage-small signal analysis	188
6.2.4	Differential gain stage - Common-mode response	190
6.2.5	Differential gain stage- CM response (analysis)	191
6.2.6	Common Mode Rejection ratio	193
6.3	Non-Linearity of the differential pair	195
6.3.1	Background: Quantification of non-linearity	196
6.3.2	Non-linearity of a differential pair (analysis)	198
6.4	Miscellaneous Differential Input stages	204
6.4.1	Differential amplifier with resistive load	204
6.4.2	Degenerated differential amplifier with resistive load	205
6.4.3	Differential amplifier with diode load	206
6.4.4	Differential amplifier with folded diode load	207
6.4.5	Differential amplifier with active load	208
6.4.6	Cascode differential amplifier	209
6.4.7	Folded Cascode differential amplifier	210
6.4.8	Problem: Folded Cascode differential amplifier.	211
6.4.9	Fully differential amplifiers - the common-mode problem	212
6.4.10	Fully differential amplifiers with CMFB	215
6.5	Differential-to-single-ended amplifiers	216
6.5.1	Gain of diff. pair with current mirror load (Method 1)	217
6.5.2	Gain of of diff. pair with current mirror load (Method 2)	219
6.5.3	Two-stage differential to single-ended amplifier	221
6.5.4	Cascode differential to single-ended amplifier	222
6.5.5	Folded-cascode differential to single-ended amplifier	223
6.6	Advantages of Differential gain stages	224
7	High-frequency analysis	225
7.1	MOS Device Capacitances	225
7.1.1	Oxide capacitances	226
7.1.2	Diffusion capacitances	227
7.1.3	Cgs,Ggd in linear region	228
7.1.4	Layout for low capacitance	229
7.2	NMOS with capacitances : Small Signal Model	230
7.2.1	CS Gain stage with resistive load and capacitors	231
7.2.2	First-order systems (systems with 1 pole)	234
7.2.3	CS stage with RC load: Analysis including Cgd	235
7.2.4	Maximum frequency of MOS transistor	238
7.3	CS stage with finite source resistance (Miller effect)	242

7.3.1	Miller effect	243
8	Feedback.....	246
8.1	Negative feedback	247
8.1.1	General Negative Feedback system	247
8.1.2	Negative feedback - electronic system	248
8.1.3	Feedback and Opamps	249
8.1.4	Gain sensitivity of negative feedback amplifier	251
8.1.5	Effect of feedback on nonlinearity (distortion)	253
8.2	Feedback and high-frequency effects	254
8.2.1	Feedback and bandwidth	254
8.2.2	Negative feedback and stability	258
8.2.3	Feedback factor and stability	260
8.2.4	Nyquist Stability Criterion	262
8.2.5	Stability of Opamps in feedback configurations	263
8.2.6	Stability of unity-gain configurations.	265
8.2.7	Stability of systems with 1 dominant pole.....	266
9	Frequency compensation	268
9.1	Some options for frequency compensation	269
9.1.1	Frequency compensation (Method 1) illustrated	270
9.1.2	Frequency compensation (Method 2) illustrated	271
9.2	Dominant pole compensation	272
9.3	Compensation of two-stage differential amplifier	283
9.3.1	2-stage amplifier: dominant pole compensation	287
9.3.2	2-stage amplifier: Compensation by pole-splitting (intuitive analysis) ..	289
9.3.3	2-stage amplifier: Dominant-pole compensation (mathematical analysis)	292
9.3.4	2-stage amplifier: Dominant-pole compensation (numerical example)	293
9.3.5	2-stage amplifier: pole-splitting compensation: mathematical approach....	296
9.3.6	2-stage amplifier: pole-splitting compensation: (numerical example)...	300

10 Noise	304
10.1 Signal-to-Noise ratio	305
10.2 Average Power of Noise	306
10.3 Spectrum of noise (frequency content of noise)	307
10.3.1 Common Noise Spectra	308
10.3.2 Spectrum Shaping	308
10.4 Amplitude distribution of noise	309
10.5 Noise summation	310
10.5.1 Uncorrelated and dominant noise sources	311
10.6 Types of Noise	312
10.6.1 Thermal noise	312
10.6.2 Resistor thermal noise	312
10.6.3 MOSFET thermal noise	313
10.6.4 Shot noise	313
10.6.5 Diode Shot noise	313
10.6.6 Flicker noise (1/f noise)	314
10.6.7 MOSFET-Flicker noise (1/f noise)	314
10.6.8 Corner frequency	315
10.7 Noise Bandwidth	316
10.7.1 Noise bandwidth of a first-order filter	317
10.8 Input-referred noise	324
10.9 Circuit noise analysis examples	325
10.10 Opamp gain stage noise	334
10.10.1 Two-stage opamp	334
10.10.2 Input-referred noise of opamp gain stages	335
11 Opamp circuits	343
11.1 Miscellaneous Opamp Non-idealities	343
11.1.1 DC Offset	343
11.1.2 Slew Rate	351
11.1.3 Common-mode input range	356
11.2 Opamp applications	359
11.2.1 Capacitive loads	359
11.2.2 Resistive loads	371

12 Voltage and Current References	375
12.1 Supply-dependent references	375
12.1.1 Resistive Voltage divider	375
12.1.2 Resistor MOS Diode Voltage divider	376
12.1.3 MOS Diode Voltage divider	377
12.2 Supply-independent references	379
12.2.1 Self-biased current reference	379
12.2.2 Constant gm biasing.....	380
12.3 Bandgap Voltage Reference	383
12.3.1 Negative Temperature coefficient Voltage	384
12.3.2 Positive Temperature coefficient Voltage	386
12.3.3 Zero Temperature-Coefficient Voltage.....	387
12.3.4 Bandgap Voltage Reference circuit	388
12.3.5 Bandgap design issues	389
Appendix Bipolar-Junction Transistors (BJT)	391

1 Introduction

1.1 Analog Circuit Design

Concerned with the design of circuits for analog systems and analog signal processing.

Analog Signals e.g. voltage, current, charge

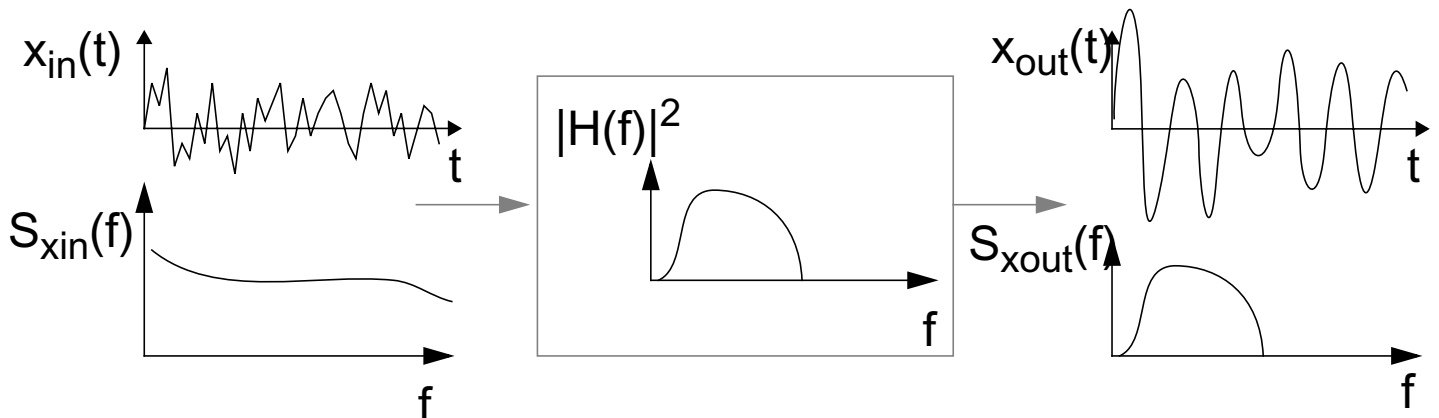
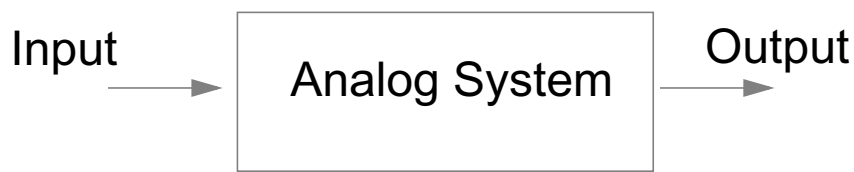
Time-continuous

Amplitude continuous

Signal Processing

Amplification

Filtering



Specifications:

Gain

Frequency Response

Signal-to-Noise Ratio

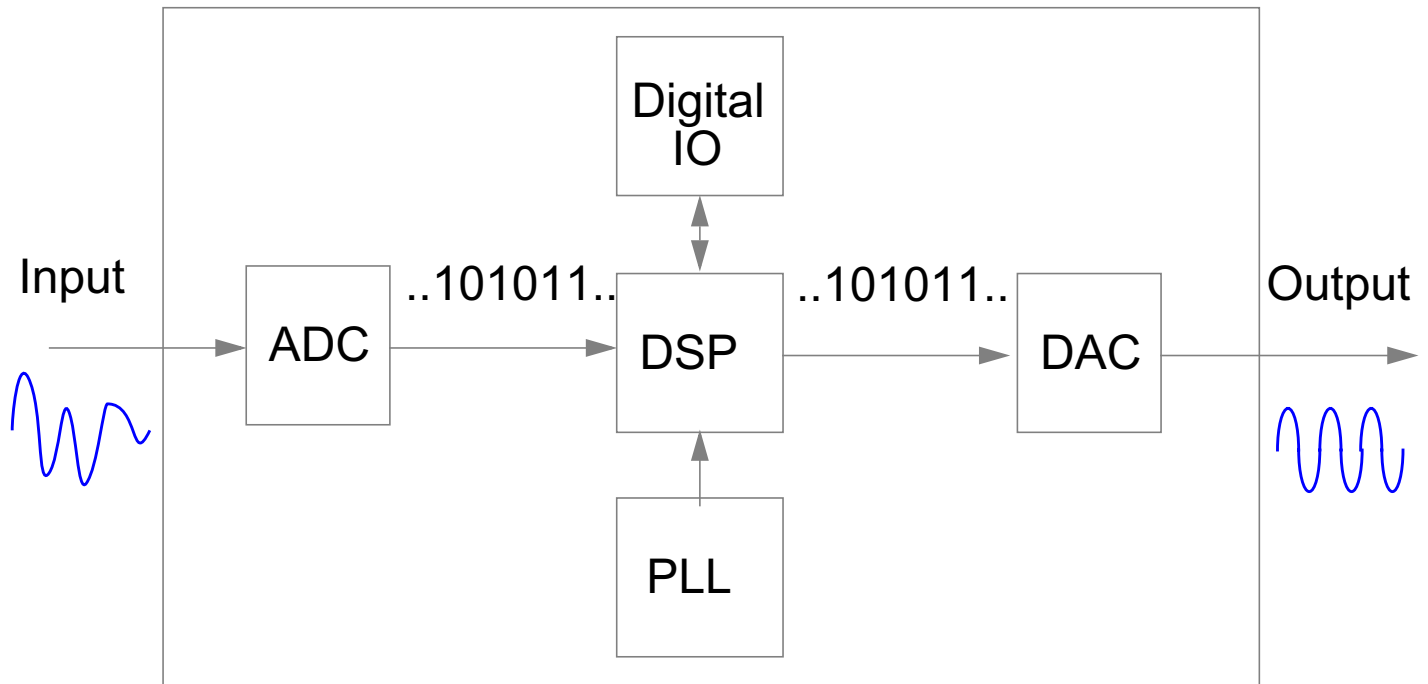
Linearity

Offset

1.2 'Mixed-Signal' Circuit Design

Growth in IC industry is driven by digital.

Signal processing moving into digital domain-DSP



Need for more analog/mixed signal circuitry to support DSP:

A/D, D/A converters

Reference circuitry

PLLs

Digital IO Buffers

Specifications:

Resolution

Range

1.3 Historical Overview

Where are analog circuits used?

Up to 1980's mainly analog IC's

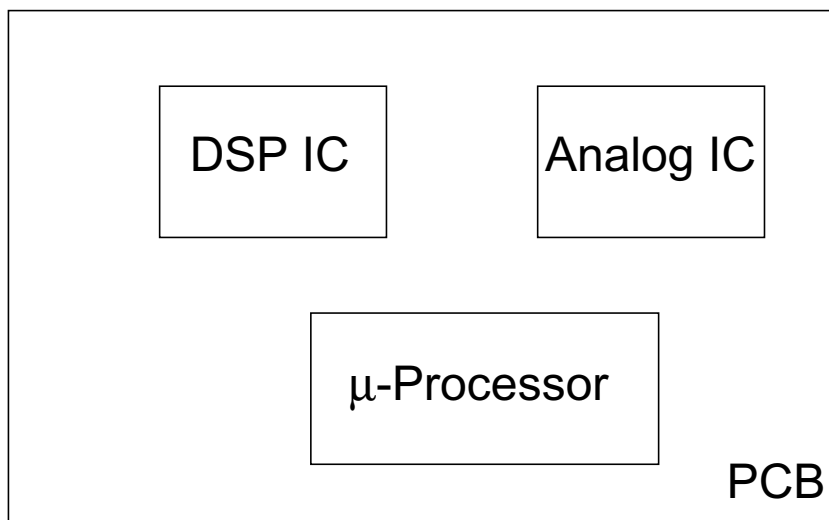
Discrete opamps

Power amps

1980's, 1990's more integration

e.g. CCTV

Compact Disc



Today:

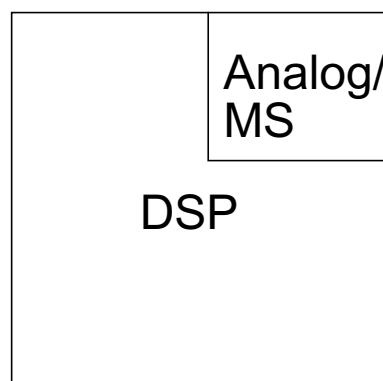
Ever more digital signal processing power on a single chip

This drives the development of the IC industry

There are still analog circuits on the chip (System on Chip)

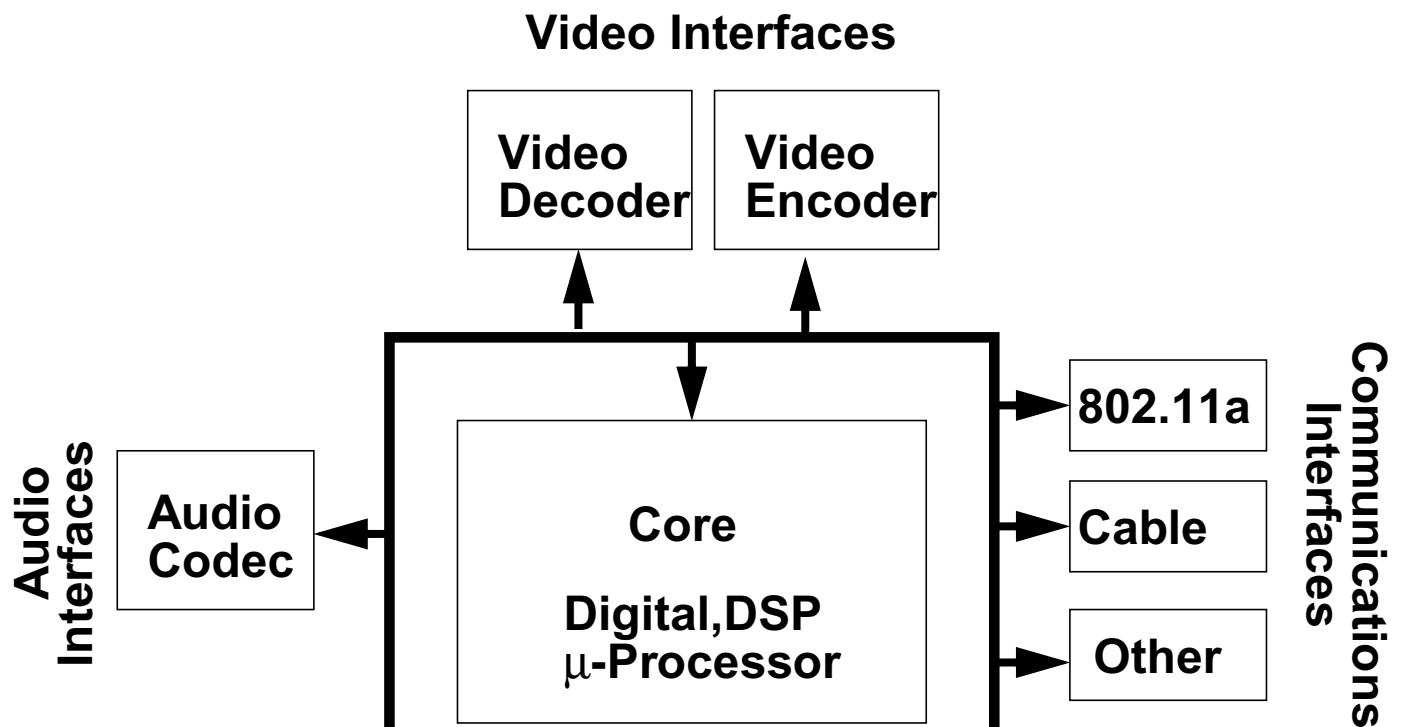
Or you can partition product into separate analog and digital chips

Also digitally-assisted analog circuits - use digital calibration to correct imperfections in the analog design.

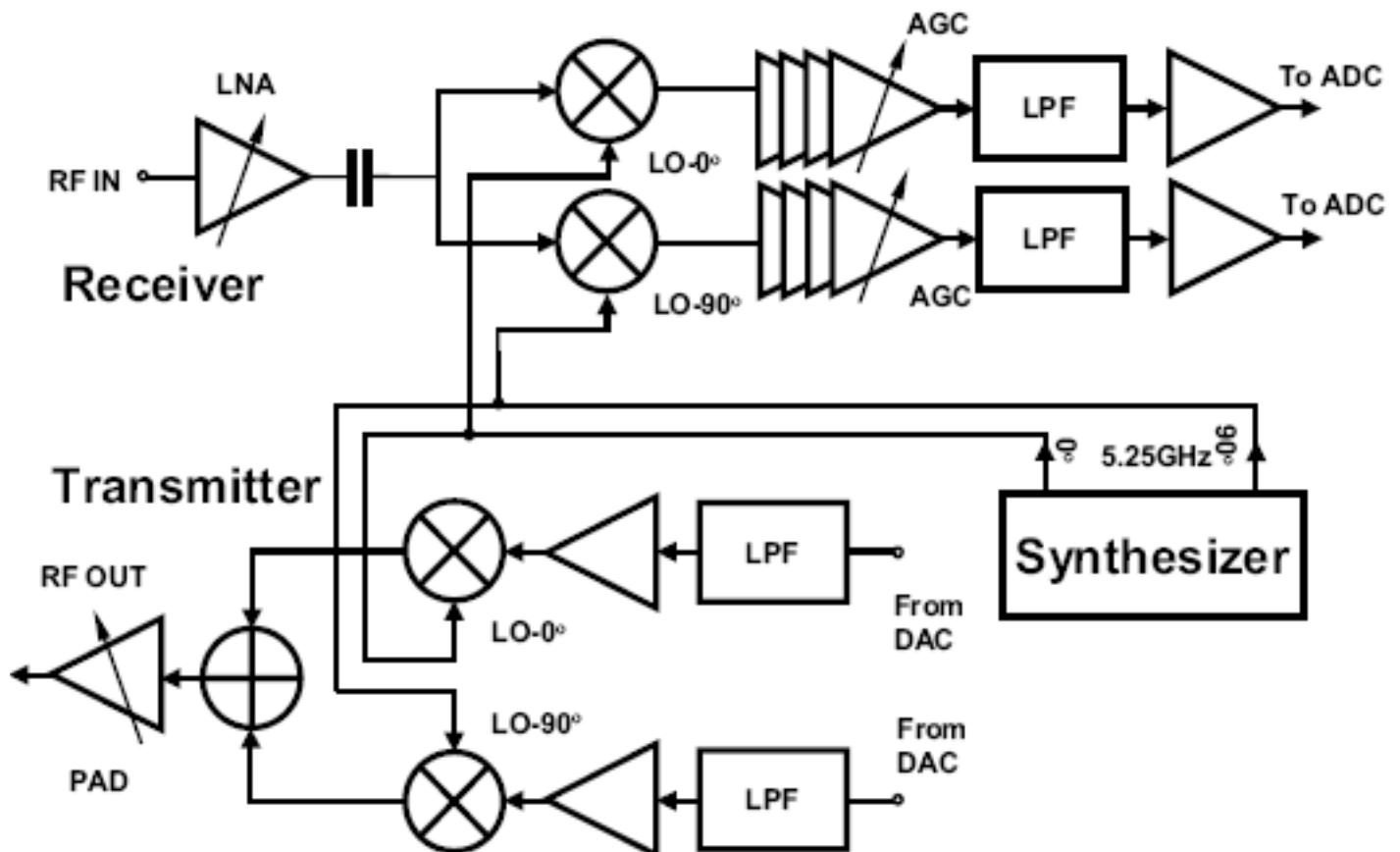


Where are analog and mixed-signal circuits used?

Primarily as interface circuits e.g. front-end signal processing for wireline and wireless communications systems transceivers.

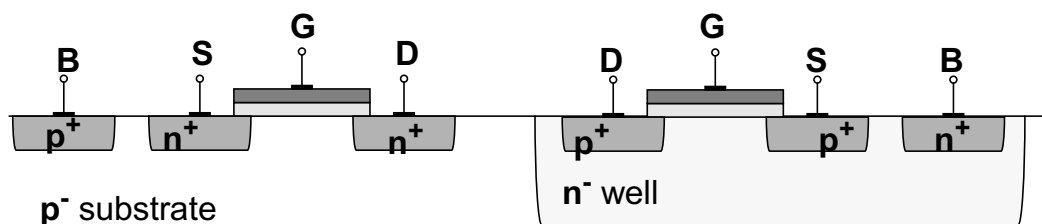


e.g. direct conversion CMOS transceiver for IEEE 802.11a WLANs

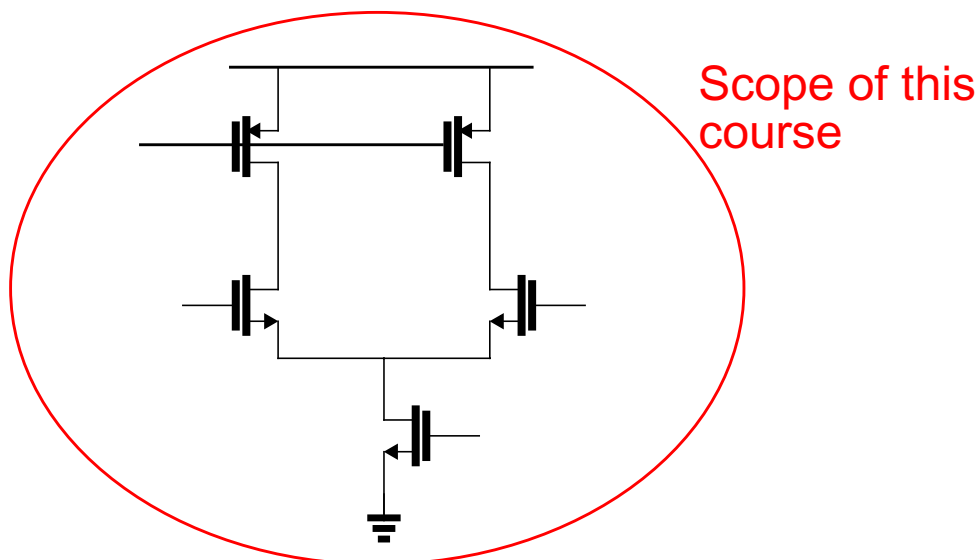


1.4 Analog design - levels of abstraction

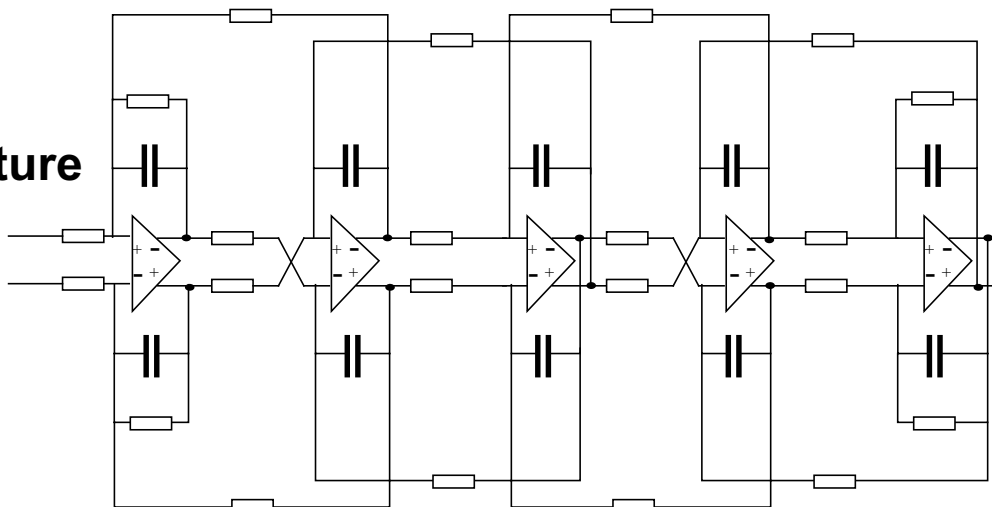
Device



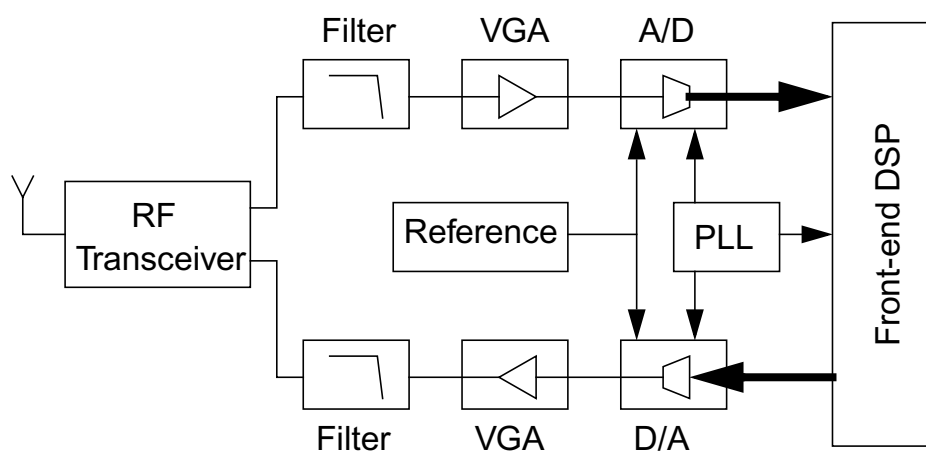
Circuit



Architecture



System



1.5 Course Objective

To provide a basic understanding of transistor-level circuit design.

This is especially important for analog designers but RF, digital and system designers also need a good grounding in transistor level circuits.

The focus of the course will be integrated analog CMOS design.

1.6 Course Contents

Introduction

Review of MOS transistor basics

MOSFET structures

MOSFET operation

Derivation of IV characteristics

Second-order effects

Basic Circuit Techniques

Review of network elements and concepts

Small-signal analysis

Small-signal equivalent circuit

Transistor small-signal parameters

Small-signal model

Single stage amplifiers

Common-source stage

Source follower stage

Common-gate stage

Cascode stage

Current Sources and Current Mirrors

Basic current sources

Cascode current mirror

Static and random errors

Layout aspects

Differential amplifiers

Single stage differential amplifier

Common-Mode Rejection Ratio

Power-Supply Rejection Ratio

Two-stage differential amplifier

Frequency Effects

MOS device capacitances
High-frequency small-signal model
Frequency response of transistor gain stages
Bode diagrams

Feedback

General negative feedback system
Feedback effects
Stability and feedback

Opamps

Single-stage opamps
Two-stage opamps
Opamp non-idealities
Frequency compensation
Opamp applications
Filtering

Noise

Noise Power Spectral Density
Noise amplitude
Noise types and device noise
Noise bandwidth
Noise analysis of simple gain stages.

Voltage and Current references

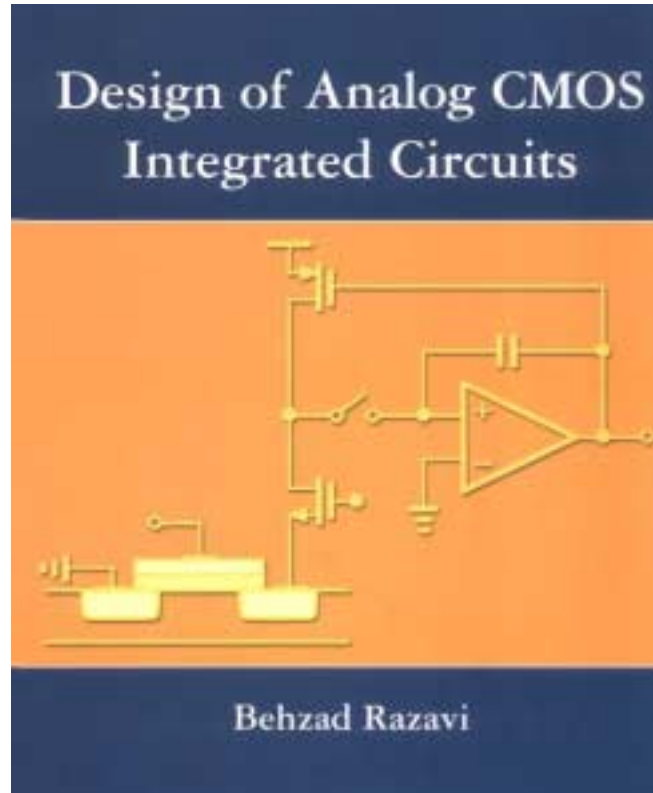
Supply-independent references
Bandgaps

1.7 Recommended books

Design of Analog CMOS Integrated Circuits

Behzad Razavi

McGraw-Hill Inc



Bipolar and MOS Analog Integrated Circuit Design

David Johns, Ken Martin

John Wiley & Sons

Cmos Circuit Design, Layout, and Simulation

R. Jacob Baker, Harry W. Li, David E. Boyce

Institute of Electrical & Electronic Engineers

CMOS Analog Circuit Design

Philip E. Allen, Douglas R. Holberg

Oxford University Press Inc, USA

Analysis and Design of Analog Integrated Circuits

Paul Gray, Paul Hurst, Stephen Lewis, Robert Meyer

John Wiley and Sons

1.8 General Course Items

Lecture notes will be given as handouts and made available in pdf format.

Each section concludes with a circuit analysis-type problem.

The problem solution as well as any relevant supplementary notes will be discussed in the following class

Classes (TP1):

Tue 1200-1300 O'Kane B10A

Fri 0900-1000 Elec L1

Note: It will not be possible to fulfill all these times in TP1, so there will still be some catch-up lectures in TP2 (Fri 0900-1000)

Exam

4 questions, attempt 3, 1.5 hrs

Questions are problem-based, similar to problems in notes.
70% of the module marks are allocated to the written exam.

Labs

The course includes 4 circuit design Lab sessions, plus a Lab assignment.

The Labs sessions are planned for early 2014.

Tentative: 4 sessions on Mon/Tue 1600-1900 Elec L3

These Labs cover the basics of analog CAD analog using the industry-standard Cadence Virtuoso Open Access design flow, also known as Cadence IC6.

The labs focus on the Cadence Composer schematic entry tool and on using the Cadence Spectre transistor-level simulator through the Analog Design Environment interface.

The goals of the labs are to familiarise the student with the Cadence Virtuoso Open Access design flow, with the Cadence Spectre simulator, and with the concepts of process models and simulation types through simulating some of the circuits from the UE4002 course. Comparison of results derived from hand calculations with those obtained from simulations is also highlighted.

30% of the module marks are allocated to the labs.

2 Review of MOS Transistor basics

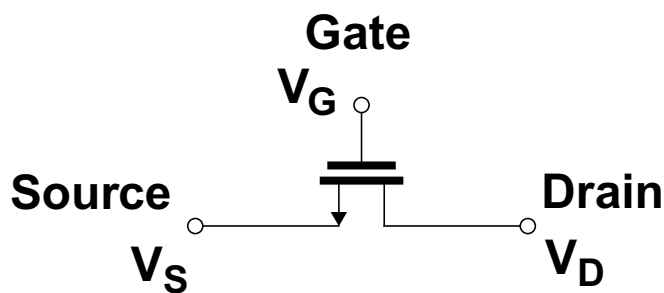
Basic uses of a MOS transistor:

1. As a switch \Rightarrow digital
2. Amplification \Rightarrow analog

2.1 MOSFET switch

MOSFET = Metal-Oxide-Silicon Field Effect Transistor

n-type MOSFET (NMOS) as a switch:



If V_G is high w.r.t. V_S or V_D then drain is connected to the source:

Questions:

For what value of V_G does the device turn on?

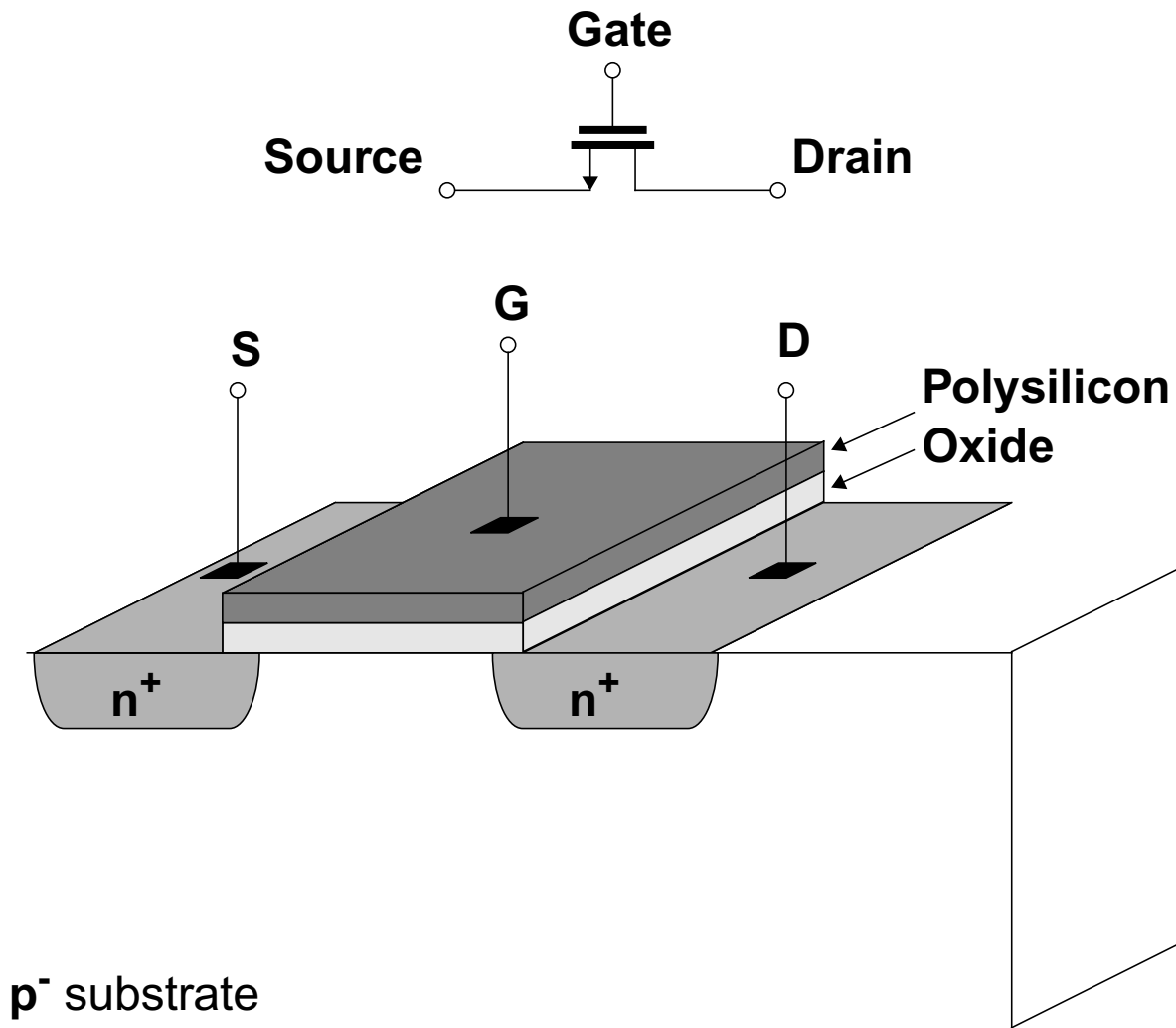
What is the resistance between source and drain?

What does this resistance depend on?

How fast can the switch operate?

2.2 NMOS device structure

NMOS



p- (lightly doped, high ohmic) substrate (bulk)

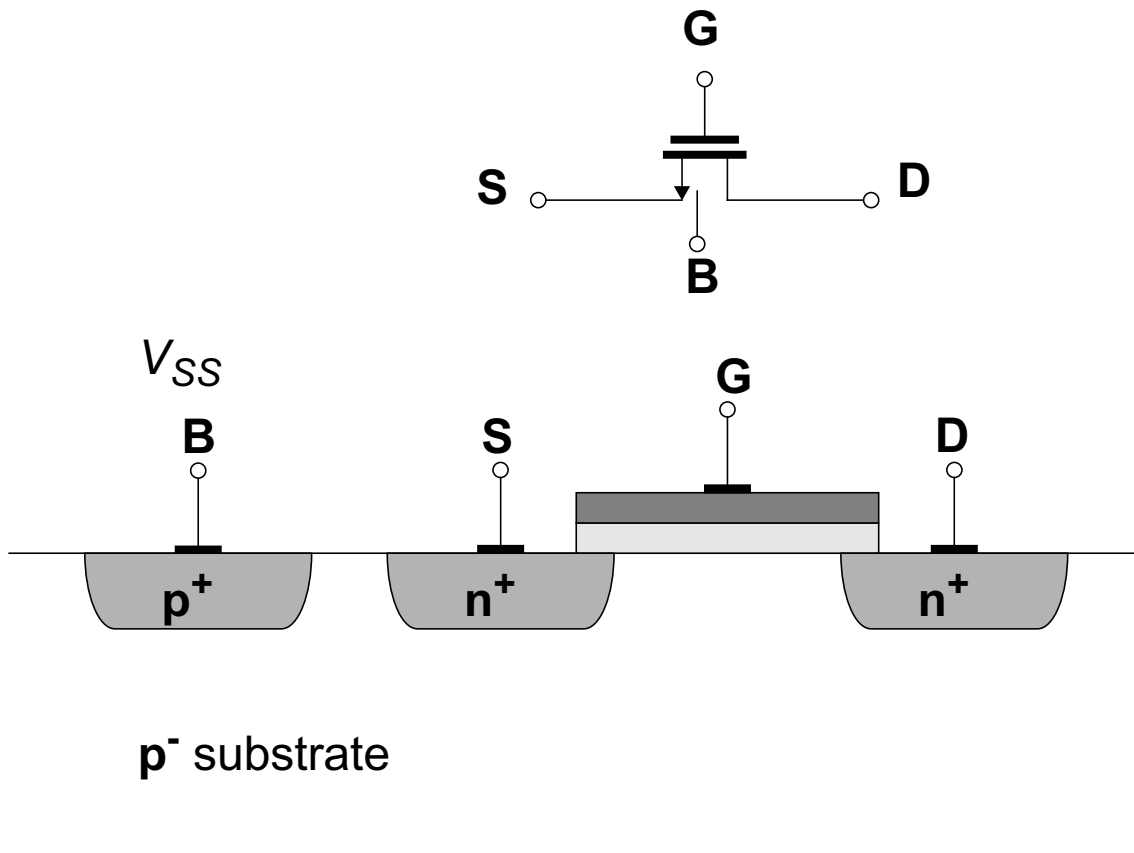
n+ (heavily doped, lower ohmic) source, drain diffusions/implants

Polysilicon (heavily doped, low ohmic) gate

Gate oxide (SiO₂, insulating)

2.2.1 Backgate connection

Need to define the bulk potential - fourth terminal
Connect to the most negative supply



Basic operation:

Positive voltage on Gate w.r.t. substrate leads to repulsion of p-type carriers in the substrate and (for increased gate voltage) formation of n channel underneath gate.

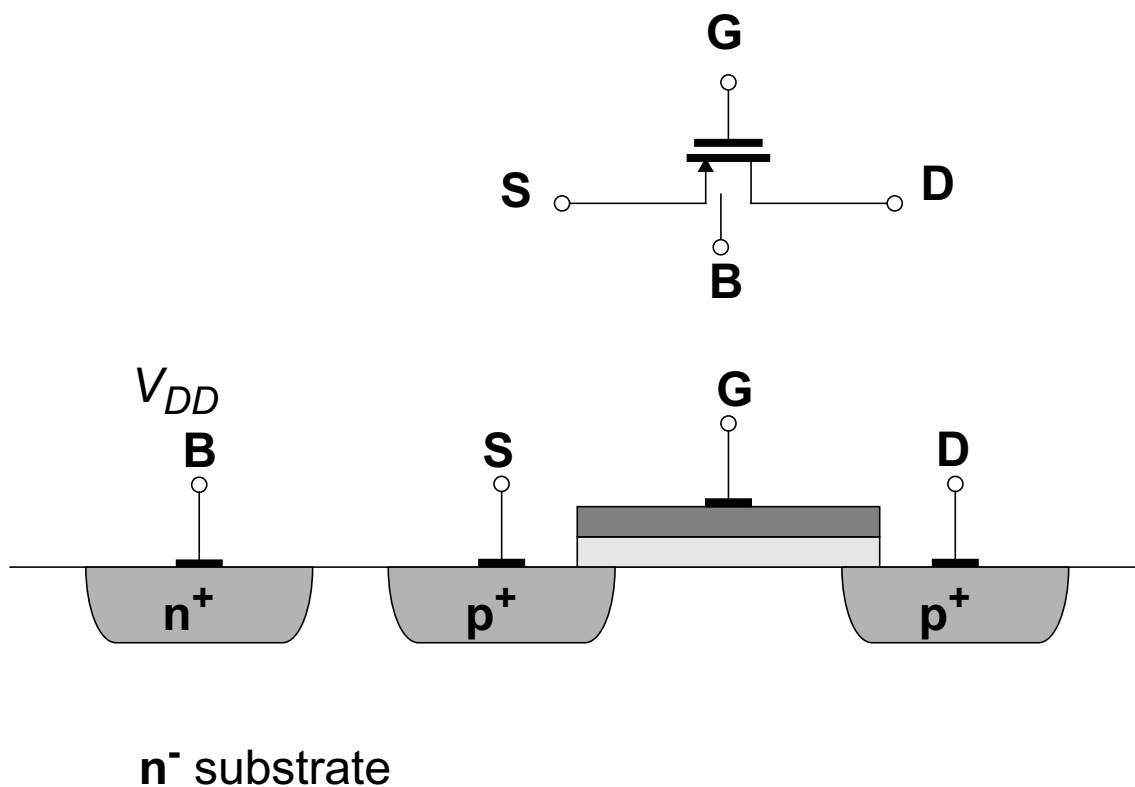
Current can flow if potential applied between drain and source

Note: 'active' channel under gate region

MOS devices are 'surface' devices

Isolation enables large scale integration

2.3 PMOS device structure



Connect bulk to the most positive supply,
so p-n junctions reverse-biased

Basic operation:

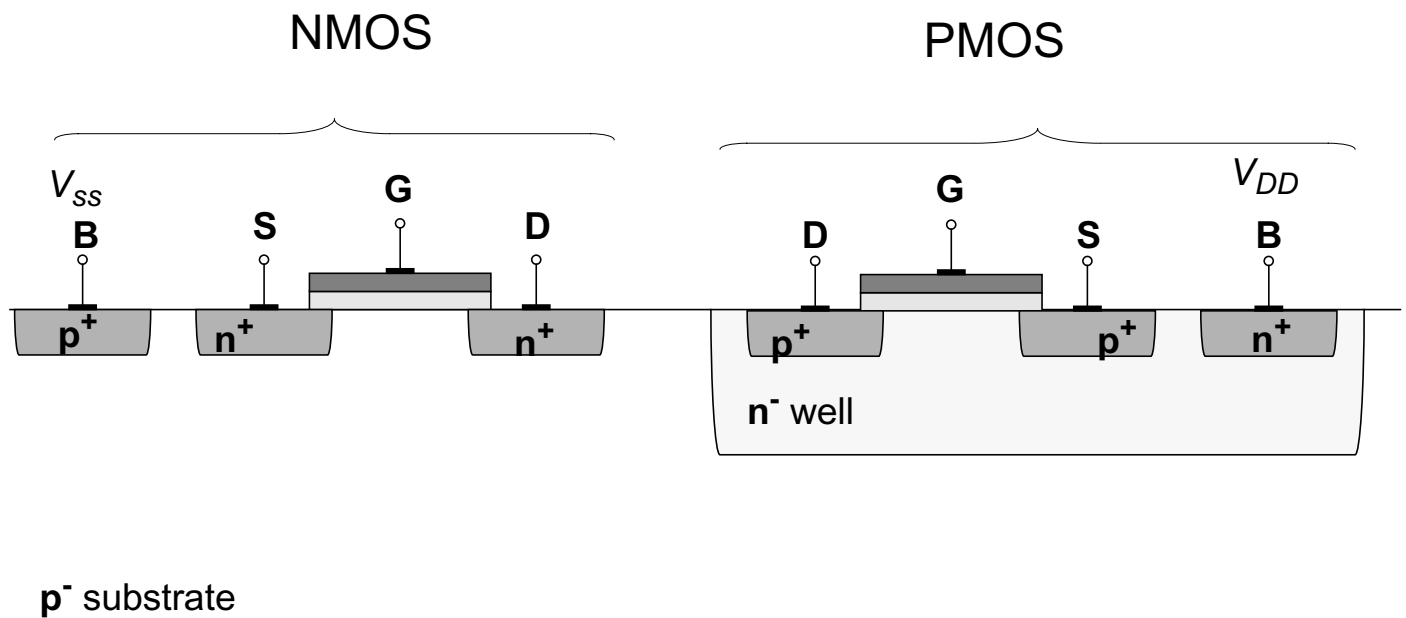
Negative voltage on Gate w.r.t. substrate leads to repulsion of n-type carriers in the substrate and (for increased gate voltage) formation of p channel underneath gate.

Current can flow if potential applied between drain and source

2.4 CMOS technology

(Complementary MOS)

Integrate NMOS and PMOS on single wafer



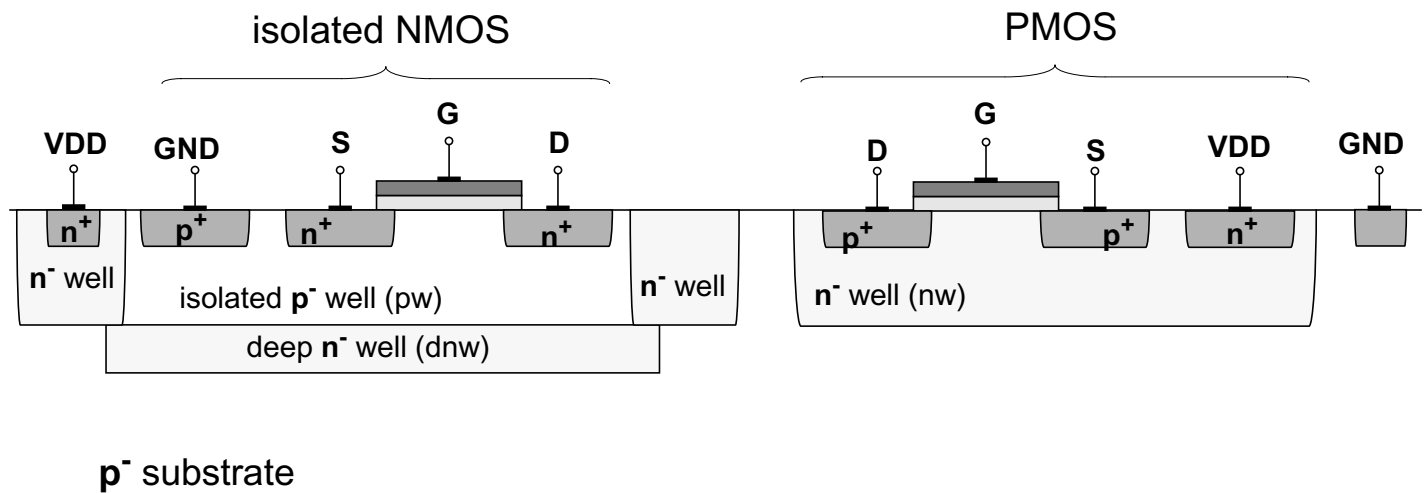
N.B. n well technology shown (n substrate with p well also possible)

pmos devices have own bulk.

Connect p substrate to most negative supply (usually ground)

Connect n well to the most positive supply (of the well or system)

2.4.1 CMOS with DNW



Some processes have a deep nwell option.

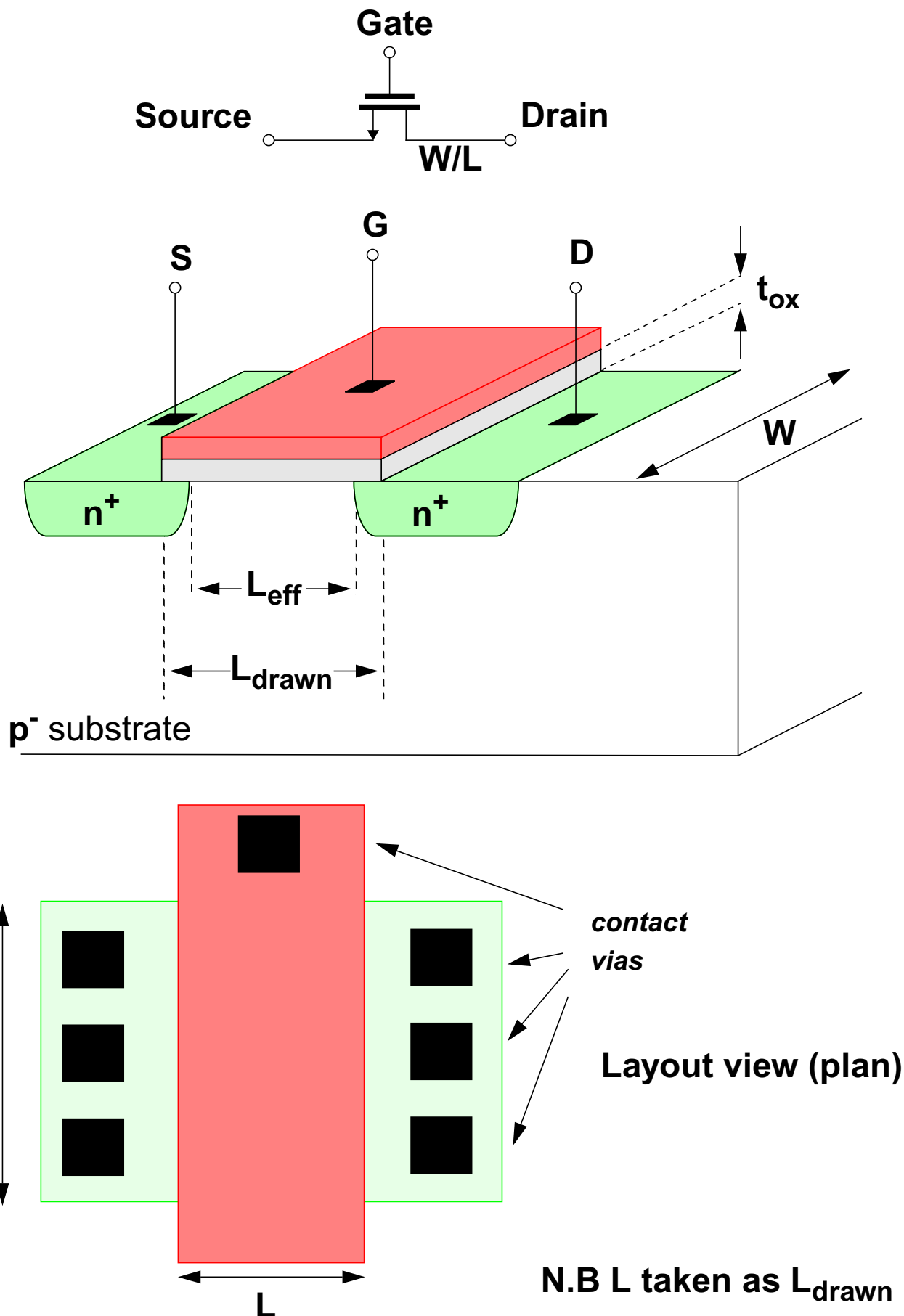
This allows isolation of NMOS from the substrate

Connect p substrate to most negative supply (usually ground)

Connect n well to the most positive supply (of the well or system)

Connect isolated p well to the most **negative** supply (of the well or system).

2.5 MOSFET dimensions



2.6 MOSFET dimensions (scaling)

Moore's Law (1975): Number of transistors per chip will double every 18 months

Year	V_{DD}	L_{min}	T_{ox}
1990	5V	1 μ m	30nm
1996	3.3V	0.35 μ m	7.5nm
1998	2.5V	0.25 μ m	5nm
2000	1.8V	0.18 μ m	3.5nm
2002	1.2V	0.13 μ m	2.5nm
2004	1-1.2V	0.09 μ m	2.0nm
2006	1-1.2V	65nm	1.5nm
2008	1V	45nm	1nm
2012	1V	28nm	~1nm

Good news for digital design

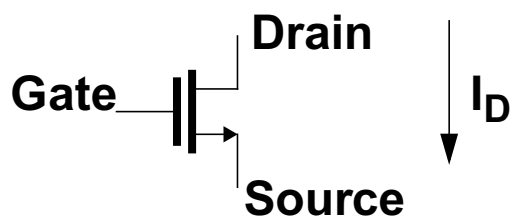
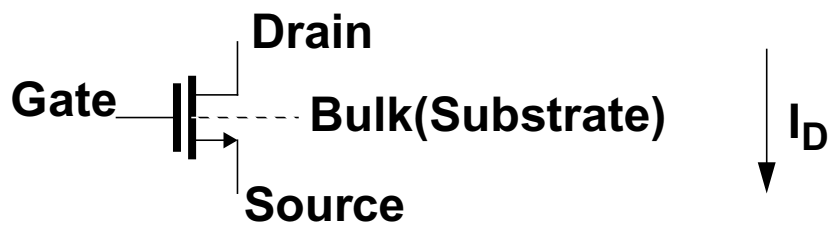
Some good news for analog design

But fundamental problems:

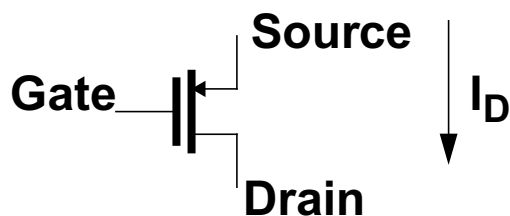
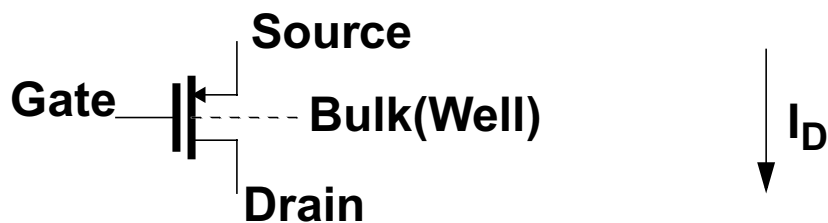
- 1.Reduced V_{DD} => reduced headroom, S/N ratio
- 2.Transistors have poor analog properties e.g. low gain
- 3.Productivity
- 4.Interference

For 0.18 μ m processes and below, a 3.3V/2.5V process option is often provided and used for the analog circuitry (cheaper than re-designing analog circuitry to a lower supply voltage in a new generation process)

2.7 MOSFET Symbols



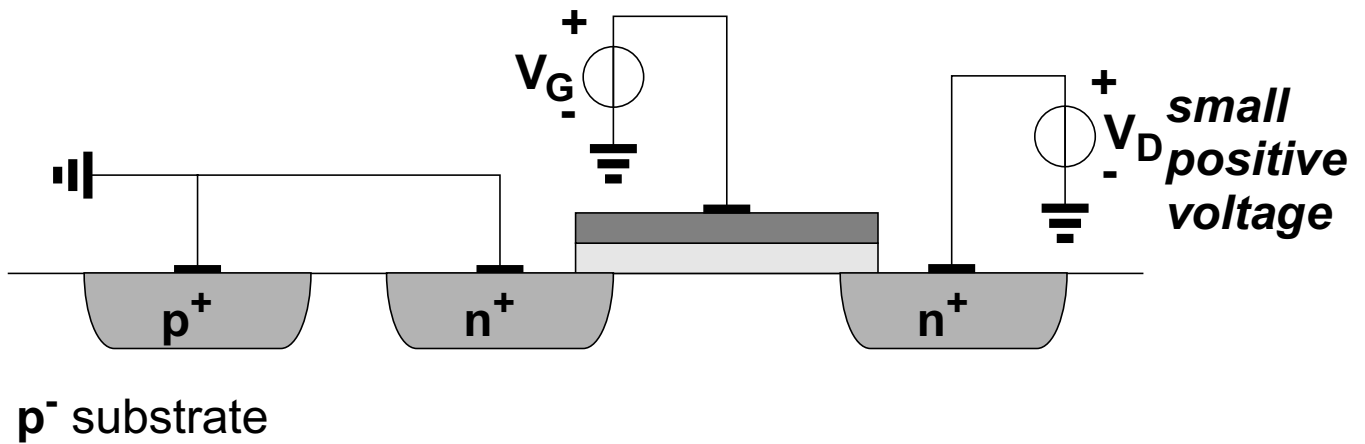
Used when substrate is tied to V_{SS} as is generally the case



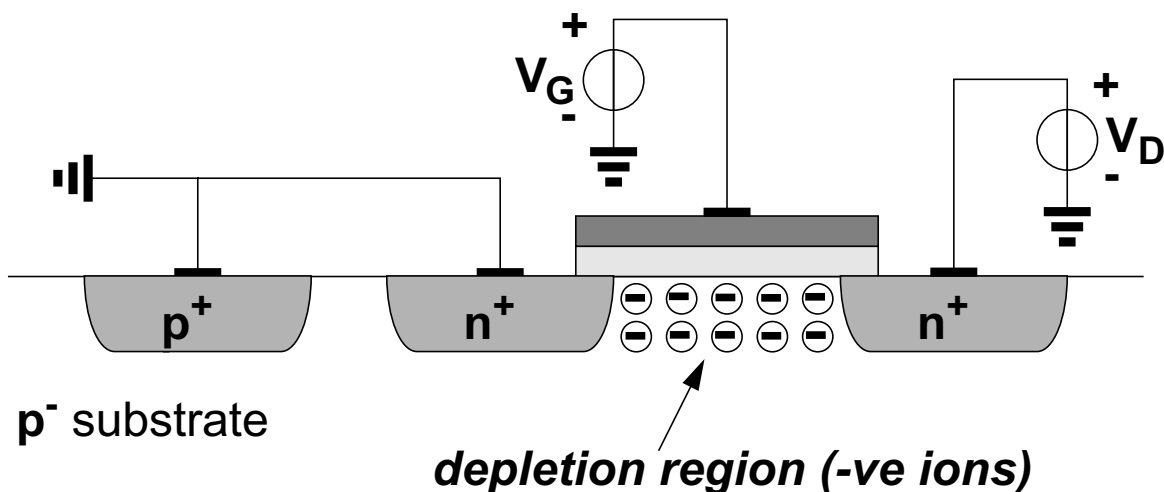
Used when well is tied to V_{DD}

2.8 MOSFET Operation

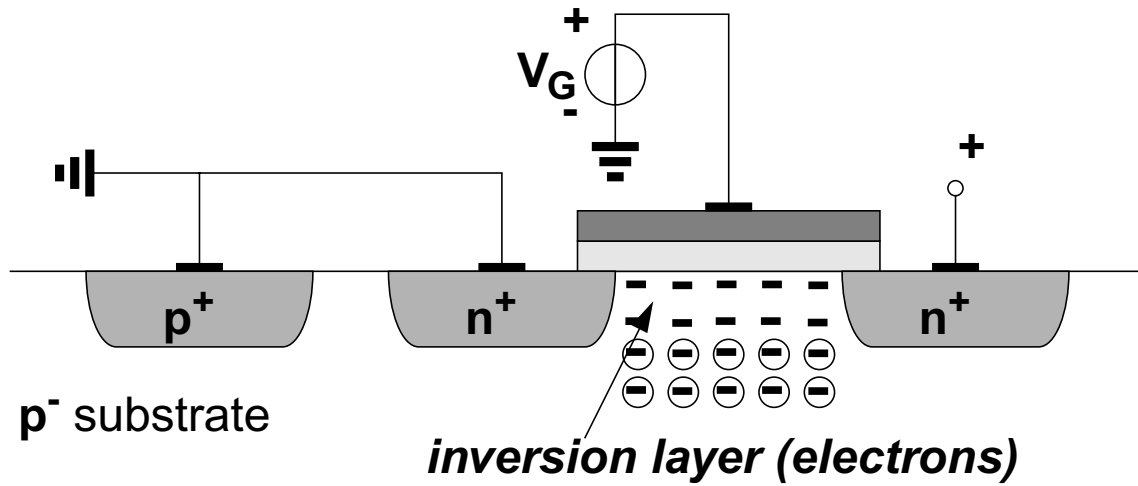
1. Bulk, source grounded, drain positive, apply positive gate voltage



2. As V_G increases, holes repelled under gate \Rightarrow depletion region



3. V_G increases further, potential under oxide increases => inversion
Electrons flow from source through channel to drain



2.9 Threshold voltage

Voltage at which the transistor 'turns on'.

Defined as the gate-source voltage at which the concentration of electrons under the gate is equal to the concentration of holes in the p- substrate.

$$V_t = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

Φ_{MS} = difference between gate and Si work functions.

$2\Phi_F$ = surface potential change.

Q_{dep} = charge in the depletion region

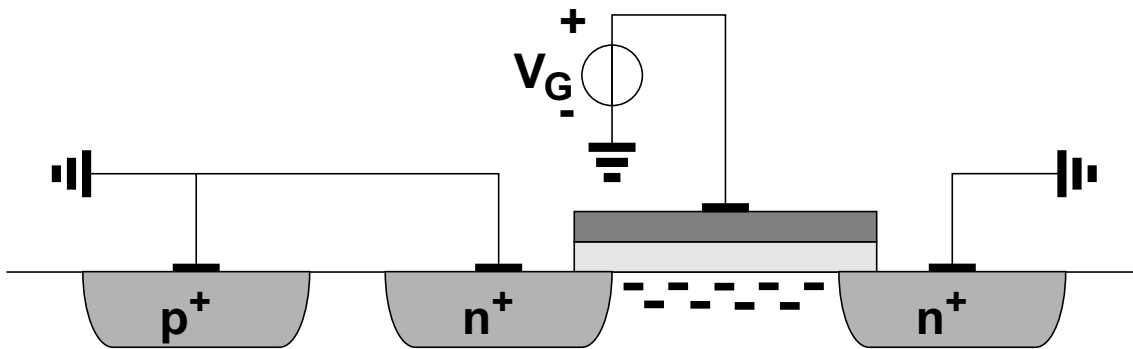
C_{ox} = gate oxide capacitance per unit area

Note: This is a physical definition. The actual quoted value is measured from IV characteristic.

Often in terms of V_G required for a certain I_D/W

2.10 Derivation of IV characteristic

What happens when $V_{GS} > V_t$



p^- substrate

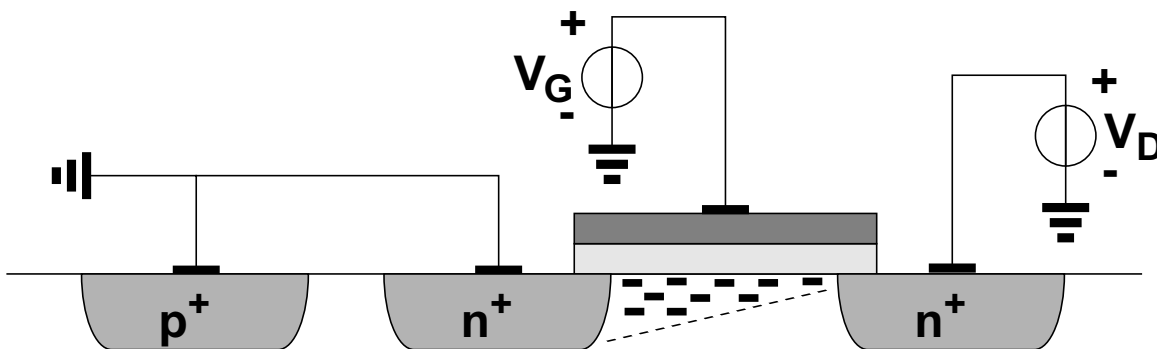
As V_G increases extra charge on gate mirrored in channel

Charge in channel:

$$Q = WLC_{ox}(V_{GS} - V_t) \quad (\text{from } Q = CV \quad C = \frac{\epsilon A}{D} \equiv C_{ox} \cdot A)$$

Charge density

$$Q_d = WC_{ox}(V_{GS} - V_t)$$



p^- substrate

If V_D is increased then charge density at point x along channel:

$$Q_d(x) = WC_{ox}(V_{GS} - V(x) - V_t)$$

Current is given by charge density times charge velocity:

$$I_D = -WC_{ox}(V_{GS} - V(x) - V_t)v$$

$$I_D = -WC_{ox}(V_{GS} - V(x) - V_t)v$$

$$I_D = WC_{ox}[V_{GS} - V(x) - V_t]\mu_n \frac{dV}{dx} V(x)$$

from $v = \mu_n E$ charge mobility x electric field

$$\text{and } E = -\frac{dV}{dx}$$

Integrating

$$\begin{aligned} \int_{x=0}^L I_D dx &= \int_{V=0}^{V_{DS}} WC_{ox}\mu_n(V_{GS} - V(x) - V_t)dV \\ &= \int_{V=0}^{V_{DS}} \mu_n C_{ox} W [(V_{GS} - V_t) - V(x)] dV \end{aligned}$$

Since I_D is constant along the channel

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

This equation describes a parabola

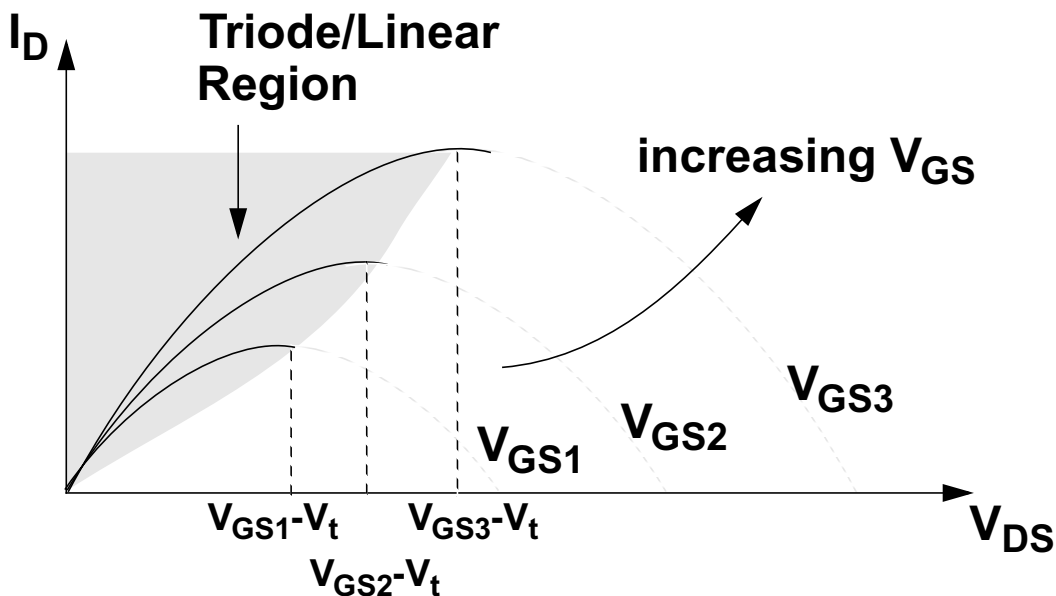
What is maximum current?

$$\frac{\partial I_D}{\partial V_{DS}} = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_t) - V_{DS}]$$

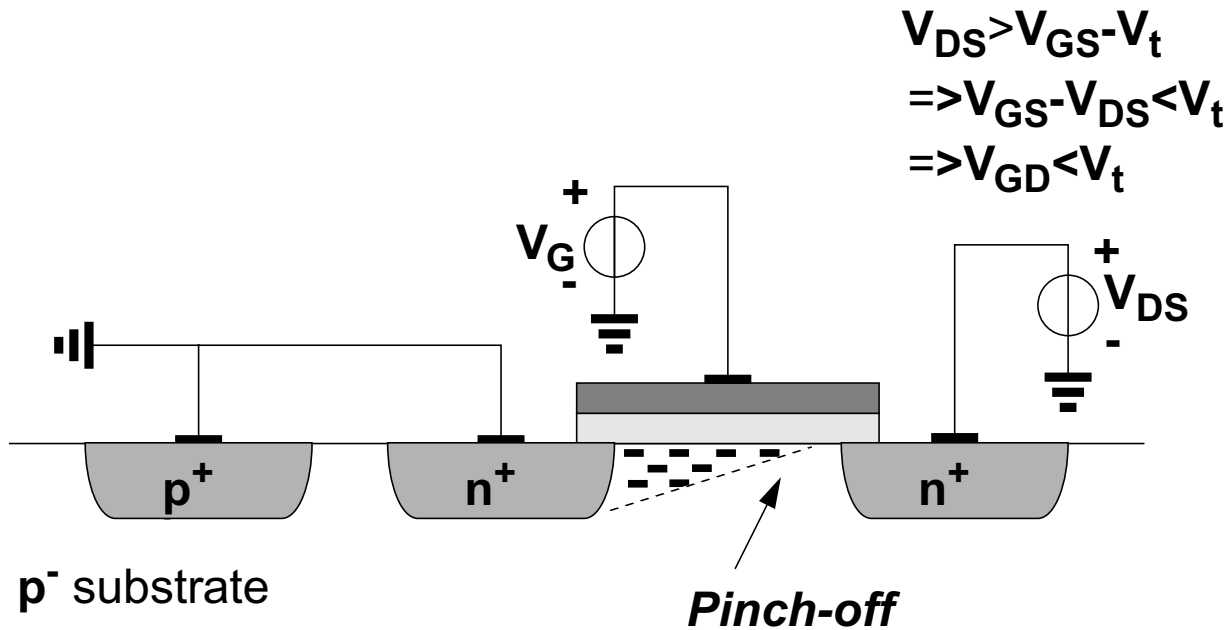
=> Peak is when $V_{GS} - V_t = V_{DS}$ and peak current is

$$I_{D,max} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t)^2 - \frac{(V_{GS} - V_t)^2}{2} \right]$$

$$I_{D,max} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$



What happens when V_{DS} is increased beyond this maximum?



When $V_{DS} > V_{GS} - V_t$, the effective gate drive at the drain end of the channel is insufficient to support the inversion layer i.e. $V_{GD} < V_t$ and the channel is pinched-off

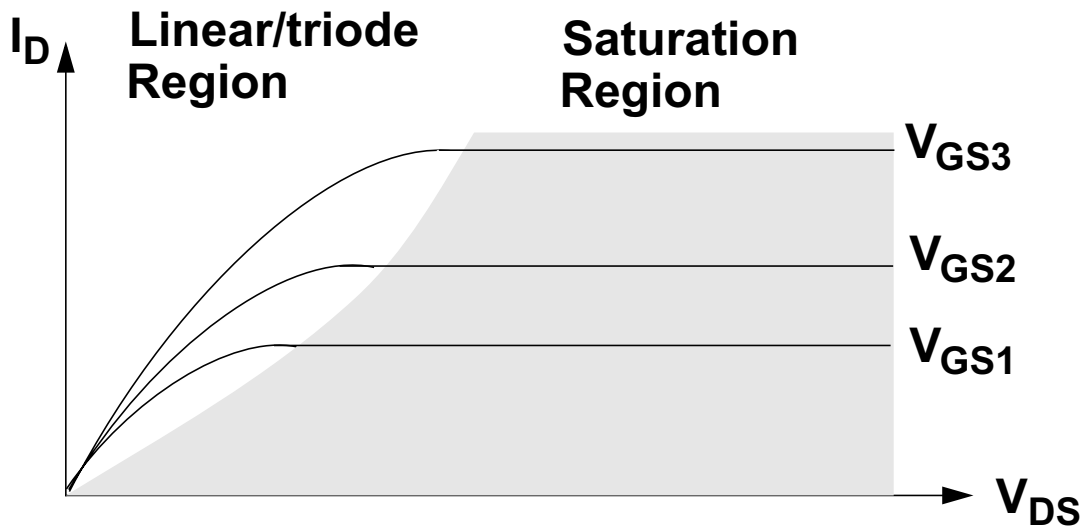
(

I_D does not increase any more with increasing V_{DS} .

This is referred to as channel saturation.

Current in saturation is given by

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$



Saturation (Active) Region

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

This equation is known as the MOS **square-law** relationship.
Note

$$I_D = f(\mu_n C_{ox}) \quad \text{Technology}$$

$$I_D = f(V_{GS} - V_t)^2 \quad \text{Bias conditions}$$

$$I_D = f\left(\frac{W}{L}\right) \quad \text{Geometry}$$

2.11 MOS Operating Regions

Three distinct regions of operation

NMOS (V_t positive)

1. **Cutoff** : $V_{GS} \leq V_t$

$$I_D = 0$$

2. **Triode (Linear)** $V_{GS} - V_t > 0$ and: $V_{DS} < V_{GS} - V_t$

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

3. **Saturation** $V_{GS} - V_t > 0$ and: $V_{DS} \geq V_{GS} - V_t$

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_t)^2$$

PMOS (V_t negative)

1. **Cutoff** : $V_{GS} \geq V_t$

$$I_D = 0$$

2. **Triode (Linear)** $V_{GS} - V_t < 0$ and: $V_{DS} > V_{GS} - V_t$

$$I_D = -\mu_p C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

3. **Saturation** $V_{GS} - V_t < 0$ and: $V_{DS} \leq V_{GS} - V_t$

$$I_D = -\frac{\mu_p C_{ox} W}{2L} (V_{GS} - V_t)^2$$

Note:

$V_{GS}-V_t$ effective drive voltage sometimes referred to as V_{GT} or V_{EFF}

The minimum value for V_{DS} for the transistor to be in saturation (i.e. $V_{GS}-V_t$) is also known as V_{sat} , V_{dsat}

The quantity $\mu_n C_{ox}$ ($\mu_p C_{ox}$) is often referred to as β_n (β_p) or as K_n (K_p)

Triode region is also known as linear region. Why?

For low values of V_{DS} , specifically if $V_{DS} \ll 2(V_{GS}-V_t)$ then

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS}-V_t)V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (1)$$

becomes

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS}-V_t)V_{DS} \quad (2)$$

i.e. the drain current is a linear function of V_{DS} , the drain-source voltage

=> channel is a linear resistor with a resistance given by

$$R_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS}-V_t)} \quad (3)$$

Resistance is determined by gate overdrive voltage

Note that in cutoff region $R_{DS} = \infty$.

Application as variable, controllable resistor in:

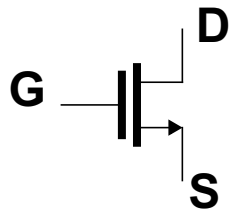
Gain-control circuits

Filtering applications

Problems: NMOS Operating regions

1. What is the operating region of the following nmos transistors?
Take $V_t = 1V$ and assume the bulk is tied to the source.

(i)

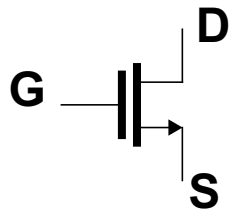


$$V_G = 2V$$

$$V_S = 0V$$

$$V_D = 3V$$

(ii)

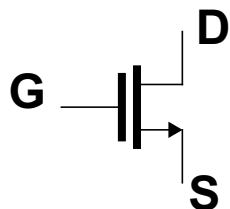


$$V_G = 2V$$

$$V_S = 0V$$

$$V_D = 0.5V$$

(iii)

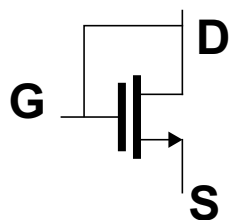


$$V_G = 0.5V$$

$$V_S = 0V$$

$$V_D = 3V$$

(iv)



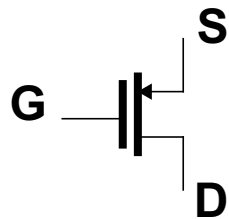
$$V_S = 0V$$

$$V_D = 2V$$

Problems: PMOS Operating regions

1. What is the operating region of the following pmos transistors?
Take $V_t = -1V$ and assume the bulk is tied to the source.

(i)

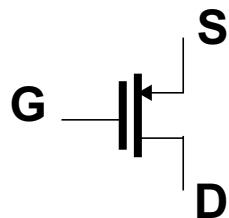


$$V_G = 3V$$

$$V_S = 5V$$

$$V_D = 3V$$

(ii)

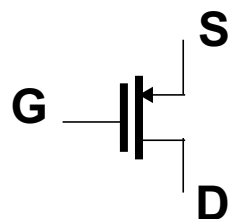


$$V_G = 3V$$

$$V_S = 5V$$

$$V_D = 4.5V$$

(iii)

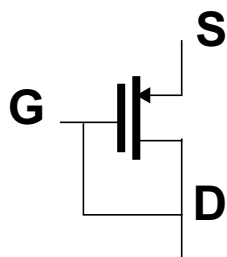


$$V_G = 4.5V$$

$$V_S = 5V$$

$$V_D = 3V$$

(iv)



$$V_S = 5V$$

$$V_D = 3V$$

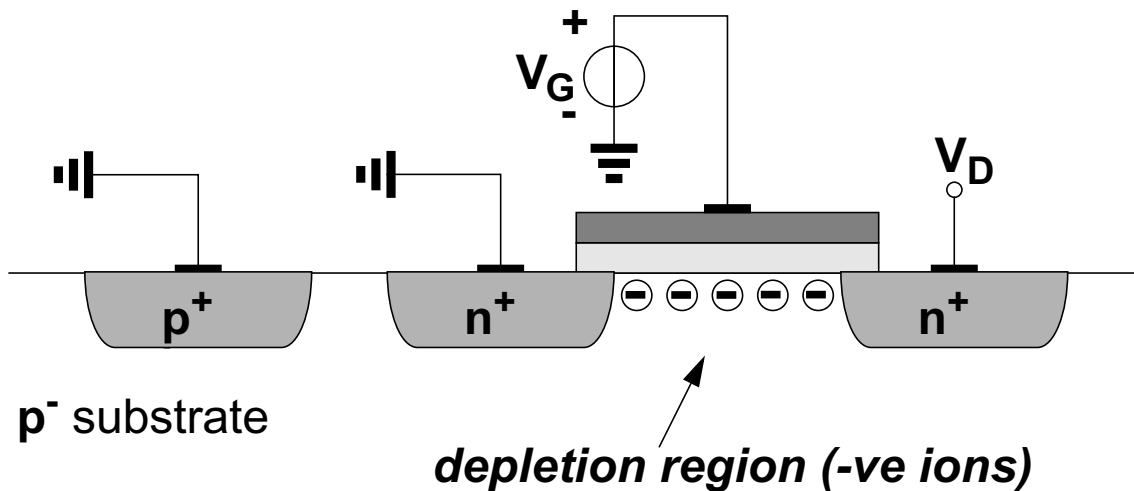
2.12 Second-Order Effects

2.12.1 Body effect

When source and bulk are at the same potential then we define

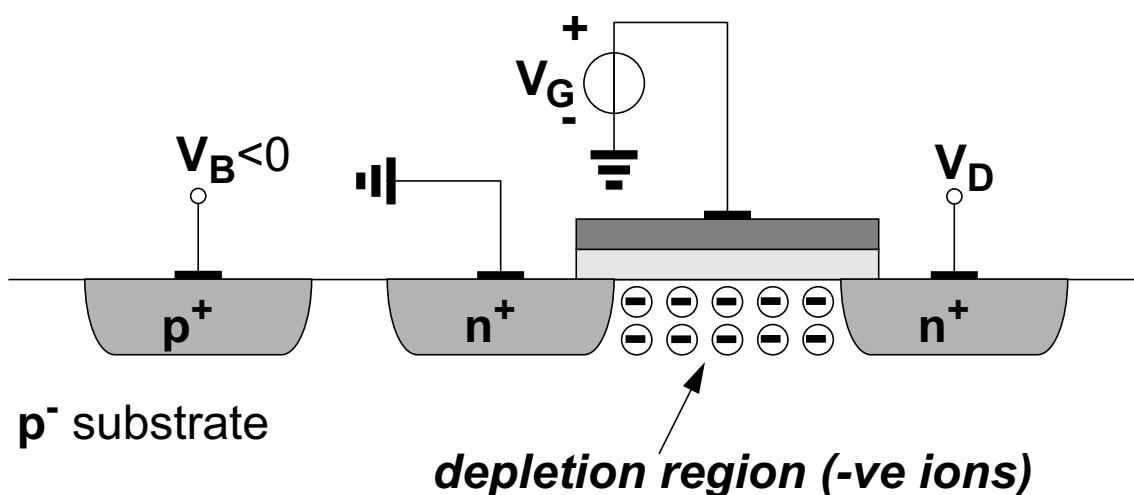
$$V_t = V_{t0}$$

If $V_B < V_S$ then V_t increases - body effect



V_G just under $V_t \Rightarrow$ depletion layer under gate

If V_B is made negative then positive charge is attracted away from channel \Rightarrow depletion layer increases



Total charge on gate must be increased to compensate extra charge in depletion layer i.e. V_G must increase.

$$V_t = V_{to} + \gamma(\sqrt{2|\Phi_F| + V_{SB}} - \sqrt{2|\Phi_F|})$$

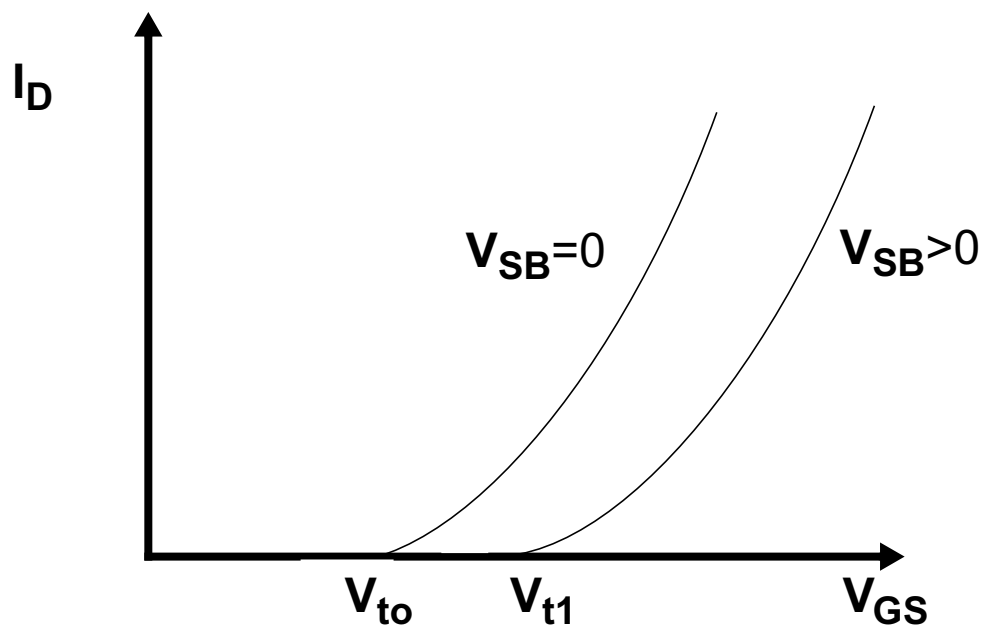
$$\gamma = \frac{\sqrt{2q\epsilon_{Si}N_{sub}}}{C_{ox}}$$

$$V_{to} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

γ = body effect constant (typically $0.3V^{0.5}$)

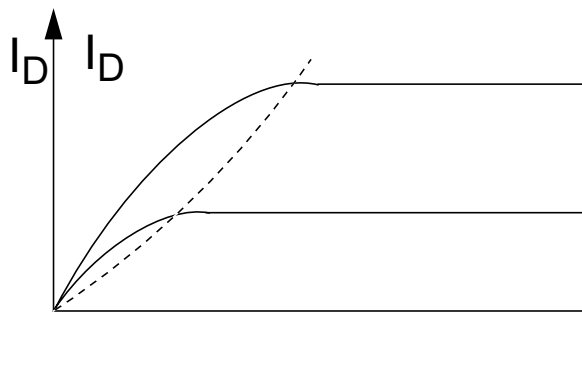
dependancy on $N_{SUB} \Rightarrow$ higher for well transistors

Body effect is an undesirable second order effect

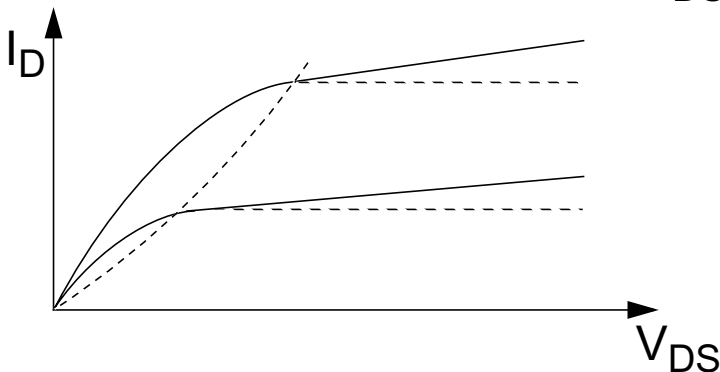


2.12.2 Channel Length modulation

Effect of change in V_{DS} on I_{DS} in saturation region



In ideal case I_D does not change with increasing V_{DS} in saturation region



In fact increasing V_{DS} does result in higher I_D
 \rightarrow channel length modulation
 \Rightarrow output resistance/ conductance

$$I_D = \frac{\mu_n C_{ox} W}{2} \frac{V_{GS} - V_t}{L} (V_{GS} - V_t)^2$$

$$I_D = \frac{\mu_n C_{ox} W}{2} \frac{V_{GS} - V_t}{L'} (V_{GS} - V_t)^2$$

where L' is reduced channel length due to pinch-off

$$L' = L - \Delta L$$

$$\frac{1}{L'} = \frac{1}{L - \Delta L} = \frac{1}{L \left(1 - \frac{\Delta L}{L}\right)} \cong \frac{1}{L} \left(1 + \frac{\Delta L}{L}\right)$$

Let $\frac{\Delta L}{L} = \lambda V_{DS}$ assuming first-order relation

$$I_D = \frac{\mu_n C_{ox} W}{2} \frac{V_{GS} - V_t}{L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$

λ = channel length coefficient - typically $\frac{0.01 \text{ to } 0.1}{L} V^{-1}$

$$\lambda \propto \frac{1}{L}$$

2.12.3 Subthreshold Conduction

Model assumes abrupt turn-off when $V_{GS}-V_t$ falls to zero

In reality when $V_{GS}-V_t$ is less than 100mV the transistor operates in 'weak inversion' and does not behave as square-law predicts.

Even for $V_{GS} < V_t$ there is a finite I_D , a diffusion current from drain to source.

This current is exponentially related to V_{GS}

For $V_{GS}-V_t < 100\text{mV}$

$$I_D = I_{D0} \frac{W}{L} \exp\left(\frac{V_{GS}}{n \frac{kT}{q}}\right)$$

$$\frac{kT}{q} = 26\text{mV} \text{ at room temperature}$$

$$n = \frac{C_{ox} + C_{depl}}{C_{ox}} \cong 1.5$$

I_{D0} in the order of tens of nA

Traditionally used in low-power applications
Sometimes poorly modelled.

2.12.4 Velocity Saturation and other short-channel effects

Various phenomena contribute to a linearisation of the current as V_{GS} increases, primarily velocity saturation.

Derivation of IV characteristic used carrier velocity $v = \mu E$

But v approaches saturation (10^7 cm/s) for fields of about $1\text{V}/\mu\text{m}$
=> velocity saturation

Reduces mobility and thereby drain current.

$$\mu_{neff} = \frac{\mu_n}{1 + \theta(V_{GS} - V_t)} \quad \theta \approx \frac{0.2}{L} \mu_m / V$$

$$I_D = \frac{\mu_n C_{ox} W}{2} \frac{1}{L} (V_{GS} - V_t)^2$$

can be re-written as

$$I_D = \frac{\mu_n C_{ox} W}{2} \frac{1}{L} \frac{(V_{GS} - V_t)^2}{[1 + \theta(V_{GS} - V_t)]}$$

For large $V_{GS} - V_t$ this tends towards

$$I_D = \frac{\mu_n C_{ox} W}{2\theta} \frac{1}{L} (V_{GS} - V_t)$$

i.e. current linearly related to $V_{GS} - V_t$ and no longer depends on L

Other effects:

hot carrier injection, impact ionization (drain-substrate current)

Dependence of threshold voltage on channel length

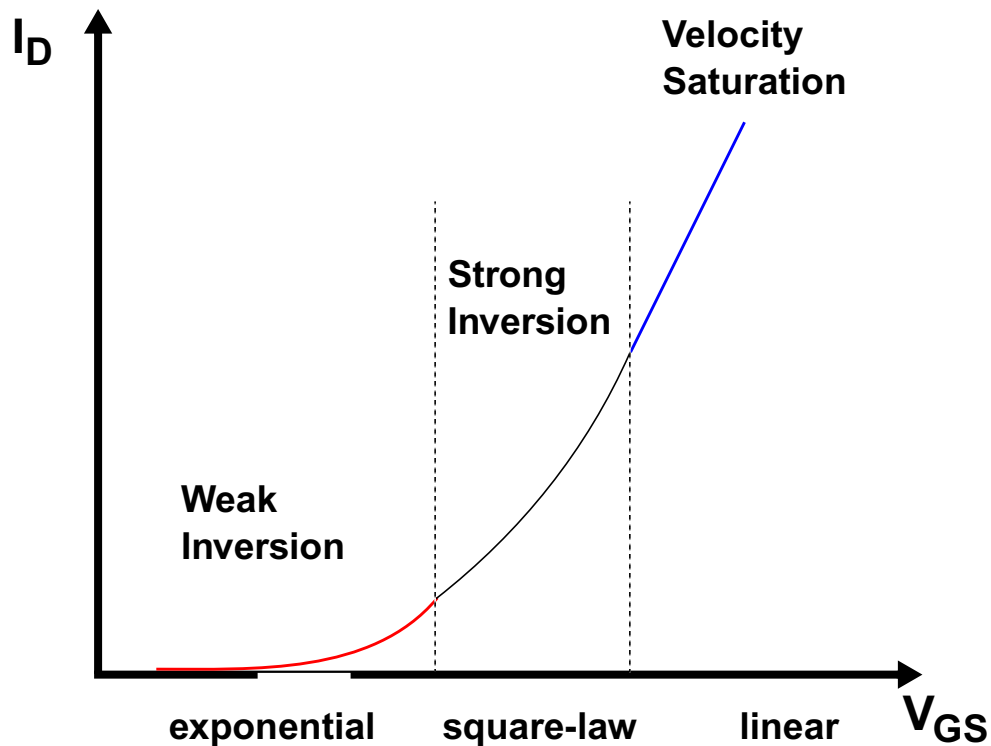
Dependence of threshold voltage on V_{DS} (drain-induced barrier lowering, DIBL).

Can partly be avoided by using transistors longer than L_{min}

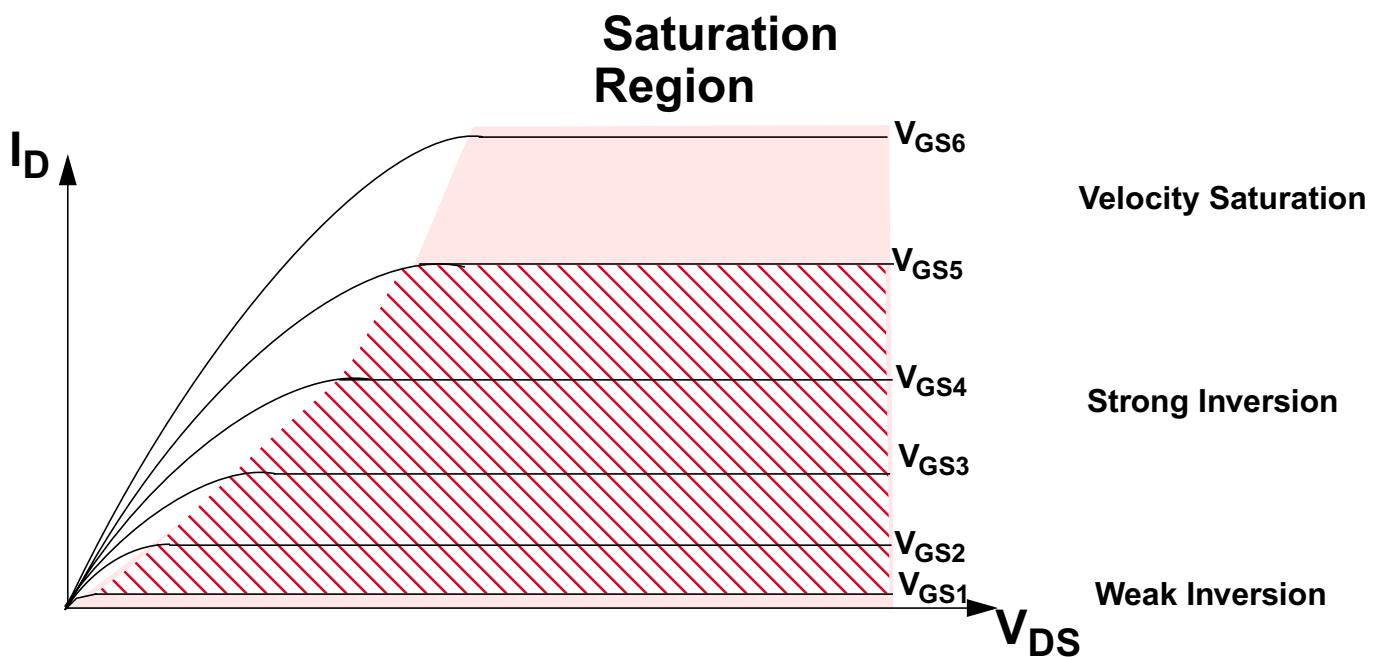
2.13 Regions of Operation

As a function of V_{GS}

N.B. $V_{DS} > V_{GS} - V_t$



As a function of V_{GS}, V_{DS}



Note: This course will use transistors biased in saturation and in the strong inversion region i.e. obeying the square-law relationship.
Note on terminology

Note

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

often written as

$$I_D = K'_n \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

and

$$I_D = \frac{\mu_n C_{ox} W}{2 L} (V_{GS} - V_t)^2$$

as

$$I_D = \frac{K'_n W}{2 L} (V_{GS} - V_t)^2$$

K'_n (and K'_p for PMOS) are measured values.

They are less than $\mu_n C_{ox}, \mu_p C_{ox}$, in the saturated region as they include corrections for velocity saturation.

2.14 Typical values (0.35um process)

NMOS

$$V_{tn} = 0.7V$$

$$K_n = \mu_n C_{ox}$$

$$\mu_n = 570 \text{cm}^2/\text{V}/\text{s}$$

$$t_{ox} = 7.5 \text{nm (75 Angstrom)}$$

$$C_{ox} = \frac{\epsilon_{ox} \epsilon_o}{t_{ox}} = \frac{3.97 \times 8.85 \times 10^{-14} \text{F/cm}}{7.5 \times 10^{-7} \text{cm}} = 47 \times 10^{-8} \text{F/cm}^2 \\ = 4.7 \text{fF}/\mu\text{m}^2$$

$$K_n = \mu_n C_{ox} = 270 \mu\text{A}/\text{V}^2$$

PMOS

$$V_{tp} = -0.7V$$

$$K_p = \mu_p C_{ox}$$

$$\mu_p = 190 \text{cm}^2/\text{V}/\text{s}$$

$$K_p = \mu_p C_{ox} = 90 \mu\text{A}/\text{V}^2$$

K_n', K_p' may be much less as they take second-order effects into account. Typical values used here:

$$K_n' = 200 \mu\text{A}/\text{V}^2$$

$$K_p' = 50 \mu\text{A}/\text{V}^2$$

Graphical Example

Drain current I_D as function of applied gate-source voltage V_{GS}

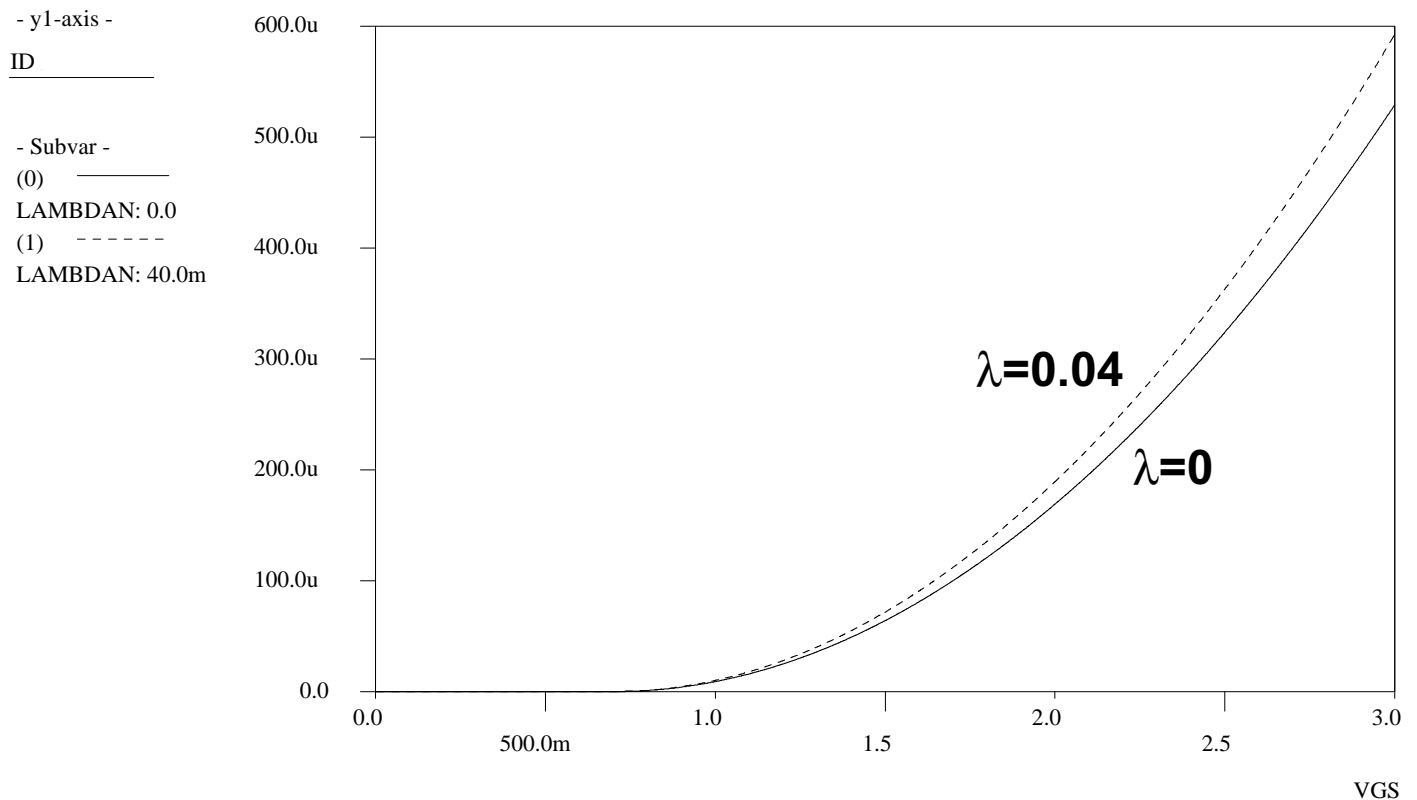
$V_{DS}=3V$

Simple square model used with

$W=1, L=1, K_n'=200\mu A/V^2, V_t=0.7V$

$\lambda=0, 0.04V^{-1}$

$$I_D = \frac{K_n'}{2} \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$



Graphical Example

Drain current I_D as function of applied drain-source voltage V_{DS}

$V_{GS}=1V, 1.25V, 1.5V$

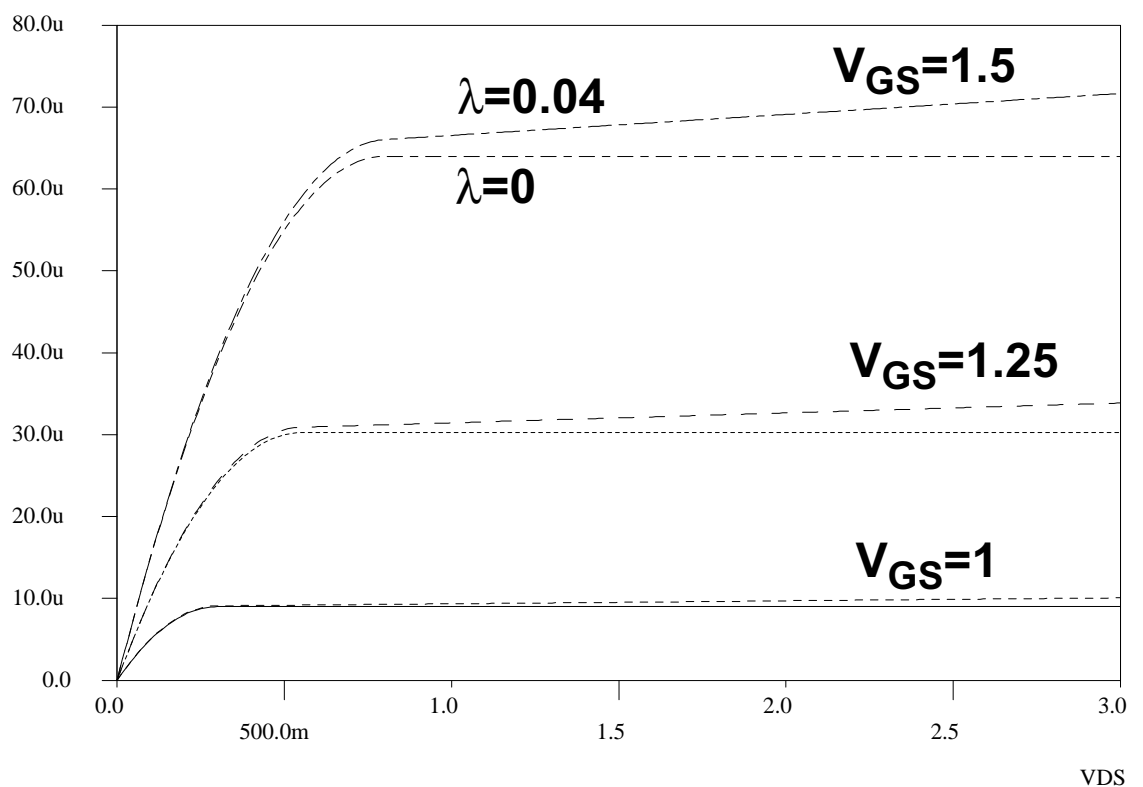
Simple square model used with

$W=1, L=1, K_n'=200\mu A/V^2, V_t=0.7V$

$\lambda=0, 0.04V^{-1}$

- y1-axis -

I_D



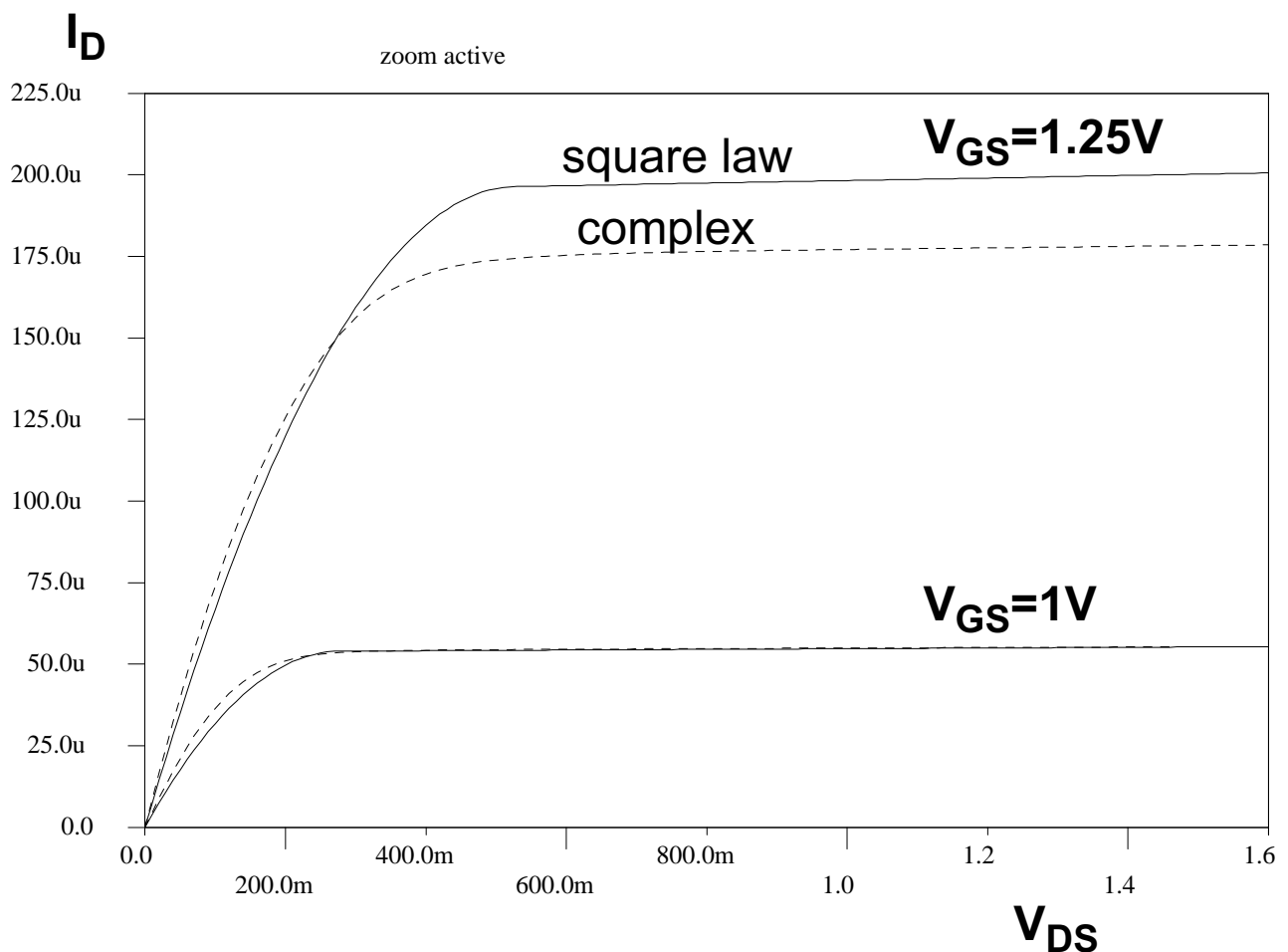
How accurate is simple square-law model in a real process?

The following graph gives I_D v V_{DS} for $V_{GS}=1V$, $1.25V$ for an NMOS in a $0.35\mu m$ process with $W/L=10/1$.

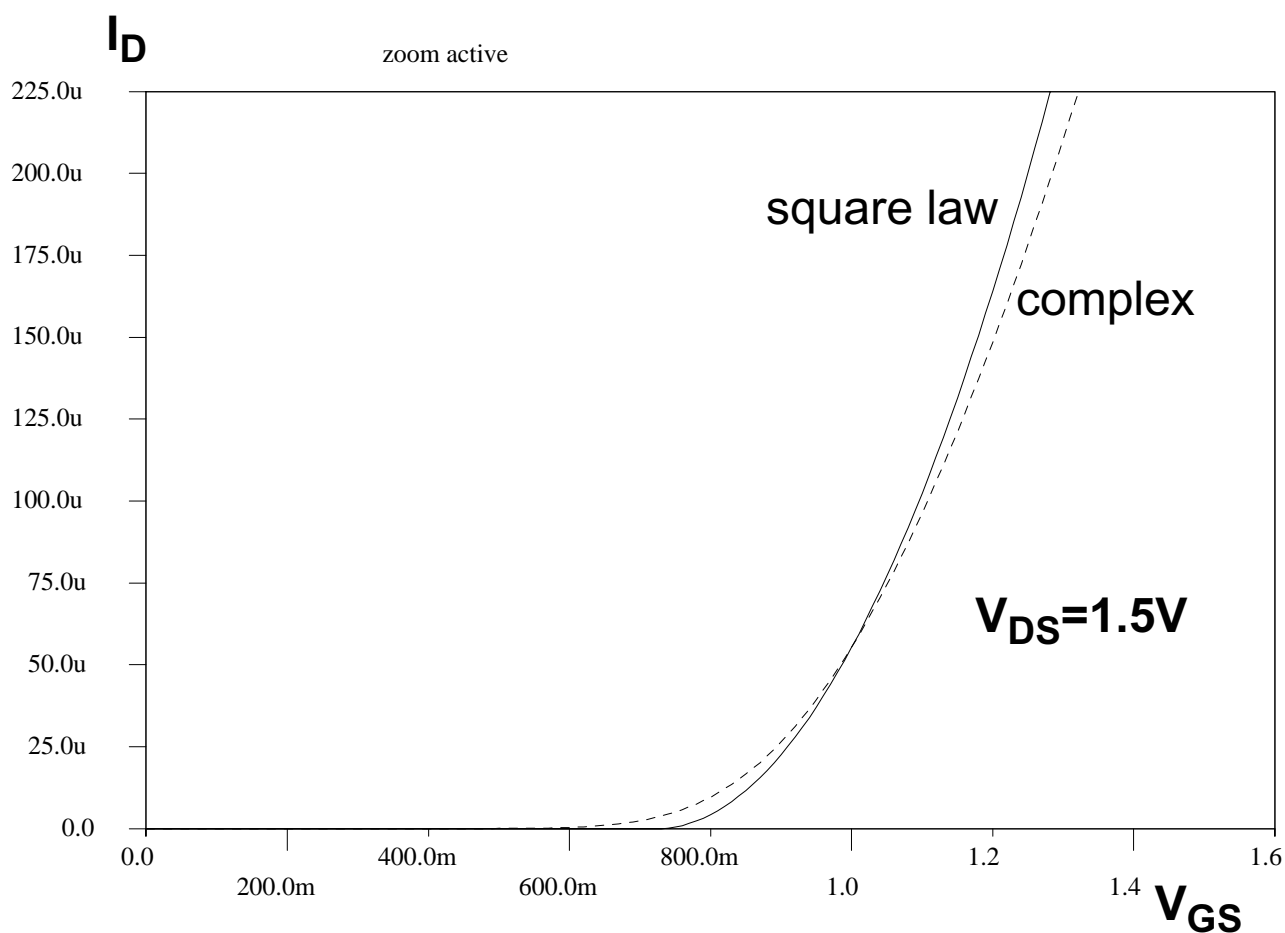
The solid line shows the current given by the simple square-law model.

The dashed line shows the current given by the complex models used in IC development. These models are an accurate reflection of the actual performance on Silicon.

For the simple model V_t has been set to $V_t=723mV$ as given by the process data, and K_n' and λ have been taken to give a good fit to the real model for the current in saturation with $V_{GS}=1.0V$. ($K_n'=140\mu A/V^2$, $\lambda = 0.02V^{-1}$).

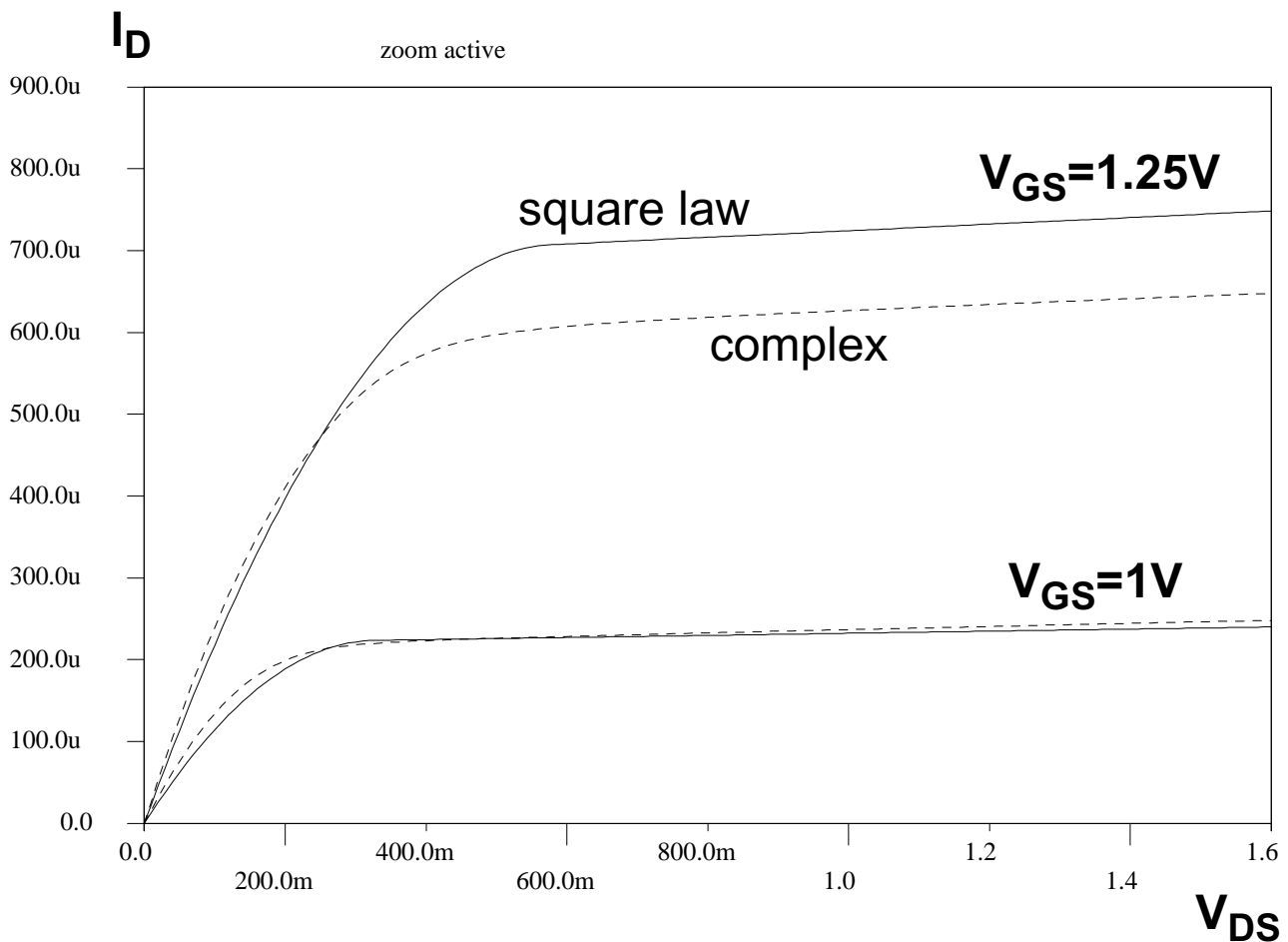


The following graph shows I_D as a function of V_{GS} , with $V_{DS}=1.5V$.

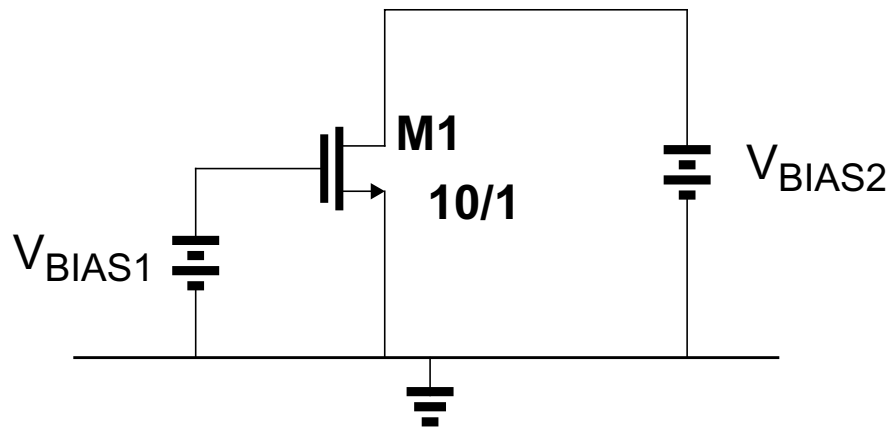


The following graph gives I_D v V_{DS} for $V_{GS}=1V, 1.25V$ for an nmos in a $0.35\mu m$ process with $W/L=10/0.35$, i.e. using minimum length. The solid line shows the current given by the simple square-law model and the dotted line the complex real model.

For the simple model V_t has been set to $V_t=673mV$ as given by the process data, K_n' had the same value as previously ($K_n'=140\mu A/V^2$) and λ has been scaled with L (i.e $0.02/0.35$).



Problem: DC Biasing (1)



Using the equations derived

(i) Calculate the drain current of M1 if

$$V_{BIAS1} = 1.25V$$

$$V_{BIAS2} = 1.0V$$

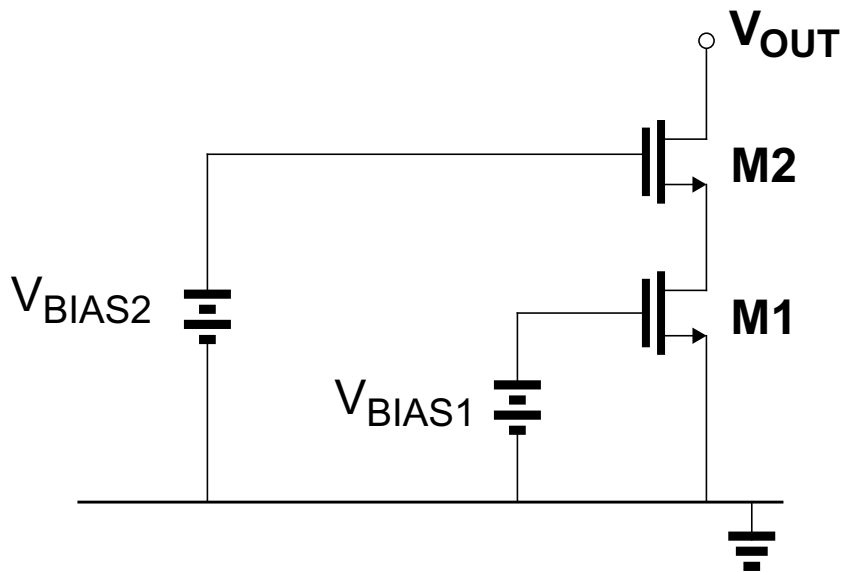
$$V_t = 0.75V$$

$$K_n = 200 \mu A/V^2$$

(ii) Calculate the drain current if V_{BIAS1} is reduced to 1V.

(iii) How could M1 be re-dimensioned to restore the original drain current.

Problem: DC Biasing (2)



The body effect may be ignored.

- (i) The circuit shown is to be biased for optimal low-voltage operation.

If

$$V_{BIAS1} = 1.2V$$

$$V_t = 0.8V$$

$$(W/L)_{M2} = (W/L)_{M1}$$

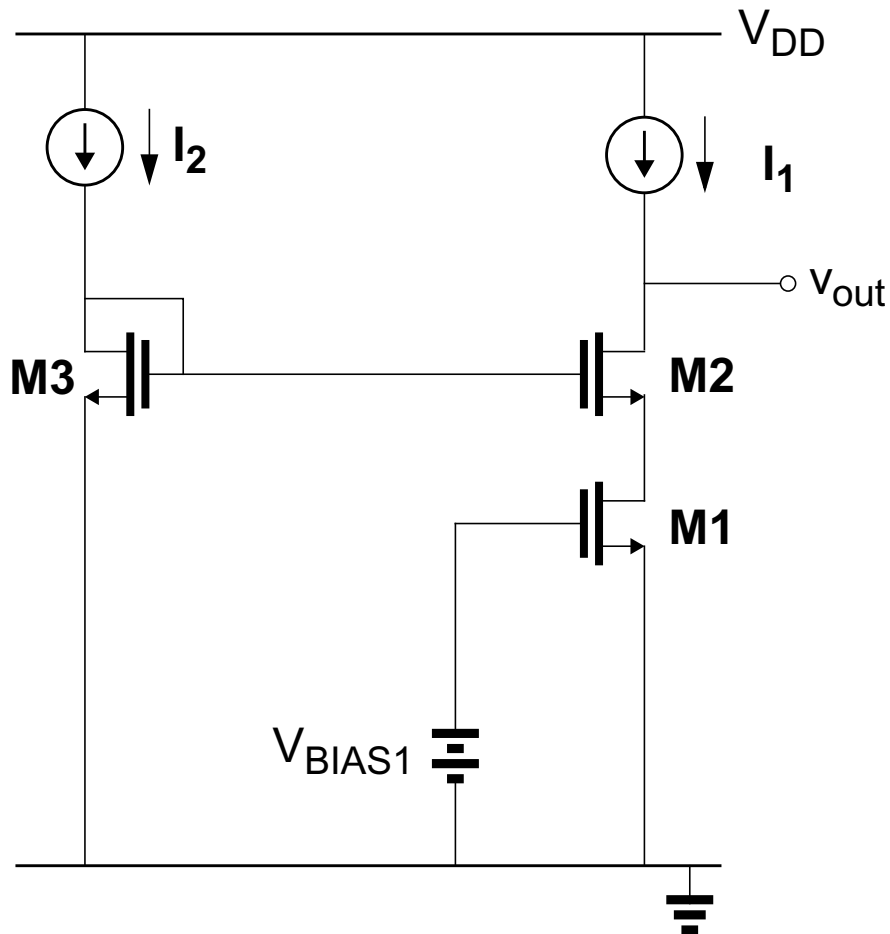
calculate the minimum value of the voltage at the output node (i.e. at the drain of M2) for both M1 and M2 to be in saturation and the value of V_{BIAS2} necessary to achieve this.

Neglect λ for this calculation.

- (ii) Repeat the calculations if the aspect ratio of M2 is four times that of M1

$$\text{i.e. } (W/L)_{M2} = 4 * (W/L)_{M1}$$

Problem: DC Biasing (3)



The body effect may be ignored.

- (i) The circuit shown is to be biased for optimal low-voltage operation.

If

$$V_{\text{BIAS1}} = 1.25\text{V}, V_t = 1\text{V}, I_1 = 100\mu\text{A}$$

$$(W/L)_{M1} = (W/L)_{M2} = (W/L)_{M3} = 16\mu\text{m}/1\mu\text{m}$$

calculate the minimum value of the voltage at the output node (i.e. at the drain of M2) for both M1 and M2 to be in saturation and the value of I_2 necessary to achieve this.

Neglect λ for this calculation.

- (ii) For low power I_2 is changed to $40\mu\text{A}$.

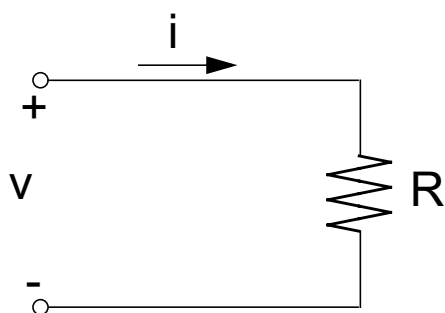
What value of $(W/L)_{M3}$ is required to preserve the bias conditions of M1 and M2.

3 Basic Circuit Techniques

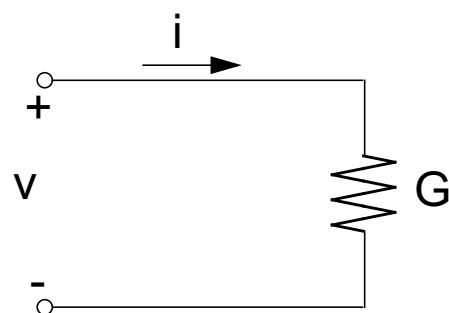
3.1 Review of network elements and concepts

3.1.1 Resistance, Conductance

Resistance

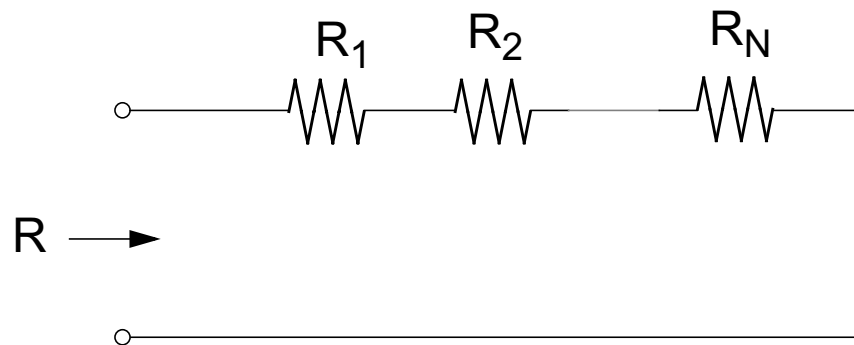


Conductance



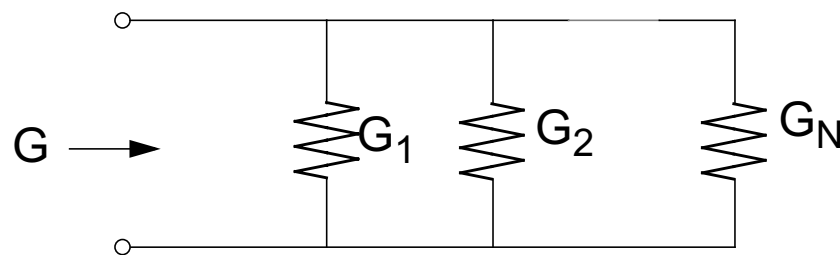
Ohm's Law $v = Ri$ $G = \frac{1}{R}$ $i = Gv$

Resistors in series



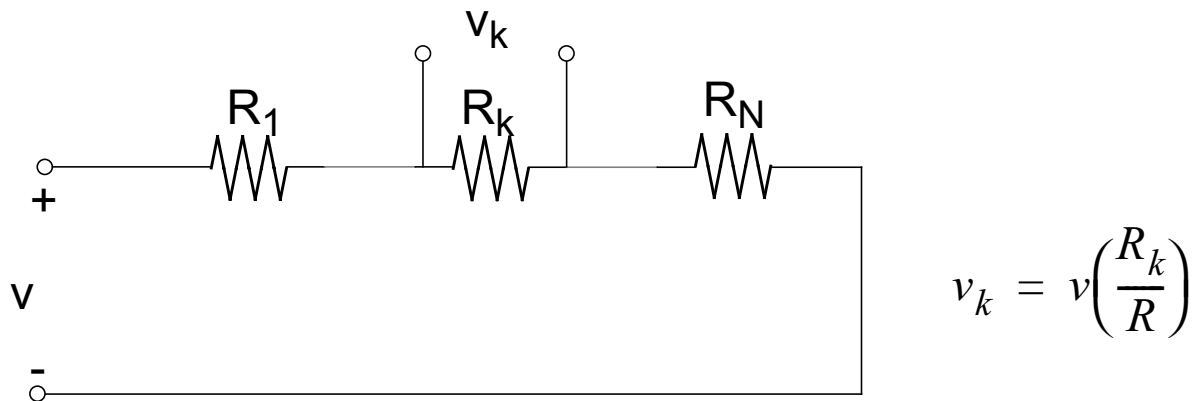
$$R = \sum_{n=1}^N R_n$$

Conductances in parallel

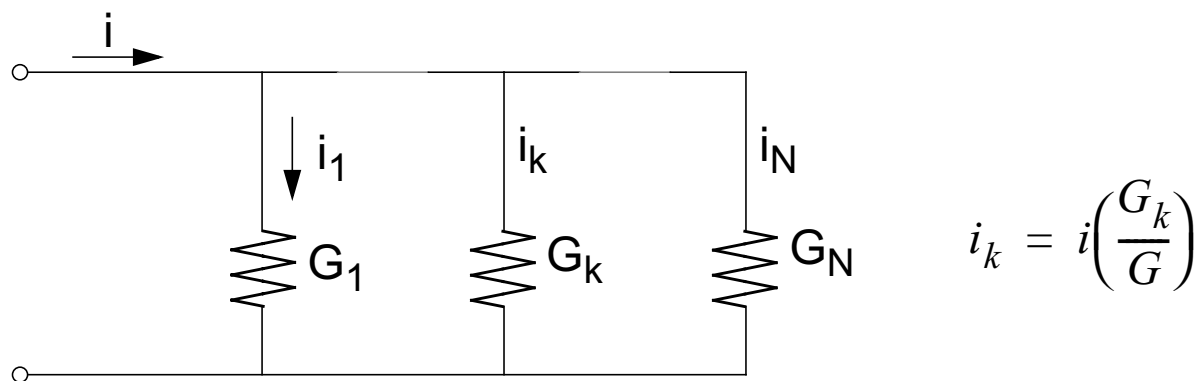


$$G = \sum_{n=1}^N G_n$$

Voltage distribution in series-connected resistances

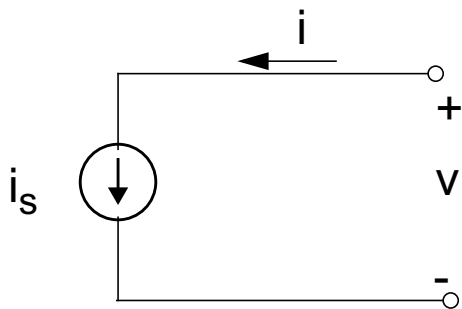


Current distribution in parallel-connected conductances



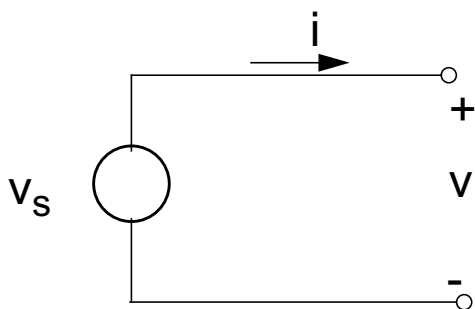
3.1.2 Ideal Independent Sources

Current source



$$i = i_s \text{ for any value of } v$$

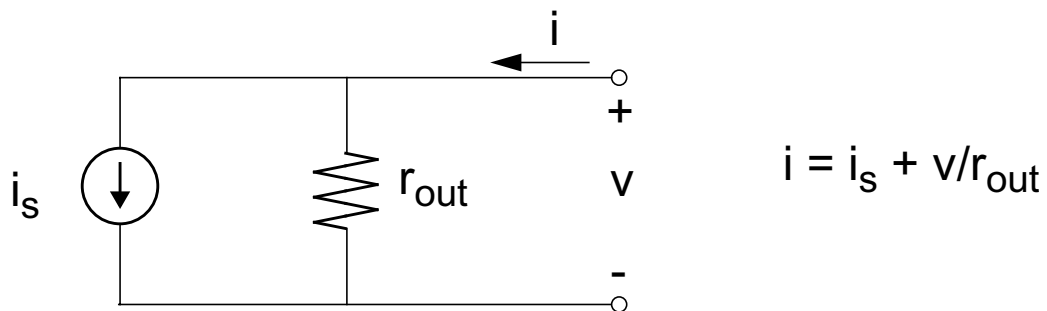
Voltage source



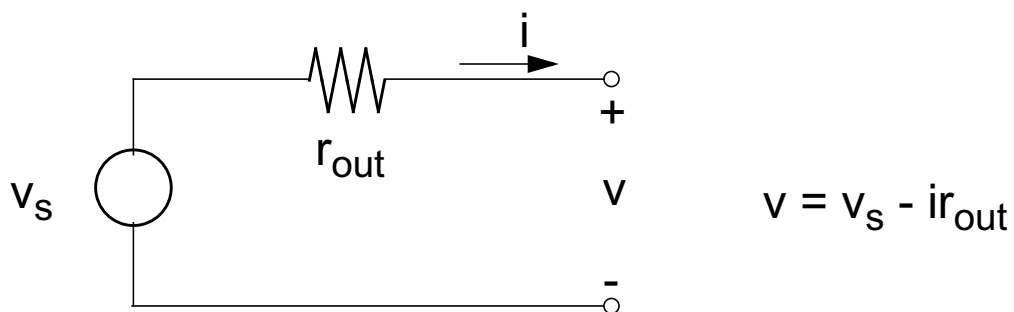
$$v = v_s \text{ for any value of } i$$

3.1.3 Real Independent Sources

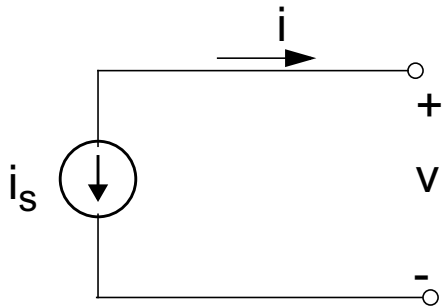
Current source with finite output resistance



Voltage source with finite output resistance



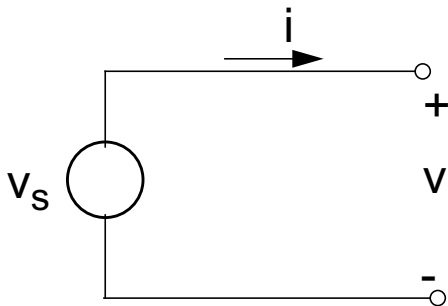
3.1.4 Dependent Sources



$i_s = g.v_k$ where v_k is v on some node k
(or between 2 nodes)

or

$i_s = \alpha.i_k$ where i_k is i through some branch k



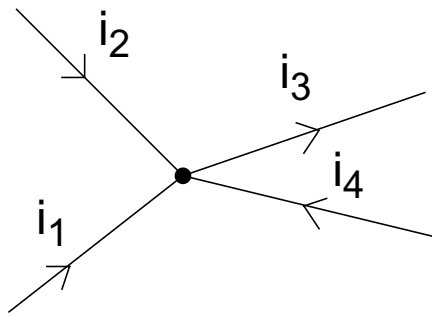
$v_s = \mu.v_k$ where v_k is v on some node k
(or between 2 nodes)

or

$v_s = r.i_k$ where i_k is i through some branch k

3.1.5 Kirchhoff's current law

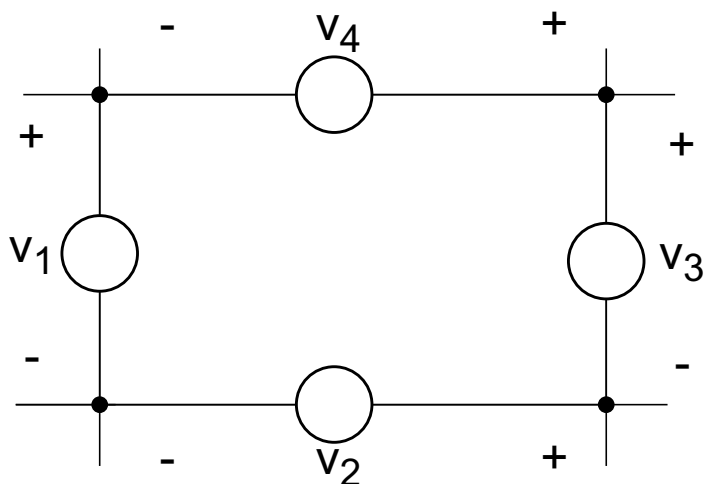
Sum of all branch currents into a node is zero



$$i_1 + i_2 - i_3 + i_4 = 0$$

3.1.6 Kirchhoff's voltage law

Sum of all branch voltages in a loop is zero



$$V_1 - V_2 - V_3 + V_4 = 0$$

3.2 Small-signal analysis in transistor circuits

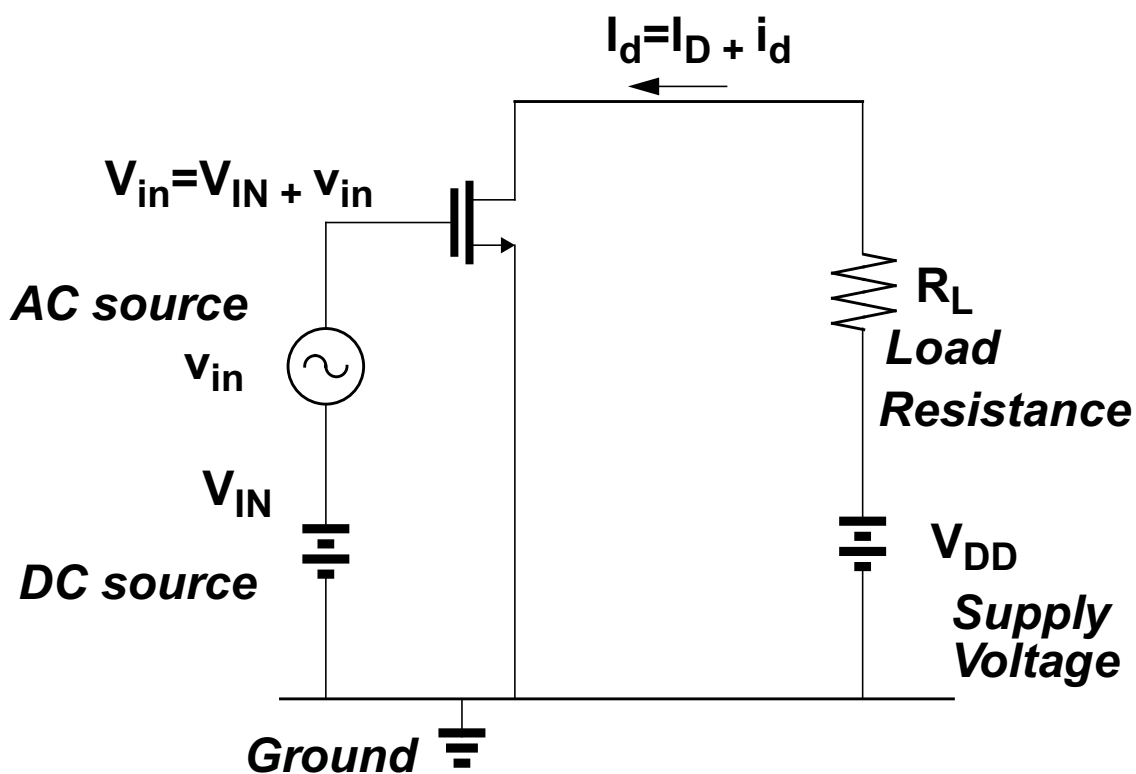
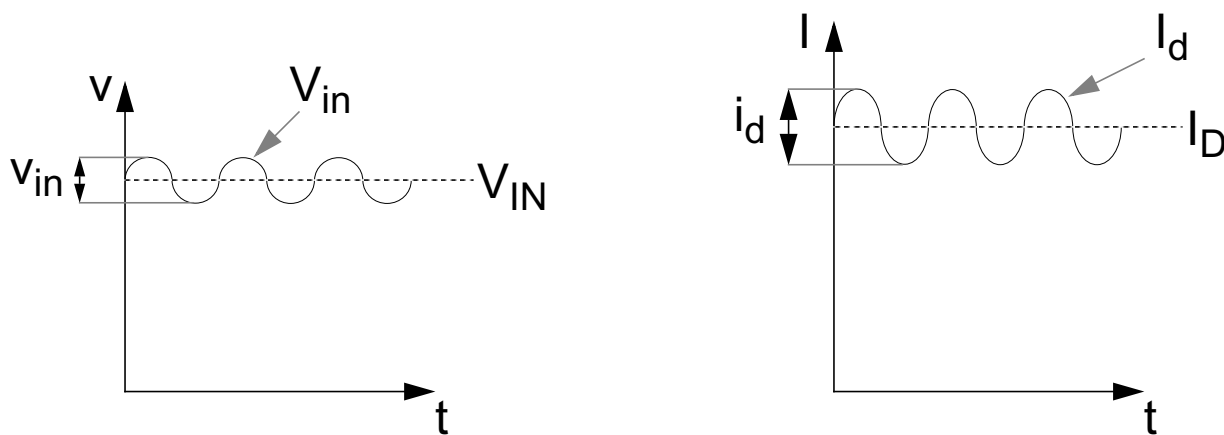
3.2.1 Notation

Upper case I , V Large signal quantities

Lower case i , v Small signal (ac) quantities

Bias the transistor with a DC voltage source V_{IN} so that a large signal current I_D is flowing

Superimpose a small-signal voltage v_{in} which causes a small-signal current i_d



3.2.2 Linearisation

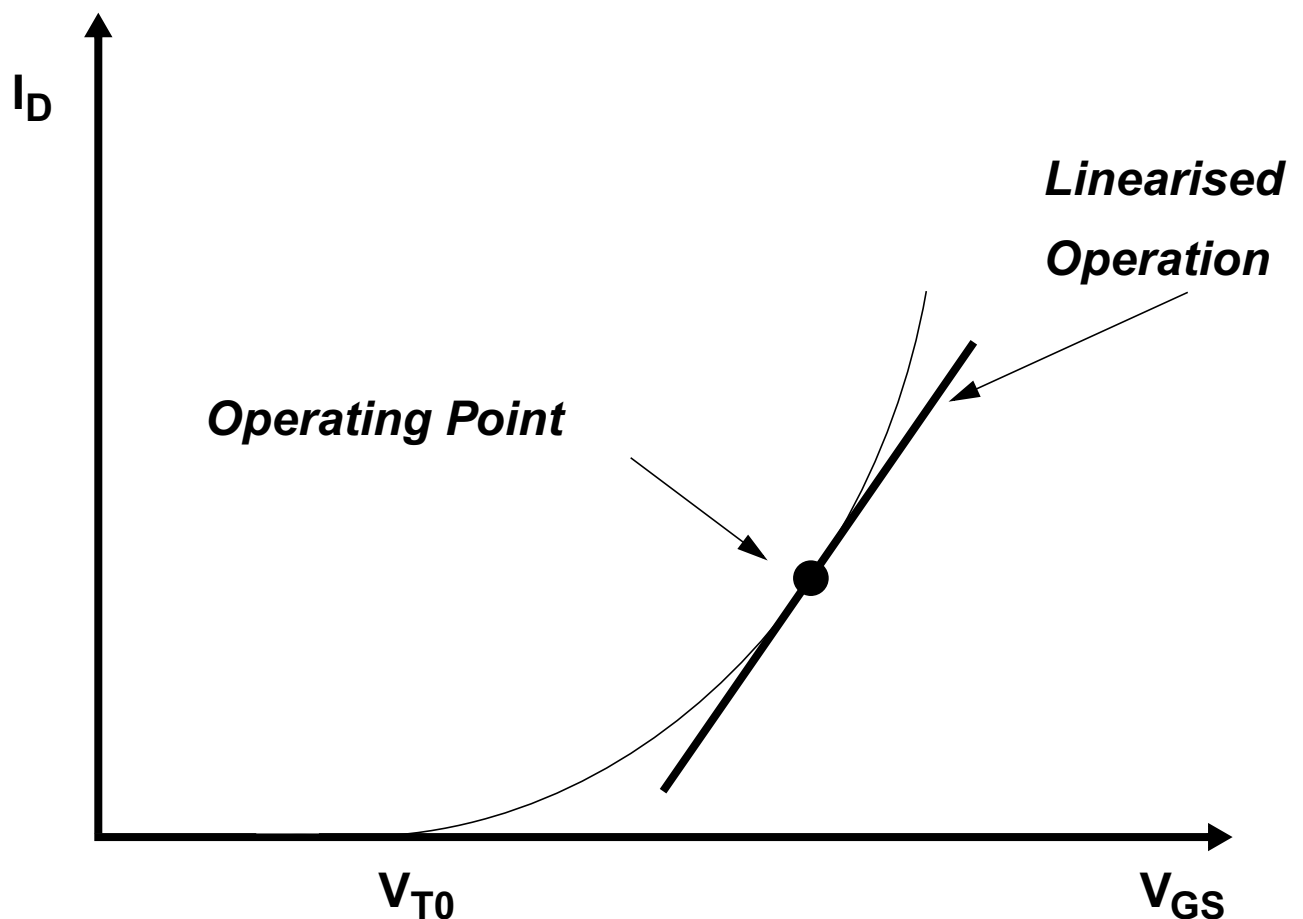
Large signal behaviour of MOS devices is non-linear.

Analysis is difficult.

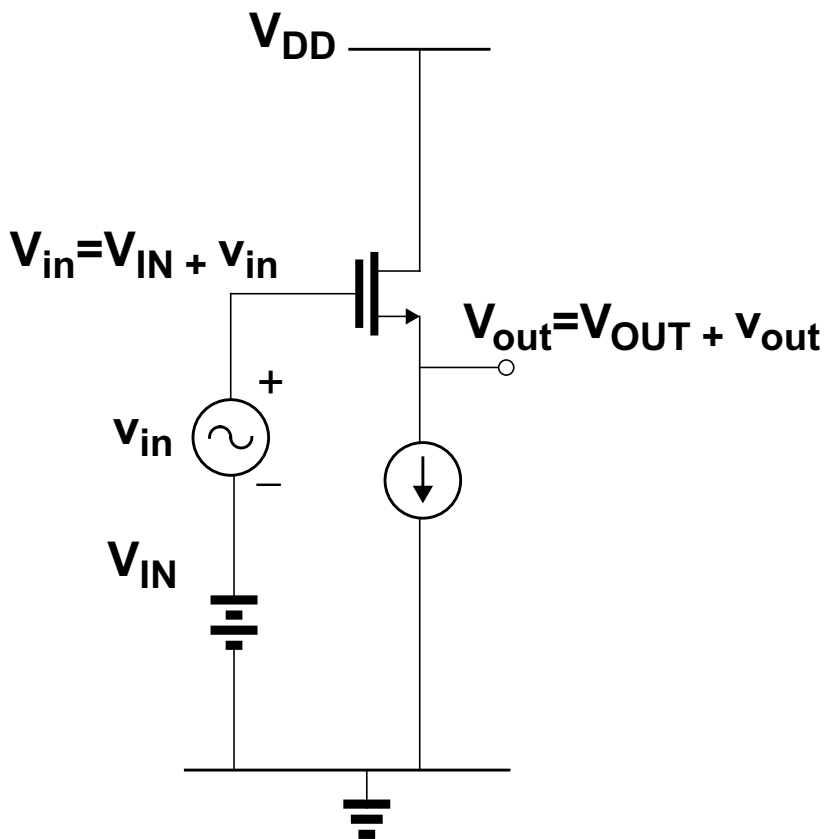
If signals are small then transistor behaviour can be analysed as linear.

DC Operating point determined by large signal I, V.

Transistor behaviour linearised at the DC Operating point i.e. small signal parameters are derivatives of the large signal characteristic at the operating point



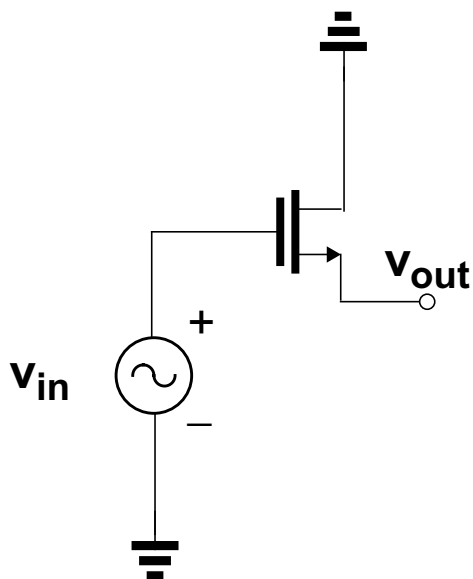
3.2.3 Small-signal equivalent circuits



Small-signal equivalence:

All DC voltage sources \rightarrow short circuits

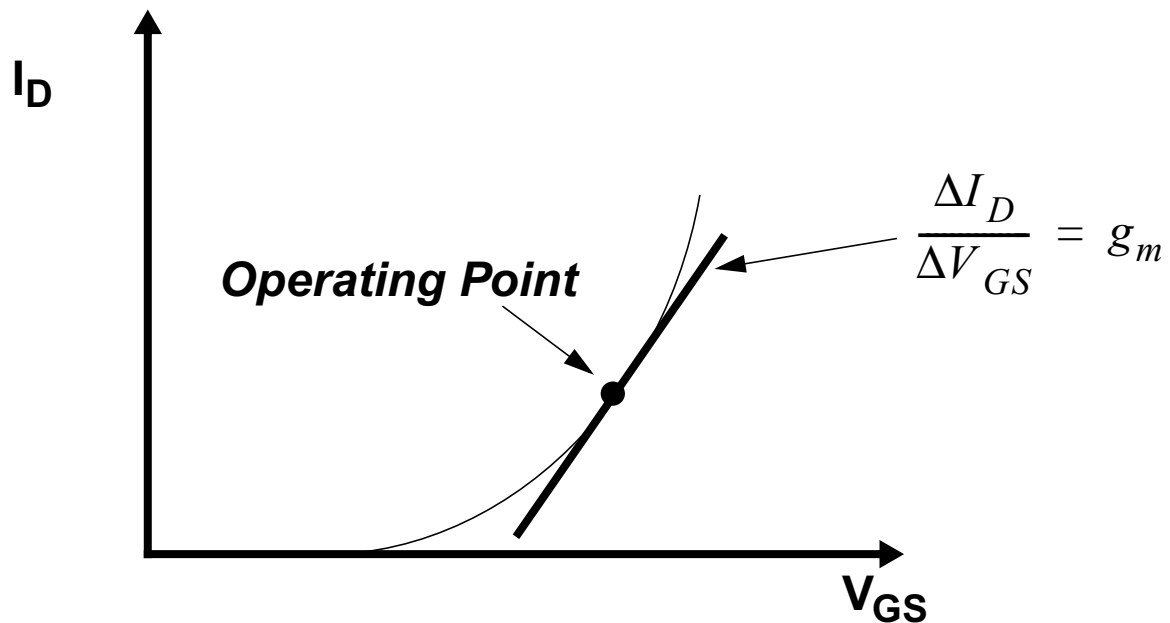
All DC current sources \rightarrow open circuits



3.3 MOS Small-signal parameters (NMOS)

3.3.1 Transconductance g_m

Change in drain current when gate-source voltage is changed



(i) Cutoff: $g_m=0$

(ii) Linear/triode region

$$I_D = K'_n \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$g_m = \left. \frac{\delta I_d}{\delta V_{GS}} \right|_{V_{DS} \text{ constant}} = K'_n \frac{W}{L} V_{DS}$$

(iii) Saturation region

$$I_D = \frac{K'_n W}{2L} (V_{GS} - V_t)^2$$

Three useful equations can be derived for the saturation region.

$$g_m = \left. \frac{\delta I_d}{\delta V_{GS}} \right|_{V_{DS} \text{ constant}} = \underline{K'_n \frac{W}{L} (V_{GS} - V_t)} \quad (\text{i})$$

From (i)

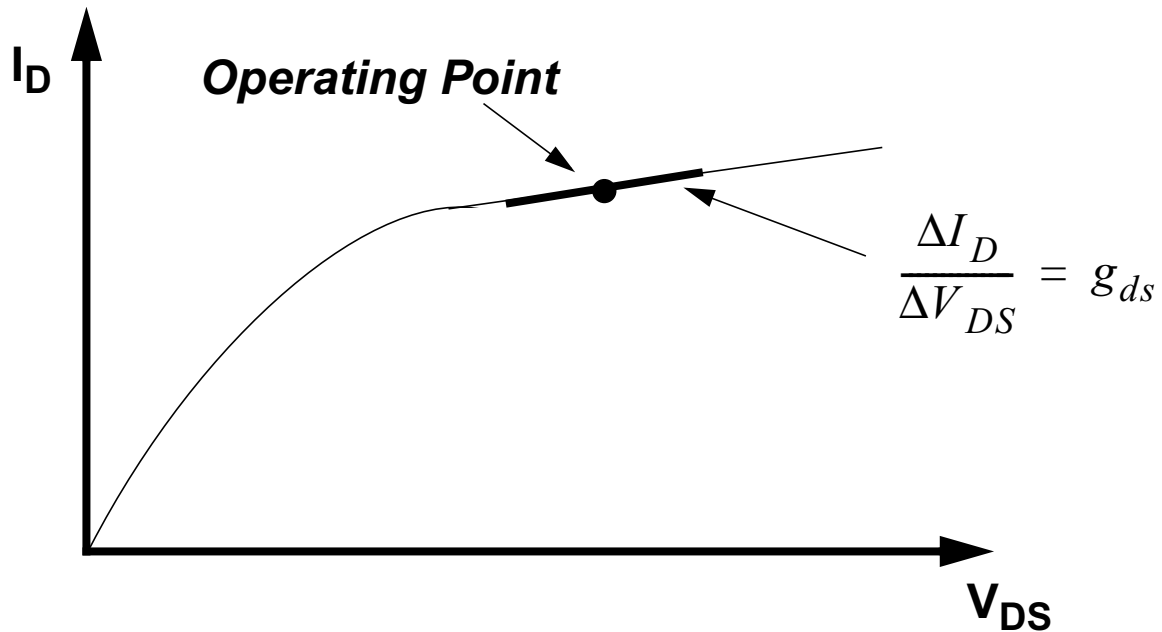
$$g_m = K'_n \frac{W}{L} \sqrt{\frac{I_D}{\frac{K'_n W}{2L}}}$$
$$\underline{g_m = \sqrt{2K'_n \frac{W}{L} I_D}} \quad (\text{ii})$$

Also from (i)

$$\underline{g_m = \frac{2I_D}{(V_{GS} - V_t)}} \quad (\text{iii})$$

3.3.2 Output conductance g_{ds}

Change in drain current when drain-source voltage is changed



1. Cutoff: $g_{ds}=0$

2. Linear/triode region

$$I_D = K'_n \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$g_{ds} = \left. \frac{\delta I_d}{\delta V_{dS}} \right|_{V_{GS} \text{ constant}} = K'_n \frac{W}{L} [V_{GS} - V_t - V_{DS}]$$

3. Saturation

$$I_D = \frac{K'_n W}{2 L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$

$$g_{ds} = \frac{\delta I_d}{\delta V_{dS}} = \lambda \left[\frac{K'_n W}{2 L} (V_{GS} - V_t)^2 \right] \underline{\cong \lambda I_D}$$

3.3.3 Back-gate (bulk) transconductance g_{mb}

Change in drain current when source-bulk voltage is changed

$$g_{mb} = \frac{\delta I_D}{\delta V_{BS}}$$

This change is caused by the body (back-gate) effect

To derive use

$$\frac{\delta I_D}{\delta V_{SB}} = \frac{\delta I_D}{\delta V_t} \cdot \frac{\delta V_t}{\delta V_{SB}}$$

$$\frac{\delta I_D}{\delta V_t} = -\frac{\delta I_D}{\delta V_{GS}} = -g_m$$

$$V_t = V_{to} + \gamma(\sqrt{2|\Phi_F| + V_{SB}} - \sqrt{2|\Phi_F|})$$

$$\frac{\delta V_t}{\delta V_{SB}} = \frac{\gamma}{2\sqrt{2|\Phi_F| + V_{SB}}}$$

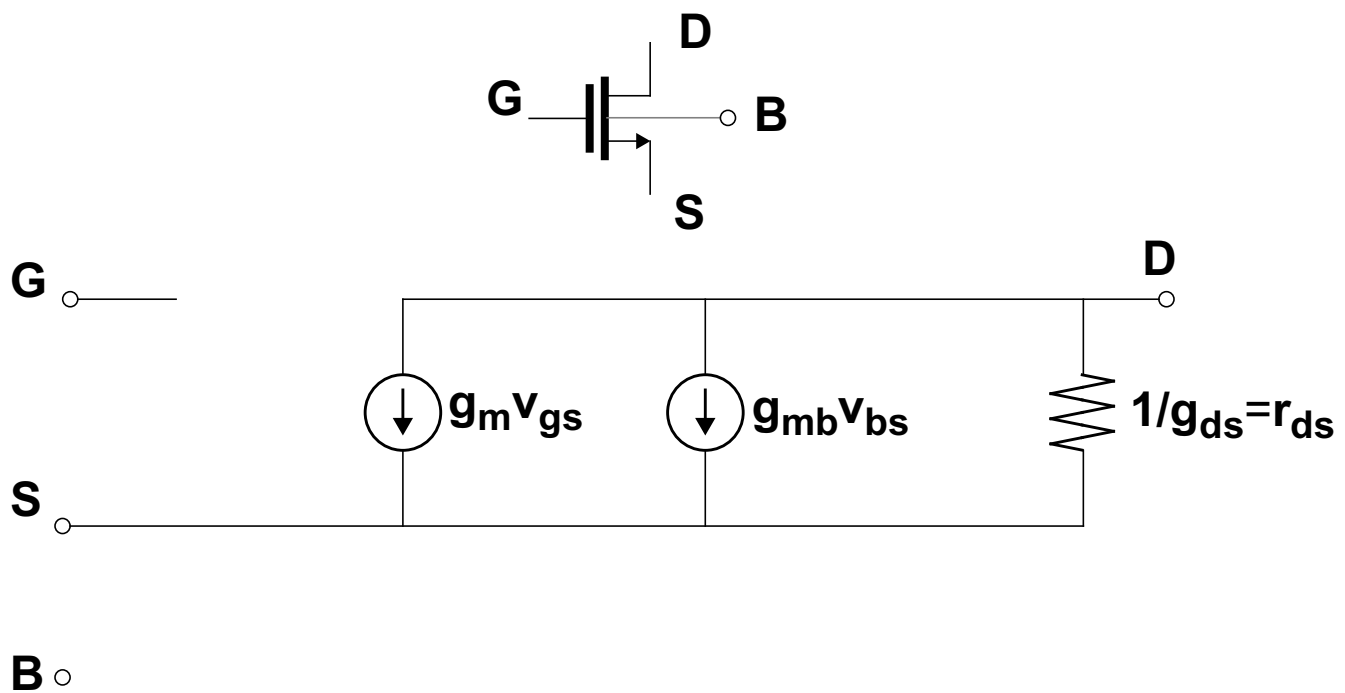
$$\Rightarrow \frac{\delta I_D}{\delta V_{SB}} = \frac{\delta I_D}{\delta V_t} \cdot \frac{\delta V_t}{\delta V_{SB}} = -g_m \frac{\gamma}{2\sqrt{2|\Phi_F| + V_{SB}}}$$

$$g_{mb} = \frac{\delta I_D}{\delta V_{BS}} = \underline{g_m \eta}$$

Note that η varies from approx 0.1 to 0.3

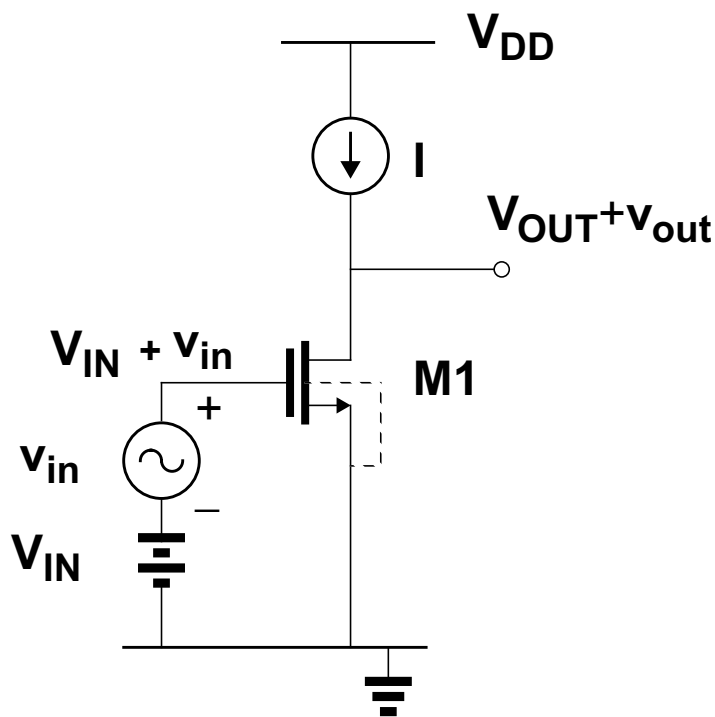
If the source is connected to the bulk then ΔV_{SB} is zero and we do not need to take g_{mb} into account.

3.4 Small Signal Model (Low-Frequency)



Low frequency model - no capacitors

Problem: Small-signal model

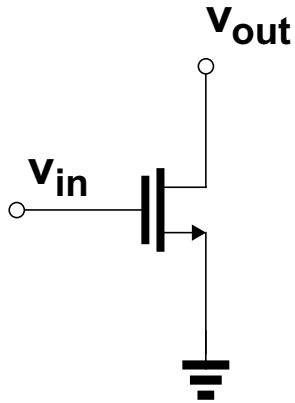


- (i) Draw the small-signal equivalent circuit
- (ii) What is the small-signal voltage gain in terms of the small-signal parameters of M1
- (iii) Explain the result in terms of the large-signal behaviour assuming M1 is in saturation
- (iv) What is the small signal gain if $I=100\mu\text{A}$, $\lambda=0.1\text{V}^{-1}$, $V_{GS}-V_t=200\text{mV}$

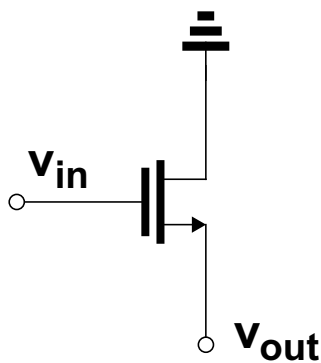
4 Single-stage amplifiers

For a single transistor: basically 3 possibilities

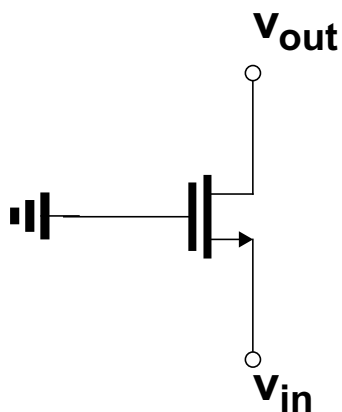
Common Source



Source Follower (Common Drain)

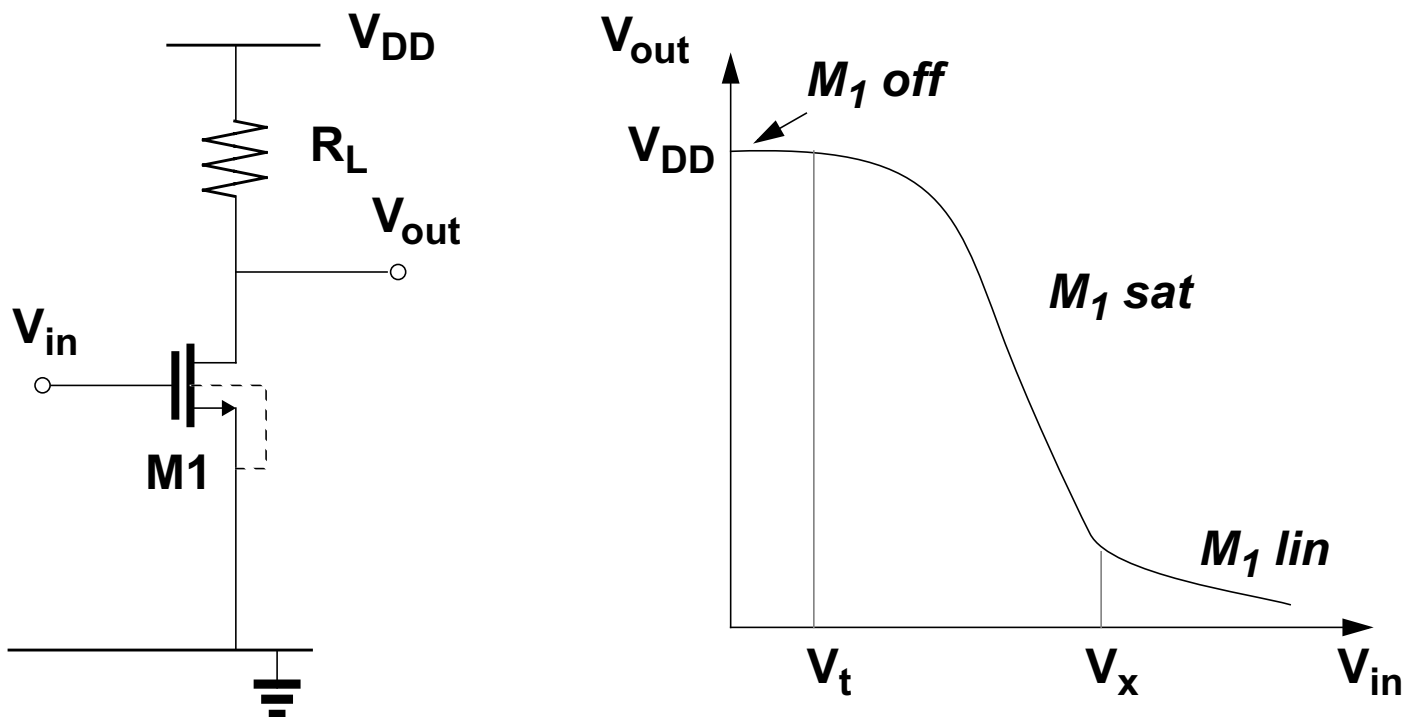


Common Gate



4.1 Common source stage with Resistive Load

4.1.1 CS stage with resistor load - Large-signal behaviour



1. $V_{in}=0 \Rightarrow M1$ off $\Rightarrow V_{out}=V_{DD}$

2. V_{in} increases.

When $V_{in} > V_t$ M1 turns on in saturation and current flows

$$V_{out} = V_{DD} - I_D R_L$$

$$V_{out} = V_{DD} - \frac{K'_n W}{2L} (V_{in} - V_t)^2 R_L$$

3. M1 remains in saturation until $V_{in}-V_t > V_{out}$. This occurs when $V_{in}=V_x$

$$V_x - V_t = V_{DD} - \frac{K'_n W}{2L} (V_x - V_t)^2 R_L$$

For $V_{in} > V_x$ M1 is in triode region

$$V_{out} = V_{DD} - K'_n \frac{W}{L} \left((V_{in} - V_t) V_{out} - \frac{V_{out}^2}{2} \right) R_L$$

4. Increasing V_{in} still further:

M1 will go into deep triode if $V_{out} \ll 2(V_{in} - V_t)$

In this case V_{out} is determined by the resistive divider R_{DS} and R_L

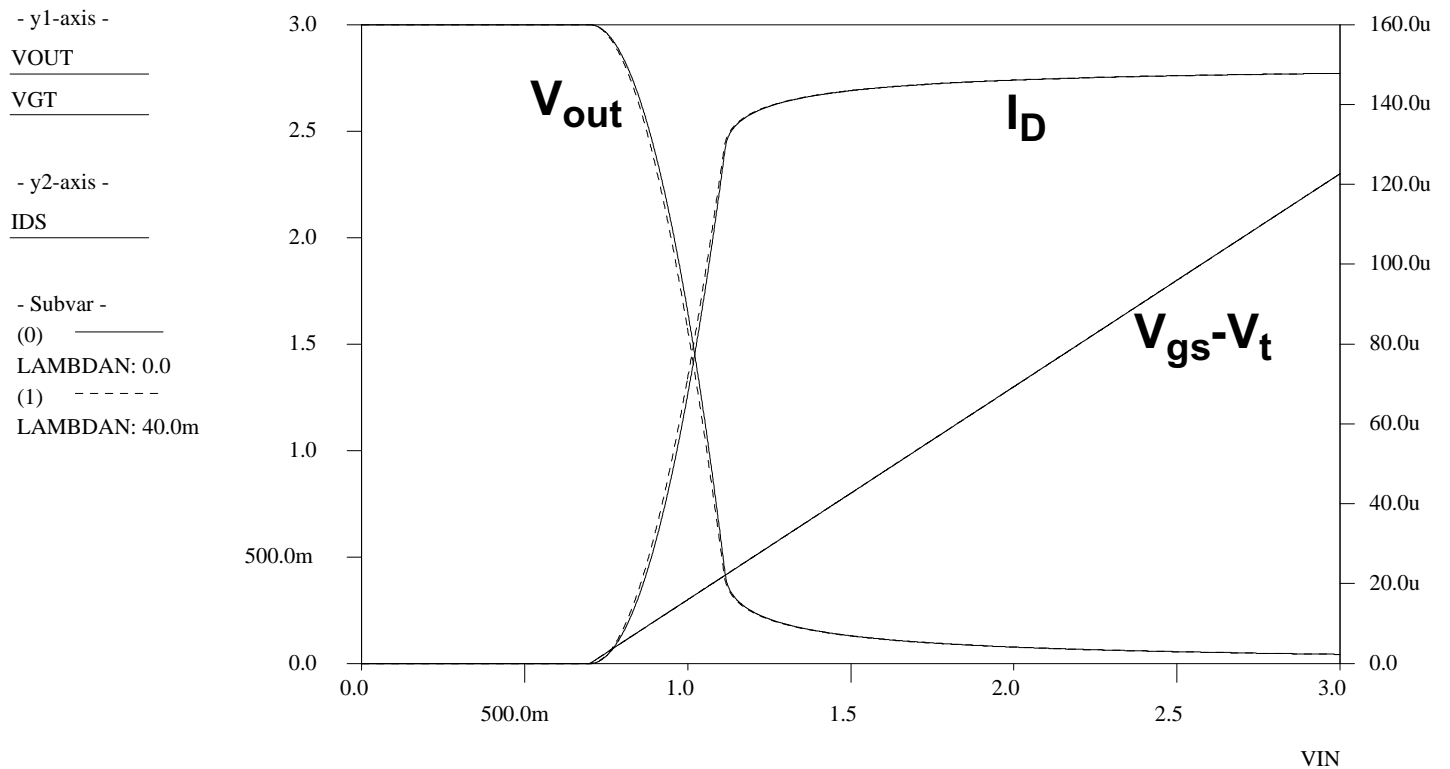
$$V_{out} = V_{DD} \left(\frac{R_{DS}}{R_{DS} + R_L} \right) = \left(\frac{V_{DD}}{1 + \frac{R_L}{R_{DS}}} \right)$$

$$V_{out} = \left(\frac{V_{DD}}{1 + R_L \left(\mu_n C_{ox} \frac{W}{L} (V_{in} - V_t) \right)} \right)$$

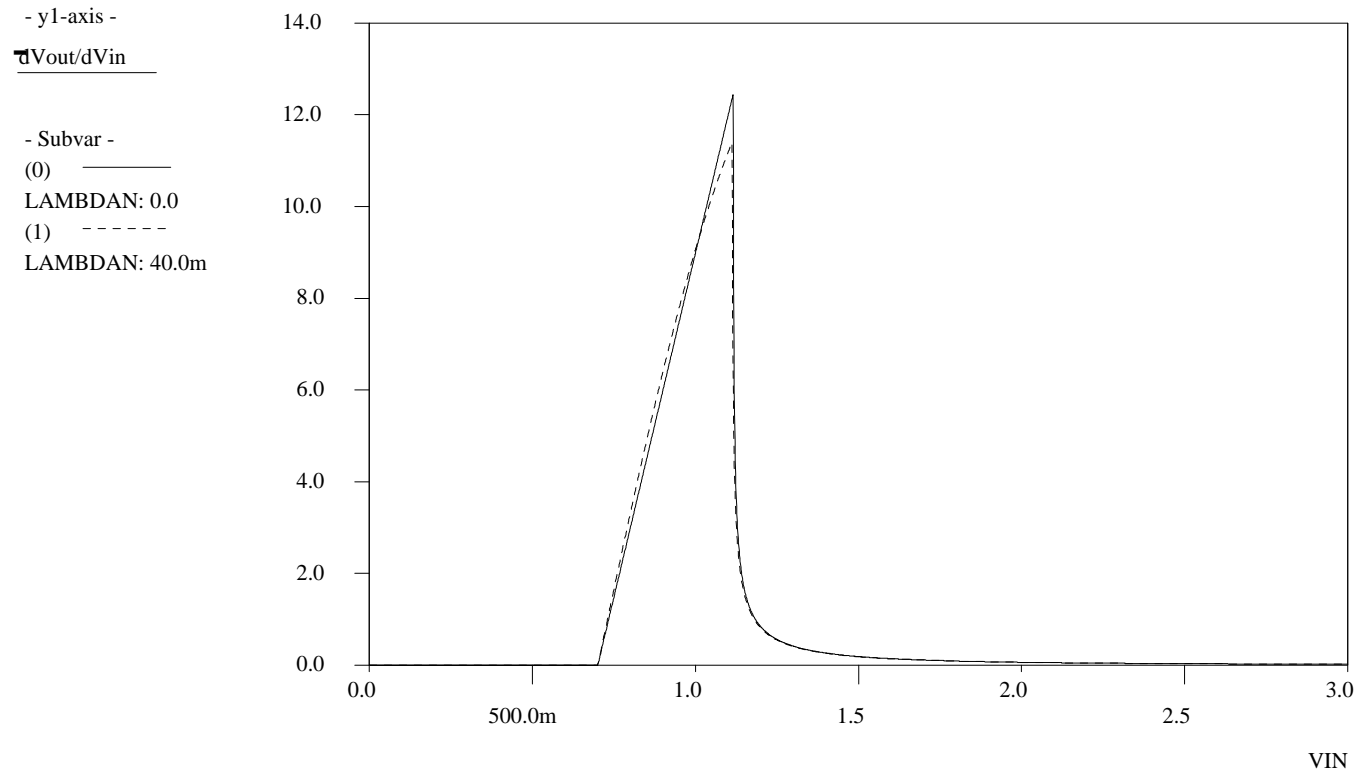
Graphical Example

Simulated: $V_{DD}=3V$, $W/L = 10/1$, $V_{tn}=0.7V$, $K_n'=160\mu A/V$, $R_L=20k\Omega$.
 $\lambda=0$, $0.04V^{-1}$

Output voltage, current



Derivative of output voltage w.r.t. input voltage (gain)



Note: non-linearity in output signal due to changing gain.

4.1.2 Gain of CS stage with resistive load

In active/saturation region

$$V_{out} = V_{DD} - \frac{K'_n W}{2L} (V_{in} - V_t)^2 R_L$$

Gain given by

$$\frac{\delta V_{out}}{\delta V_{in}} = -K'_n \frac{W}{L} (V_{in} - V_t) R_L$$

$$\frac{\delta V_{out}}{\delta V_{in}} = -g_m R_L$$

4.1.3 Gain of CS stage, R load, with output conductance

$$V_{out} = V_{DD} - \frac{K'_n W}{2L} (V_{in} - V_t)^2 (1 + \lambda V_{out}) R_L$$

$$\begin{aligned} \frac{\delta V_{out}}{\delta V_{in}} &= -K'_n \frac{W}{L} (V_{in} - V_t) (1 + \lambda V_{out}) R_L \\ &\quad - \frac{K'_n W}{2L} (V_{in} - V_t)^2 R_L \lambda \frac{\delta V_{out}}{\delta V_{in}} \end{aligned}$$

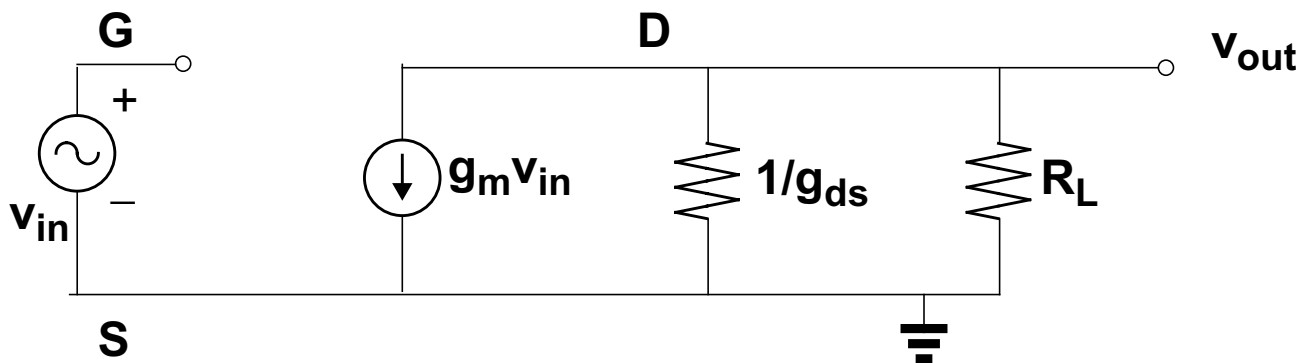
$$\frac{\delta V_{out}}{\delta V_{in}} \approx -g_m R_L - I_D R_L \lambda \frac{\delta V_{out}}{\delta V_{in}}$$

$$\frac{\delta V_{out}}{\delta V_{in}} = \frac{-g_m R_L}{1 + \lambda I_D R_L} = \frac{-g_m R_L}{1 + g_{ds} R_L}$$

$$\frac{\delta V_{out}}{\delta V_{in}} = \frac{-g_m}{g_{ds} + \frac{1}{R_L}}$$

4.1.4 CS stage with Resistive Load: Small-signal analysis

Equivalent small-signal circuit



Various calculation methods:

Using KCL at output

$$g_m v_{in} + v_{out} g_{ds} + \frac{v_{out}}{R_L} = 0$$

$$v_{out} \left(g_{ds} + \frac{1}{R_L} \right) = -g_m v_{in}$$

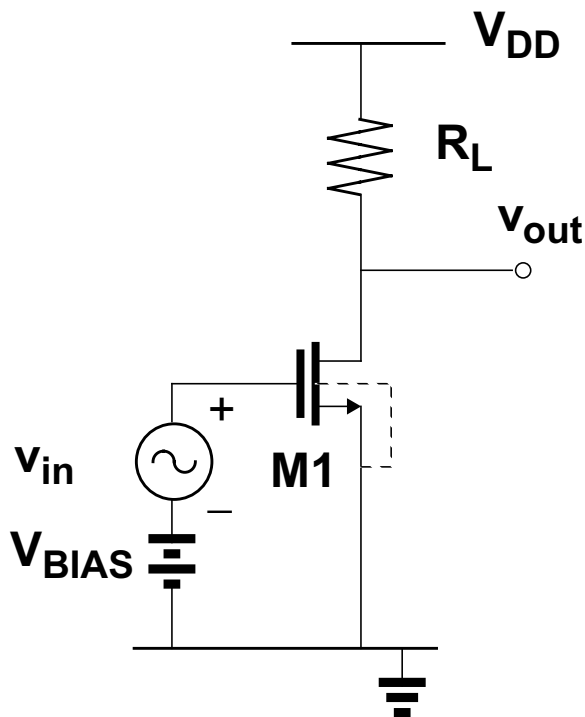
$$\frac{v_{out}}{v_{in}} = \frac{-g_m}{g_{ds} + \frac{1}{R_L}}$$

Voltage at output:

$$v_{out} = \frac{-g_m v_{in}}{g_{ds} + \frac{1}{R_L}}$$

$$\frac{v_{out}}{v_{in}} = \frac{-g_m}{g_{ds} + \frac{1}{R_L}}$$

Example - Common source stage with Resistive load



Draw the small signal model.

What is small signal voltage gain if

$$V_{\text{BIAS}} = 1.25$$

$$V_{\text{DD}} = 5\text{V}$$

$$K_n' = 100\mu\text{A}/\text{V}^2$$

$$\lambda = 0.04/\text{L} [\text{V}^{-1}] \text{ (L in } \mu\text{m)}$$

$$V_t = 0.75\text{V}$$

$$W/L \text{ M1} = 16/2$$

$$R_L = 20\text{k}\Omega$$

Check if M1 is in saturation

$$I_D = \frac{K_n' W}{2 L} (V_{\text{GS}} - V_t)^2 = 50 \times 8 \times 0.25 = 100\mu\text{A}$$

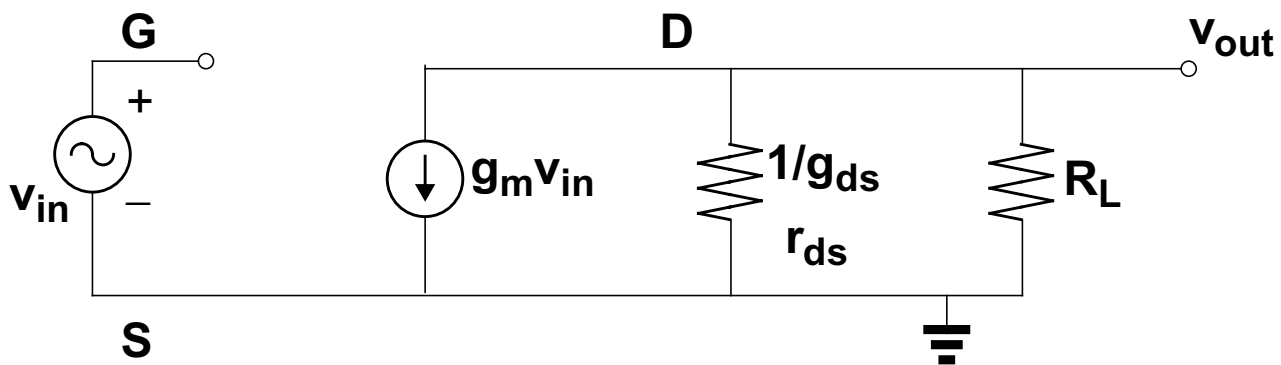
$\uparrow \qquad \qquad \uparrow$
 $\frac{\mu\text{A}}{\text{V}^2} \qquad \text{V}^2$

$$V_D = V_{\text{DD}} - (I_D \times R_L) = 5\text{V} - (100\mu\text{A} \times 20\text{k}) = 3\text{V}$$

$$V_{\text{GS}} - V_t = 1.25\text{V} - 0.75\text{V} = 0.5\text{V}$$

$$V_D > V_{\text{GS}} - V_t \Rightarrow \text{M1 is saturated}$$

Equivalent small-signal circuit



Using KCL at output

$$g_m v_{in} + v_{out} g_{ds} + v_{out} R_L = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_m}{g_{ds} + \frac{1}{R_L}}$$

Using Ohm's Law at output

$$v_{out} = -g_m v_{in} (r_{ds} \parallel R_L)$$

$$\frac{v_{out}}{v_{in}} = -g_m (r_{ds} \parallel R_L)$$

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2 \times 100\mu A}{1.25V - 0.75V} = 400\mu A/V$$

$$g_{ds} = \lambda I_D = \frac{0.04}{2} \cdot 100\mu A = 2\mu A/V \Rightarrow r_{ds} = 500k$$

$$\left| \frac{v_{out}}{v_{in}} \right| = \frac{400\mu A/V}{2\mu A/V + \frac{1}{20k}} \cong 8$$

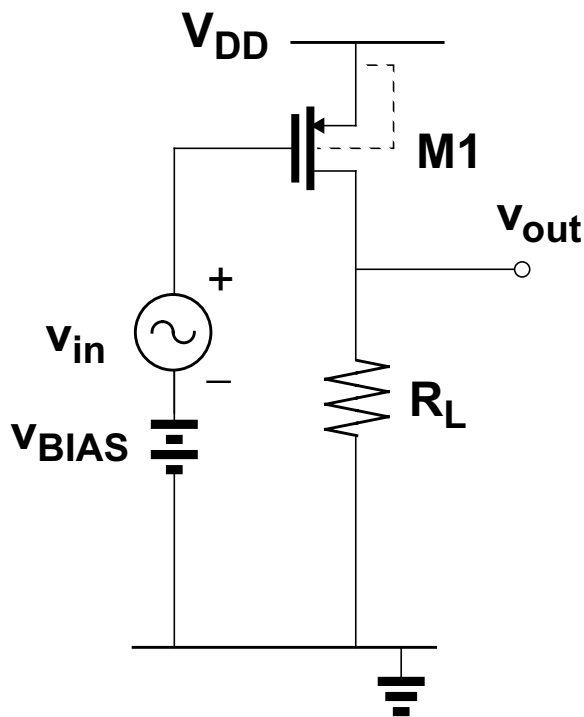
$$\left| \frac{v_{out}}{v_{in}} \right| = 400\mu A/V (20k \parallel 500k) \cong 8 \quad (R_L \text{ dominates})$$

Note: gain usually expressed in dB

$$A = 20 \log \left| \frac{v_{out}}{v_{in}} \right| = 18dB$$

Resistive loads give (relatively) low gain.

Problem: PMOS common-source stage with resistive load

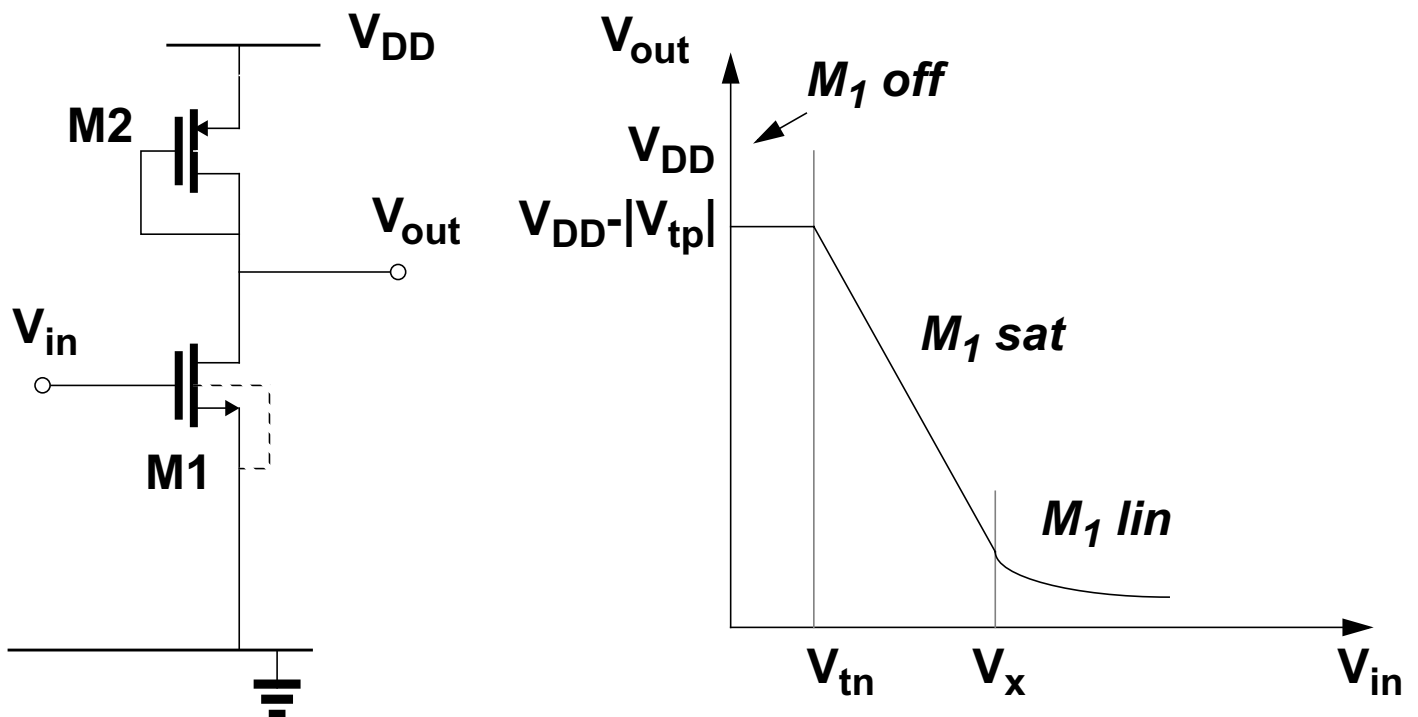


$$V_{BIAS}=3.5V, V_t=1V, \lambda=0.05V^{-1}, I_{D1}=100\mu A, V_{DD}=5V$$

- (i) Draw the small signal model for the circuit shown.
- (ii) What is the low-frequency small signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters and R_L ?
- (iii) What is the value of g_{m1} ?
What is the value of g_{ds1} ?
- (iv) What is the largest value of R such that M1 is operating in the saturated region?
- (v) What value of R gives the largest small-signal gain?
What is the largest small-signal gain?

4.2 Common source stage with Diode Load

4.2.1 CS stage with diode load -Large-signal behaviour



1. $V_{in}=0 \Rightarrow M1$ off $\Rightarrow V_{out}=V_{DD}-V_{tp}$

2. V_{in} increases.

When $V_{in} > V_{tn}$ M1 turns on in saturation and a current I flows

$$V_{out} = V_{DD} - |V_{gs2}|$$

$$V_{out} = V_{DD} - \sqrt{\frac{2I}{K'_p \frac{W_2}{L_2}}}$$

$$V_{out} = V_{DD} - \sqrt{\frac{2I}{K'_p \frac{W_2}{L_2}}}$$

$$V_{out} = V_{DD} - \sqrt{\frac{2}{K'_p \frac{W_2}{L_2}}} \cdot \sqrt{\frac{K'_n W_1}{2 L_1} (V_{gs1} - V_{tn})^2}$$

$$V_{out} = V_{DD} - \sqrt{\frac{K'_n \frac{W_1}{L_1}}{K'_p \frac{W_2}{L_2}}} \cdot (V_{in} - V_{tn})$$

In saturation the small-signal gain is given by

$$\frac{\delta V_{out}}{\delta V_{in}} = - \sqrt{\frac{K'_n \frac{W_1}{L_1}}{K'_p \frac{W_2}{L_2}}} \quad \begin{array}{l} \text{i.e. independent of bias conditions} \\ \Rightarrow \text{linear transfer characteristic} \\ \text{however } K'_n, K'_p \text{ vary independently} \end{array}$$

3. M1 goes out of saturation when $V_{out} < V_{in} - V_{tn}$ i.e. when

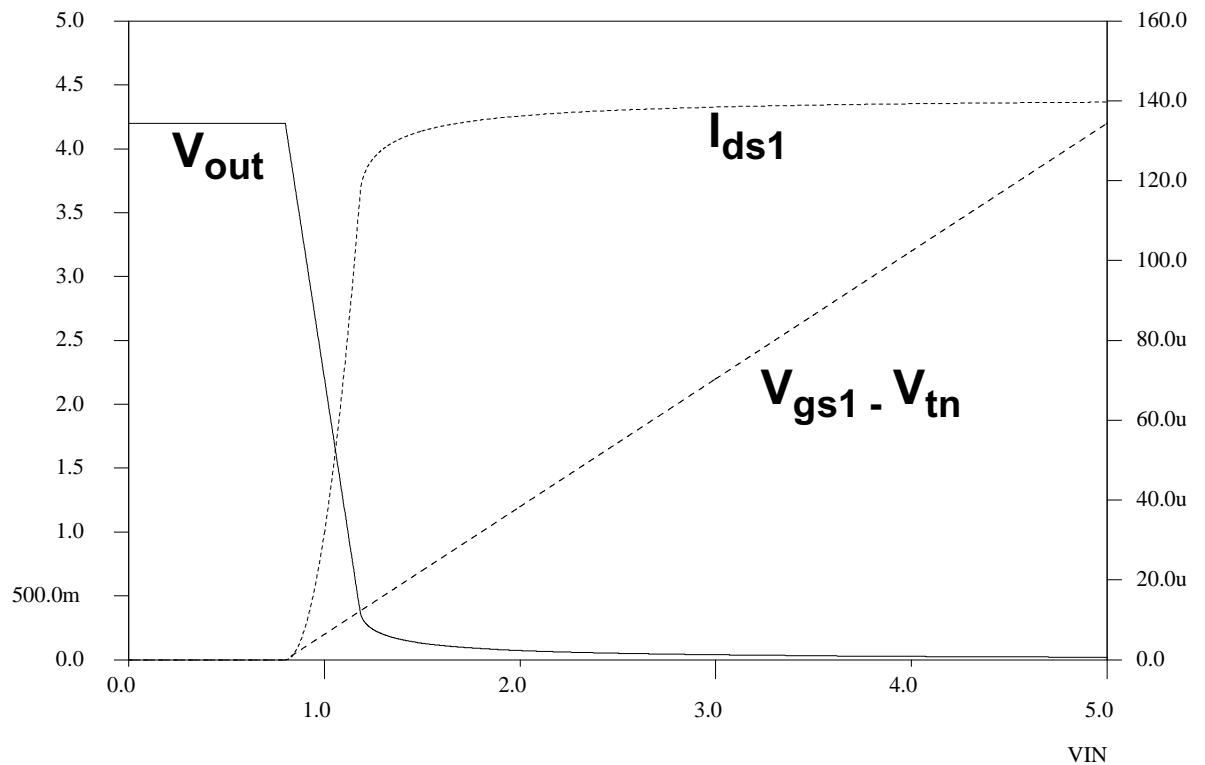
$$V_{out} = V_{DD} - \sqrt{\frac{K'_n \frac{W_1}{L_1}}{K'_p \frac{W_2}{L_2}}} \cdot (V_{in} - V_{tn}) < (V_{in} - V_{tn})$$

Common source stage with Diode Load - Graphical Example

$V_{DD}=5V$, $W_n/L_n = 10/1$, $W_p/L_p = 1/2.5$, $V_{tn}=0.8V$, $V_{tp}=-0.8V$,
 $K_n'=160\mu A/V$, $K_p'=40\mu A/V$.

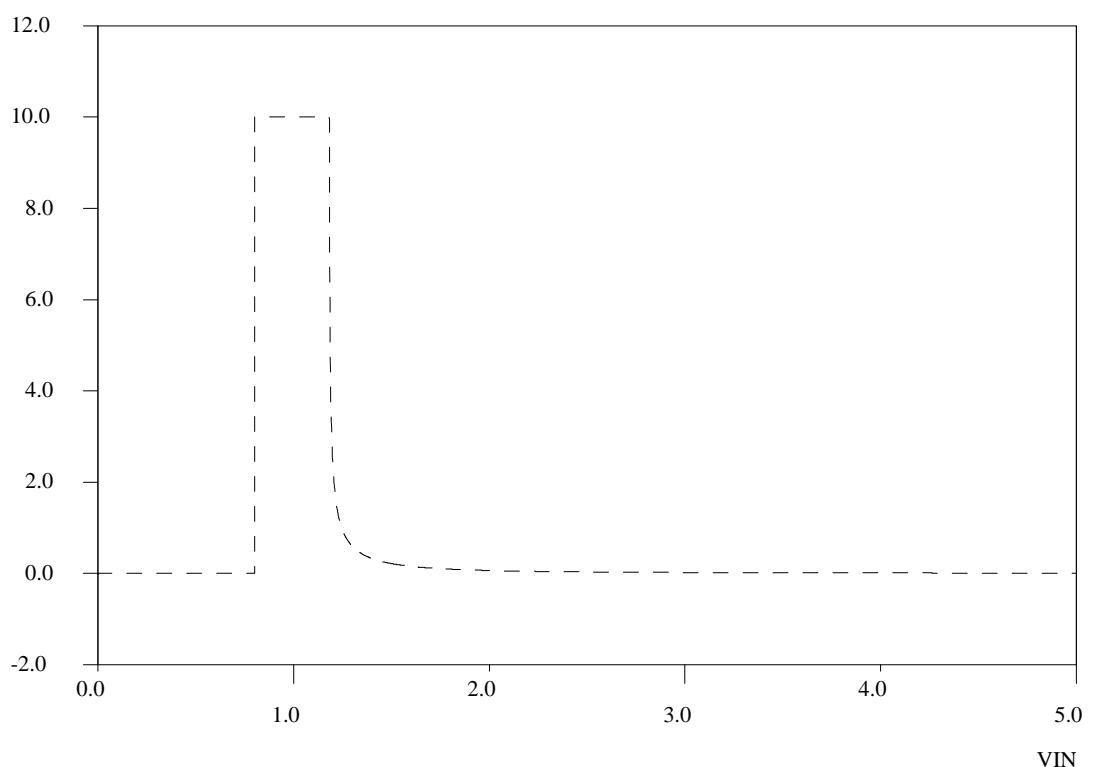
Output voltage, current

- y1-axis -
VOUT
VGTN
- y2-axis -
IDSN



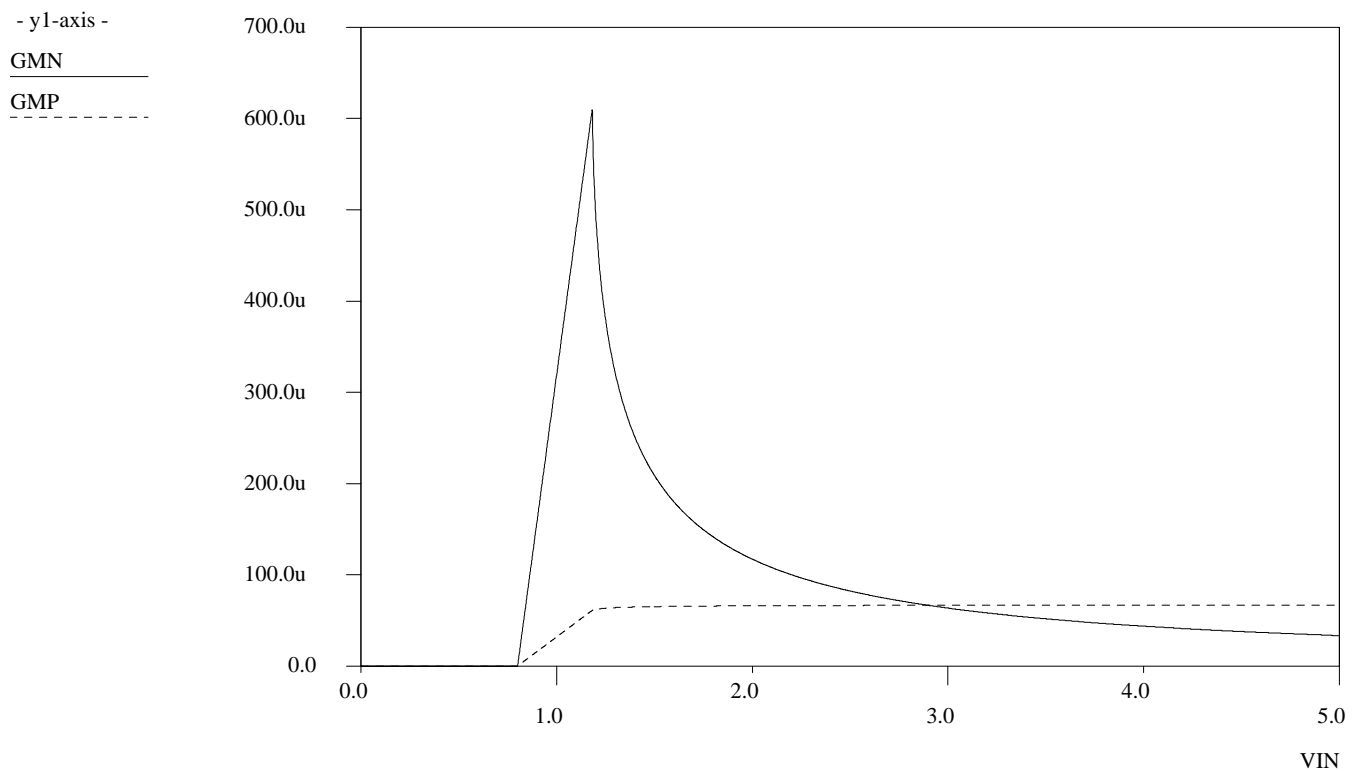
Derivative of output voltage (gain)

- y1-axis -
 $-dV_{out}/dV_{in}$



Common source stage with Diode Load - Graphical Example (contd.)

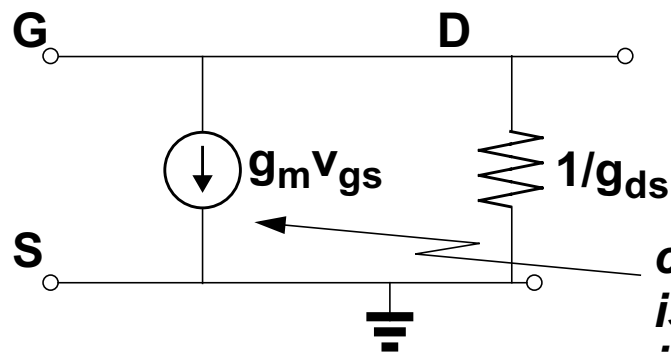
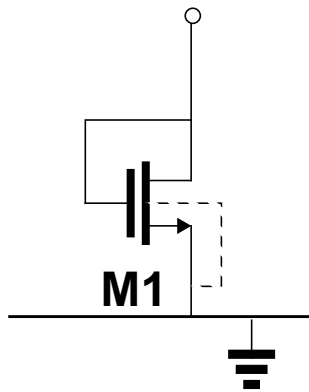
Transconductances.



Note constant gain due to constant g_{mn}, g_{mp} ratio.

4.2.2 Diode-connected MOS (small-signal model)

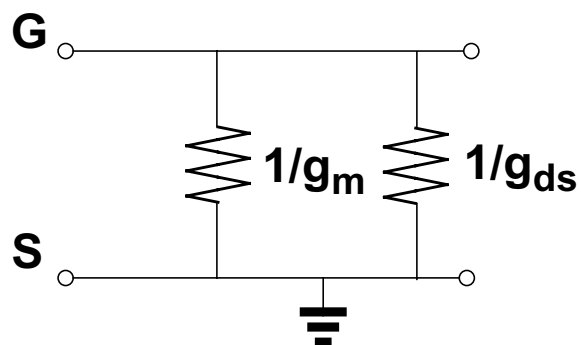
What is small-signal equivalent circuit?



current-source is determined by its terminals

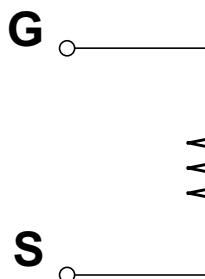
$$i = g_m v_{gs}$$

$$r = \frac{v}{i} = \frac{v}{g_m v_{gs}}$$



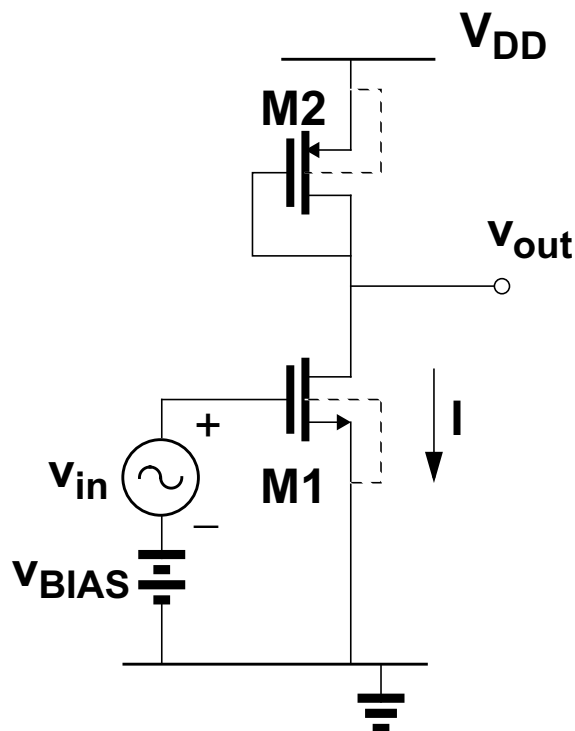
=> equivalent for small-s

$$g_m \gg g_{ds} \Rightarrow$$



4.2.3 CS stage with Diode Load - small-signal analysis

Example Problem - Common source stage with Diode Load (small-signal analysis)



- (i) Draw the small signal model for the circuit shown.
- (ii) What is the low-frequency small signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters?

Assume that $g_{m1} \gg g_{ds1}, g_{ds2}$ and that $g_{m2} \gg g_{ds1}, g_{ds2}$

- (iii) Calculate the gain if

$$V_{GS1} = 1V,$$

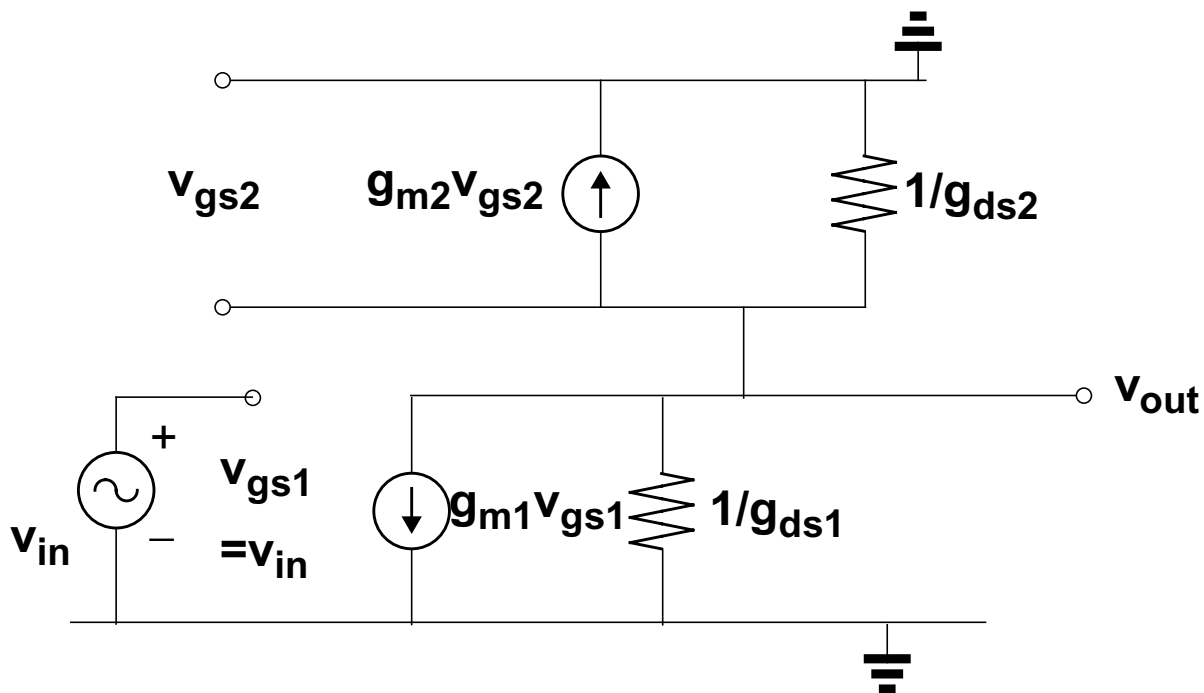
$$|V_{GS2}| = 2.8V,$$

$$|V_t| = 0.8V \text{ for } M1, M2.$$

Assume M1 is in saturation.

Solution

- (i) Draw the small signal model for the circuit shown in Figure 2. Ignore all capacitances.



- (ii) What is the low-frequency small signal voltage gain (v_{out}/v_{in})? Assume that $g_{m1} \gg g_{ds1}, g_{ds2}$ and that $g_{m2} \gg g_{ds1}, g_{ds2}$

Current at output node

$$g_{m1}v_{gs1} + g_{m2}v_{gs2} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$g_{m1}v_{in} + g_{m2}v_{out} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \cong -\frac{g_{m1}}{g_{m2}}$$

Alternatively recognise that the current of the current-source $g_{m2}v_{gs2}$ is determined by voltage across its terminals i.e. is equivalent to a resistance $1/g_{m2}$.

Since $1/g_{m2} \ll 1/g_{ds2}$, $1/g_{m2} \ll 1/g_{ds1}$, can write directly

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2}}$$

(iii) Calculate the gain if $V_{GS1}=1V$, $|V_{GS2}|=2.8V$, $|V_t| = 0.8V$ for M1,M2.

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2}}$$

Need $g_{m1} > g_{m2}$ for gain

$$= -\frac{2I/(V_{GS1} - V_{tn})}{2I/(|V_{GS2}| - |V_{tp}|)} = -\frac{|V_{GS2}| - |V_{tp}|}{V_{GS1} - V_{tn}}$$

$$= -\frac{2.8 - 0.8}{1 - 0.8} = -10$$

In dB:

$$A = 20\log\left|\frac{v_{out}}{v_{in}}\right| = 20dB$$

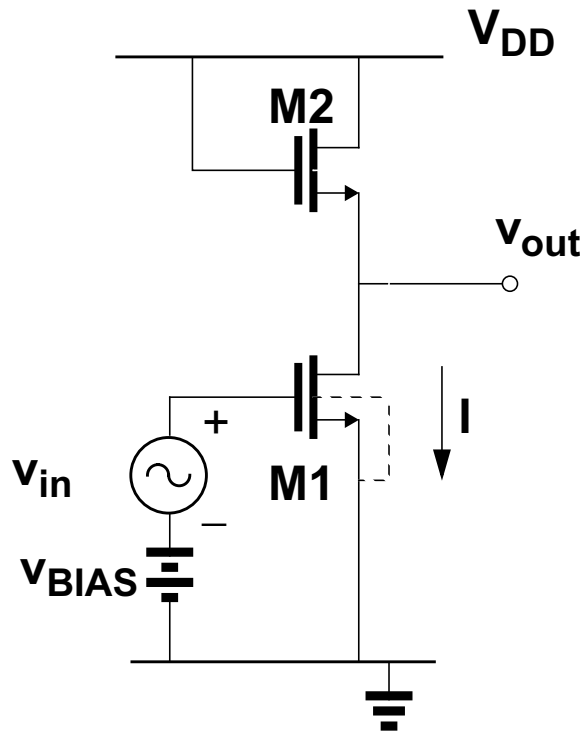
For high gain need $|V_{GS2}| > V_{GS1}$

Gain is limited by max. value of V_{GS2} and min. value of V_{GS1}

↓
headroom

↓
200mV for
strong inversion

Problem: - Common source stage with NMOS Diode Load



Assume M1 is biased in saturation.

- (i) Draw the small signal model for the circuit shown.
- (ii) What is the low-frequency small signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters?

Assume that $g_{m1} \gg g_{ds1}, g_{ds2}$ and that $g_{m2} \gg g_{ds1}, g_{ds2}$

- (iii) Calculate the gain if

$$W1=25, L1=1$$

$$W2=1, L2=1$$

$$\eta=0.3$$

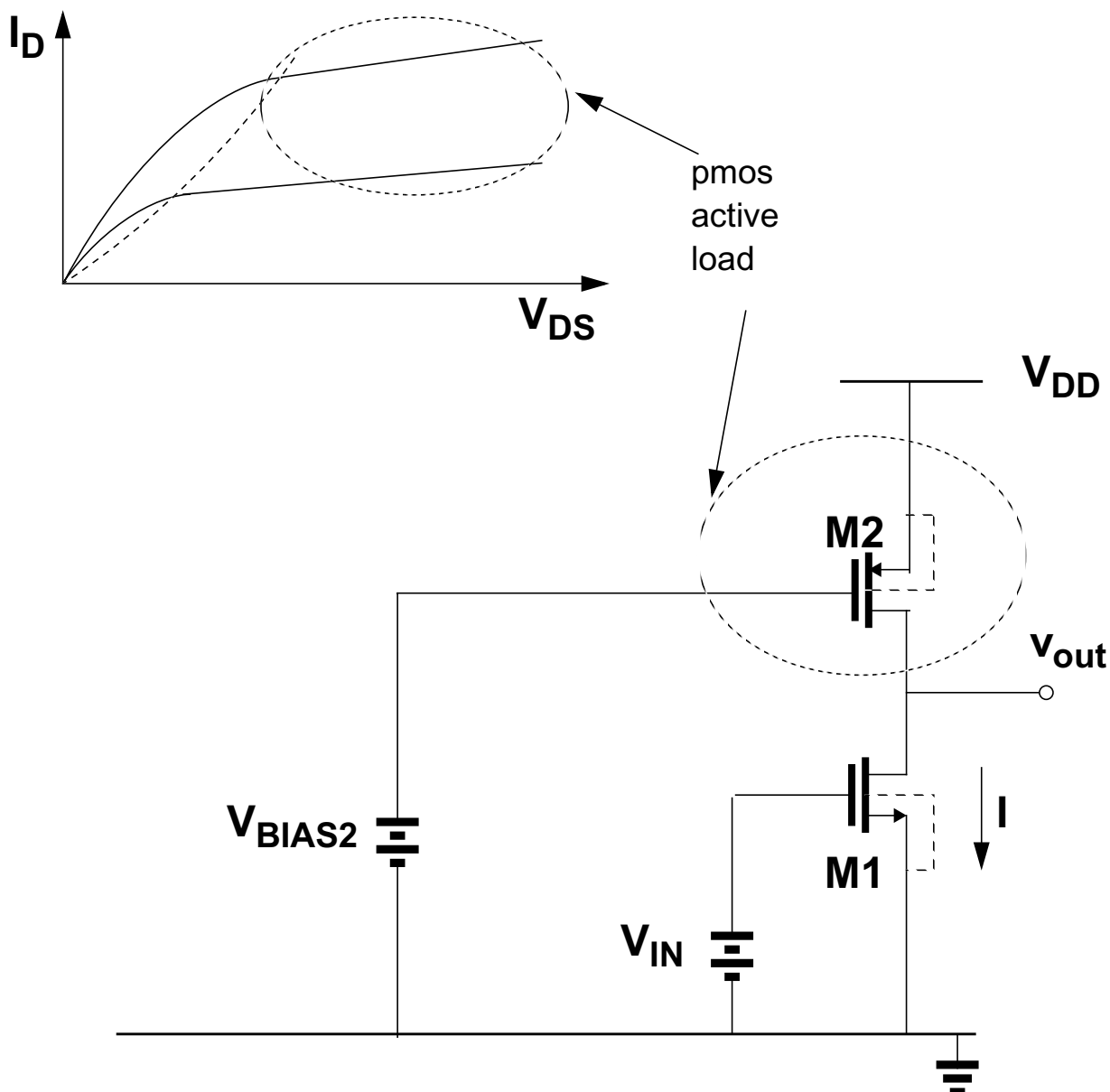
4.3 Common source stage with active load

Resistive load: gain costs voltage headroom

Diode load: gain costs voltage headroom

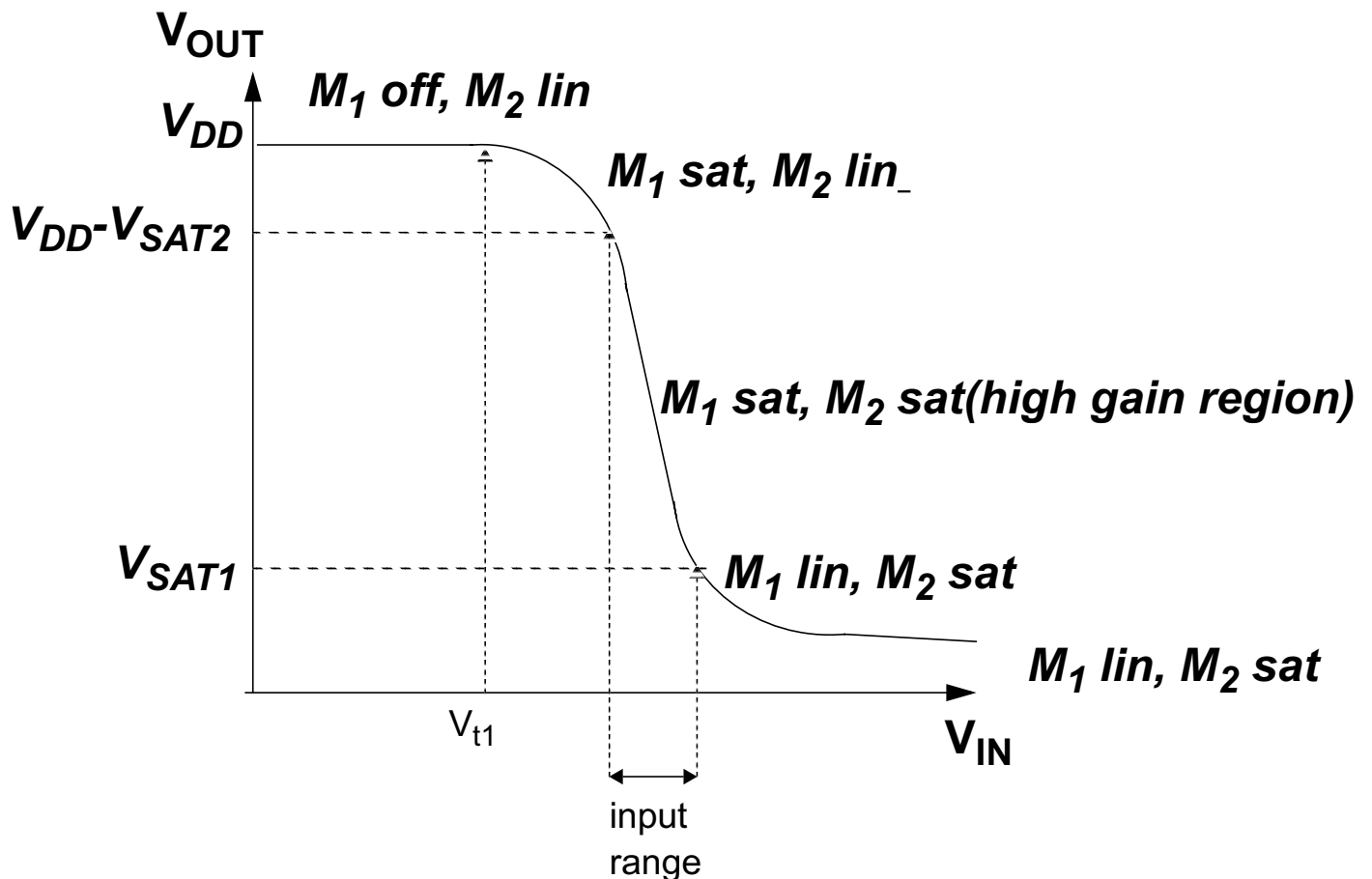
Need to decouple gain from dc voltage headroom

Use active load e.g. pmos in saturation



4.3.1 Common source stage with active load - Large signal behaviour

Sweep V_{in} from 0 to V_{DD}



Assume $V_{DD} - V_{BIAS2} > |V_{tp}|$

Initially M_1 off, V_{out} at $V_{DD} \Rightarrow M_2$ in linear region.

V_{IN} increases beyond $V_{tn} > M_1$ turns on in saturation.

V_{IN} increases further: I_{D1} increases, V_{out} decreases.

For a certain V_{out} , both M_1 and M_2 in saturation

For high gain both transistors need to be saturated

V_{in} increases further: V_{out} decreases M_1 goes out of saturation

Useful (high gain) output swing limited to $V_{DD} - V_{SAT1} - V_{SAT2}$

Allowed input swing for high gain is limited.

Large-signal behaviour with both M1, M2 in saturation

$$V_{out} = V_{DD} - |V_{ds2}|$$

Derive expression for V_{ds2} in terms of bias current I

$$I = \frac{K'_p W}{2 L} (V_{gsp} - V_{tp})^2 (1 + \lambda_p V_{ds2})$$

$$V_{ds2} = \frac{1}{\lambda_p} \left(\frac{I}{\frac{K'_p W}{2 L} (V_{gsp} - V_{tp})^2} - 1 \right)$$

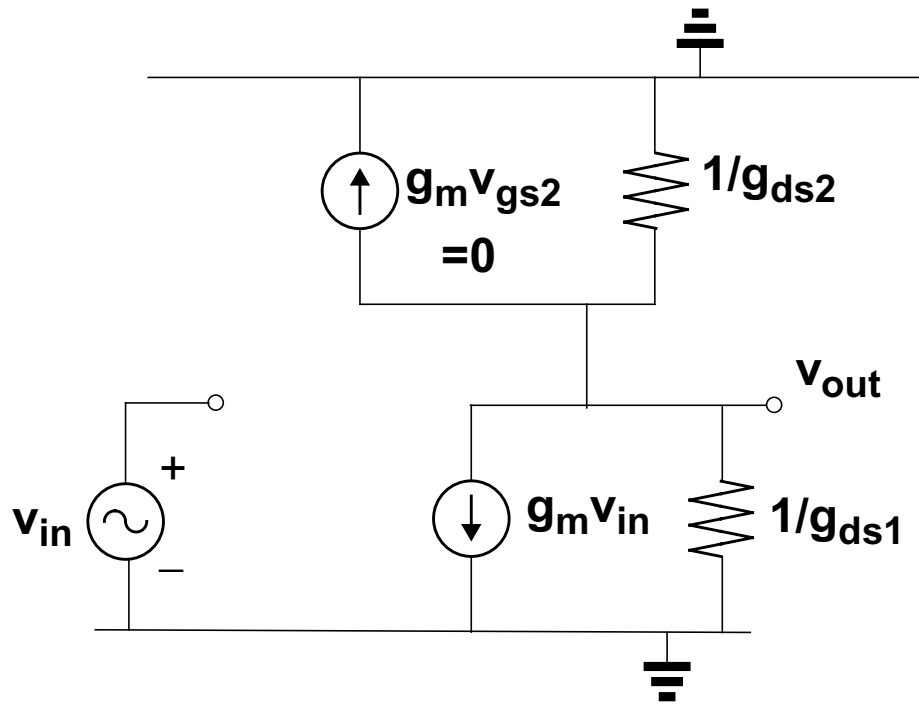
$$V_{out} = V_{DD} - \frac{1}{\lambda_p} \left(\frac{\frac{K'_n W}{2 L} (V_{gsn} - V_{tn})^2 (1 + \lambda_n V_{out})}{\frac{K'_p W}{2 L} (V_{gsp} - V_{tp})^2} - 1 \right)$$

$$\frac{\delta V_{out}}{\delta V_{in}} = -\frac{1}{\lambda_p} \left(\frac{\frac{K'_n W}{2 L}}{\frac{K'_p W}{2 L} (V_{gsp} - V_{tp})^2} \left(2(V_{gsn} - V_{tn})(1 + \lambda_n V_{out}) + \lambda_n \frac{\delta V_{out}}{\delta V_{in}} (V_{gsn} - V_{tn})^2 \right) \right)$$

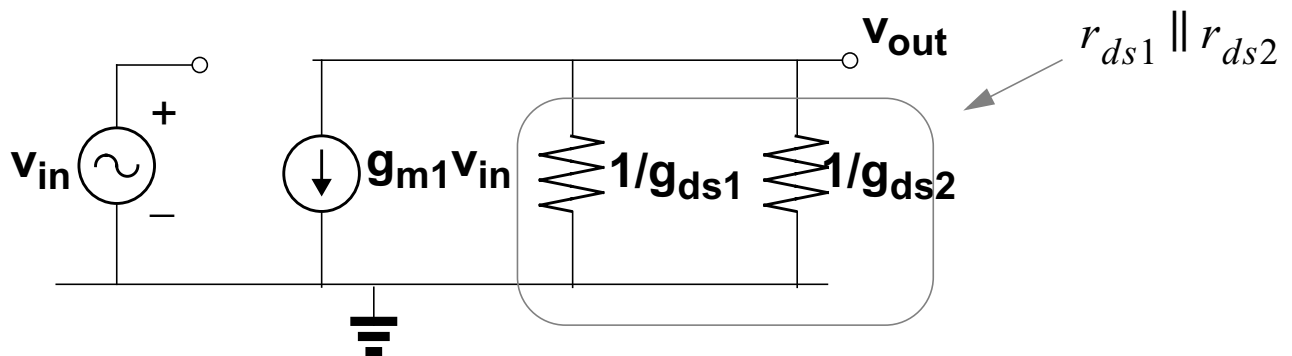
$$\frac{\delta V_{out}}{\delta V_{in}} \left(\lambda_p \frac{K'_p W}{2 L} (V_{gsp} - V_{tp})^2 + \lambda_n \frac{K'_n W}{2 L} (V_{gsn} - V_{tn})^2 \right) = -K'_n \frac{W}{L} (V_{gsn} - V_{tn})(1 + \lambda_n V_{out})$$

$$\frac{\delta V_{out}}{\delta V_{in}} = -\frac{g_{mn}}{(\lambda_n + \lambda_p)I}$$

4.3.2 CS stage with active load - small-signal analysis



Can redraw if wish:



$$g_{m1}v_{in} + (g_{ds1} + g_{ds2})v_{out} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

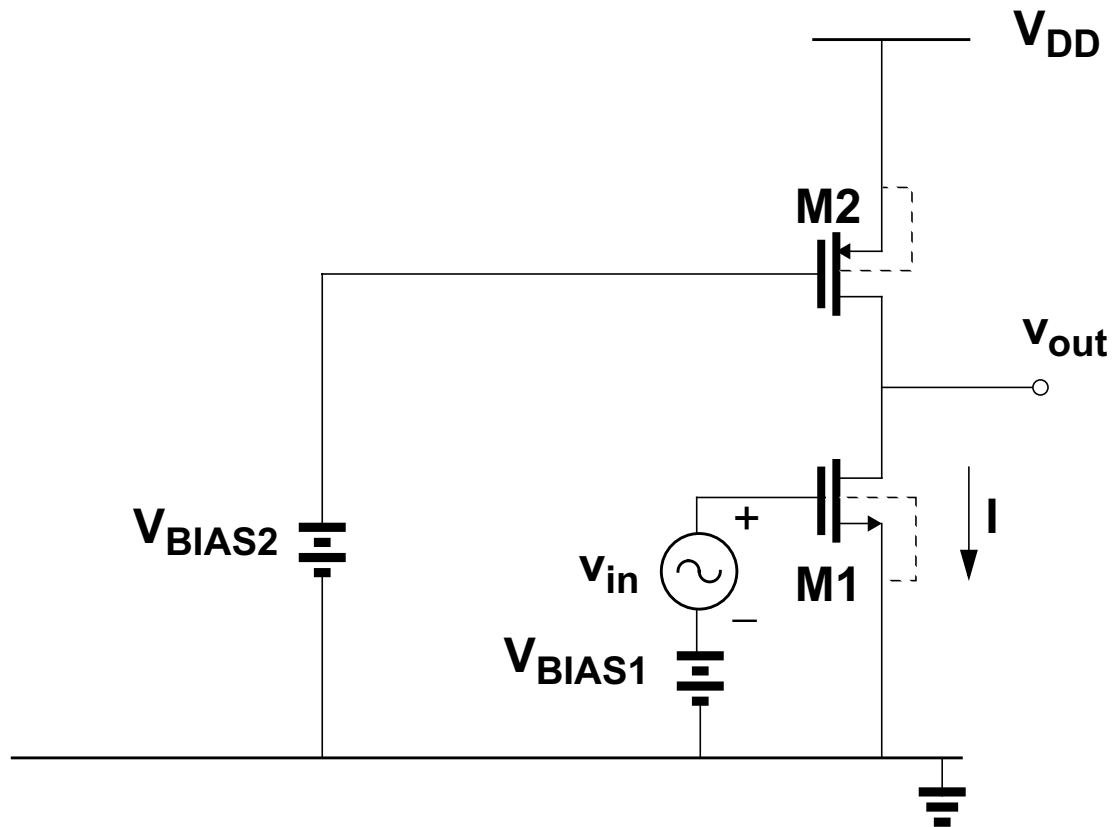
$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{(\lambda_n + \lambda_p)I}$$

$$\lambda \propto \frac{1}{L} \Rightarrow \text{Increase } L \text{ for more gain}$$

$$\text{But increasing } L \text{ increases } V_{SAT} = \sqrt{\frac{I}{(K'_n/2)W/L}}$$

Can increase W to restore V_{SAT} but get larger i.e. slower devices.

Example Problem - CS stage with active load



$V_{BIAS1}=1.2$, $V_{BIAS2}=1.8$, $V_{DD}=3$
 $V_{tn}=0.8V$, $V_{tp}=-0.8V$,
 $\lambda_p=0.04/L \text{ V}^{-1}$, $\lambda_n=0.04/L \text{ V}^{-1}$
 $K_n'=160\mu A/V$, $K_p'=40\mu A/V$
 $W1=10$, $L1=1$, $W2=40$, $L2=1$

- (i) Calculate the small-signal gain if both M1 and M2 are in saturation.
- (ii) What is the effect on the gain if the widths and lengths of all transistors are doubled?
- (iii) What happens if only the width of M2 doubled?

Solution

(i) Small-signal gain

Use previously derived expression for gain

$$\begin{aligned}\frac{v_{out}}{v_{in}} &= -\frac{g_{m1}}{g_{ds1} + g_{ds2}} \\&= -\frac{2I/(V_{GS1} - V_{t1})}{(\lambda_n + \lambda_p)I} = -\frac{2}{(V_{GS1} - V_{t1})(\lambda_n + \lambda_p)} \\&= -\frac{2}{0.4 \cdot 0.08} = -62.5 = 36dB\end{aligned}$$

(ii) Effect on the gain if the widths and lengths of all transistors are doubled

W/L constant so current constant

W/L unchanged \Rightarrow same current, same $V_{GS} - V_t$

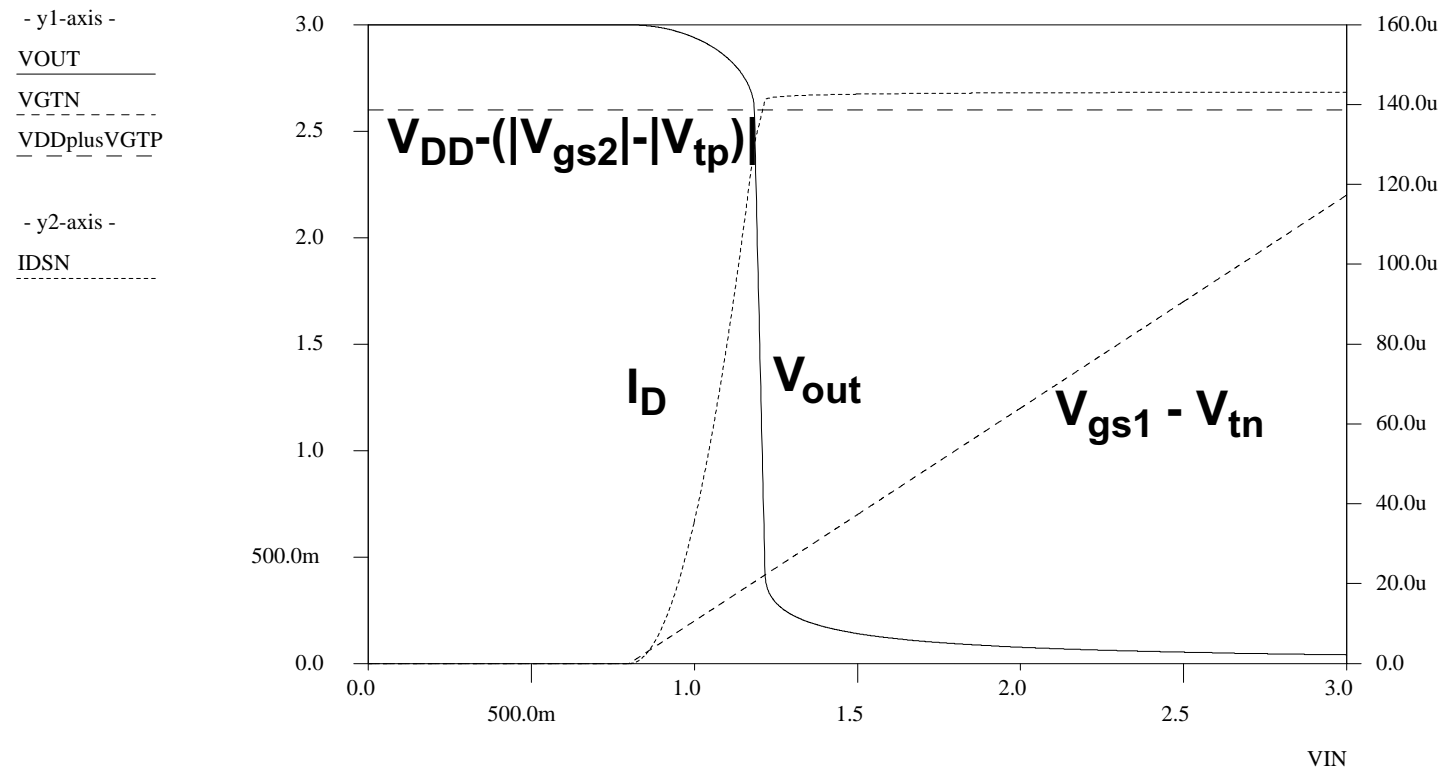
\Rightarrow devices still in saturation

$\Rightarrow g_{m1}$ unchanged

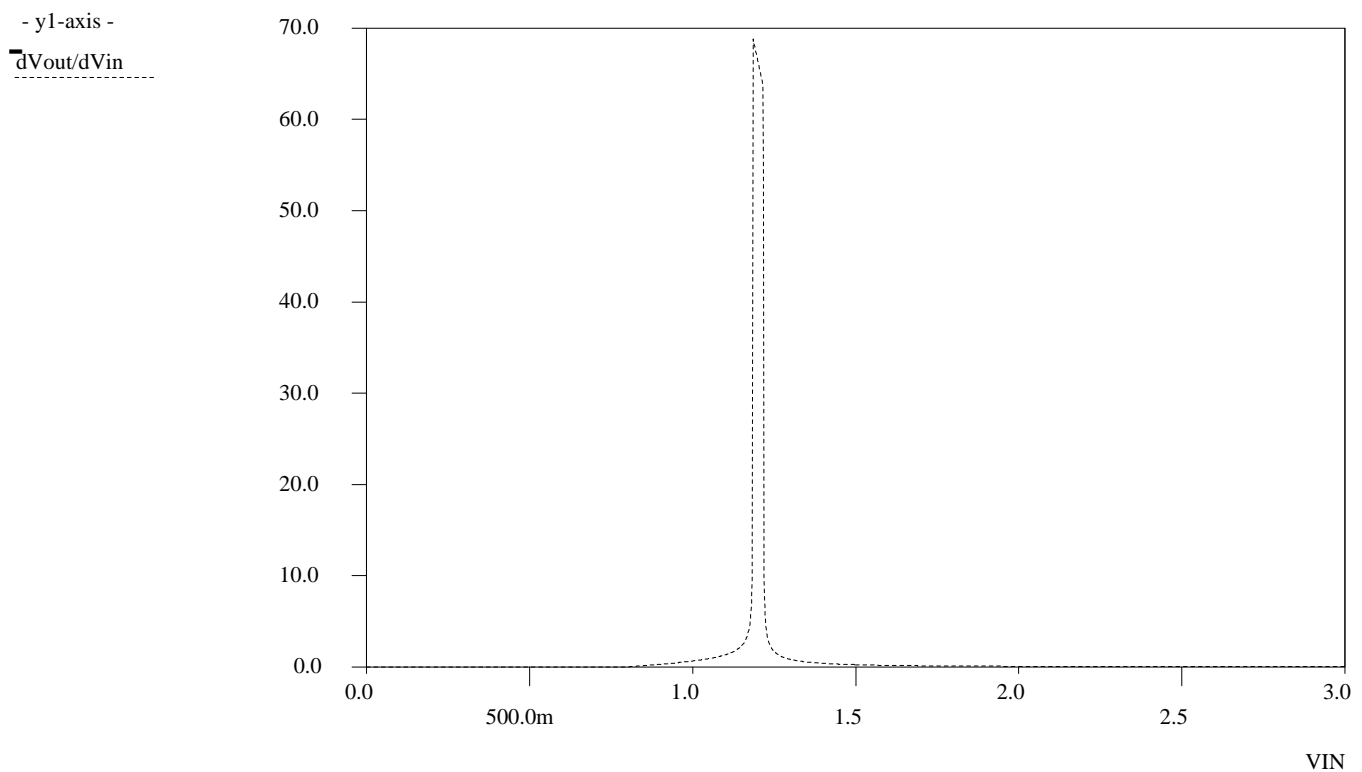
$$\lambda_{p,n} = \frac{0.04}{L} \Rightarrow \text{gds halved}$$

\Rightarrow gain doubled

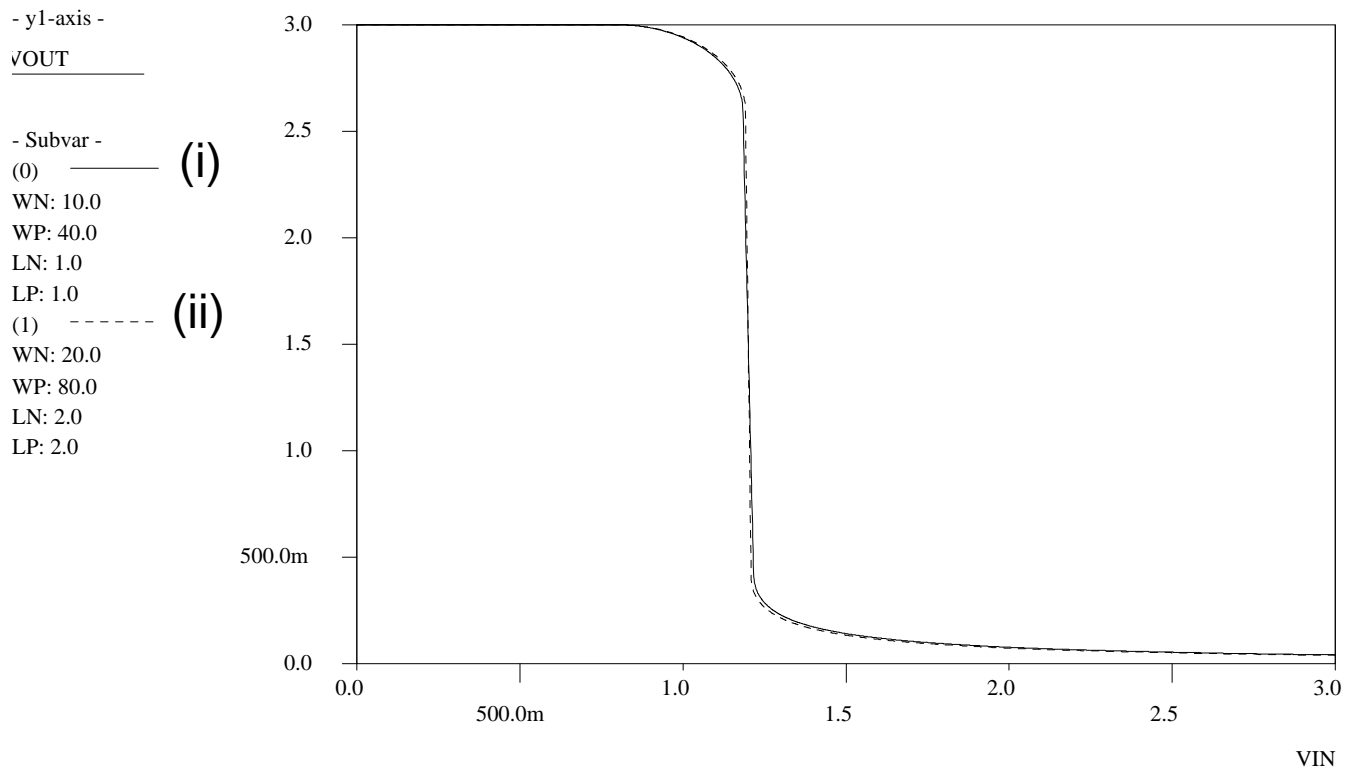
Output voltage, current for (i)



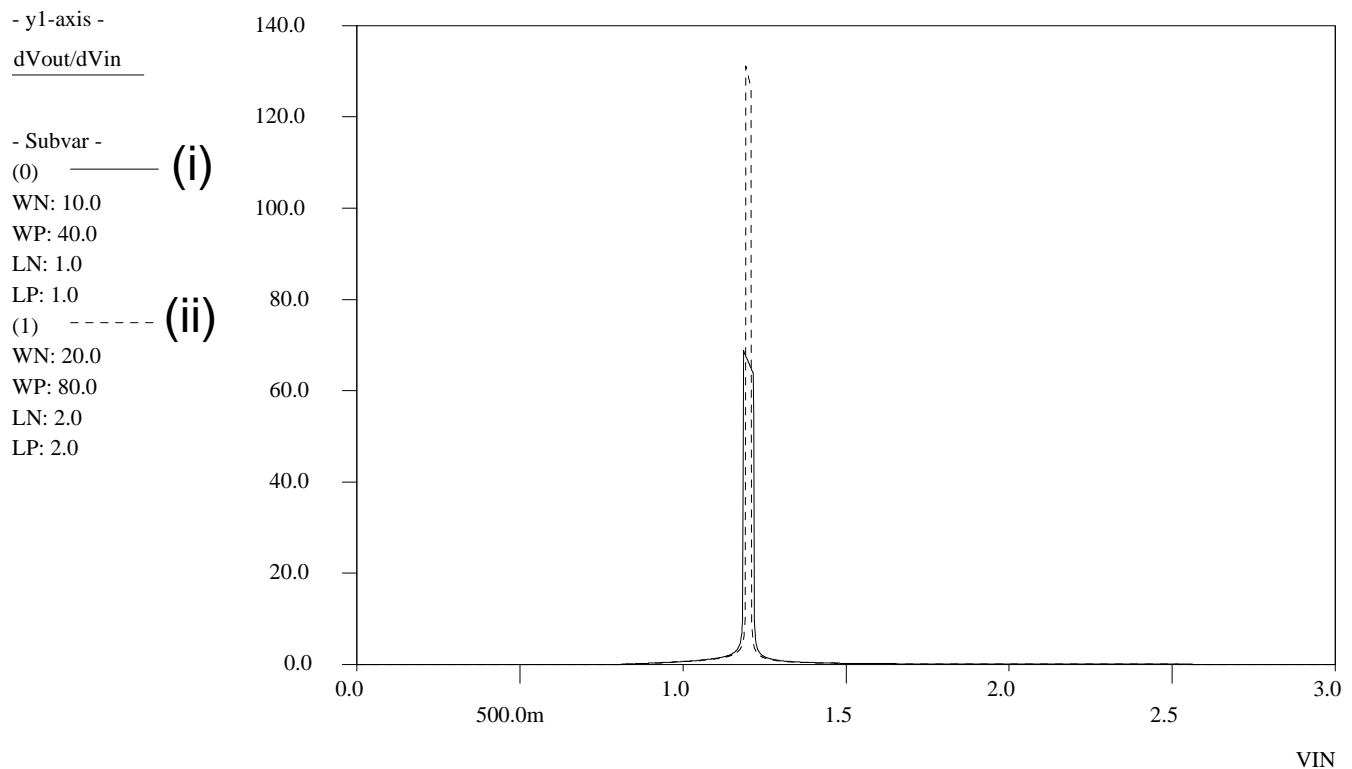
Derivative of output voltage (gain) for (i)



Output voltage for (i), (ii)



Derivative of output voltage (i.e. gain) for (i), (ii)



(iii) Effect on the gain if only the width of M2 doubled
 If width of M2 is doubled and V_{BIAS2} remains the same then output current of M2 doubles if M2 remains in saturation.
 However as V_{BIAS1} is unchanged so V_{GS} of M1 unchanged.
 Voltage at output rises i.e. V_{DS} of M1 increases.
 However as current is only a weak function of V_{DS} in saturation, the output voltage needs to rise a lot for even a small increase in current.
 \Rightarrow M2 will go into linear region long before current from M1 doubles.
 M2 out of saturation means gain collapses.

To restore M2 to saturation, V_{BIAS1} needs to increase so that current of M1 is doubled in saturation.
 $\Rightarrow V_{GS1} - V_{tn}$ needs to increase by $\sqrt{2}$
 $\Rightarrow V_{BIAS1}$ needs to increase to 1.365V
 If this happens:

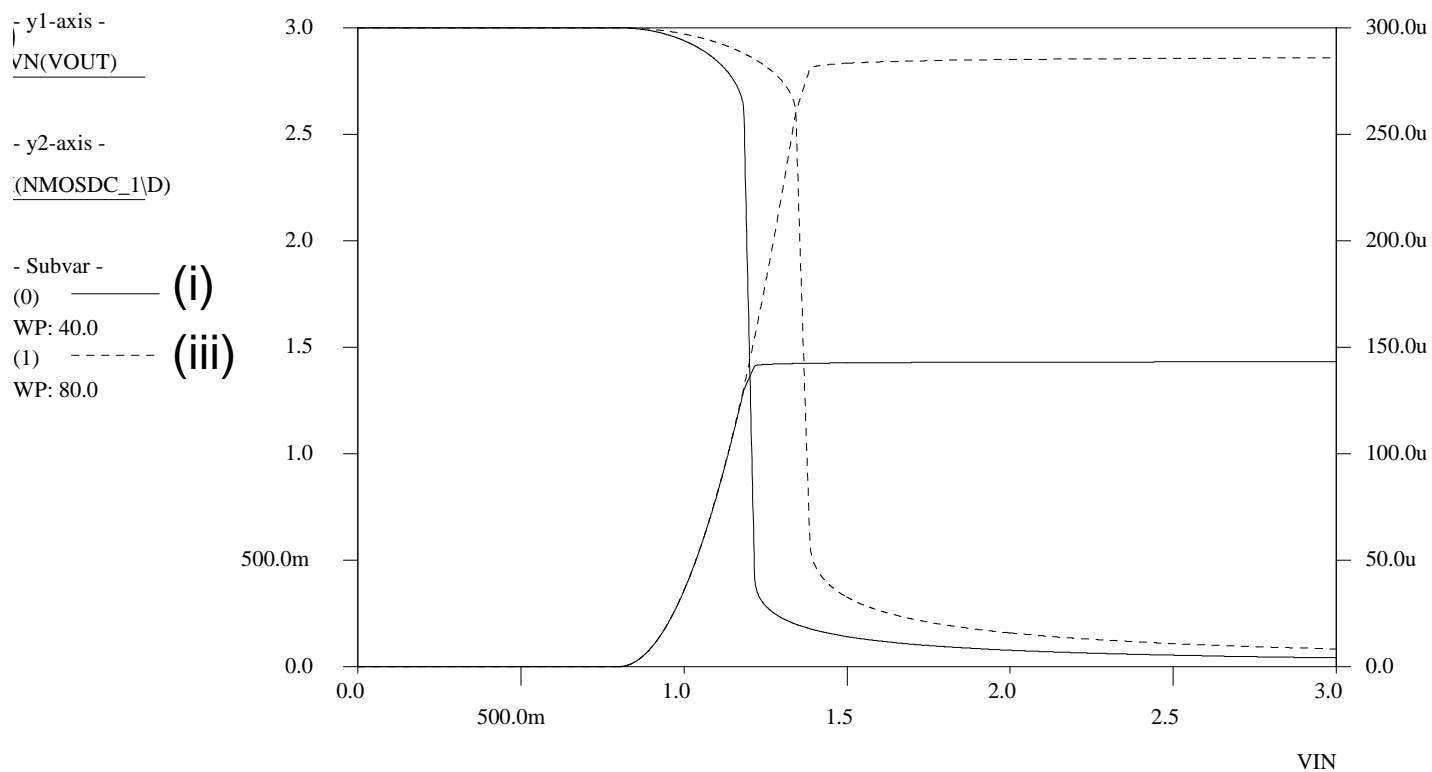
$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

Using $g_m = \sqrt{2K'_n \frac{W}{L} I_D} \Rightarrow g_m \text{ increases by } \sqrt{2}$

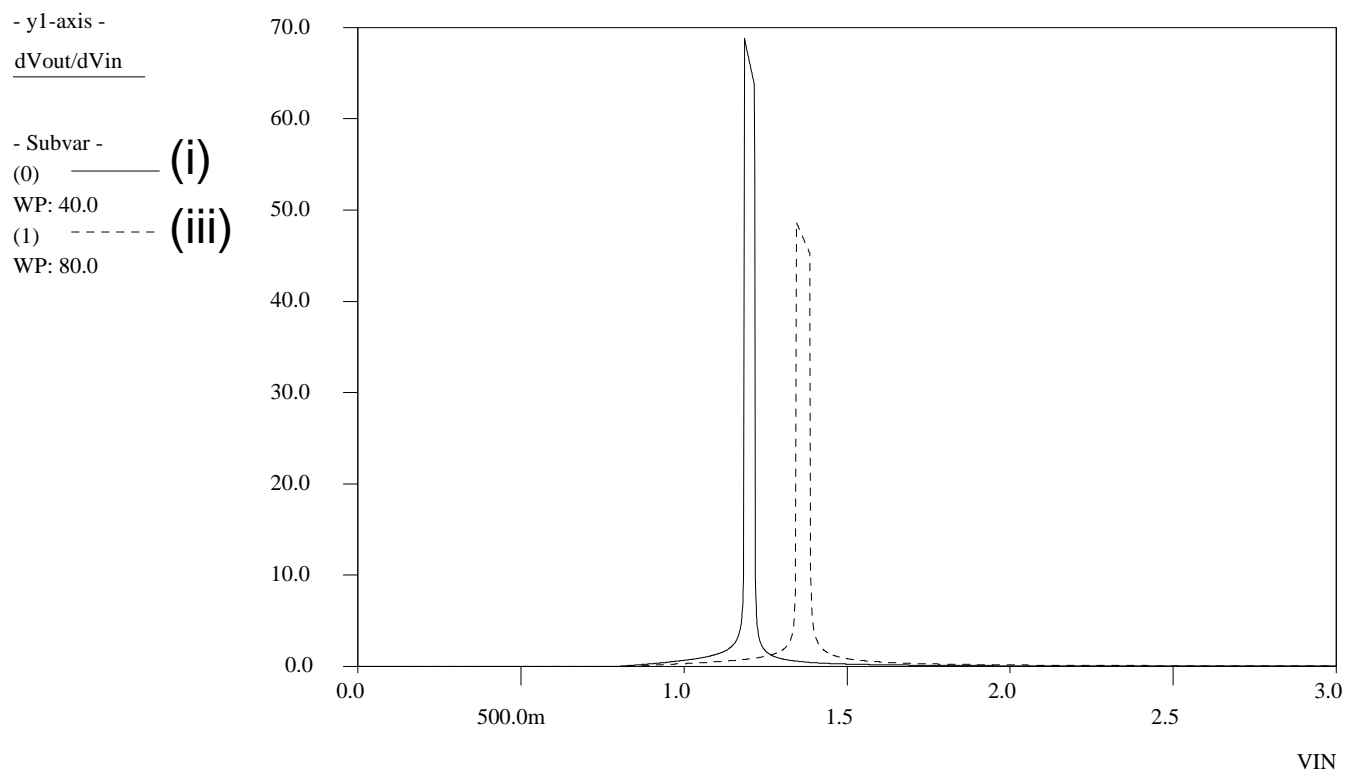
Using $g_{ds1} = (\lambda_n + \lambda_p)I \Rightarrow g_{ds} \text{ increases by } 2$

\Rightarrow gain decreases by $\sqrt{2}$

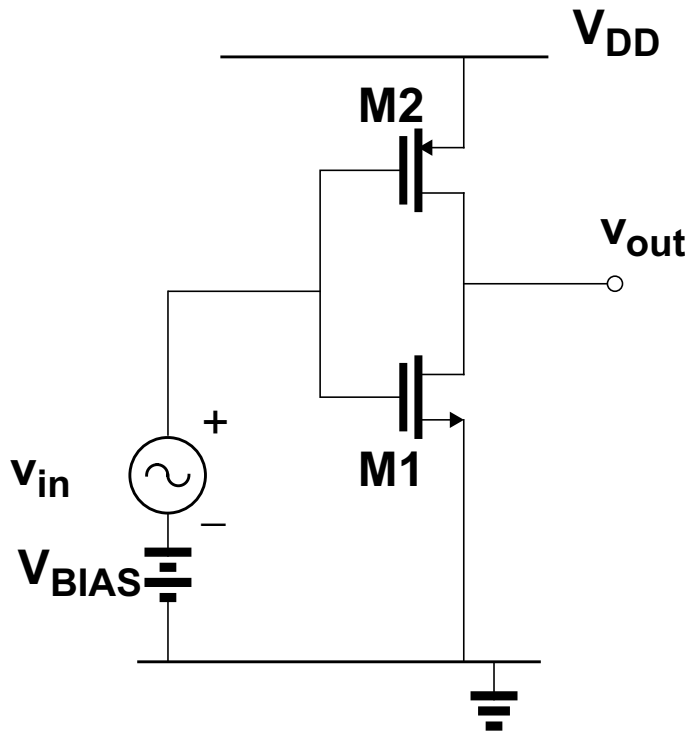
Output voltage, current for (i), (iii)



Derivative of output voltage (gain) for (i), (iii)



Problem: CS stage (CMOS Inverter)



Assume M1 and M2 are biased in saturation.

- (i) Draw the small signal model for the circuit shown.
- (ii) Derive an expression for the low-frequency small signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters?

Assume that $g_{m1} \gg g_{ds1}, g_{ds2}$ and that $g_{m2} \gg g_{ds1}, g_{ds2}$

- (iii) Calculate the gain if

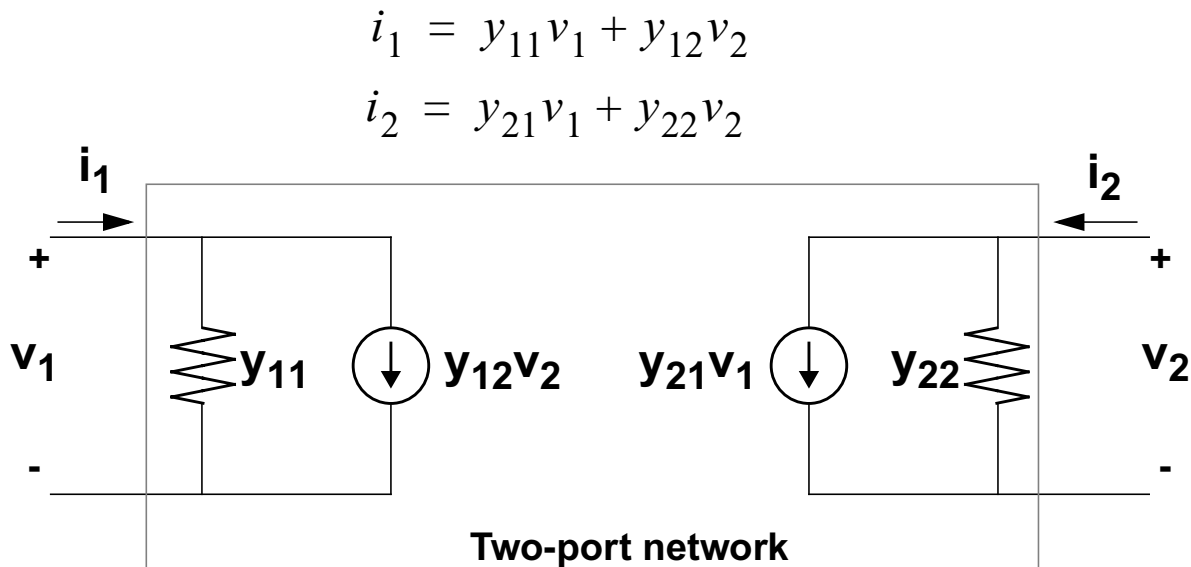
$$\begin{aligned} V_{DD} &= 3, V_{BIAS} = 1.5, |V_t| = 1 \\ I_D &= 100 \mu A, \lambda_p = \lambda_n = 0.05 V^{-1} \\ W_1 &= 10, L_1 = 1 \\ W_2 &= 40, L_2 = 1 \end{aligned}$$

4.4 Two-port analysis and y-parameters

We have analysed the small-signal gain of the common source stage with 3 different loads - resistive, diode, active.

A more general model, independent of load, would be useful.

=> two-port model with admittance (y) parameters



Assumption: linear network, no independent sources

$$y_{11} = \left. \frac{i_1}{v_1} \right|_{v_2 = 0}$$

Input admittance, output short-circuited

$$y_{12} = \left. \frac{i_1}{v_2} \right|_{v_1 = 0}$$

Reverse transconductance, input short-circuited

$$y_{21} = \left. \frac{i_2}{v_1} \right|_{v_2 = 0}$$

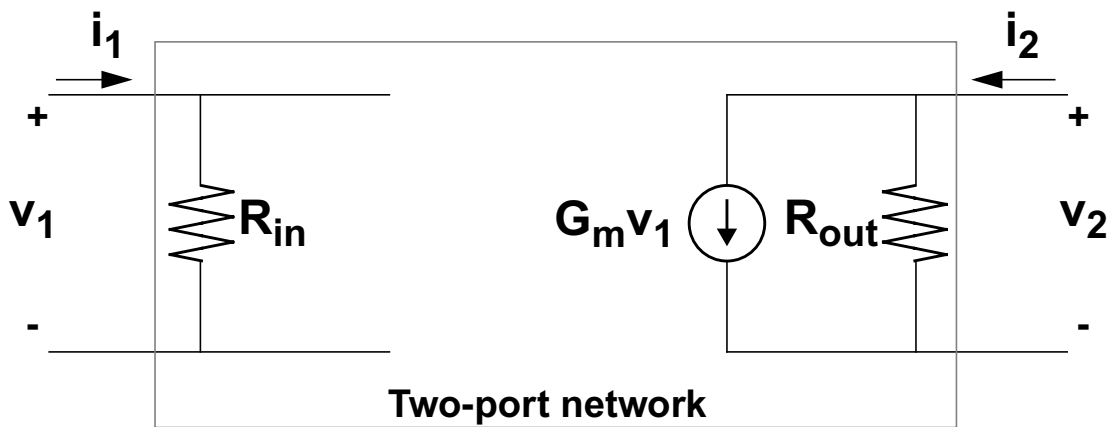
Forward transconductance, output short-circuited

$$y_{22} = \left. \frac{i_2}{v_2} \right|_{v_1 = 0}$$

Output admittance, input short-circuited

If network is unilateral, reverse transconductance is zero

Redraw network:



Define $R_{in} = \frac{1}{y_{11}}$ $G_m = y_{21}$ $R_{out} = \frac{1}{y_{22}}$ $G_{out} = \frac{1}{R_{out}}$

Intrinsic (unloaded i.e. $i_2=0$) gain of network given by

$$G_{m1}v_1 + \frac{v_2}{R_{out}} = 0 \quad \text{or} \quad G_{m1}v_1 + G_{out}v_2 = 0$$

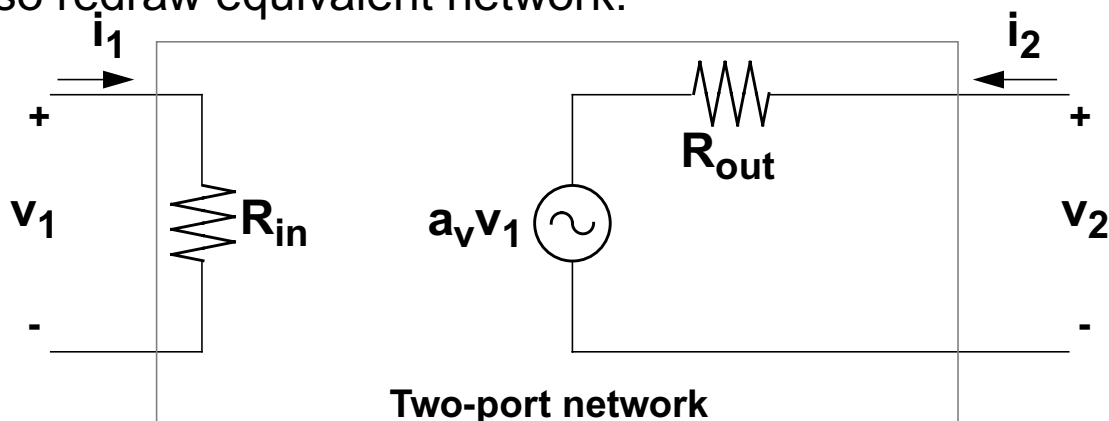
$$a_v = \left. \frac{v_2}{v_1} \right|_{i_2=0} = -G_m R_{out} = -\frac{G_m}{G_{out}}$$

If output is loaded by Z_L then the gain of network given by

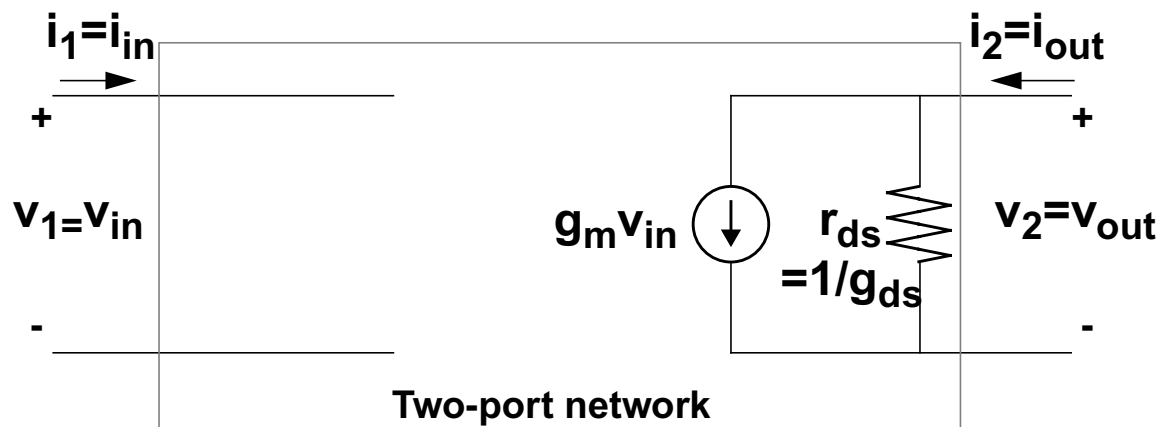
$$G_{m1}v_1 + G_{out}v_2 + G_L v_2 = 0$$

$$a_v = \left. \frac{v_2}{v_1} \right|_{i_2=0} = -G_m (R_{out} \parallel R_L) = -\frac{G_m}{G_{out} + G_L}$$

Can also redraw equivalent network:



Example: Common source stage (output unloaded)



$$G_m = \left. \frac{i_{out}}{v_{in}} \right|_{v_2 \equiv v_{out} = 0} = g_m$$

$$R_{in} = \left. \frac{v_{in}}{i_{in}} \right|_{v_2 \equiv v_{out} = 0} = \infty$$

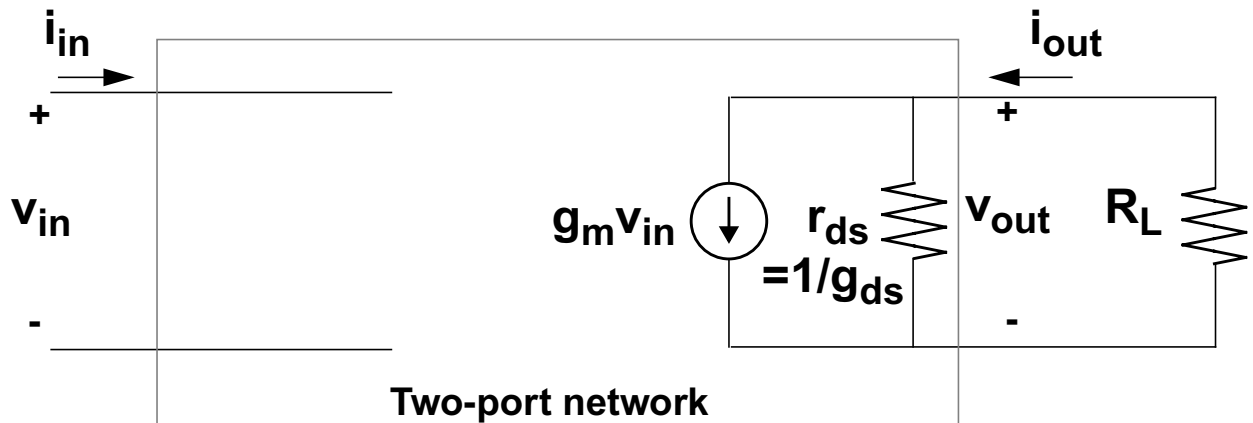
$$R_{out} = \left. \frac{v_{out}}{i_{out}} \right|_{v_1 \equiv v_{in} = 0} = r_{ds} = \frac{1}{g_{ds}} \Rightarrow G_{out} = g_{ds}$$

Unloaded gain given by

$$a_v = \left. \frac{v_{out}}{v_{in}} \right|_{i_{out} = 0} = -\frac{G_m}{G_{out}} = -\frac{g_m}{g_{ds}}$$

Example: Common source stage (output loaded)

Connect load at output



Gain now given by

$$a_v = -G_m(R_{out} \parallel R_L) = -\frac{G_m}{G_{out} + G_L}$$

$$a_v = -g_m(r_{ds} \parallel R_L) = -\frac{g_m}{g_{ds} + \frac{1}{R_L}}$$

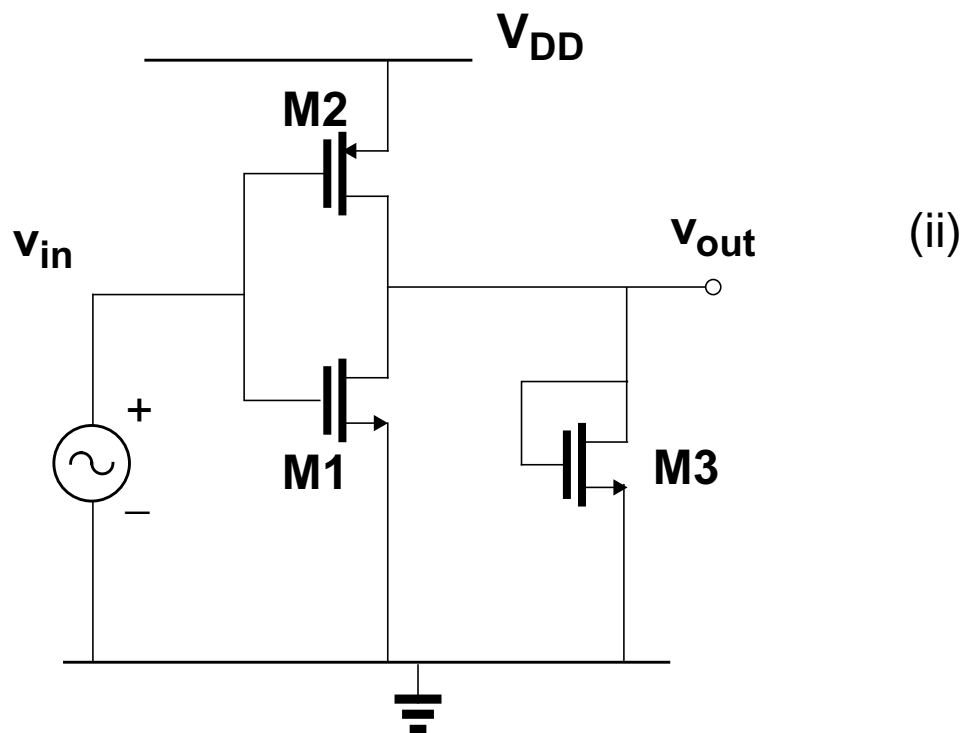
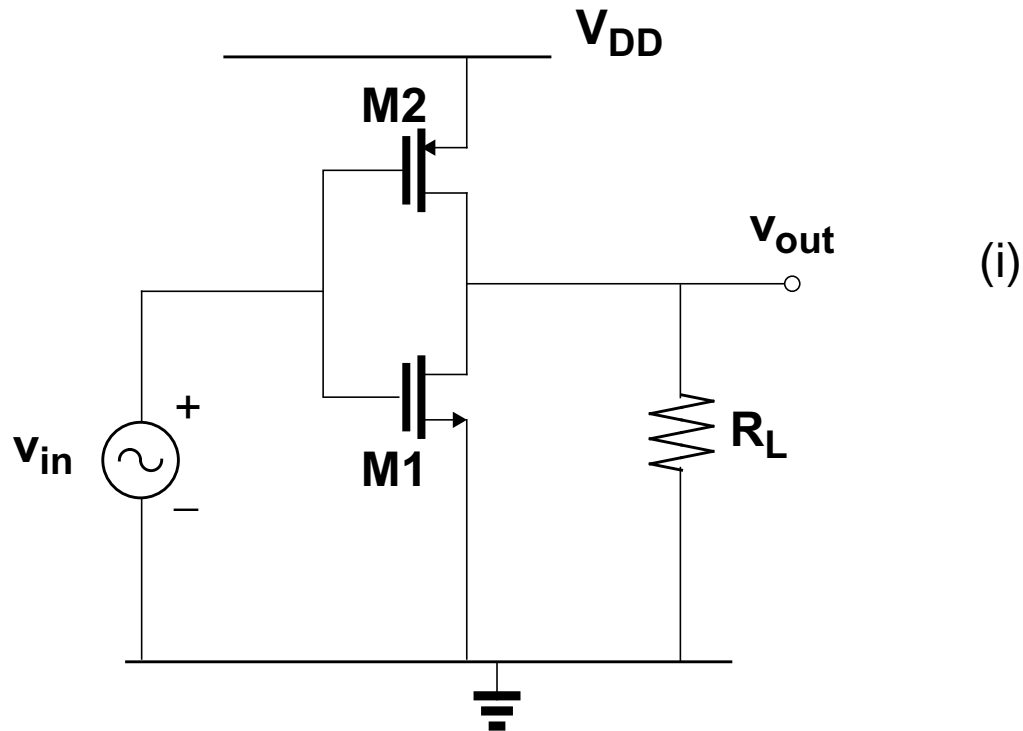
Can write directly

$$a_v = -\frac{g_m}{g_{ds} + \frac{1}{R_L}} \quad \text{for resistive load}$$

$$a_v = -\frac{g_{mn}}{g_{dsn} + g_{mp} + g_{dsp}} \quad \text{for PMOS diode load}$$

$$a_v = -\frac{g_{mn}}{g_{dsn} + g_{dsp}} \quad \text{for active PMOS load}$$

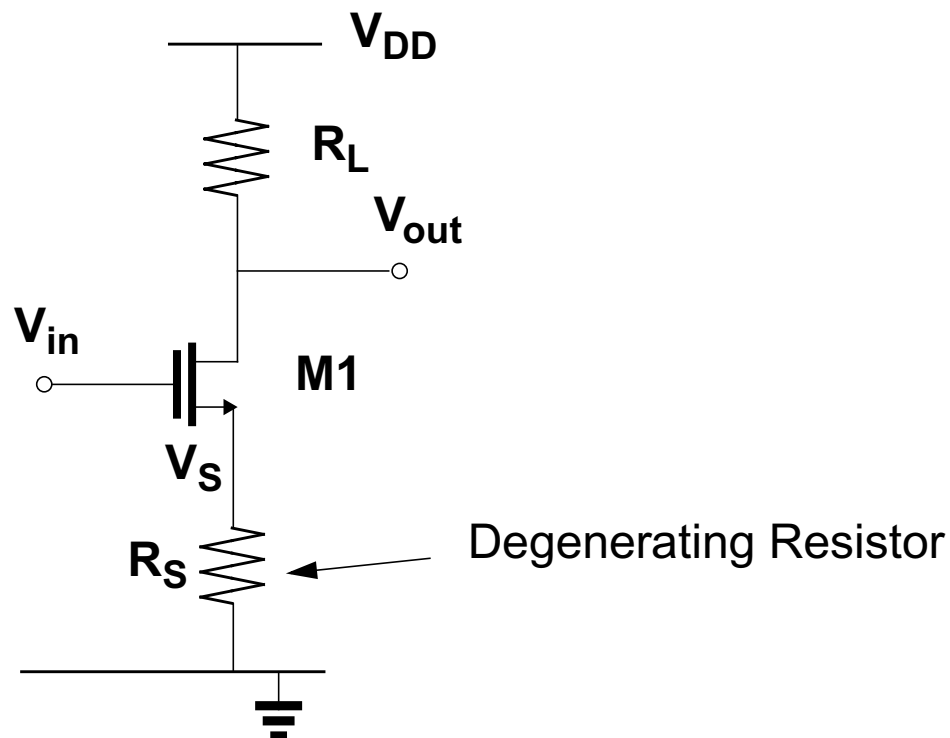
Problem: CMOS Inverter & y-parameters



Use y-parameters to calculate the small-signal gain of a CMOS inverter (both devices are in saturation) with

- (i) resistive load
- (ii) NMOS diode load

4.5 CS stage with Resistive degeneration



Common source stage: non-linear voltage-current relationship due to square-law dependence of drain current on overdrive voltage V_{GT}

Can cause non-linearity (distortion) in output voltage signal

Previously: used MOS diode load to cancel non-linearity

Other possibility: source degeneration

Part of V_{in} across transistor, part across R_S

4.5.1 CS stage with Res. degeneration - Large-signal behaviour

$V_{in} = 0 \Rightarrow$ M1 off. $V_{out} = V_{DD}$

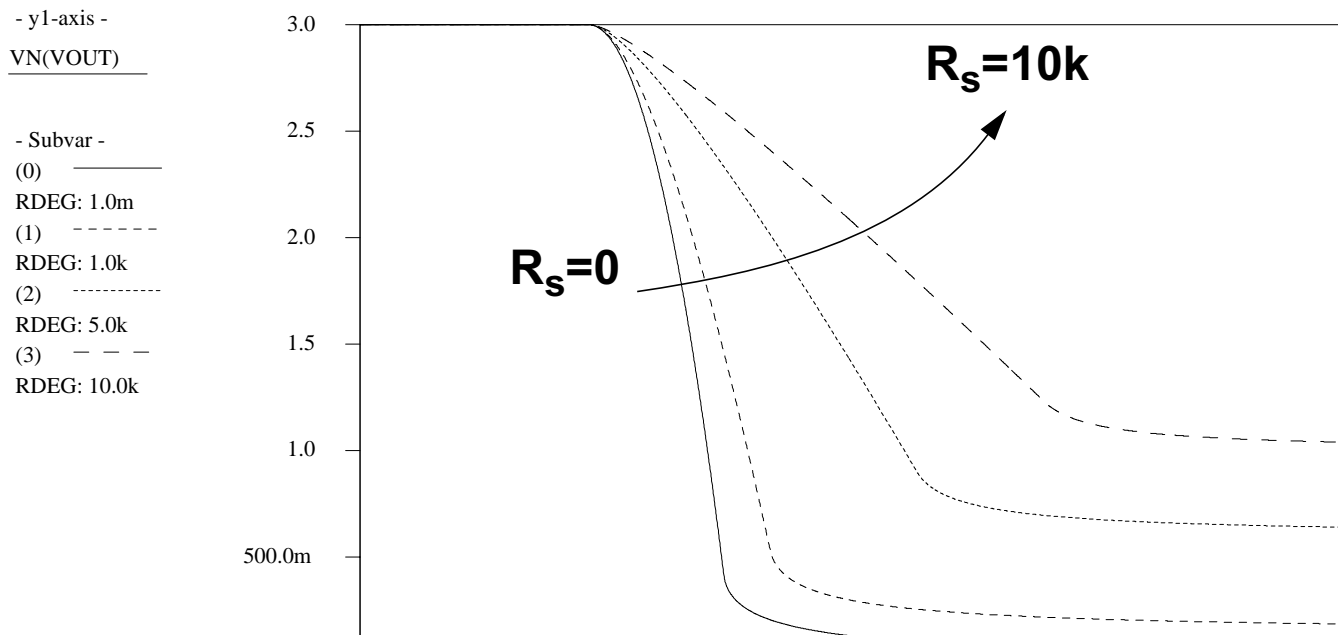
$V_{in} > V_t \Rightarrow$ M1 turns on, current flows, V_{out} falls

Increase in V_{in} : some of V_{in} across M_1 gate sources, some across R_S
 I_{D1} increases less than when $R_S=0$ ($G_m < g_m$)

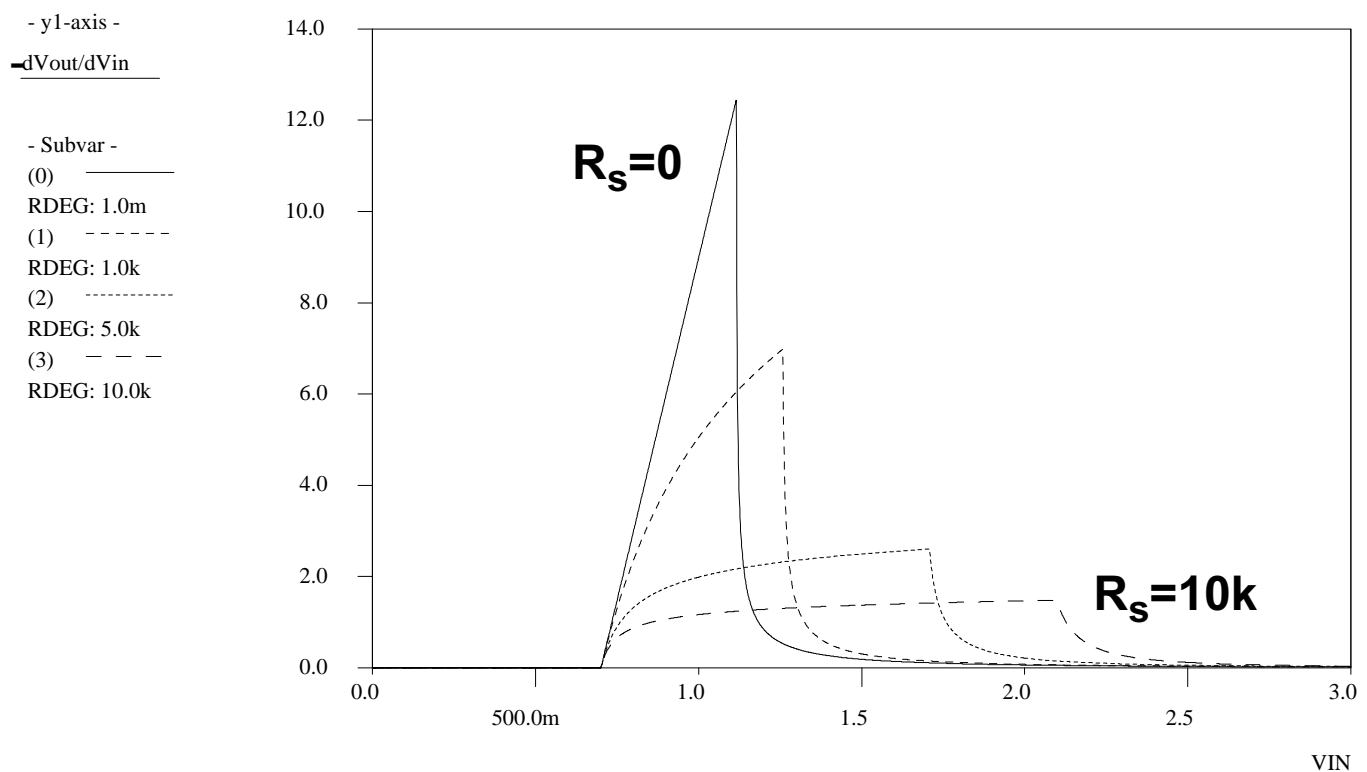
Common source stage with Resistive degeneration

$V_{DD}=3V$, $W/L = 10/1$, $V_{tn}=0.7V$, $K_n'=160\mu A/V$, $R_L=20k\Omega$.

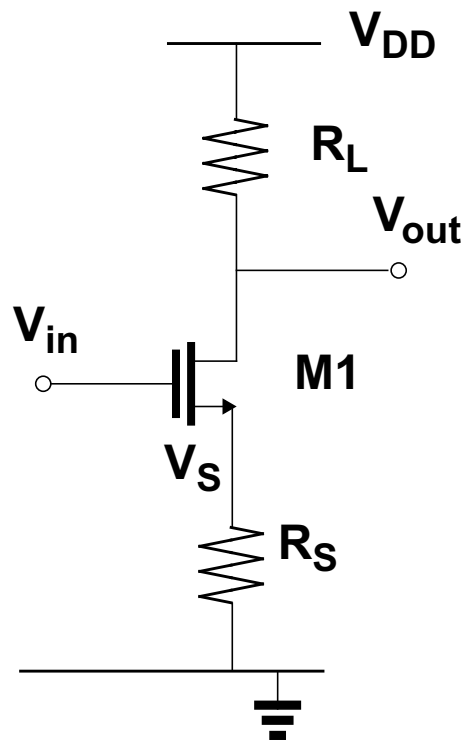
Output voltage as V_{in} is swept from 0V



Derivative of output voltage (gain)



4.5.2 CS stage with Res. degeneration - Large-signal behaviour: transconductance



First-order approach, neglecting body effect, output conductance:

$$\begin{aligned}
 I_D &= \frac{K'_n W}{2L} (V_{GS} - V_t)^2 = \frac{K'_n W}{2L} (V_{in} - V_S - V_t)^2 \\
 &= \frac{K'_n W}{2L} (V_{in} - I_D R_S - V_t)^2
 \end{aligned}$$

Interested first of all in transconductance of stage i.e.

$$\begin{aligned}
 G_m &= \frac{\delta I_D}{\delta V_{in}} \\
 \sqrt{I_D} &= \sqrt{\frac{K'_n W}{2L}} (V_{in} - I_D R_S - V_t)
 \end{aligned}$$

Neglect body effect for first-order approximation

$$\frac{\delta \sqrt{I_D}}{\delta V_{in}} = \sqrt{\frac{K'_n W}{2L}} \left(1 - R_S \frac{\delta I_D}{\delta V_{in}} \right)$$

$$\frac{\delta \sqrt{I_D}}{\delta V_{in}} = \sqrt{\frac{K'_n W}{2 L}} \left(1 - R_S \frac{\delta I_D}{\delta V_{in}} \right)$$

$$\frac{\delta \sqrt{I_D}}{\delta I_D} \cdot \frac{\delta I_D}{\delta V_{in}} = \sqrt{\frac{K'_n W}{2 L}} \left(1 - R_S \frac{\delta I_D}{\delta I_D} \cdot \frac{\delta I_D}{\delta V_{in}} \right)$$

$$\frac{\delta I_D}{\delta V_{in}} \left(\frac{1}{2 \sqrt{I_D}} + \sqrt{\frac{K'_n W}{2 L}} R_S \right) = \sqrt{\frac{K'_n W}{2 L}}$$

$$\frac{\delta I_D}{\delta V_{in}} = \frac{\sqrt{\frac{K'_n W}{2 L}}}{\frac{1}{2 \sqrt{I_D}} + \sqrt{\frac{K'_n W}{2 L}} R_S} = \frac{\sqrt{2 K'_n \frac{W}{L} I_D}}{1 + \sqrt{2 K'_n \frac{W}{L} I_D} R_S}$$

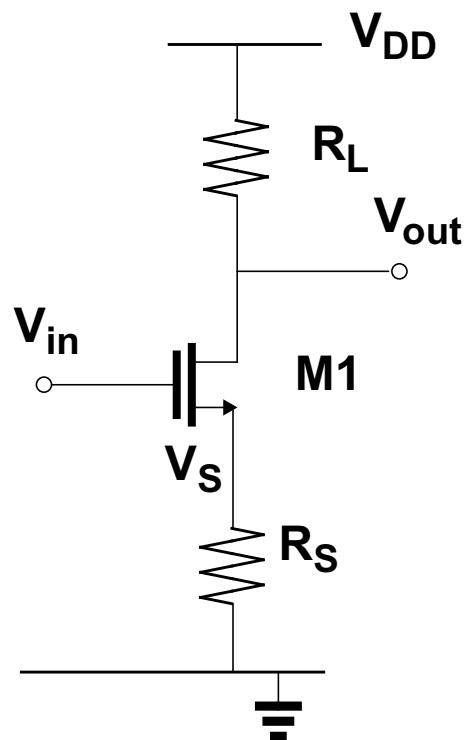
$$G_m = \frac{\delta I_D}{\delta V_{in}} = \frac{g_m}{1 + g_m R_S}$$

If $g_m R_S \gg 1$ then

$$G_m = \frac{\delta I_D}{\delta V_{in}} \approx \frac{1}{R_S}$$

i.e non-linearity removed

4.5.3 CS with res. degeneration. Large-signal behaviour : gain



$$V_{out} = V_{DD} - I_D R_L$$

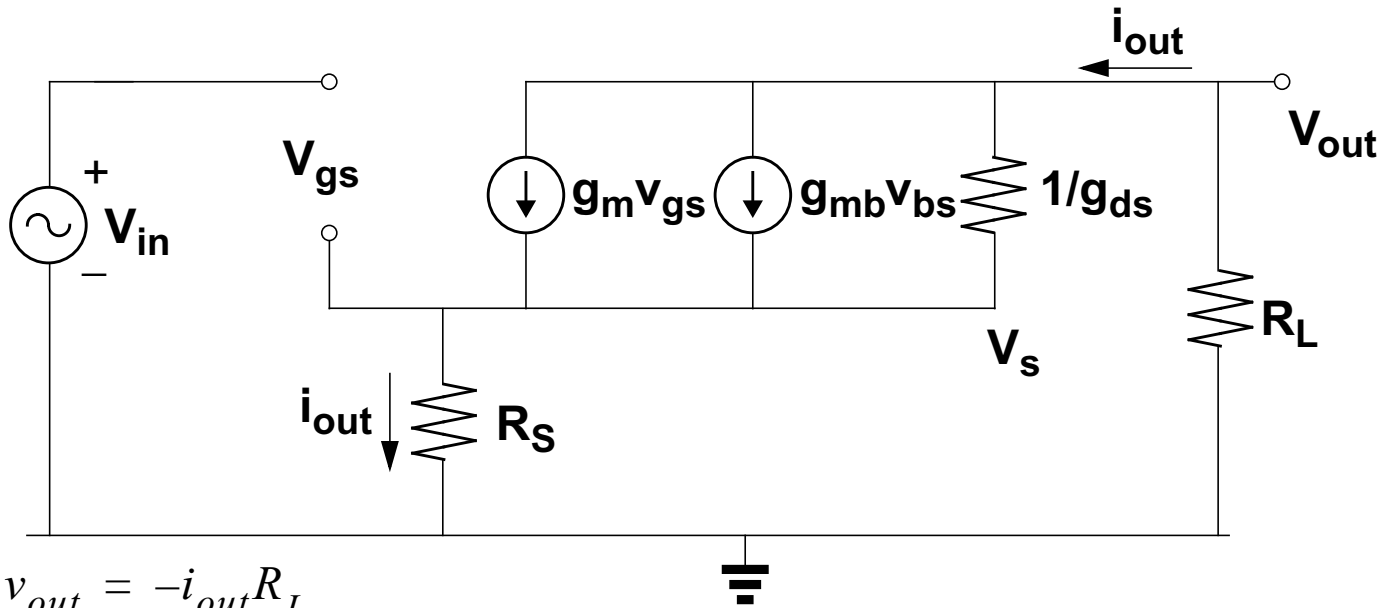
$$Gain = \frac{\delta V_{out}}{\delta V_{in}} = -\frac{g_m R_L}{1 + g_m R_S} = -\frac{R_L}{\frac{1}{g_m} + R_S}$$

If $g_m R_S \gg 1$ then

$$Gain \approx \frac{R_L}{R_S} \quad \text{i.e. linear}$$

Amount of linearisation is dependent on $g_m R_S$

4.5.4 CS with res. degeneration: Small-signal gain



$$v_{out} = -i_{out}R_L$$

$$i_{out} = g_m v_{gs} + g_{mb} v_{bs} + (v_{out} - v_s)g_{ds}$$

$$= g_m(v_{in} - v_s) - g_{mb}v_s + (v_{out} - v_s)g_{ds}$$

$$= g_m v_{in} - (g_m + g_{mb})i_{out}R_S + v_{out}g_{ds} - i_{out}R_Sg_{ds} \quad \begin{matrix} v_{bs} = -v_s \\ v_s = i_{out}R_S \end{matrix}$$

$$= \frac{g_m v_{in} + v_{out}g_{ds}}{1 + (g_m + g_{mb})R_S + g_{ds}R_S}$$

$$v_{out} = -\left(\frac{g_m v_{in} + v_{out}g_{ds}}{1 + (g_m + g_{mb})R_S + g_{ds}R_S}\right)R_L$$

$$v_{out}\left(1 + \frac{g_{ds}R_L}{1 + (g_m + g_{mb})R_S + g_{ds}R_S}\right) = -\frac{g_m v_{in}R_L}{1 + (g_m + g_{mb})R_S + g_{ds}R_S}$$

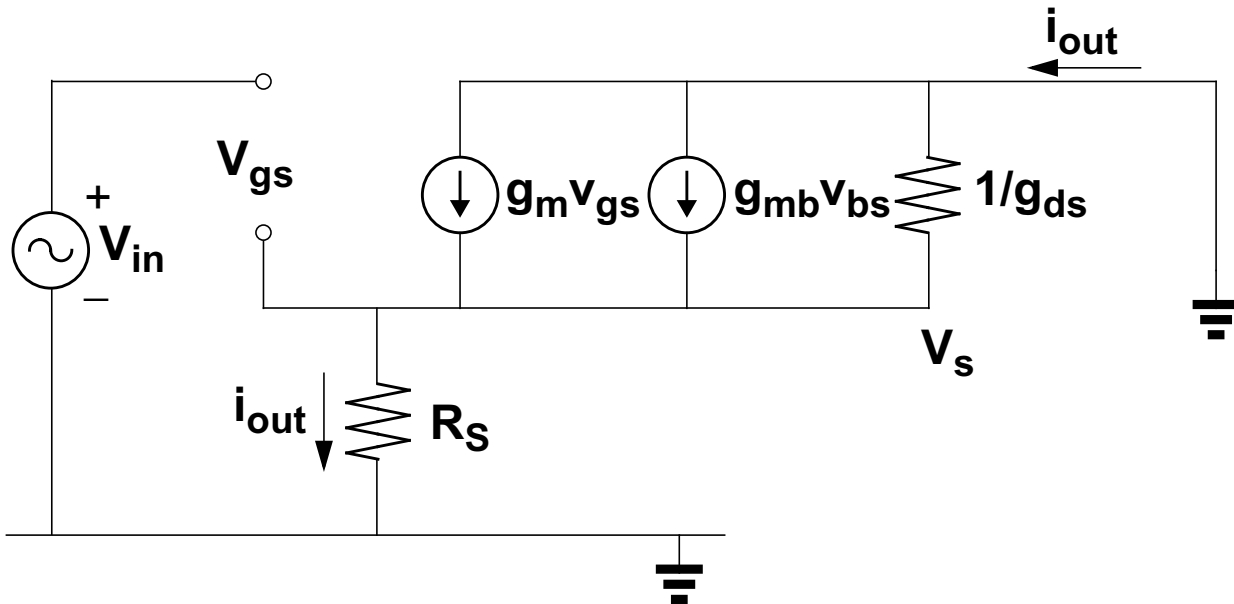
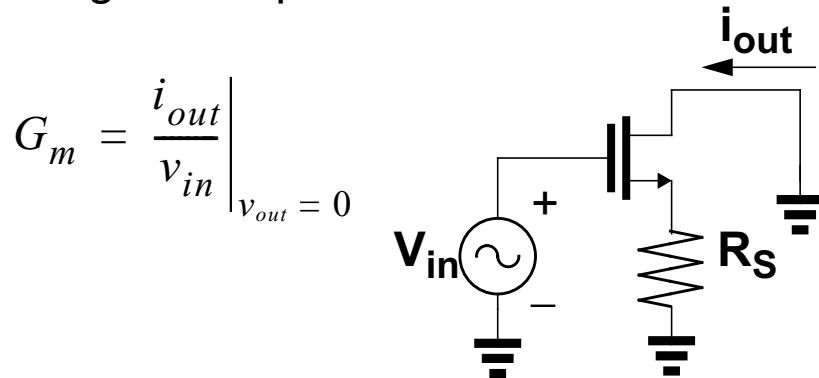
$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_L}{1 + (g_m + g_{mb})R_S + g_{ds}R_S + g_{ds}R_L} \quad \frac{v_{out}}{v_{in}} = \frac{g_m R_L}{A\left(1 + \frac{(g_{ds}R_L)}{A}\right)} = \frac{g_m R_L}{A + g_{ds}R_L}$$

If body effect is ignored, and R_S, R_L same order, this reduces to

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_L}{1 + g_m R_S}$$

4.5.5 CS with res. degeneration: Transconductance G_m

Small-signal **short-circuit** transconductance (G_m) of the stage is the input voltage to output current transfer with output shorted



$$i_{out} = g_m v_{gs} + g_{mb} v_{bs} - v_s g_{ds}$$

$$v_{gs} = v_{in} - v_s$$

$$= g_m (v_{in} - v_s) - g_{mb} v_s - v_s g_{ds}$$

$$v_{bs} = -v_s$$

$$= g_m v_{in} - (g_m + g_{mb}) i_{out} R_S - i_{out} R_S g_{ds}$$

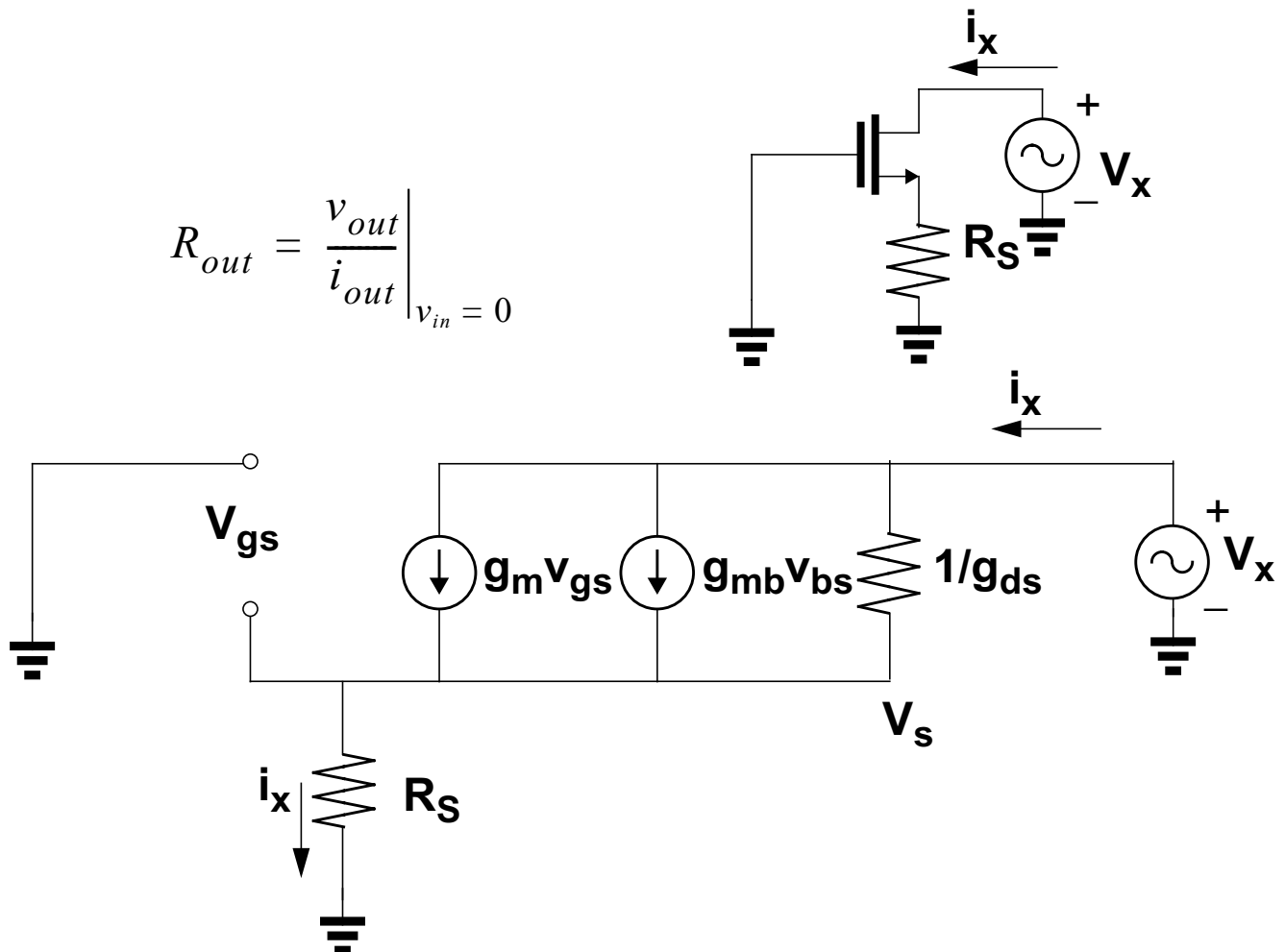
$$v_s = i_{out} R_S$$

$$i_{out} (1 + (g_m + g_{mb}) R_S + g_{ds} R_S) = g_m v_{in}$$

$$G_m = \frac{i_{out}}{v_{in}} = \frac{g_m}{1 + (g_m + g_{mb}) R_S + g_{ds} R_S}$$

4.5.6 CS with res. degeneration: Small-signal output resistance

Output resistance is resistance looking into the output, with the input grounded.



Connect input to ground, apply test voltage at output, derive current

$$\begin{aligned}
 i_x &= g_m v_{gs} + g_{mb} v_{bs} + (v_x - v_s) g_{ds} & v_{bs} &= -v_s \\
 &= -(g_m + g_{mb}) v_s + v_x g_{ds} - v_s g_{ds} & v_{gs} &= -v_s \\
 &= (g_m + g_{mb}) i_x R_S + v_x g_{ds} - i_x R_S g_{ds} & v_s &= i_x R_S
 \end{aligned}$$

$$i_x (1 + (g_m + g_{mb}) R_S + g_{ds} R_S) = v_x g_{ds}$$

$$R_{out} = \frac{v_x}{i_x} = \frac{1}{g_{ds}} (1 + (g_m + g_{mb}) R_S + g_{ds} R_S)$$

CS with resistive degeneration: Output resistance- two insights

1. Effect of degeneration on output resistance of CS stage

$$R_{out} = \frac{1}{g_{ds}}(1 + (g_m + g_{mb})R_S + g_{ds}R_S)$$

Since $g_m + g_{mb} \gg g_{ds}$

$$R_{out} \approx \frac{1}{g_{ds}}(1 + (g_m + g_{mb})R_S)$$

Output resistance of transistor has been increased by factor $1 + (g_m + g_{mb})R_S$

2. Effect of cascoding transistor on R_S

$$R_{out} = \frac{1}{g_{ds}}(1 + (g_m + g_{mb})R_S + g_{ds}R_S)$$

$$R_{out} = \frac{1}{g_{ds}} + \frac{(g_m + g_{mb})}{g_{ds}}R_S + R_S$$

$$R_{out} = \left(1 + \frac{(g_m + g_{mb})}{g_{ds}}\right)R_S + \frac{1}{g_{ds}}$$

$$R_{out} \approx \left(\frac{(g_m + g_{mb})}{g_{ds}}\right)R_S + \frac{1}{g_{ds}}$$

=> output resistance of R_S has been increased by factor $(g_m + g_{mb})/g_{ds}$

Neglecting body effect we can say that output resistance has been increased by intrinsic gain of the transistor

CS with resistive degeneration: Alternative derivation of gain

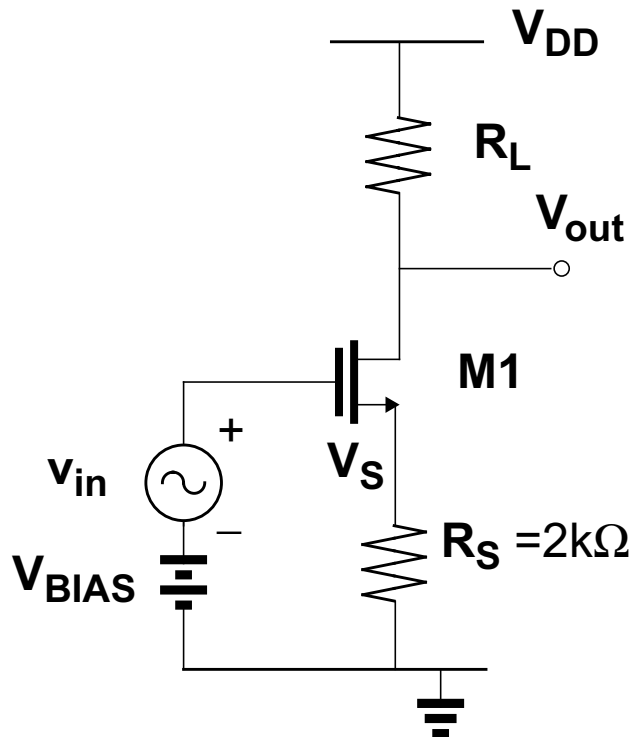
Note on calculation of gain

From study of y-parameters know that gain given by

$$\begin{aligned} A_v &= -G_m(R_{out} \parallel R_L) = \frac{-G_m}{(G_{out} + G_L)} \\ &= -\frac{\frac{g_m}{1 + g_m R_S + g_{ds} R_S}}{\frac{g_{ds}}{(1 + g_m R_S + g_{ds} R_S)} + \frac{1}{R_L}} \\ &= -\frac{\frac{g_m R_L}{1 + g_m R_S + g_{ds} R_S}}{\frac{g_{ds} R_L}{(1 + g_m R_S + g_{ds} R_S)} + 1} \\ &= -\frac{g_m R_L}{1 + g_m R_S + g_{ds} R_S + g_{ds} R_L} \end{aligned}$$

i.e. same gain as calculated directly

Problem: CS stage with resistive degeneration



Assume M1 is in saturation, ignore the body effect, take $g_m \gg g_{ds}$
Assume the stage is biased such that $g_m R_S = 2$
 $V_{\text{DD}} = 3\text{V}$, $V_{\text{BIAS}} = 1.75\text{V}$, $V_t = 1\text{V}$.

- (i) Calculate the value of the stage transconductance G_m
- (ii) What is the largest value of R_L such that M1 is in saturation
(Take $\lambda = 0$ for this calculation)
- (iii) What is the value of the small-signal gain for this R_L ?

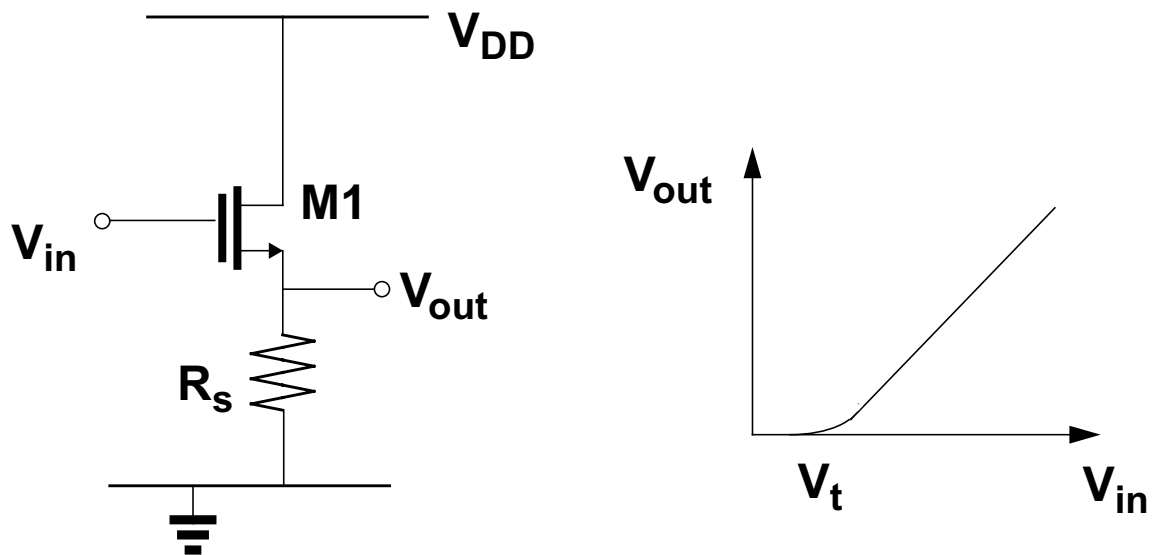
4.6 Source Follower (common-drain) stage

From common source stages we see that to achieve a high gain (in a limited supply voltage) we need a large output impedance.

If however we need to drive a low-impedance load then we need a buffer stage i.e. a stage with a low output impedance.

The source follower can perform this buffer function with a gain approaching unity.

4.6.1 Source Follower - Large-signal behaviour



For $V_{in} = 0$, M1 is off and $V_{out} = 0$

When $V_{in} > V_t$ M1 turns on (in saturation)

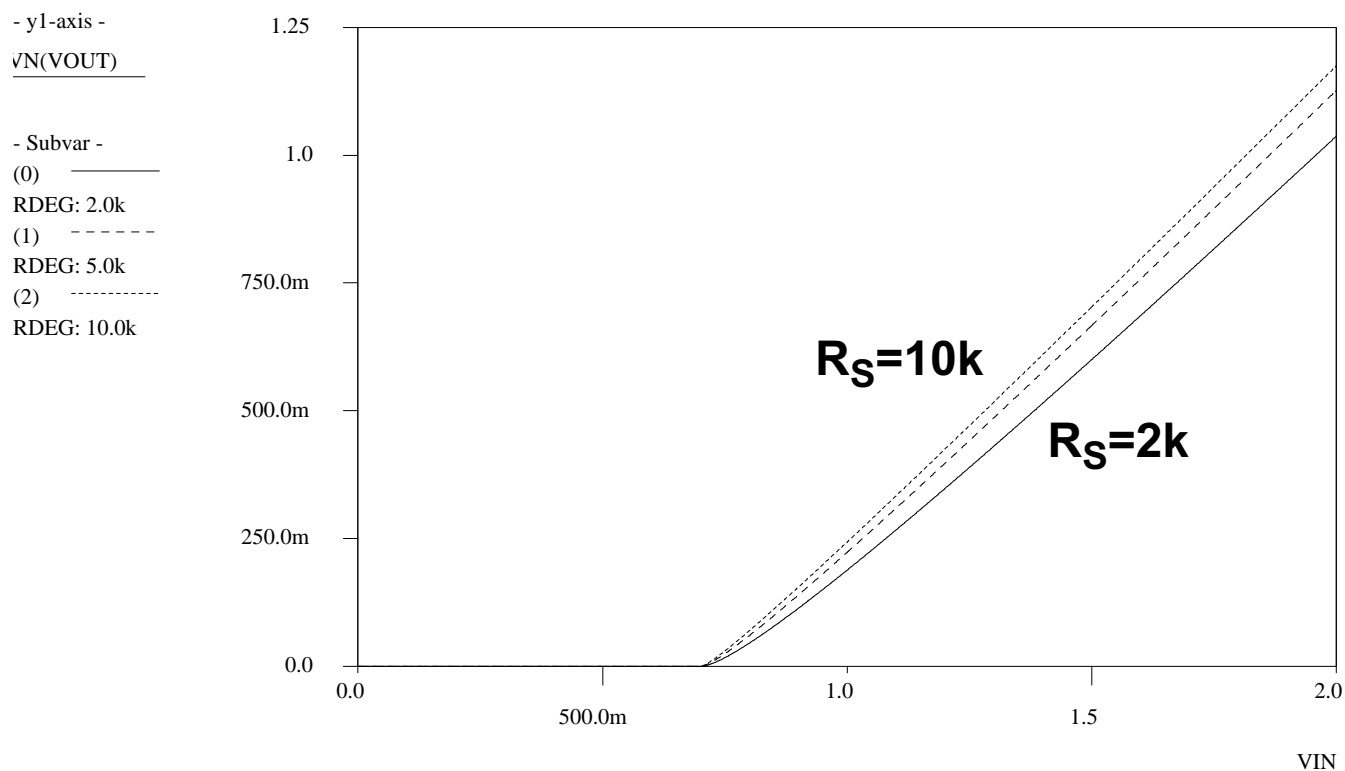
As V_{in} increases further V_{out} follows V_{in} with a voltage difference (levelshift) equal to V_{gs} .

Some non-linearity in V_{out} v. V_{in} characteristic, due to increasing current through M1 as V_{out} increases (due in turn to finite R_s).

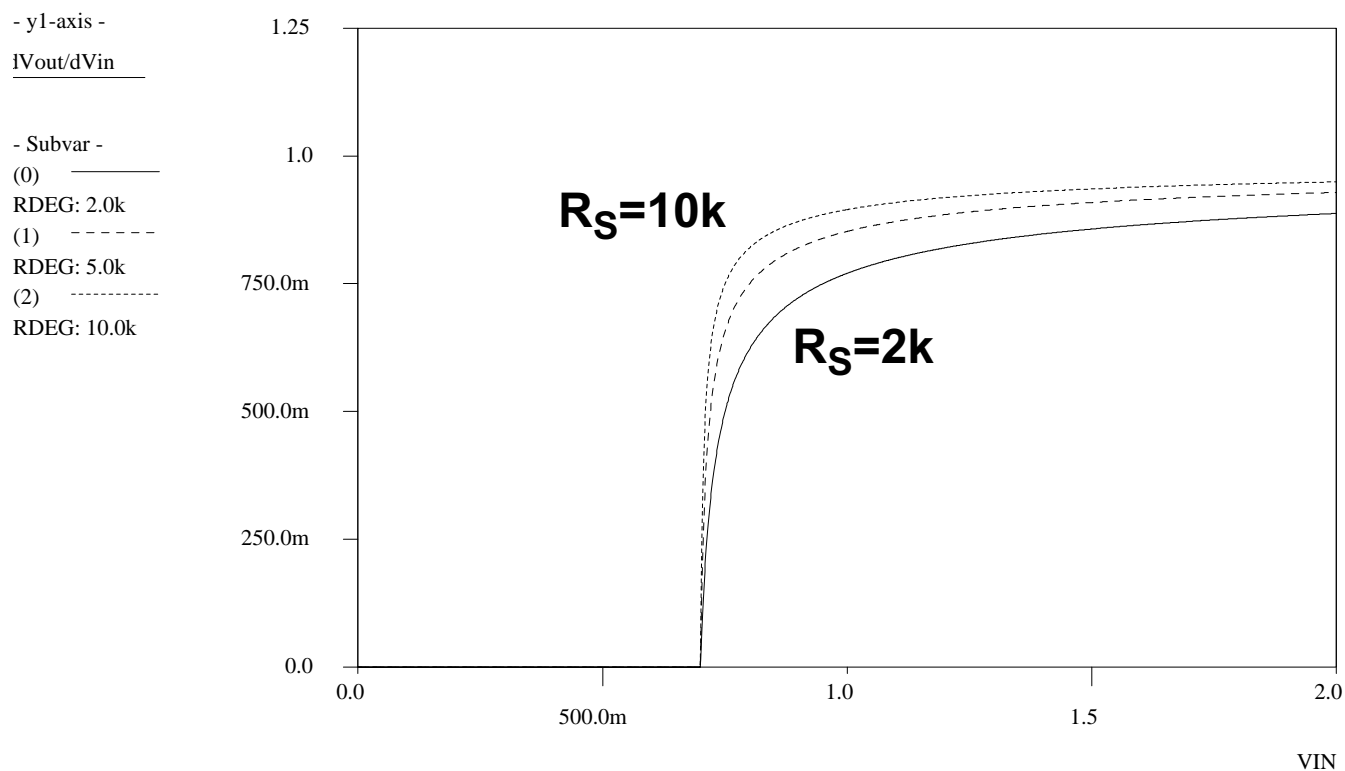
Source-follower is often used as a DC levelshifter. In this application R_s should be as high as possible i.e. use a current source.

Source follower graphical example

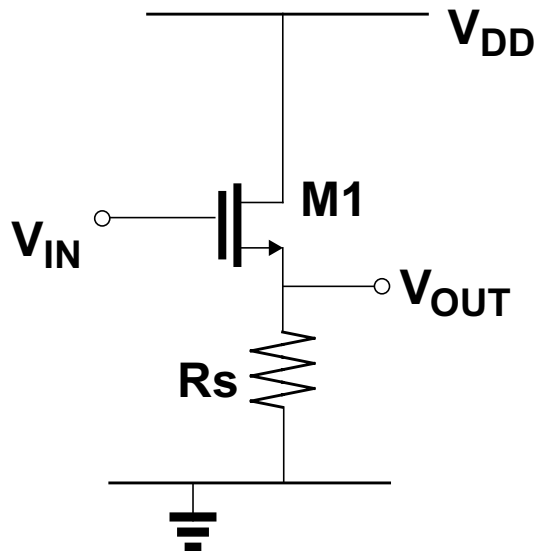
Vout v. Vin



Derivative of Vout v. Vin
(Body effect ignored)



4.6.2 Source follower: large signal behaviour analysis



$$V_{out} = I_D R_S$$

$$= \frac{K'_n W}{2L} (V_{GS} - V_t)^2 R_S = \frac{K'_n W}{2L} (V_{in} - V_{out} - V_t)^2 R_S$$

$$\frac{\delta V_{out}}{\delta V_{in}} = \frac{K'_n W}{2L} 2(V_{in} - V_{out} - V_t) \left(1 - \frac{\delta V_{out}}{\delta V_{in}} - \frac{\delta V_t}{\delta V_{in}} \right) R_S$$

$$\frac{\delta V_t}{\delta V_{in}} = \frac{\delta V_t}{\delta V_{out}} \cdot \frac{\delta V_{out}}{\delta V_{in}} = \eta \frac{\delta V_{out}}{\delta V_{in}}$$

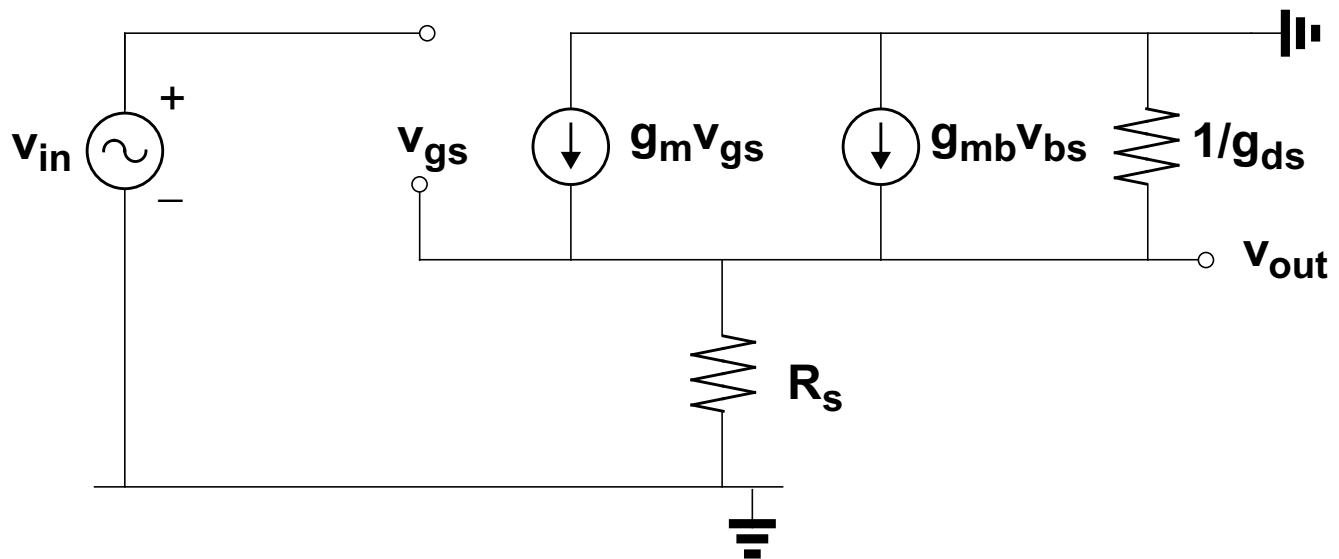
$$\frac{\delta V_{out}}{\delta V_{in}} = g_m \left(1 - \frac{\delta V_{out}}{\delta V_{in}} - \eta \frac{\delta V_{out}}{\delta V_{in}} \right) R_S$$

$$\frac{\delta V_{out}}{\delta V_{in}} = \frac{g_m R_S}{1 + (g_m + g_{mb}) R_S}$$

$$\frac{\delta V_{out}}{\delta V_{in}} = \frac{g_m}{\frac{1}{R_S} + g_m + g_{mb}}$$

4.6.3 Source Follower - Small-signal behaviour (gain)

Small-signal gain



KCL at output node

$$\frac{v_{out}}{R_s} - g_m v_{gs} - g_{mb} v_{bs} + v_{out} g_{ds} = 0$$

$$\frac{v_{out}}{R_s} - g_m (v_{in} - v_{out}) + g_{mb} v_{out} + v_{out} g_{ds} = 0$$

$$v_{out} \left(\frac{1}{R_s} + g_m + g_{mb} + g_{ds} \right) = g_m v_{in}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_m}{\frac{1}{R_s} + g_m + g_{mb} + g_{ds}}$$

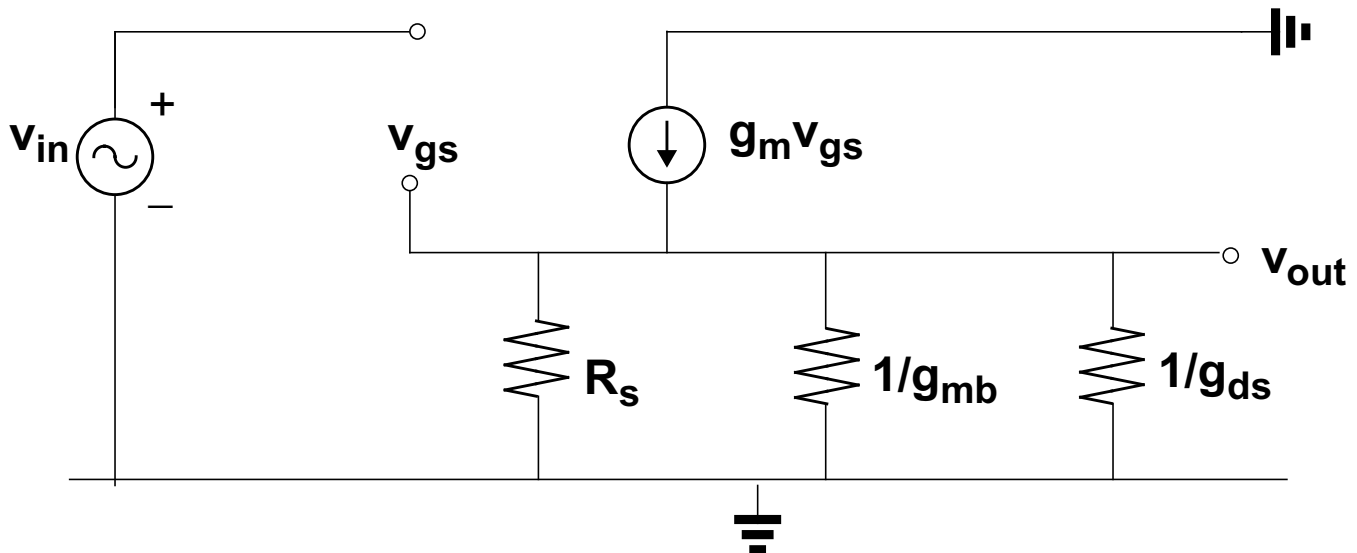
Note: Gain of source follower is less than one due to

1. body effect (significant if present as $g_{mb} \sim 0.3xg_m$)
2. Source resistance (significant unless $g_m \gg 1/R_s$)
3. output conductance (not significant as $g_m \gg g_{ds}$)

Source Follower: Alternative derivation of gain

Note: $v_{bs} = -v_{out} \Rightarrow$ current source $g_{mb}v_{bs}$ can be replaced by a resistor $1/g_{mb}$

Simplified small-signal equivalent circuit



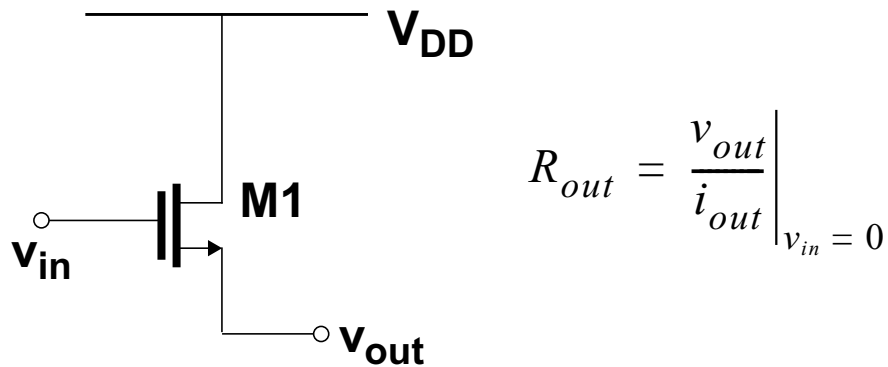
$$\frac{v_{out}}{R_s} + v_{out}g_{mb} + v_{out}g_{ds} = g_mv_{gs}$$

$$g_m(v_{in} - v_{out}) = v_{out}\left(\frac{1}{R_s} + g_{mb} + g_{ds}\right)$$

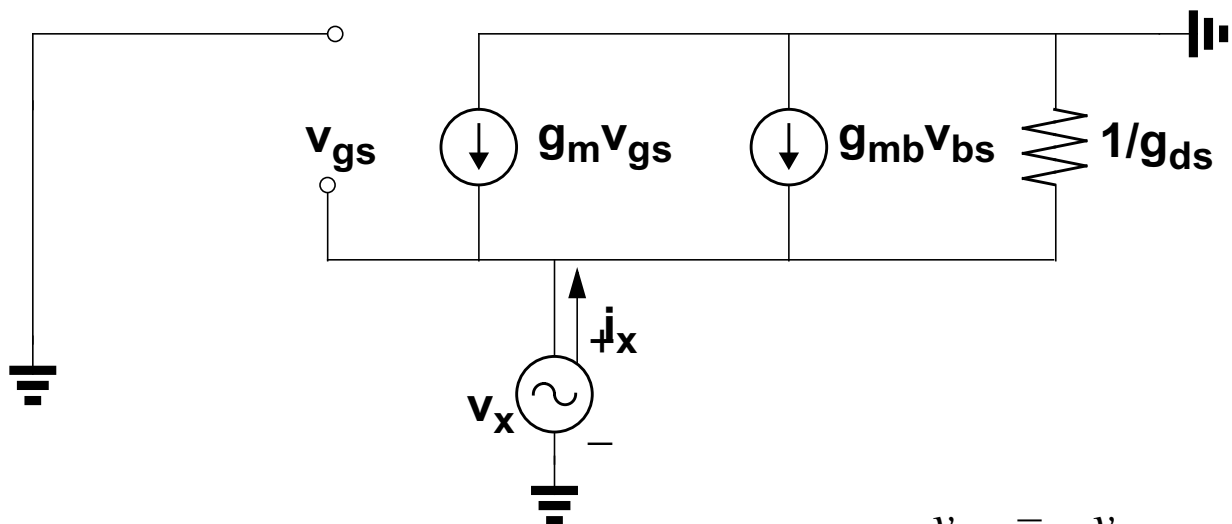
$$\frac{v_{out}}{v_{in}} = \frac{g_m}{g_m + g_{mb} + g_{ds} + \frac{1}{R_s}}$$

Note: $v_{gs} = v_{in} - v_{out}$

4.6.4 Source follower - output resistance R_{out}



Connect input to ground, apply test voltage at output, derive current



$$v_{gs} = -v_x$$

$$v_{bs} = -v_x$$

$$i_x = -g_m v_{gs} - g_{mb} v_{bs} + g_{ds} v_x$$

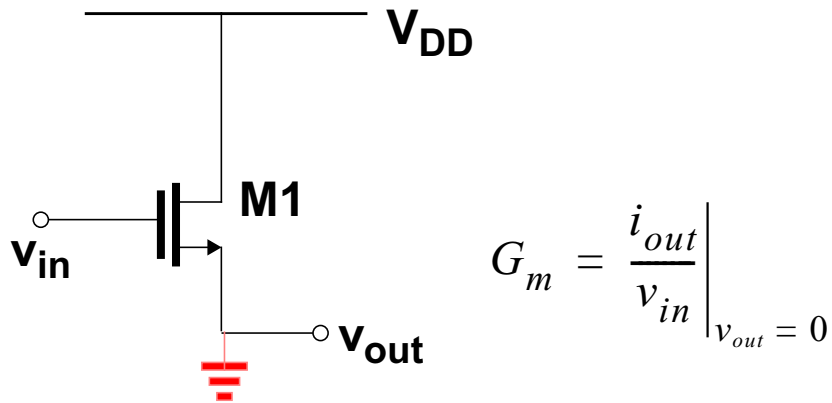
$$= g_m v_x + g_{mb} v_x + g_{ds} v_x$$

$$R_{out} \equiv \frac{v_x}{i_x} = \frac{1}{g_m + g_{mb} + g_{ds}} \approx \frac{1}{g_m + g_{mb}}$$

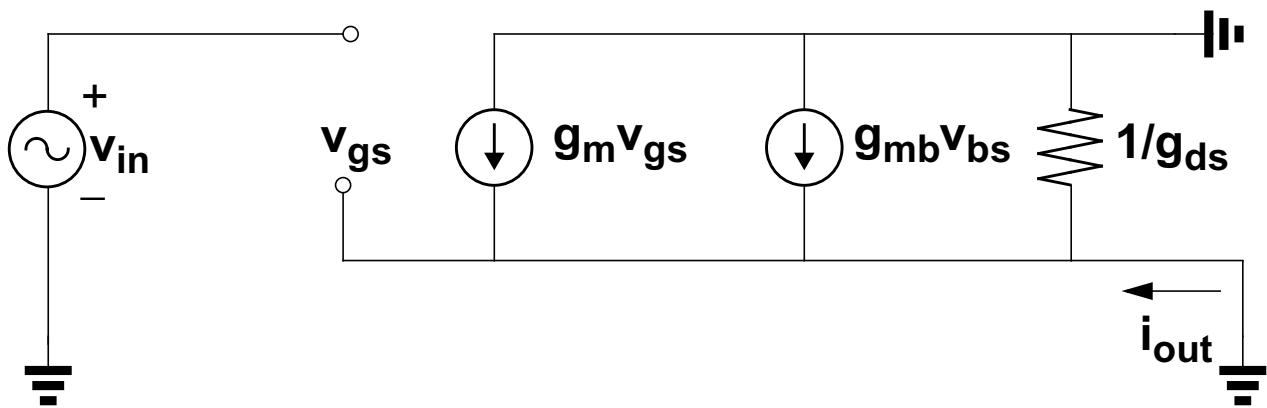
Alternatively: recognise current sources $g_m v_{gs}$, $g_{mb} v_{bs}$ can be replaced by resistors $1/g_m$, $1/g_{mb}$ respectively and write result directly

Note: this is a relatively low output resistance (compared to $1/g_{ds}$)

4.6.5 Source follower - Transconductance G_m



Small-signal equivalent circuit



Note: $v_{bs}=0$, no voltage across $1/g_{ds} \Rightarrow$ no current

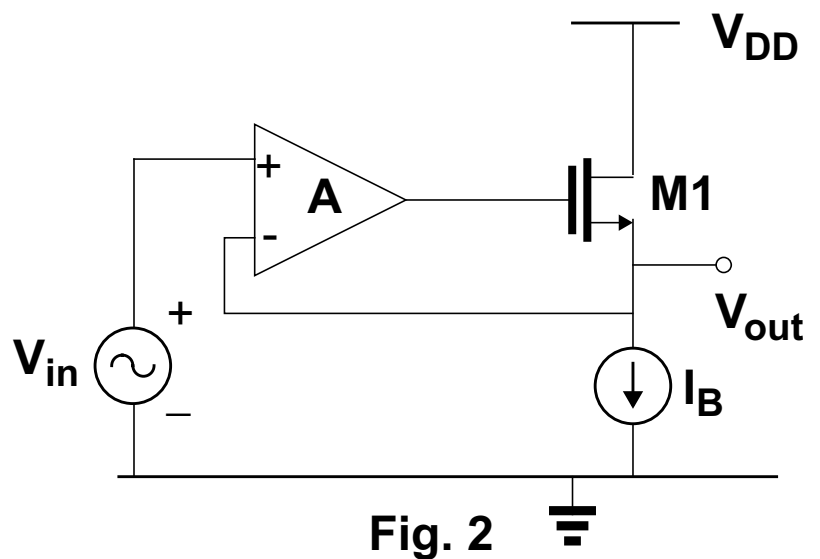
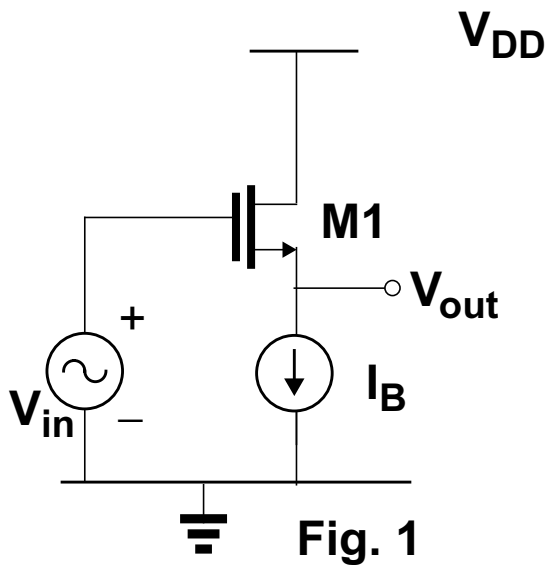
$$i_{out} = -g_m v_{gs} = -g_m v_{in}$$

$$G_m \equiv \frac{i_{out}}{v_{in}} = -g_m$$

Small-signal gain

$$\begin{aligned} A_v &= -G_m (R_{out} \parallel R_S) = \frac{-G_m}{(G_{out} + G_S)} \\ &= \frac{g_m}{g_m + g_{mb} + g_{ds} + \frac{1}{R_S}} \end{aligned}$$

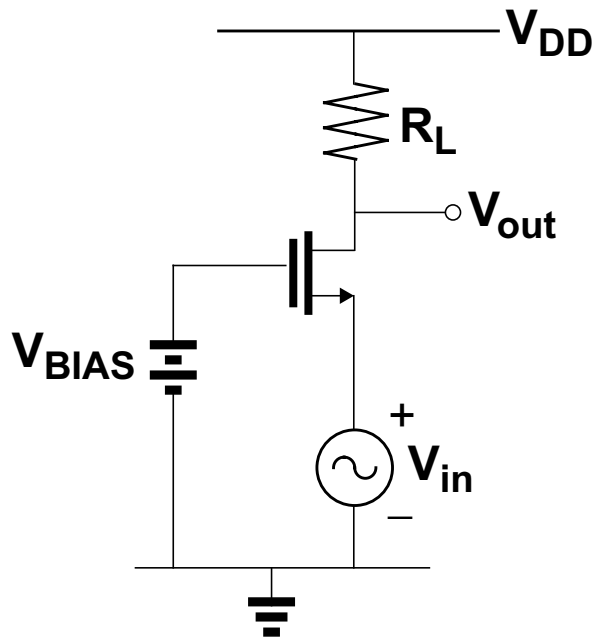
Problem - Source follower



Assume M1 is in saturation, ignore the body effect

- (i) Draw the small signal model.
 - (ii) What is the small-signal low-frequency gain of the circuit in terms of g_m and g_{ds} ?
 - (iii) If $I_B = 200\mu A$, $V_{GS} = 1.5V$, $V_t = 1V$, calculate the small-signal low-frequency gain. Take $\lambda = 0.02V^{-1}$
 - (iv) What is the conductance/resistance at the output node?
 - (v) In Fig.2 an ideal amplifier has been added to reduce the output resistance. Draw the small signal model.
 - (vi) What is the impedance at the output node in terms of A , g_m and g_{ds} ?
- (To simplify the analysis assume $g_m \gg g_{ds}$)

4.7 Common Gate stage



Also possible to input a signal at the source with the gate biased with a dc voltage and take the output signal at the drain
 - common gate
 Sometimes used for impedance definition (termination).

Large-signal behaviour: gain

$$V_{out} = V_{DD} - I_D R_L$$

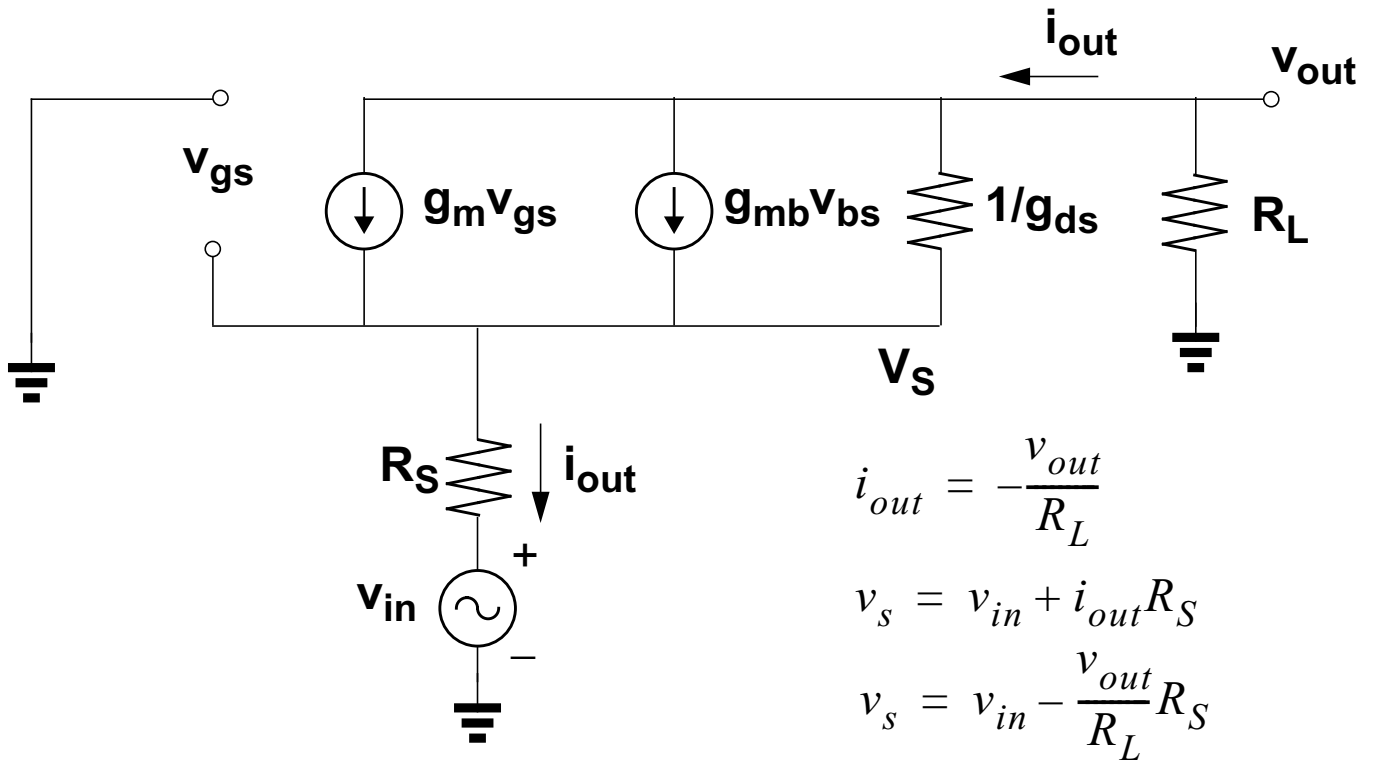
$$V_{out} = V_{DD} - \frac{K'_n W}{2 L} (V_{BIAS} - V_{in} - V_t)^2 R_L$$

$$\frac{\delta V_{out}}{\delta V_{in}} = -\frac{K'_n W}{2 L} 2(V_{GS} - V_{in} - V_t) \left(-1 - \frac{\delta V_t}{\delta V_{in}} \right) R_L$$

$$\frac{\delta V_t}{\delta V_{in}} = \frac{\delta V_t}{\delta V_{SB}} = \eta$$

$$\frac{\delta V_{out}}{\delta V_{in}} = g_m (1 + \eta) R_L \equiv (g_m + g_{mb}) R_L$$

4.7.1 Common gate small-signal voltage gain



$$-\frac{v_{out}}{R_L} = g_m v_{gs} + g_{mb} v_{bs} + (v_{out} - v_s) g_{ds}$$

$$-\frac{v_{out}}{R_L} = -(g_m + g_{mb}) v_s + v_{out} g_{ds} - v_s g_{ds}$$

$$-\frac{v_{out}}{R_L} = -(g_m + g_{mb}) \left(v_{in} - \frac{v_{out}}{R_L} R_S \right) + v_{out} g_{ds} - \left(v_{in} - \frac{v_{out}}{R_L} R_S \right) g_{ds}$$

$$-\frac{v_{out}}{R_L} = -(g_m + g_{mb} + g_{ds}) v_{in} + \left((g_m + g_{mb}) \frac{R_S}{R_L} + g_{ds} + \frac{R_S}{R_L} g_{ds} \right) v_{out}$$

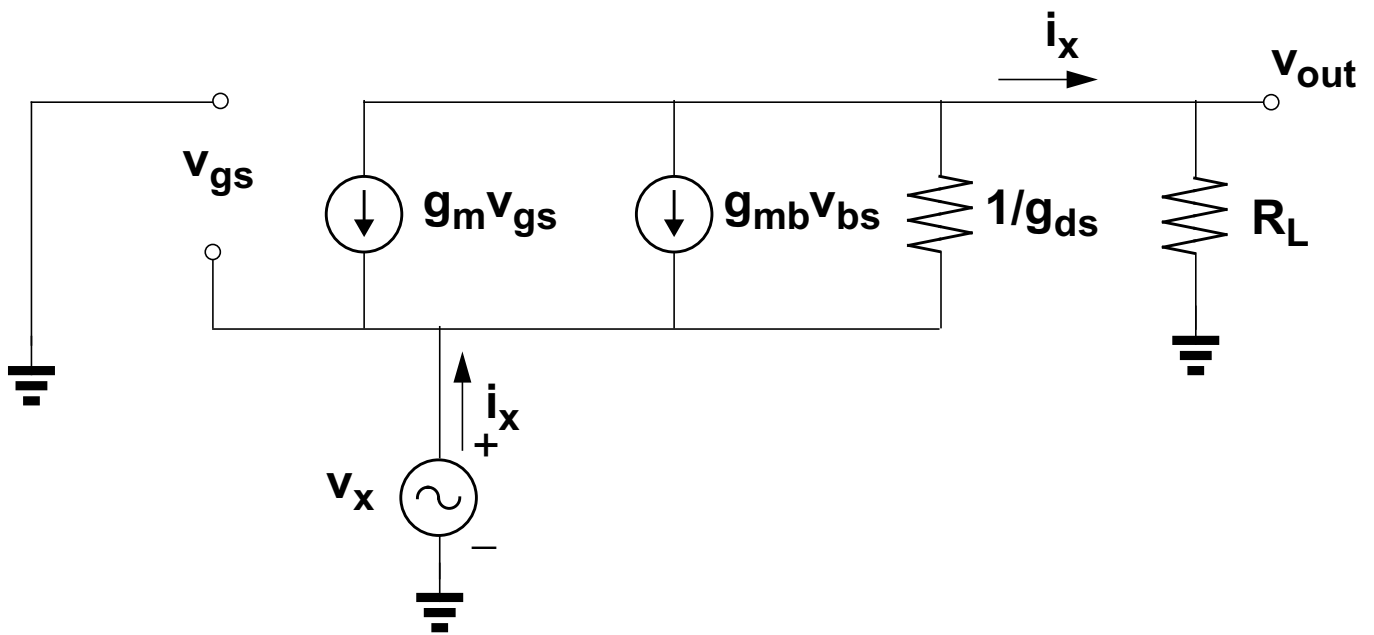
$$\frac{v_{out}}{v_{in}} = \frac{(g_m + g_{mb} + g_{ds})}{\frac{1}{R_L} + (g_m + g_{mb}) \frac{R_S}{R_L} + g_{ds} + \frac{R_S}{R_L} g_{ds}}$$

Note: this reduces to

$$\frac{v_{out}}{v_{in}} = \frac{(g_m + g_{mb} + g_{ds}) R_L}{1 + (g_m + g_{mb}) R_S + g_{ds} R_L + g_{ds} R_S}$$

$$\frac{v_{out}}{v_{in}} \equiv (g_m + g_{mb}) R_L$$

4.7.2 Common gate - input resistance



Note: input resistance not infinite as in previous stages.

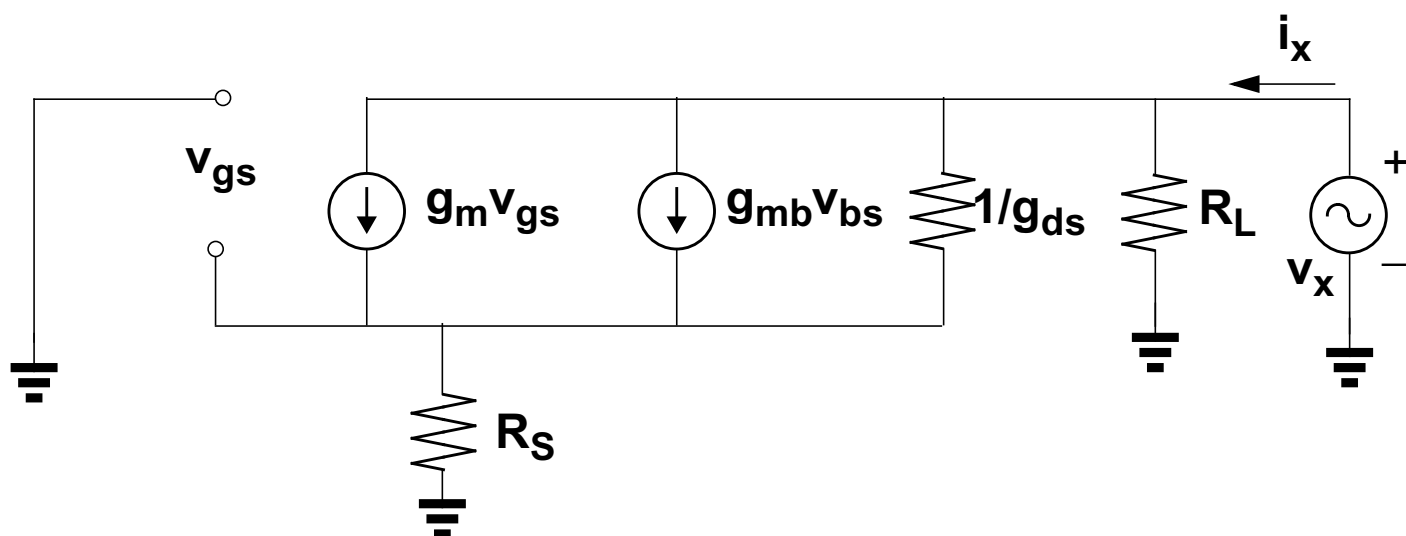
$$i_x = (v_x - v_{out})g_{ds} - g_mv_{gs} - g_{mb}v_{bs}$$

$$i_x = (v_x - i_x R_L)g_{ds} + g_mv_x + g_{mb}v_x$$

$$\frac{v_x}{i_x} = \frac{1 + g_{ds}R_L}{g_m + g_{mb} + g_{ds}} \approx \frac{1}{g_m + g_{mb}} + \frac{R_L}{\frac{g_m + g_{mb}}{g_{ds}}}$$

If R_L is in the order of $1/g_{ds}$, common gate stage reduces it to order $1/g_m$
 => application in impedance matching

4.7.3 Common gate - output resistance



Note similarity with CS stage with resistive degeneration

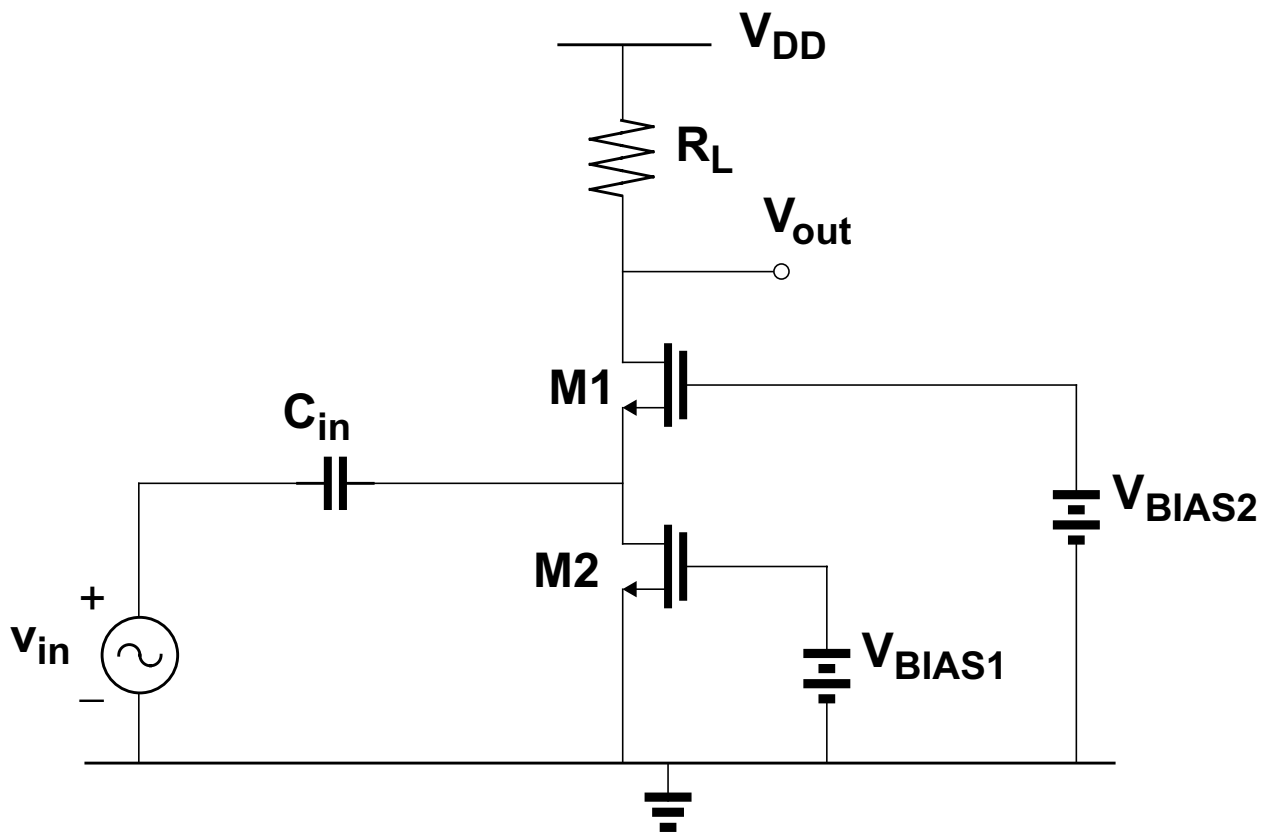
$$R_{out} = \frac{1}{g_{ds}} (1 + (g_m + g_{mb})R_S + g_{ds}R_S) \parallel R_L$$

see derivation P109 *Alternatively*

$$R_{out} \approx \frac{1}{g_{ds}} (1 + (g_m + g_{mb})R_S) \parallel R_L$$

$$R_{out} \approx \left(\left(\frac{g_m + g_{mb}}{g_{ds}} \right) R_S \right) \parallel R_L$$

Problem: Common-gate stage



$V_{DD}=3.3V$, $V_t=0.6V$, $I_{D1}=1mA$

It is required for an input stage to a system to have an input resistance of $200\Omega \pm 10\%$ and a gain of about 20dB.

Assume the input signal couples through C_{in} without loss.

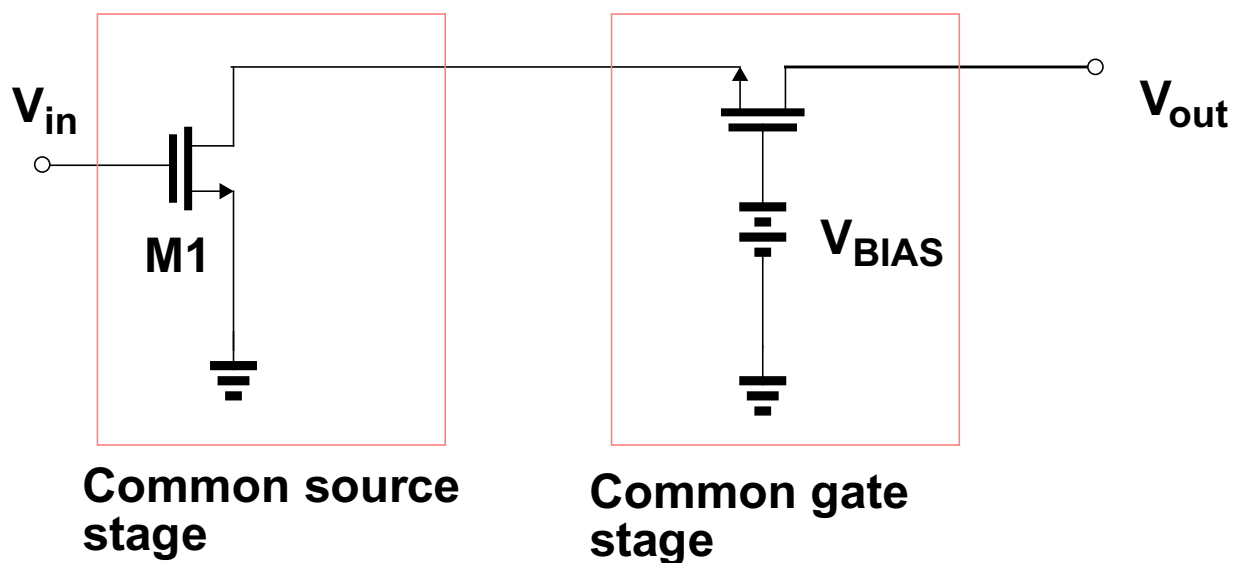
- (i) Suggest values for g_{m1} and R_L to meet this specification.
- (ii) Assuming M1 and M2 have the same W/L and M2 is just in saturation, what is the range of allowed voltages for V_{BIAS2} ?

4.8 Cascode Stage

Want more gain - use cascode stage

Can be seen as a cascade of a common source and a common gate stage

We can surmise that transconductance G_m will be similar to common source stage, but that output impedance R_{out} will be much greater.



4.8.1 Cascode Stage: Biasing requirements

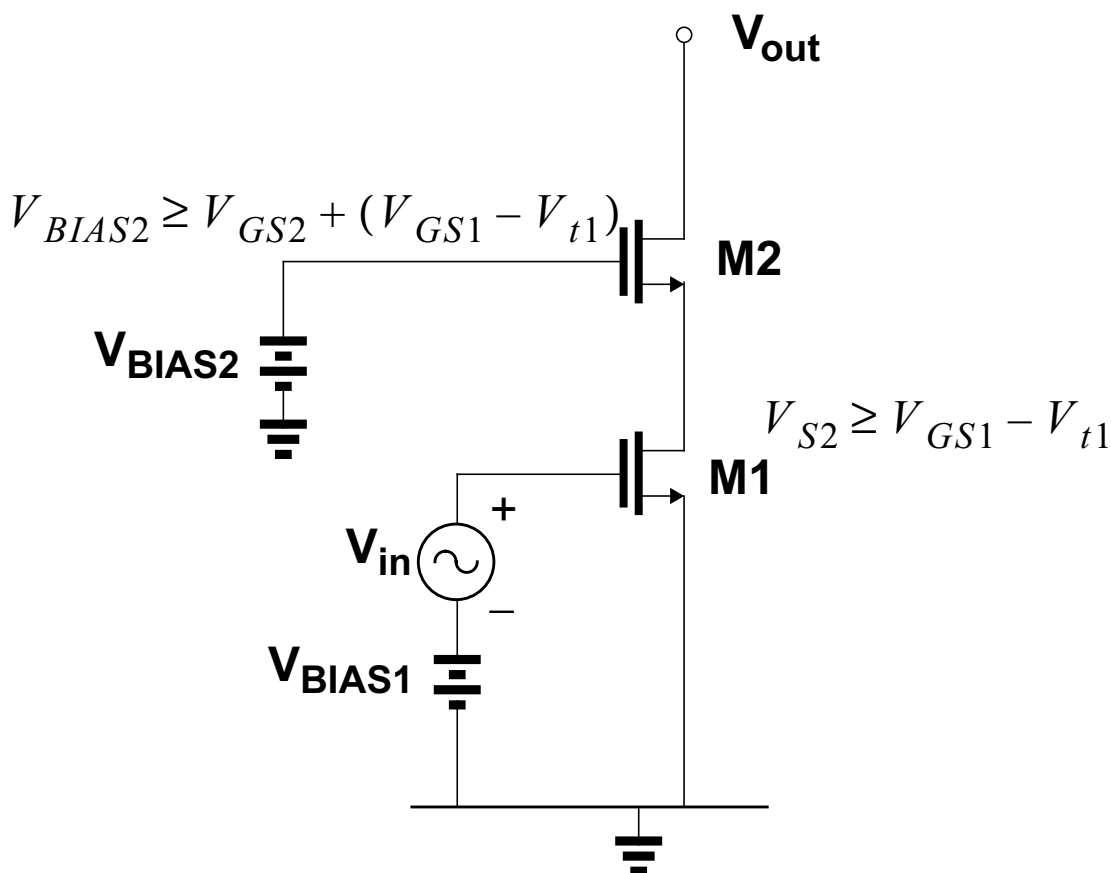
For high gain both transistors need to be in saturation:

$$V_{OUT} \geq (V_{BIAS2} - V_{GS2}) + (V_{GS2} - V_{t2})$$

$$V_{OUT} \geq V_{BIAS2} - V_{t2}$$

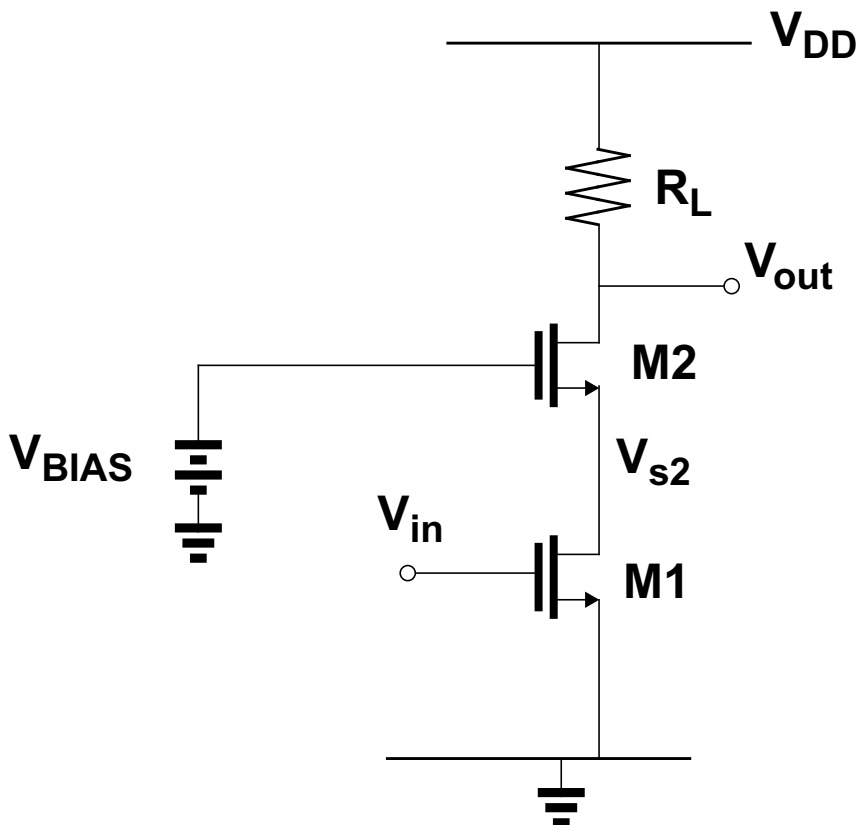
If V_{BIAS2} is such that M1 is just in saturation:

$$V_{OUT} \geq (V_{GS1} - V_{t1}) + (V_{GS2} - V_{t2})$$



Minimum voltage at output = sum of overdrive voltages of both transistors

4.8.2 Cascode Stage: Large signal behaviour



Assume V_{BIAS} is sufficiently large (i.e. will support conditions on previous page)

$V_{in} = 0$:

V_{out} charged to V_{DD} ,

M2 is off but V_{s2} is charged to $V_{BIAS} - V_t$ (neglecting subthreshold conduction)

Increase V_{in} :

When $V_{in} > V_t$: M1 turns on in saturation , current flows

M2 turns on in saturation

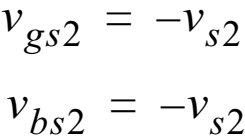
V_{GS2} increases, V_{s2} and V_{out} fall.

V_{in} increases further

V_{s2} and V_{out} will decrease further

M1 and M2 will at some stage go out of saturation.

The order depends on the bias conditions.



KCL at output node (drain of M2):

$$i_{out} = g_{m2}v_{gs2} + g_{mb2}v_{bs2} - v_{s2}g_{ds2}$$

$$i_{out} = -g_{m2}v_{s2} - g_{mb2}v_{s2} - v_{s2}g_{ds2}$$

$$v_{s2} = -\frac{i_{out}}{g_{m2} + g_{mb2} + g_{ds2}}$$

KCL at source of M2:

$$i_{out} = g_{m1}v_{in} + v_{s2}g_{ds1}$$

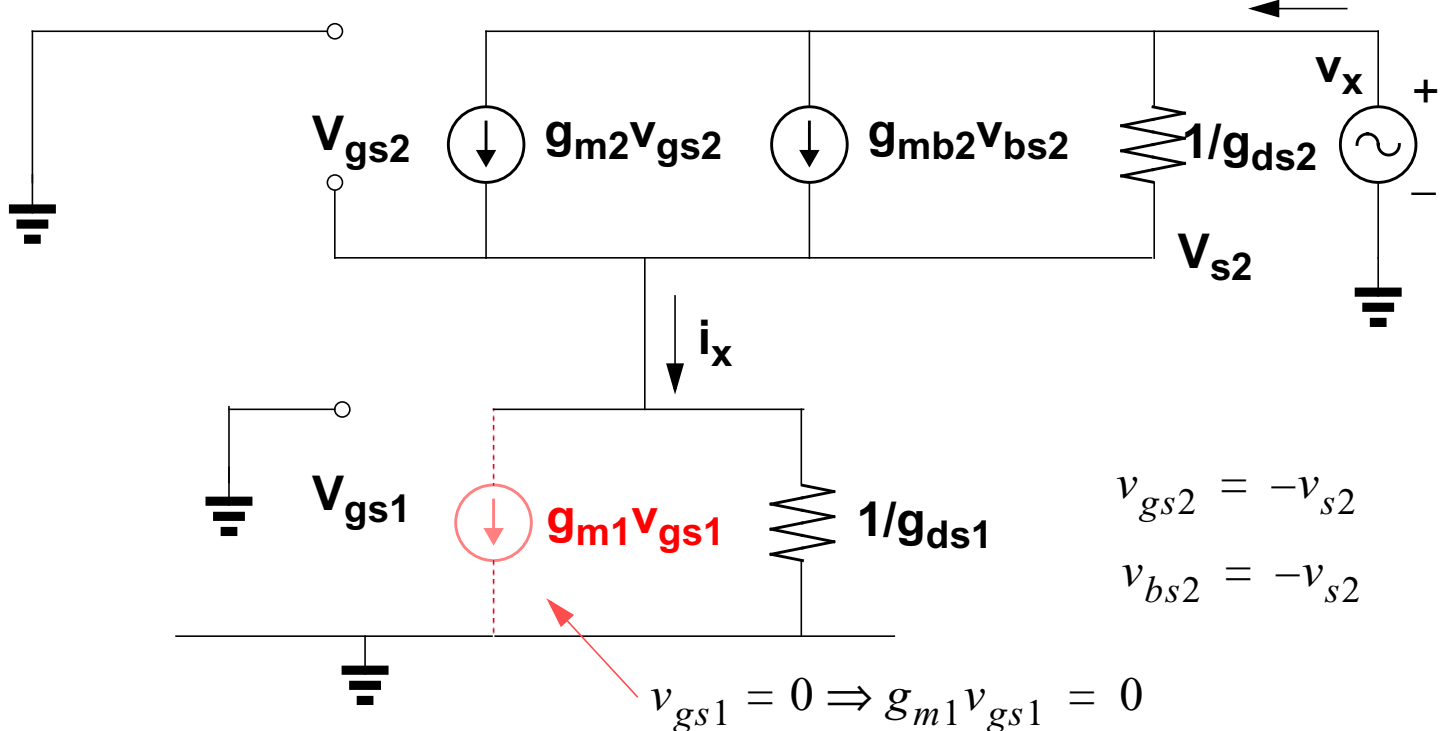
$$i_{out} = g_{m1}v_{in} - \frac{i_{out}}{g_{m2} + g_{mb2} + g_{ds2}}g_{ds1}$$

$$G_m = \frac{i_{out}}{v_{in}} = \frac{g_{m1}}{1 + \frac{g_{ds1}}{g_{m2} + g_{mb2} + g_{ds2}}} \approx g_{m1}$$

=> G_m is slightly less than g_{m1} due to the current division at the drain of M1

4.8.4 Cascode: Output Resistance R_{out}

Short input, apply test voltage at output:, measure current i_x



$$\dot{i}_x = g_{m2}v_{gs2} + g_{mb2}v_{bs2} + (v_x - v_{s2})g_{ds2}$$

$$\dot{i}_x = -g_{m2}v_{s2} - g_{mb2}v_{s2} + v_x g_{ds2} - v_{s2} g_{ds2}$$

Since $v_{s2} = \frac{i_x}{g_{ds1}}$

$$i_x = -(g_{m2} + g_{mb2}) \frac{i_x}{g_{ds1}} + v_x g_{ds2} - \frac{i_x}{g_{ds1}} g_{ds2}$$

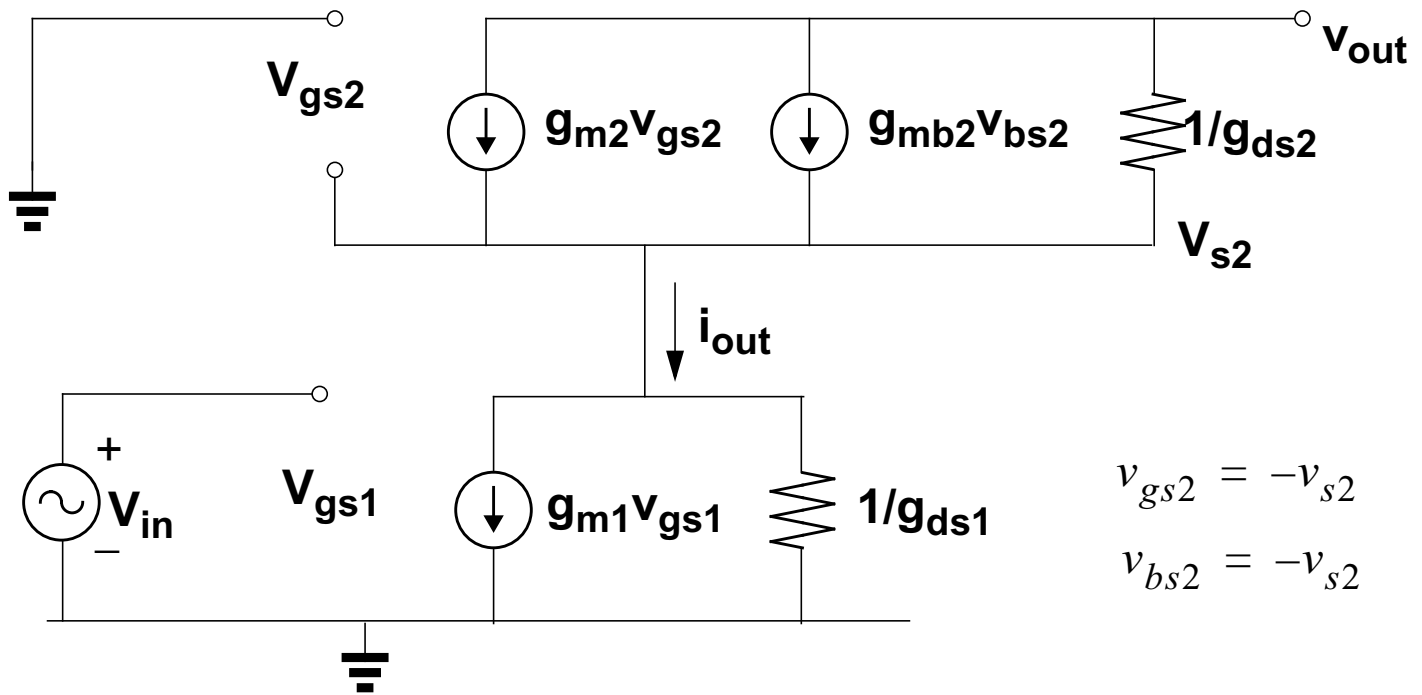
$$r_{out} = \frac{v_x}{i_x} = \frac{1}{g_{ds2}} \left(1 + \frac{g_{m2} + g_{mb2}}{g_{ds1}} + \frac{g_{ds2}}{g_{ds1}} \right) \approx \frac{1}{g_{ds1}} \left(\frac{g_{m2} + g_{mb2}}{g_{ds2}} \right)$$

=> Output resistance has been increased by $(g_{m2} + g_{mb2})/g_{ds2}$

Neglecting body effect we can say output resistance is increased by g_{m2}/g_{ds2} i.e. by the intrinsic gain of the cascode transistor.

Alternatively output conductance is reduced by g_{m2}/g_{ds2}

4.8.5 Cascode: Small-signal voltage gain



KCL at output node (drain of M2):

$$(v_{out} - v_{s2})g_{ds2} + g_{m2}v_{gs2} + g_{mb2}v_{bs2} = 0$$

$$(v_{out} - v_{s2})g_{ds2} - (g_{m2} + g_{mb2})v_{s2} = 0$$

KCL at source of M2:

$$(v_{out} - v_{s2})g_{ds2} + g_{m2}v_{gs2} + g_{mb2}v_{bs2} = g_{m1}v_{in} + v_{s2}g_{ds1}$$

$$0 = g_{m1}v_{in} + v_{s2}g_{ds1}$$

$$v_{s2} = -\frac{g_{m1}}{g_{ds1}} v_{in}$$

$$v_{out}g_{ds2} + \frac{g_{m1}}{g_{ds1}}g_{ds2}v_{in} + (g_{m2} + g_{mb2})\left(\frac{g_{m1}}{g_{ds1}}v_{in}\right) = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{1}{g_{ds2}} \left(\frac{g_{m1}}{g_{ds1}} g_{ds2} + (g_{m2} + g_{mb2}) \frac{g_{m1}}{g_{ds1}} \right)$$

$$\frac{v_{out}}{v_{in}} = -\left(\frac{g_{m1}}{g_{ds1}} + \frac{(g_{m2} + g_{mb2})}{g_{ds2}} \frac{g_{m1}}{g_{ds1}}\right) \approx -\frac{(g_{m2} + g_{mb2})}{g_{ds2}} \frac{g_{m1}}{g_{ds1}}$$

Neglecting body effect we can say gain is increased by g_{m2}/g_{ds2} i.e. by the intrinsic gain of the cascode transistor.

Intrinsic gain of cascode stage is product of gains of 2 transistors.

Alternative derivation of gain.

$$\text{Gain} = -G_m R_{out}$$

$$-G_m R_{out} = - \left(\frac{g_{m1}}{1 + \frac{g_{ds1}}{g_{m2} + g_{mb2} + g_{ds2}}} \cdot \frac{1}{g_{ds2}} \left(1 + \frac{g_{m2} + g_{mb2}}{g_{ds1}} + \frac{g_{ds2}}{g_{ds1}} \right) \right)$$

$$= - \left(\frac{g_{m1}}{1 + \frac{g_{ds1}}{g_{m2} + g_{mb2} + g_{ds2}}} \cdot \left(\frac{1}{g_{ds2}} + \frac{g_{m2} + g_{mb2}}{g_{ds2} g_{ds1}} + \frac{1}{g_{ds1}} \right) \right)$$

$$= - \left(\frac{g_{m1}}{\frac{g_{m2} + g_{mb2} + g_{ds2} + g_{ds1}}{g_{m2} + g_{mb2} + g_{ds2}}} \cdot \left(\frac{g_{m2} + g_{mb2} + g_{ds2} + g_{ds1}}{g_{ds2} g_{ds1}} \right) \right)$$

$$= - \frac{g_{m1} (g_{m2} + g_{mb2} + g_{ds2})}{g_{ds2} g_{ds1}}$$

$$= - \left(\frac{g_{m1}}{g_{ds1}} + \frac{(g_{m2} + g_{mb2}) g_{m1}}{g_{ds2} g_{ds1}} \right)$$

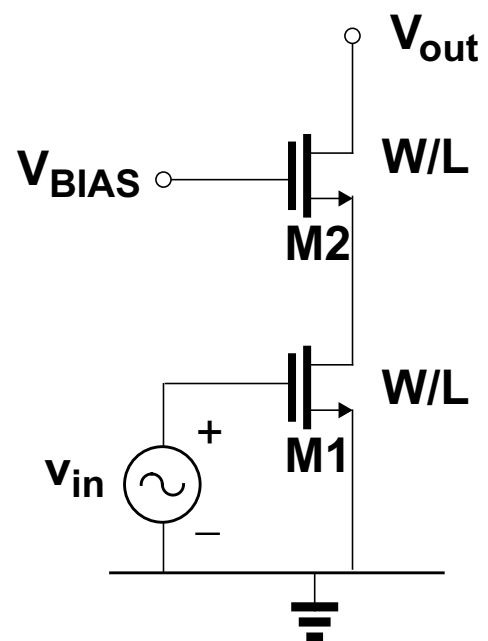
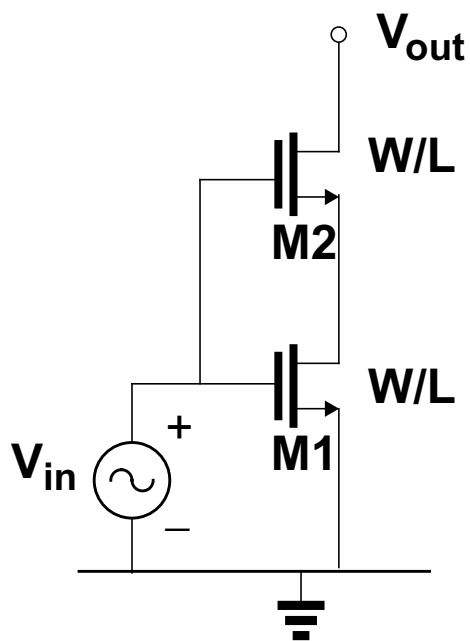
i.e same as calculated directly

Problem - Cascode stage output resistance, voltage headroom:

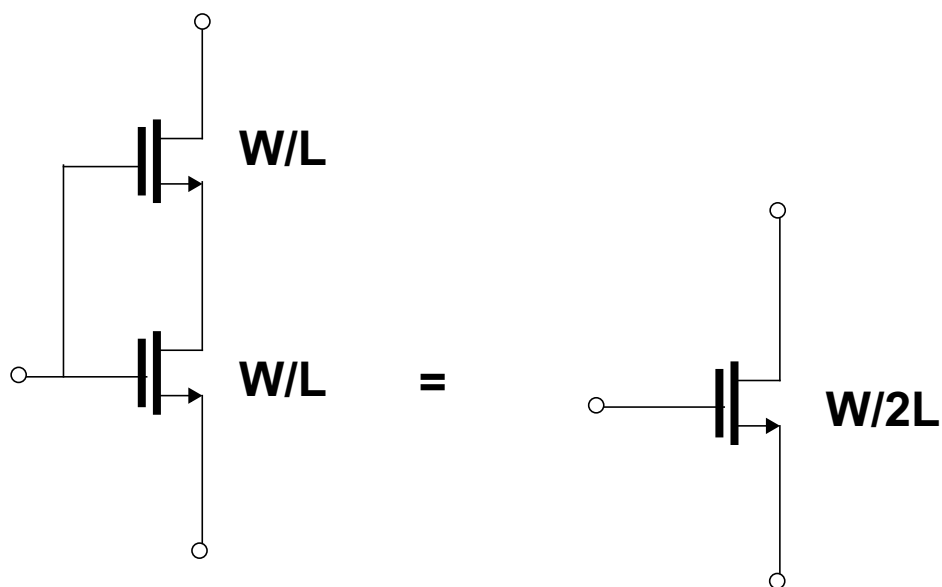
Compare the two stages shown in terms of

- (i) output resistance
- (ii) gain
- (iii) voltage headroom required

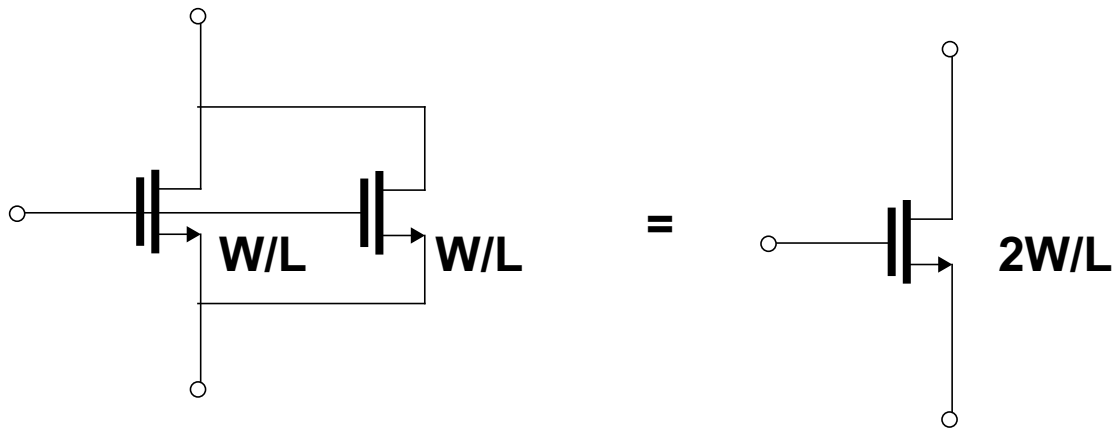
Assume both stages have same bias current. Ignore body effect.



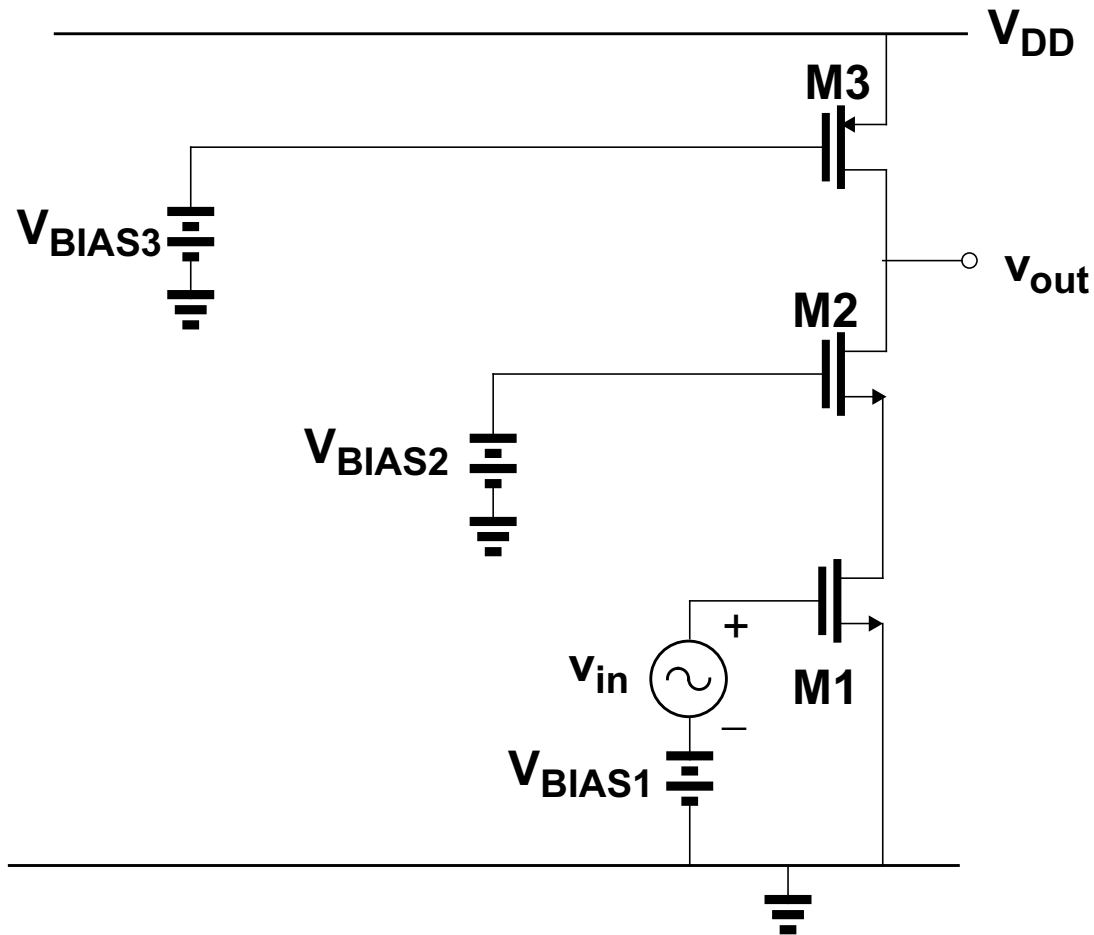
Note:



Also:



4.8.6 Cascode gain stage with active load



$$Gain \approx -\frac{g_{m1}}{g_{cascode} + g_{load}} = -g_{m1}(r_{cascode} \parallel r_{load})$$

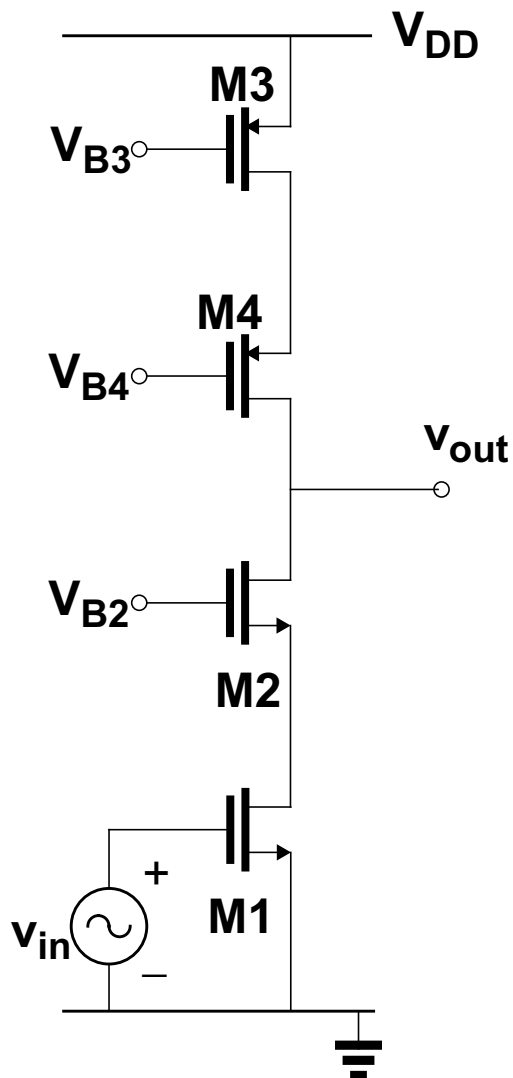
$$= -\frac{g_{m1}}{\frac{g_{ds1}}{g_{m2}/g_{ds2}} + g_{ds3}}$$

**conductance
on n side reduced**

**conductance
on p side dominant**

Need to increase impedance looking into p side

4.8.7 Cascode gain stage with cascode load



$$Gain = - \frac{g_{m1}}{\frac{g_{ds1}}{g_{m2}/g_{ds2}} + \frac{g_{ds3}}{g_{m4}/g_{ds4}}}$$

If $g_{m4}=g_{m2}$

and $g_{ds1}=g_{ds2}=g_{ds3}=g_{ds4}$

$$Gain = -\frac{1}{2} \frac{g_{m1}}{g_{ds1}} \frac{g_{m2}}{g_{ds2}}$$

Problem: Cascode stage gain

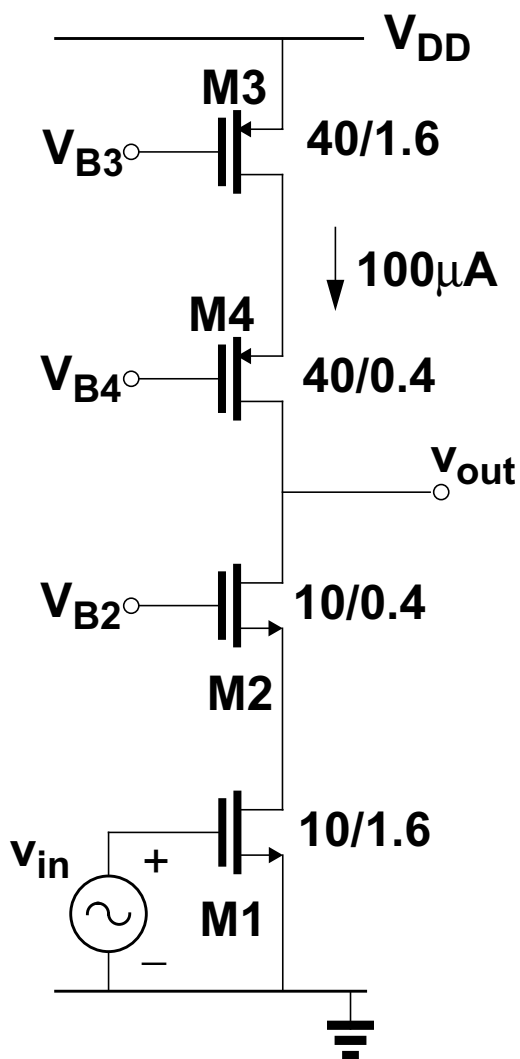
Calculate approximate gain of cascode stage shown below.

Assume all transistors biased in saturation.

Ignore body effect

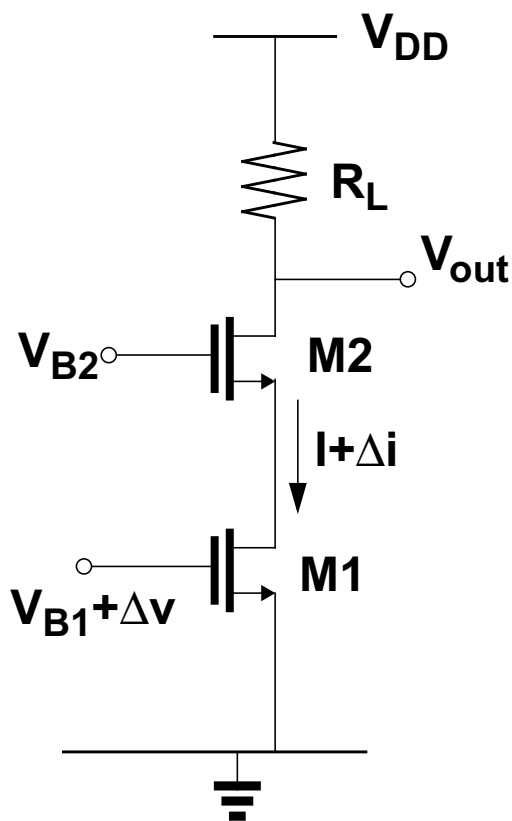
$$K_n' = 200 \mu\text{A/V}, K_p' = 50 \mu\text{A/V}$$

$$\lambda_n = \lambda_p = 0.04/\text{L V}^{-1}$$



4.9 Folded Cascode stage

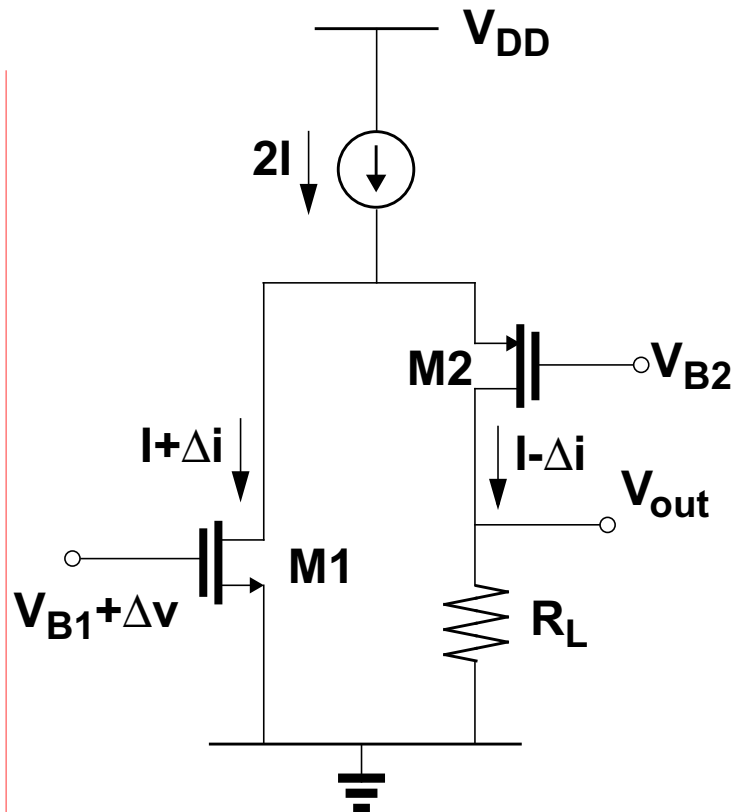
Compare the following gain stages



Small signal input voltage Δv
 \Rightarrow small-signal current $\Delta i = g_m \Delta v$

Total current $= I + \Delta i$

small-signal output voltage
 $\Delta v_{out} = \Delta i \cdot R_L = g_m \Delta v R_L$



Small signal input voltage Δv
 \Rightarrow small-signal current $\Delta i = g_m \Delta v$

Total current in left branch $= I + \Delta i$

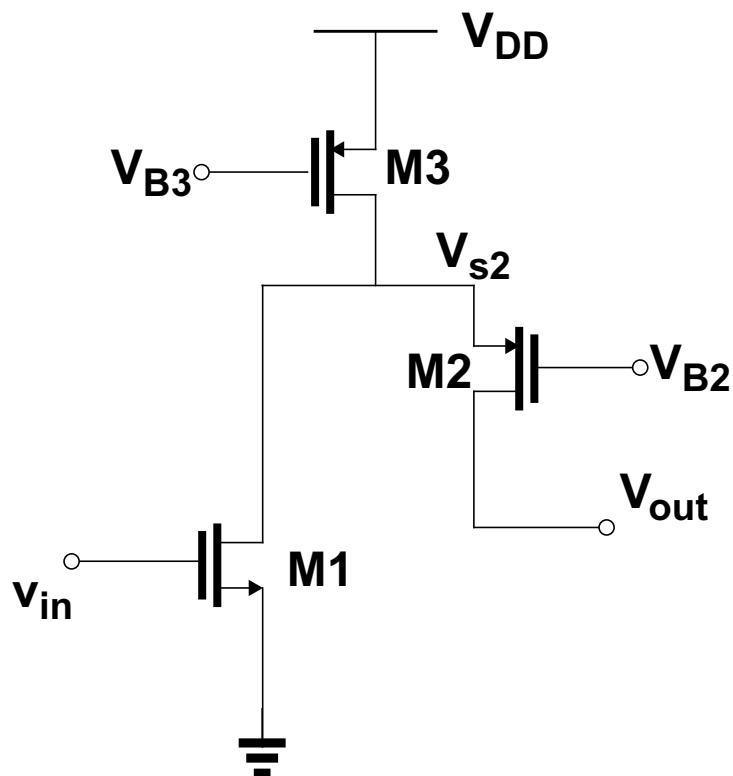
If current source is ideal its current cannot change

Total current in right branch $= I - \Delta i$

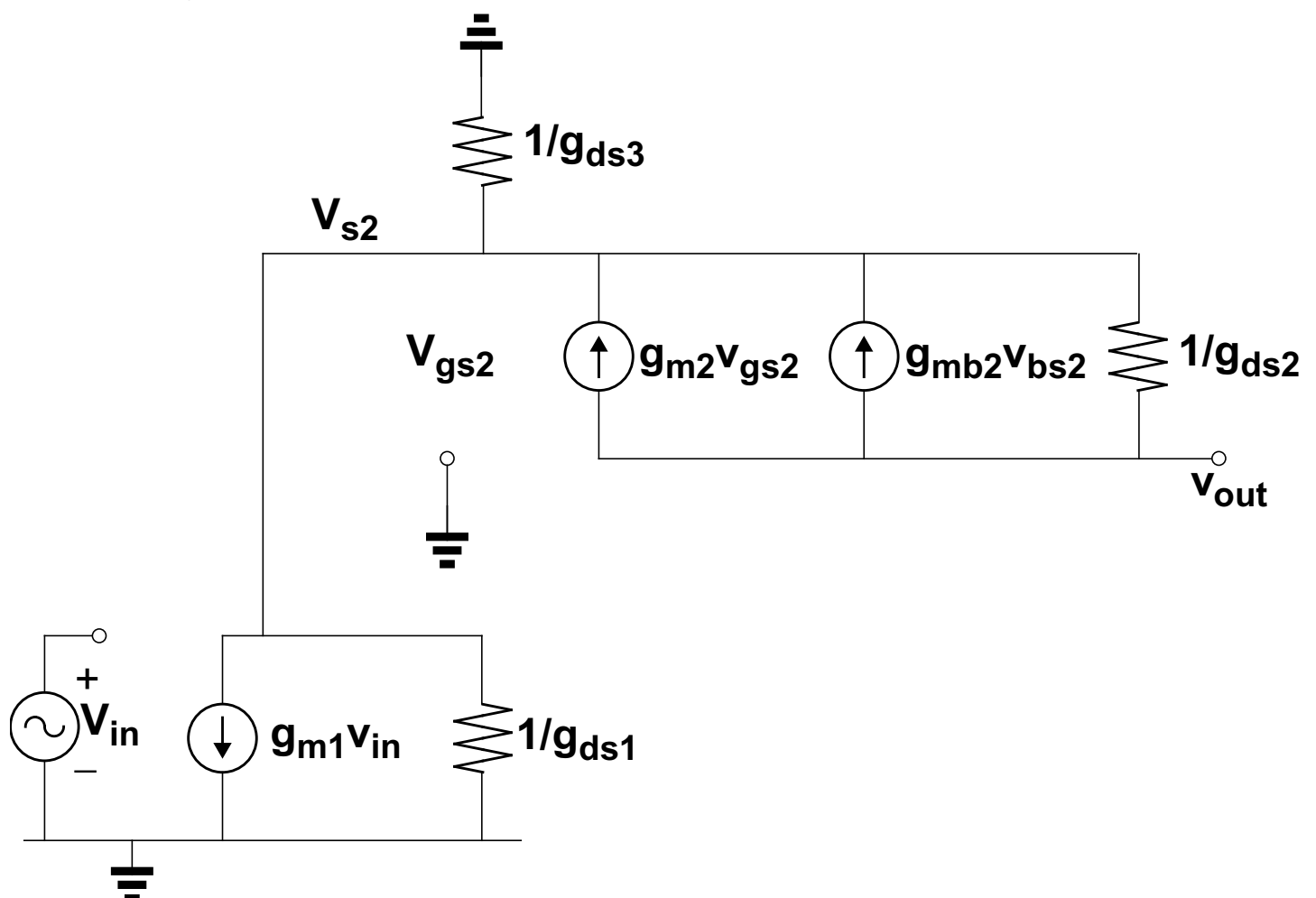
small-signal output voltage
 $\Delta v = \Delta i \cdot R_L = g_m \Delta v R_L$

'Folded' cascode

4.9.1 Folded cascode stage: Small-signal equiv. circuit

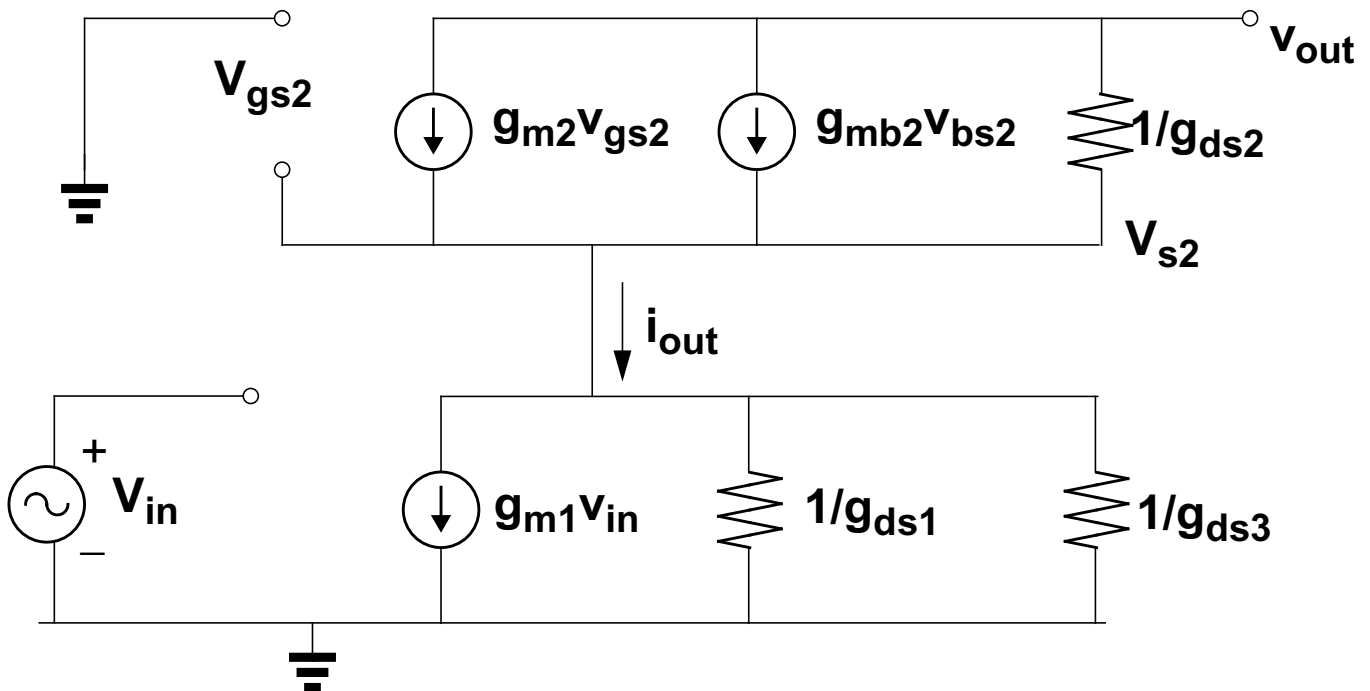


Small-signal equivalent circuit:



Folded cascode stage: Small-signal equivalent circuit (cont.)

Re-drawing we get the same small-signal equivalent circuit as for a normal cascode but output resistance of M3 is in parallel with that of M1



This reduces output resistance, gain of folded cascode (could also cascode M3 to reduce this effect)

$$G_m \approx g_{m1}$$

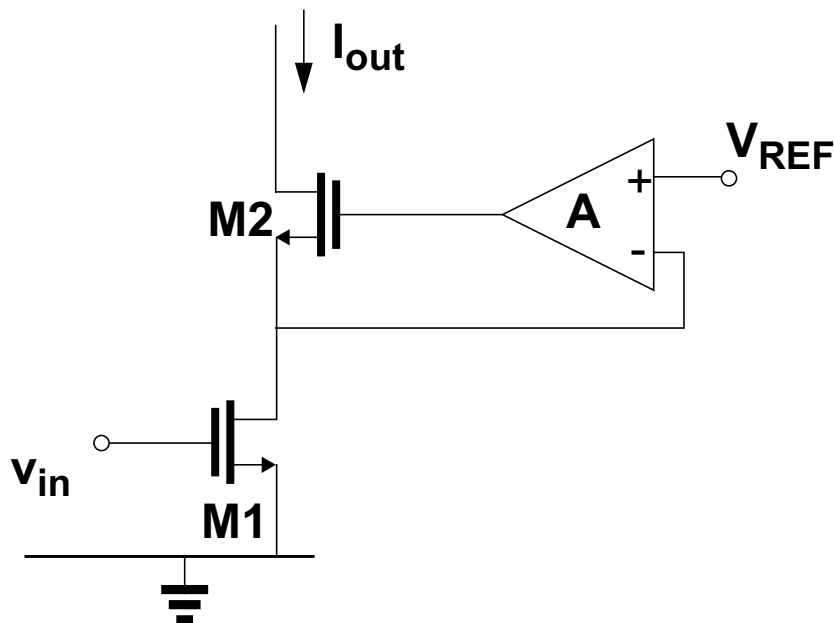
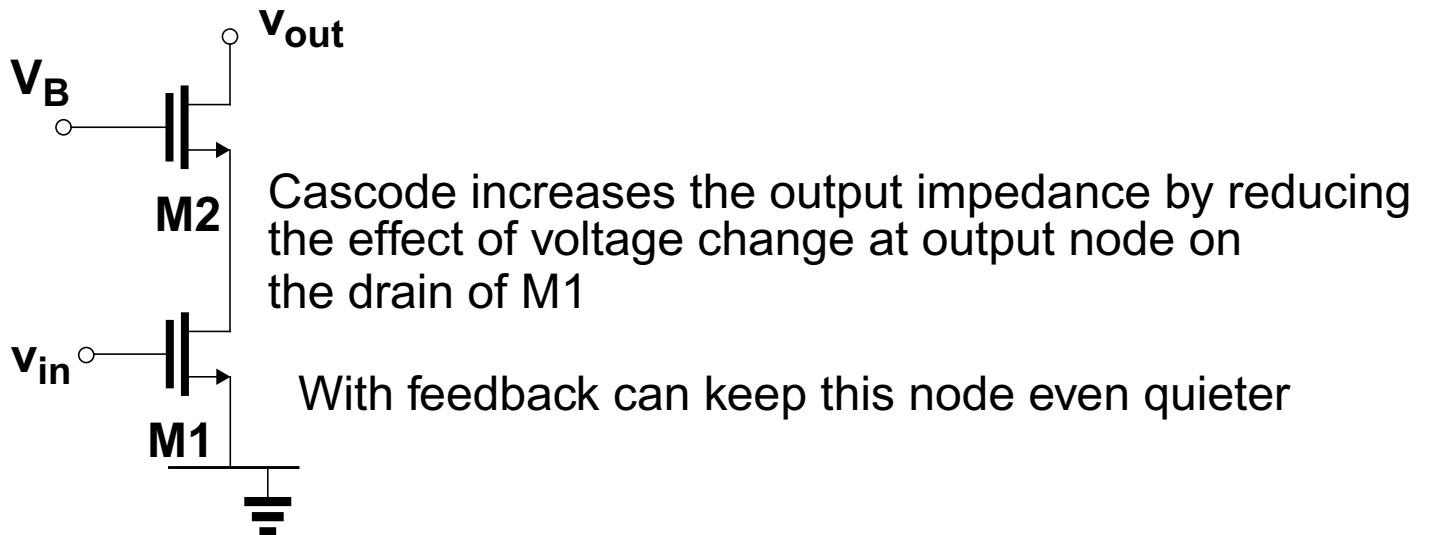
$$g_{out} \approx \frac{g_{ds1} + g_{ds3}}{\left(\frac{g_{m2} + g_{mb2}}{g_{ds2}} \right)} \quad r_{out} \approx \frac{1}{g_{ds1} + g_{ds3}} \left(\frac{g_{m2} + g_{mb2}}{g_{ds2}} \right)$$

$$\frac{v_{out}}{v_{in}} \approx \frac{g_{m1}}{g_{ds1} + g_{ds3}} \frac{(g_{m2} + g_{mb2})}{g_{ds2}}$$

Folded cascodes: more current, less gain.
But often used in opamps.

4.10 Regulated cascodes

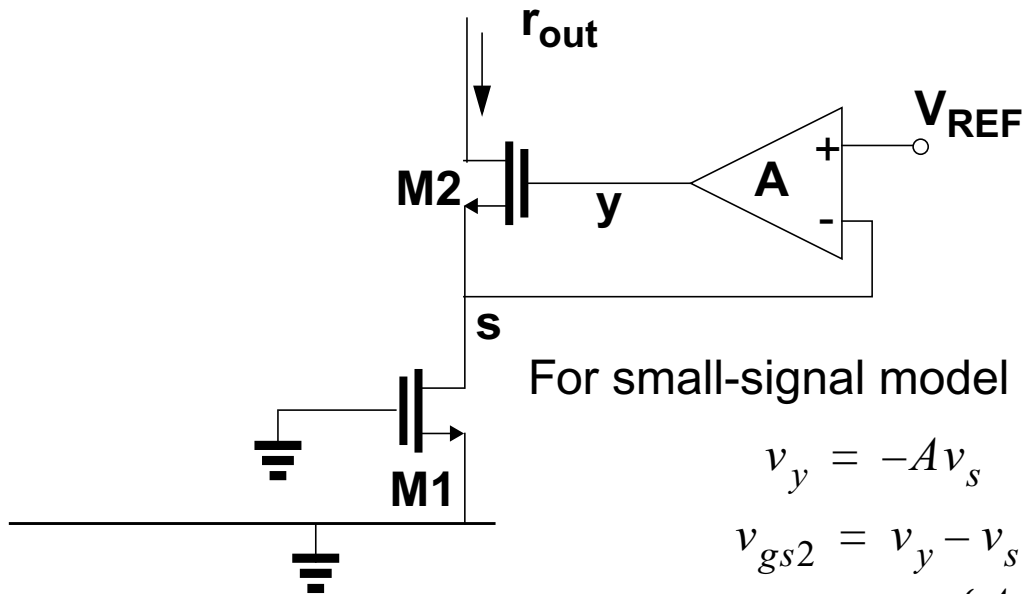
Negative feedback can be used to increase output resistance (and gain) even further.



Intuitively
$$r_{out} \cong r_{ds1} \frac{g_{m2}}{g_{ds2}} (A + 1)$$

4.10.1 Regulated cascodes : output resistance

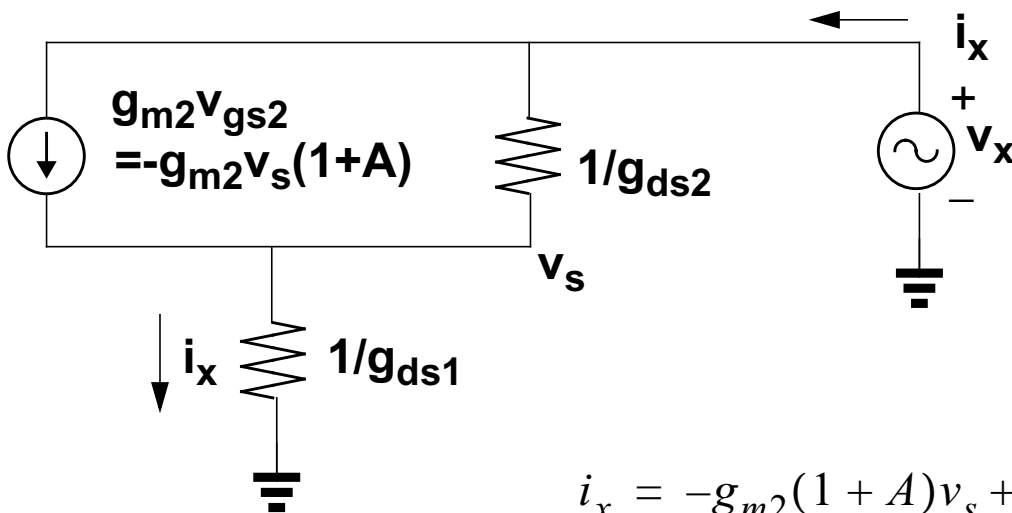
Measure output resistance looking into drain of M2 (with input at gnd)



$$v_y = -A v_s$$

$$v_{gs2} = v_y - v_s$$

$$v_{gs2} = -v_s(A + 1)$$



$$i_x = -g_{m2}(1 + A)v_s + (v_x - v_s)g_{ds2}$$

Since $v_s = \frac{i_x}{g_{ds1}}$

$$i_x = -g_{m2}(1 + A)\frac{i_x}{g_{ds1}} + \left(v_x - \frac{i_x}{g_{ds1}}\right)g_{ds2}$$

$$i_x \left(1 + \frac{g_{m2}(1 + A)}{g_{ds1}} + \frac{g_{ds2}}{g_{ds1}}\right) = v_x g_{ds2}$$

$$\frac{v_x}{i_x} = \frac{1}{g_{ds2}} \left(1 + \frac{g_{m2}(1 + A)}{g_{ds1}} + \frac{g_{ds2}}{g_{ds1}}\right)$$

$$r_{out} \cong r_{ds1} \frac{g_{m2}}{g_{ds2}} (A + 1)$$

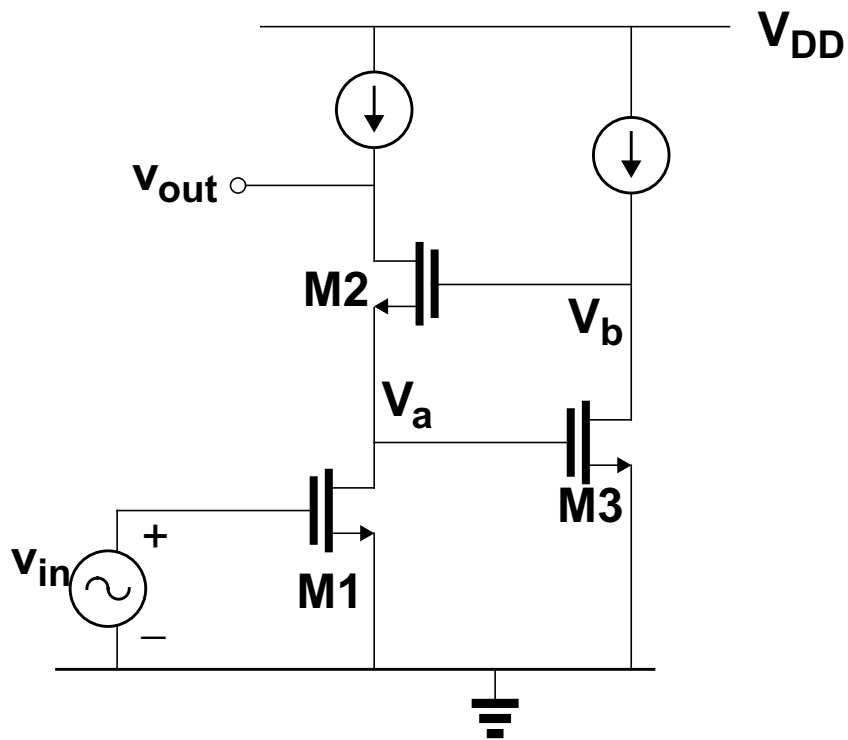
r_{out} has been increased by a factor $A+1$

Problem- regulated cascode:

What is voltage gain of stage shown below?

Assume all transistors are biased in saturation.

Ignore body effect.



5 Current Mirrors and Current sources

5.1 Bias current provision on an IC

Most circuits require a DC biasing current.

The usual strategy on an IC is

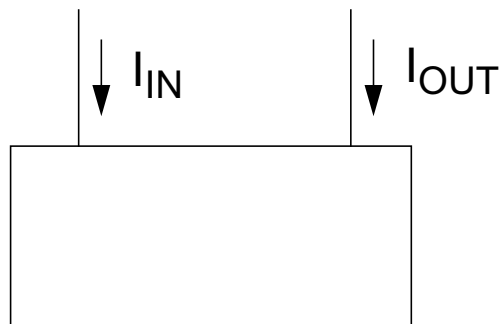
Generate one reference bias current

Copy (mirror) it around IC as required -> current mirror

5.1.1 DC Current mirrors

A good DC current mirror:

- (i) Has good DC accuracy (static and random)
- (ii) Has a high output resistance (i.e. low dependence of output current on voltage)
- (iii) Has good output compliance (i.e. will work as a current source even for low voltages at the output)



5.1.2 Current sources and small-signal gain

Gain of stages we have examined determined by

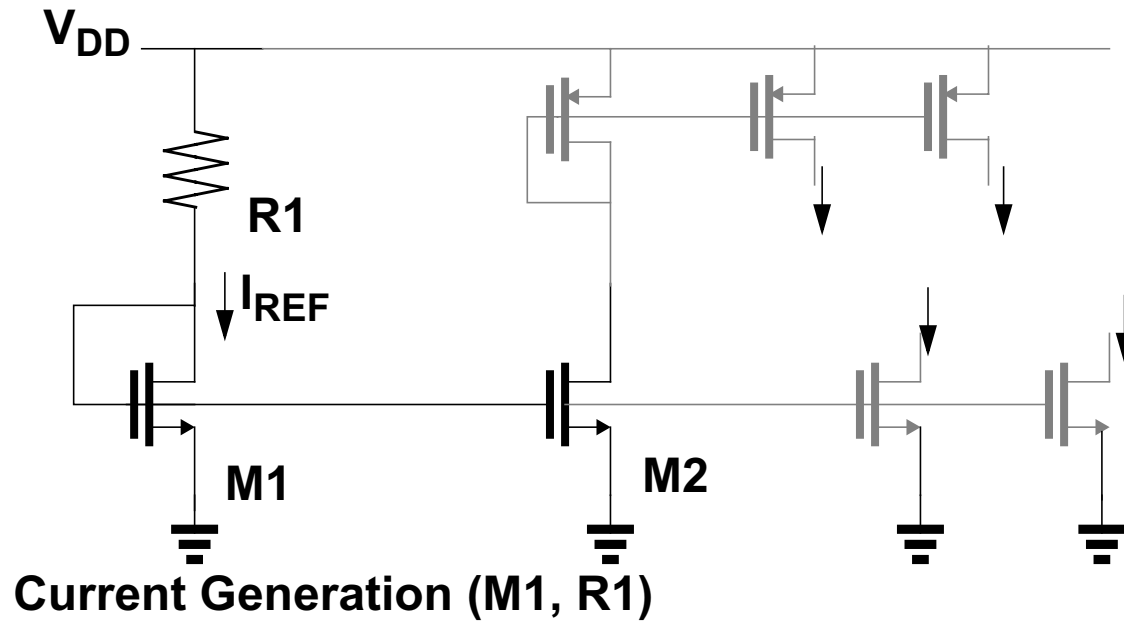
- (i) Transconductance G_m
- (ii) Output resistance of the stage itself in parallel with the output resistance of the load

We have come across various load resistances:

- (i) Resistor: relatively low resistance, increasing resistance costs voltage headroom
- (ii) MOS Diode (low resistance $1/g_m$)
- (iii) Saturated transistor load (high resistance $1/g_{ds}$)
- (iv) Cascode load (very high resistance g_m/g_{ds})
- (v) Ideal DC current source load: infinite output resistance

As the load of a high-gain stage is usually the output of a current source, the design of high output resistance current mirrors and of high gain stages are interlinked.

5.1.3 Current-generation with low accuracy requirement:



$$I_{REF} = I_{D1} = \frac{V_{DD} - V_{GS1}}{R_1} = \frac{K'_n W_1}{2 L_1} (V_{GS1} - V_t)^2$$

Dimension M1 to give required current

Note: I_{D1} is supply-dependent

process-dependent (V_t , K'_n , R_1)

temperature-dependent (V_t , K'_n , R_1)

Current Mirror (M1, M2)

If M2 is in saturation then (and neglecting output conductance) I_{D2} is given by

$$I_{D2} = \frac{K'_n W_2}{2 L_2} (V_{GS2} - V_t)^2$$

$$\frac{I_{D2}}{I_{D1}} = \frac{\frac{K'_n W_2}{2 L_2} (V_{GS2} - V_t)^2}{\frac{K'_n W_1}{2 L_1} (V_{GS1} - V_t)^2} = \frac{W_2}{L_2} \frac{L_1}{W_1}$$

i.e. ratio of output current to input current determined by ratio of sizes of M2 to M1

I_{REF} can be copied further as shown

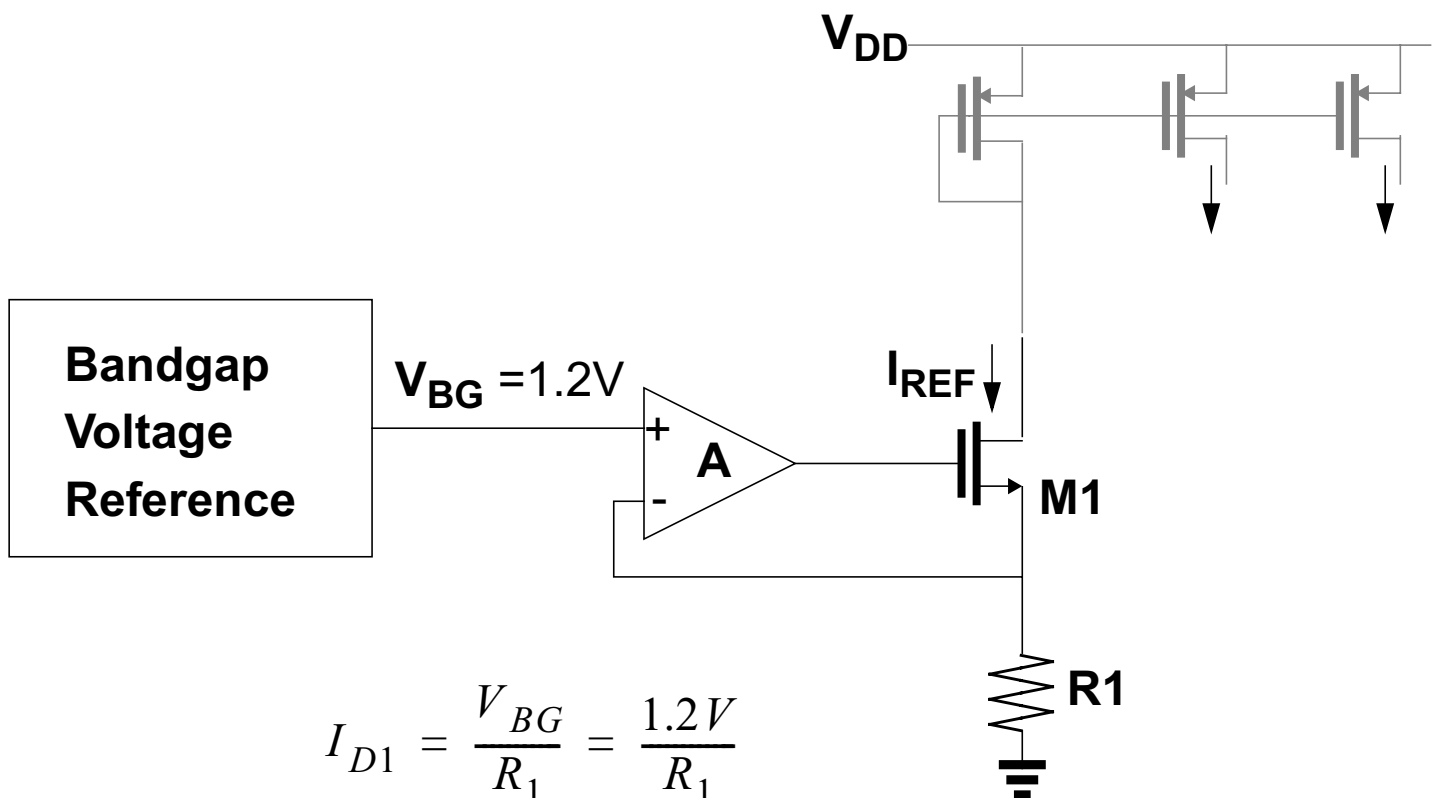
5.1.4 Current-generation with high accuracy requirement:

Not easy to generate an absolutely accurate current reference on IC

It is possible to generate an accurate voltage reference:

Bandgap voltage reference.

Usual approach: copy bandgap voltage over external resistor



Common application:

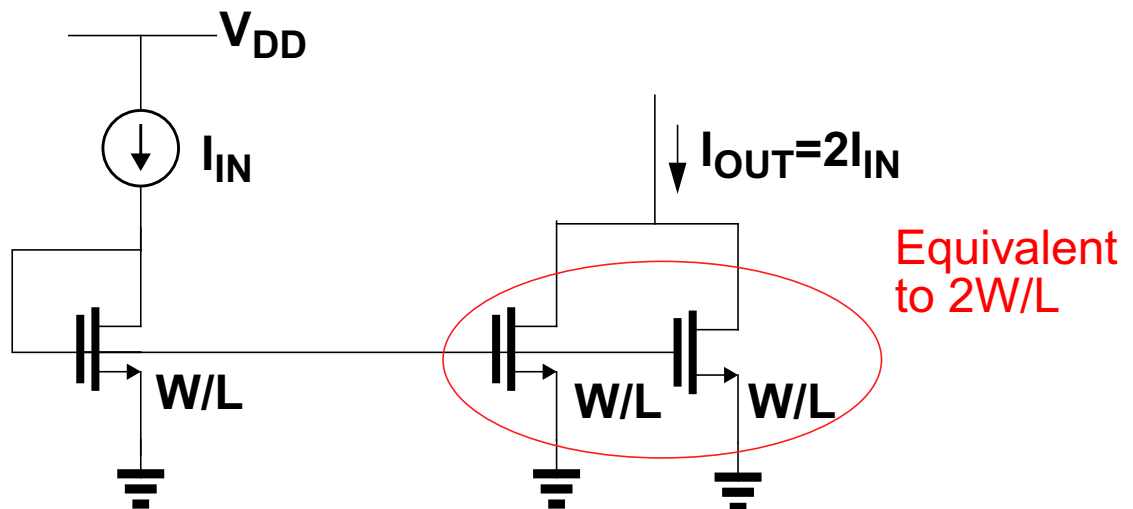
$$I_{D1} = \frac{1.2V}{12k\Omega} = 100\mu A$$

5.2 Simple Current mirrors

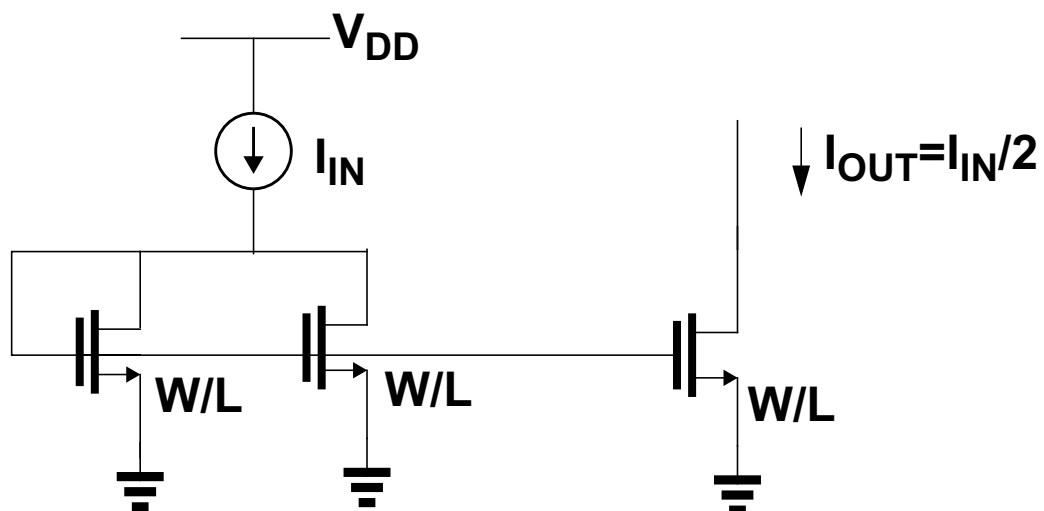
For accuracy (in IC processing) use unit transistors.

Also for accuracy (in IC processing) scale widths not lengths.

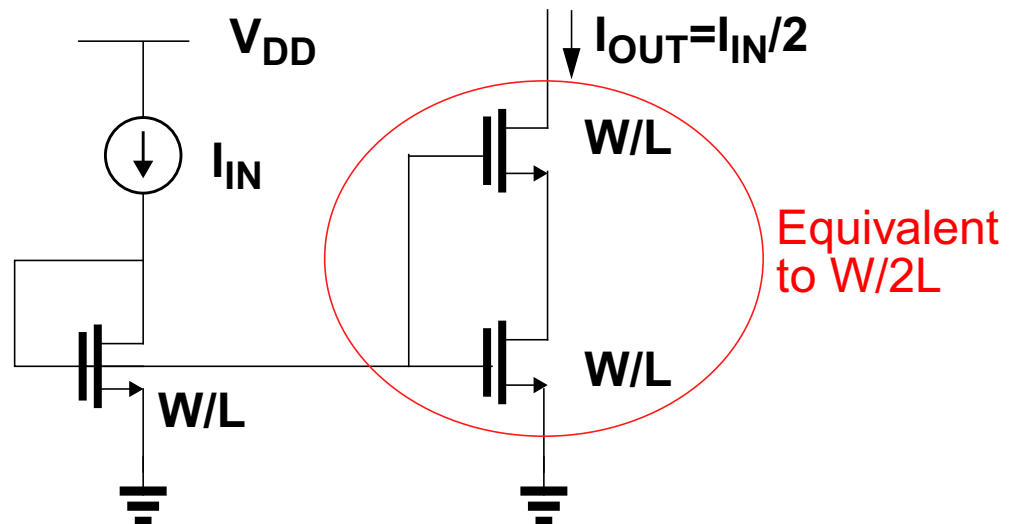
Multiplying:



Dividing:

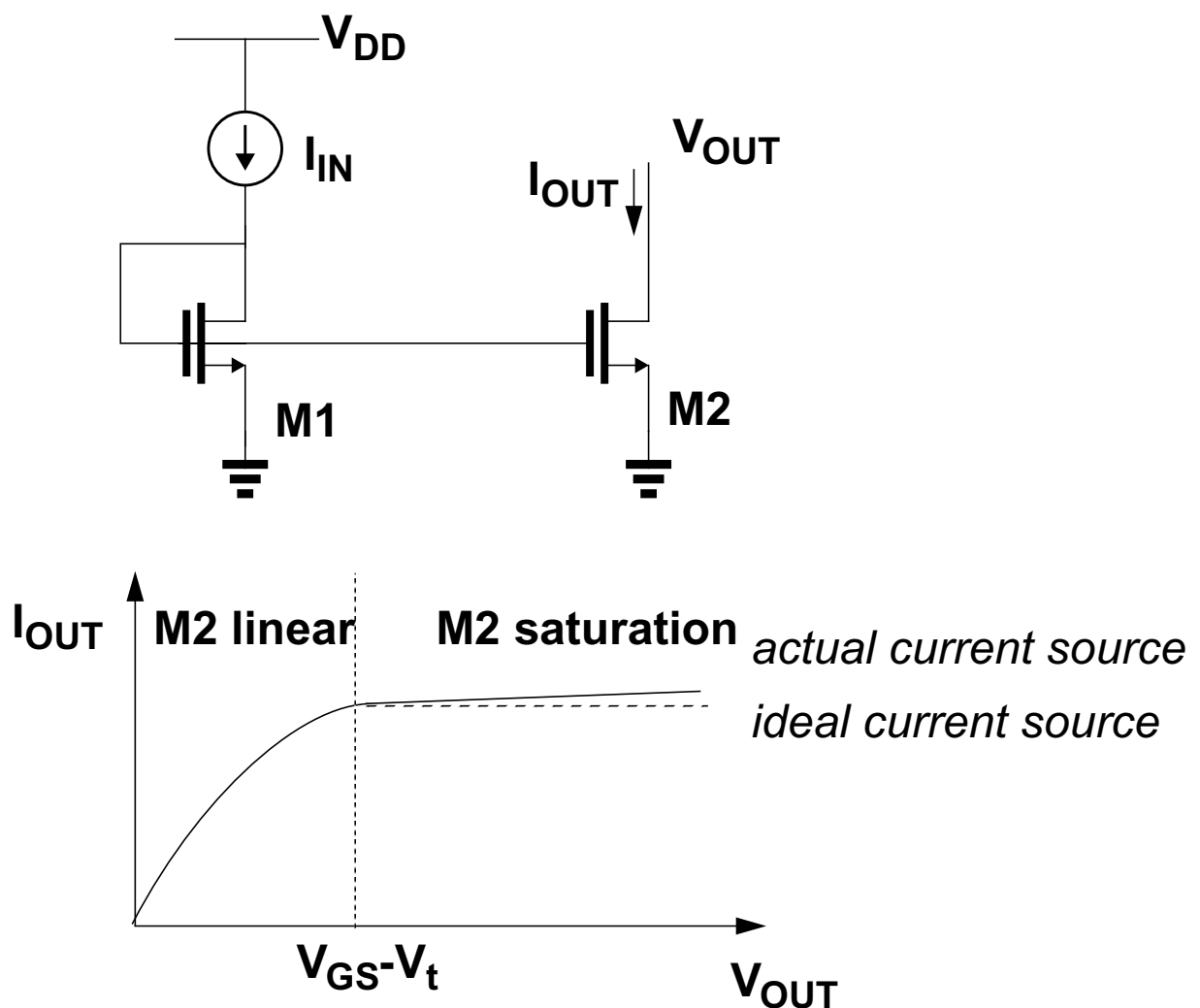


Alternatively (for current division):



Can be useful to prevent transistors going into sub-threshold

5.2.1 Accuracy of Current mirrors



M1 is in saturation.

For accurate current mirroring and high output resistance, M2 must also be in saturation

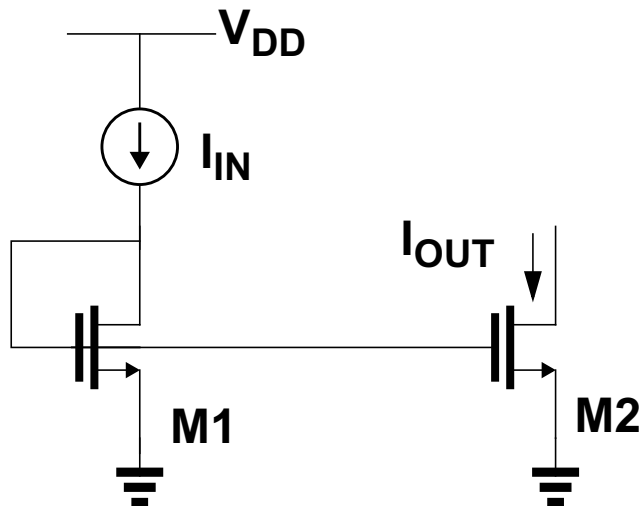
i.e. there is a minimum voltage required at V_{OUT}

$$V_{OUT} > V_{GS} - V_t$$

This is called 'output compliance' - minimum voltage at the output of the mirror such that the mirror performs to spec.

Accuracy of Current mirrors (contd.)

If M2 is in saturation there is still an inaccuracy in current mirroring as the voltage at the drain of M2 varies (due to output conductance)



$$I_{D1} = \frac{K'_n W_1}{2 L_1} (V_{GS} - V_t)^2 (1 + \lambda V_{DS1})$$

$$I_{D2} = \frac{K'_n W_2}{2 L_2} (V_{GS} - V_t)^2 (1 + \lambda V_{DS2})$$

$$\frac{I_{D2}}{I_{D1}} = \frac{W_2/L_2}{W_1/L_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

If V_{DS2} is not equal to V_{DS1} then we get mirroring inaccuracy
Inaccuracy dependent on λ .

Recall:

$$\lambda \propto \frac{1}{L}$$

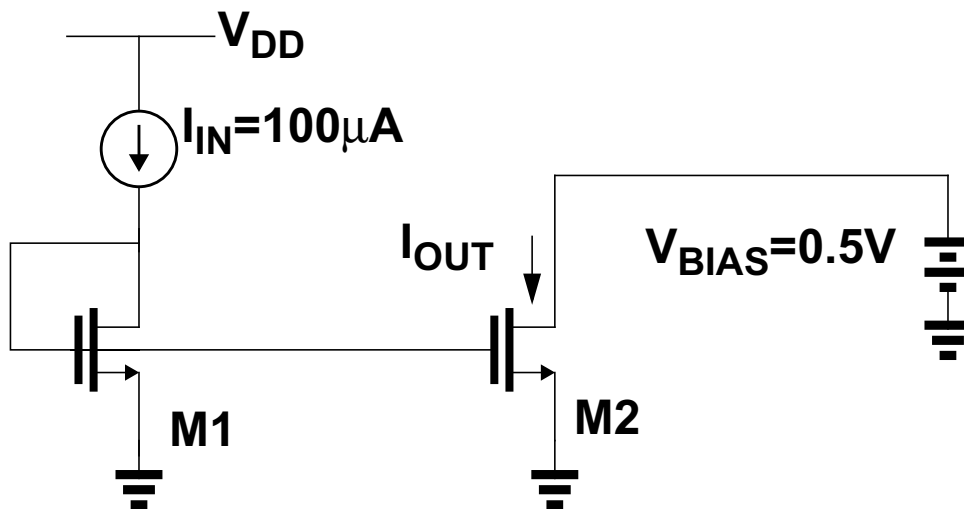
For better accuracy (higher output resistance) use larger L

Note: small signal output resistance of current mirror

$$r_{out} = \frac{1}{g_{ds2}}$$

Example - Current mirror accuracy :

What is the relative error in I_{OUT} in the following circuit?



Take $V_t = 0.8V$,

$V_{GS} - V_t = 0.2V$,

$\lambda = 0.04/L \text{ V}^{-1}$,

$L_1, L_2 = 1\mu m$, $W_1/L_1 = W_2/L_2$

$$\begin{aligned}\frac{I_{D2}}{I_{D1}} &= \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} = \frac{1 + 0.04 \times 0.5}{1 + 0.04 \times 1} \\ &= \frac{1 + 0.04 \times 0.5}{1 + 0.04 \times 1} = \frac{1.02}{1.04} = 0.98\end{aligned}$$

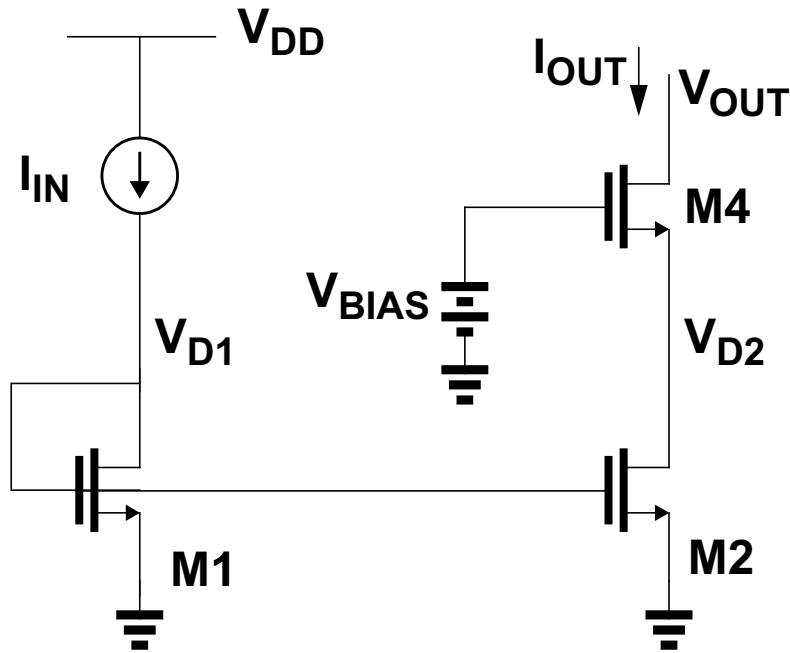
i.e. 2% mismatch

To improve accuracy increase L (at cost of voltage headroom)

In other words increase output impedance.

Alternatively ensure $V_{DS2} = V_{DS1}$

5.3 Cascode Current Mirror



Cascode will increase output resistance of current mirror

$$r_{out} \cong \frac{g_{m4}}{g_{ds4}} \cdot \frac{1}{g_{ds2}}$$

Biasing:

For M2 to be in saturation

$$V_{D2} \geq V_{GS2} - V_t$$

$$V_{BIAS} - V_{GS4} \geq V_{GS2} - V_t$$

For M4 to be in saturation

$$V_{OUT} - V_{D2} \geq V_{BIAS} - V_{D2} - V_t$$

$$V_{OUT} \geq V_{BIAS} - V_t$$

For optimal mirroring accuracy

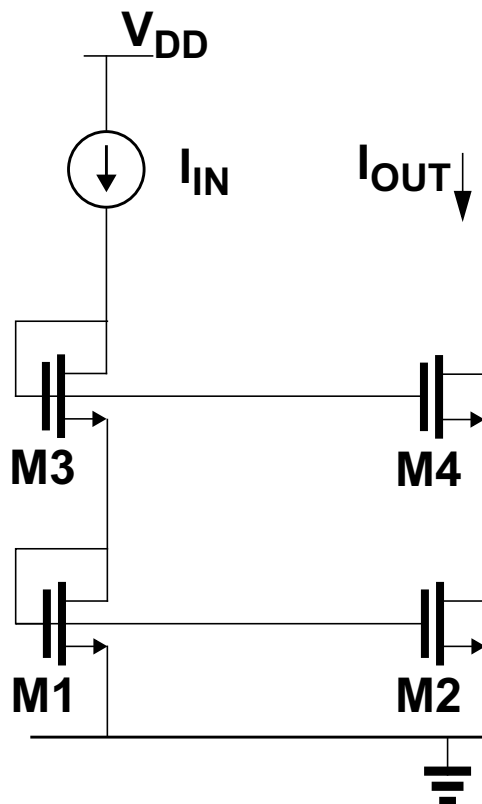
$$V_{D2} = V_{D1}$$

$$V_{BIAS} - V_{GS4} = V_{GS1}$$

5.3.1 Cascode Current Mirror - biasing

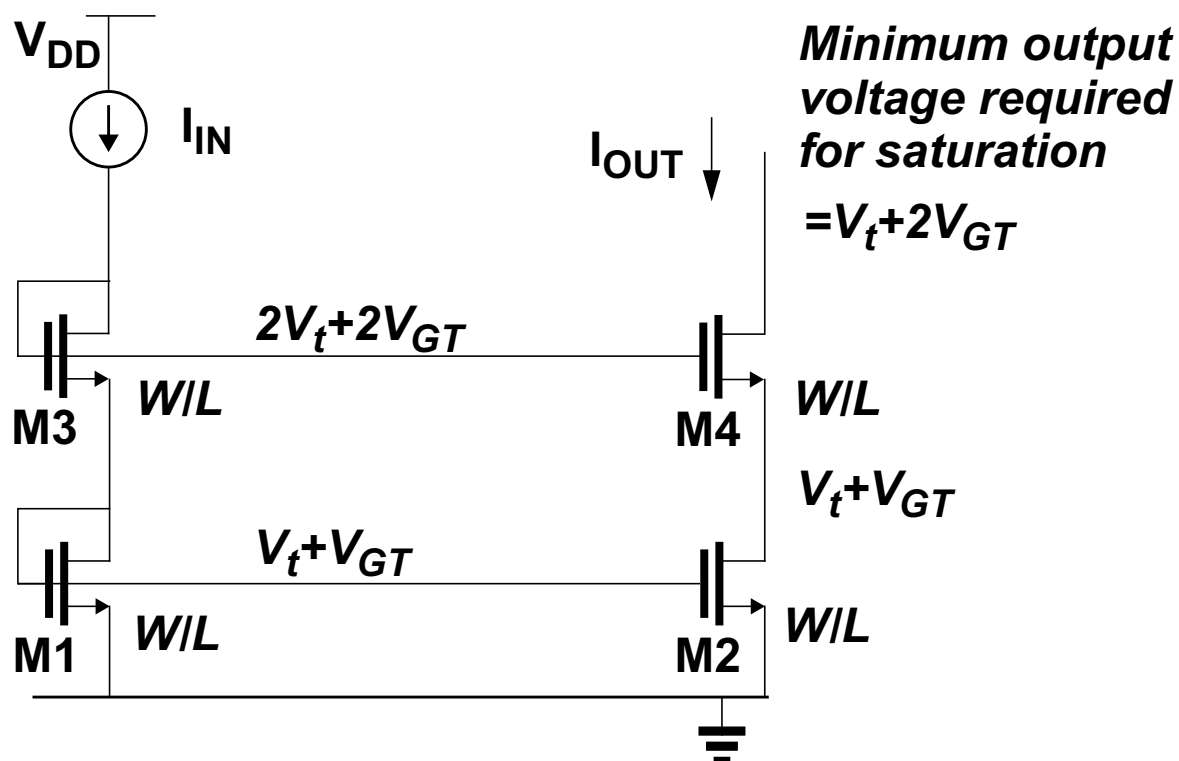
How to generate V_{BIAS} ?

Use extra MOS diode



5.3.2 Cascode Current Mirror - output compliance

Consider the case where all transistors have same dimensions
Ignore body effect for simplicity



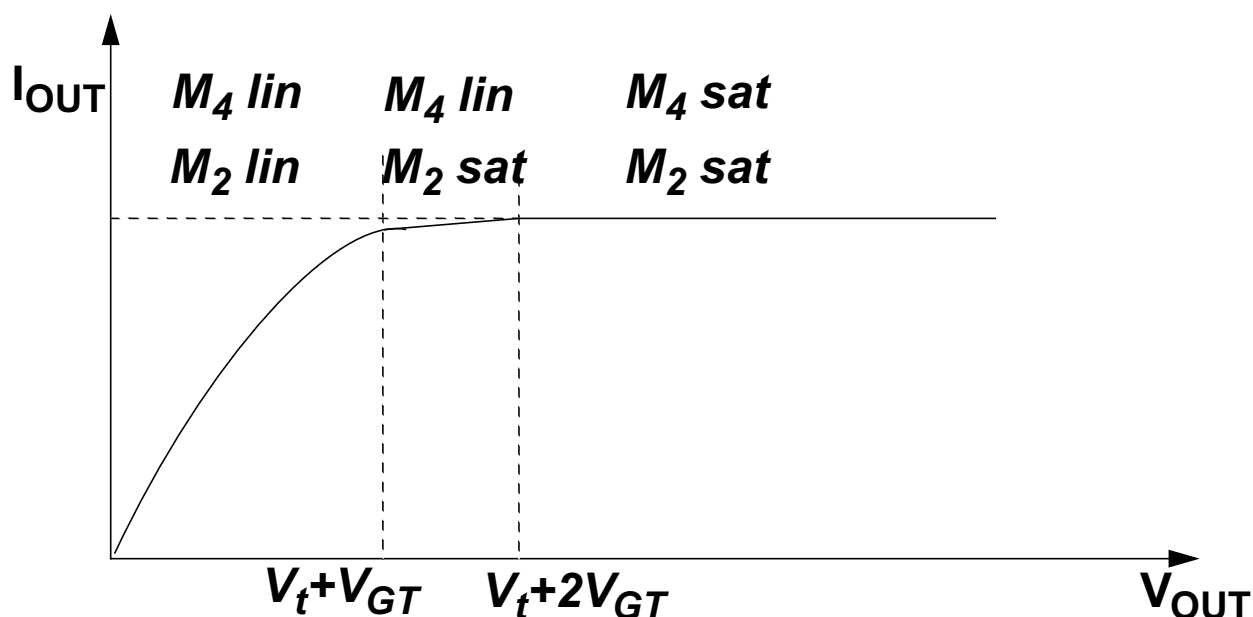
Expressing $V_{GS} - V_t$ as V_{GT} = the effective drive voltage

Assuming all devices same size and ignoring body effect

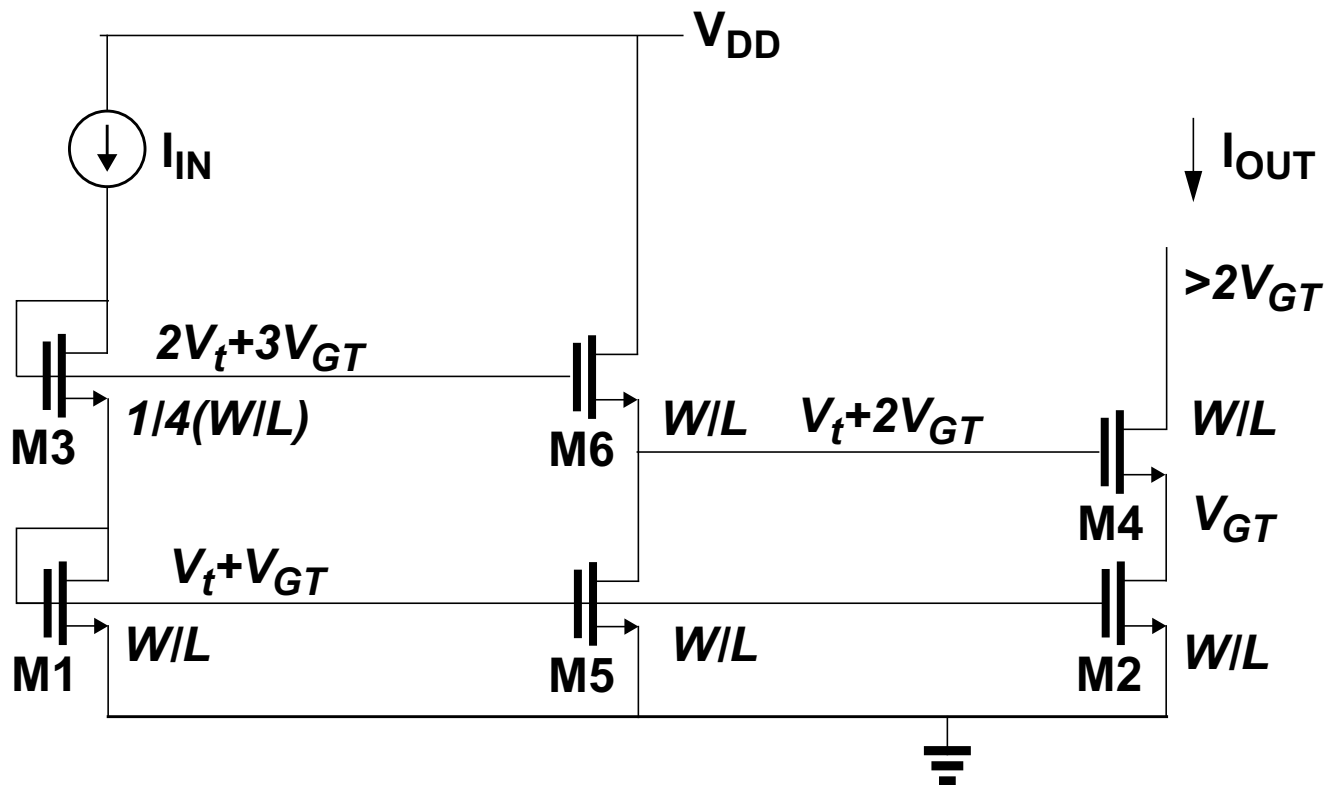
Min. voltage at output to keep output devices in saturation $V_t + 2V_{GT}$

This is rather high (should be possible with $2V_{GT}$)

Note that $V_{DS1} = V_{DS2}$ in this mirror => good accuracy



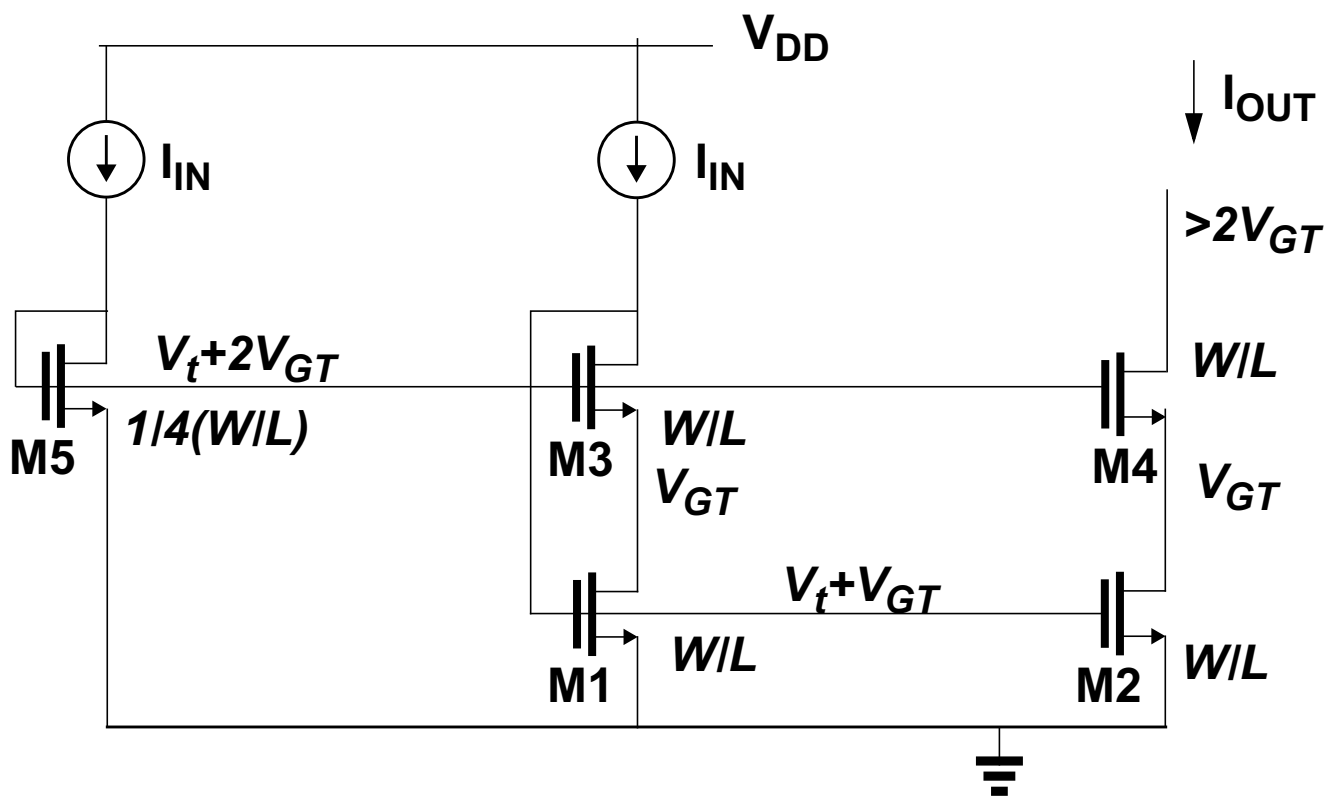
Cascode Current Mirror - output compliance (contd)



Min. voltage at output to keep output devices in saturation: $2V_{GT}$

Note: $V_{DS2} \neq V_{DS1} \Rightarrow$ biasing not optimal from an accuracy point of view.

5.3.3 Low voltage cascode Current Mirror



Same idea as before.

Minimum voltage at output to keep output devices in saturation: $2V_{GT}$

Note: $V_{DS2} = V_{DS1} \Rightarrow$ accurate current mirror.

So optimally biased for voltage headroom and accuracy

Reference branch (M3, M1) is also low-voltage

This is standard construction used today

5.4 Accuracy of Current mirrors - mismatch

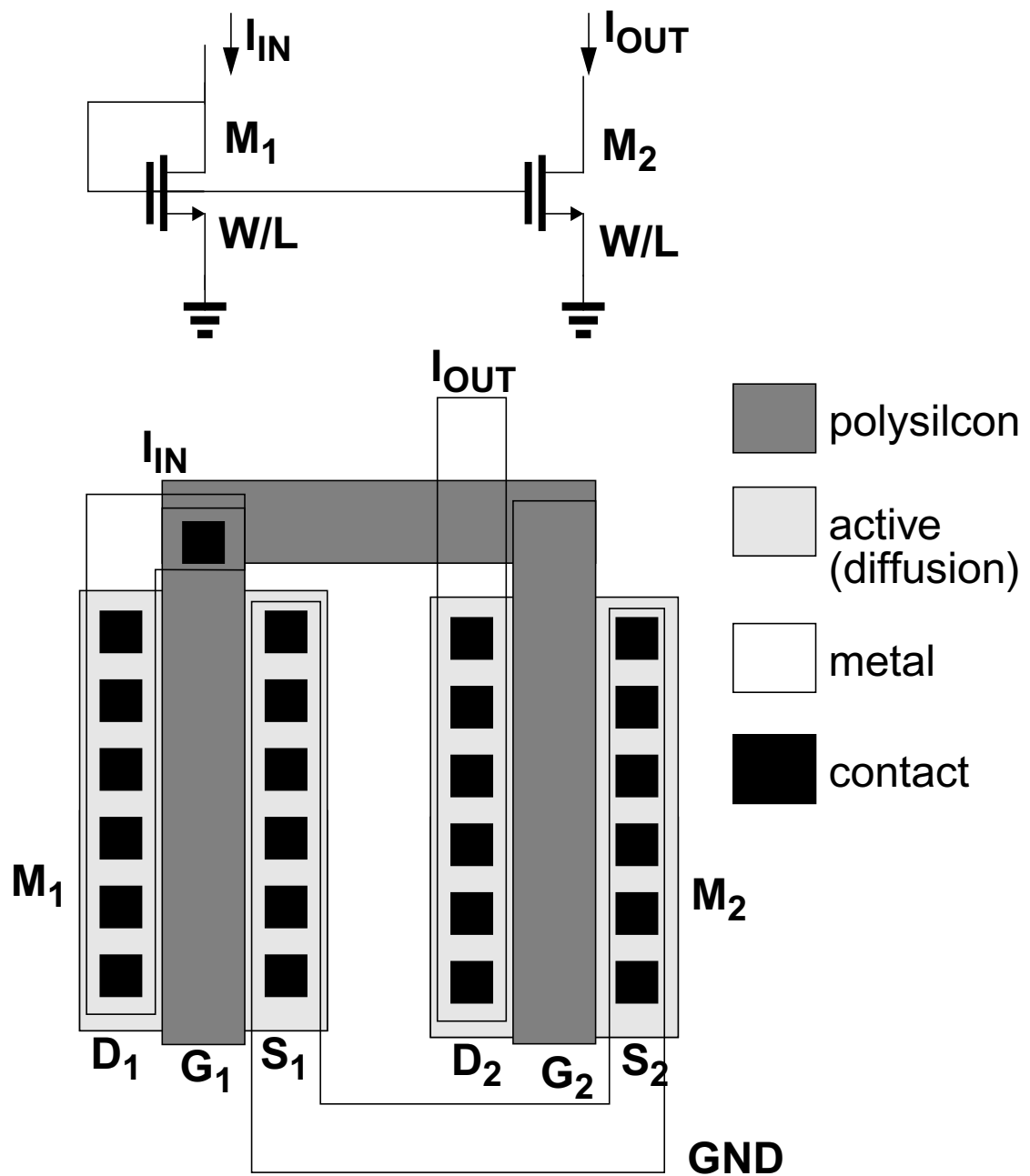
We have assumed that transistors with the same dimensions are perfectly matched, i.e. have the same electrical behaviour

In reality mismatch between identically drawn transistors occurs due to

1. Static errors due to layout
 2. Random errors due to processing
 - (i) random variations in doping levels in channel and gate
 - (ii) variations in lengths and widths of devices with identical layout
- These cause mismatch in K_n' , K_p' and V_t and so variations in drain current

5.4.1 Layout of current mirrors

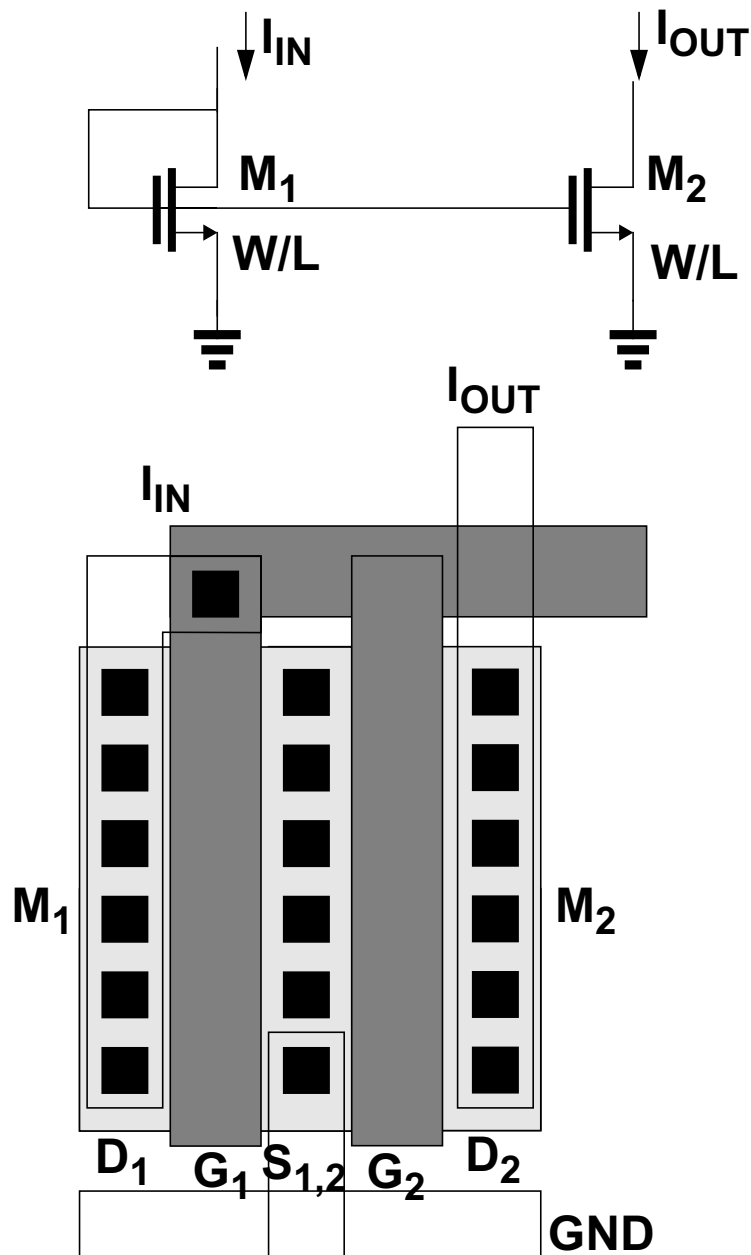
Layout for good matching



Use unit transistors, same W, L

Same orientation

Layout for low area



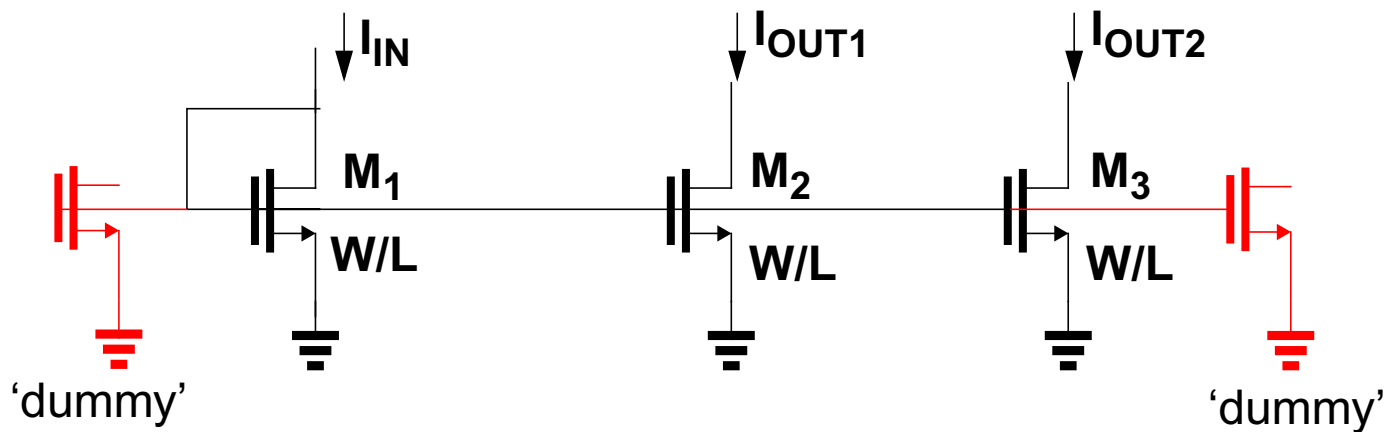
Can merge common sources to save area

But: Input transistor has drain-source orientation

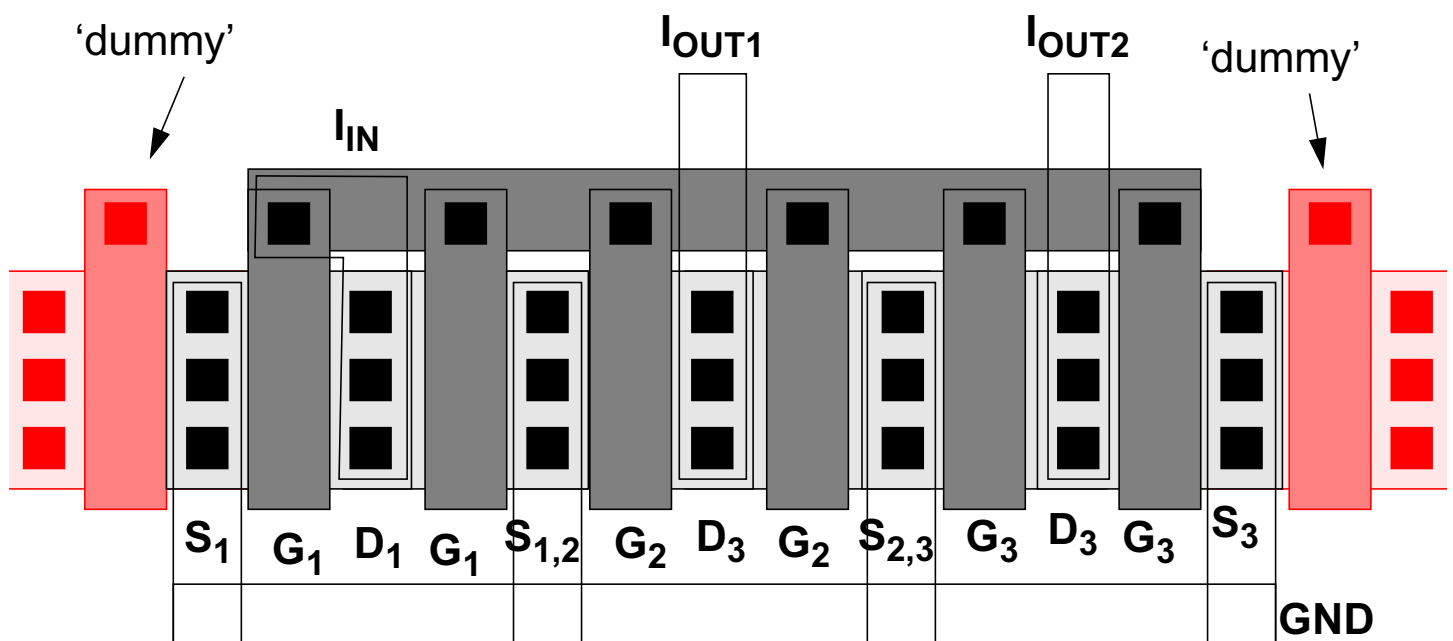
Output transistor has source-drain orientation

Bad for matching

Layout for low area, good matching



Implement M_1 , M_2 , M_3 as 2 'folded' transistors in parallel, each with width $W/2$



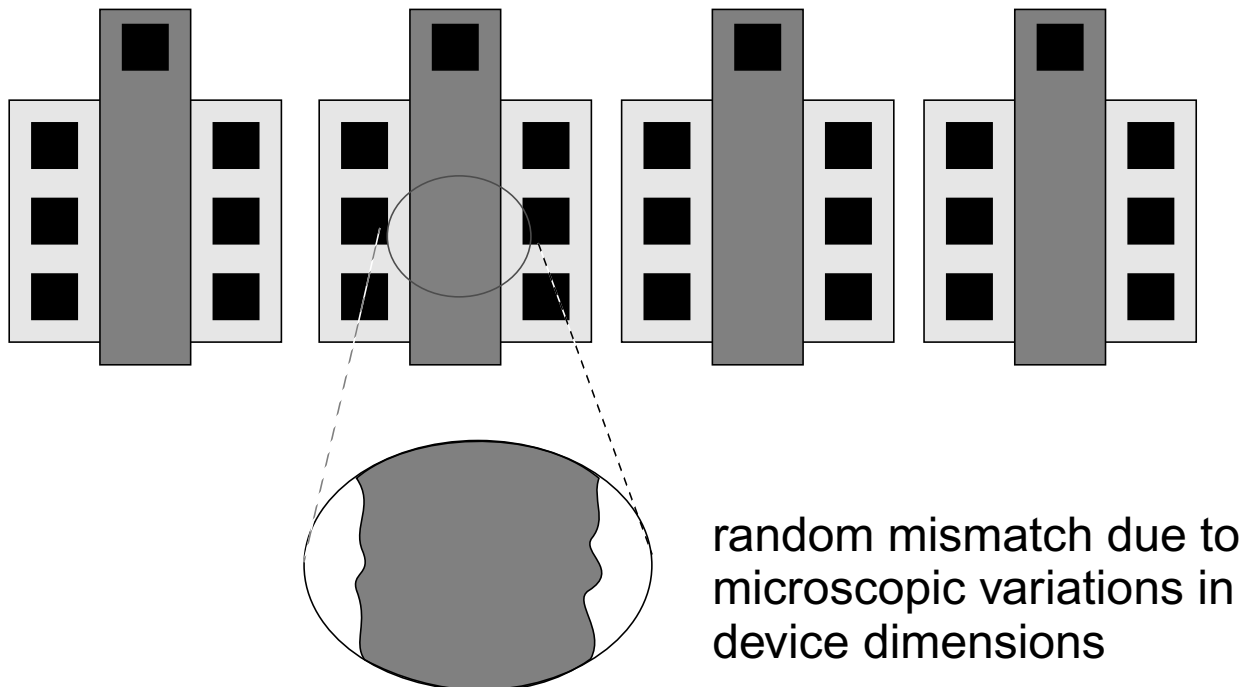
If merging transistors: keep same drain-source orientation
=> even number of folds

Add dummy devices at ends for same environment

Many other tricks for cancelling V_t gradients etc.

5.4.2 Random errors due to processing.

Even with good layout there are still variations in lengths and widths of devices with identical layout



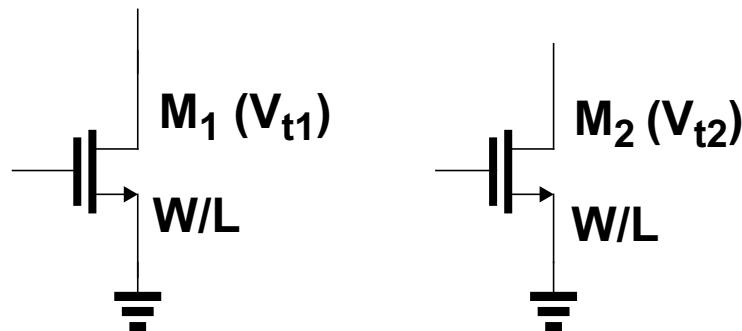
Note: under-diffusion is a particular problem - gives ΔL
For analog circuits always use $L=2..5$ times L_{\min} for matching-critical transistors.

These along with random variations in doping levels in the channel and gate cause mismatch in K_n', K_p' and V_t and so variations in drain current.

5.4.3 V_t variation

Usually the variation in V_t is dominant (over K_n' , K_p')

So two nominally identical transistors will have a difference in threshold voltages denoted by ΔV_t



$$\Delta V_t \equiv V_{t1} - V_{t2}$$

ΔV_t is generally in the order of mV (so $\ll V_t$ and $\ll V_{GS} - V_t$ if transistor is biased in strong inversion).

As mismatch is a result of random processes the value ΔV_t cannot be predicted exactly. It is however possible to predict its magnitude with a certain probability.

It has been observed that

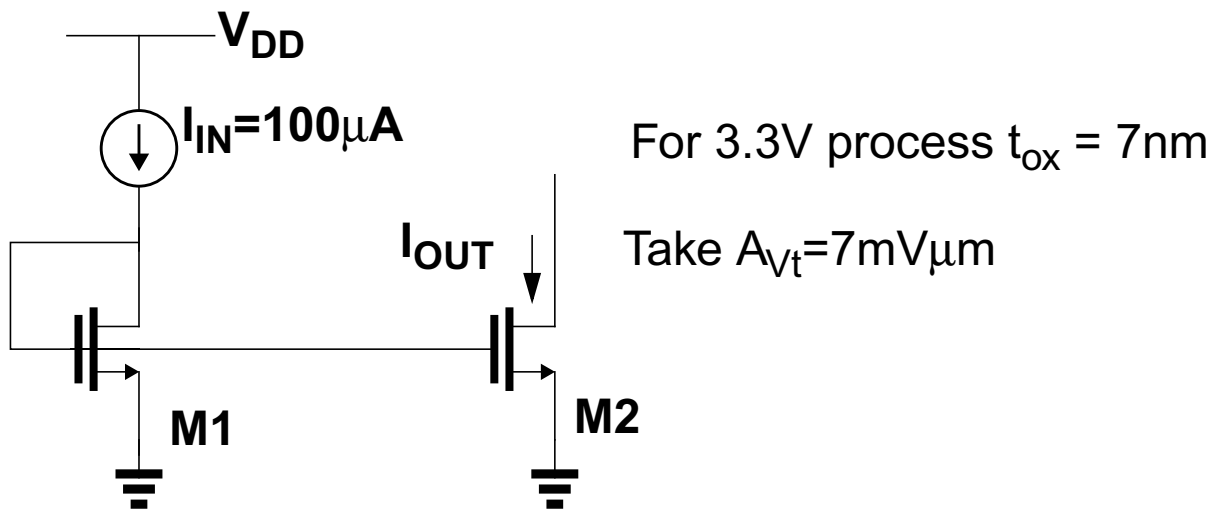
- (i) ΔV_t has a normal or Gaussian distribution
- (ii) The spread of V_t mismatch between two 'matched' devices (ΔV_t) is given by

$$\sigma_{\Delta V_t} = \frac{A_{V_t}}{\sqrt{WL}} \quad \text{where } A_{V_t} \text{ is a constant for a given process}$$

A_{V_t} units mV μ m
 $\sigma_{\Delta V_t}$ is 1 sigma variation in V_t

A_{V_t} has been observed to scale with gate oxide thickness and is approximately equal to the gate oxide thickness in nm

Example: Current source inaccuracy due to V_t mismatch



Take $V_t = 0.8\text{V}$,
 $V_{GS} - V_t = 0.2\text{V}$,
 $\lambda = 0.04/\text{L V}^{-1}$,
 $W = 10\mu\text{m}$, $L = 1\mu\text{m}$

$$\sigma_{\Delta V_t} = \frac{A_{Vt}}{\sqrt{WL}} = \frac{7\text{mV}\mu\text{m}}{\sqrt{10\mu\text{m} \cdot 1\mu\text{m}}} = 2.2\text{mV}$$

This is the 1σ mismatch in V_t of M1 and M2

This value is small compared to the overdrive voltage $V_{GS} - V_t$

=> Use small-signal analysis to calculate inaccuracy

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2 \times 100\mu\text{A}}{0.2\text{V}} = 1\text{mA/V} = 1\mu\text{A/mV}$$

$$\sigma_{I_D} = g_m \sigma_{\Delta V_t} = 2.2\mu\text{A}$$

i.e. 1σ sigma mismatch in drain currents of 2.2%

usually specify 3σ mismatch for 99.7% yield

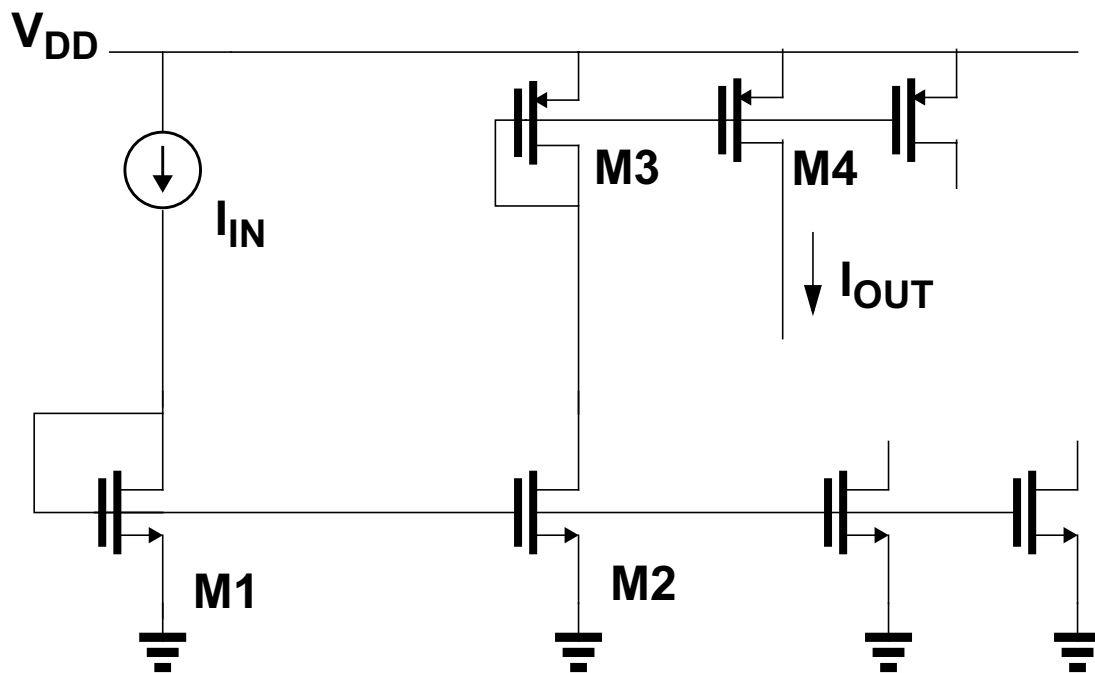
For better accuracy need larger area, or higher $V_{GS} - V_t$

Current source inaccuracy due to V_t mismatch (cont.)

Each mirror adds an error

Errors are random and so uncorrelated

=> add quadratically



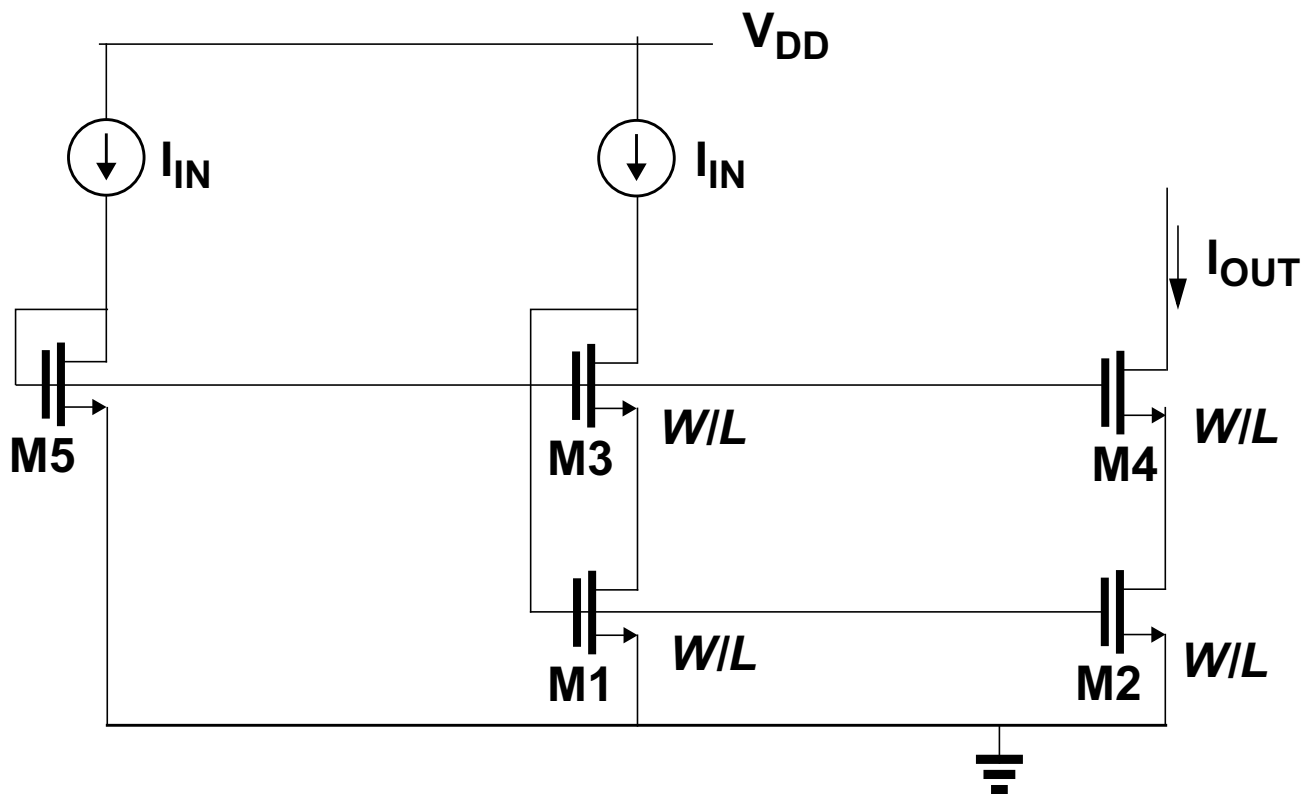
Series of 1:1 mirrors

i.e. if M1,M2 have 1σ sigma mismatch in drain currents of x%
and M3,M4 have 1σ sigma mismatch in drain currents of y%

Total 1σ sigma mismatch between I_{IN} and I_{OUT}

$$\sigma\left(\frac{I_{OUT}}{I_{IN}}\right) = \sqrt{x^2 + y^2}$$

5.4.4 Mismatch in cascode current mirrors



Mismatch in mirroring devices M1 and M2 has same effect as in ordinary mirror: $\sigma_{\Delta V_t}$ is multiplied by g_m to give current mismatch

Mismatch in cascode devices M3 and M4 causes mismatch in voltages at drains of M1 and M2.

This mismatch is multiplied by g_{ds} to give current mismatch

$g_{ds} \ll g_m \Rightarrow$ much less effect

Matching of cascode devices less critical and often use L_{min} .

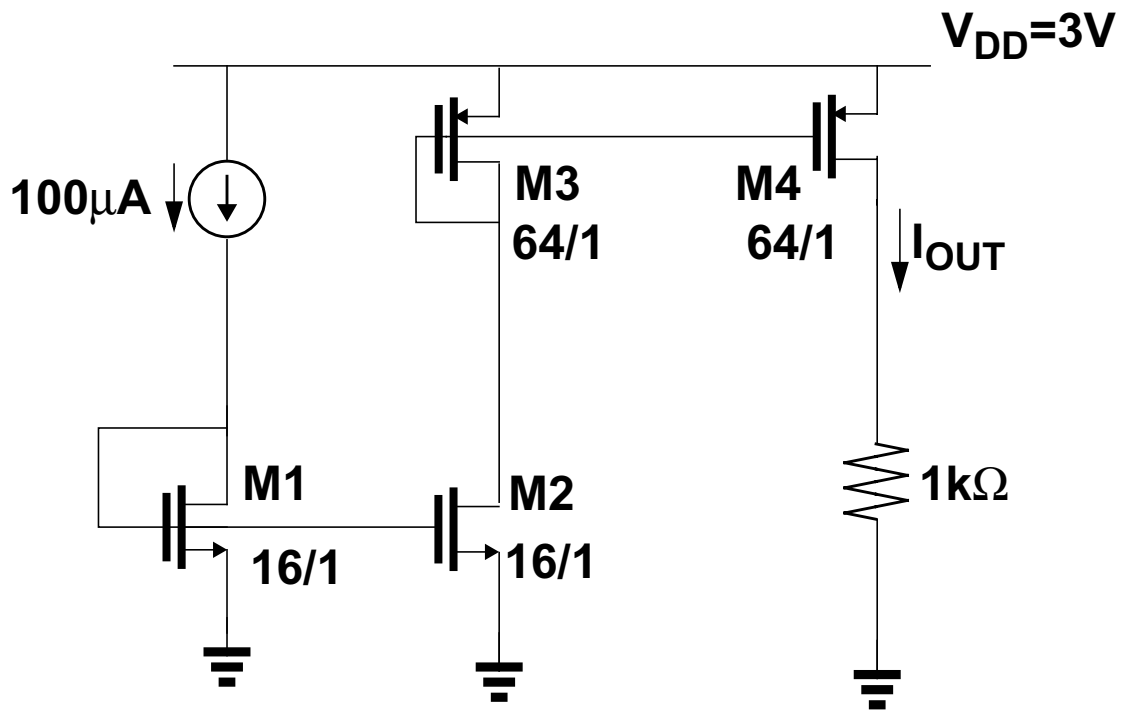
Problem: Current source inaccuracy due to V_t mismatch

Estimate the nominal value and the 3σ spread of the current I_{OUT} in the circuit below.

$$A_{V_t} = 10 \text{ mV}/\mu\text{m}$$

$$K_n' = 200 \mu\text{A}/\text{V}^2, K_p' = 50 \mu\text{A}/\text{V}^2, V_t = 0.75 \text{ V}$$

Assume all errors have a normal distribution and are uncorrelated.

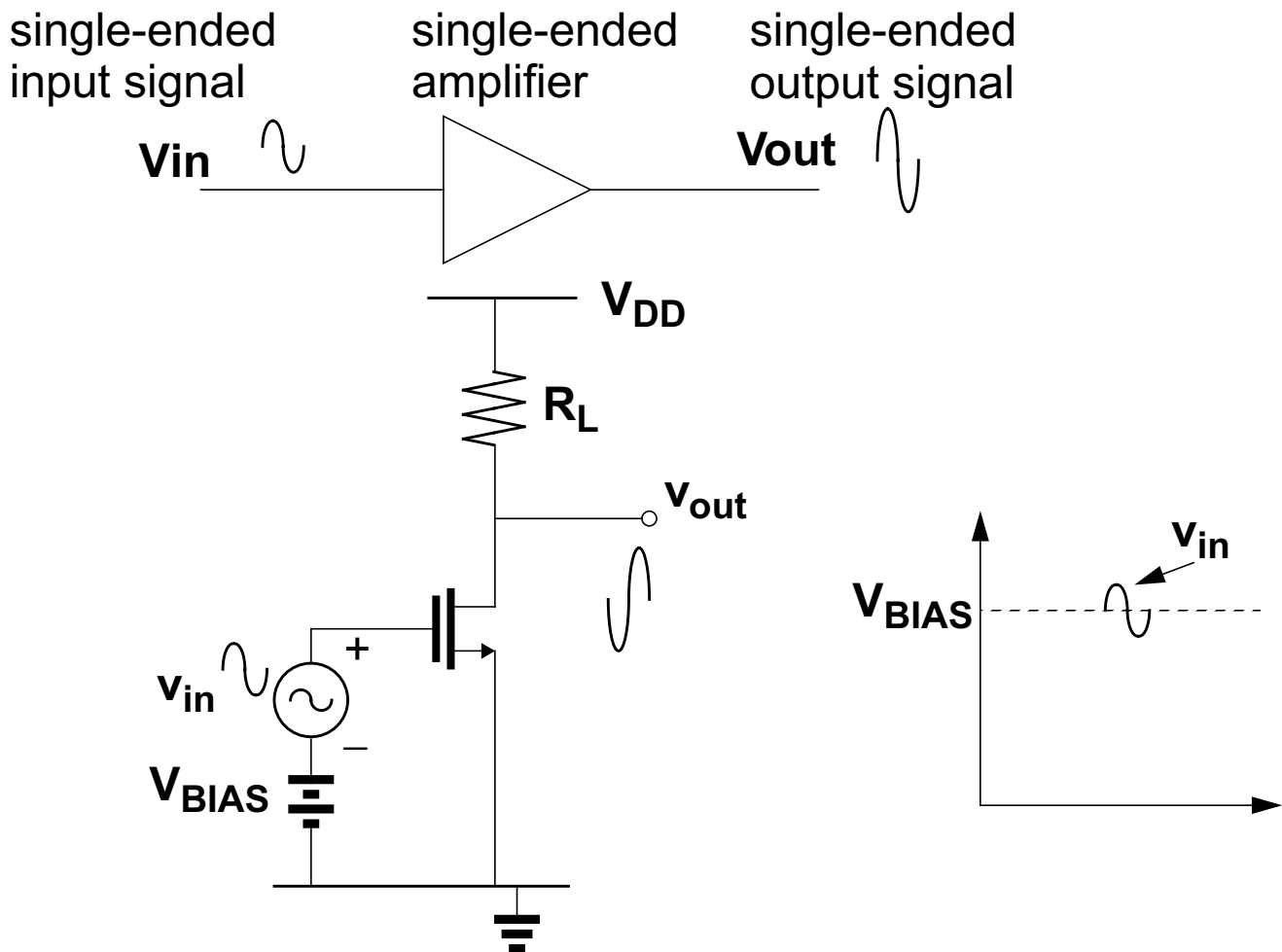


6 Differential Amplifiers

6.1 Differential amplifiers - definitions

All the amplifiers we have looked at so far have been 'single-ended' - they amplify single-ended signals.

Single-ended Signal: A single-ended signal is one measured with respect to a fixed potential, usually ground.



The single-ended ac signal v_{in} sits on a DC bias voltage V_{BIAS} . The DC voltage on which an ac signal sits is also known as the '**common-mode voltage**' of the ac signal.

We define the ac value (e.g. amplitude, rms or peak-peak value) of the signal as its value with respect to the ac ground V_{BIAS}

The amplifier cannot distinguish between change in v_{in} and V_{BIAS} and will amplify both.

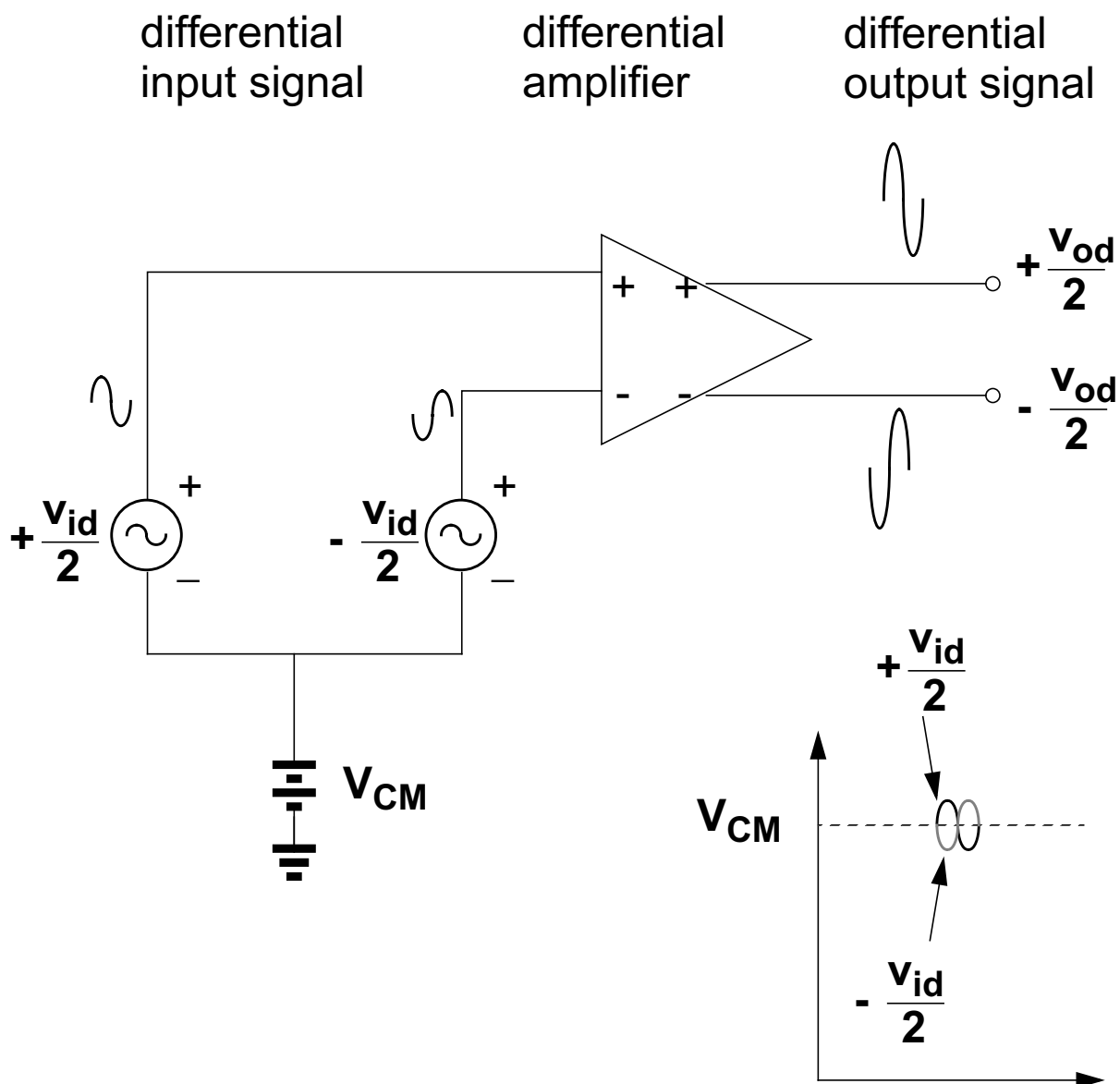
(Equally any ground or other disturbance will be amplified)

Amplifier has no 'common-mode rejection'

Differential signal: A differential signal is measured between 2 nodes that have equal and opposite transitions around a fixed potential.

That fixed potential is called the **common-mode voltage**

The differential signal consists of 2 separate components or half-signals with equal amplitude but opposite phase.



Differential amplifiers are designed to amplify the differential signal but not to react to changes in the common mode voltage. This property is known as **common-mode rejection**.

The **amplitude** of a differential signal is the difference between its two half-signals

$$v_{id} = \frac{v_{id}}{2} - \left(-\frac{v_{id}}{2}\right)$$

$$v_{od} = \frac{v_{od}}{2} - \left(-\frac{v_{od}}{2}\right)$$

For example if each half-signal has a peak-peak amplitude of 500mVpp, then the total signal amplitude is 1Vpp.

We define 2 separate gains for differential amplifiers:

The **differential gain** is defined as the change in the differential output signal for a given change in differential input signal

$$A_{dm}|_{v_{cm}=0} = \frac{v_{od}}{v_{id}}$$

The **common-mode gain** is defined as the change in the common mode output voltage for a given change in common-mode input voltage

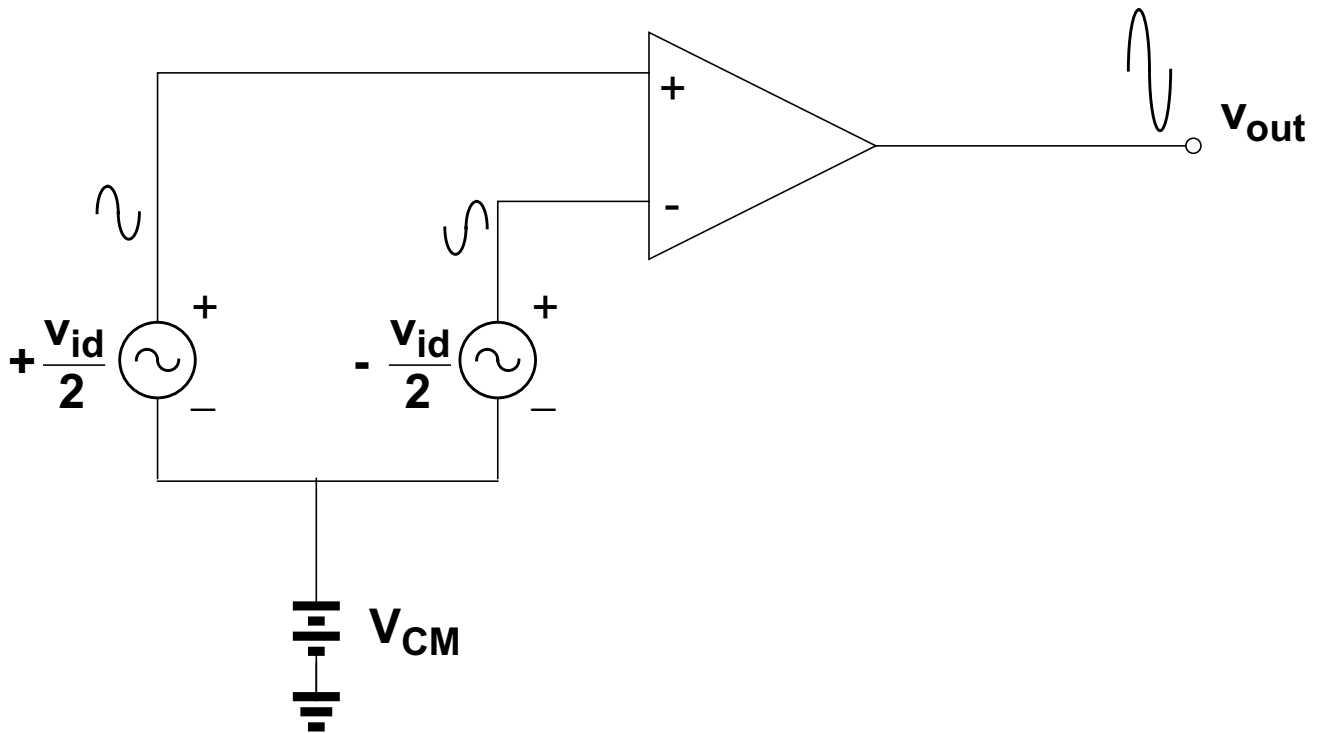
$$A_{cm}|_{v_{id}=0} = \frac{v_{ocm}}{v_{cm}}$$

The **common-mode rejection** ratio is defined as the ratio of the differential gain to the common-mode gain and is a figure of merit for differential amplifiers.

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right|$$

Differential to single-ended amplifiers

Not all differential amplifiers have differential outputs, some convert a differential input signal to a single-ended output signal.

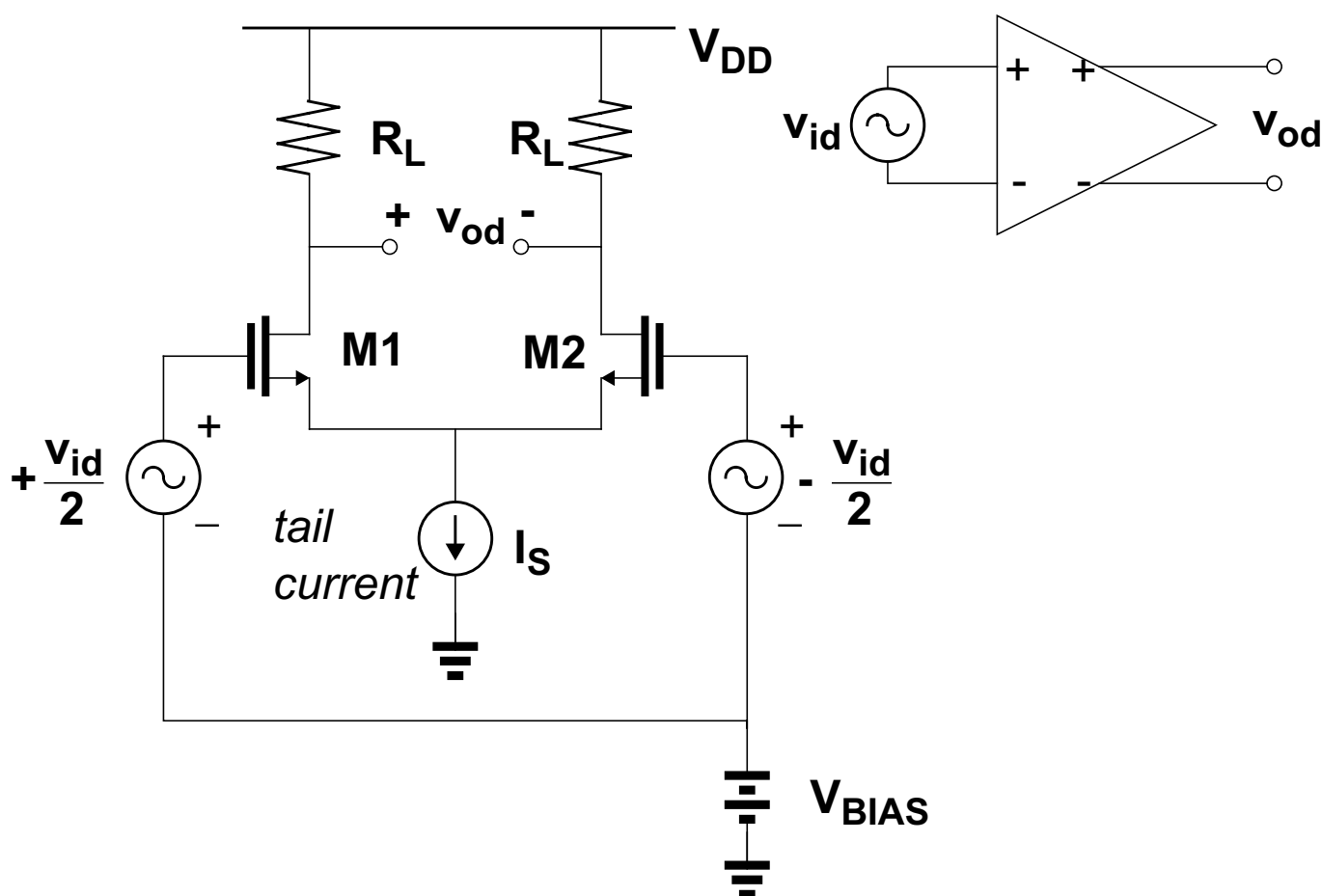


$$A_{dm}|_{v_{cm}=0} = \frac{v_{out}}{v_{id}}$$

$$A_{cm}|_{v_{id}=0} = \frac{v_{ocm}}{v_{cm}}$$

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right|$$

6.2 Differential Gain stage



M1, M2 share the bias current, often called the tail current. In the quiescent state (i.e. with the differential signals equal to zero) half the current flows through each transistor.

M1, M2 have a common source - the tail node

The input signal is differential

V_{BIAS} sets the common-mode voltage

Note that (if the current source is ideal) a change in the common-mode voltage will not change the bias current I_S and so will not change the output common-mode (infinite CMRR).

In practice the CMRR will be determined by the quality of this current source.

6.2.1 Differential gain stage - Small-signal behaviour

How does the circuit react to a small-differential input signal?

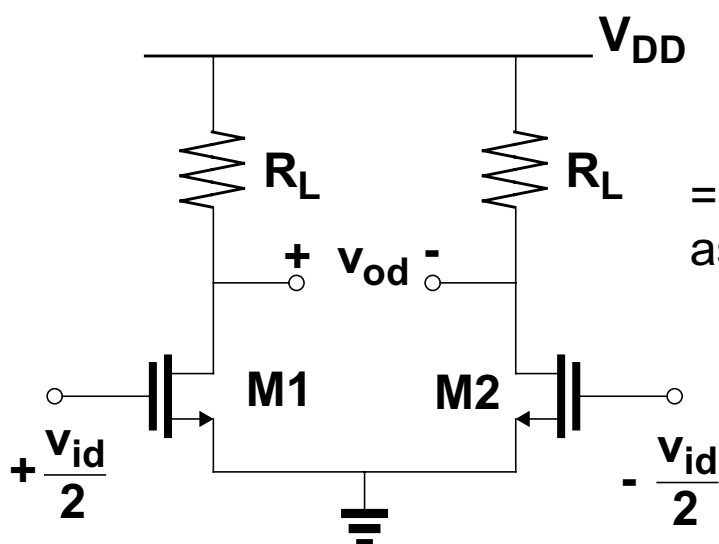
Consider a small positive voltage increment on the positive input and an equal negative change on the negative input

If we consider the transistors to behave linearly for small signals, and given that the sum of the two currents will stay the same there will be an increase in current in M1 and an equal decrease in current in M2.

What happens to the dc voltage at the common source node?

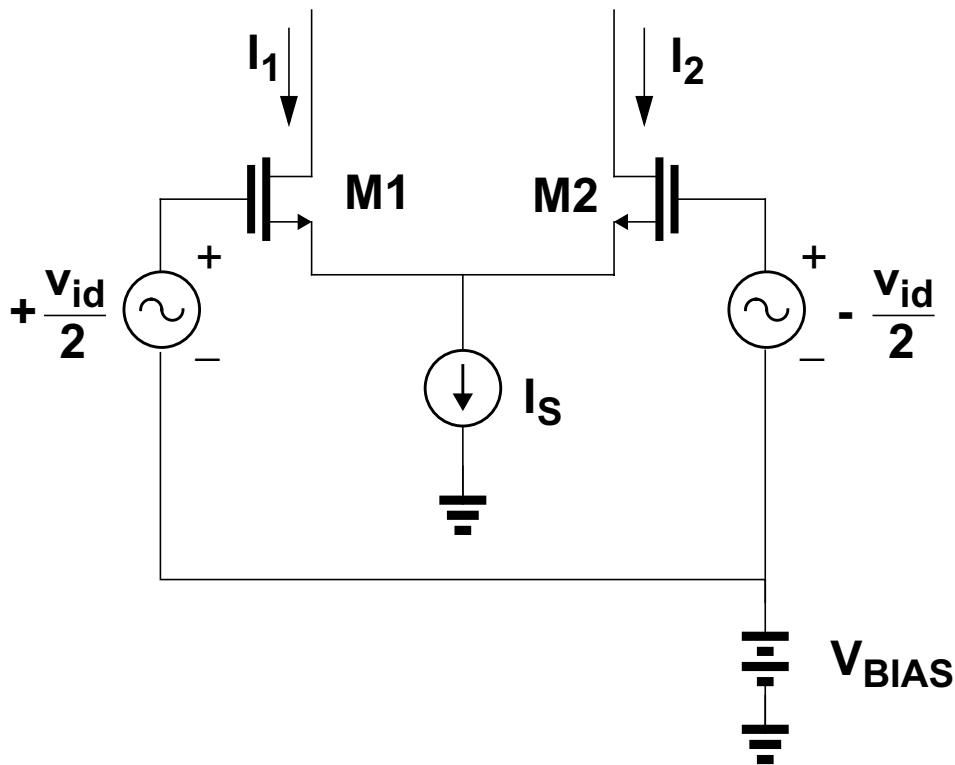
The increase in current in M1 means an increase in V_{GS1} , with an equal decrease in V_{GS2} . The only way this can happen is for the common source node to stay at the same potential.

As it does not change potential we can consider it an ac ground.



For small-signal inputs
the tail node does not move
=> we can treat tail node
as a small signal (ac) ground

6.2.2 Differential stage : Large signal transfer function



We are interested in the transfer function *of the input differential voltage to the output differential currents* i.e. from v_{id} to I_1 - I_2

Assume circuit symmetrical, $M1=M2$, both in saturation.
Ignore body effect, output conductance.

$$V_{GS1} - V_t = A$$

$$V_{GS2} - V_t = B$$

$$V_{GS1} - V_{GS2} = A - B = v_{id}$$

$$I_1 = \frac{K'_n W}{2L} A^2$$

$$I_2 = \frac{K'_n W}{2L} B^2$$

$$I_1 + I_2 = \frac{K'_n W}{2L} (A^2 + B^2) = I_S$$

$$I_1 - I_2 = \frac{K'_n W}{2L} (A^2 - B^2) = \frac{K'_n W}{2L} (A + B)(A - B)$$

Differential stage : Large signal transfer function (contd.)

$$I_1 - I_2 = \frac{K'_n W}{2L} (A^2 - B^2) = \frac{K'_n W}{2L} (A + B)(A - B)$$

want to get this in terms of $(A^2 + B^2)$ and $A - B$

Use

$$(A + B)^2 = 2(A^2 + B^2) - (A - B)^2$$

$$(A + B) = \sqrt{2(A^2 + B^2) - (A - B)^2}$$

$$I_1 - I_2 = \frac{K'_n W}{2L} (A - B) \sqrt{2(A^2 + B^2) - (A - B)^2}$$

$$I_1 - I_2 = \frac{K'_n W}{2L} v_{id} \sqrt{\frac{4I_S}{K'_n \frac{W}{L}} - v_{id}^2}$$

This is valid for
$$-\sqrt{\frac{2I_S}{K'_n \frac{W}{L}}} < v_{id} < \sqrt{\frac{2I_S}{K'_n \frac{W}{L}}}$$

Outside this: $I_1 = 0$ and $I_2 = I_S$ or $I_2 = 0$ and $I_1 = I_S$

Differential stage : Large signal transfer function (contd.)

Transfer function

$$I_1 - I_2 = \frac{K'_n W}{2L} v_{id} \sqrt{\frac{4I_S}{K'_n \frac{W}{L}} - v_{id}^2}$$

Note

1. Quiescent Overdrive voltage $V_{GS} - V_t$ (when $v_{id} = 0$) is given by

$$V_{GS} - V_t = \sqrt{\frac{I_S}{K'_n \frac{W}{L}}}$$

2. Transfer function is approx. linear for small v_{id} i.e for

$$v_{id}^2 \ll \frac{4I_S}{K'_n \frac{W}{L}}$$

3. Range of input voltage for which transfer function is linear is determined by quiescent value of $V_{GS} - V_t$

Increase $V_{GS} - V_t \rightarrow$ Increase linear input range

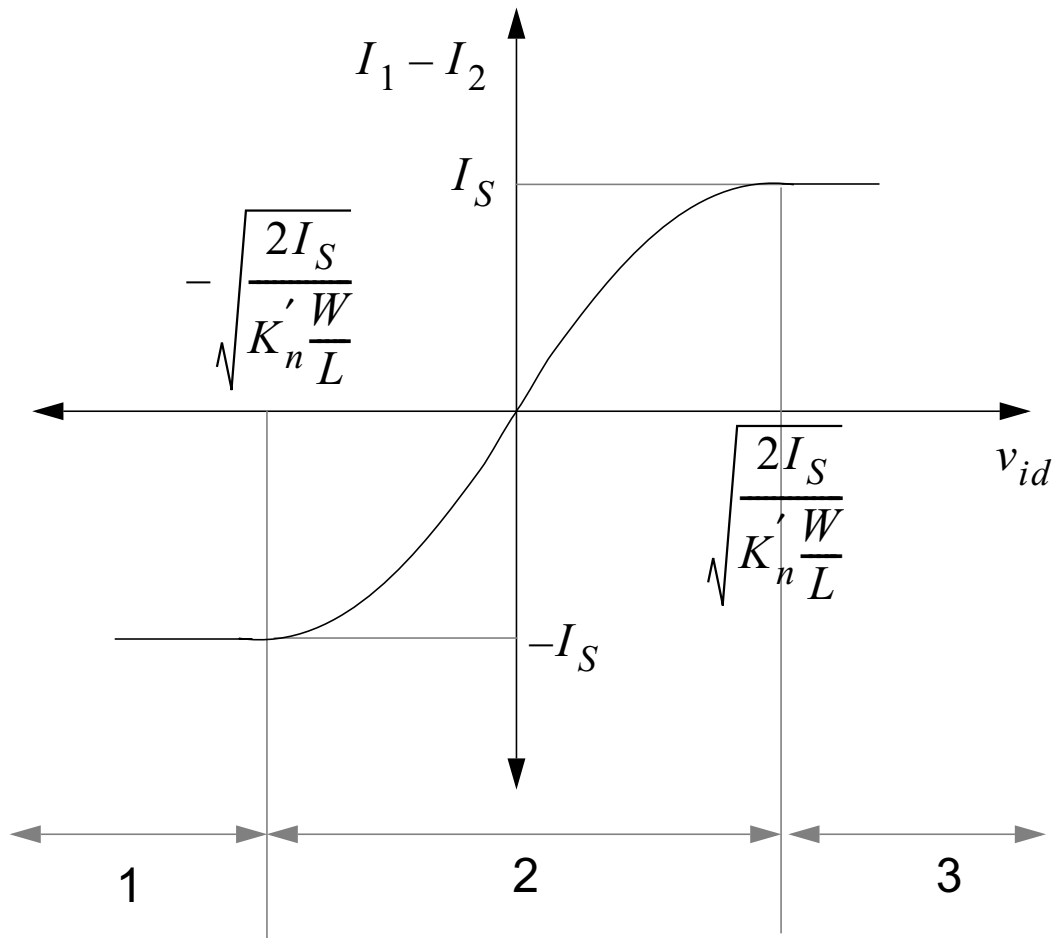
3. It can be shown than for a sine-wave input of amplitude V_m

$$THD = \frac{V_m^2}{32(V_{GS} - V_t)^2}$$

If $V_m = 0.2(V_{GS} - V_t)$ then

$$THD = \frac{0.2^2 (V_{GS} - V_t)^2}{32(V_{GS} - V_t)^2} = 0.125 = -58dB$$

Differential stage : Large signal transfer function (contd.)



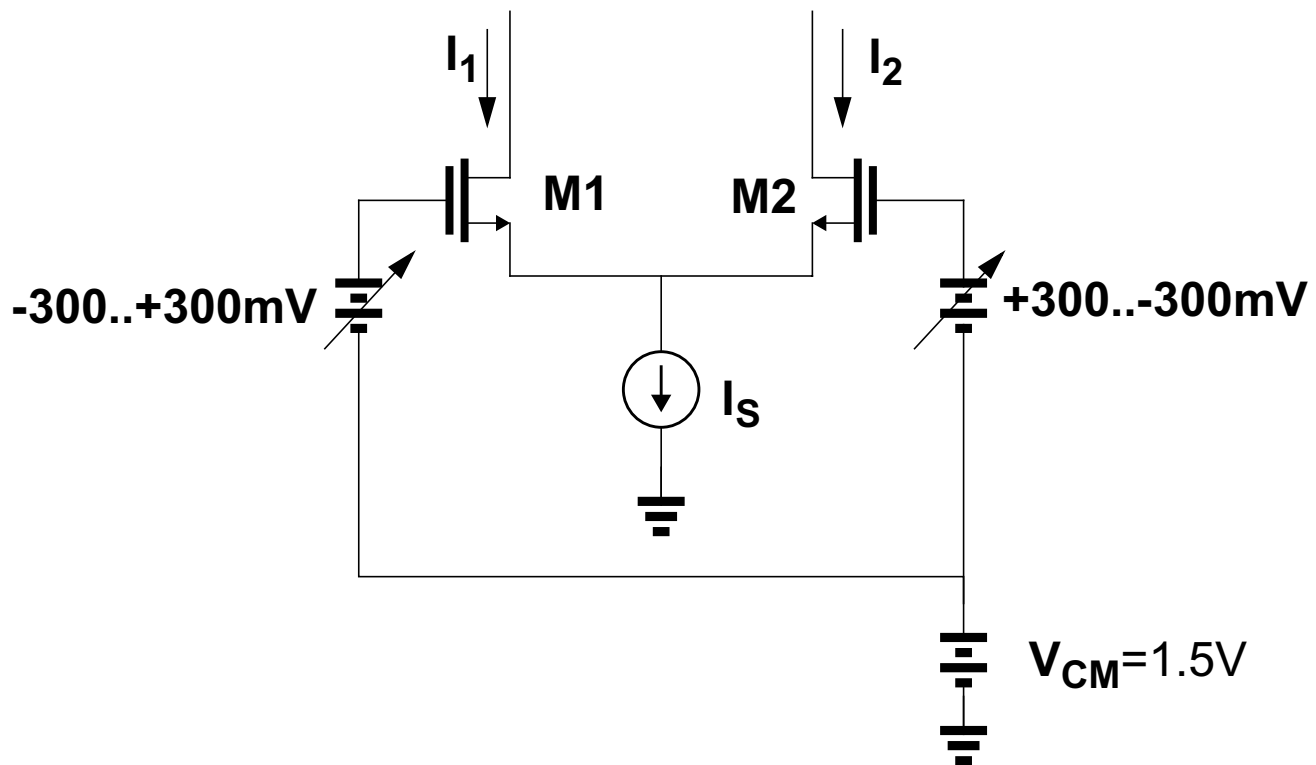
3 regions of operation

$$1 \quad I_1 - I_2 = -I_S \quad v_{id} < -\sqrt{\frac{2I_S}{K_n' \frac{W}{L}}}$$

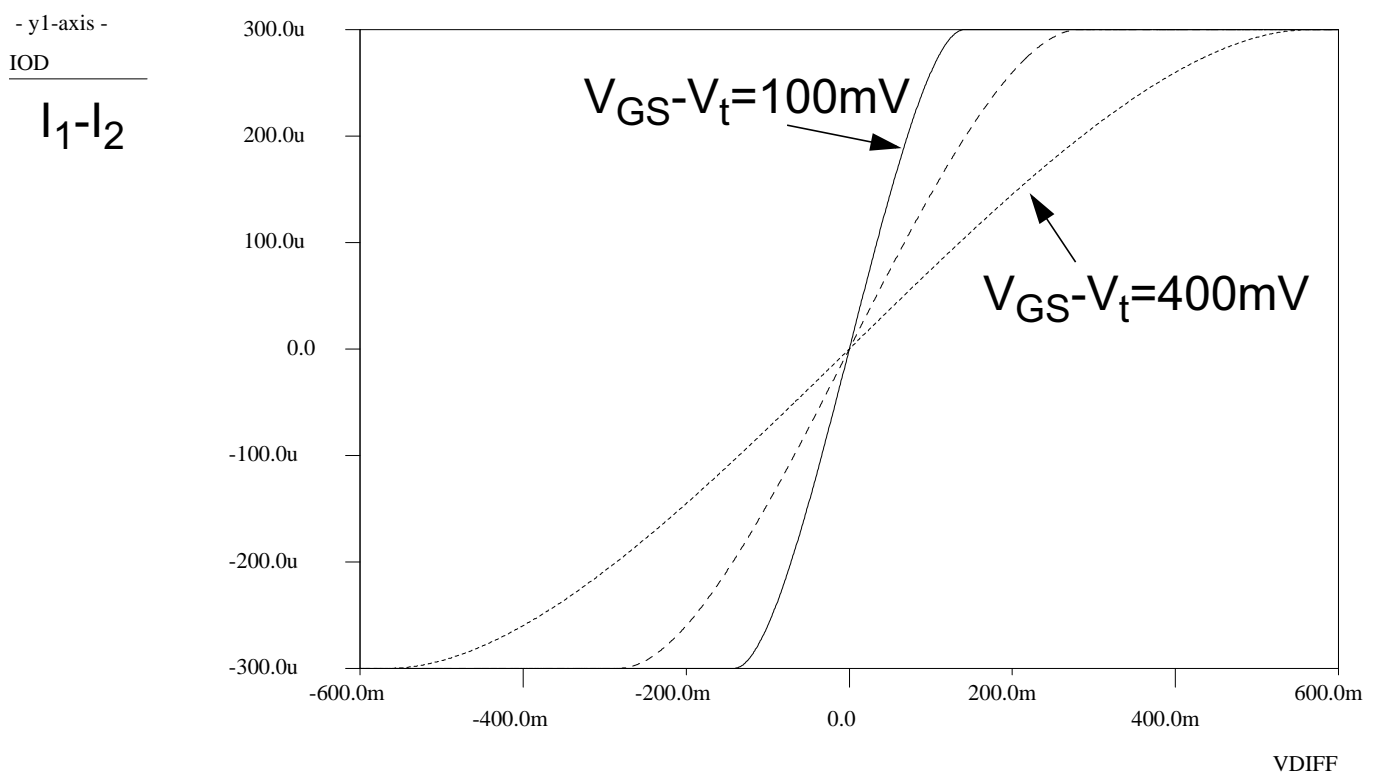
$$2 \quad I_1 - I_2 = \frac{K_n' W}{2L} v_{id} \sqrt{\frac{4I_S}{K_n' \frac{W}{L}} - v_{in}^2} \quad -\sqrt{\frac{2I_S}{K_n' \frac{W}{L}}} < v_{id} < \sqrt{\frac{2I_S}{K_n' \frac{W}{L}}}$$

$$3 \quad I_1 - I_2 = I_S \quad v_{id} > \sqrt{\frac{2I_S}{K_n' \frac{W}{L}}}$$

Differential Gain stage-Input voltage ramp



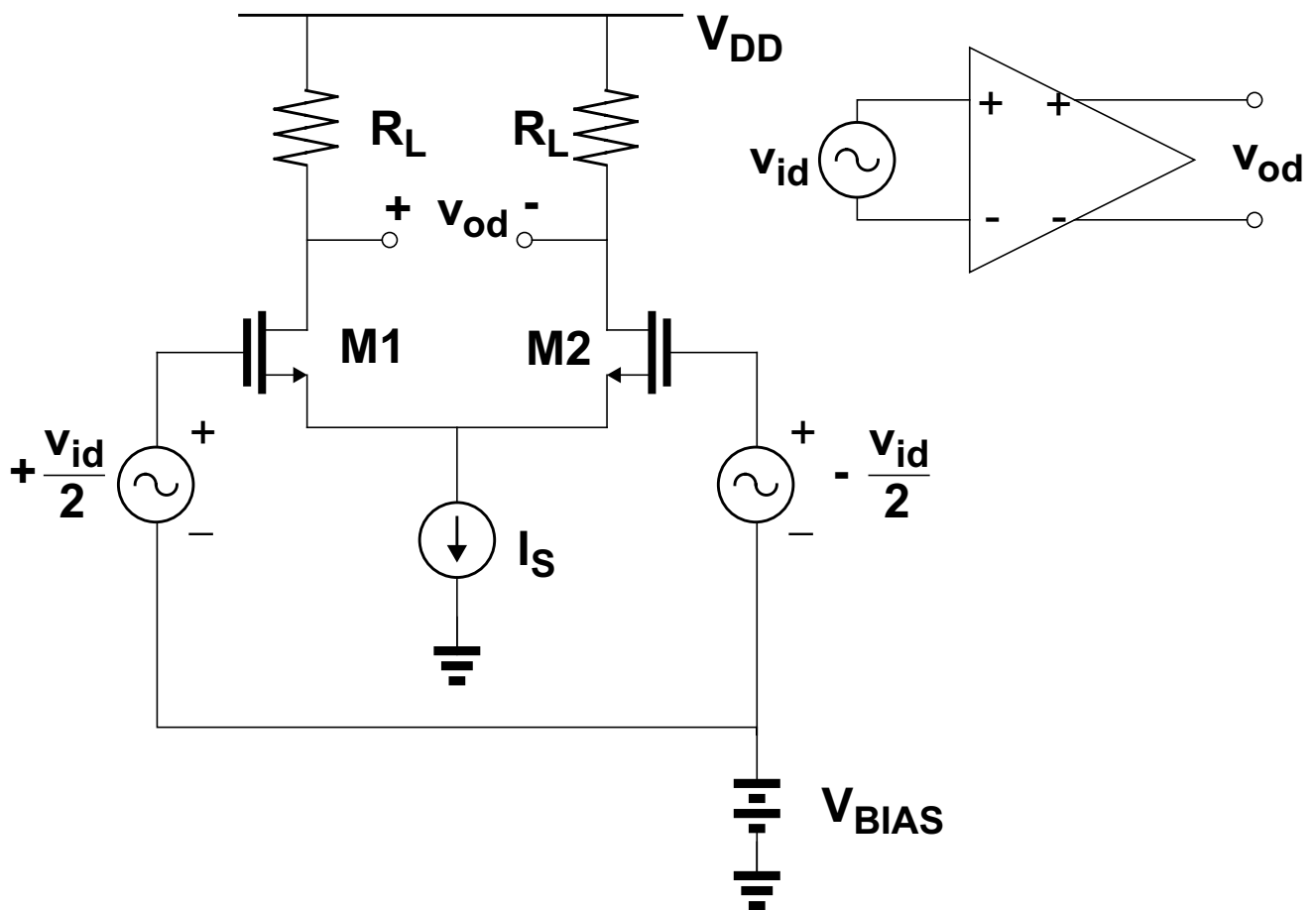
Look at response to differential voltage ramp at input
(Simulation using $K_n' = 150 \mu\text{A}/\text{V}^2$, $I_S = 300 \mu\text{A}$, $V_{GS} - V_t = 0.1, 0.2, 0.4 \text{V}$)



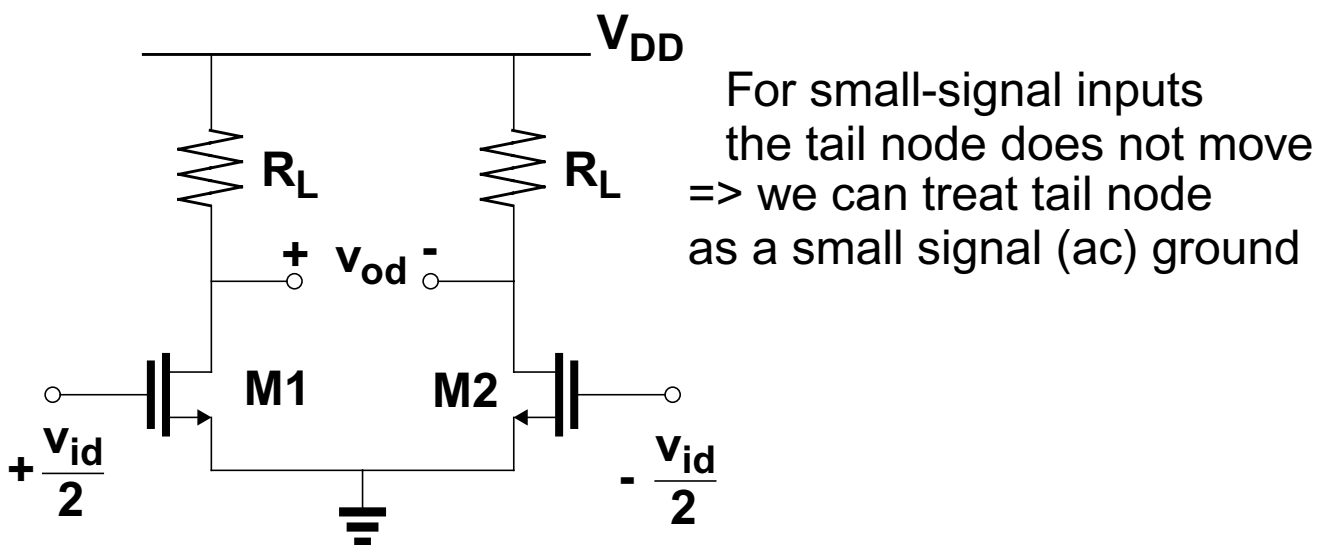
=> Dimension $V_{GS} - V_t$ according to maximum input signal and linearity requirements

6.2.3 Differential Gain stage-small signal analysis

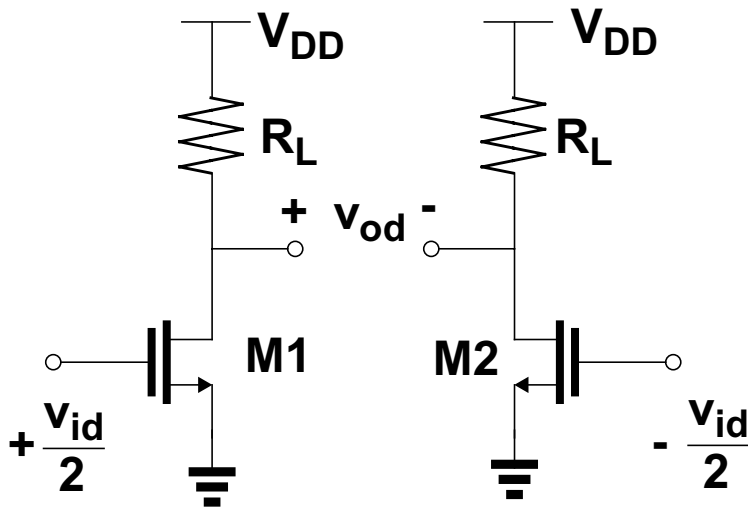
Take the differential stage with resistive load.



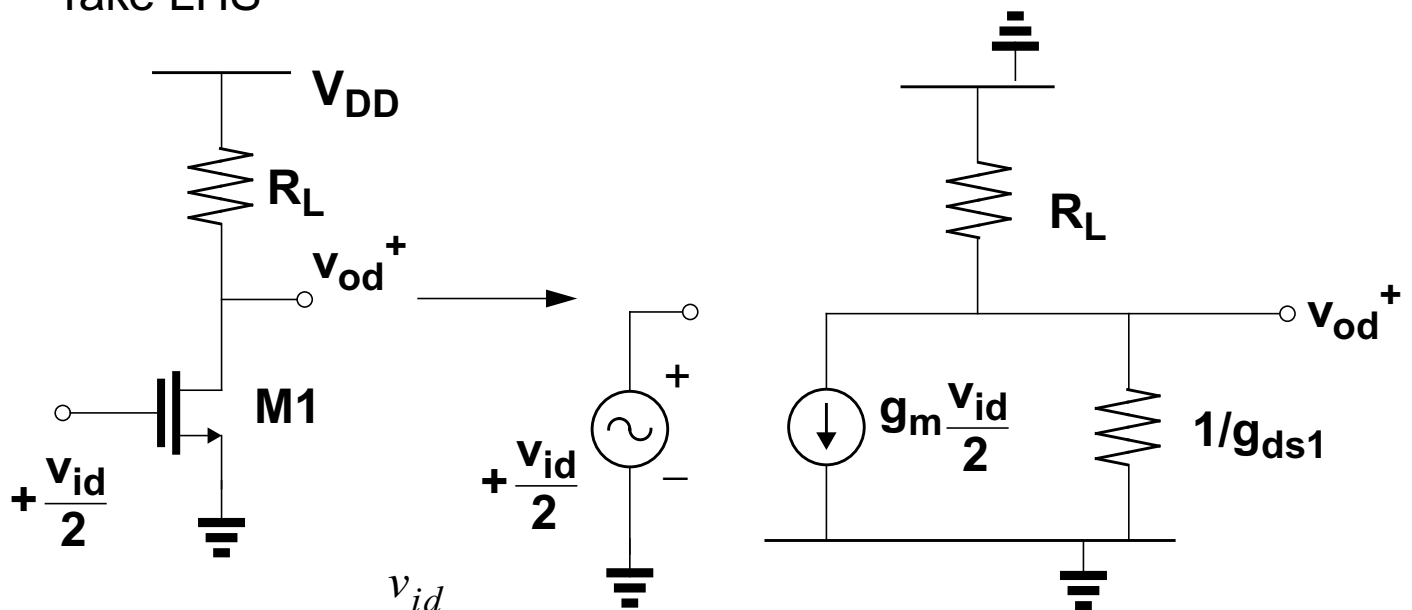
For small-signal analysis we can treat the tail node as a small signal ground



The circuit is symmetrical => We can split it into two identical halves



Take LHS



$$v_{od}^+ = -\frac{g_{m1} \frac{v_{id}}{2}}{g_{ds1} + \frac{1}{R_L}}$$

$$v_{od} = v_{od}^+ - v_{od}^- = -\frac{g_{m1} \frac{v_{id}}{2}}{g_{ds1} + \frac{1}{R_L}} - \left(-\frac{g_{m2} \left(-\frac{v_{id}}{2} \right)}{g_{ds2} + \frac{1}{R_L}} \right)$$

Assume M1=M2

$$v_{od} = -\frac{g_m}{g_{ds} + \frac{1}{R_L}} v_{id} \quad A_{dm} = \frac{v_{od}}{v_{id}} = -\frac{g_m}{g_{ds} + \frac{1}{R_L}} \approx -g_m R_L$$

assuming R_L dominates

6.2.4 Differential gain stage - Common-mode response

The common mode response is the change in common-mode output voltage for a given change in the common mode input voltage.

Note that the common-mode output voltage (i.e. the voltage at the output nodes when the differential input signal is zero) is

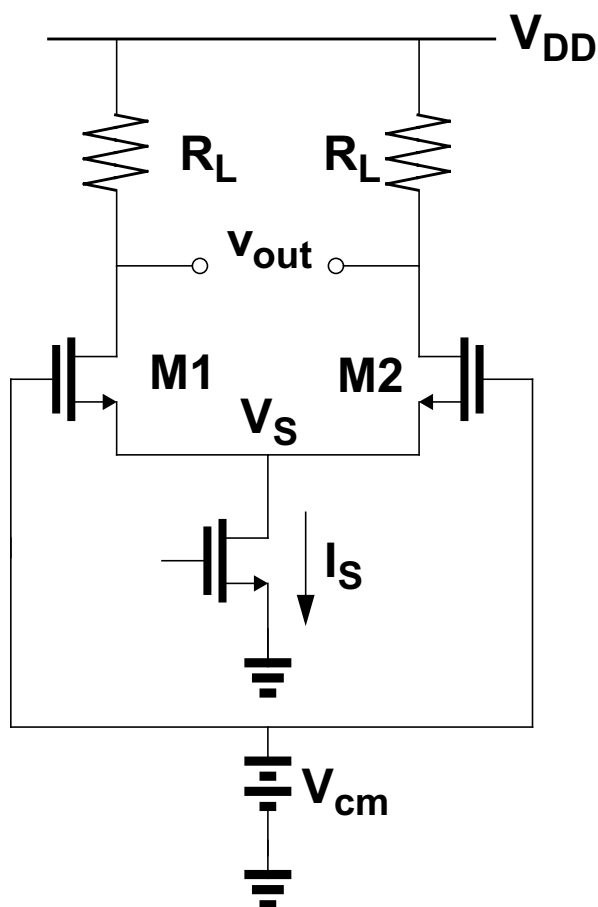
$$V_{OC} = V_{DD} - \frac{I_S}{2} R_L$$

Increase input common-mode voltage V_{CM}

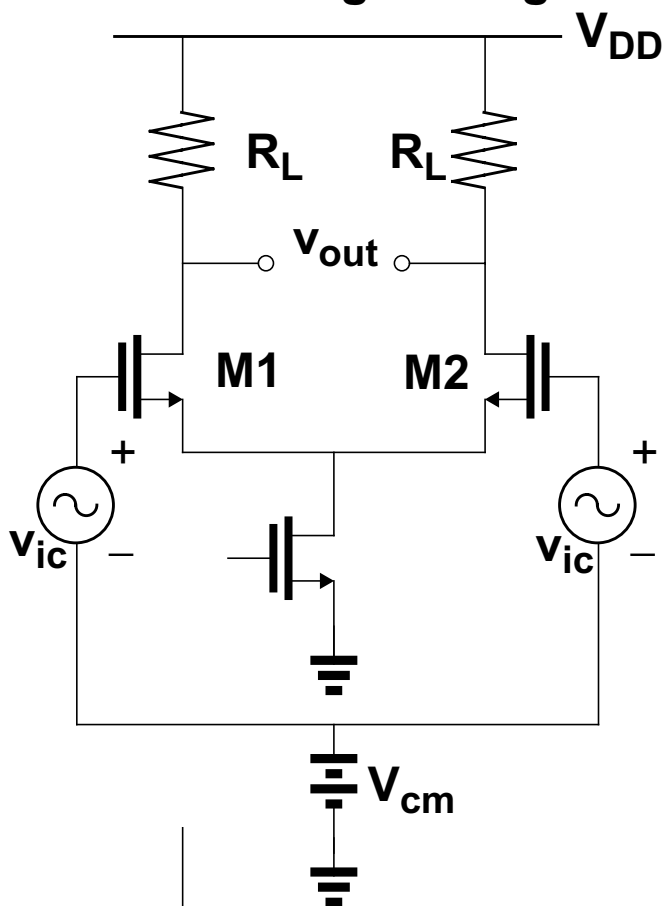
V_S will follow V_{CM}

I_S will increase due to finite output impedance of current source

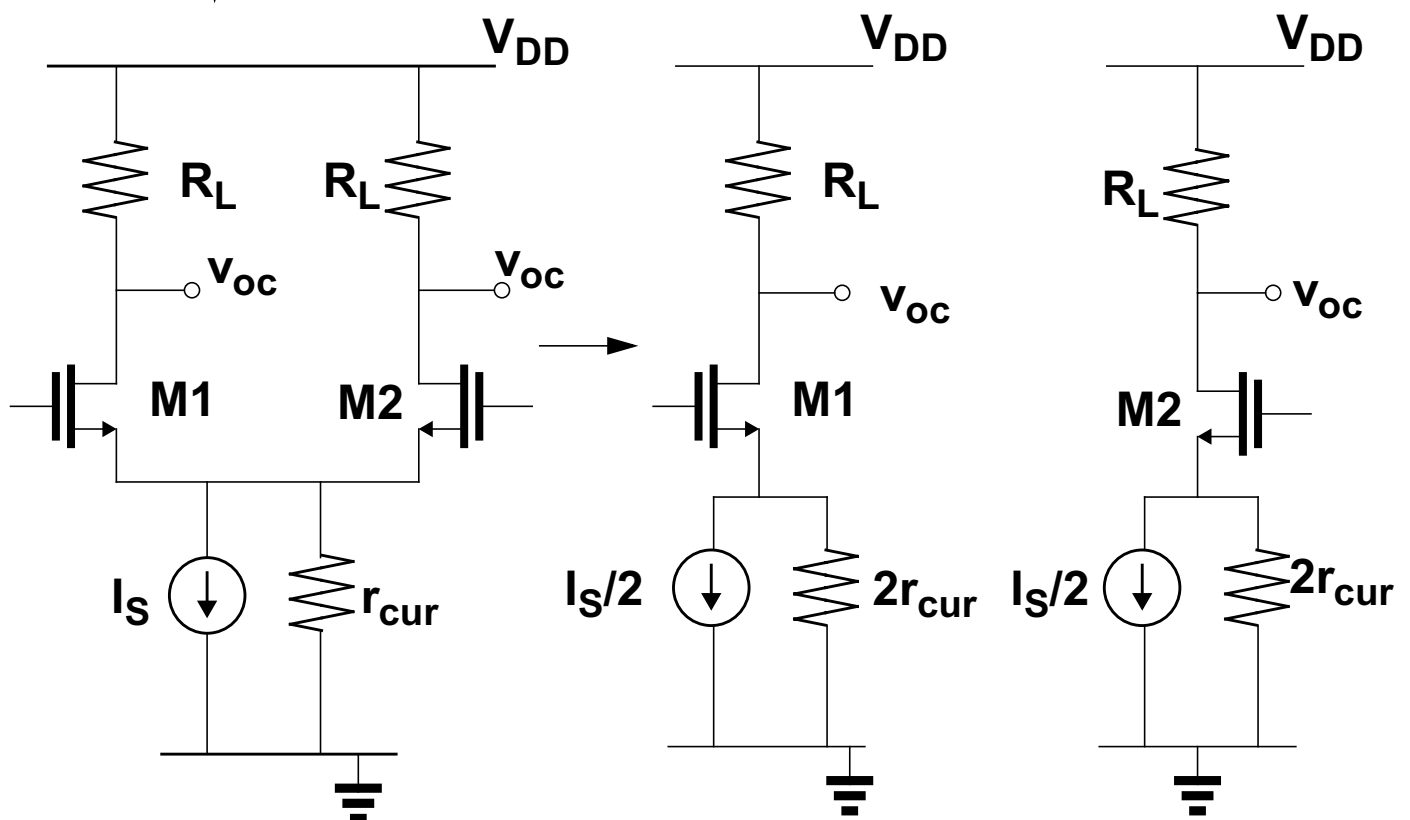
Output common-mode level decreases



6.2.5 Differential gain stage- CM response (analysis)



Apply a small common mode voltage signal to both inputs and calculate output voltage change.

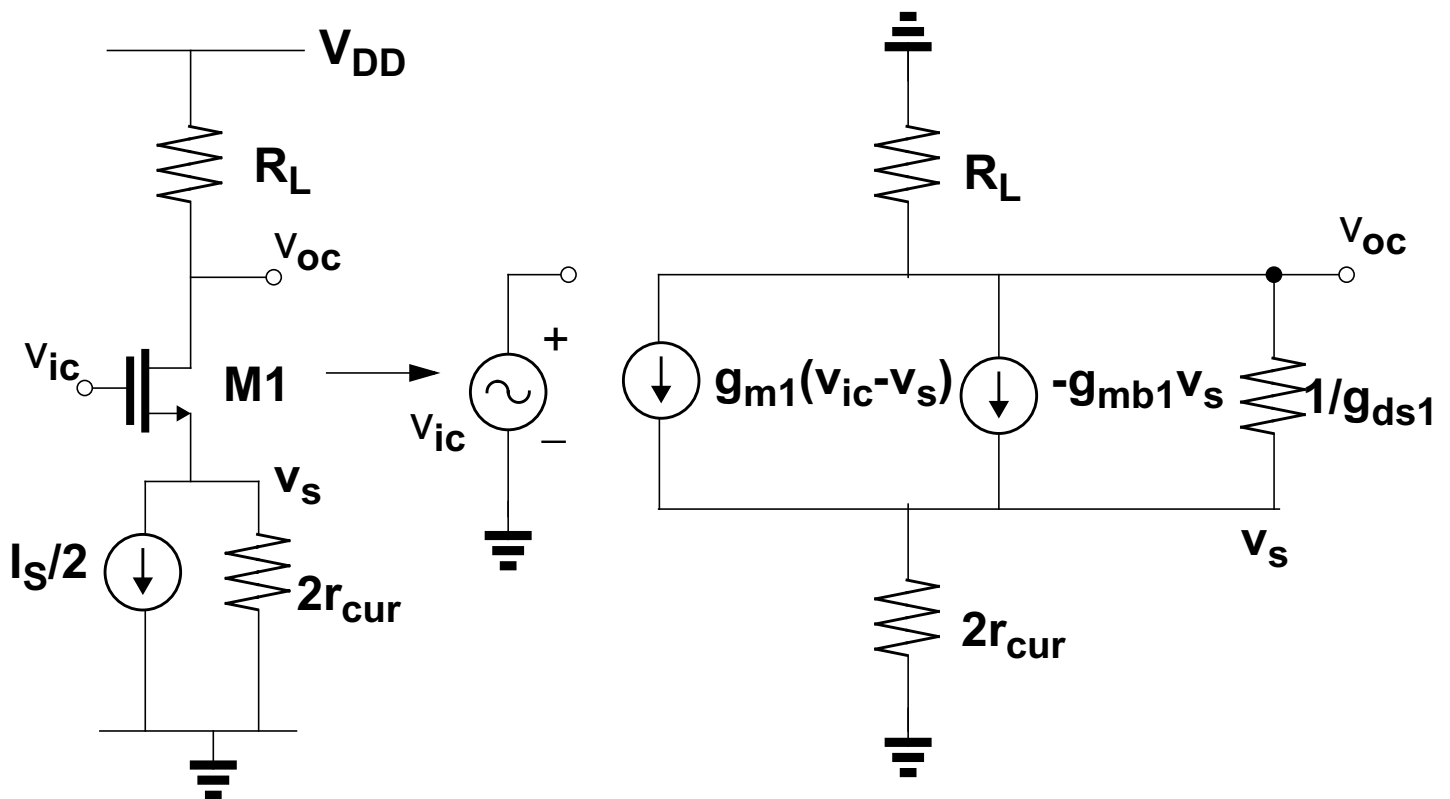


Equivalent circuit for tail current source

Split into identical half circuits

Differential gain stage- Common-mode response (analysis)

Same thing happens to both circuits so just look at one side



This is a common source stage with resistive degeneration
From analysis on P. 116 (with $R_S = 2R_{cur}$)

$$A_{cm} = \frac{v_{oc}}{v_{ic}} = -\frac{g_m R_L}{1 + (g_m + g_{mb})2R_{cur} + g_{ds}2R_{cur} + g_{ds}R_L}$$

Simplifying this

$$A_{cm} = \frac{v_{oc}}{v_{ic}} = -\frac{g_m R_L}{1 + (g_m + g_{mb})2R_{cur} + g_{ds}R_L}$$

Simplify further assuming $(g_m + g_{mb})2R_{cur} \gg g_{ds}R_L$
and ignoring body effect

$$A_{cm} = \frac{v_{oc}}{v_{ic}} \approx -\frac{R_L}{2R_{cur}}$$

6.2.6 Common Mode Rejection ratio

The common-mode rejection ratio is a figure of merit for differential amplifiers. It is defined as

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right|$$

$$A_{dm} = -g_m R_L$$

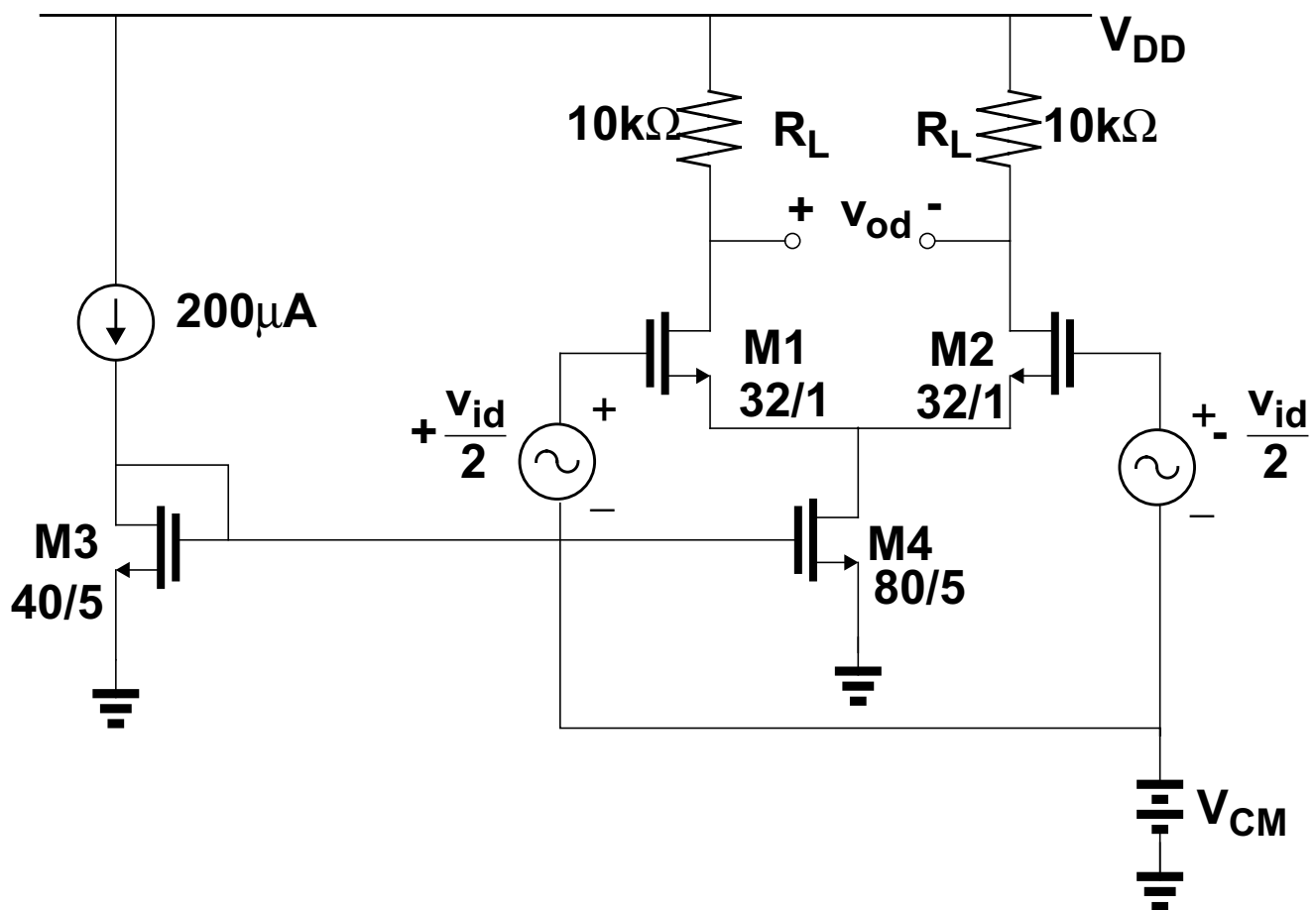
$$A_{cm} = -\frac{R_L}{2R_{cur}}$$

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right| = \frac{-g_m R_L}{-\frac{R_L}{2R_{cur}}} = 2g_m R_{cur}$$

To maximise CMRR:

large g_m

large r_{cur} (e.g. cascode the tail current source).



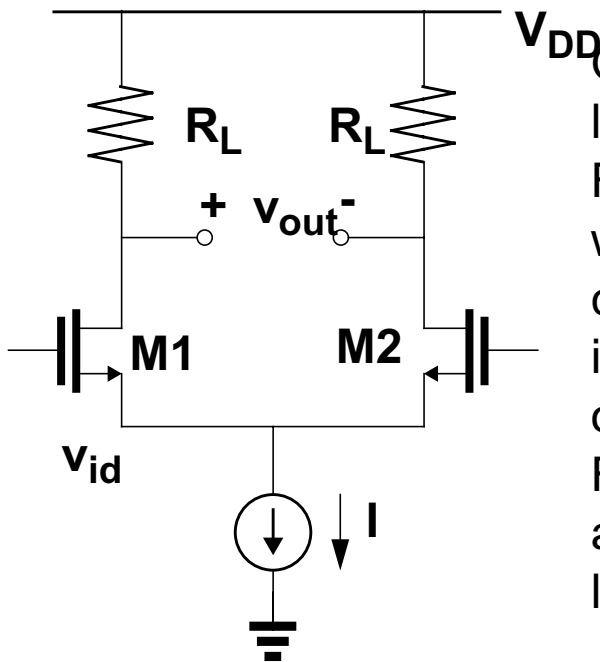
- (i) What is the allowed range of the common-mode input voltage (i.e. the range in the quiescent state such that all transistors remain in saturation)?
- (ii) What is the value of the differential gain?
- (iii) What is the value of the common-mode gain?
- (iv) What is the CMRR?

$$V_{DD}=3.3V$$

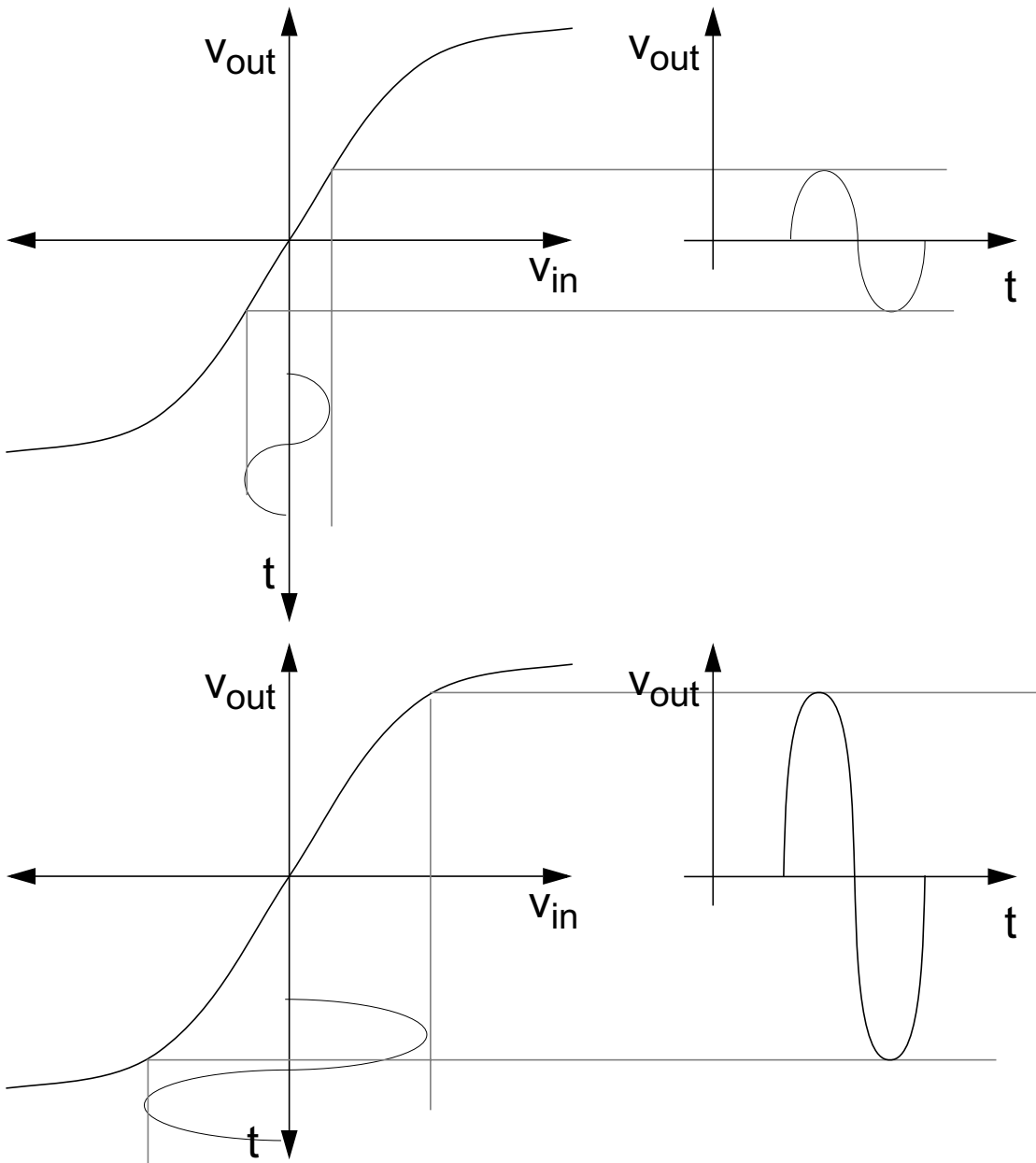
$$V_t=1V, \lambda_n=0.04/L \text{ V}^{-1}$$

$$K_n' = 200 \mu A/V$$

6.3 Non-Linearity of the differential pair

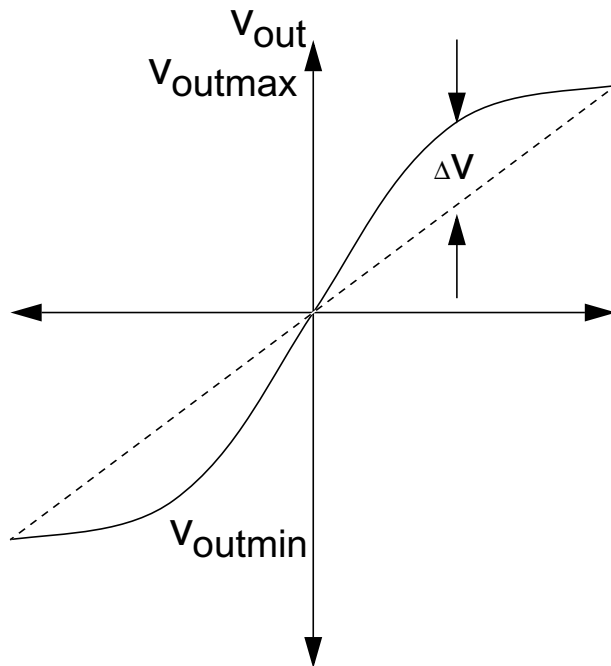


Our small signal analysis assumes linear transconductances
 For larger signals the slope of i_{out}/v_{in} will vary, so that an incremental change in v_{in} will result in a different incremental change in i_{out} depending on the input dc level.
 For example for the differential amplifier the output will saturate for large input signal swings.



6.3.1 Background: Quantification of non-linearity

1. Percentage deviation for straight line



Non-linearity expressed as the maximum deviation of the output characteristic from a straight line
i.e. in example above

$$Nonlinearity = \frac{\Delta v}{v_{outmax} - v_{inmax}}$$

Usually expressed as a percentage

Background: Quantification of non-linearity (contd.)

2. Harmonic content

Apply a sine wave at the input and measure the harmonic content at the output.

Note: for small non-linearities i/o characteristic can be approximated by a Taylor expansion:

$$v_{out}(t) = \alpha_1 v_{in}(t) + \alpha_2 v_{in}^2(t) + \alpha_3 v_{in}^3(t) + \dots$$

Usually the first few terms are dominant

For a sine wave input

$$v_{in}(t) = A \cos \omega t$$

$$v_{out}(t) = \alpha_1 A \cos \omega t + \alpha_2 A^2 \cos^2 \omega t + \alpha_3 A^3 \cos^3 \omega t + \dots$$

$$v_{out}(t) = \alpha_1 A \cos \omega t + \frac{\alpha_2 A^2}{2} (1 + \cos 2\omega t) + \frac{\alpha_3 A^3}{4} (3 \cos \omega t + \cos 3\omega t) +$$

Note that higher-order terms give higher harmonics

In general even-order terms give even harmonics and odd-order terms give odd-order harmonics

Also magnitude of nth harmonic grows with the nth power of the input signal amplitude

Harmonic distortion is usually expressed as the ratio of the sum of the power of all non-fundamental harmonics to the power of the fundamental-> **Total Harmonic Distortion**

e.g. if the second and third harmonics are dominant then

$$THD = \frac{\left(\frac{\alpha_2 A^2}{2}\right)^2 + \left(\frac{\alpha_3 A^3}{4}\right)^2}{\left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)^2}$$

For CD, digital audio : require THD of about -80dB (0.01%)
video: -60dB (0.1%)

6.3.2 Non-linearity of a differential pair (analysis)

$$I_{D1} - I_{D2} = K'_n \frac{W}{L} (V_{GS} - V_t) \left(v_{id} - \frac{v_{id}^3}{8(V_{GS} - V_t)^2} \right)$$

For a sine wave input $v_{id}(t) = V_m \cos \omega t$

$$I_{D1} - I_{D2} = K'_n \frac{W}{L} (V_{GS} - V_t) \left(V_m \cos \omega t - \frac{V_m^3 \cos^3 \omega t}{8(V_{GS} - V_t)^2} \right)$$

$$\cos^3 \omega t = \frac{(3 \cos \omega t + \cos 3 \omega t)}{4}$$

$$I_{D1} - I_{D2} = K'_n \frac{W}{L} (V_{GS} - V_t) \left(V_m \cos \omega t - \frac{V_m^3 (3 \cos \omega t + \cos 3 \omega t)}{32(V_{GS} - V_t)^2} \right)$$

$$\text{If } V_m \gg \frac{3V_m^3}{32(V_{GS} - V_t)^2}$$

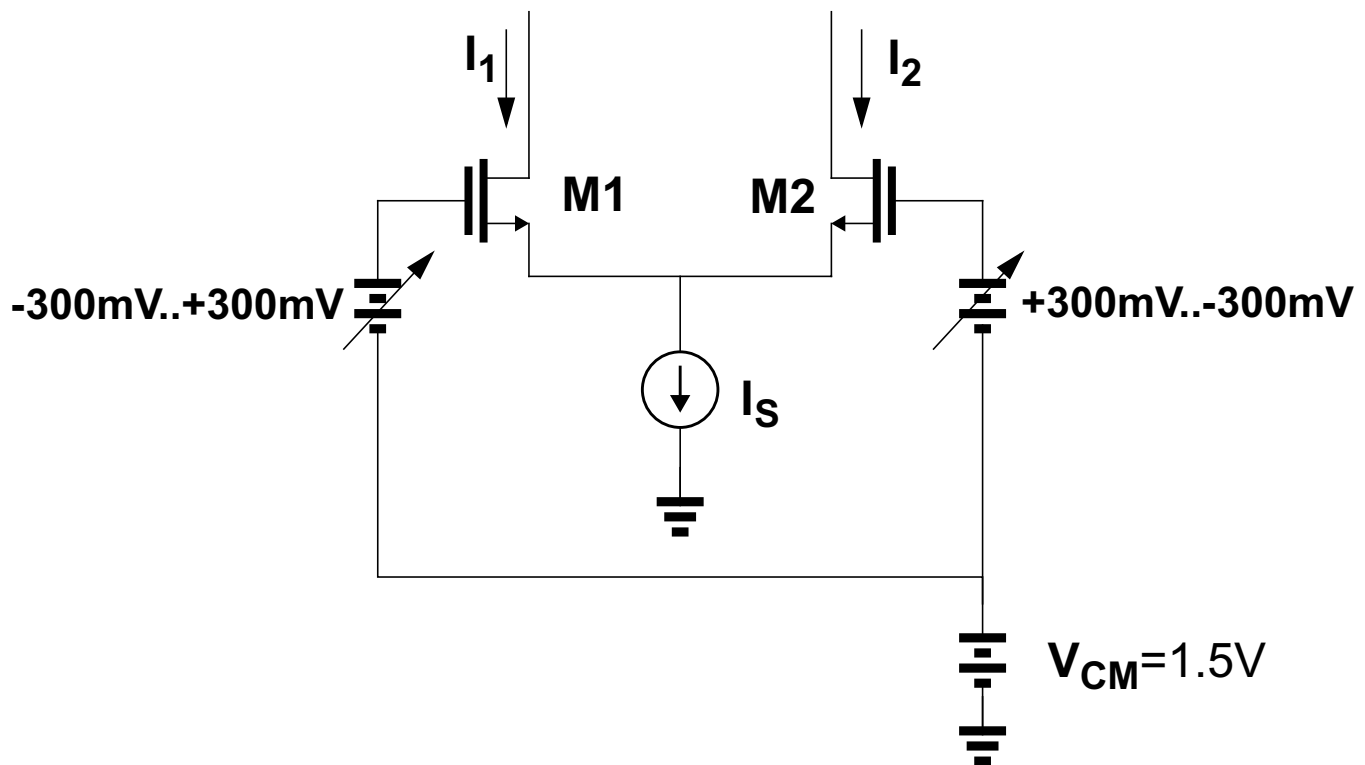
$$\text{then } THD = \frac{V_m^2}{32(V_{GS} - V_t)^2} \quad \text{i.e the ratio of the third harmonic to the first (fundamental).}$$

If $V_m = 0.2(V_{GS} - V_t)$ then

$$THD = \frac{0.2^2 (V_{GS} - V_t)^2}{32(V_{GS} - V_t)^2} = 0.125\% = -58 \text{ dB}$$

Example: Differential pair P. 187

1. DC simulation



Look at response to differential voltage ramp at input
(Simulation using $K_n' = 150\mu A/V^2$, $I_S = 300\mu A$, $V_{GS} - V_t = 0.1, 0.2, 0.4V$)

Examine voltages, currents for the following case:

Input pair are each 50/1

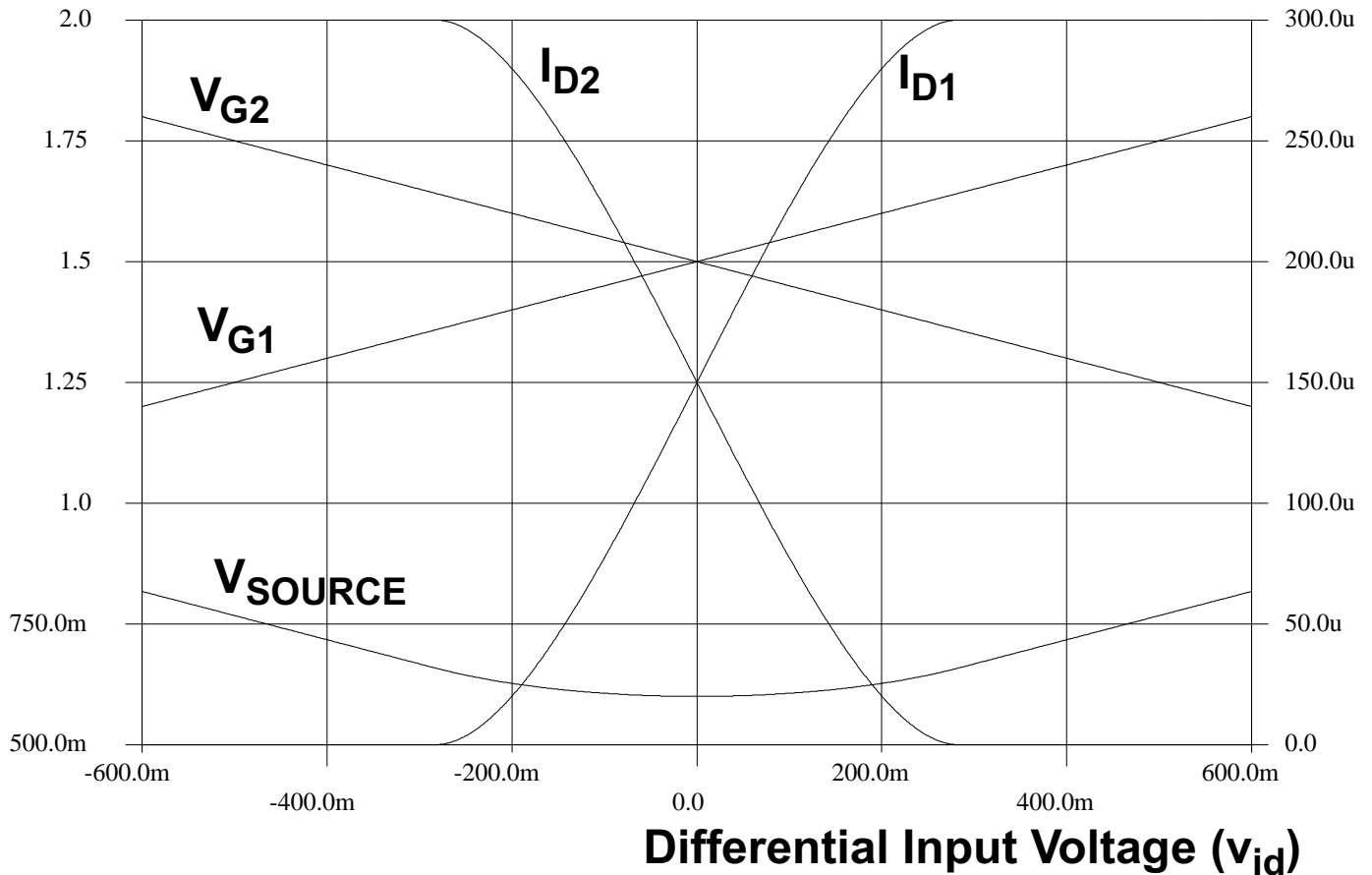
Note: The overdrive voltage when the differential input voltage is zero is given by:

$$V_{GS1} - V_t = \sqrt{\frac{2I_D}{K_n' \frac{W}{L}}} = \sqrt{\frac{2 \cdot 150\mu A}{150\mu A/V^2 \frac{50}{1}}} = 0.2V$$

DC simulation:

Voltage

Current



It can be seen that for small values of v_{id} , the voltage at the common source node V_{SOURCE} is constant.

Note also that the circuit ‘saturates’ when v_{id} is greater than

$$v_{id} > \sqrt{\frac{2I_S}{K'_n \frac{W}{L}}} = \sqrt{\frac{2 \cdot 300\mu A}{150\mu A/V^2 \frac{50}{1}}} = 282.8mV$$

2. Transient simulation

Take the previous circuit, now with a resistive load of $10k\Omega$ to V_{DD} . ($V_{DD}=5V$)

Apply a differential sine wave of amplitude 40mV to the input

What is the gain of circuit?

What is the distortion in output signal.

First: hand calculation

$$Gain \approx -g_m R_L$$

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2 \times 150\mu A}{0.2V} = 1500\mu A/V$$

$$Gain \approx g_m R_L = 1500\mu A/V \times 10k\Omega = 15$$

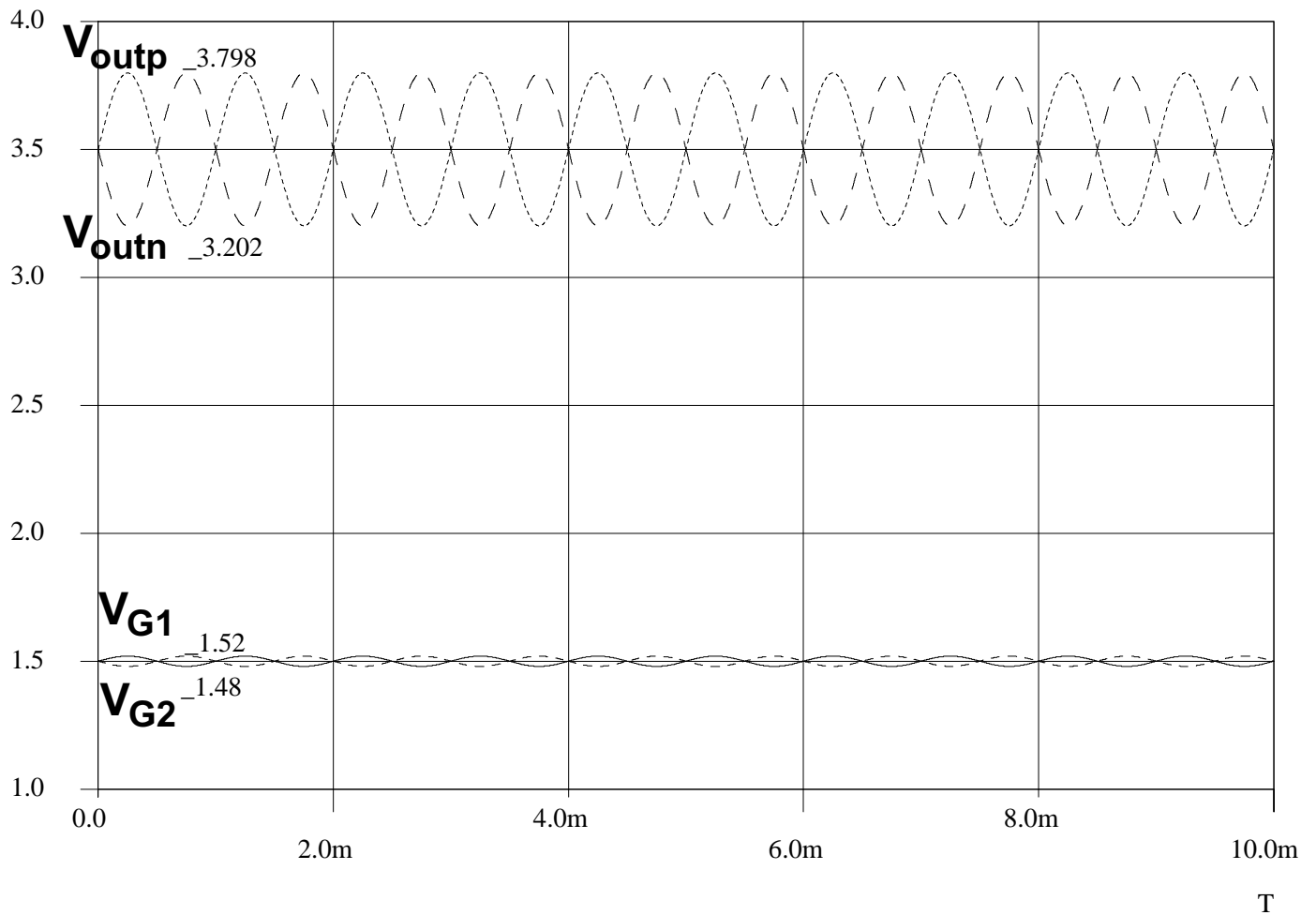
We can also calculate the output common-mode voltage:

$$V_{cmout} = V_{DD} - I_D R_L = 5 - 150\mu A \times 10k\Omega = 3.5V$$

From hand calculations we predict a differential output signal of 600mV, biased around 3.5V

With $V_m=0.2(V_{GS}-V_t)$ we also predict a third harmonic at -58dB w.r.t the signal.

Transient Simulation Results



In the simulation a positive 1kHz sine-wave of amplitude 20mV (superimposed on the common-mode voltage of 1.5V) is applied to the gate of M1, and a negative sine-wave of amplitude 20mV is applied to the gate of M1.

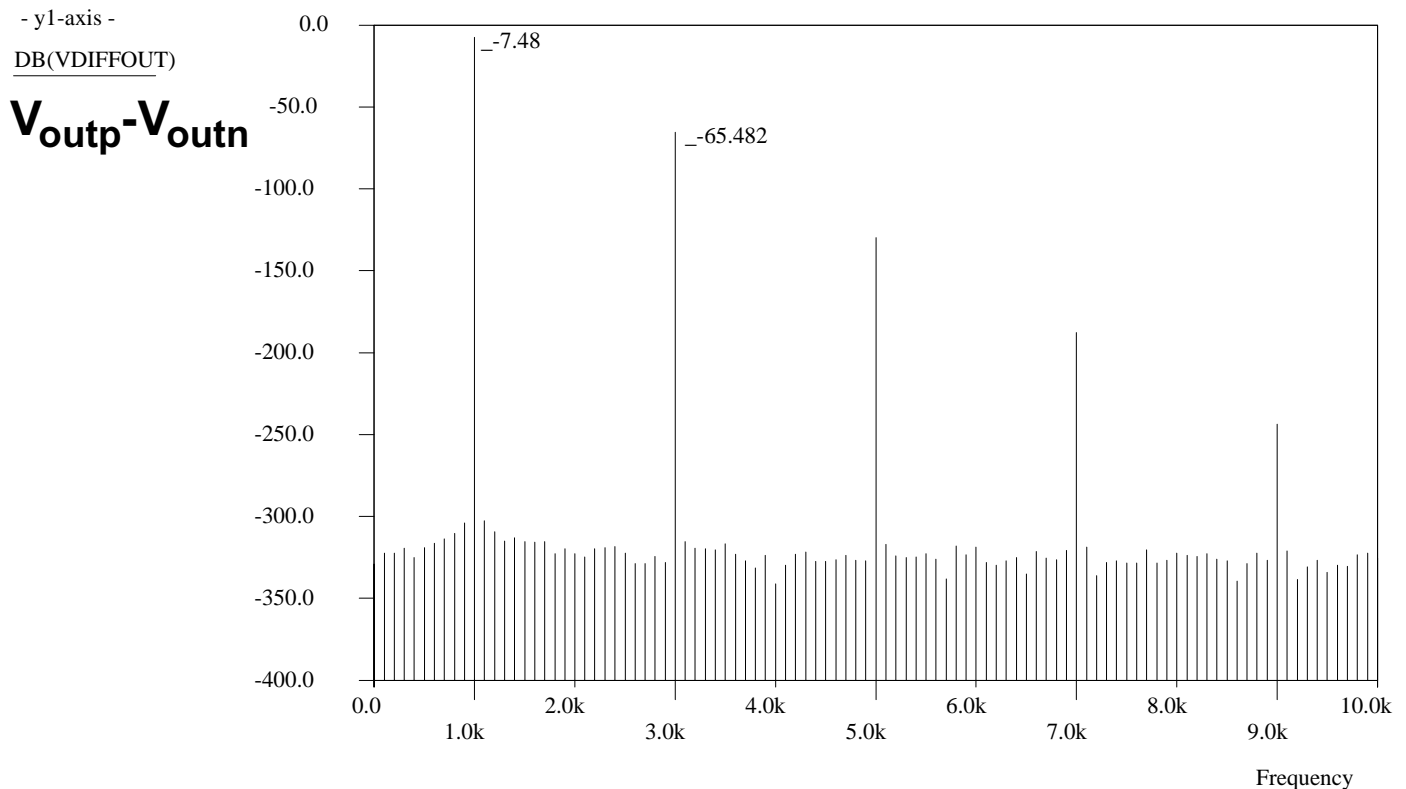
This gives a total differential input voltage of amplitude 40mV.

We see that the output sine wave is biased around 3.5V.

Each output has an amplitude of 298mV for a total differential amplitude of 596mV i.e. a gain of 14.9, close to that predicted.

Frequency Spectrum

If we do a fourier transform (FFT) of the output signal we get the following spectrum



Note that output amplitudes are in dB and have been normalised to rms

i.e for the fundamental

$$20\log\left(\frac{V_m}{\sqrt{2}}\right) = 20\log\frac{0.596}{2} = -7.5dB$$

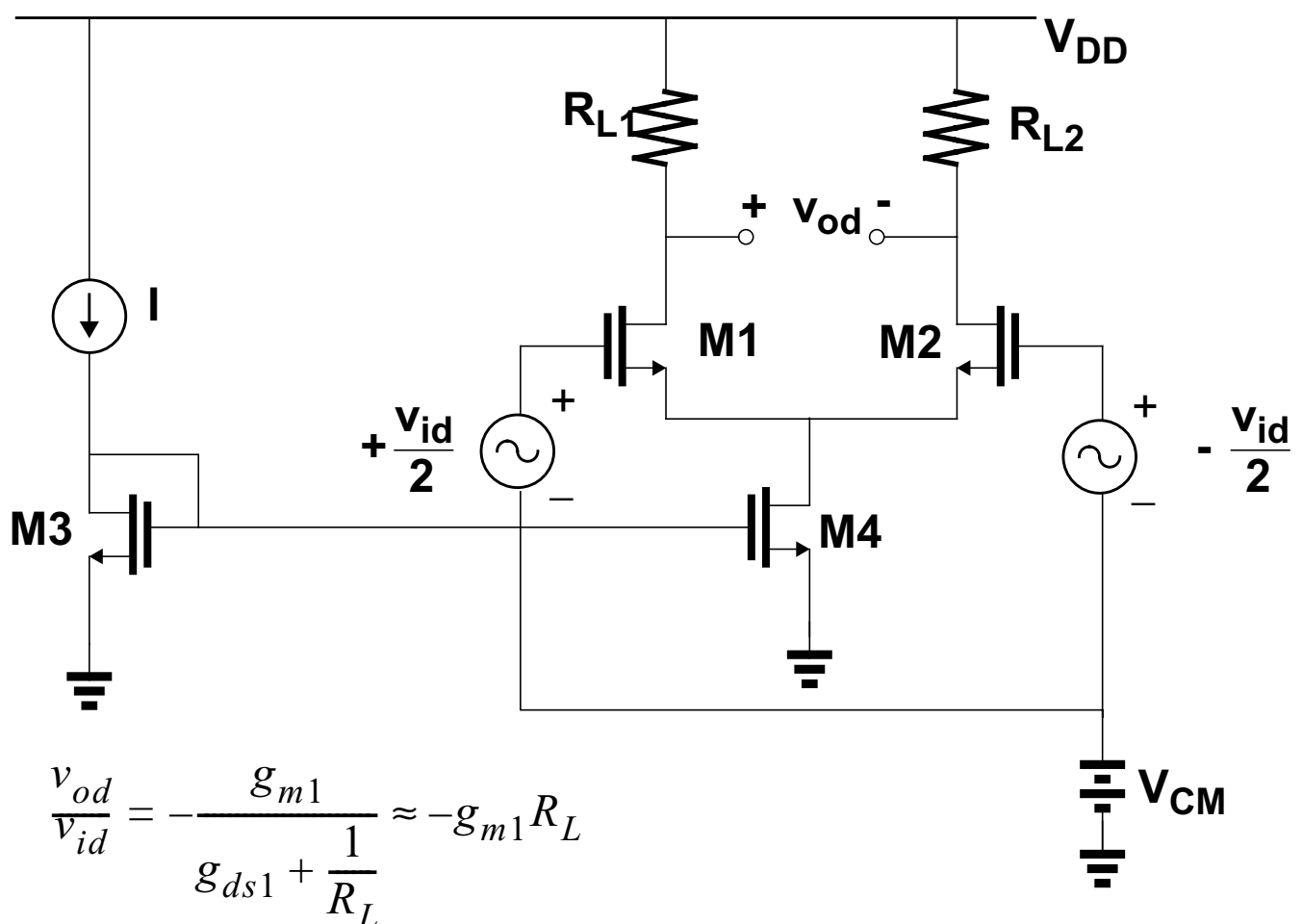
We see only odd harmonics of the fundamental, and the dominant third harmonic is 58dB down w.r.t. the fundamental.

6.4 Miscellaneous Differential Input stages

Any of the single-ended common-source gain stages we have looked at can also be used in a differential configuration.

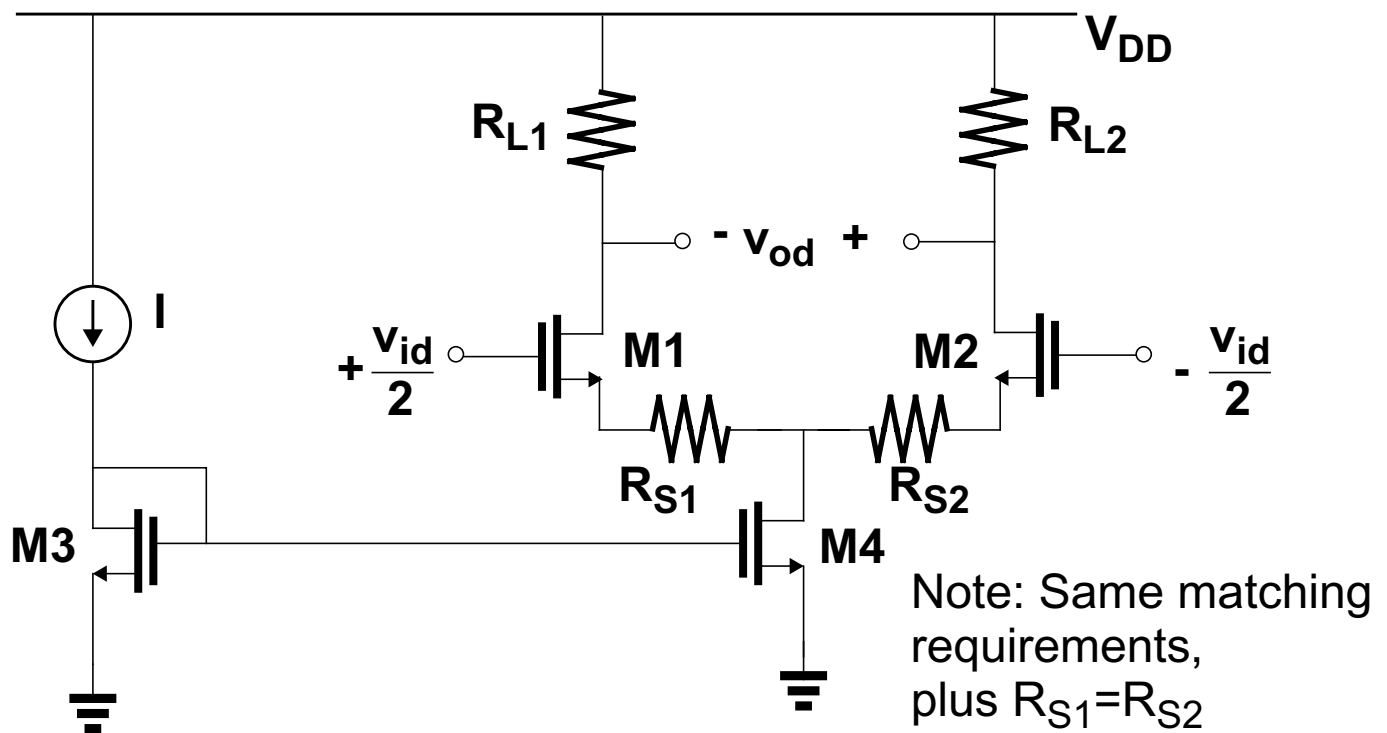
The concept of ac ground at the tail node still holds and the half-circuit method can be used to analyse the small-signal gain of the circuit.

6.4.1 Differential amplifier with resistive load



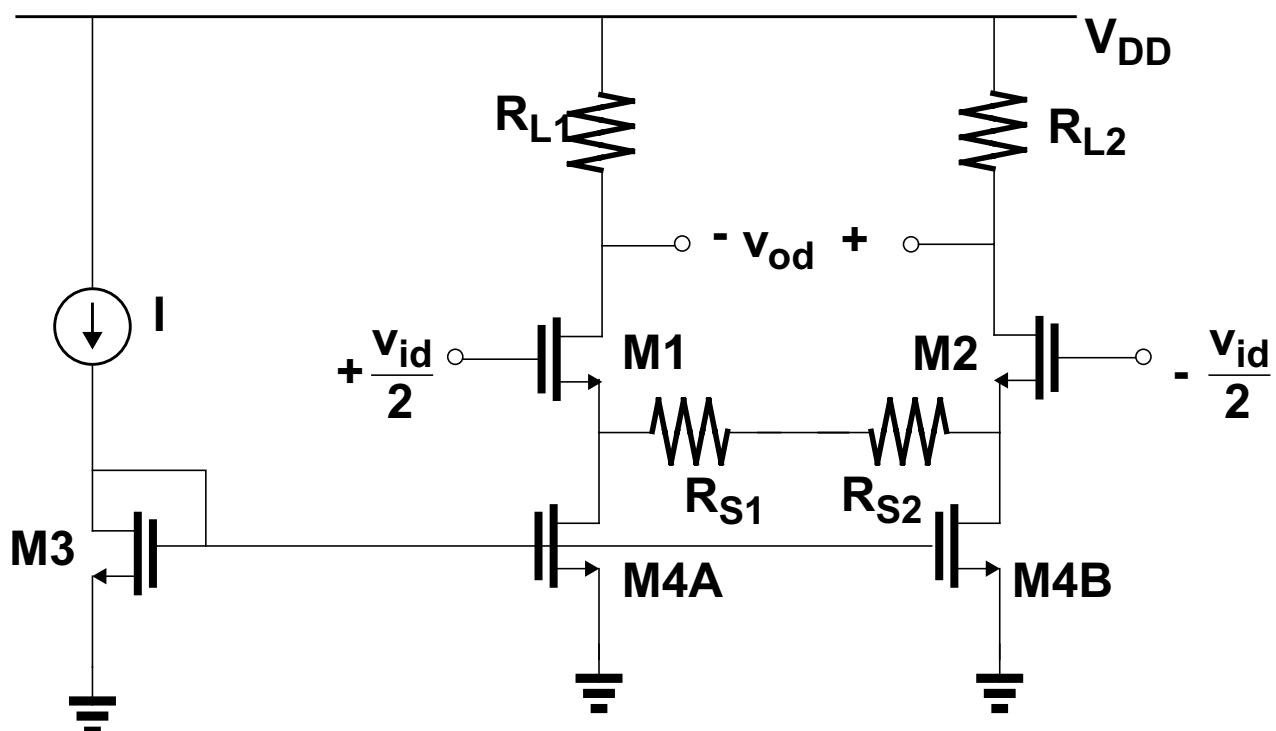
Note: $M1=M2$, $R_{L1}=R_{L2}$, $M4=\alpha M3$ (depending on scaling)

6.4.2 Degenerated differential amplifier with resistive load

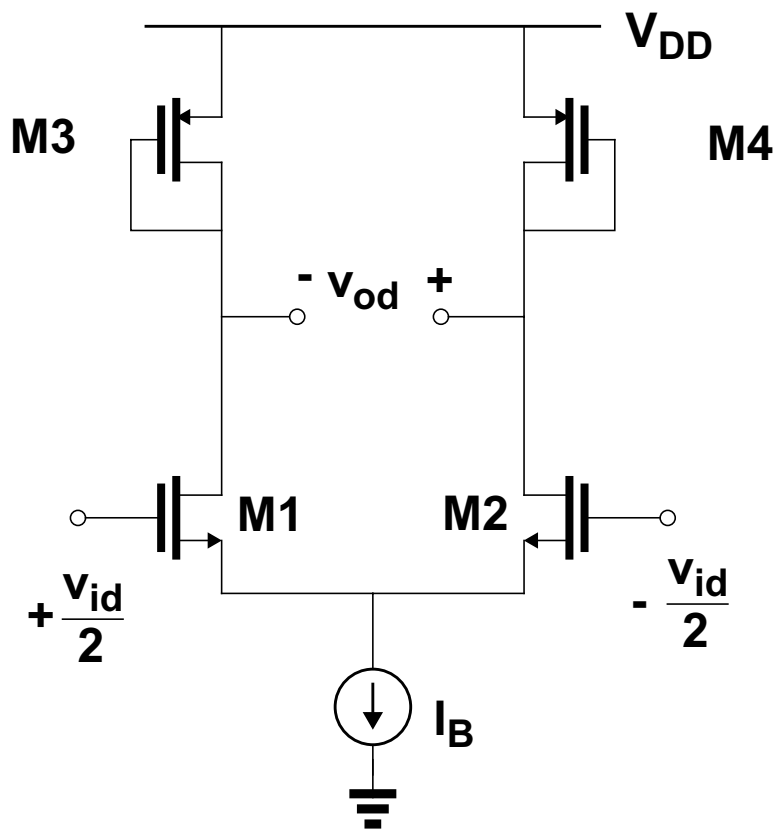


$$\frac{v_{od}}{v_{id}} \approx \frac{g_m R_L}{1 + g_m R_S} = \frac{R_L}{\frac{1}{g_m} + R_S} \approx \frac{R_L}{R_S} \text{ if } g_m R_S \gg 1$$

Alternatively



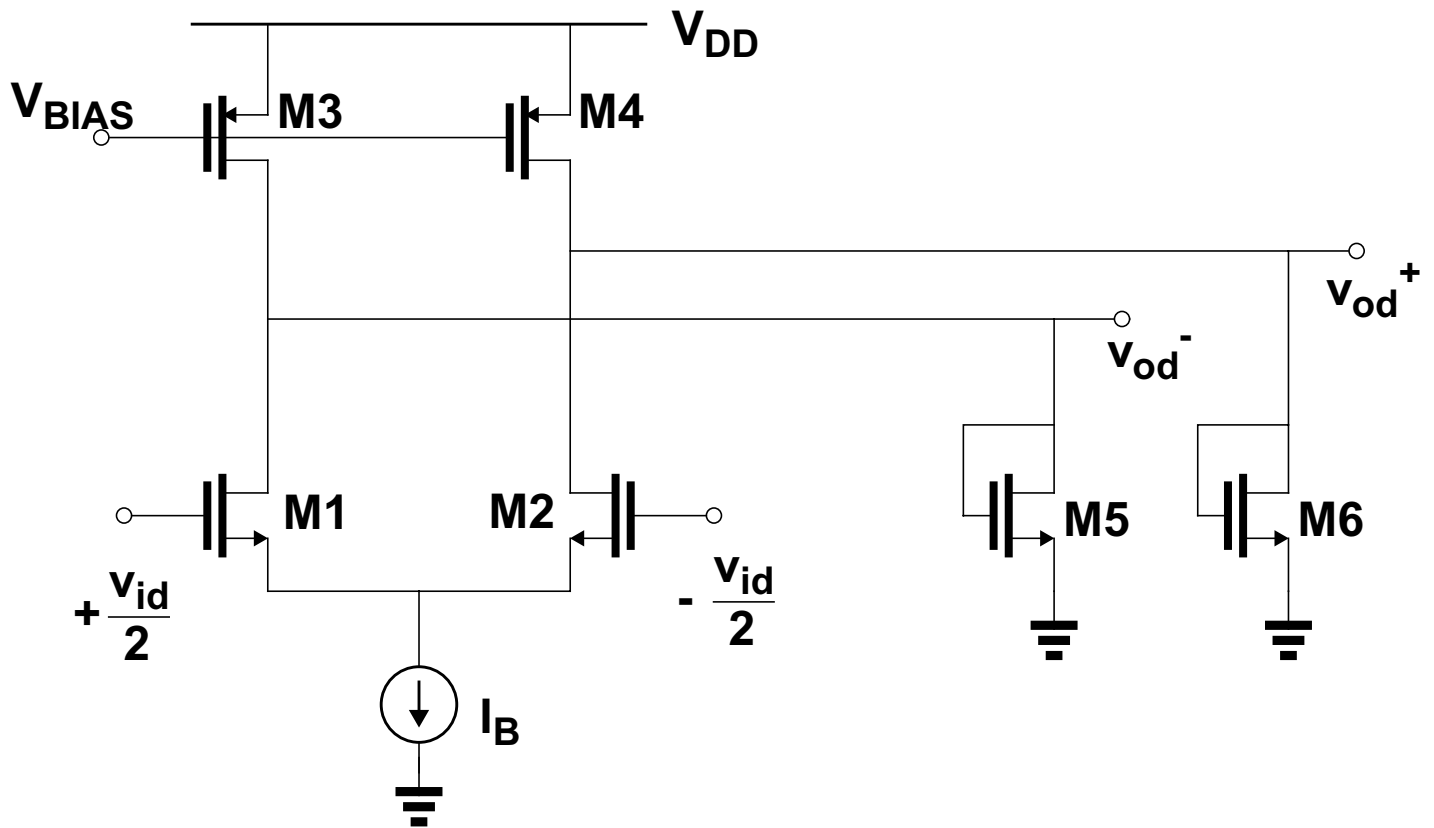
6.4.3 Differential amplifier with diode load



$M1=M2, M3=M4$

$$\frac{v_{od}}{v_{id}} = -\frac{g_{m1}}{g_{ds1} + g_{m3} + g_{ds3}} \approx -\frac{g_{m1}}{g_{m3}}$$

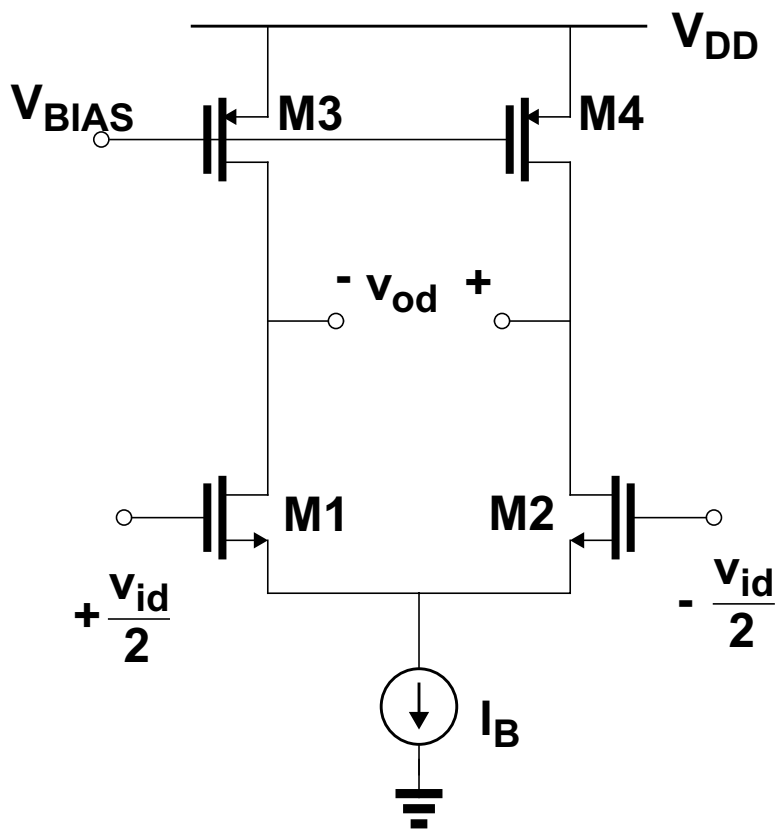
6.4.4 Differential amplifier with folded diode load



$M1=M2, M3=M4, M5=M6$

$$\frac{v_{od}}{v_{id}} = \frac{g_{m1}}{g_{ds1} + g_{ds3} + g_{m5} + g_{ds5}} \approx \frac{g_{m1}}{g_{m5}}$$

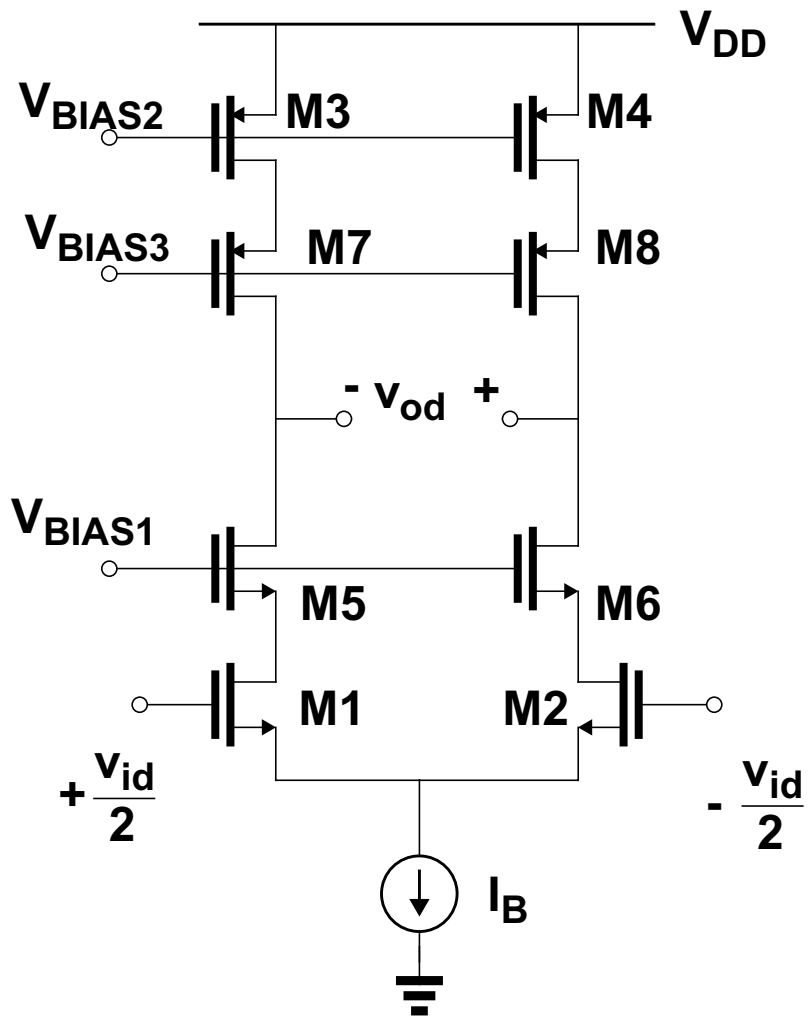
6.4.5 Differential amplifier with active load



$$M1=M2, M3=M4$$

$$\frac{v_{od}}{v_{id}} = \frac{g_{m1}}{g_{ds1} + g_{ds3}}$$

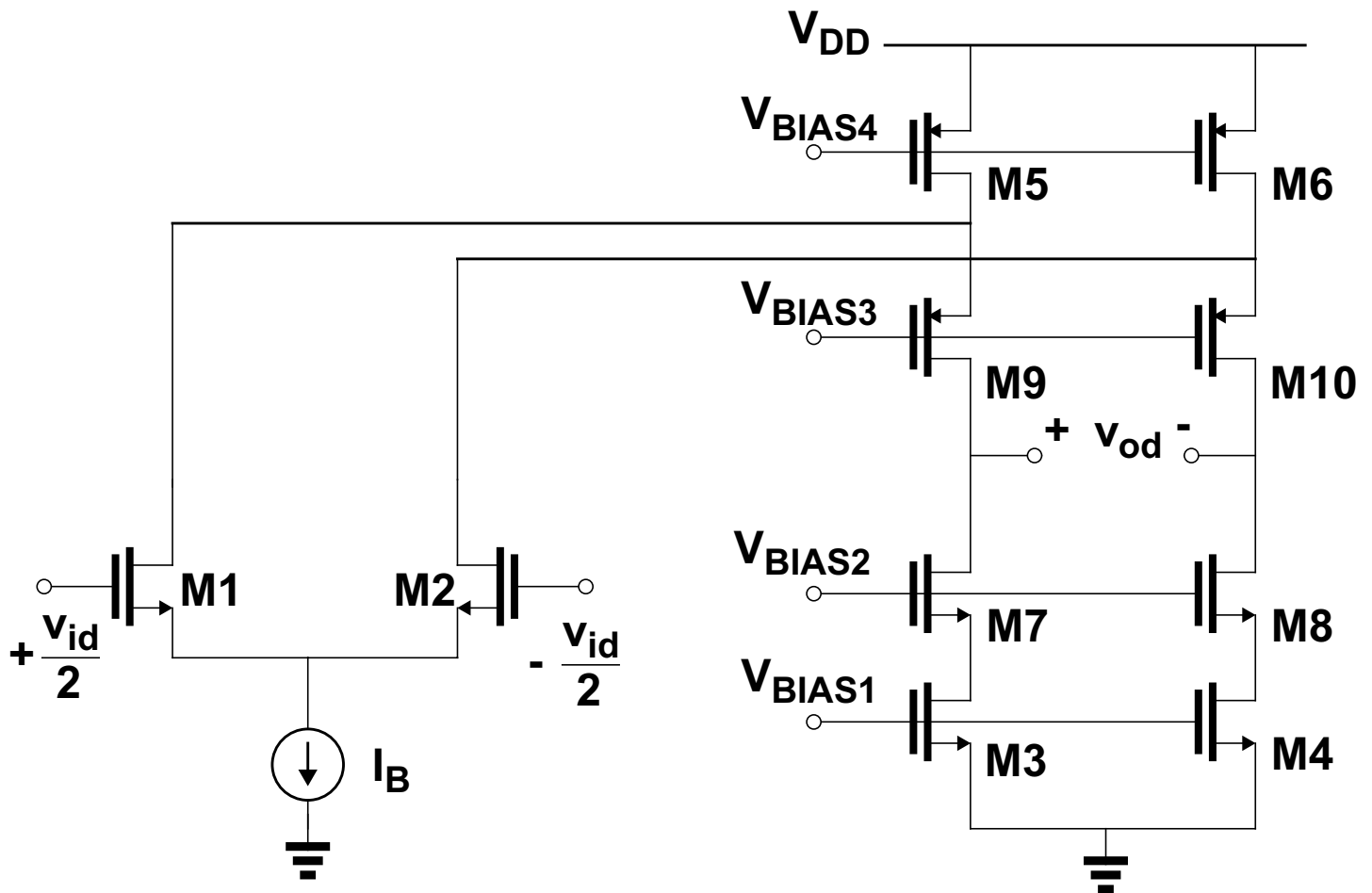
6.4.6 Cascode differential amplifier



$M1=M2$, $M3=M4$, $M5=M6$, $M7=M8$

$$\frac{v_{od}}{v_{id}} = \frac{g_{m1}}{\frac{g_{ds1}}{g_{m5}/g_{ds5}} + \frac{g_{ds3}}{g_{m7}/g_{ds7}}}$$

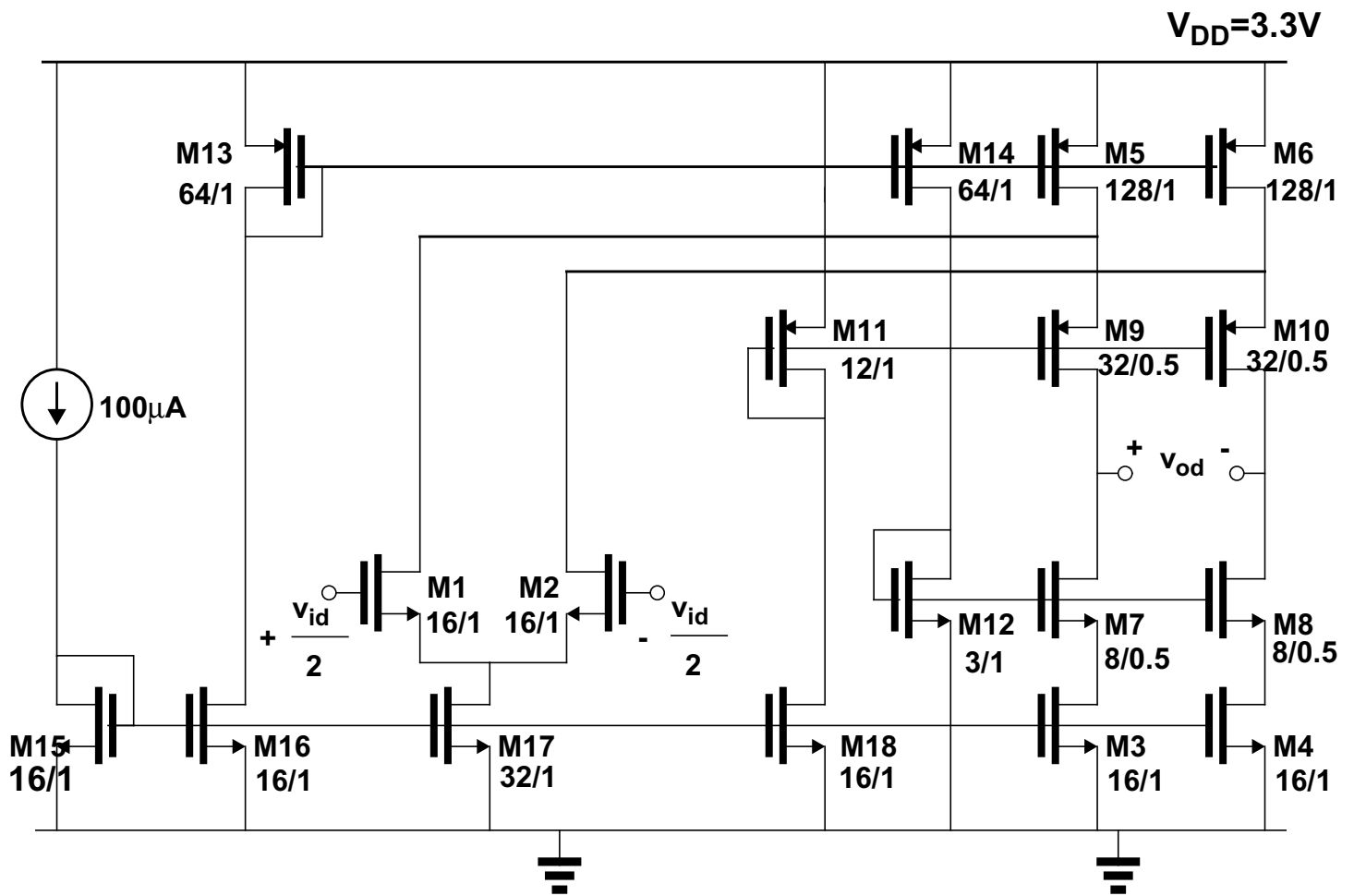
6.4.7 Folded Cascode differential amplifier



$M1=M2$, $M3=M4$, $M5=M6$, $M7=M8$, $M9=M10$

$$\frac{v_{od}}{v_{id}} = \frac{g_{m1}}{\frac{g_{ds3}}{g_{m7}/g_{ds7}} + \frac{g_{ds1} + g_{ds5}}{g_{m9}/g_{ds9}}}$$

6.4.8 Problem: Folded Cascode differential amplifier.



Calculate the small-signal gain of the folded-cascode amplifier shown.

Dimensions are as shown.

Assume all transistors are in saturation.

$K_n' = 200\mu A/V^2$, $K_p' = 50\mu A/V^2$, $V_t = 0.75V$, $\lambda = 0.04/L V^{-1}$

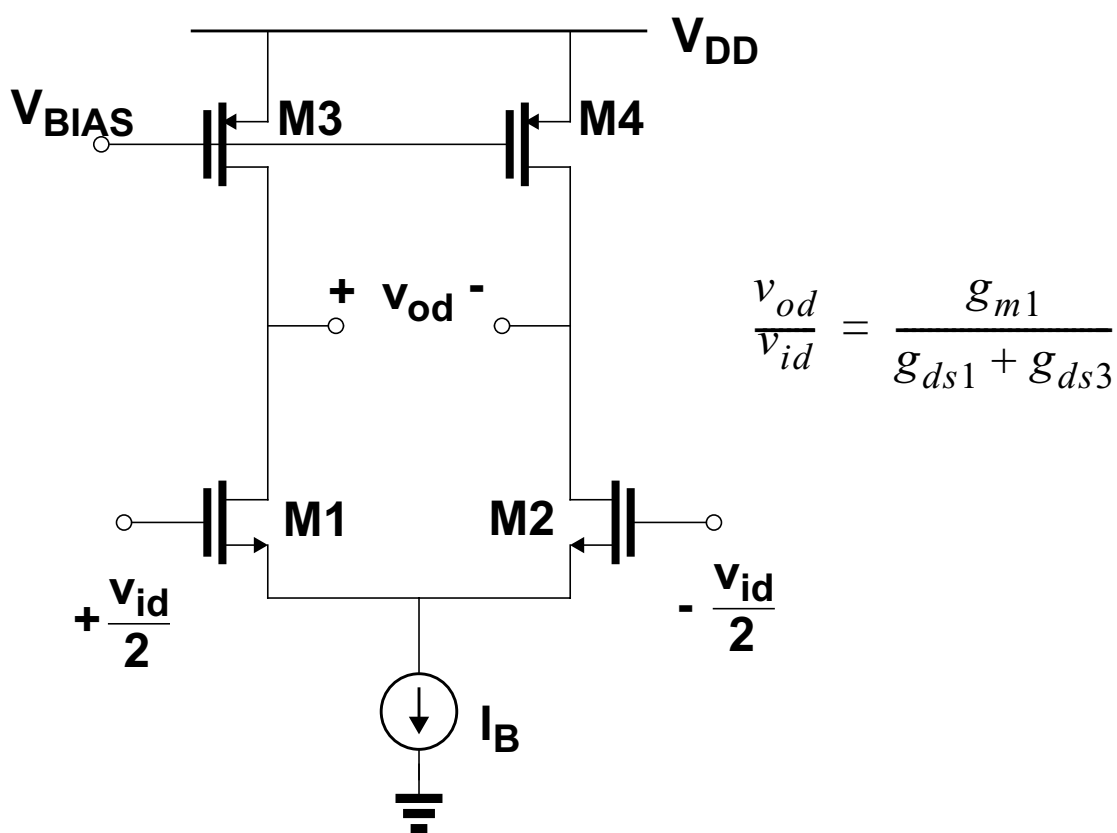
6.4.9 Fully differential amplifiers - the common-mode problem

Fully-differential amplifiers: Differential input, differential output.

Fully differential amplifiers are the amplifier of choice in most signal-processing applications.

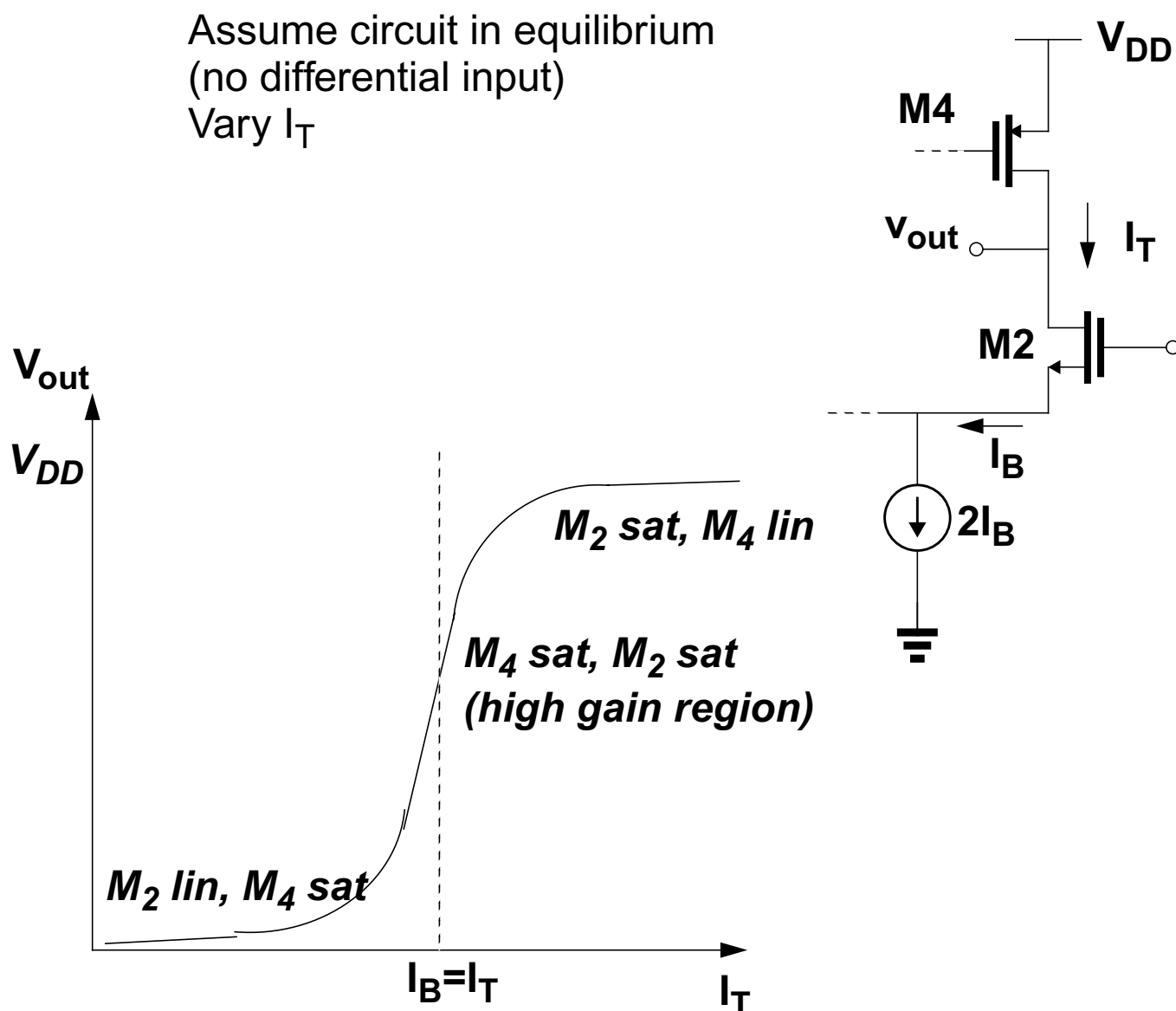
However, high-gain fully-differential amplifiers use high-impedance gain nodes, whose common-mode voltage is poorly defined.

Example: Differential amplifier with active load.



Fully differential amplifiers - the common-mode problem (contd)

What is problem with mismatch between top and bottom currents?
Look at large signal relationship between I_T and I_B



e.g. if $I_T > I_B$ the only way for the circuit to resolve this is for the drains of M_4 and M_2 (i.e. node v_{out}) to increase in potential thereby reducing the current from M_4 and increasing the current from M_2 via the output conductance.

For large mismatch this may force M_4 out of saturation

How do we solve this?

Common-mode feedback (CMFB)

In practice every fully differential amplifier needs a common-mode feedback circuit to ensure the output voltage is kept at a well-defined DC potential



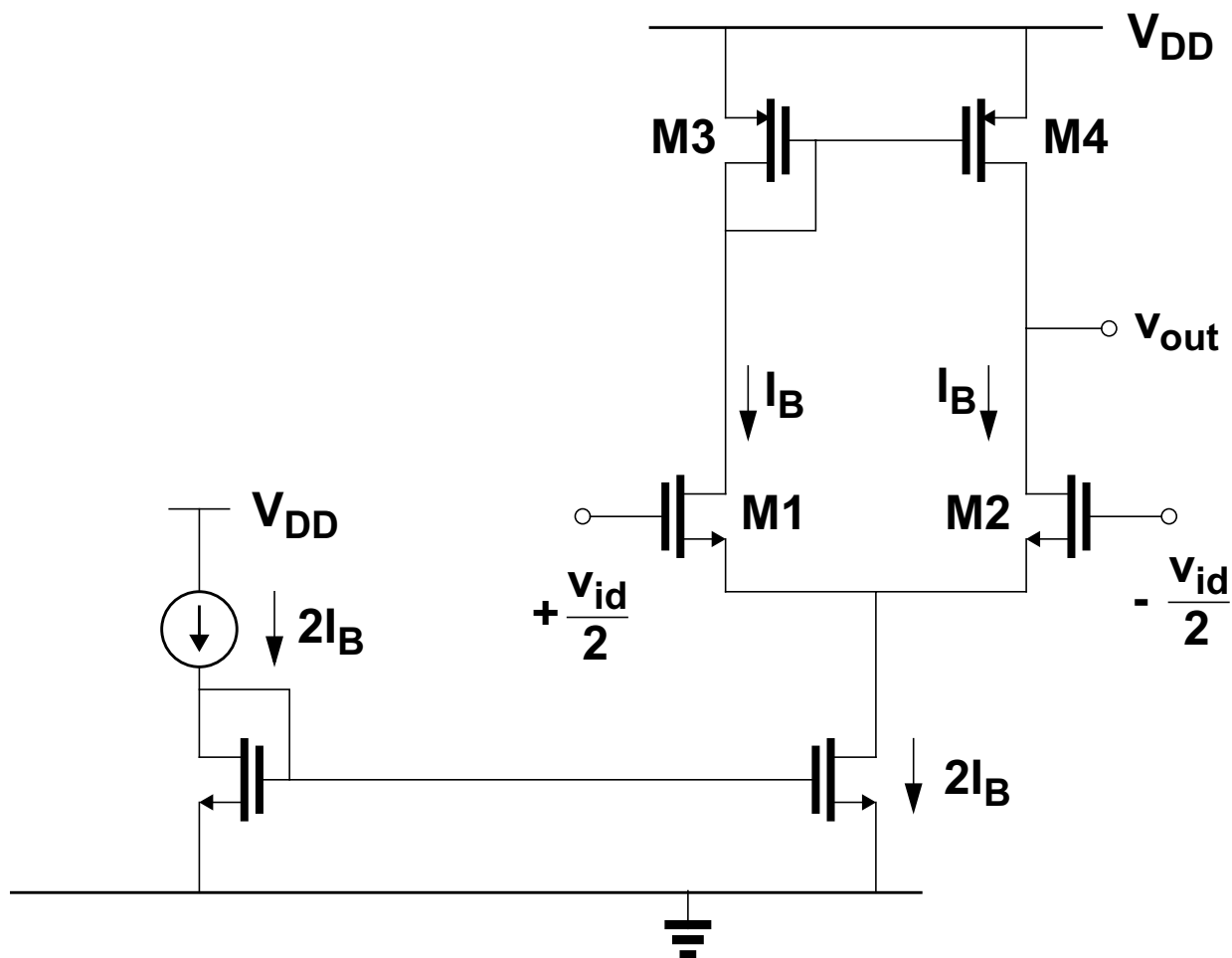
The diff. pair M10, M11 compare V_{cmout} to the desired voltage V_{ref} . In the nom situation ($V_{ref}=V_{cmout}$), half the NMOS diff pair current is from I_{B1} and half (I_{B2}) is controlled by the CMFB circuit (M9..M14). If say $2I_T > I_{B1} + I_{B2}$, then V_{cmout} rises, then $V_{cmout} > V_{ref}$, more current will flow through M10 and be mirrored into the tail via M13, M14 until $2I_T = I_{B1} + I_{B2}$.

Note: Stability of both differential and CMFB circuits need to be considered.

6.5 Differential-to-single-ended amplifiers

Many applications use or require a single-ended output (e.g. current reference circuit on P. 156).

Differential amplifier with current-mirror load



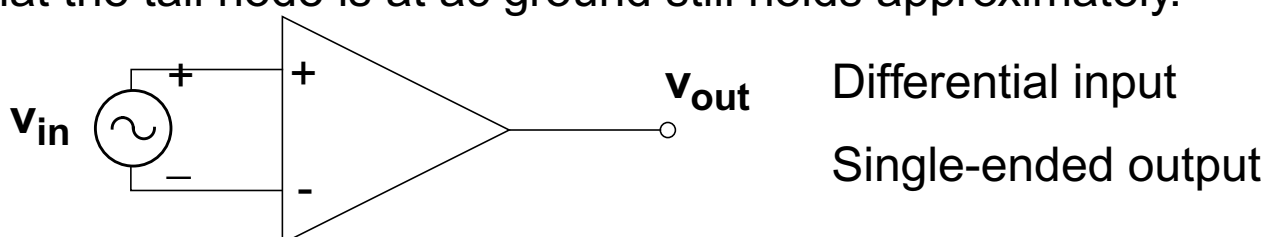
Replace top current source with a current mirror

Small-signal current due to $+v_{id}/2$ is also mirrored into output node, where it combines with small signal current due to $-v_{id}/2$, to force small-signal output voltage change.

->Differential to single-ended conversion

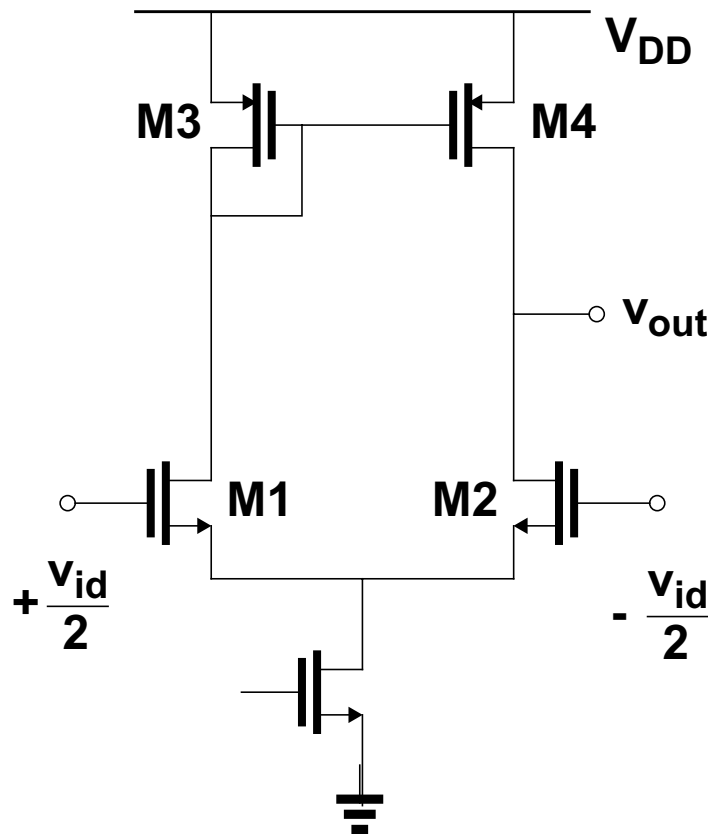
Note 1: quiescent currents shown (i.e. when $v_{id}=0$)

Note 2: Though the circuit is not entirely symmetrical due to the different connections of M3 and M4 the idea that the tail node is at ac ground still holds approximately.



6.5.1 Gain of diff. pair with current mirror load (Method 1)

Circuit is no longer symmetric, must look at LHS, RHS separately.



Assume :

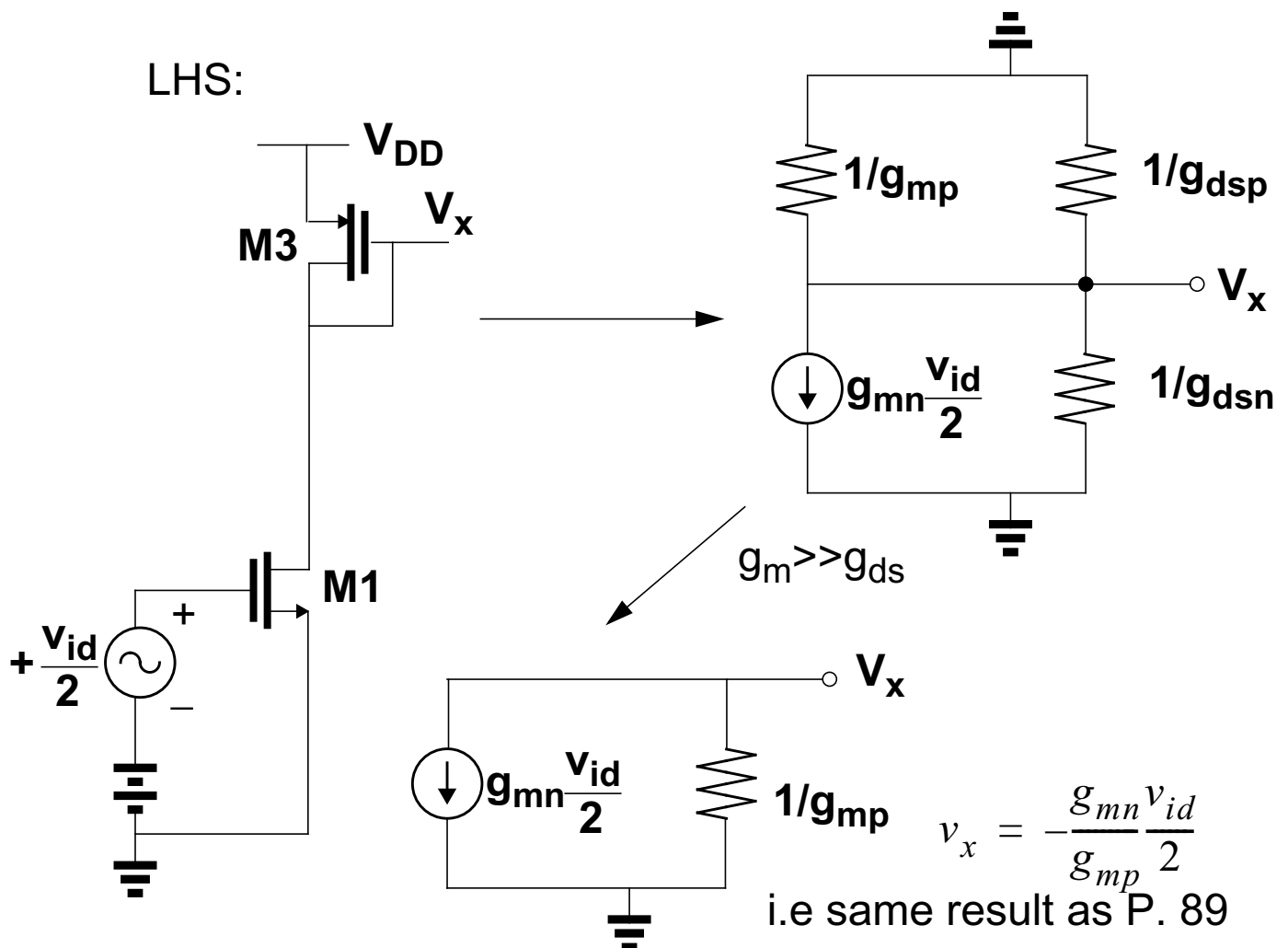
$$g_{m1}=g_{m2}=g_{mn}$$

$$g_{m3}=g_{m4}=g_{mp}$$

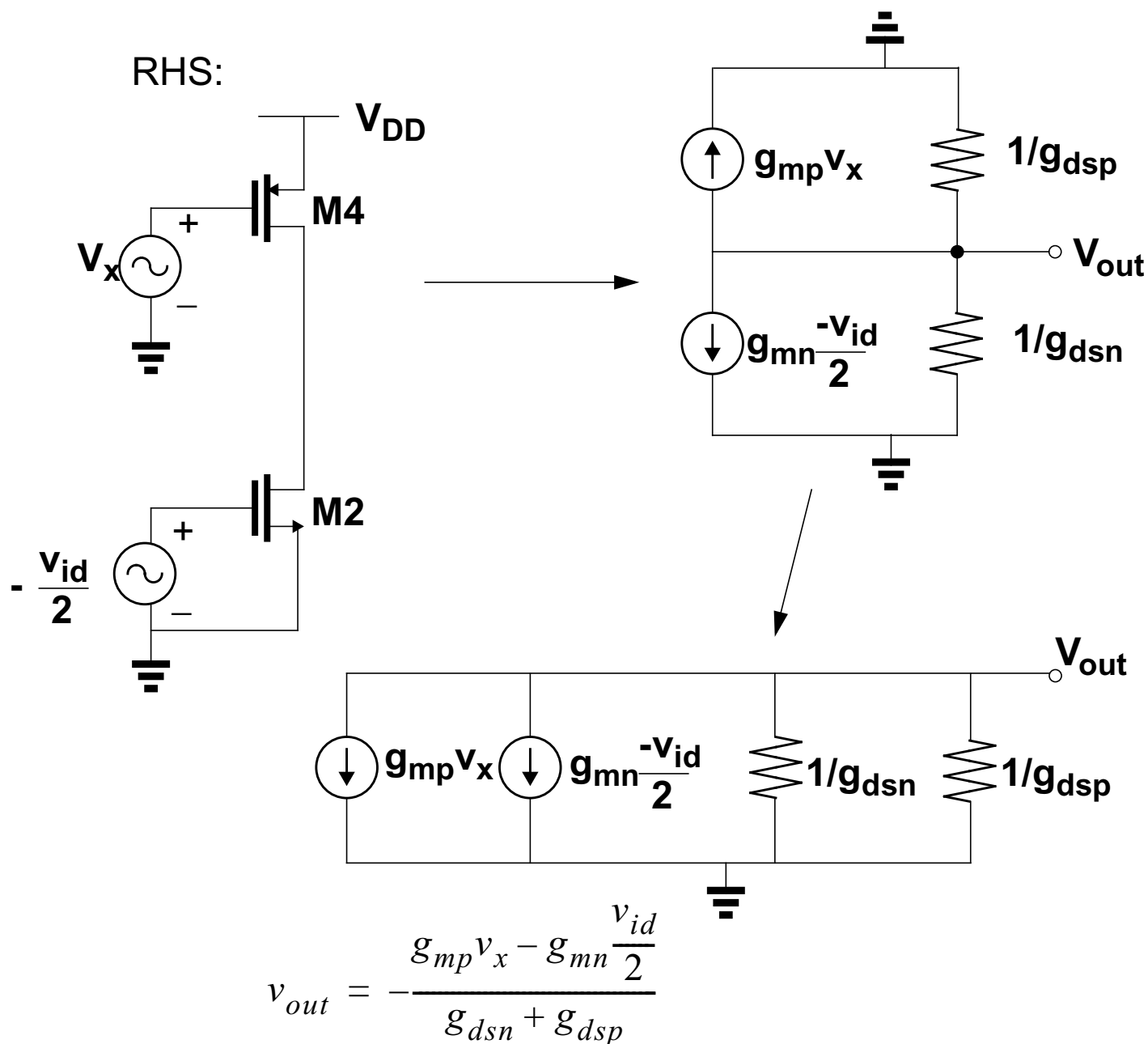
$$g_{ds3}=g_{ds4}=g_{dsp}$$

$$g_{ds1}=g_{ds2}=g_{dsn}$$

LHS:



Gain of differential pair with current mirror (contd.)



Substitute for v_x

$$v_{out} = -\frac{g_{mp}\left(-\frac{g_{mn}v_{id}}{g_{mp}2}\right) - g_{mn}\frac{v_{id}}{2}}{g_{dsn} + g_{dsp}}$$

$$Gain = \frac{v_{out}}{v_{id}} = \frac{g_{mn}}{g_{dsn} + g_{dsp}}$$

i.e. same gain as for the fully differential version

6.5.2 Gain of of diff. pair with current mirror load (Method 2)

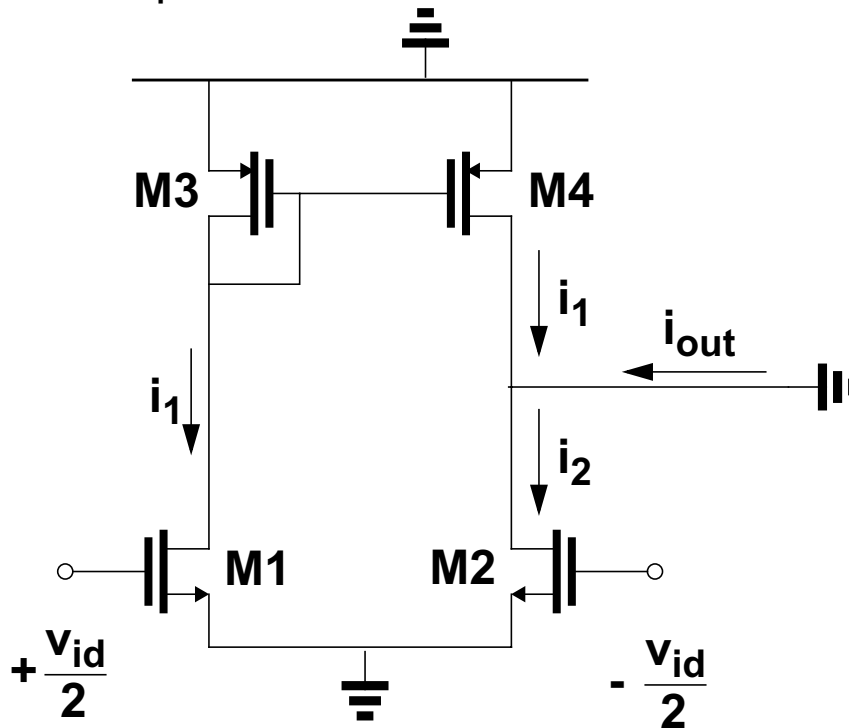
Recall: $G_m = i_{out}/v_{id}$ with output shorted to ground

With transconductance and output resistance we can calculate

Simple ac equivalent circuit:

$$Gain = -G_m R_{out}$$

$$Gain = -\frac{G_m}{G_{out}}$$



Transconductance:

Measure current flowing in output

LHS: $v_{id}/2$ gives a change in current at the drain of M1

$$i_1 = g_{mn} \frac{v_{id}}{2}$$

This is mirrored to the output node

RHS: $-v_{id}/2$ gives a change in current at the drain of M2

$$i_2 = g_{mn} \left(-\frac{v_{id}}{2} \right)$$

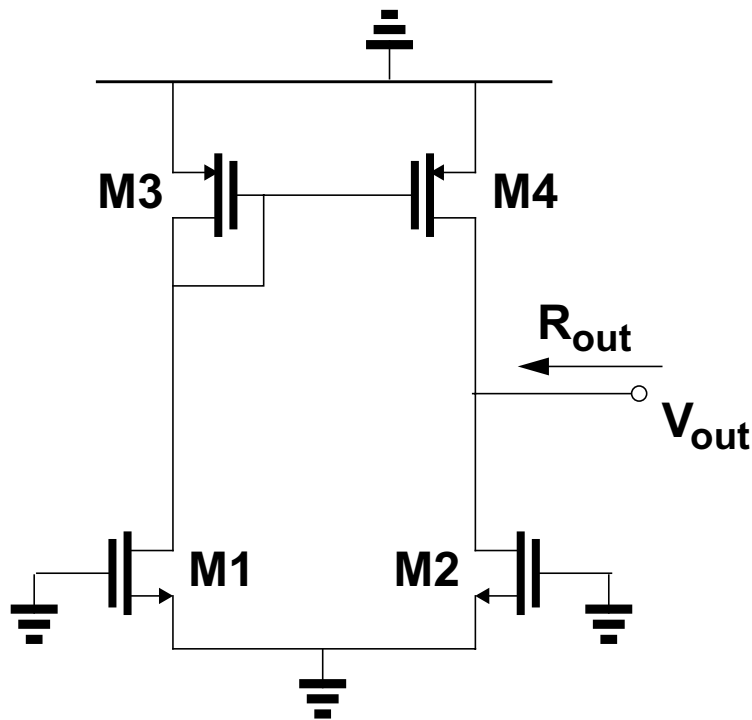
$$i_{out} = i_2 - i_1 = g_{mn} \left(-\frac{v_{id}}{2} \right) - g_{mn} \frac{v_{id}}{2}$$

$$G_m = \frac{i_{out}}{v_{id}} = -g_{mn}$$

Output resistance R_{out} of differential pair with current mirror

R_{out}

What is resistance looking into output node with inputs shorted?



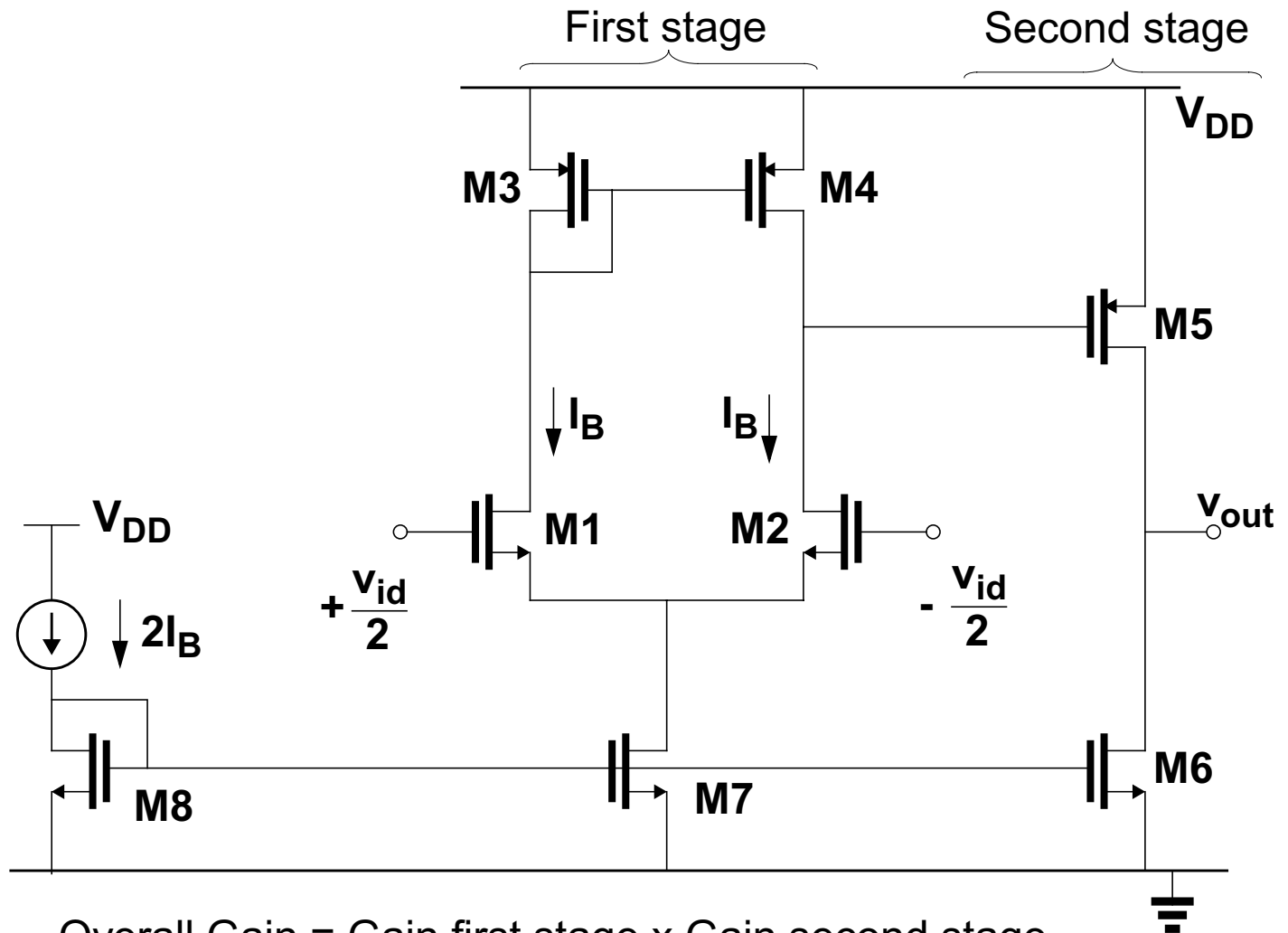
It is simply the inverse of the sum of the output conductances of M2 and M4

$$R_{out} = \frac{1}{g_{dsn} + g_{dsp}}$$

$$Gain = -G_m R_{out} = \frac{g_{mn}}{g_{dsn} + g_{dsp}}$$

Gain of many circuits can be seen by inspection as in this case.

6.5.3 Two-stage differential to single-ended amplifier



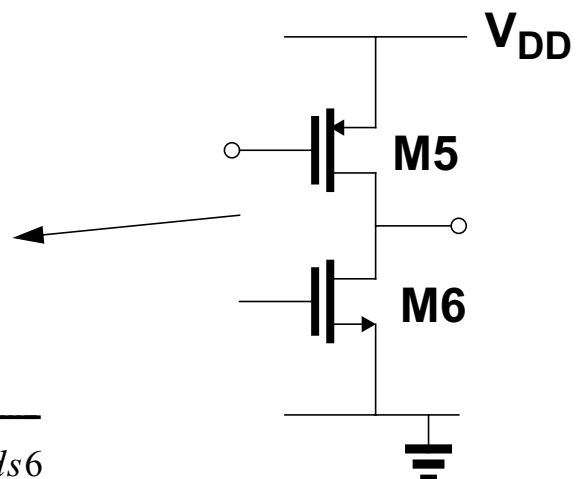
Overall Gain = Gain first stage x Gain second stage

Overall Gain = Gain₁ x Gain₂

$$Gain_1 = \frac{g_{m1}}{g_{ds2} + g_{ds4}}$$

$$Gain_2 = -\frac{g_{m5}}{g_{ds5} + g_{ds6}}$$

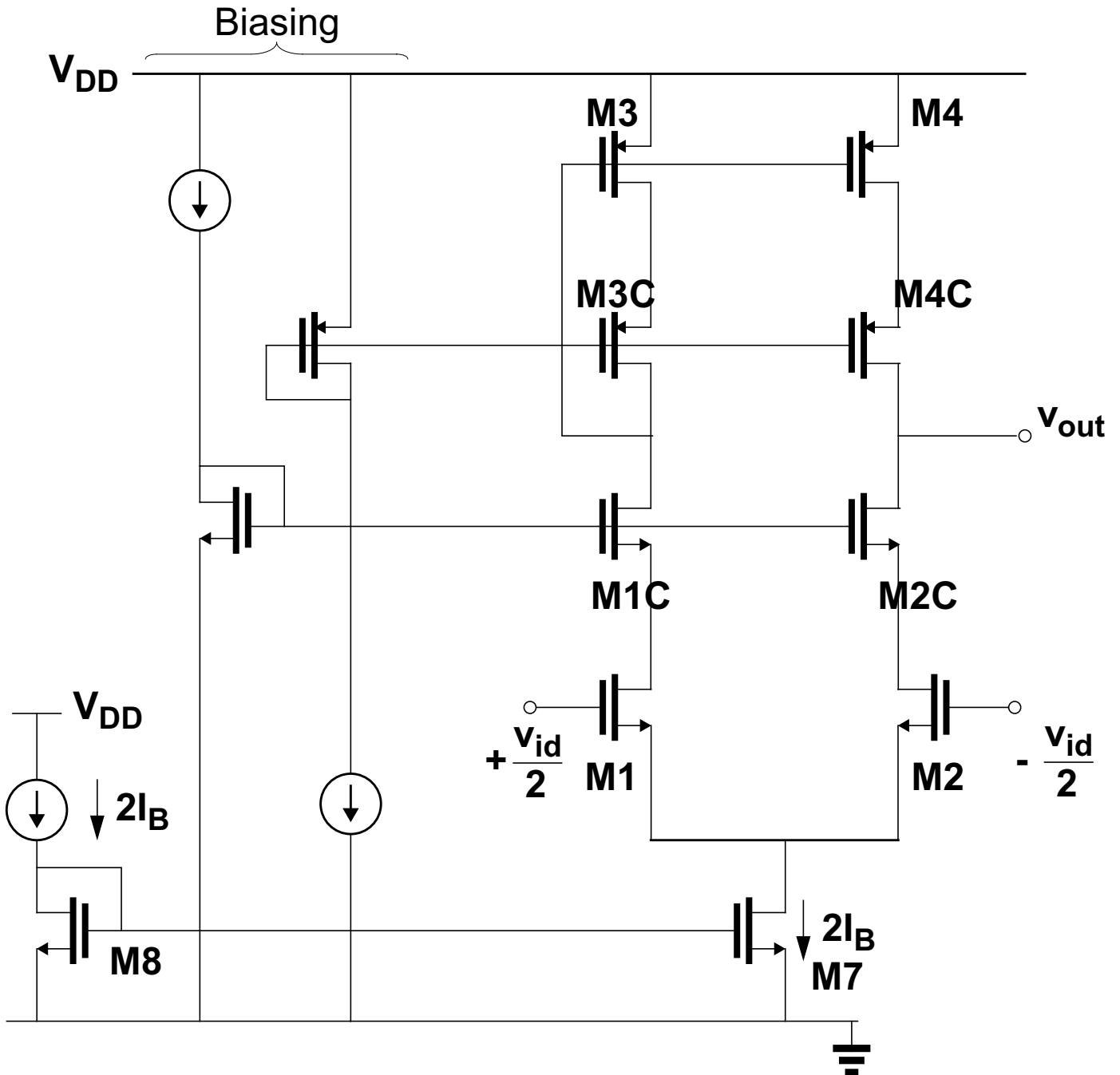
$$Gain = -\frac{g_{m1}}{g_{ds2} + g_{ds4}} \cdot \frac{g_{m5}}{g_{ds5} + g_{ds6}}$$



N.B. This gives a negative gain.

For convenience we usually call the gate of M2 the positive input
This gives a positive overall gain.

6.5.4 Cascode differential to single-ended amplifier

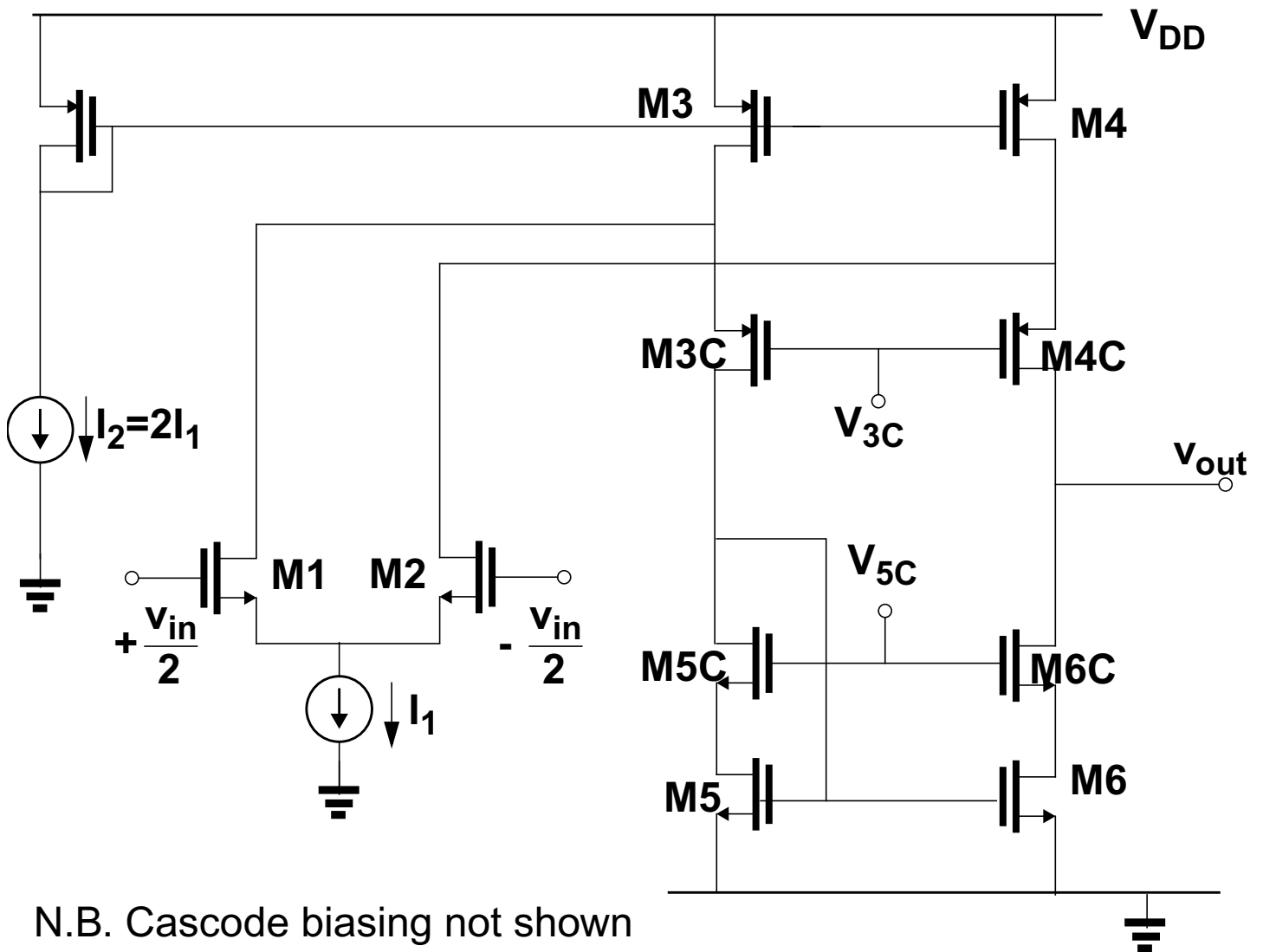


If $M1=M2$, $M1C=M2C$, $M3=M4$, $M3C=M4C$, $M7=M8$

$$G_m = -g_{m1} \quad G_{out} = \frac{g_{ds2}}{g_{m2C}/g_{ds2C}} + \frac{g_{ds4}}{g_{m4C}/g_{ds4C}}$$

$$Gain = \frac{g_{m1}}{\frac{g_{ds2}}{g_{m2C}/g_{ds2C}} + \frac{g_{ds4}}{g_{m4C}/g_{ds4C}}}$$

6.5.5 Folded-cascode differential to single-ended amplifier



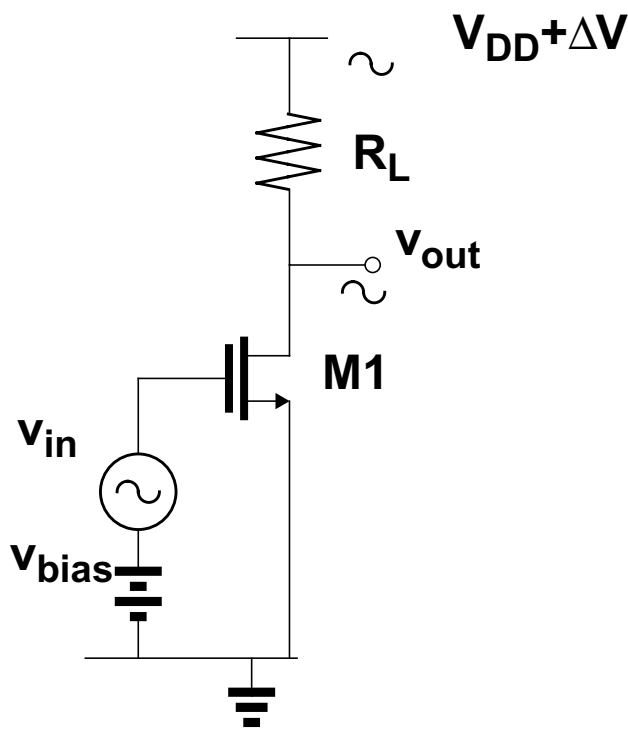
If $M1=M2$, $M3=M4$, $M3C=M4C$, $M5=M6$, $M5C=M6C$

$$G_m = -g_{m1} \quad G_{out} = \frac{g_{ds2} + g_{ds4}}{g_{m4C}/g_{ds4C}} + \frac{g_{ds6}}{g_{m6C}/g_{ds6C}}$$

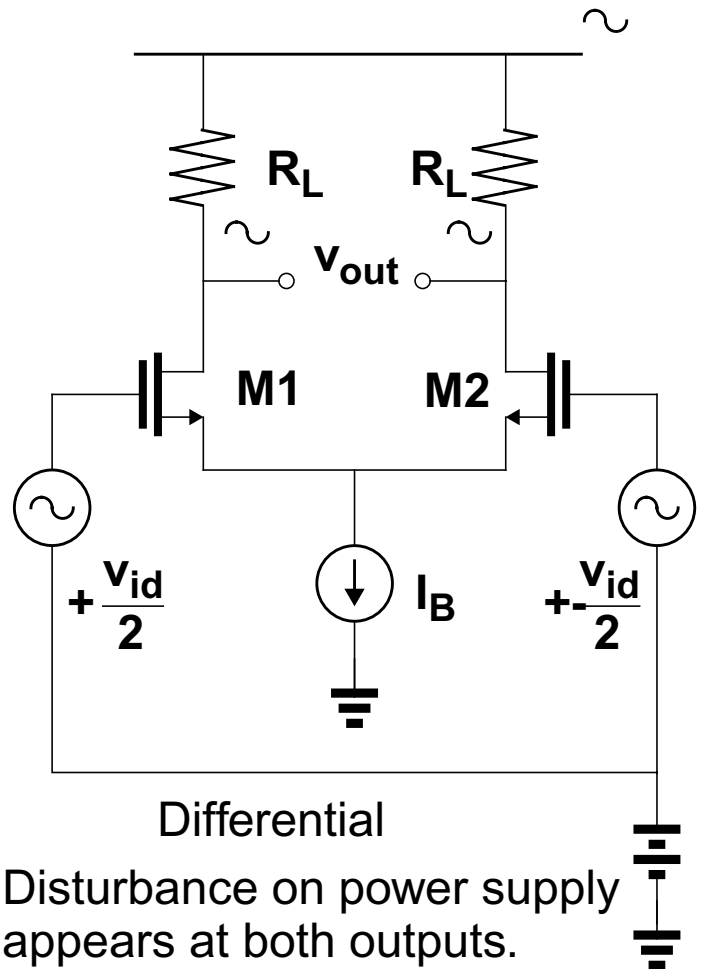
$$Gain = -\frac{g_{m1}}{\frac{g_{ds2} + g_{ds4}}{g_{m4C}/g_{ds4C}} + \frac{g_{ds6}}{g_{m6C}/g_{ds6C}}}$$

6.6 Advantages of Differential gain stages

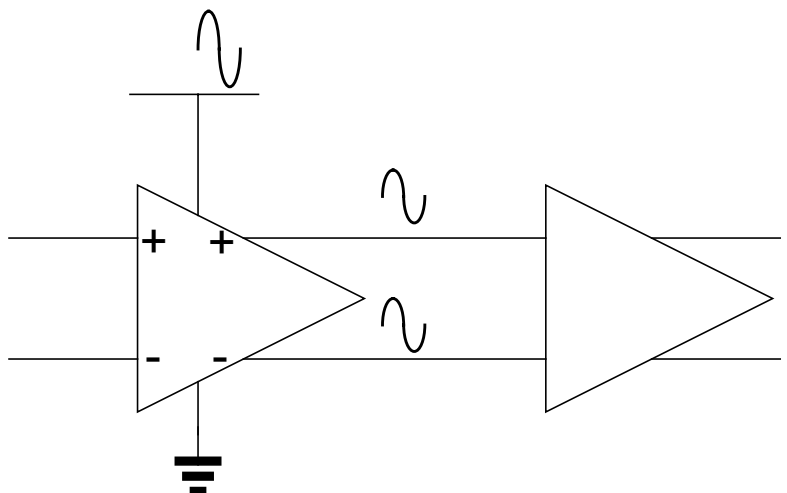
1. Suitable topology for op-amps
2. Common Mode Rejection
3. Extra signal swing
4. Better power supply noise rejection



Single-ended
Disturbance on power supply
appears at output
No power supply rejection



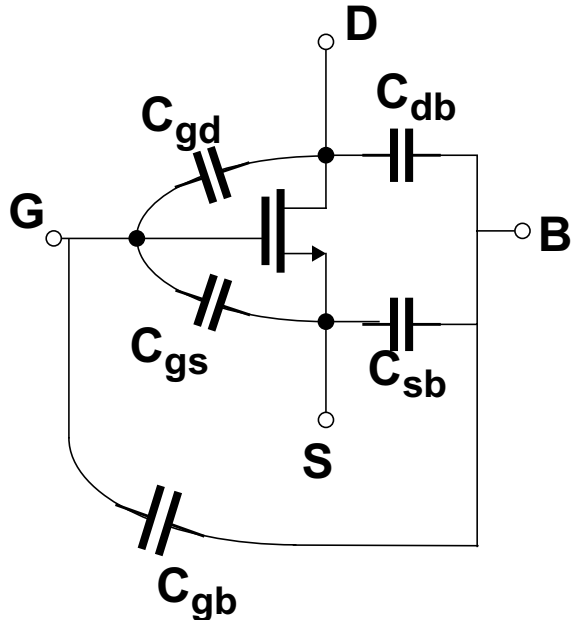
Differential
Disturbance on power supply
appears at both outputs.
Will be rejected by the
following differential stage



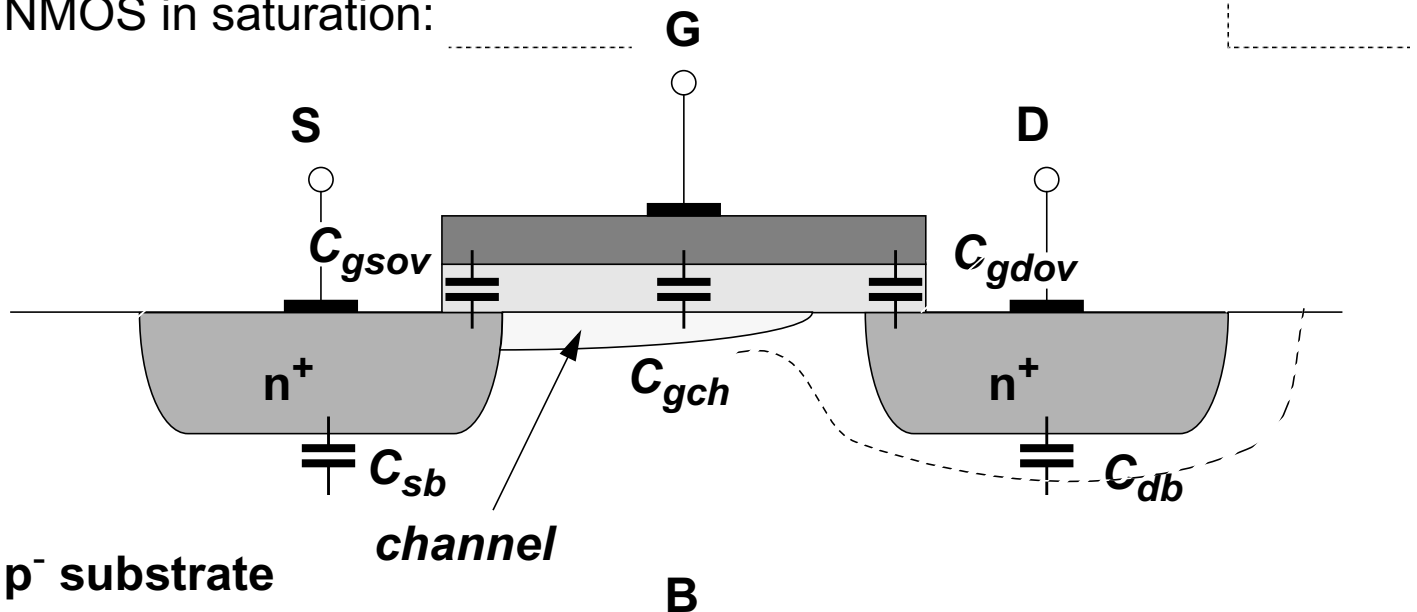
7 High-frequency analysis

7.1 MOS Device Capacitances

Consider the parasitic capacitances of a MOS transistor.
There is a capacitance between each of the terminals



NMOS in saturation:



- C_{gch} : Oxide capacitance between gate and channel
- $C_{gs\text{ov}}$: Oxide overlap capacitance between gate and source
- $C_{gd\text{ov}}$: Oxide overlap capacitance between gate and drain
- C_{sb} : Junction capacitance between source and bulk
- C_{db} : Junction capacitance between drain and bulk

7.1.1 Oxide capacitances

Oxide capacitances in saturation region:

C_{gs} = Overlap capacitance + Gate to channel capacitance:

$$C_{gs} = C_{gsov}W + \frac{2}{3}C_{ox}WL_{eff} \quad \text{factor 2/3 because channel pinched-off at drain}$$

$$C_{gd} = C_{gdov}W$$

C_{gsov} , C_{gdov} typical values $0.1 \text{ fF}/\mu\text{m}$ of channel width

C_{ox} typical values depend on t_{ox}

e.g. $t_{ox} = 10\text{nm}$ (100 Angstrom)

$$C_{ox} = \frac{\epsilon_{ox}\epsilon_o}{t_{ox}} = \frac{3.97 \times 8.85 \times 10^{-14} \text{ F/cm}}{10 \times 10^{-7} \text{ cm}} = 35 \times 10^{-8} \text{ F/cm}^2 \\ = 3.5 \text{ fF}/\mu\text{m}^2$$

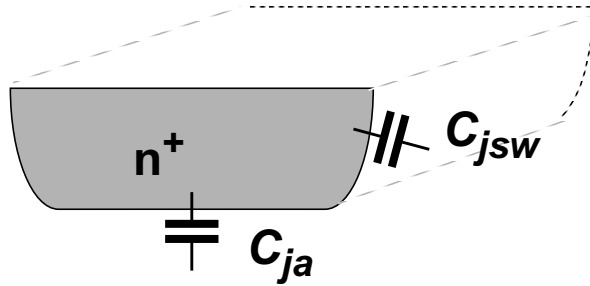
C_{ox} increases as t_{ox} decreases

7.1.2 Diffusion capacitances

Diffusion (junction) capacitances:

C_{db} , C_{sb} : junction capacitances (reversed-biased diode)

Each consists of 2 components: bottom-plate C_{ja}
and sidewall C_{jsw}



$$C_{sb} = \frac{C_{ja}AS}{\left(1 + \frac{V_{SB}}{\psi_o}\right)^{MJ}} + \frac{C_{jsw}PS}{\left(1 + \frac{V_{SB}}{\psi_o}\right)^{MJSW}}$$

AS: Area of source

PS: Perimeter of source

ψ_o =built-in potential

C_{ja} typical value 1fF/ μm^2

C_{jsw} typical value 0.1fF/ μm

MJ typical value 0.3

$MJSW$ typical value 0.1

Similarly

$$C_{db} = \frac{C_{ja}AD}{\left(1 + \frac{V_{DB}}{\psi_o}\right)^{MJ}} + \frac{C_{jsw}PD}{\left(1 + \frac{V_{DB}}{\psi_o}\right)^{MJSW}}$$

AD: Area of drain

PD: Perimeter of drain

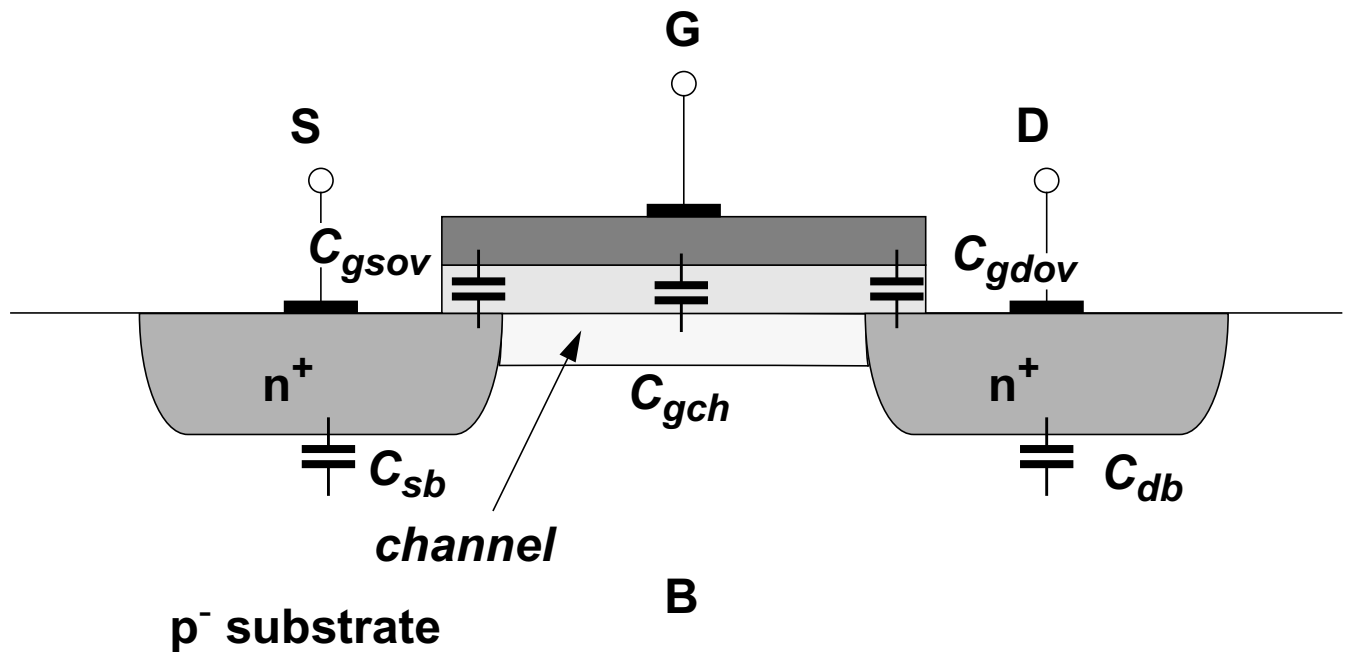
ψ_o =built-in potential

V_{DB} : Drain-bulk voltage

As voltage across junction increases capacitance decreases

7.1.3 C_{gs}, G_{gd} in linear region

NMOS in linear region: Channel extends from source to drain



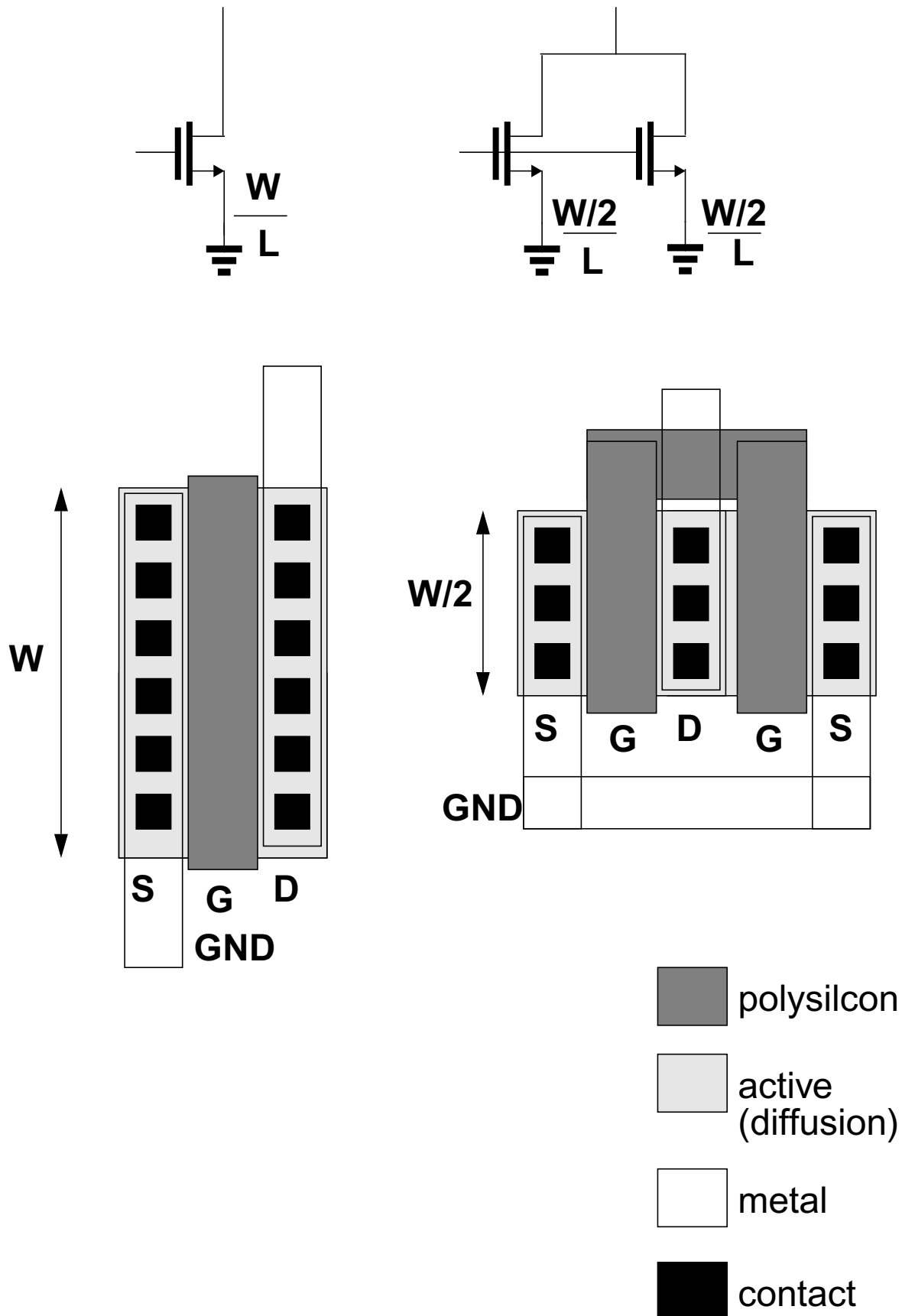
Capacitance from gate to channel is split between source and drain

$$C_{gs} = C_{gsov}W + \frac{1}{2}C_{ox}WL_{eff}$$

$$C_{gd} = C_{gdov}W + \frac{1}{2}C_{ox}WL_{eff}$$

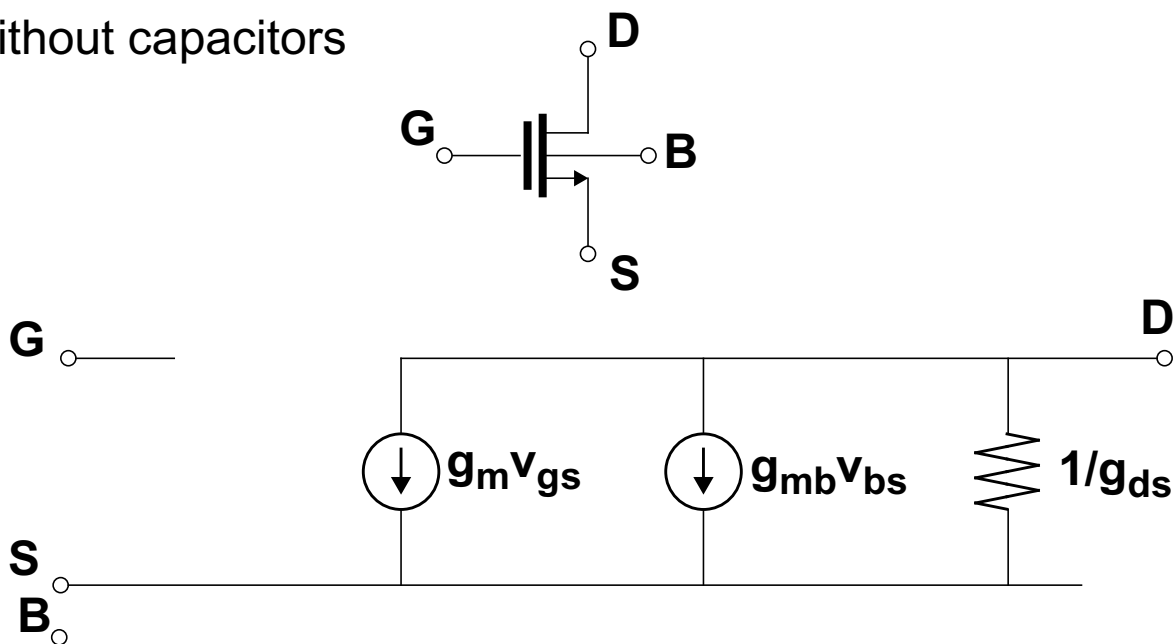
7.1.4 Layout for low capacitance

Use 'folded' transistors to reduce capacitance on drain

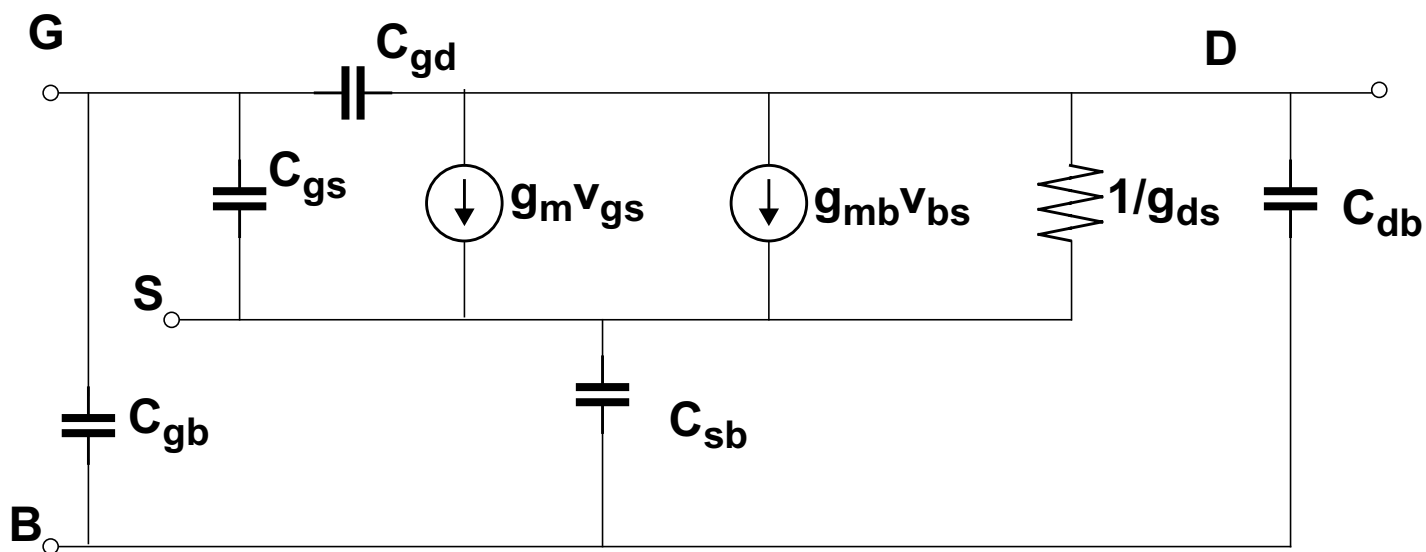
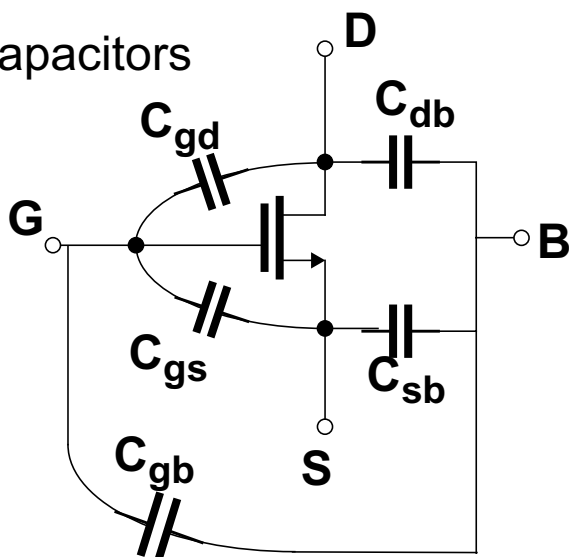


7.2 NMOS with capacitances : Small Signal Model

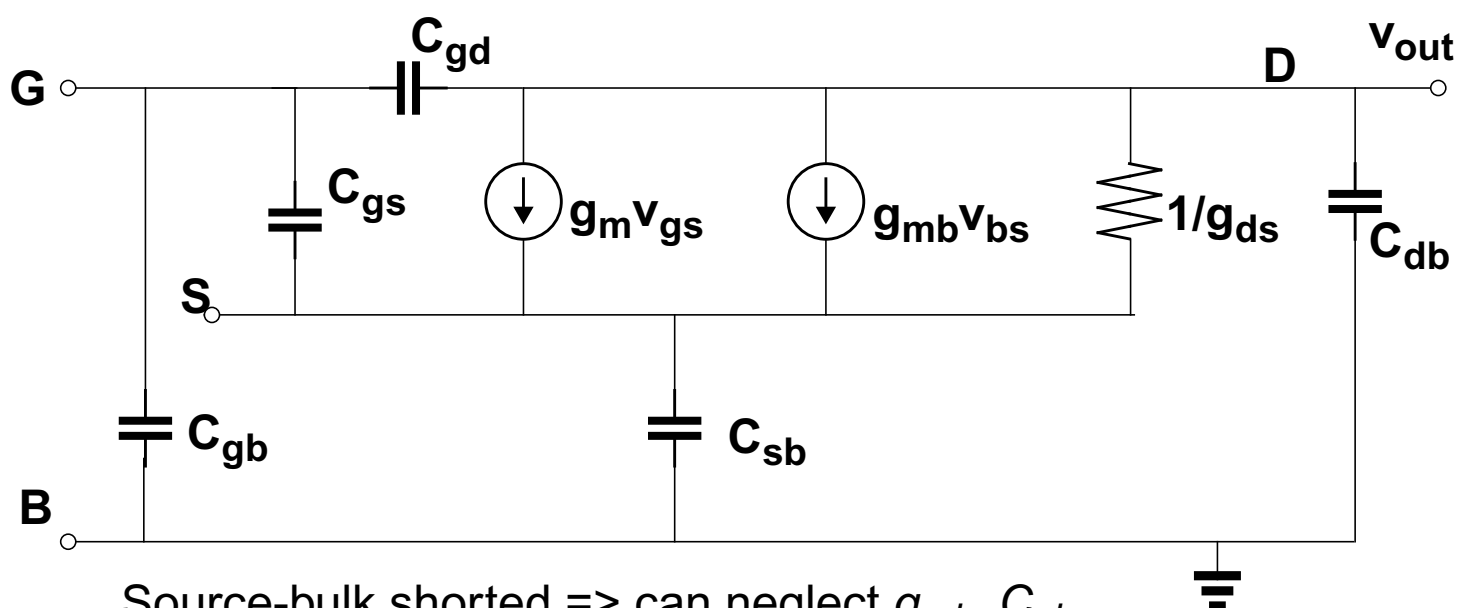
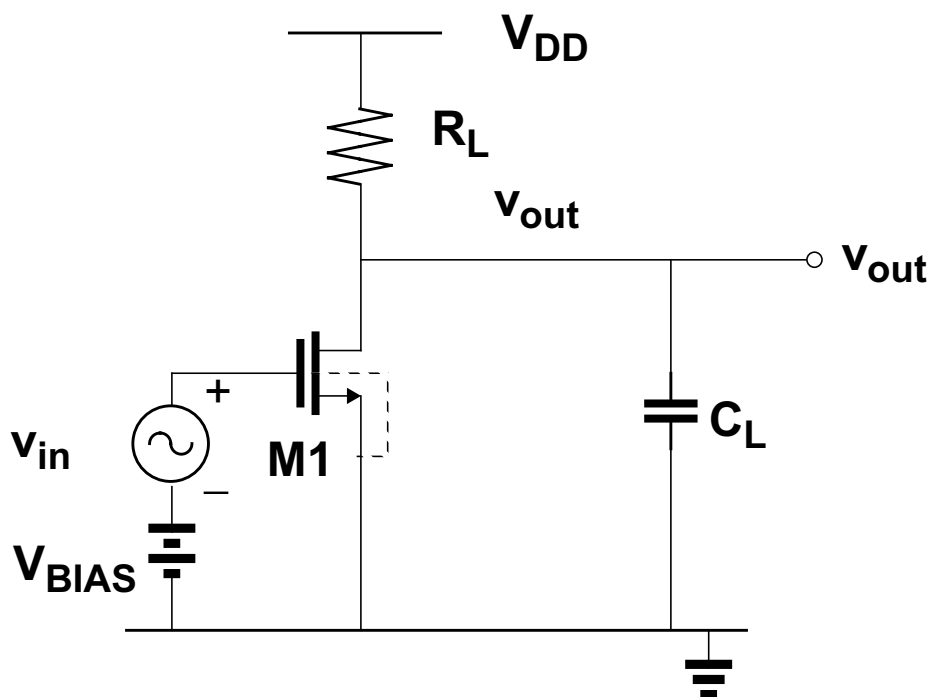
Without capacitors



With capacitors



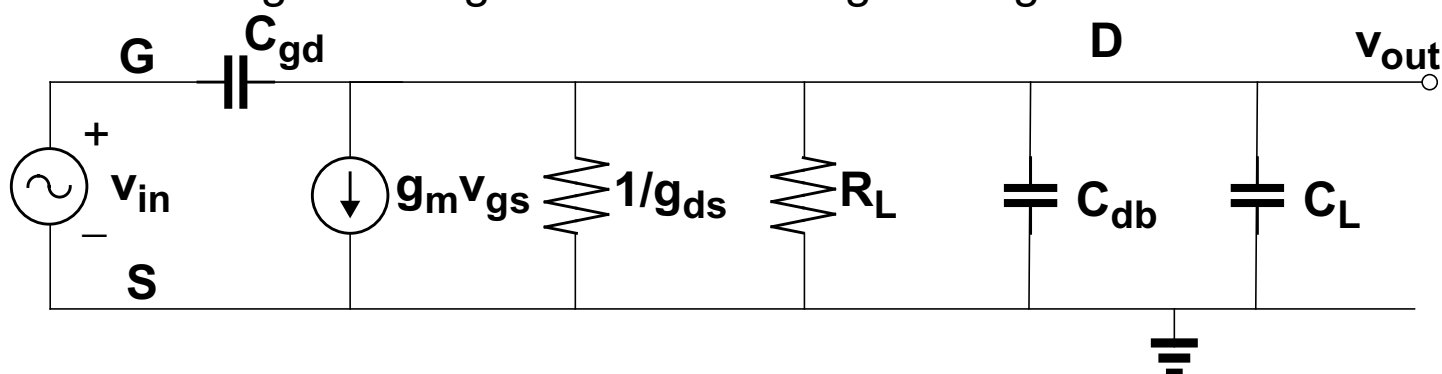
7.2.1 CS Gain stage with resistive load and capacitors



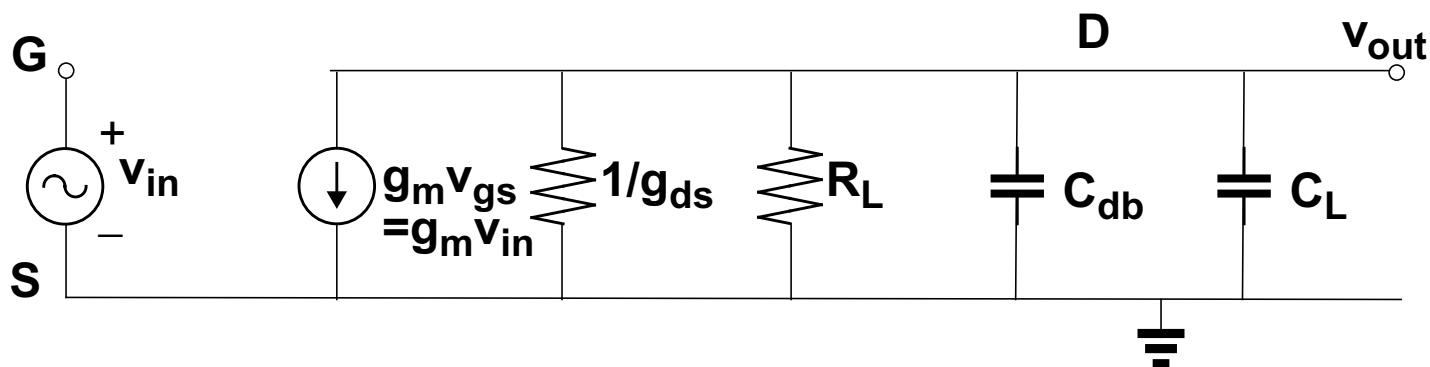
Source-bulk shorted \Rightarrow can neglect g_{mb} , C_{sb}

C_{gs} and C_{gb} are driven directly by a signal source
 \Rightarrow these can be neglected.

Now drawing small-signal model of the gain stage:



Example: Gain stage with resistive load and capacitors (contd.)



Recall: $\text{C} \parallel \text{---} Z(s) = \frac{1}{sC} \quad s = j\omega$

In first instance ignore C_{gd}

KCL at output node:

$$g_m v_{in} + v_{out} g_{ds} + \frac{v_{out}}{R_L} + v_{out} s(C_L + C_{db}) = 0$$

$$v_{out}(s) = -\frac{g_m v_{in}}{g_{ds} + \frac{1}{R_L} + s(C_L + C_{db})}$$

$$a(s) = \frac{v_{out}}{v_{in}}(s) = -\frac{g_m}{g_{ds} + \frac{1}{R_L} + s(C_L + C_{db})}$$

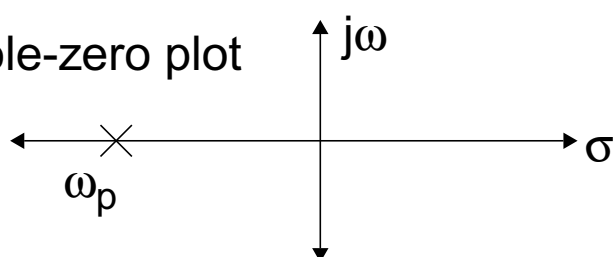
$$a(s) = \frac{v_{out}}{v_{in}}(s) = -\frac{g_m}{g_{ds} + \frac{1}{R_L}} \left(\frac{1}{1 + \frac{s(C_L + C_{db})}{g_{ds} + 1/R_L}} \right)$$

LF gain:

$$\frac{1}{1 - \frac{s}{\omega_p}}$$

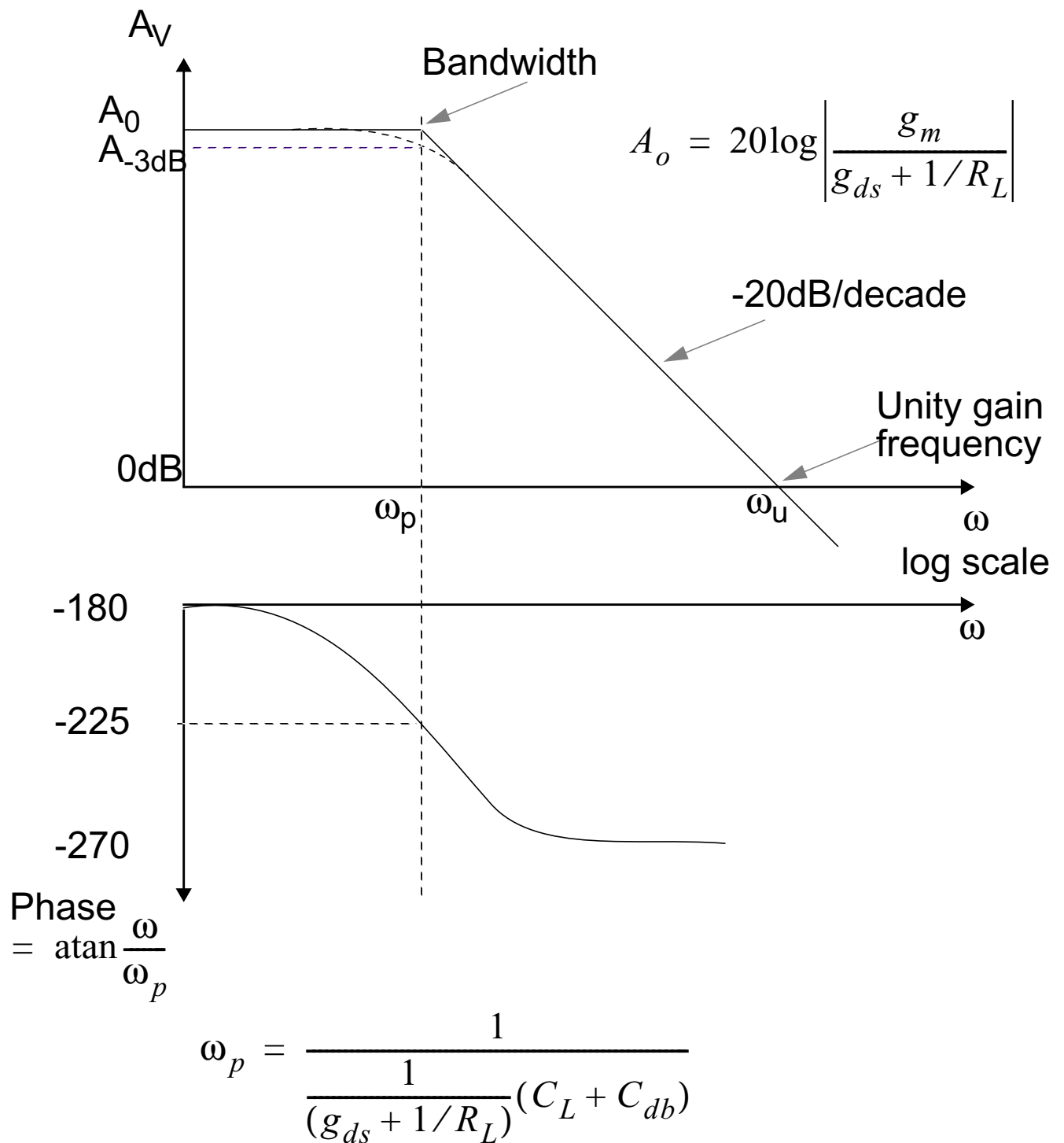
$$\omega_p = -\frac{g_{ds} + 1/R_L}{C_L + C_{db}}$$

Pole-zero plot



ω_p is the pole frequency (in rad./s)

Bode plot

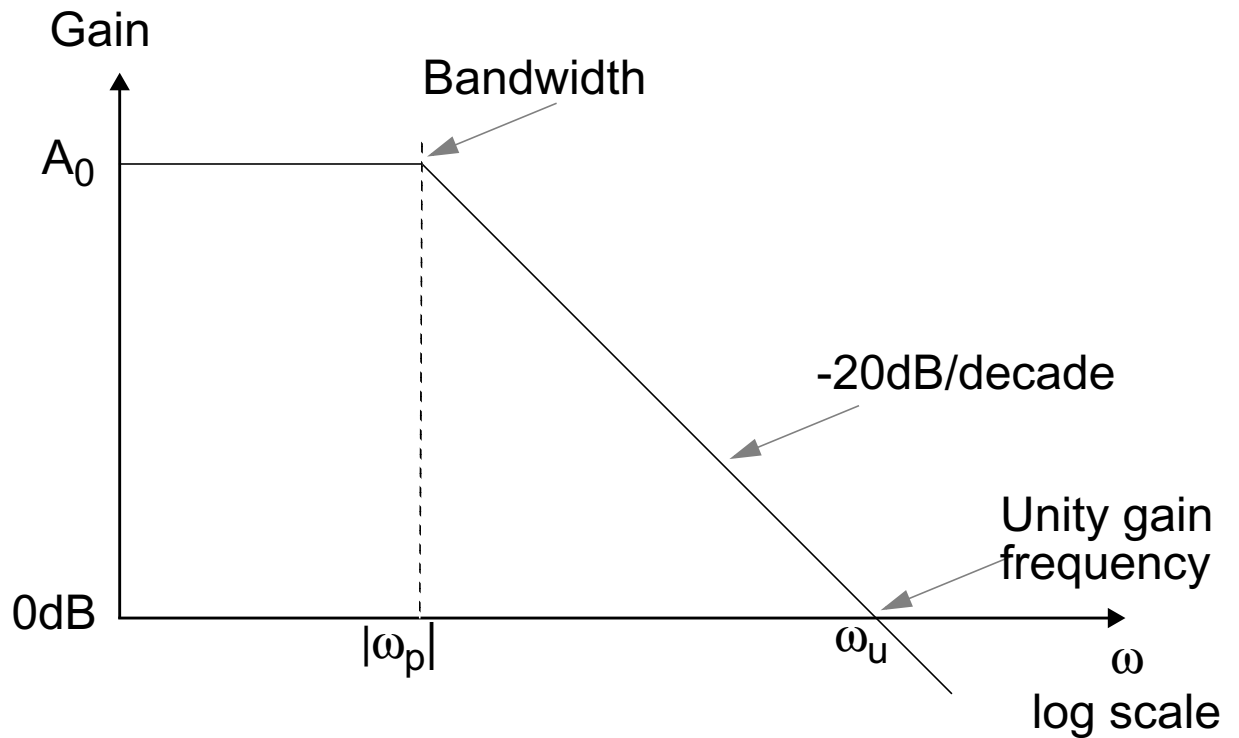


Pole associated with a node:

$$\omega_p = - \frac{1}{\text{resistance at node x capacitance at node}}$$

$$\omega_p = - \frac{\text{conductance at node}}{\text{capacitance at node}}$$

7.2.2 First-order systems



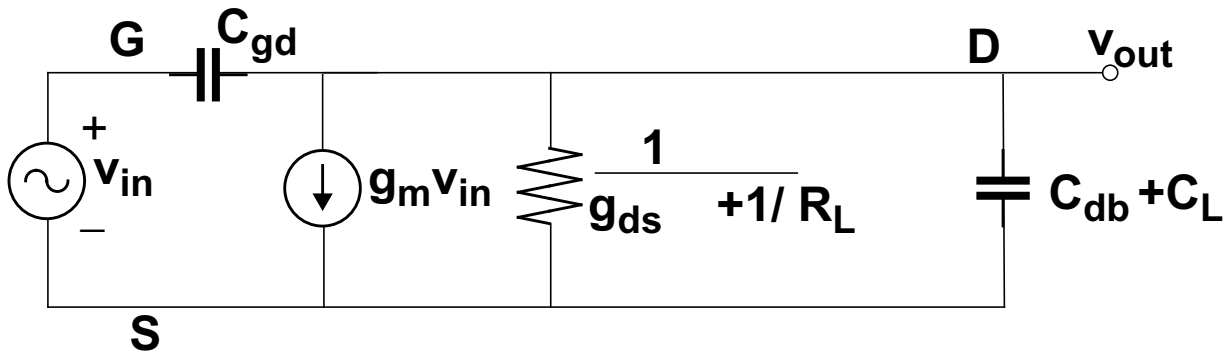
For a first order system

Unity gain frequency = Gain x Bandwidth (GBW)

Note: Bandwidth \Rightarrow 3dB bandwidth = pole frequency

$$\begin{aligned}\omega_u &= A_o |\omega_p| \\ &= \frac{g_m}{g_{ds} + 1/R_L} \cdot \frac{g_{ds1} + 1/R_L}{C_L + C_{db}} \\ &= \frac{g_m}{C_L + C_{db}}\end{aligned}$$

7.2.3 CS stage with RC load: Analysis including C_{gd}



KCL at output node:

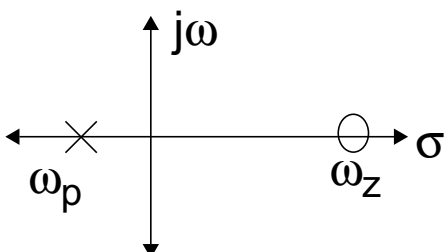
$$(v_{out} - v_{in})sC_{gd} + g_m v_{in} + v_{out}g_{ds} + \frac{v_{out}}{R_L} + v_{out}s(C_L + C_{db}) = 0$$

$$v_{in}(g_m - sC_{gd}) + v_{out}(g_{ds} + 1/R_L + s(C_{gd} + C_L + C_{db})) = 0$$

$$a(s) = \frac{v_{out}}{v_{in}}(s) = -\frac{g_m - sC_{gd}}{g_{ds} + 1/R_L + s(sC_{gd} + C_L + C_{db})}$$

$$a(s) = \frac{v_{out}}{v_{in}}(s) = -\frac{g_m}{g_{ds} + 1/R_L} \left(\frac{1 - s\frac{C_{gd}}{g_m}}{1 + \frac{s(C_{gd} + C_L + C_{db})}{g_{ds} + 1/R_L}} \right)$$

Pole-zero plot



LF gain:

$$\frac{1 - \frac{s}{\omega_z}}{1 - \frac{s}{\omega_p}}$$

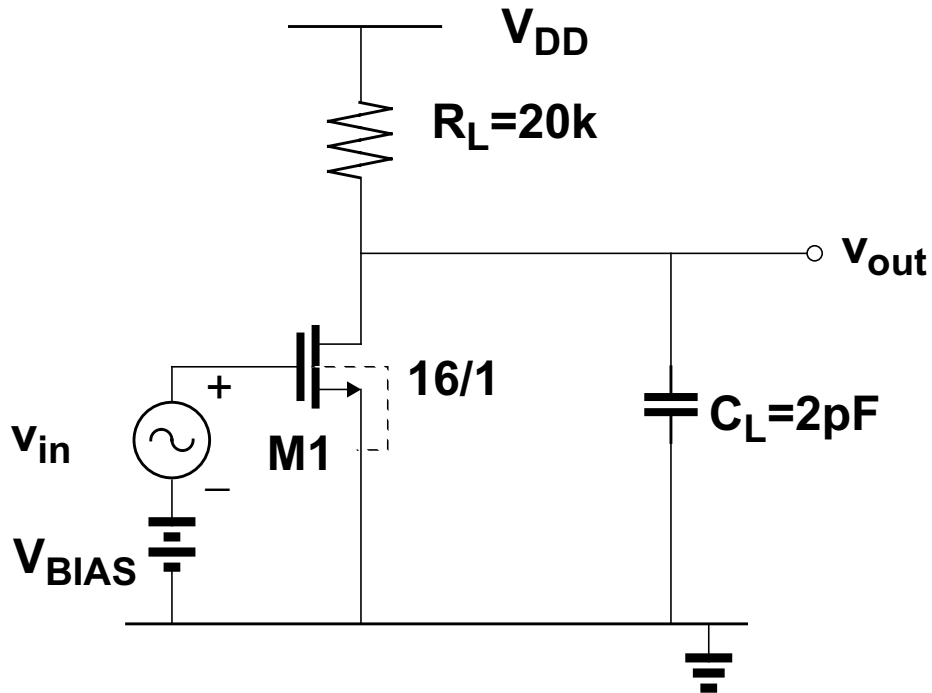
$$|\omega_z| = \frac{g_m}{C_{gd}}$$

$$|\omega_p| = \frac{g_{ds} + 1/R_L}{C_{gd} + C_L + C_{db}}$$

ω_z is the zero frequency (in rad./s)

ω_p is the pole frequency (in rad./s)

Example - CS stage, RC load



From previously: $g_m = 400\mu A/V$

$$g_{ds} = 2\mu A/V$$

Recall $\left| \frac{v_{out}}{v_{in}} \right| \cong g_m R_L = 400\mu A/V \times 20k\Omega = 8 \equiv 18dB$

$$\omega_z = \frac{g_m}{C_{gd}}$$

Take: $C_{gd} = C_{gd0l} \times W$
 $= 0.1fF/\mu m \times 16$
 $= 1.6fF$

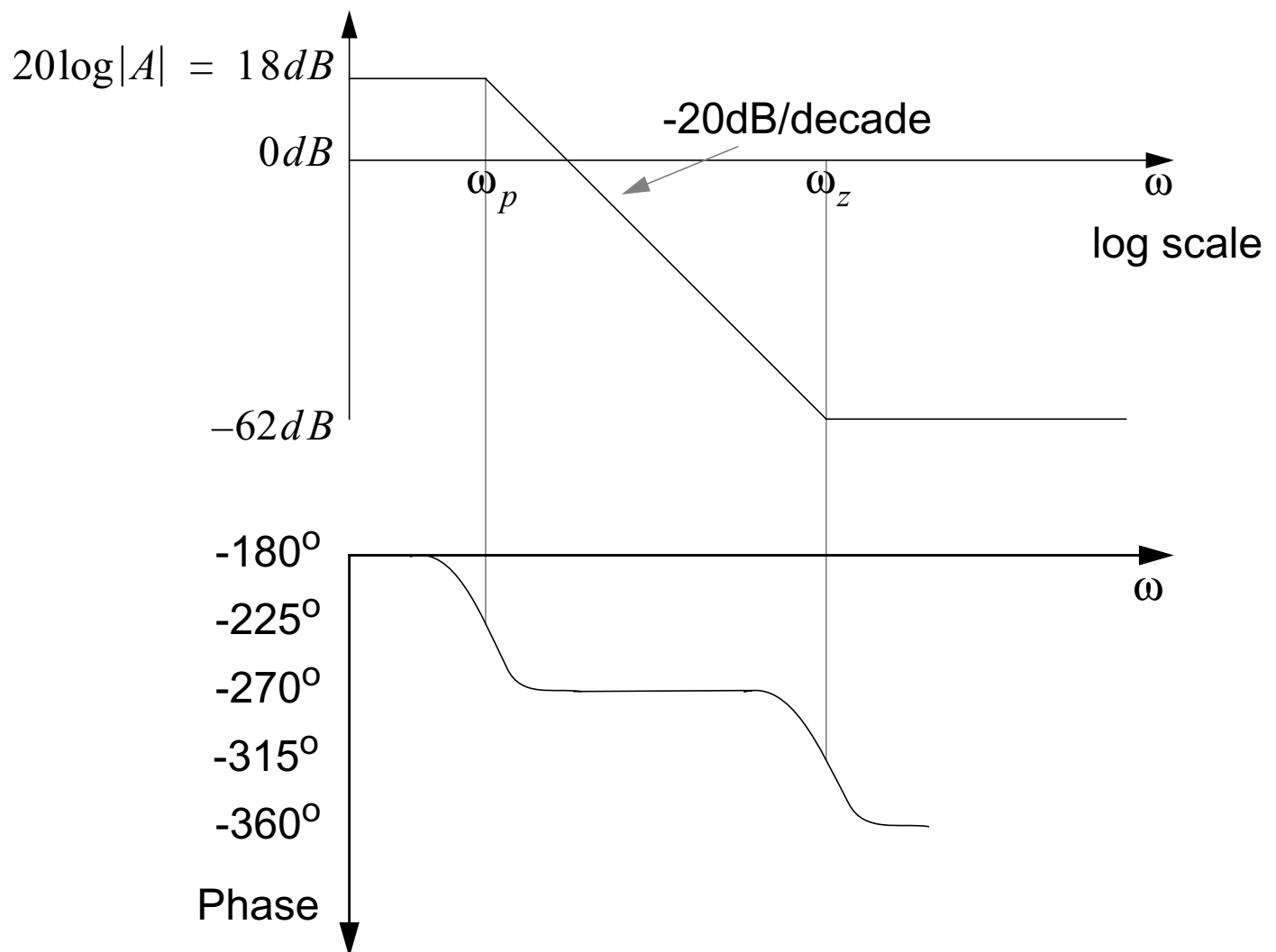
$$\omega_z = \frac{400\mu A/V}{1.6fF} = 250 Grad/s$$

$$\omega_p = \frac{g_{ds} + \frac{1}{R_L}}{C_L + C_{db} + C_{gd}}$$

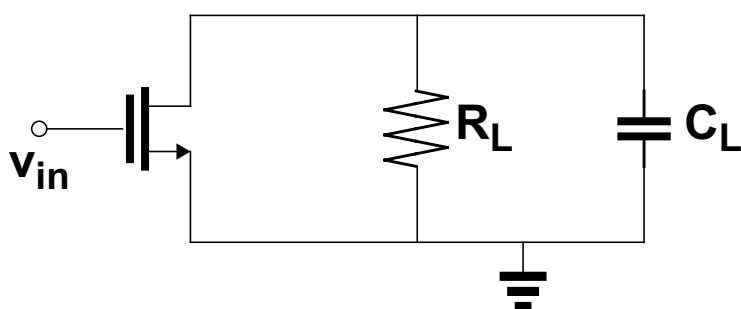
Take: $C_{db} = 1fF/\mu m \text{ of } W$
 $= 16fF$

$$\omega_p = \frac{2\mu A/V + \frac{1}{20k\Omega}}{2pF + 16fF + 1.6fF} \approx \frac{1}{20k\Omega \times 2pF} = 25Mrad/s$$

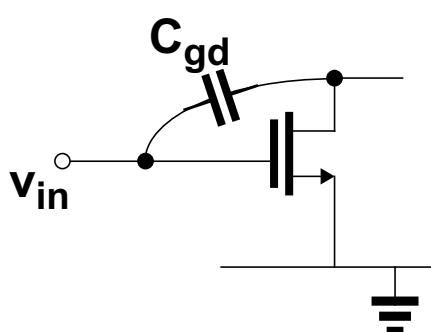
Bode plot



Explanation for pole and zero

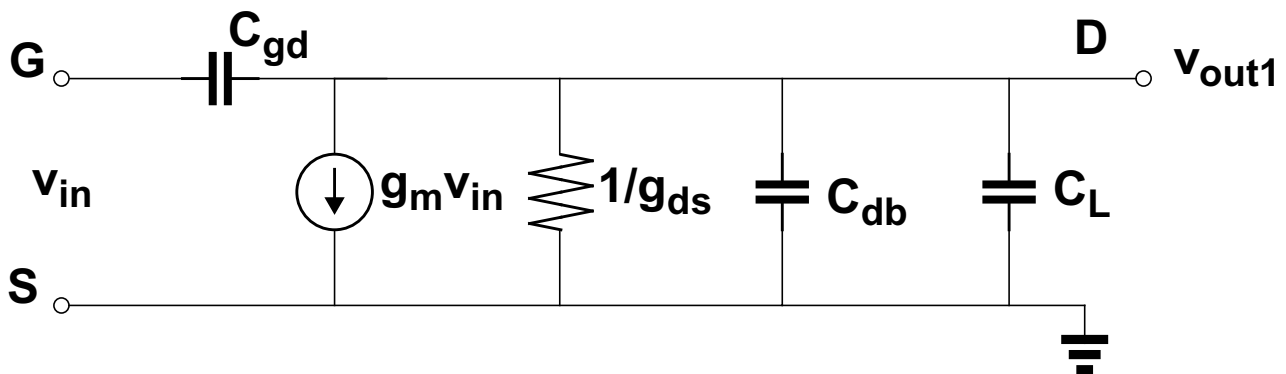
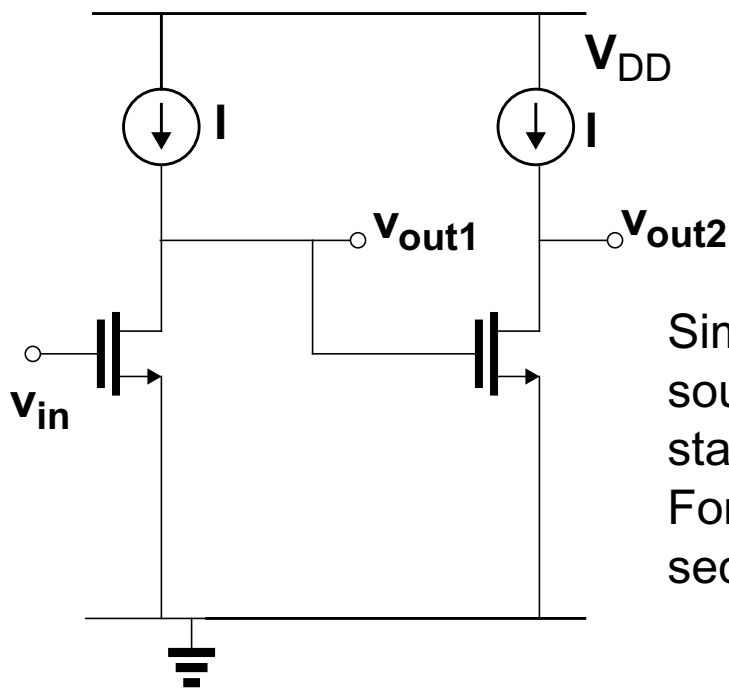


Pole occurs when the (impedance of the) capacitor takes over from the resistor R_L as the dominant load



Zero occurs when the transistor gain becomes so low that the signal feeding through C_{gd} becomes important

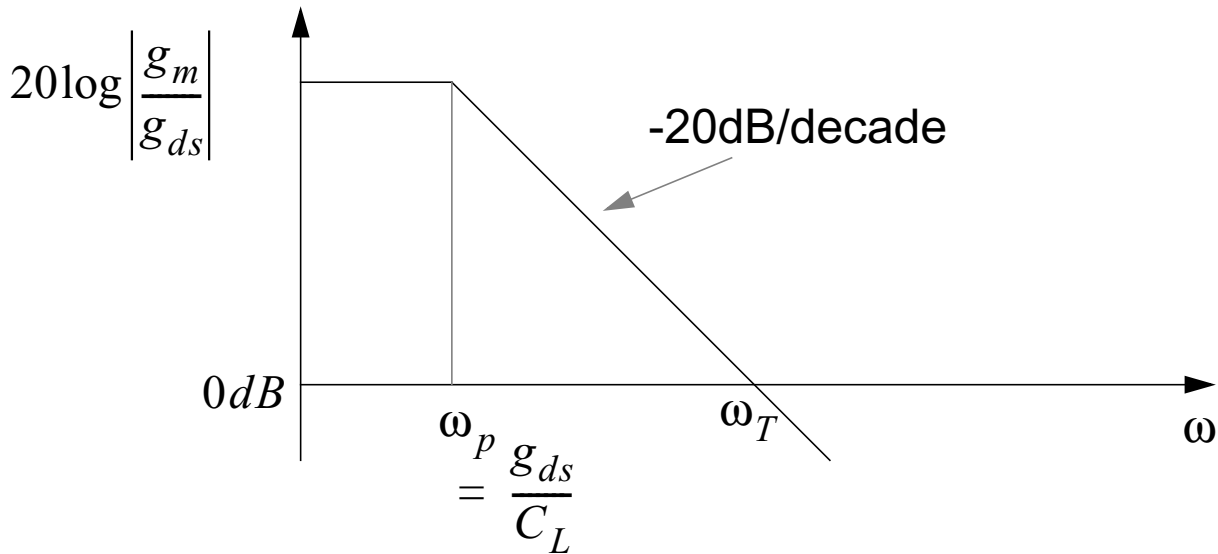
7.2.4 Maximum frequency of MOS transistor



Assume $C_L \gg C_{db}$, and ignore C_{gd}

$$a(s) = \frac{v_{out}}{v_{in}}(s) = -\frac{g_{m1}}{g_{ds1}} \left(\frac{1}{1 + \frac{sC_L}{g_{ds}}} \right)$$

Bode plot



In a single pole system the unity gain frequency is given by the product of the low-frequency gain and the bandwidth (GBW)
For transistor

$$GBW = \frac{g_m}{g_{ds}} \cdot \frac{g_{ds}}{C_L} = \frac{g_m}{C_L} \equiv \omega_T$$

$$\omega_T = \frac{g_m}{C_L}$$

Recall: $K_n' = \mu_n C_{ox}$

$$\omega_T = \frac{K_n' \frac{W}{L} (V_{GS} - V_t)}{\frac{2}{3} C_{ox} WL} = \frac{\frac{3}{2} \mu_n (V_{GS} - V_t)}{L^2}$$

For NMOS in typical $0.5\mu\text{m}$ process ($\mu_n = 580\text{cm}^2/\text{V/s}$)

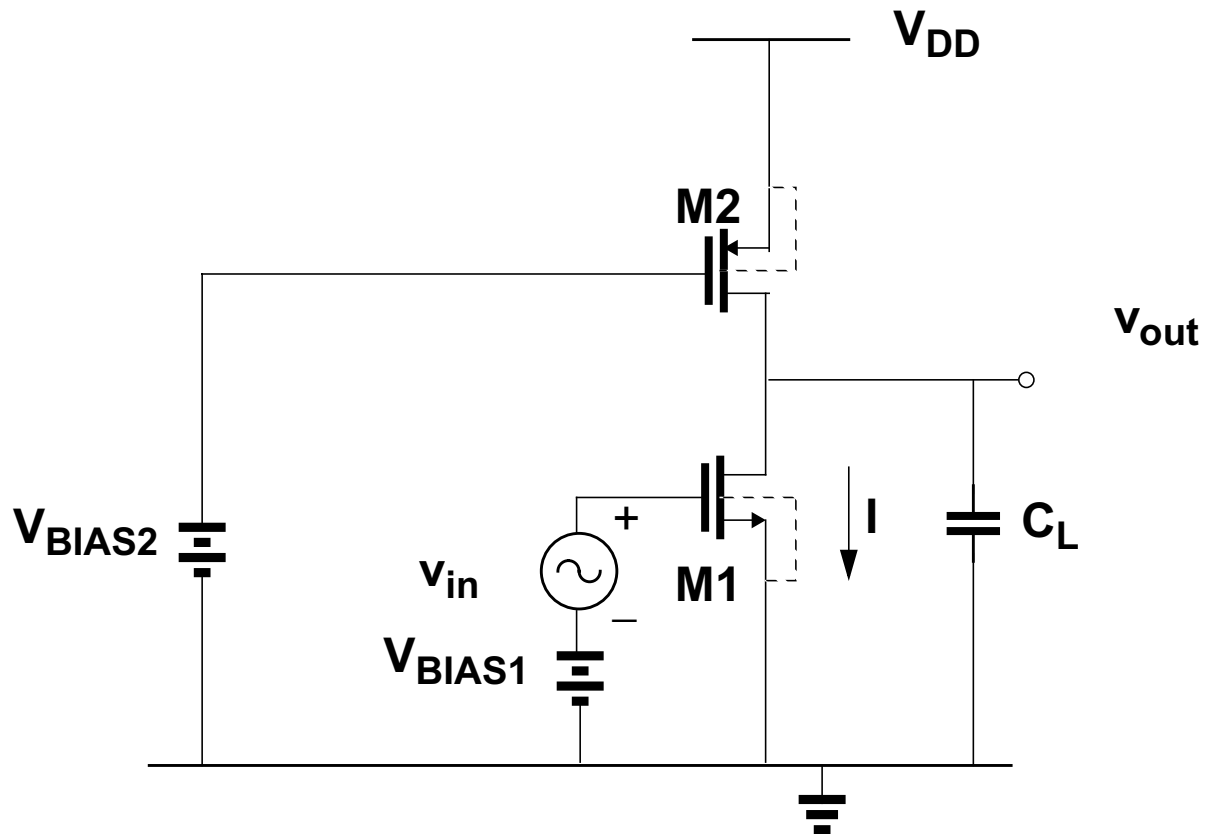
Take $V_{GS} - V_t = 400\text{mV}$

$$\omega_T = \frac{\frac{3}{2} 580 \times 0.4 V}{(0.5 \times 10^{-4})^2} = 139 \times 10^9 \text{ Rad/s}$$

$$f_T = \frac{\omega_T}{2\pi} = 22.1 \text{ GHz}$$

In practice get less due to C_{db}

Problem: CS stage with active load, h.f. analysis



$$V_{BIAS1}=1.3, V_{BIAS2}=1.7, V_{DD}=3$$

$$V_{tn}=0.8V, V_{tp}=-0.8V,$$

$$\lambda_p=0.04/L \text{ V}^{-1}, \lambda_n=0.04/L \text{ V}^{-1}$$

$$K_n'=160\mu\text{A/V}, K_p'=40\mu\text{A/V}$$

$$W_1=10, L_1=1, W_2=40, L_2=1$$

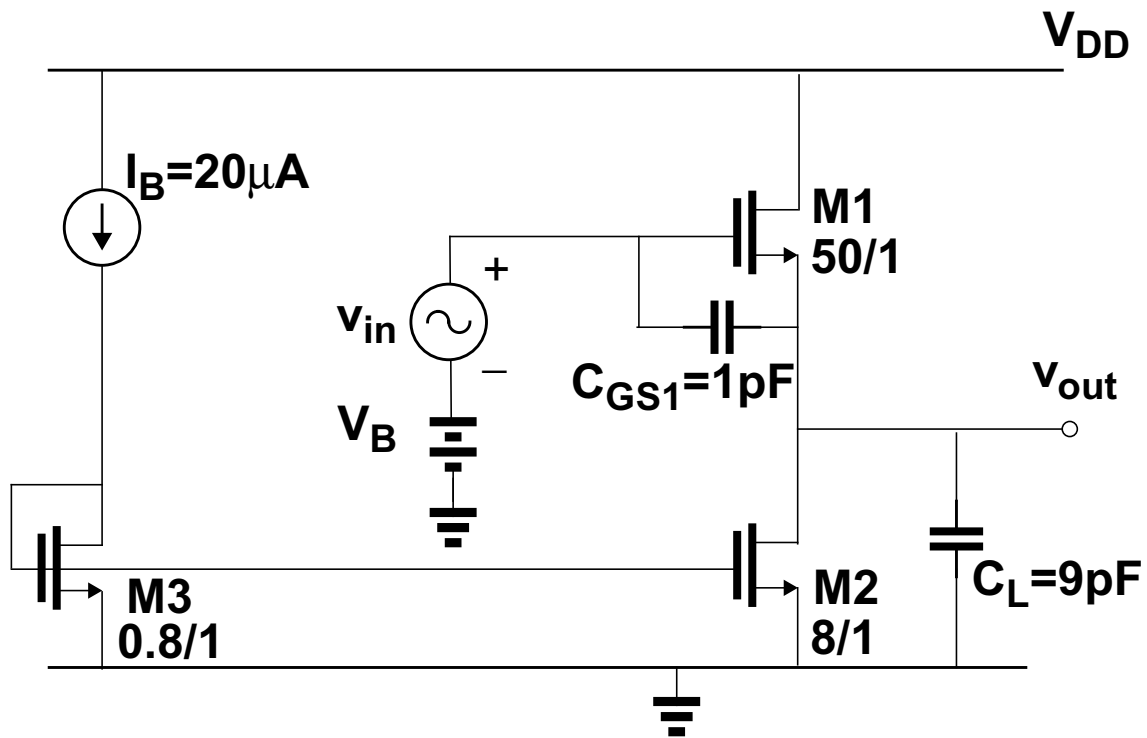
$$C_L=1\text{pF}$$

Assume all transistors are in saturation.

Ignore all capacitances except C_L

- (i) Draw the small-signal model
- (ii) Derive an expression for the gain in terms of the small-signal parameters and the load capacitance
- (iii) What is the pole frequency?
- (iv) What is the GBW?
- (v) What is the effect on the gain, pole frequency and GBW if the bias current is doubled?

Problem: Source follower stage, h.f. analysis

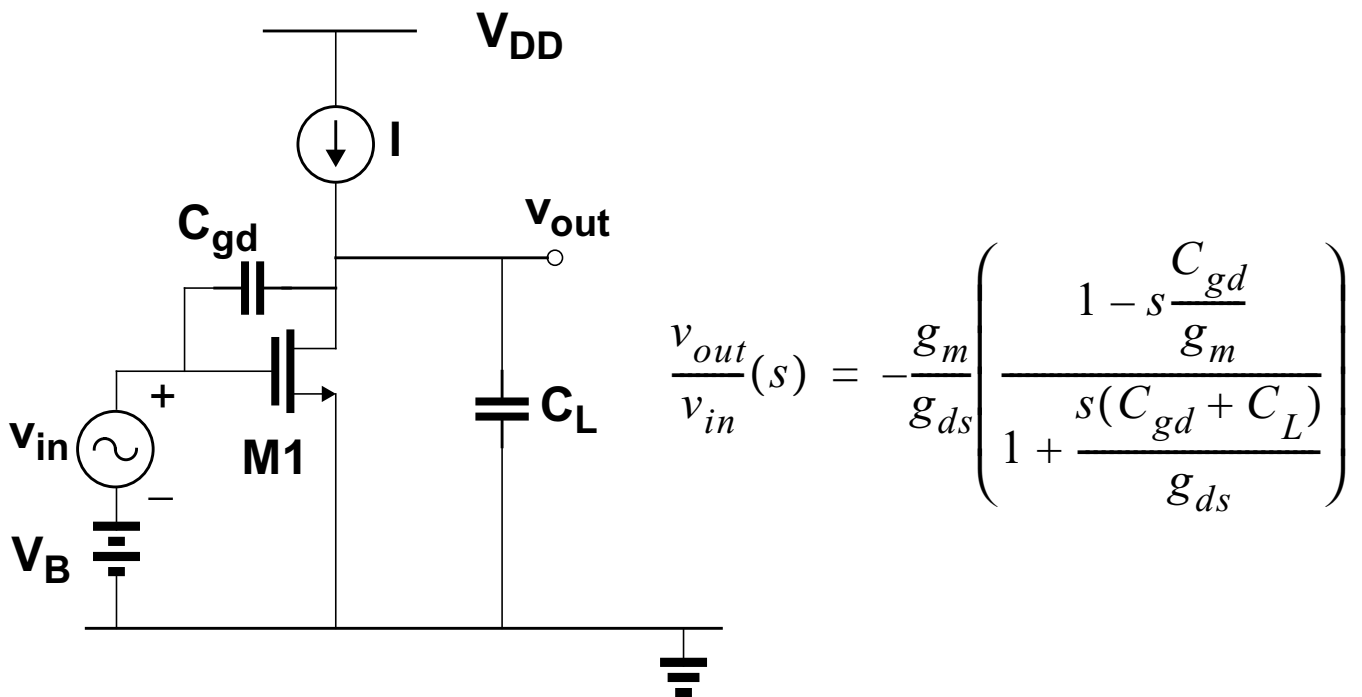


Take $K_n' = 200 \mu\text{A}/\text{V}^2$.

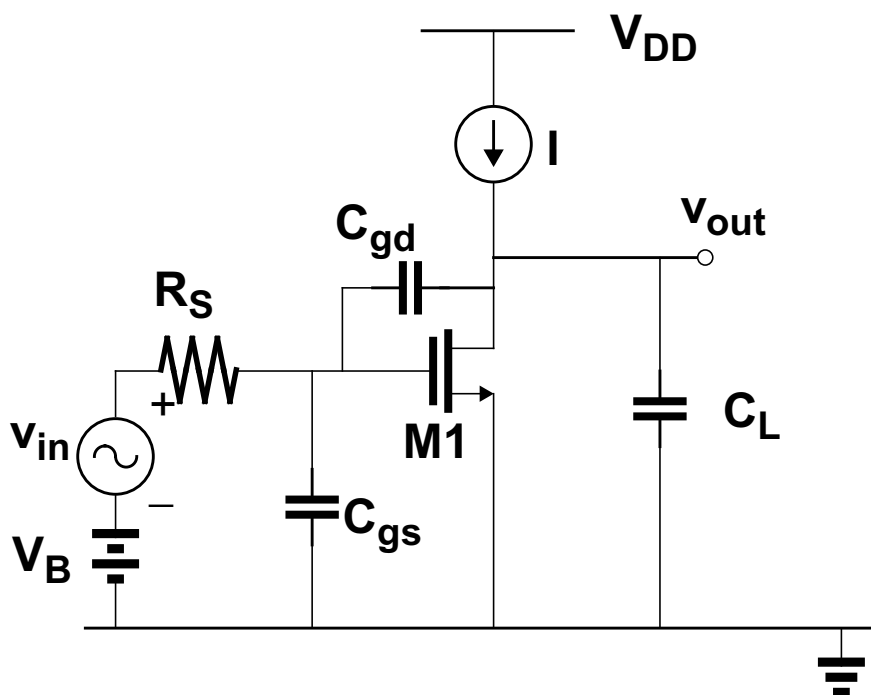
Assume all transistors are in saturation and $g_{m1}, g_{m2} \gg g_{ds1}, g_{ds2}$.

- Draw the small-signal equivalent circuit for the source follower stage shown.
- Derive an expression for the high-frequency transfer function.
- Calculate the dc gain in dB, and the break frequencies (i.e. pole and/or zero frequencies).
- Draw a Bode diagram of the gain response.
What is the value of gain at frequencies well above the break frequencies?

7.3 CS stage with finite source resistance (Miller effect)



In theory there is a pole at the input node (at infinity)
What if a source resistance is present?

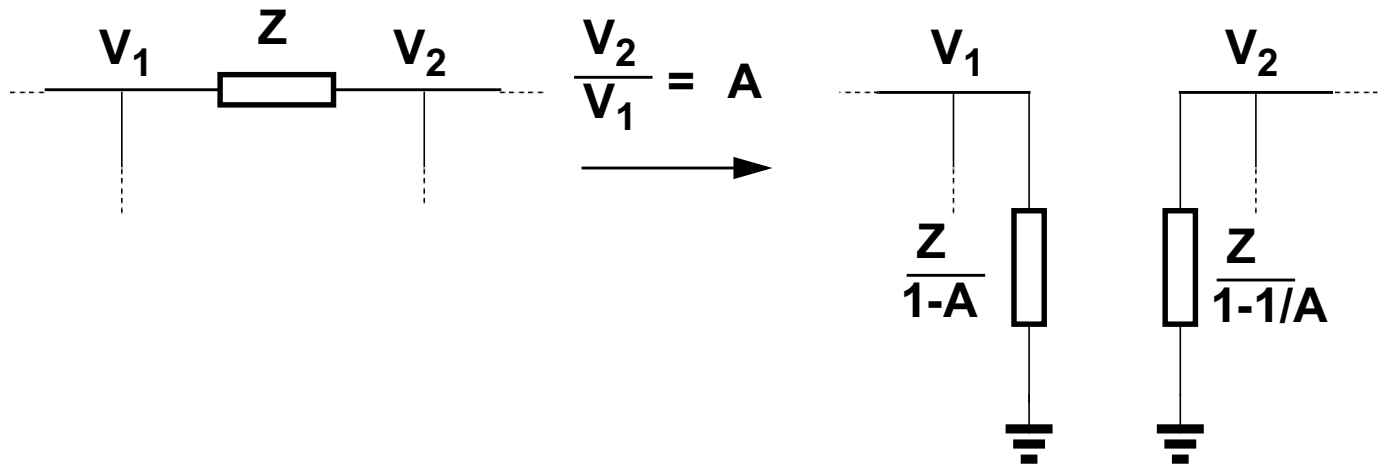


Now the pole at the gate of M1 is at a finite frequency given by

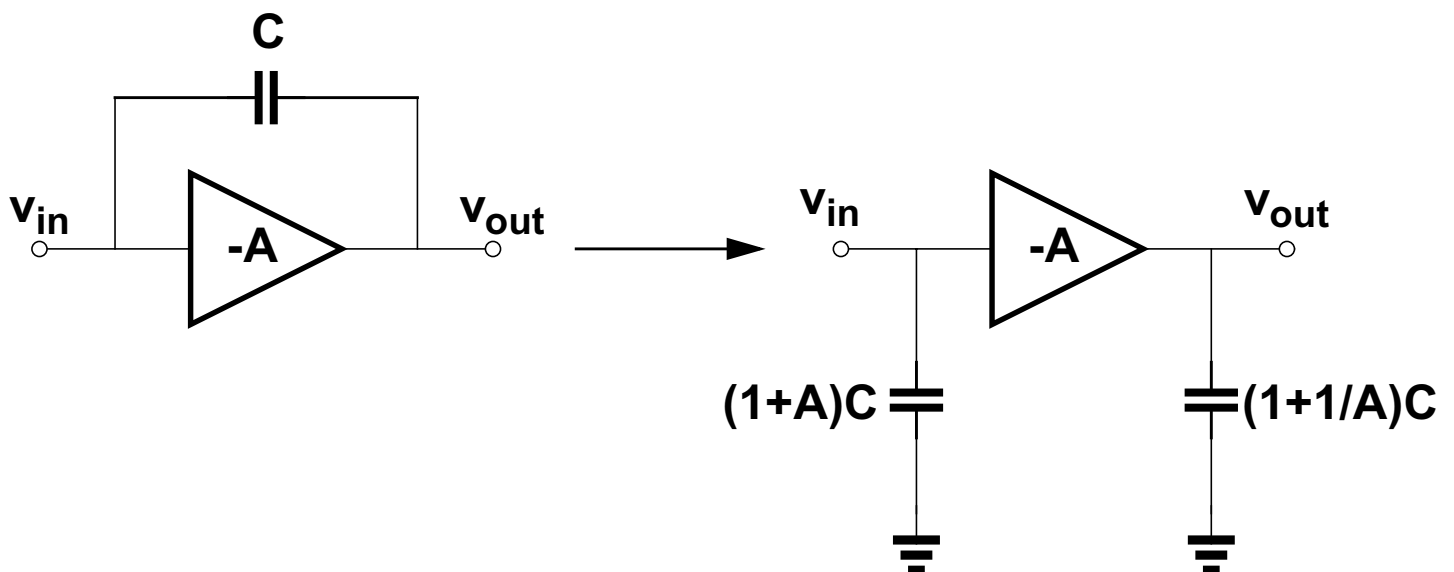
$$\omega_p = -\frac{1}{\text{resistance at node} \times \text{capacitance at node}}$$

7.3.1 Miller effect

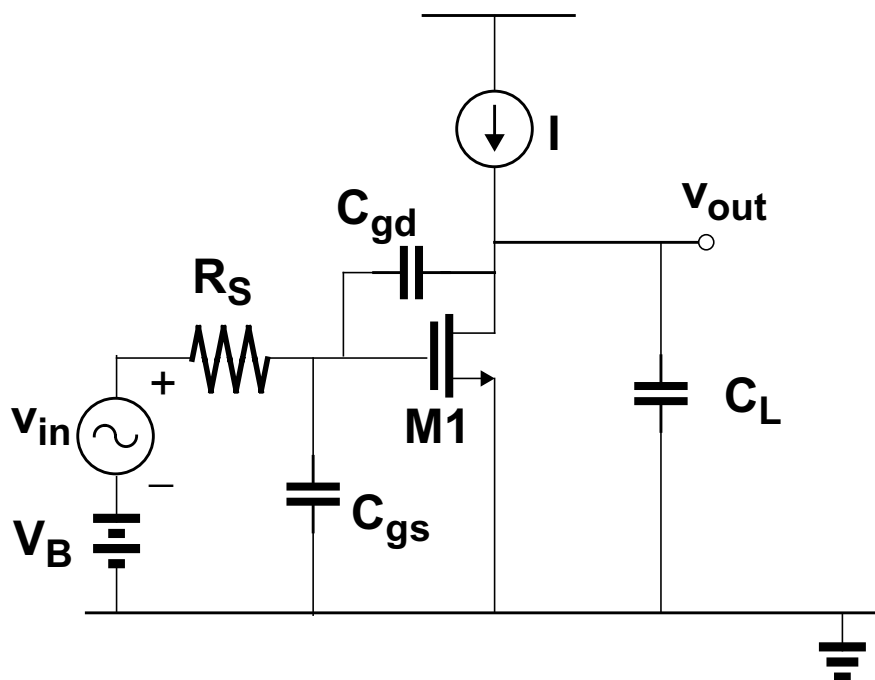
Miller's Theorem If two nodes V_1 and V_2 are connected by an impedance Z , then this branch can be replaced by two branches connecting the nodes to ground with impedances as shown below.



Most common application is the effective multiplication of a capacitance across a negative gain device



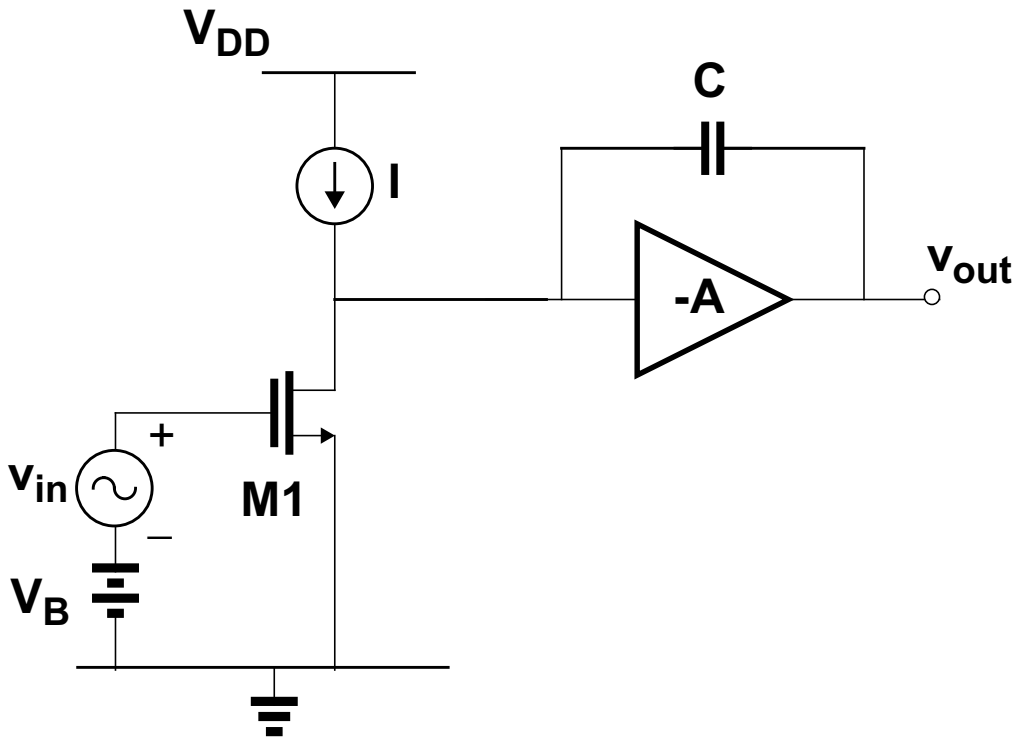
CS with finite source resistance (Miller Effect), contd.



Now the pole at the gate of M1 is approximately given by

$$|\omega_p| = \frac{1}{R_S \left[C_{gs} + C_{gd} \left(1 + \frac{g_{m1}}{g_{ds1}} \right) \right]}$$

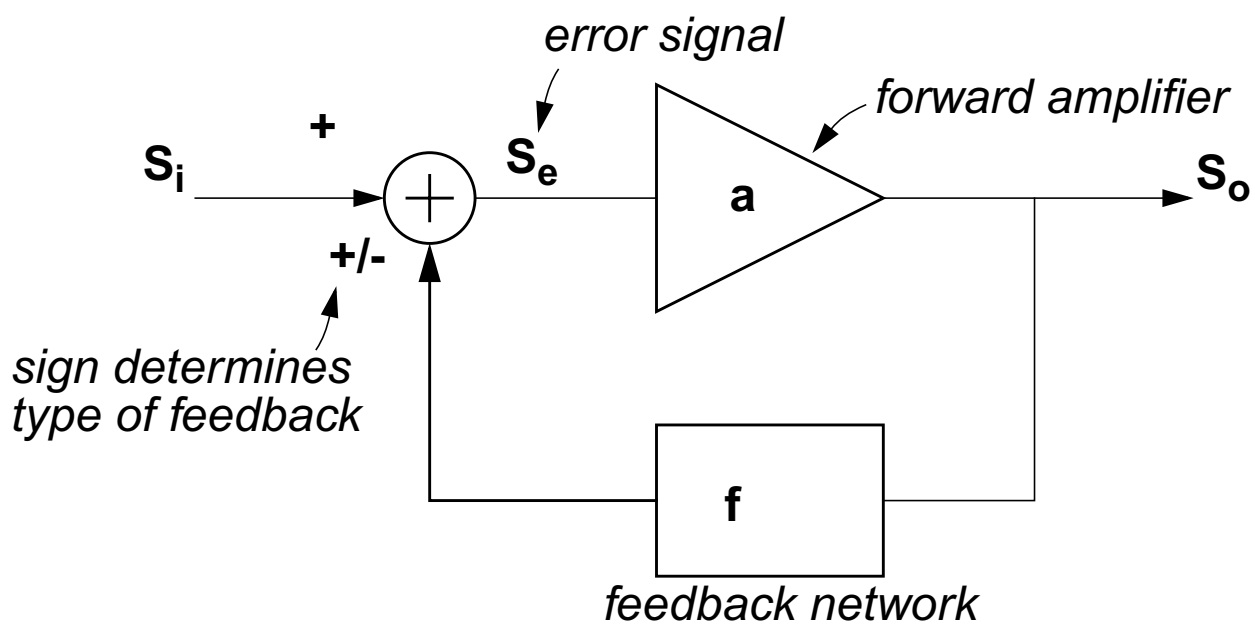
Problem: Miller capacitance.



A gain stage is cascaded with an ideal amplifier with gain $-A$. Assume M1 is in saturation.

- (i) Write an expression for the small-signal low-frequency voltage gain (v_{out}/v_{in}) of this circuit.
- (ii) Write an expression for the frequency of the dominant pole
- (iii) Calculate the small-signal voltage gain, and the pole frequency if
 W/L of M1 = 25/1, $V_B = 1V$, $V_{tn} = 0.75V$, $K_n' = 200\mu A/V^2$, $\lambda_n = 0.04V^{-1}$
 $A = -100$, $C = 1pF$.

8 Feedback



2 types of feedback:

Positive feedback

Feedback signal is added to input signal

Used in design of oscillators

Negative feedback

Feedback signal is subtracted from input signal

Used in design of amplifiers

Here we deal with negative feedback

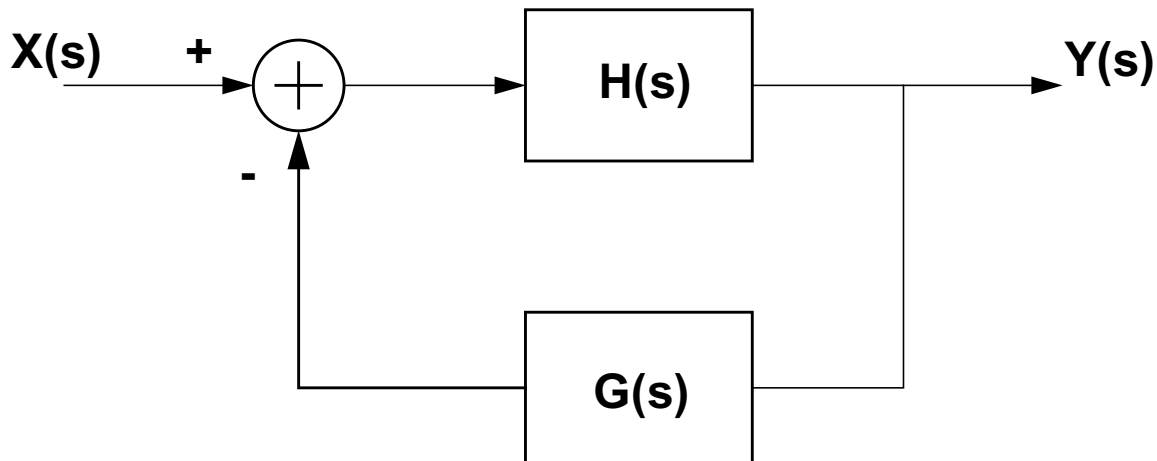
What can negative feedback do for us?

1. Gain desensitization: reduce sensitivity to changes in forward gain
2. Enables us to trade gain for bandwidth
3. Modify input, output impedances

But.. always issues with stability when we use feedback.

8.1 Negative feedback

8.1.1 General Negative Feedback system



$$Y(s) = H(s)(X(s) - G(s)(Y(s)))$$

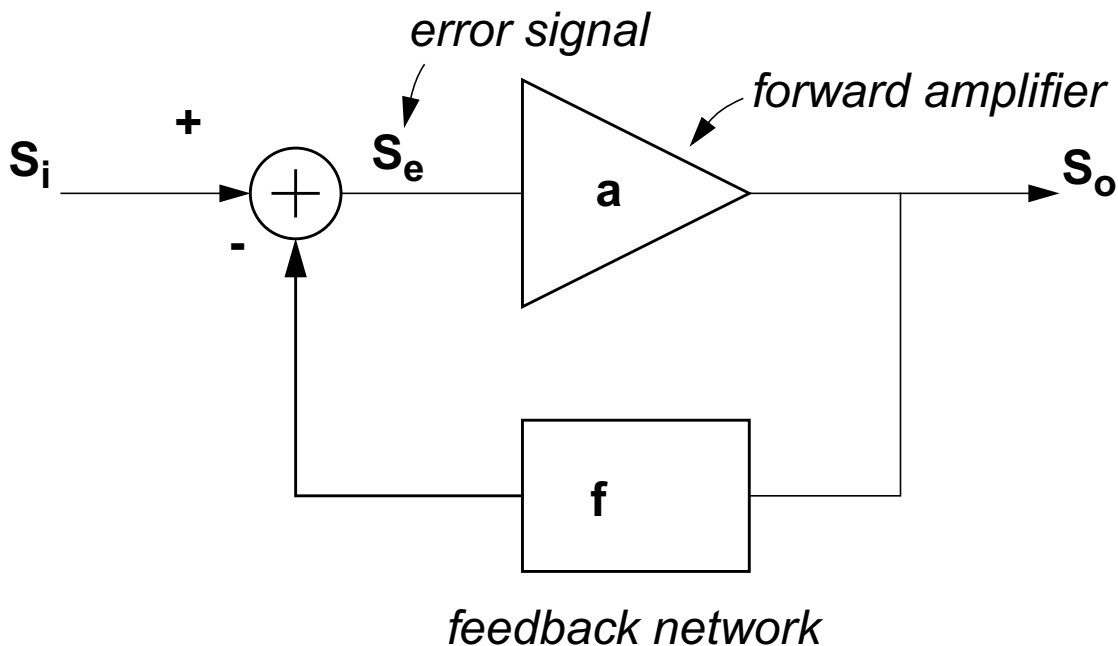
Closed loop transfer function:
$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 + G(s)H(s)}$$

$H(s)$: Open-loop transfer function
 $G(s)H(s)$: Loop gain

Most cases of interest to us: $H(s)$ is an amplifier and $G(s)$ is a passive and frequency-independent network (e.g. resistive divider).

8.1.2 Negative feedback - electronic system

Electronic system, low-frequency model



$$S_o = a(S_i - fS_o)$$

Closed loop transfer function:
$$\frac{S_o}{S_i} = \frac{a}{1 + af}$$

a : amplifier gain
 f : feedback factor
 af : loop gain

If loop gain is large i.e. $af \gg 1$ then

$$\frac{S_o}{S_i} = A = \frac{a}{1 + af} \cong \frac{1}{f}$$

Note:

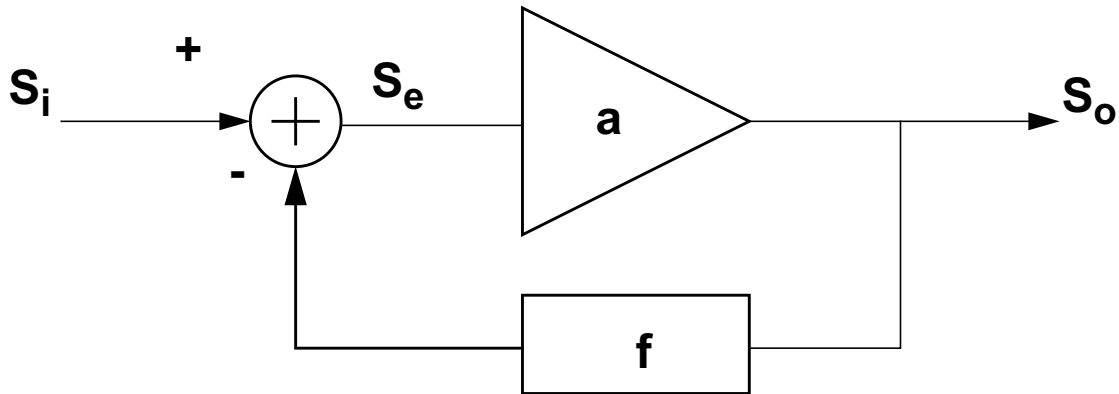
Gain is approx. independent of amplifier gain a

Feedback network which determines f is usually resistor divider or capacitor divider so closed loop gain A is stable

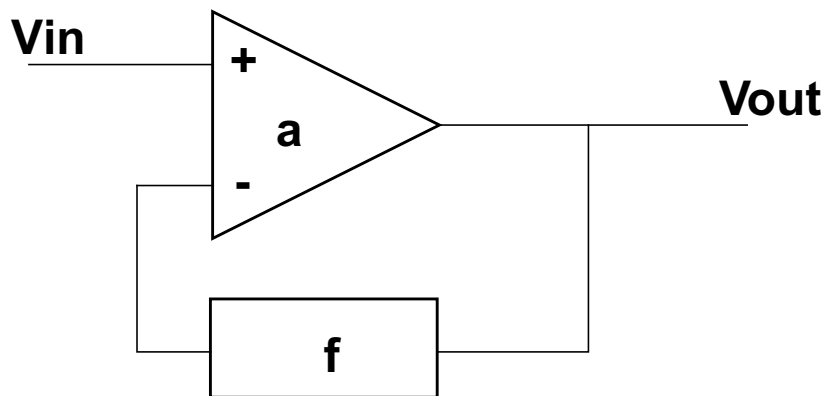
Feedback network passive $\Rightarrow f$ less than or equal to 1.

Product af also known as T

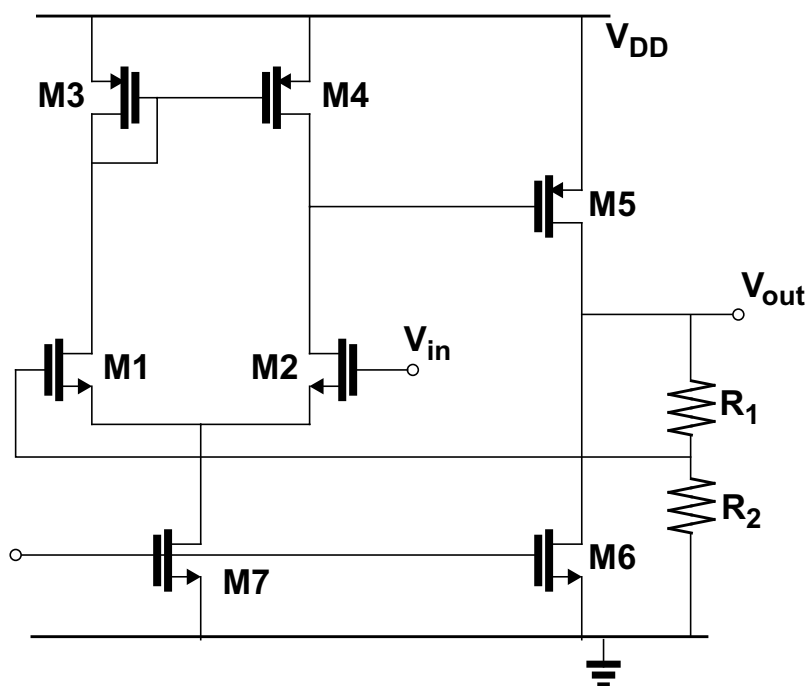
8.1.3 Feedback and Opamps



General negative feedback maps onto opamp structure

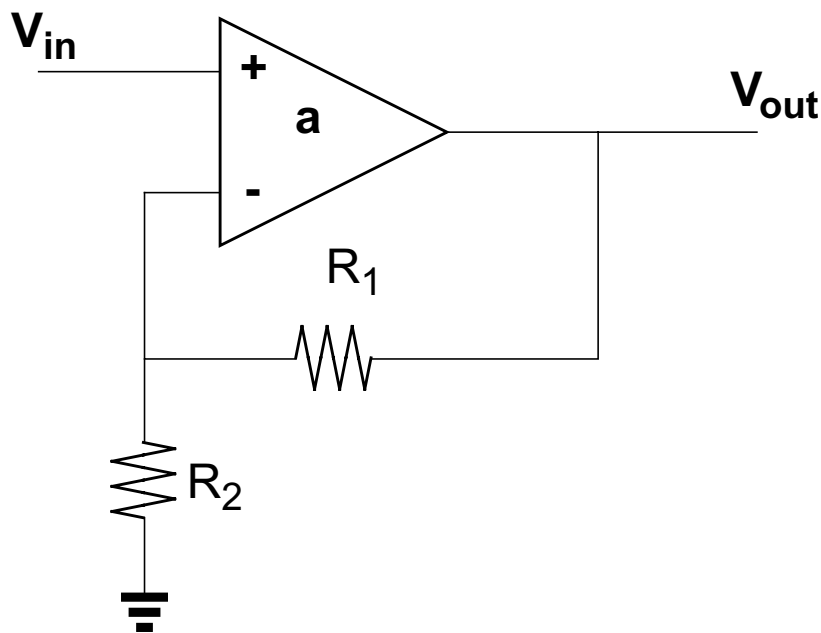


For example, our 2 stage opamp with resistive divider feedback nw



Example: Non-inverting voltage amplifier

Voltage amplifier:



Feedback quantity: voltage

Feedback factor: $f = \frac{R_2}{R_1 + R_2}$

Calculate gain: $V_{out} = a \left(V_{in} - \frac{R_2}{R_1 + R_2} V_{out} \right)$

$$\frac{V_{out}}{V_{in}} = \frac{a}{1 + a \cdot \frac{R_2}{R_1 + R_2}}$$

If loop gain $\gg 1$ i.e. if $a \cdot \frac{R_2}{R_1 + R_2} \gg 1$

then $\frac{V_{out}}{V_{in}} \cong \frac{R_1 + R_2}{R_2} = \frac{1}{f}$

8.1.4 Gain sensitivity of negative feedback amplifier

What is the sensitivity of the closed-loop gain A to

1. variations in the forward gain a
2. variations in the feedback factor f

1. Sensitivity of A w.r.t variation of forward gain a

$$A = \frac{a}{1 + af}$$

$$\frac{dA}{da} = \frac{1 + af - af}{(1 + af)^2} = \frac{A}{a} \left(\frac{1}{1 + af} \right)$$

$$\frac{dA}{A} = \frac{\frac{da}{a}}{1 + af}$$

Fractional change in A is equal to the fractional change in a attenuated by $1 + af$

=> desensitization: if the forward gain a varies with process, temperature time then the overall gain varies much less if af large

Note:

In IC technology the absolute values of gain (a) show a large spread (from batch to batch, over temperature) (typically $\pm 50\%$ 3σ)

Feedback enables us to stabilize the gain

2. Sensitivity of A w.r.t variation of feedback factor gain f

$$A = \frac{a}{1 + af}$$

$$\frac{dA}{df} = -\frac{a^2}{(1 + af)^2} = \frac{A}{f} \left(-\frac{af}{1 + af} \right)$$

$$\frac{dA}{A} = \frac{\frac{df}{f}}{-\frac{1 + af}{af}} \approx -\frac{df}{f} \quad \text{if } af \gg 1$$

Fractional change in A is approximately equal to the fractional change in f and is not attenuated by $1+af$

=> for accurate A need accurate feedback factor f .

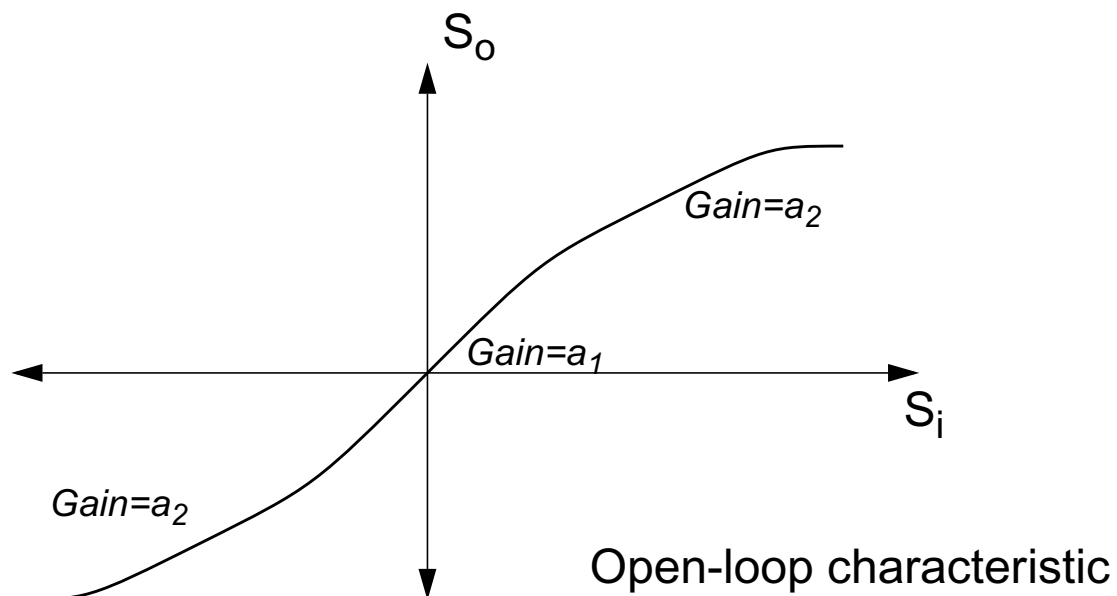
f is usually set by resistor or capacitor ratios.

Note:

In IC technology the absolute values of resistors and capacitors show a large spread (from batch to batch, temperature) (typically +20% 3σ)

However the ratio of matched resistors or capacitors on a chip (f) is highly accurate (typically $< \pm 1\text{-}2\%$ 3σ , depending on device size)

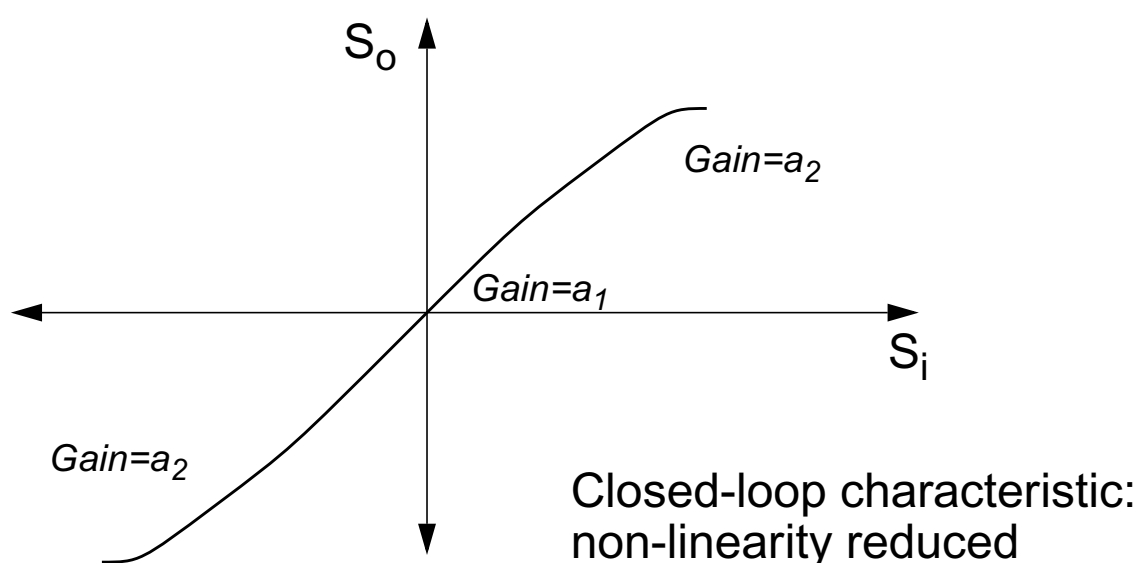
8.1.5 Effect of feedback on nonlinearity (distortion)



Non-linear amplifier: with two regions of (open-loop) gain a_1 and a_2
When this amplifier is used in a feedback configuration the two closed-loop gains A_1 and A_2 are given by

$$A_1 = \frac{a_1}{1 + a_1 f} \cong \frac{1}{f} \quad \text{if } a_1 f \gg 1$$
$$A_2 = \frac{a_2}{1 + a_2 f} \cong \frac{1}{f} \quad \text{if } a_2 f \gg 1$$

i.e. closed loop gain set by feedback factor, not by open loop gain

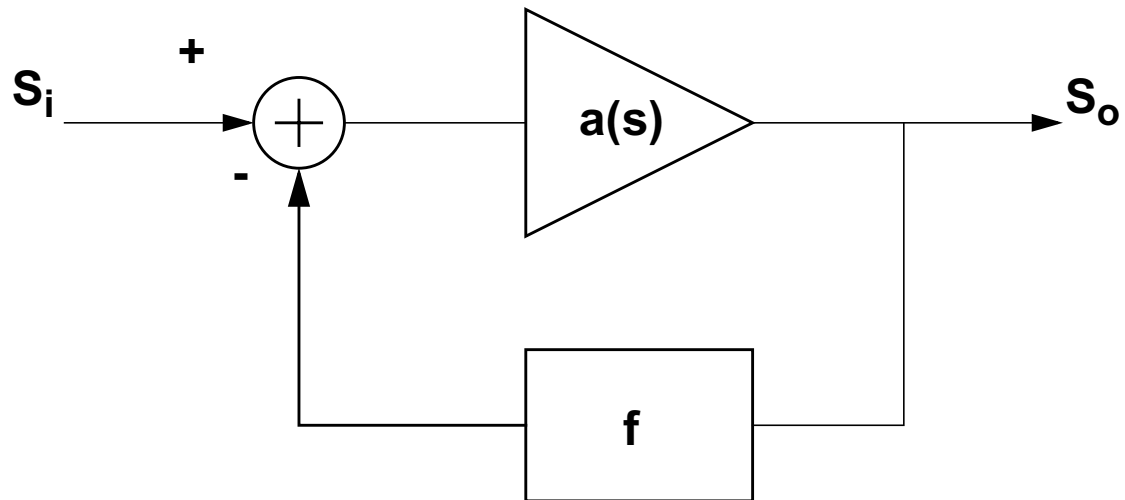


Note: 1. scales compressed.
2. saturation of amplifier for large input signals

8.2 Feedback and high-frequency effects

8.2.1 Feedback and bandwidth

Feedback allows us to trade gain for bandwidth



$$A = \frac{a(s)}{1 + a(s)f}$$

Assume an amplifier with a single pole at ω_{p1} :

$$a(s) = \frac{a_0}{1 - \frac{s}{\omega_{p1}}}$$

Closed loop gain is then given by:

$$A(s) = \frac{a(s)}{1 + a(s)f} = \frac{\frac{a_0}{1 - \frac{s}{\omega_{p1}}}}{1 + \frac{a_0}{1 - \frac{s}{\omega_{p1}}}f} = \frac{a_0}{1 - \frac{s}{\omega_{p1}} + a_0f}$$
$$A(s) = \frac{a_0}{1 + a_0f} \left(\frac{1}{1 - \frac{s}{\omega_{p1}(1 + a_0f)}} \right)$$

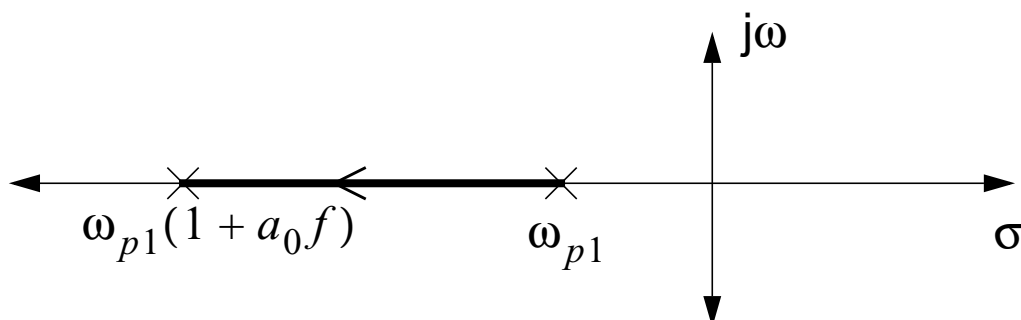
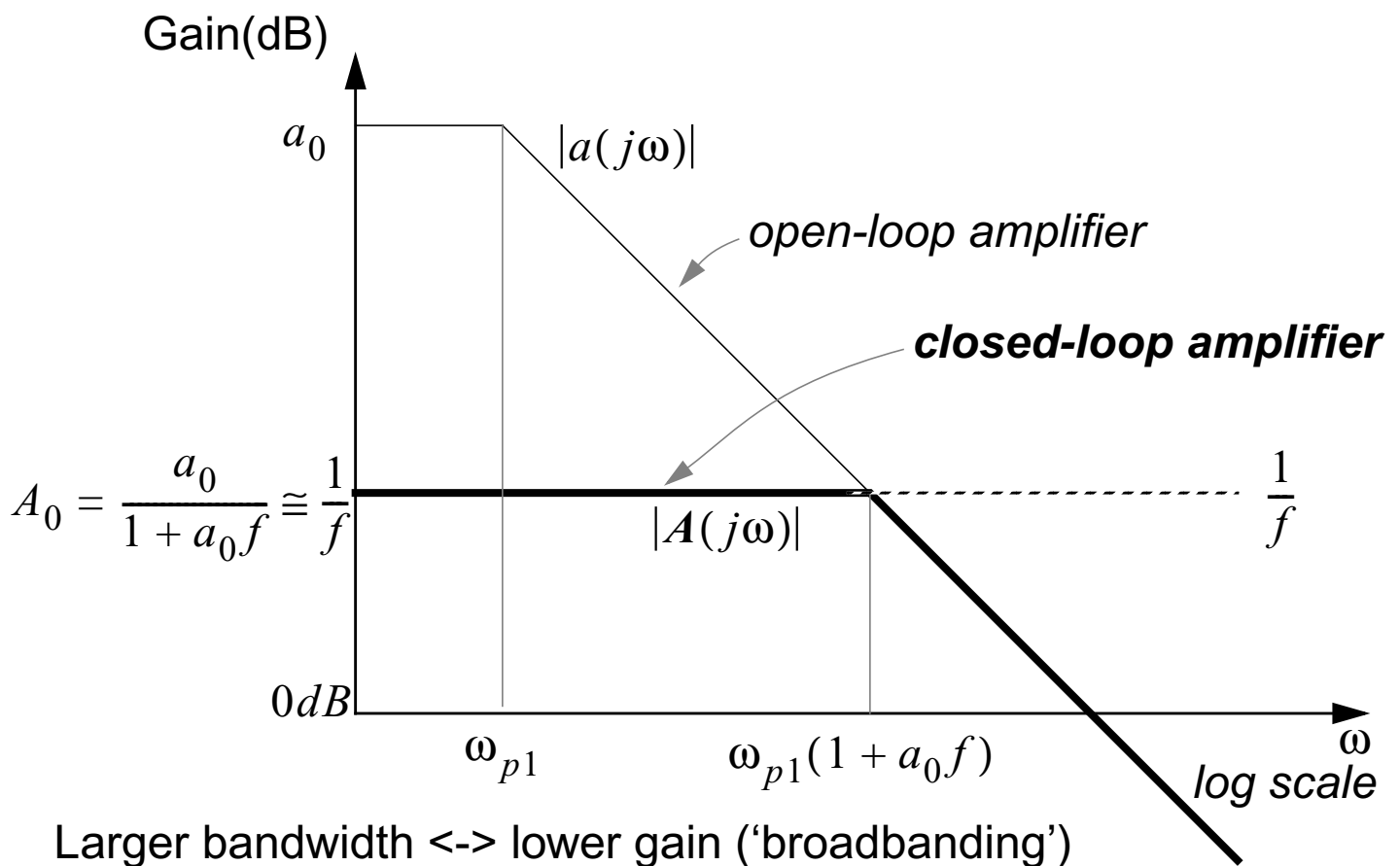
Feedback and bandwidth (contd.)

$$a(s) = \frac{a_0}{1 - \frac{s}{\omega_{p1}}}$$

open-loop amplifier pole at ω_{p1}

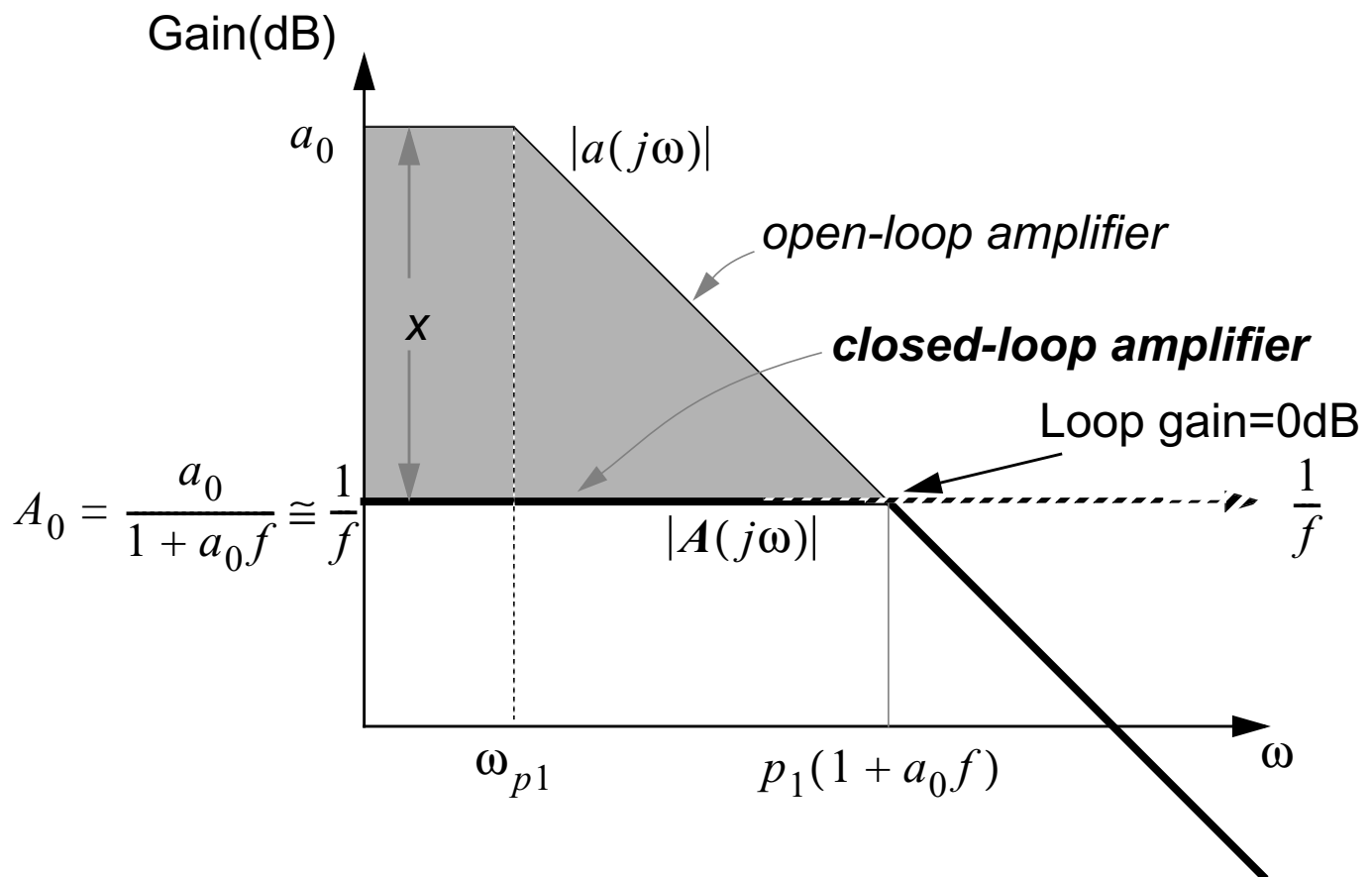
$$A(s) = \frac{a_0}{1 + a_0 f} \left(\frac{1}{1 - \frac{s}{\omega_{p1}(1 + a_0 f)}} \right)$$

closed loop amplifier pole at $\omega_{p1}(1 + a_0 f)$



Note on loop gain (1):

If $a_0 f \gg 1$ then the loop gain is the difference between the open-loop curve and the closed-loop curve in the Bode diagram



$$x = 20\log|a(j\omega)| - 20\log\left(\frac{1}{f}\right)$$

$$x = 20\log|a(j\omega)f| \quad \text{i.e. } x \text{ is the loop gain in dB}$$

$$x = 20\log|T(j\omega)|$$

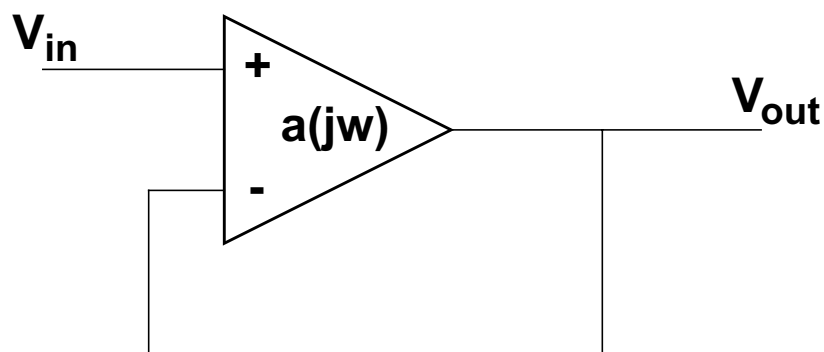
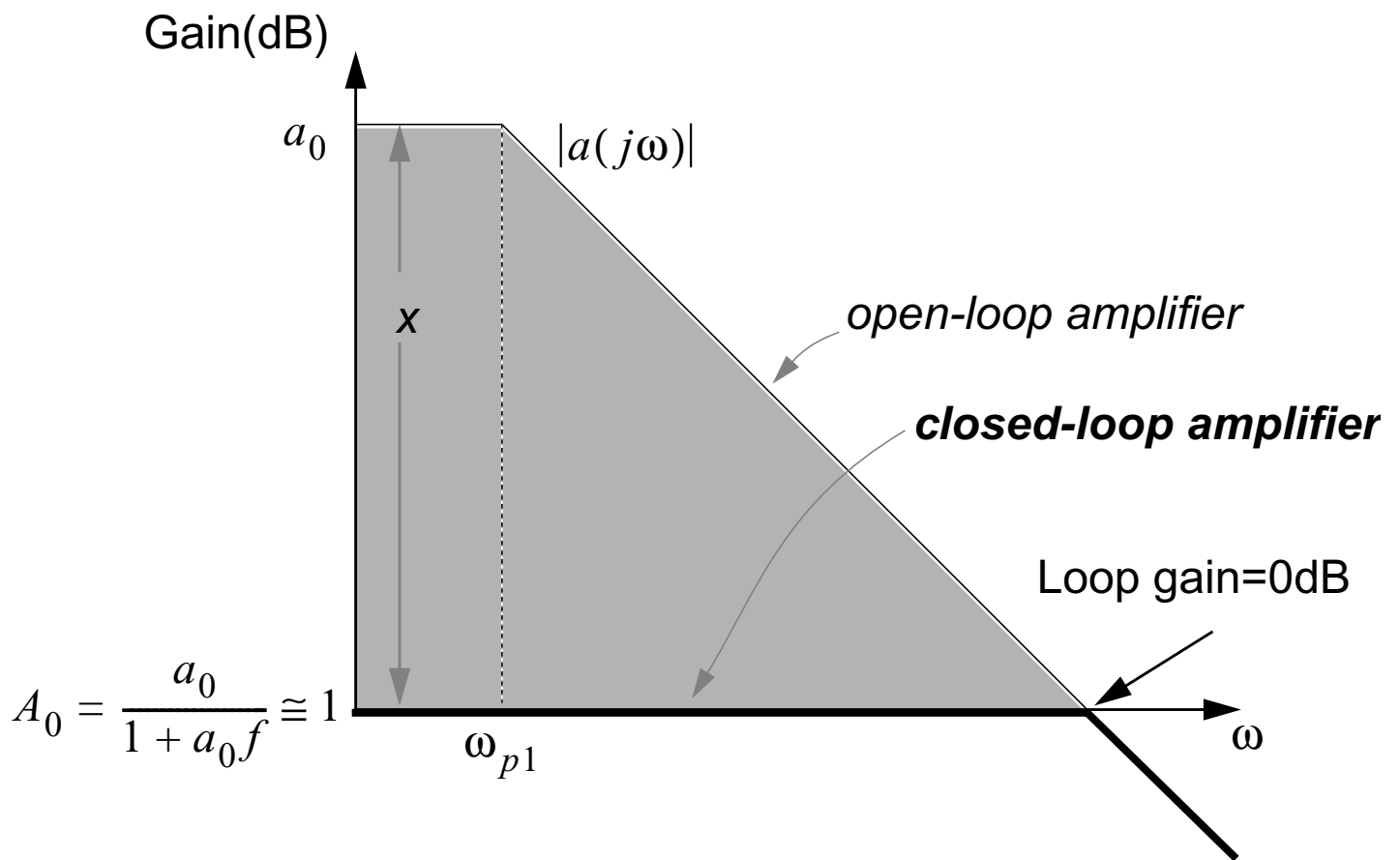
=> shaded region indicates loop gain



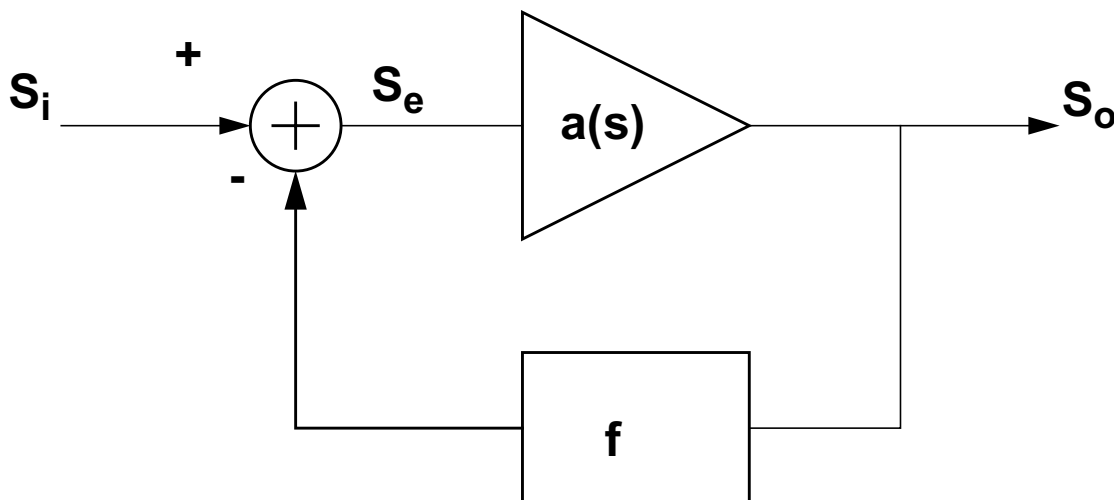
Loop gain falls to 0dB at $\omega_{p1}(1+a_0 f)$. Beyond this frequency the loop gain $|a(j\omega)f|$ or $|T(j\omega)|$ goes towards 0 and the feedback has no influence on the gain of the closed loop amplifier, i.e. open and closed loop characteristics coincide.

Note on loop gain (2):

If $f = 1$ then the loop gain $a_0 f$ is equal to a_0 and the Bode plot of the loop gain is the same as the Bode plot of the open-loop amplifier



8.2.2 Negative feedback and stability



Amplifier has a limited bandwidth, i.e. a signal propagating through it will experience a time delay due to internal RC's (poles, zeroes)

If for say a sine-wave input the delay is such that the feedback signal is inverted, and its magnitude is equal to or greater than the original signal we get positive feedback => instability

For stability of a negative feedback system: if a signal experiences 180° phase delay around the loop then the gain around the loop must be less than 1

Stability criterion:

When phase of the loop gain $a(j\omega)f$ is equal to or greater than 180° then the amplitude of the loop gain $a(j\omega)f$ must be less than 1

Note: In any feedback system 360° phase shift around the loop is required for oscillation. Negative Feedback gives us 180° phase shift so the loop itself would need to generate the remaining 180° .

For a system with m zeroes and n poles

$$A(s) = \frac{A_o \left(1 - \frac{s}{\omega_{z1}}\right) \left(1 - \frac{s}{\omega_{z2}}\right) \dots \left(1 - \frac{s}{\omega_{zm}}\right)}{\left(1 - \frac{s}{\omega_{p1}}\right) \left(1 - \frac{s}{\omega_{p2}}\right) \dots \left(1 - \frac{s}{\omega_{pn}}\right)}$$

$$|A(j\omega)| = \frac{A_o \sqrt{1 + \left(\frac{\omega}{\omega_{z1}}\right)^2} \sqrt{1 + \left(\frac{\omega}{\omega_{z2}}\right)^2} \dots \sqrt{1 + \left(\frac{\omega}{\omega_{zm}}\right)^2}}{\sqrt{1 + \left(\frac{\omega}{\omega_{p1}}\right)^2} \sqrt{1 + \left(\frac{\omega}{\omega_{p2}}\right)^2} \dots \sqrt{1 + \left(\frac{\omega}{\omega_{pn}}\right)^2}}$$

In dB:

$$20\log|A(j\omega)| = 20\log A_o + 20\log \sqrt{1 + \left(\frac{\omega}{\omega_{z1}}\right)^2} + 20\log \sqrt{1 + \left(\frac{\omega}{\omega_{z1}}\right)^2} + \dots$$

$$\dots + 20\log \sqrt{1 + \left(\frac{\omega}{\omega_{zn}}\right)^2} - 20\log \sqrt{1 + \left(\frac{\omega}{\omega_{p1}}\right)^2}$$

$$- 20\log \sqrt{1 + \left(\frac{\omega}{\omega_{p2}}\right)^2} - \dots - 20\log \sqrt{1 + \left(\frac{\omega}{\omega_{pn}}\right)^2}$$

For phase: each left-hand plane pole and each right hand plane zero contributes -90° phase shift

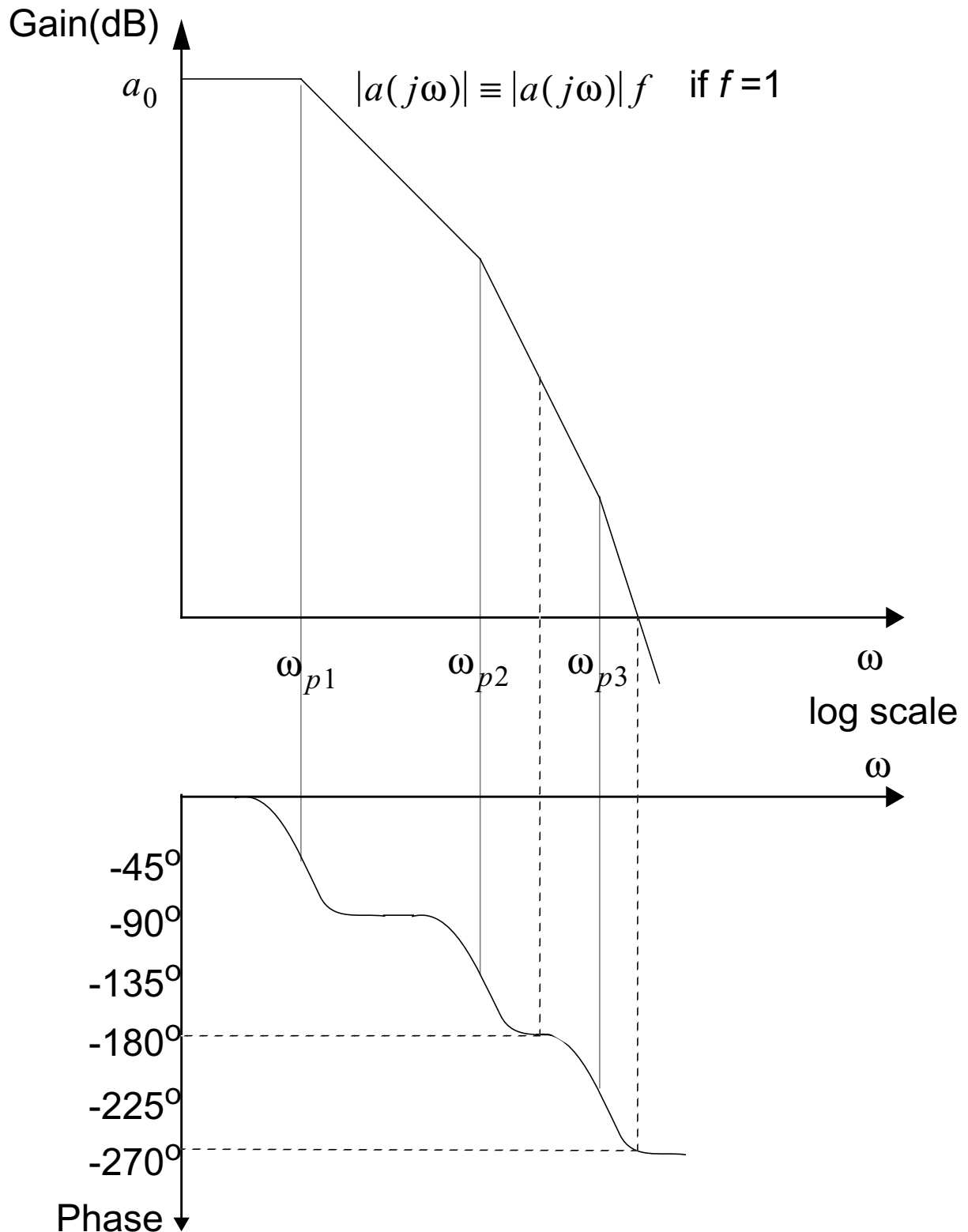
$$\text{Phase}(A(j\omega)) = -\text{atan}\left(\frac{\omega}{\omega_{z1}}\right) - \text{atan}\left(\frac{\omega}{\omega_{z2}}\right) - \dots - \text{atan}\left(\frac{\omega}{\omega_{zn}}\right)$$

$$- \text{atan}\left(\frac{\omega}{\omega_{p1}}\right) - \text{atan}\left(\frac{\omega}{\omega_{p2}}\right) - \dots - \text{atan}\left(\frac{\omega}{\omega_{pn}}\right)$$

8.2.3 Feedback factor and stability

Example: Amplifier with three poles at ω_{p1}, ω_{p2} and ω_{p3}

Plot the loop gain $|a(j\omega)f|$ with large feedback factor (e.g. $f=1$)



Large feedback factor $f=1$. So $a(j\omega)f = a(j\omega)$.

Gain in this case $|a(j\omega)f|$ is greater than 1 (0dB) when phase is 180° (phase shift also $> 180^\circ$ when gain down to 0dB)

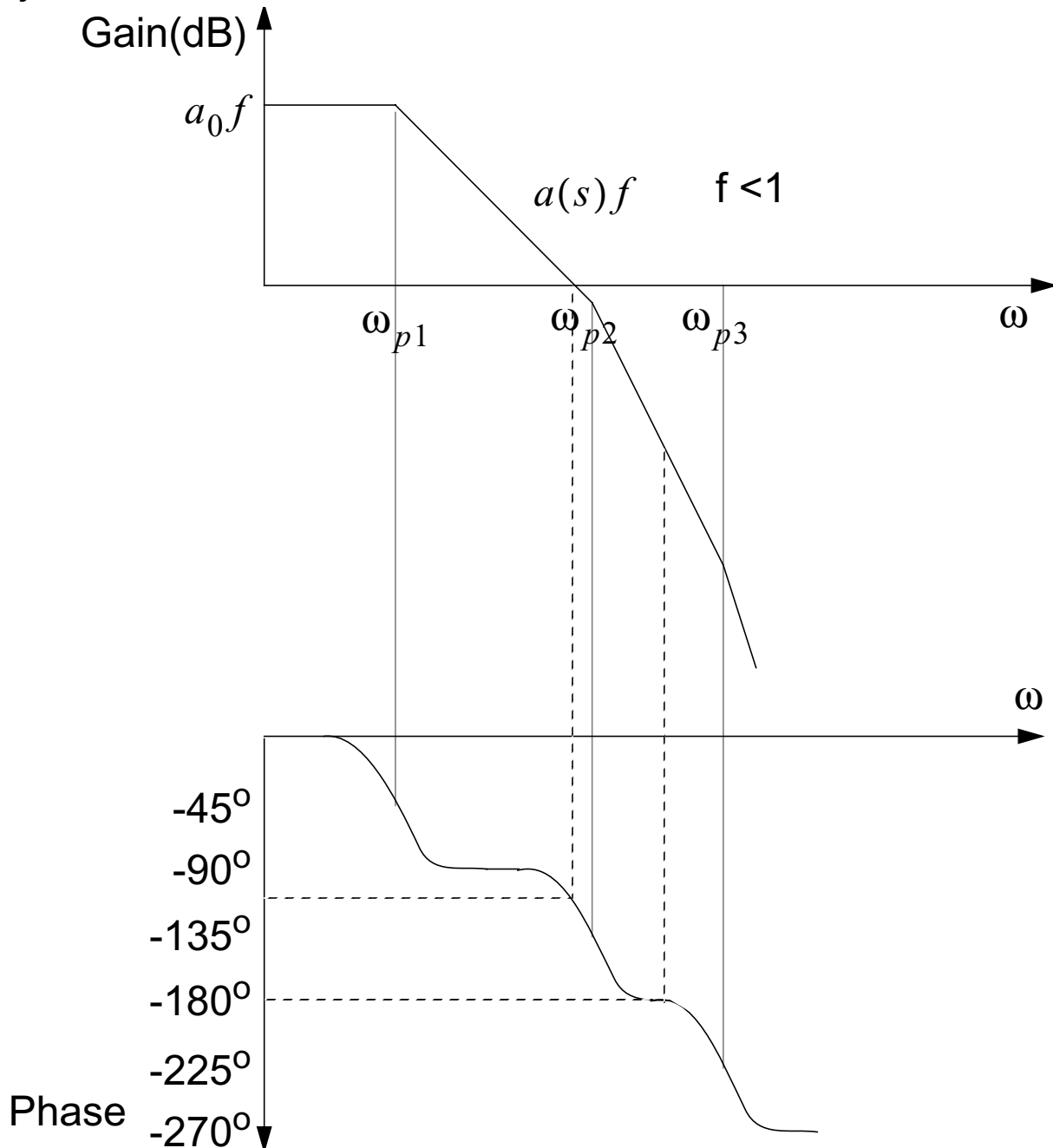
\Rightarrow system is unstable

Feedback factor and stability (contd.)

If the feedback factor is reduced the Bode plot of the loop gain $|a(j\omega)f|$ is shifted downwards i.e. $a(j\omega)f$ is attenuated

If we shift the loop gain far enough downwards (i.e. reduce the feedback factor f sufficiently) then we can reach a situation whereby the loop gain $|a(j\omega)f|$ is less than 1 (0dB) when phase is 180° .

=> system is stable



Conclusions:

Feedback factor = 1 is worst case for stability

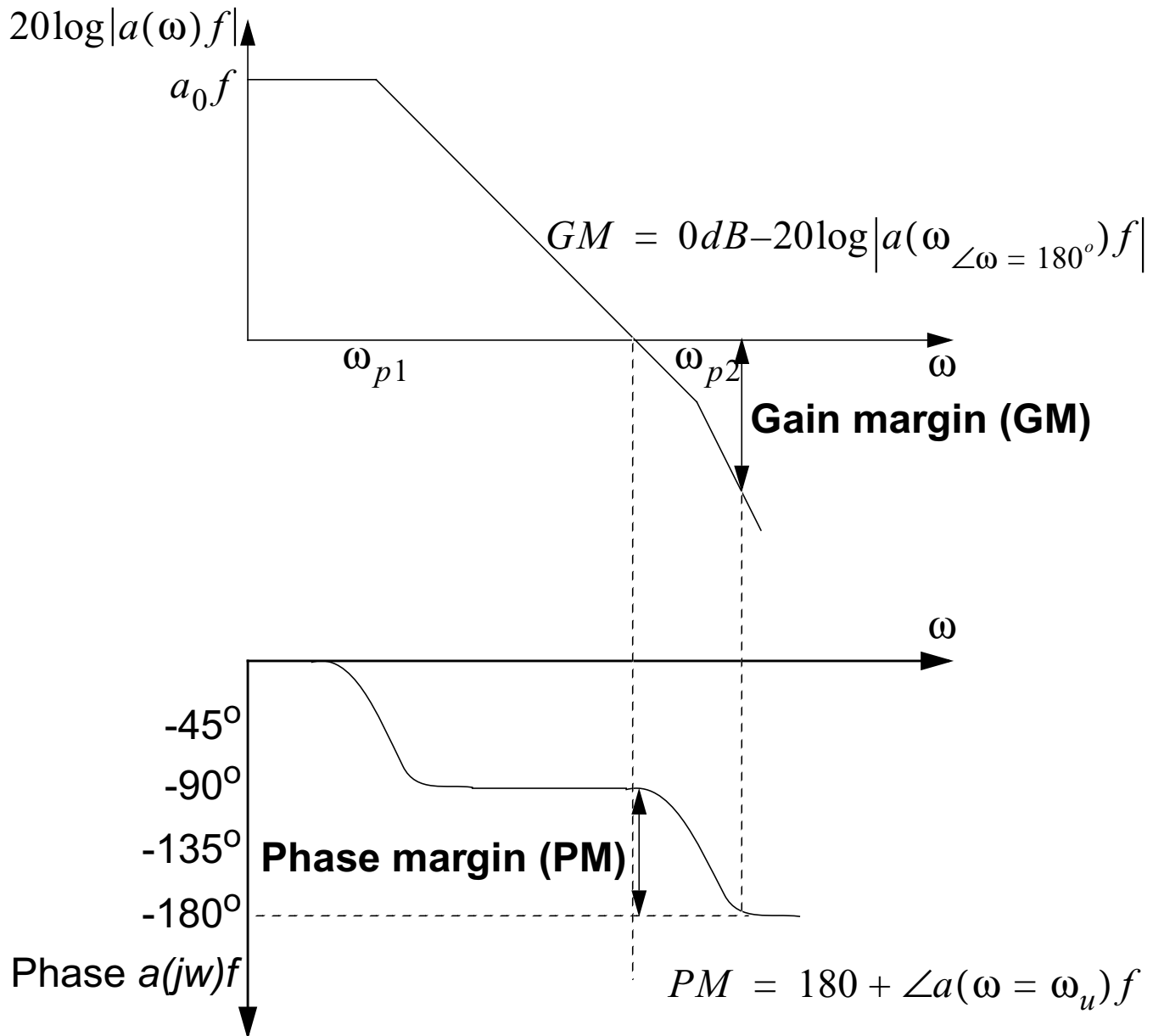
Reduce feedback factor f => easier to achieve stability

However reducing $|a(j\omega)f|$ increases gain error.

8.2.4 Nyquist Stability Criterion

Nyquist criterion for stability of negative feedback systems

When the phase shift of the loop gain $a(j\omega)f$ reaches 180° , then the amplitude of $a(j\omega)f$ must be less than 1.



Two figures of merit are used: phase margin and gain margin

Phase margin:

Difference between the phase shift at unity gain frequency and 180°

For stability must be more than 0° , usually design to 60°

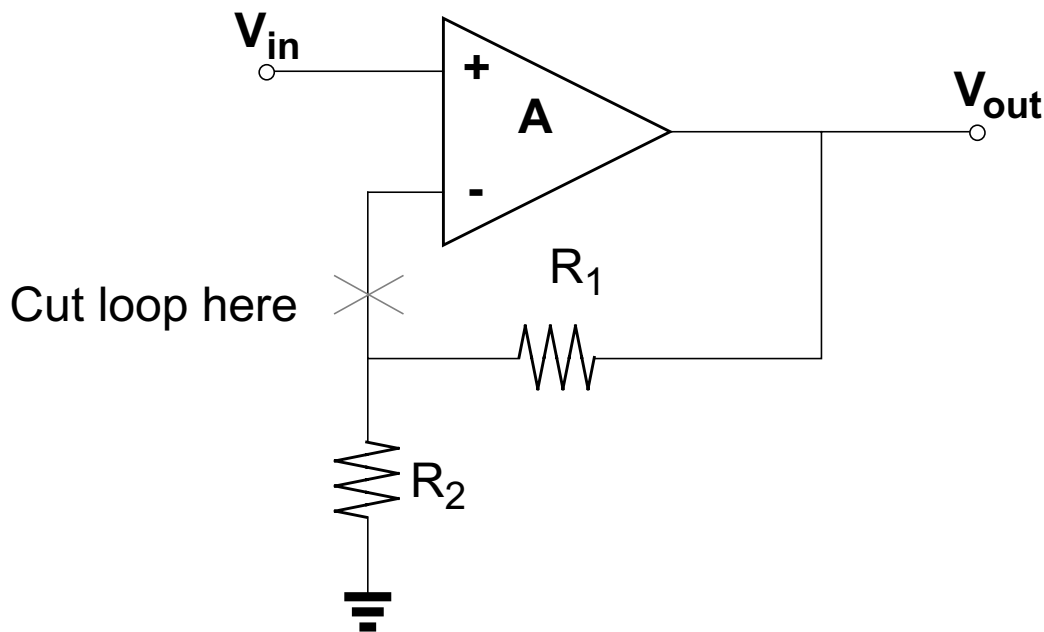
Gain margin

Amount in dB that gain is less than 1 when phase shift reaches -180°

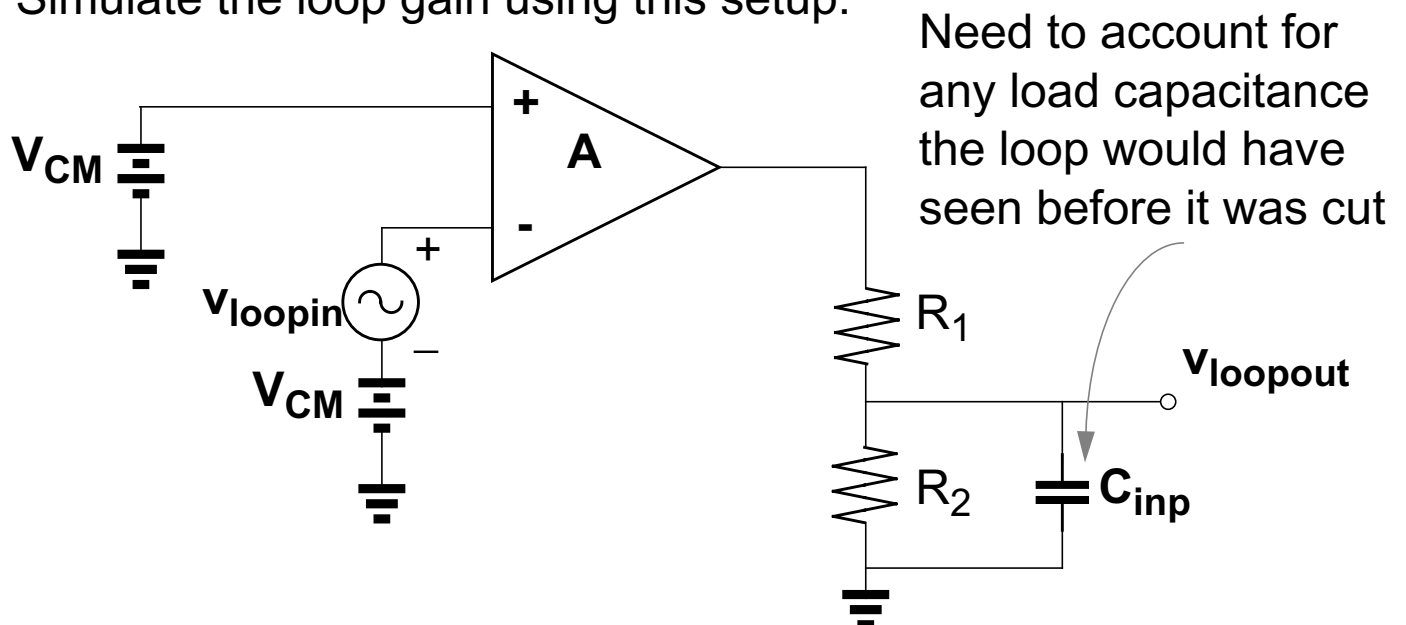
8.2.5 Stability of Opamps in feedback configurations

To determine the stability (e.g. phase margin) of a circuit with feedback plot the loop-gain and phase (by hand or simulation)
This involves 'cutting open' the loop at a convenient point, applying a small-signal test input and measuring the small-signal response at the other side

Noninverting amplifier



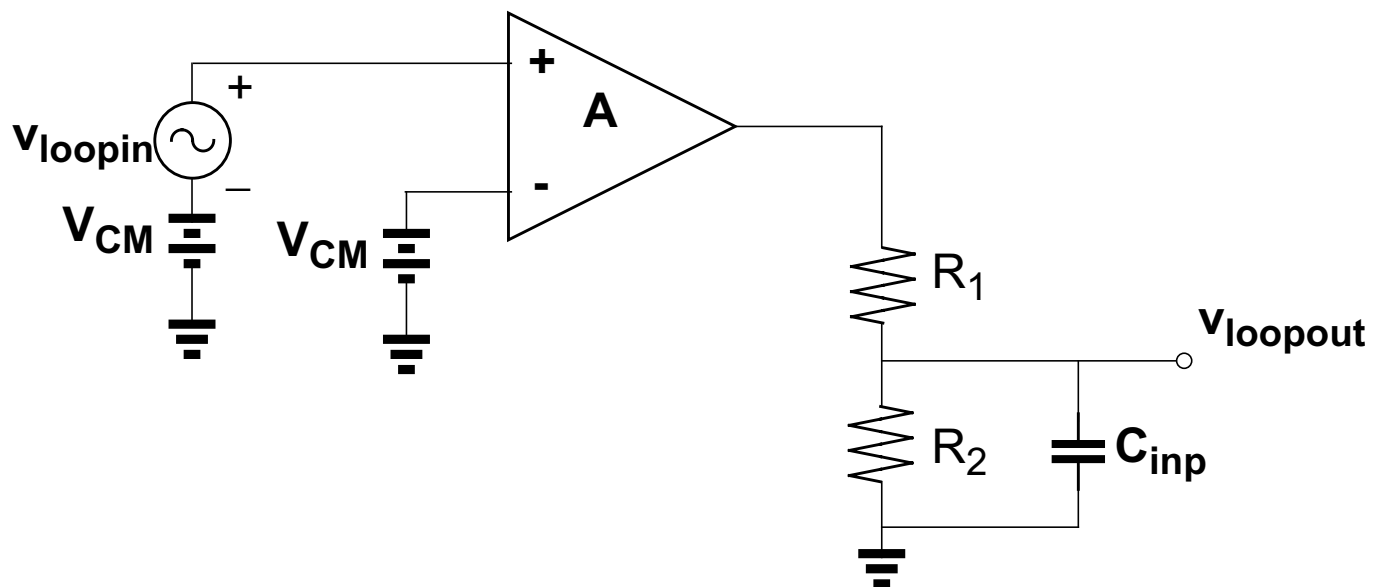
Simulate the loop gain using this setup:



When the gain has dropped to 1 (0dB) the phase shift should not have reached -180° .

Note that the phase at dc is -180° due to the negative feedback, we are interested in the phase shift beyond this.

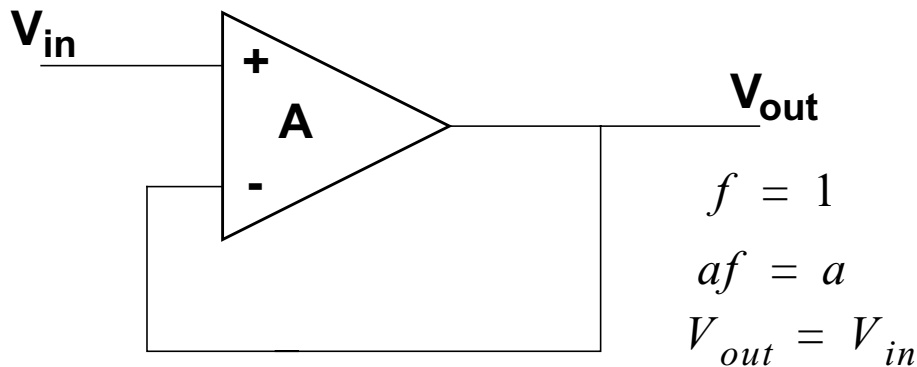
Equivalently we could use the following setup



Note that in this case the phase at dc is 0° , again we are interested in the phase shift beyond this.

8.2.6 Stability of unity-gain configurations.

We have seen that the worst case for stability is when $f=1$ e.g. for a voltage follower



Often design for this worst case i.e. design opamp such that it would be stable for $f=1$, or amplifier gain $A = \text{loop gain}$.

8.2.7 Stability of systems with 1 dominant pole

Each pole contributes a total phase shift of -90°

The phase shift due to pole p_x at frequency ω_{px} is given by

$$\text{PhaseShift} = -\text{atan}\left(\frac{\omega}{\omega_{px}}\right)$$

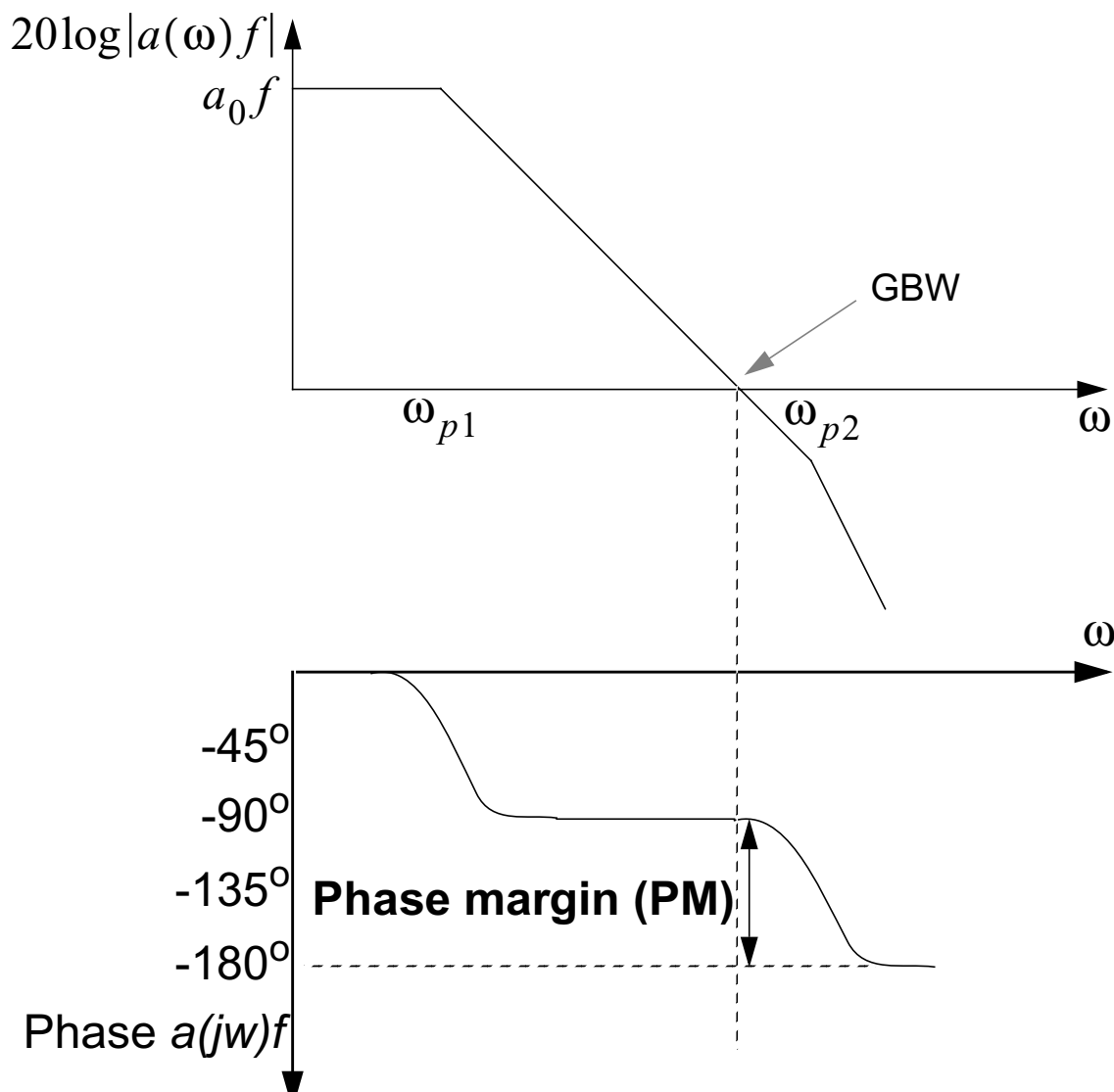
Take a system with widely-spaced poles.

The first (lowest) pole is called the dominant pole.

If the dominant pole frequency is \ll than the GBW it will have contributed -90° phase shift at the unity gain frequency.

The position of the second pole will determine the phase margin.

For a phase margin of at least 45° the second pole needs to be above the GBW



Note: Term GBW is still used even if ω_{p2} is below the unity gain frequency.

Problem - Stability and feedback factor

An amplifier has the following 3 pole transfer function

$$A(s) = \frac{A_o}{\left(1 - \frac{s}{\omega_{p1}}\right)\left(1 - \frac{s}{\omega_{p2}}\right)\left(1 - \frac{s}{\omega_{p3}}\right)}$$

$$A_o = 10^4 \text{ (80dB)}$$

$$\omega_{p1} = 1 \text{ Mrad/s}$$

$$\omega_{p2} = 100 \text{ Mrad/s}$$

$$\omega_{p3} = 1 \text{ Grad/s}$$

- (i) Draw the Bode diagram for the gain
- (ii) If this amplifier is used in a unity gain feedback configuration, what is the phase margin?
- (iii) If the feedback factor is reduced to 0.1 what is the phase margin?

9 Frequency compensation

Opamps circuits contain many poles, typically one per node, or at least one per stage.

If an opamp is used in a closed-loop negative feedback configuration then problems with stability arise if open-loop gain does not drop to unity (0dB) well before phase shift reaches -180° .

How to guarantee stability:

1. Minimize phase shift.

=> minimize number of poles => minimize number of gain stages

Disadvantage: low gain

2. Make the gain drop to unity at a lower frequency => reduce the frequency of the first pole

Disadvantage: bandwidth reduced

In practice try to minimize the number of poles (while still achieving sufficient gain). If the resultant circuit has stability problems we must compensate for stability -> frequency compensation

9.1 Some options for frequency compensation

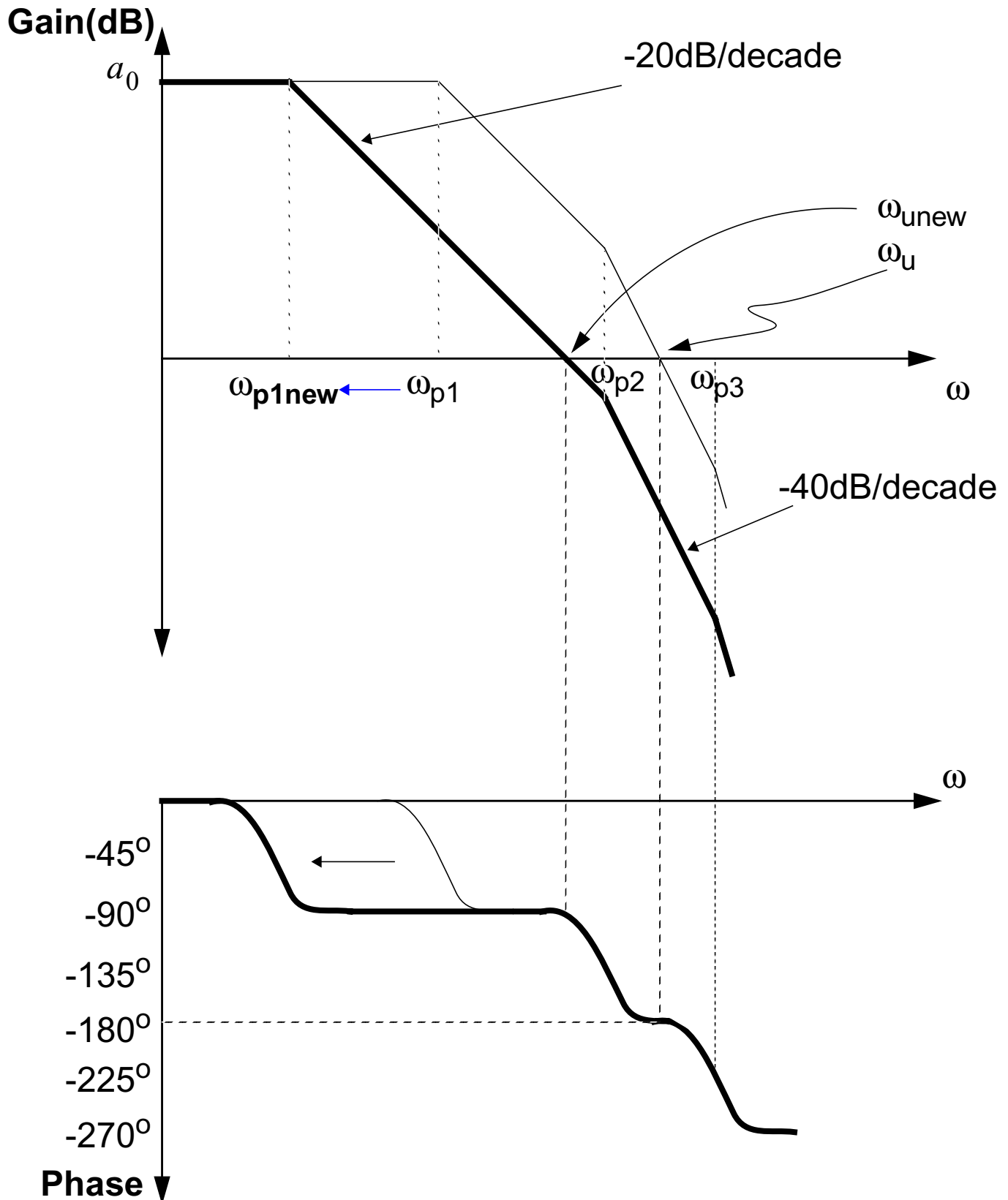
Method 1. Reduce the frequency of the first pole so that it is dominant, i.e. at a low enough frequency that the other poles only start contributing phase shift after gain < 1 .

Method 2. Pole-splitting: Technique by which first pole is reduced in frequency and second pole is increased.

Note: Could also reduce the feedback factor but this is not always an option.

9.1.1 Frequency compensation (Method 1) illustrated

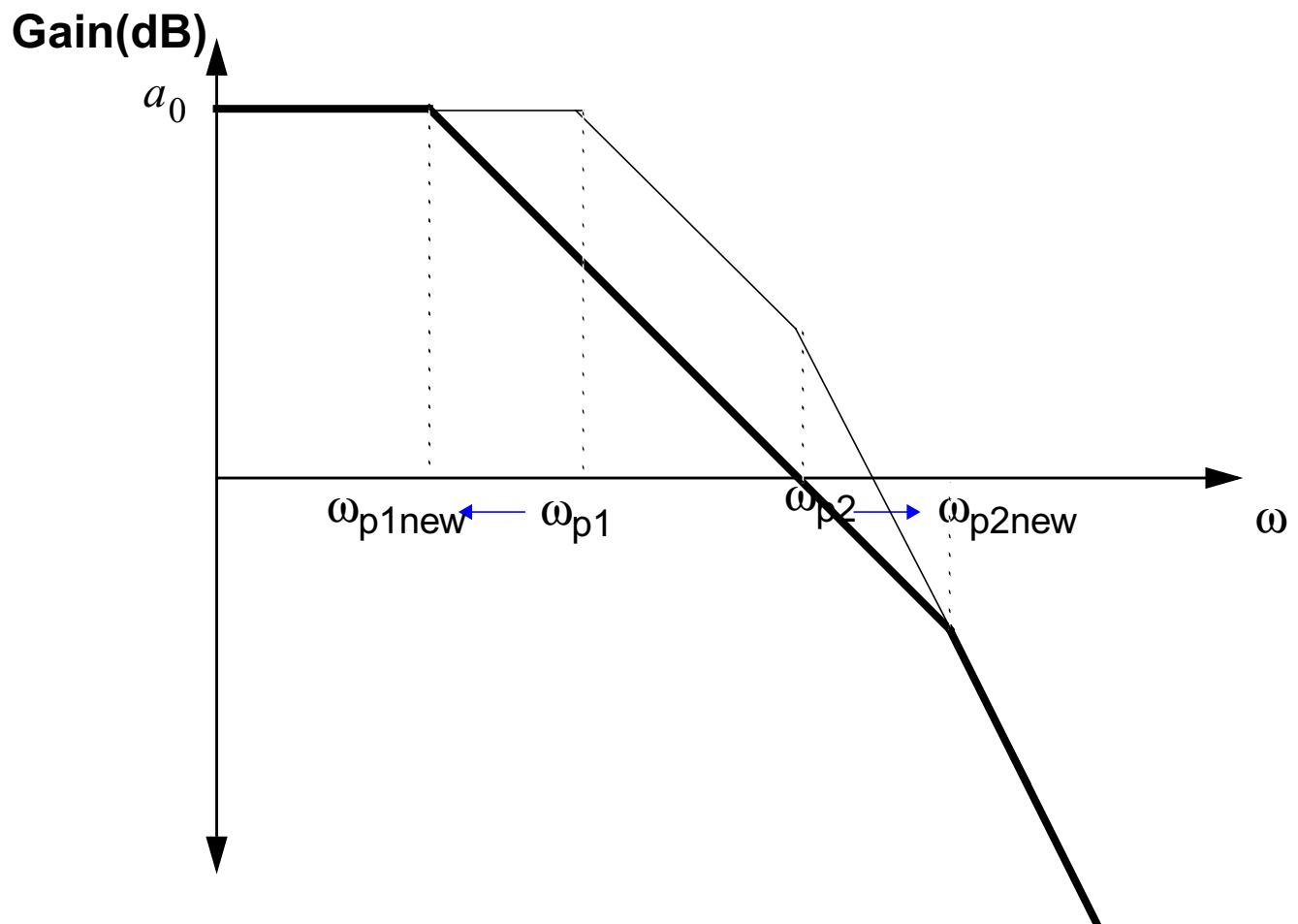
Move ω_{p1} down to $\omega_{p1\text{new}}$ such that gain roll-off is first-order through 0dB



Note: if ω_{p2} (frequency of second pole) = ω_u (unity gain frequency) and $\omega_{p3} \gg \omega_u$ then the total phase shift at $\omega_u = 135^\circ$ (90° from ω_{p1} and 45° from ω_{p2}) then phase margin = 45°

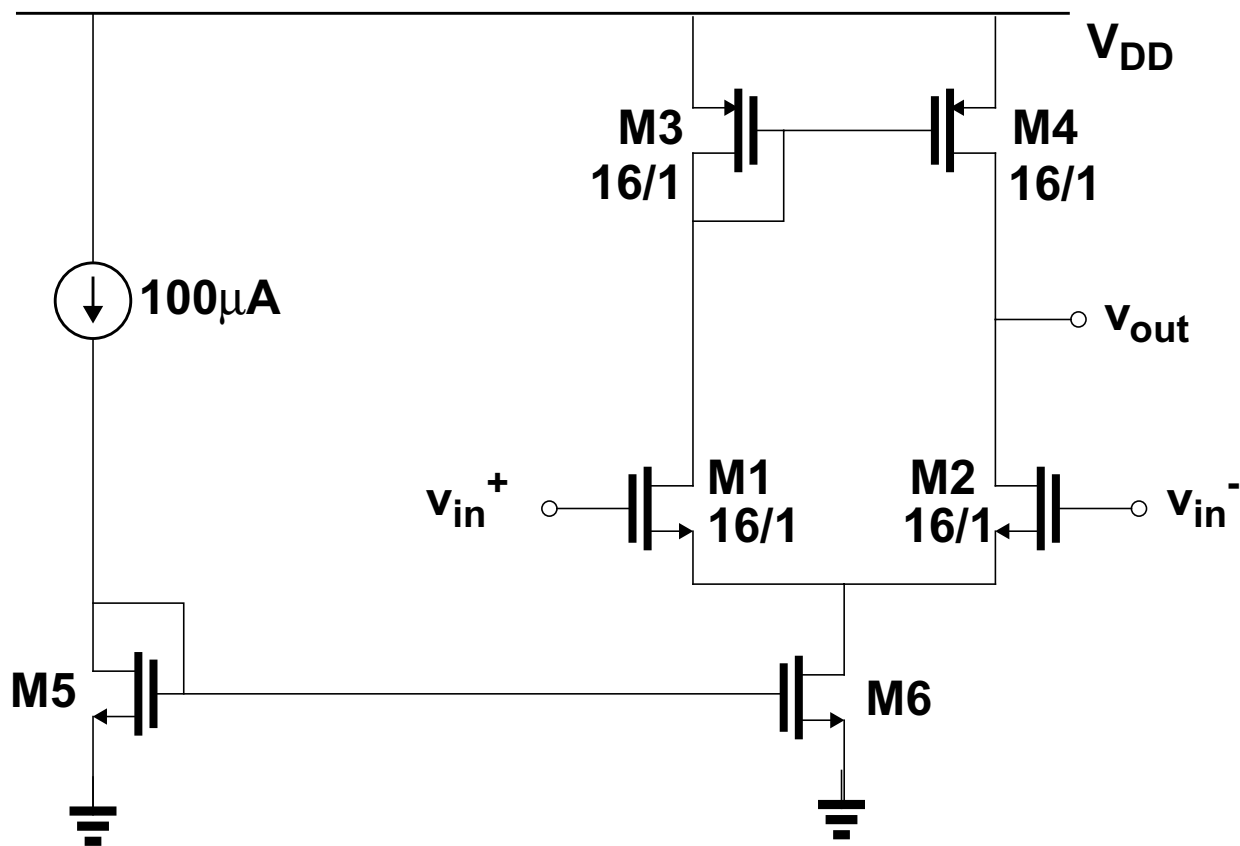
9.1.2 Frequency compensation (Method 2) illustrated

Moving ω_{p1} down to $\omega_{p1\text{new}}$ also moves ω_{p2} up to $\omega_{p2\text{new}}$, enhancing stability.



9.2 Dominant pole compensation

Example: Compensation of a simple opamp circuit

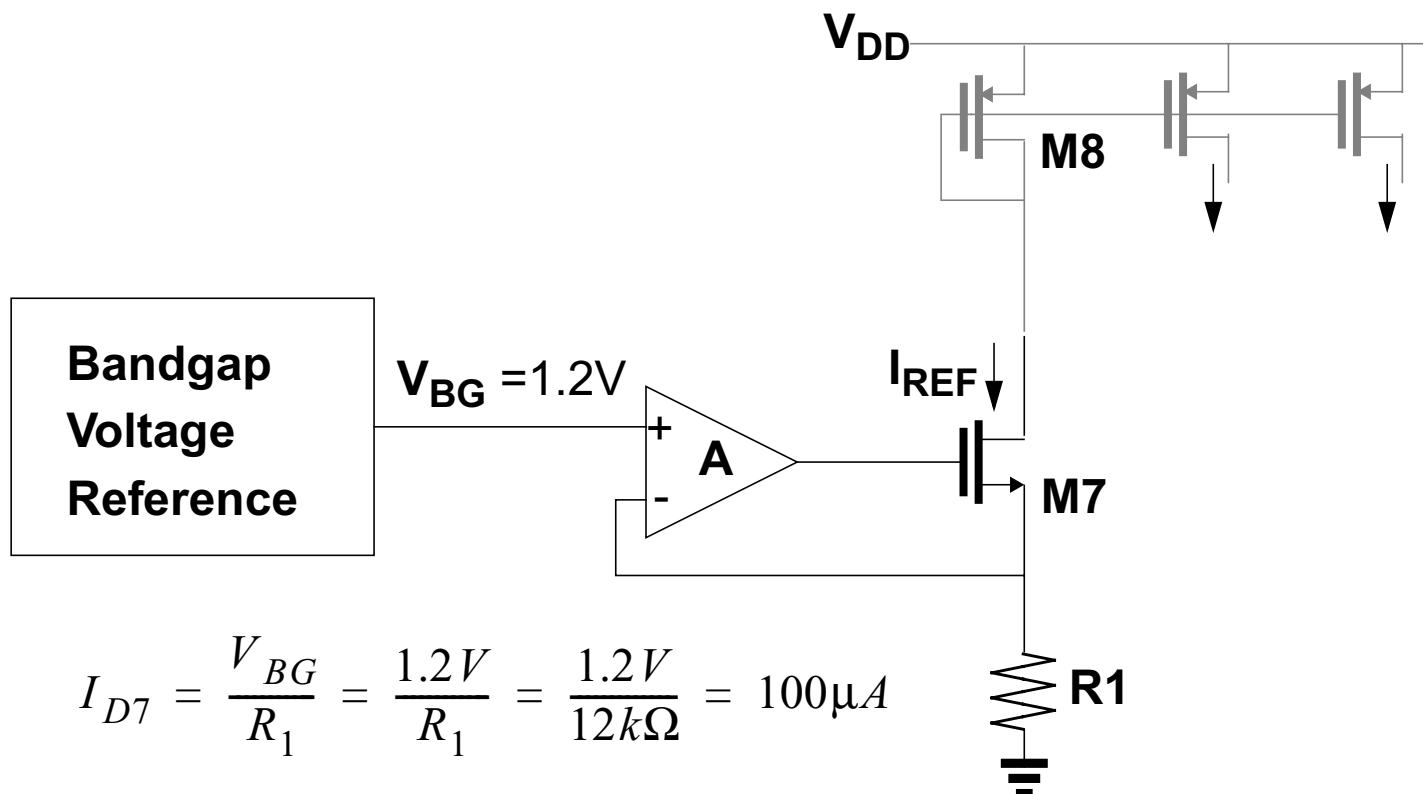


The opamp shown is to be used in the current reference circuit of P. 156. Each input transistor is to have a drain current of $100\mu A$. Body effect may be ignored.

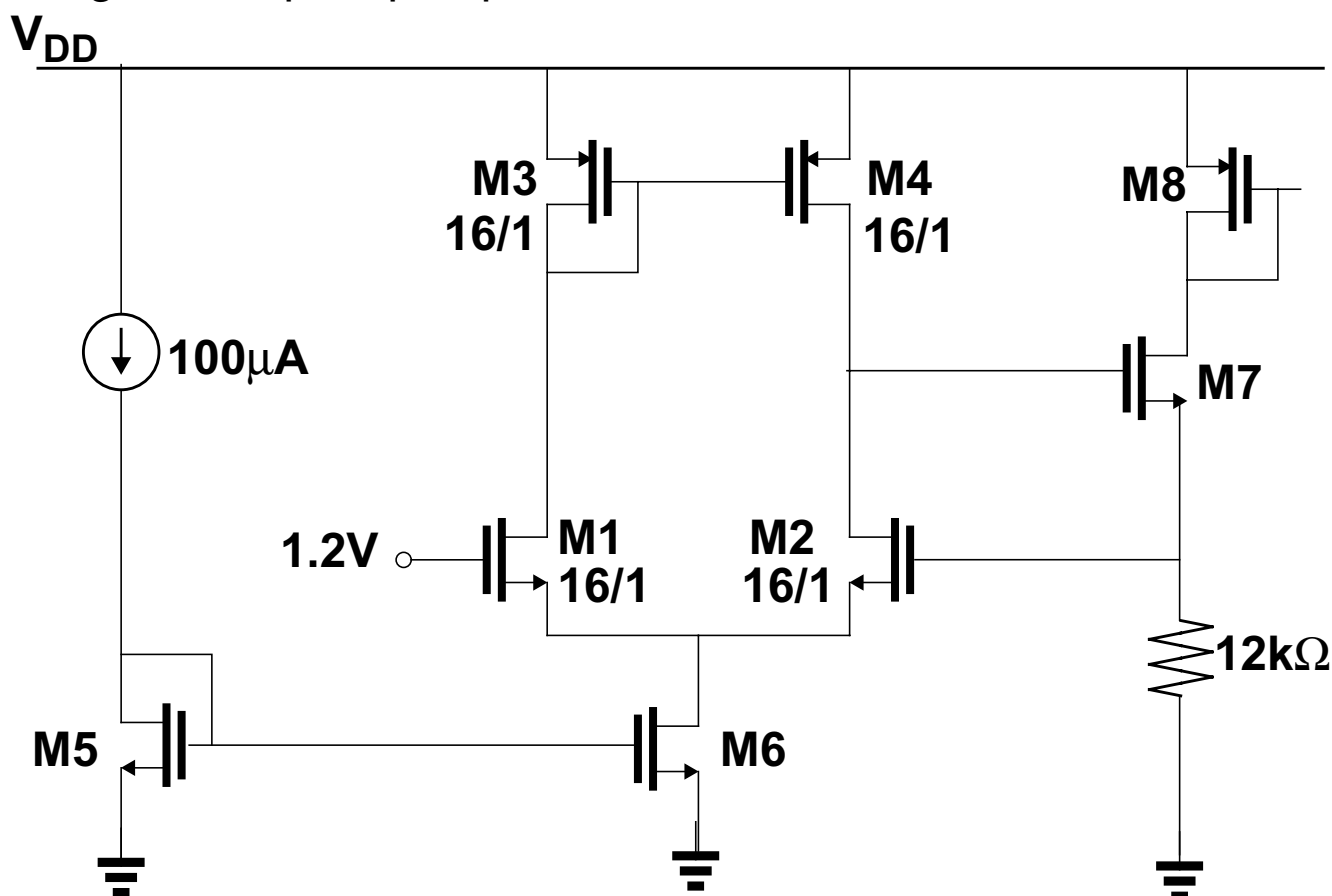
Use $V_{DD}=3.3V$, $V_{tn}=|V_{tp}|=0.7V$, $K_n'=200\mu A/V^2$, $K_p'=50\mu A/V^2$
 $\lambda_n=\lambda_p=0.04/L V^{-1}$

- Draw the full circuit
- What W/L is required for the mirror transistors M5, M6?
- What W/L is required for the source follower?
- What is the open-loop gain of the circuit?
- What is the effect on the circuit if the reference resistor is reduced from $12k\Omega$ to $3k\Omega$?
- Assess the stability of the circuit if the total capacitance at the output node of the opamp is $0.1pF$, at the gate of M3 $0.2pF$, and the total capacitance at the node above the external resistor is $1pF$

(i) Draw the full circuit
Recall the application from P. 156:



Using the simple opamp shown, the full circuit is:



(ii) What W/L is required for the mirror transistors M5, M6?

$$M1: V_{GS1} - V_t = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V \cdot \frac{16}{1}}} = 250mV$$

$$V_{GS1} = 250mV + V_t = 250mV + 700mV = 950mV$$

So the drain of M6 is at $1.2V - 950mV = 250mV$

=> $V_{GS} - V_t$ of M6 is max 250mV

M6 is to carry twice the current of M1, so will need 2XW/L of M1

=> W/L min for M6 > 32/1 (use higher L for good current mirror)

W/L of M5 must be half W/L of M6 for 1:2 mirroring ratio

(iii) What W/L is required for the source follower?

The first requirement is that M4 is in saturation.

If the amplifier is to be dimensioned optimally to give exactly 1.2V at the gate of M2, then it needs to be symmetrical

=> voltage at the drain of M3 should be equal to voltage at drain of M4.

$$\text{M3: } |V_{GS3}| - |V_t| = \sqrt{\frac{2 \cdot 100\mu A}{50\mu A/V \cdot \frac{16}{1}}} = 500mV$$

$$|V_{GS3}| = 500mV + |V_t| = 500mV + 700mV = 1.2V$$

$$V_{D3} = V_{DD} - |V_{GS3}| = 3.3V - 1.2V = 2.1V$$

For the drain of M4 to be at 2.1V then V_{GS7} needs to be 0.9V

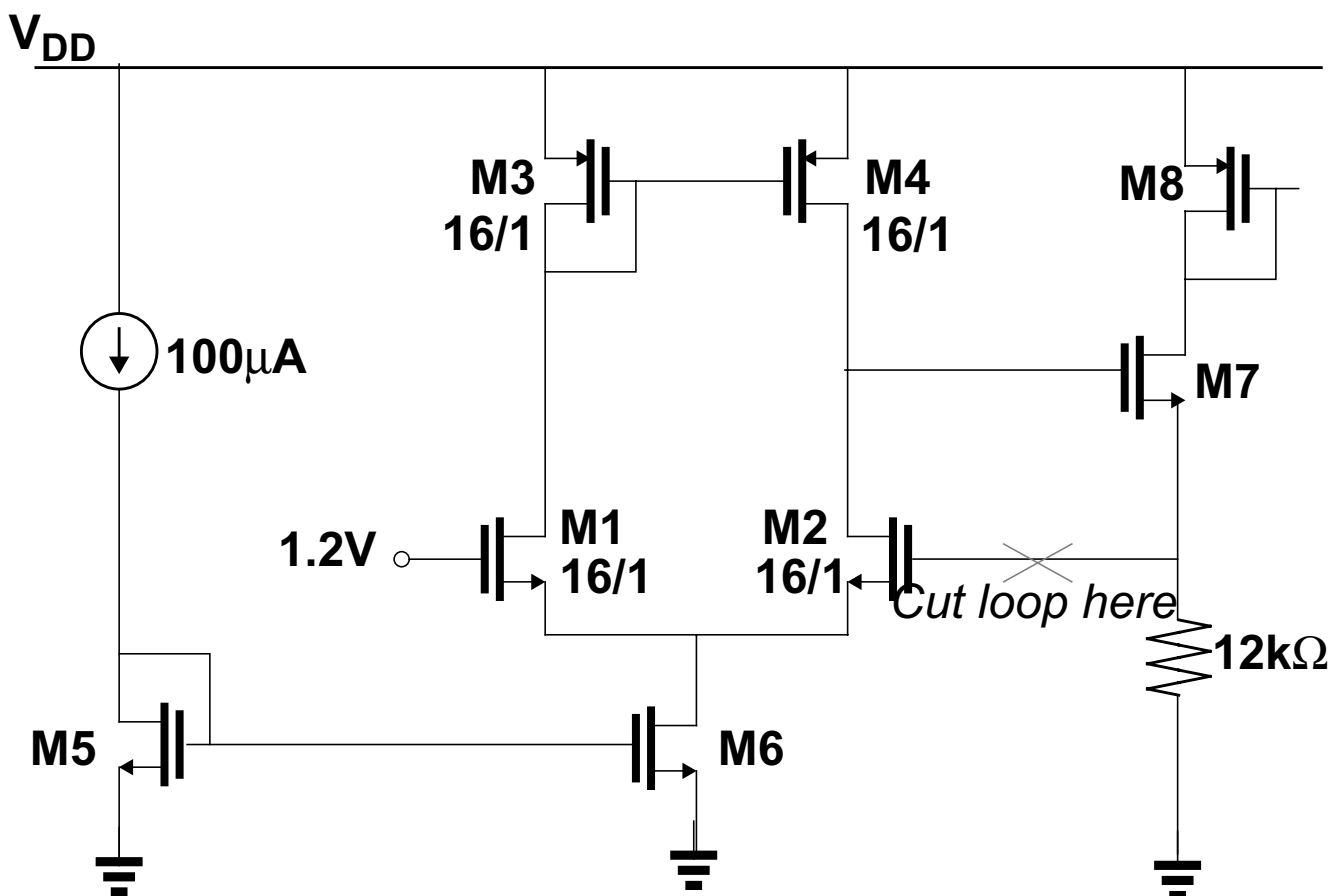
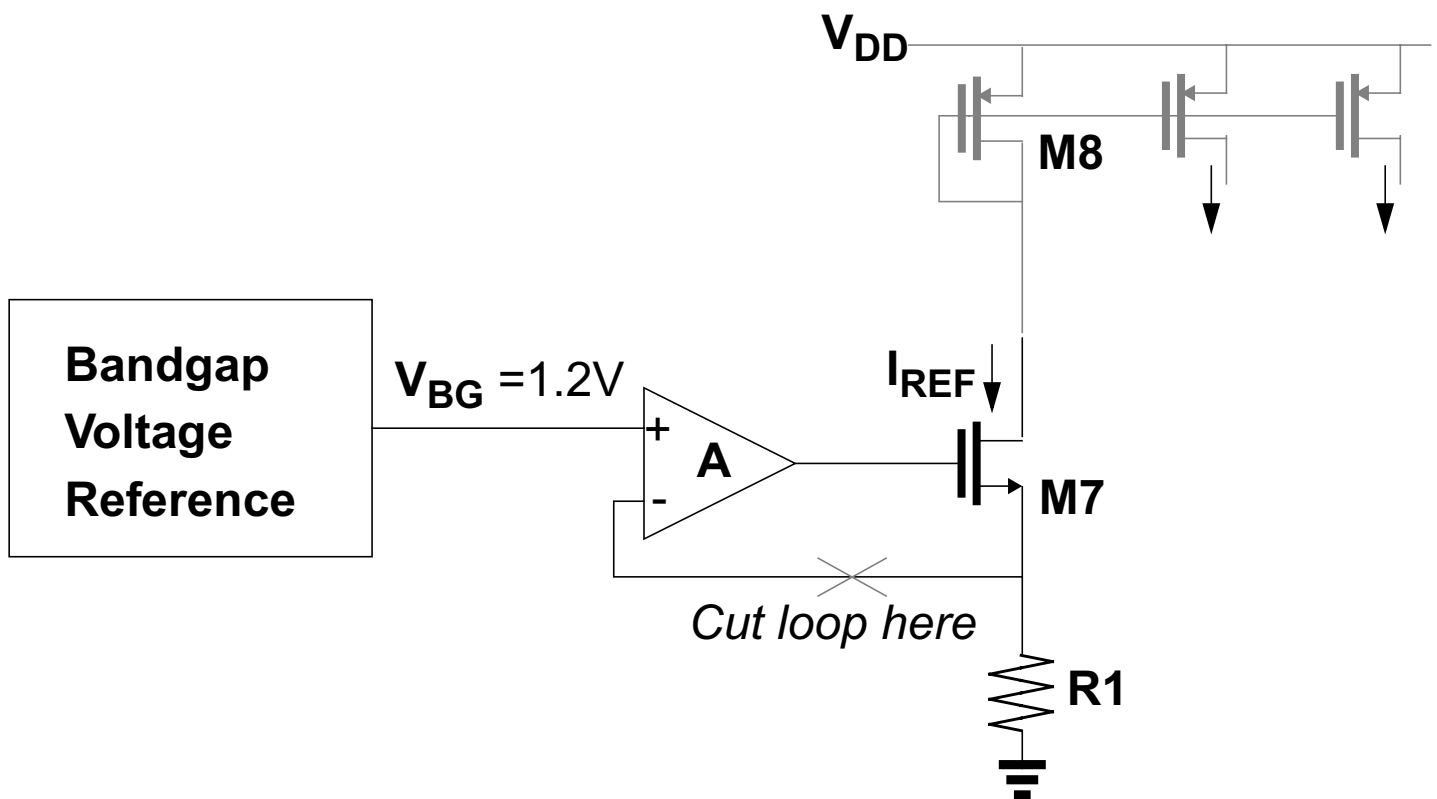
=> $V_{GS} - V_t$ of M7 = 200mV

$$\frac{W}{L} = \frac{2I_{D7}}{K'_n(V_{GS7} - V_t)^2} = \frac{2 \cdot 100\mu A}{200\mu A/V \cdot 0.2V^2} = \frac{25}{1}$$

N.B. M8 will also need to be dimensioned such that M7 is in saturation.

(iv) What is the open-loop gain of the circuit?

To measure the loop gain, imagine cutting open the loop at some point, injecting a signal and measuring the gain of that signal around the loop.



Note on 'cutting the loop'

How is this done in a circuit simulator?

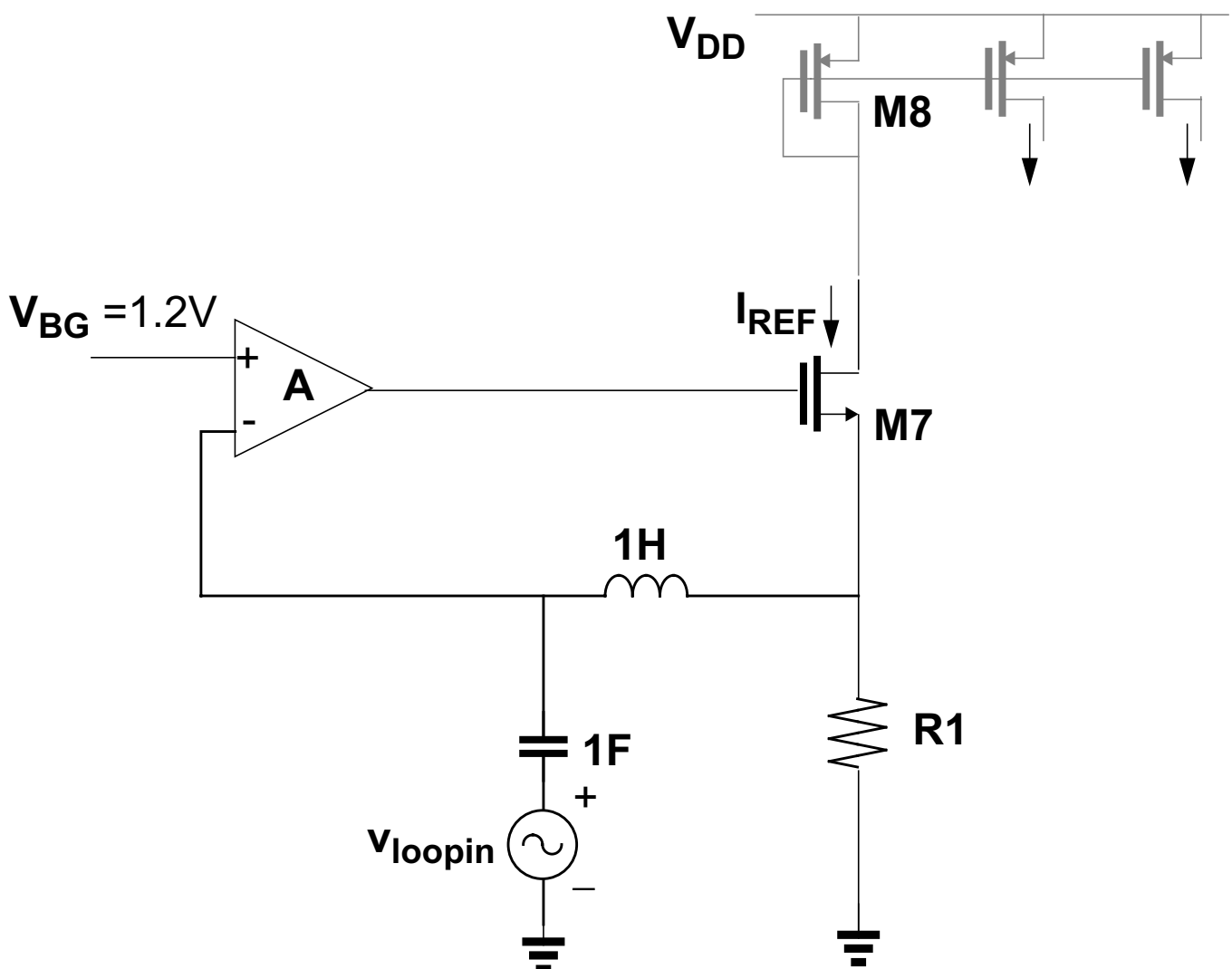
What is required is first a DC simulation so that the DC solution for the circuit (i.e. DC node voltages, branch currents, operating points etc.) is solved by the simulator.

Then an AC (small-signal) frequency-sweep simulation is performed, where the circuit is linearised around the DC operating point.

To cut the loop use frequency-dependent elements e.g.

- (i) A large inductor with zero impedance at DC and very large impedance at high frequencies. This can be used to cut the loop.
- (ii) A large capacitor with infinite impedance at DC and very low impedance at higher frequencies. This can be used to inject the signal.

Alternatively Spectre has analysis-dependent switches, or (preferably) the stb analysis



Loop Gain = Gain of diff. amp X gain of source follower

$$A_{diffamp} = -\frac{g_{m2}}{g_{ds2} + g_{ds4}}$$

$$g_{m2} = \frac{2I_{D2}}{V_{GS2} - V_t} = \frac{2 \times 100\mu A}{0.25} = 0.8mA/V$$

$$g_{ds2} = \lambda I_{D2} = \frac{0.04}{1} \times 100\mu A = 4\mu A/V$$

$$A_{diffamp} = -\frac{g_{m2}}{g_{ds2} + g_{ds4}} = -\frac{0.8mA/V}{4\mu A/V + 4\mu A/V} = -100 = 40dB$$

$$A_{sf} = \frac{g_{m7}R_L}{1 + g_{m7}R_L} = \frac{g_{m7}}{g_{m7} + \frac{1}{R_L}}$$

$$g_{m7} = \frac{2I_{D7}}{V_{GS7} - V_t} = \frac{2 \times 100\mu A}{0.2} = 1mA/V$$

$$A_{sf} = \frac{g_{m7}}{g_{m7} + \frac{1}{R_L}} = \frac{1mA/V}{1mA/V + \frac{1}{12k\Omega}} = 0.92 = -0.7dB$$

$$A_{loop} = 40dB - 0.7dB = 39.3dB$$

(v) What is the effect on the circuit if the reference resistor is reduced from $12\text{k}\Omega$ to $3\text{k}\Omega$?

As long as the opamp still has a high gain i.e. if M4 is still in saturation (it is), then there will still be about 1.2V at the gate of M2, so still 1.2V across the resistor.

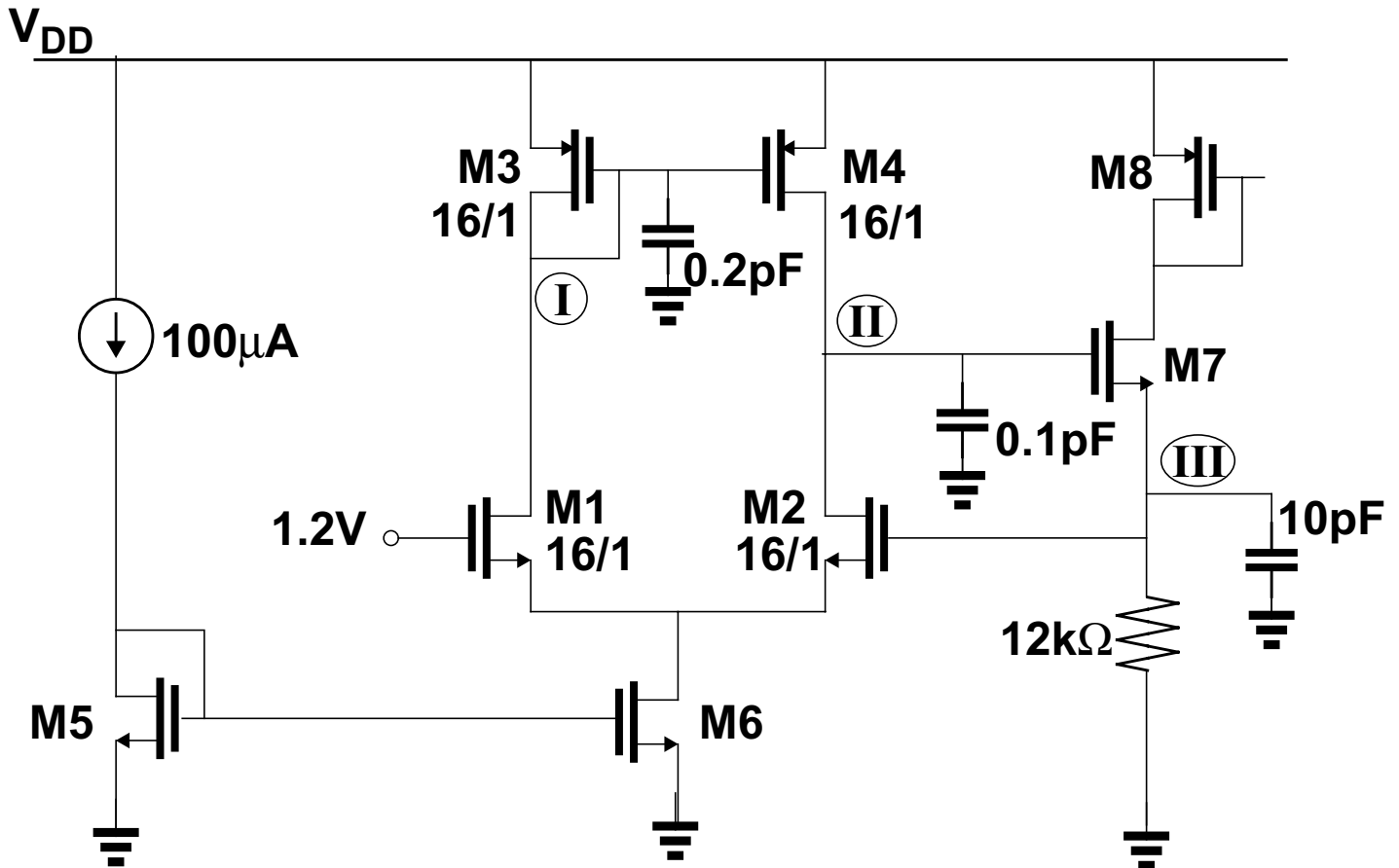
However reducing the resistor from $12\text{k}\Omega$ to $3\text{k}\Omega$ will cause the current through the resistor to increase from $100\mu\text{A}$ to $400\mu\text{A}$. This will increase $V_{GS7} : V_{GS} - V_t$ of M7 will double from 200mV to 400mV, causing the voltage at the gate of M7, and so the drains of M2, M4 to increase by 200mV. This will tend to pull more current out of M2. To compensate this the voltage at the gate of M2 reduces slightly below 1.2V.

This will introduce an input-referred offset in the opamp of approx. 200mV divided by the Loop Gain - about 2mV.

The voltage at the gate of M2 (and across the resistor) will then be 1.2V-2mV, introducing an error of about 0.17% in the output current.

If this error is unacceptable increase W/L M7 by 4 to restore the voltage at the drains of M2, M4 to 2.1V.

(vi) Assess the stability of the circuit if the total capacitance at the output node of the opamp is 0.1pF, at the gate of M3 0.2pF, and the total capacitance at the node above the external resistor is 10pF



Identify the nodes in the circuit which could have poles associated with them.

There are three: I, II and III. The other nodes are either at ac ground or are driven by the input signal, or are outside the signal path

What are the poles associated with each of these nodes?

Recall:

Pole associated with a node:

$$\omega_p = \frac{1}{\text{resistance at node} \times \text{capacitance at node}}$$

$$\omega_p = \frac{\text{conductance at node}}{\text{capacitance at node}}$$

$$\omega_{pn} = -\frac{1}{R_n C_n} = -\frac{g_n}{C_n} \quad \text{where } n \text{ represents the } n\text{th pole}$$

Poles

$$\text{Node I} \quad |\omega_{pI}| \approx -\frac{g_{m3}}{C_I} = \frac{0.4mA/V}{0.2pF} = 2Grad/s$$

$$\text{Node II} \quad |\omega_{pII}| = -\frac{g_{ds2} + g_{ds4}}{C_{II}} = -\frac{8\mu A/V}{0.1pF} = 80Mrad/s$$

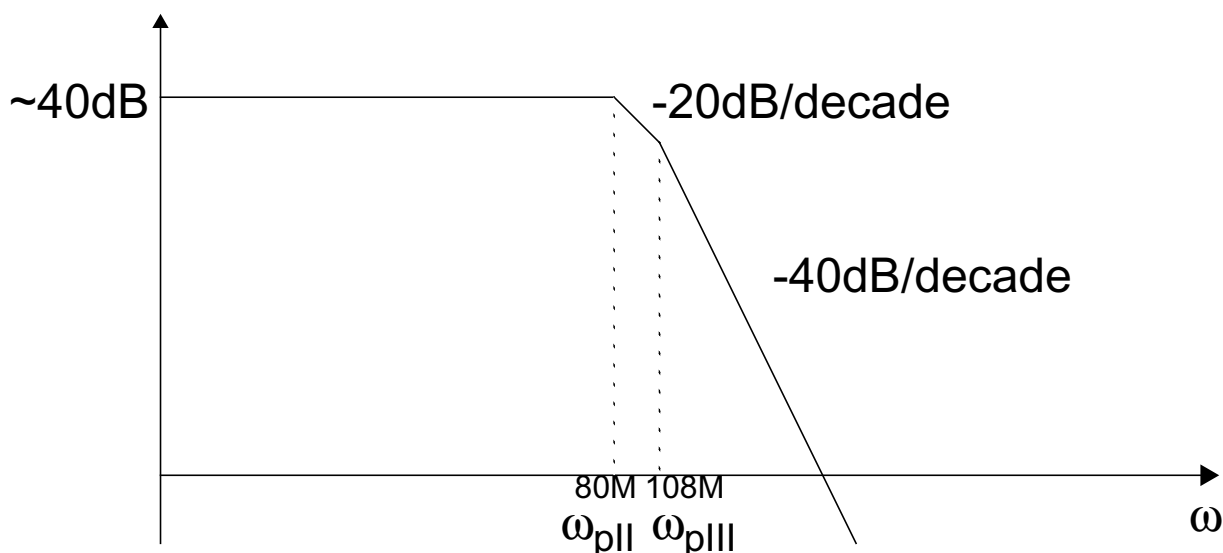
$$\text{Node III} \quad |\omega_{pIII}| = -\frac{g_{m7} + \frac{1}{R_{ext}}}{C_{III}} \approx -\frac{1mA/V + \frac{1}{12k\Omega}}{10pF} = 108Mrad/s$$

Zeroes

There are also zeroes due to feedthrough of signal through C_{gd4}, C_{gs7} , but as these are related to g_m of the transistor assume they are non-dominant

Conclusion:

Two relatively low-freq. (i.e dominant) poles in the same frequency range => unstable => we need to compensate



Compensation:

The simplest way to compensate is to make one pole dominant (i.e. reduce its frequency) such that the gain falls to unity (0dB) at a frequency at or below the frequency of the second pole (or in other words below the Gain bandwidth of the amplifier).

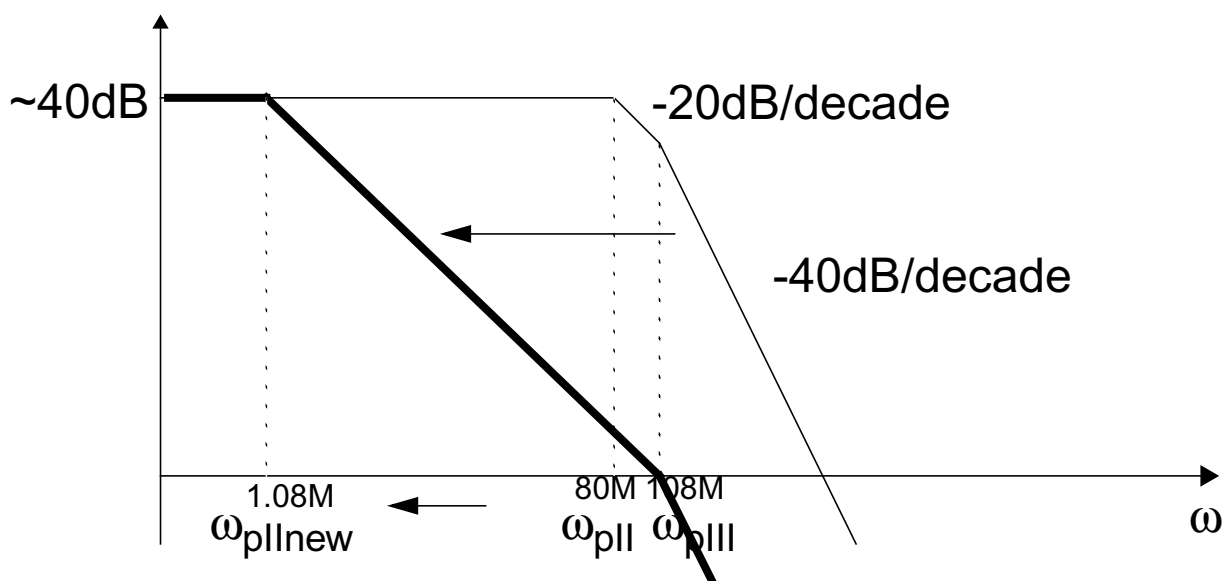
This can be done for ω_{pII} by increasing the capacitance at node II. This will guarantee a phase margin of at least 45° .

$$\omega_{pIInew} \times A_{loop} < \omega_{pIII}$$

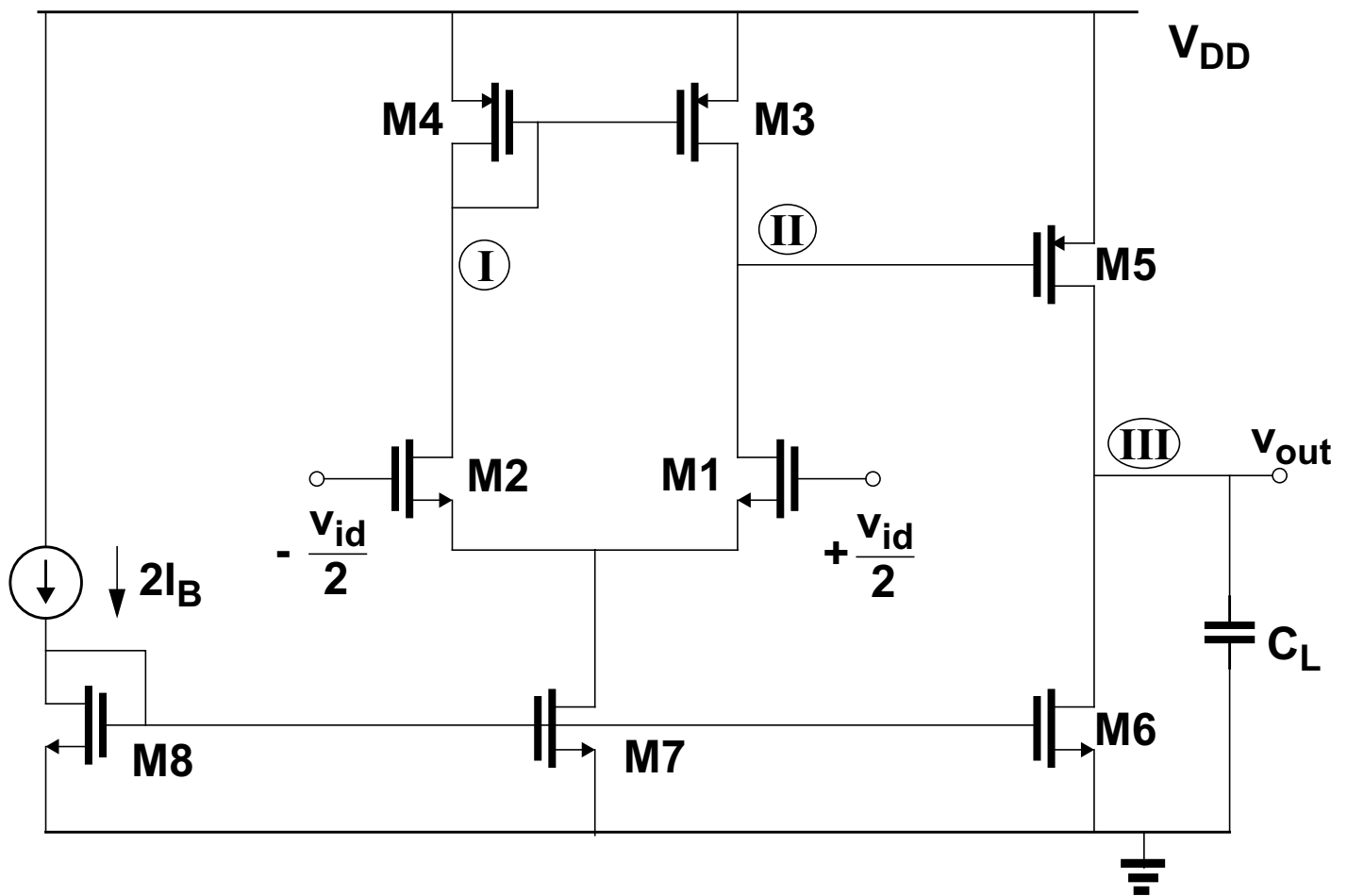
$$\omega_{pIInew} < \frac{\omega_{pIII}}{A_{loop}} = \frac{108Mrad/s}{40dB} = 1.08Mrad/s$$

$$\frac{g_{ds2} + g_{ds4}}{C_{IInew}} < 1.08Mrad/s$$

$$C_{IInew} > \frac{g_{ds2} + g_{ds4}}{1.08Mrad/s} = 7.4pF$$



9.3 Compensation of two-stage differential amplifier



Recall: dc gain of two-stage differential amplifier

$$Gain = \frac{g_{m1}}{g_{ds1} + g_{ds3}} \cdot \frac{g_{m5}}{g_{ds5} + g_{ds6}}$$

We need to ascertain if this amplifier needs compensation if used in a feedback circuit

Assume a capacitive load C_L

2 approaches:

1. Identify the poles and zeroes by observation
2. More rigorous mathematical approach

Compensation of two-stage differential amplifier (contd.)

Approach 1: Identify the poles and zeroes by observation

Where are the poles and zeroes?

Identify the nodes in the circuit which could have poles associated with them.

There are three: I, II and III. The other nodes are either at ac ground or are driven by the input signal, or are outside the signal path

What are the poles associated with each of these nodes?

Recall:

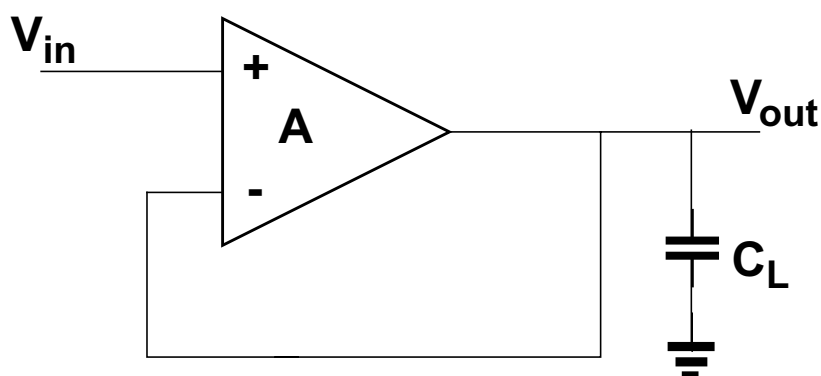
Pole associated with a node:

$$\omega_p = \frac{1}{\text{resistance at node} \times \text{capacitance at node}}$$

$$\omega_{pn} = -\frac{1}{R_n C_n} = -\frac{g_n}{C_n}$$

where n represents the nth pole

Note: In this analysis we are considering the opamp in the worst case stability configuration i.e. as a follower (with unity feedback factor). We also assume C_L includes the loading of the opamp negative input.



Compensation of two-stage differential amplifier (contd.)

Poles, zeroes of uncompensated two-stage differential amplifier.

Poles

$$\text{Node I} \quad |\omega_{pI}| = \frac{g_I}{C_I} \approx -\frac{g_{m4}}{C_I}$$

$$\text{Node II} \quad |\omega_{pII}| = \frac{g_{II}}{C_{II}} = -\frac{g_{ds1} + g_{ds3}}{C_{II}}$$

$$\text{Node III} \quad |\omega_{pIII}| = \frac{g_{III}}{C_{III}} = -\frac{g_{ds5} + g_{ds6}}{C_{III}} \approx -\frac{g_{ds5} + g_{ds6}}{C_L}$$

What about the relative order of magnitude of these poles?

Assume C_L is order of magnitude of internal gate capacitance

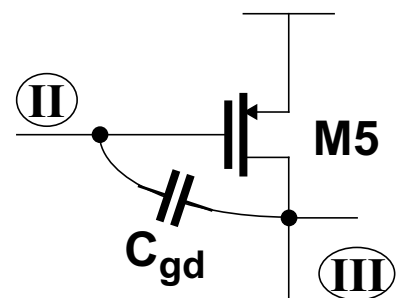
=> ω_{pII} , ω_{pIII} same order of magnitude

Since $g_m \gg g_{ds}$, ω_{pI} is at a much higher frequency than ω_{pII} or ω_{pIII}

=> non-dominant, ignore this pole

Zeroes

Recall: zero due to feedthrough of signal via C_{gd}



$$\omega_z = \frac{g_{m5}}{C_{gd}} \quad g_m \gg g_{ds}, C_{gd} \ll \text{total gate capacitance} \\ \Rightarrow \text{high frequency zero, is probably non-dominant}$$

Conclusion:

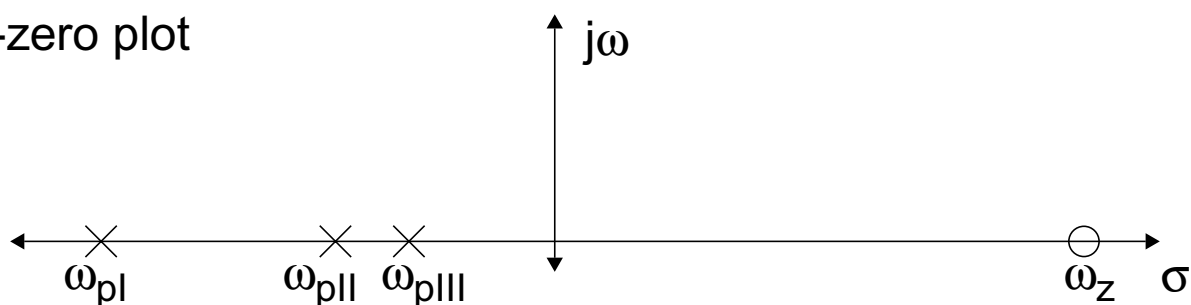
Two relatively low-freq. (i.e dominant) poles in the same frequency range => we need to compensate if using amplifier closed loop.

$$|\omega_{pIII}| = \frac{g_{ds5} + g_{ds6}}{C_L} \quad |\omega_{pII}| = -\frac{g_{ds1} + g_{ds3}}{C_{II}}$$

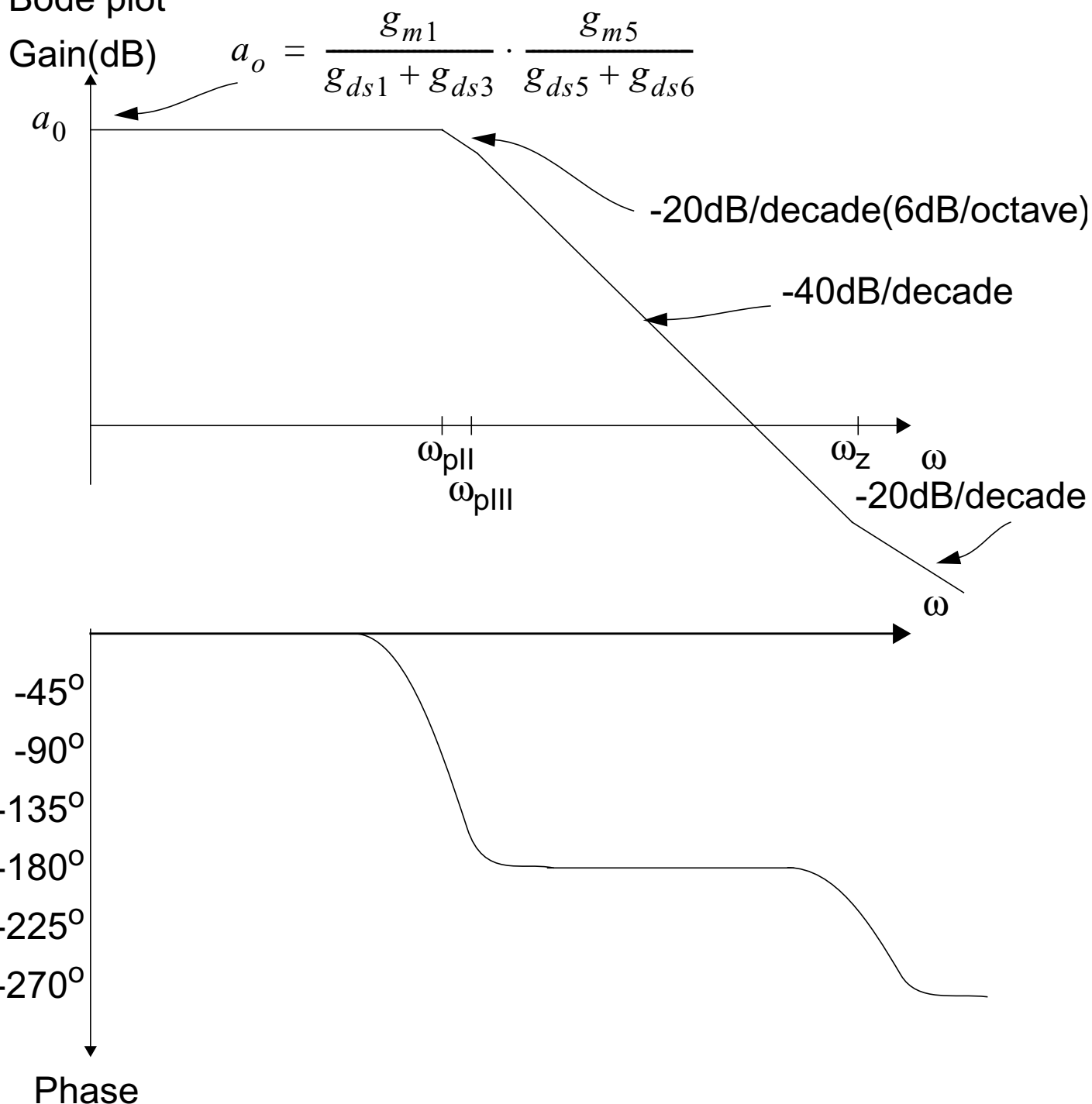
$$\text{where } C_{II} = C_{gs5} + C_{db1} + C_{db3}$$

Compensation of two-stage differential amplifier (contd.)

Pole-zero plot

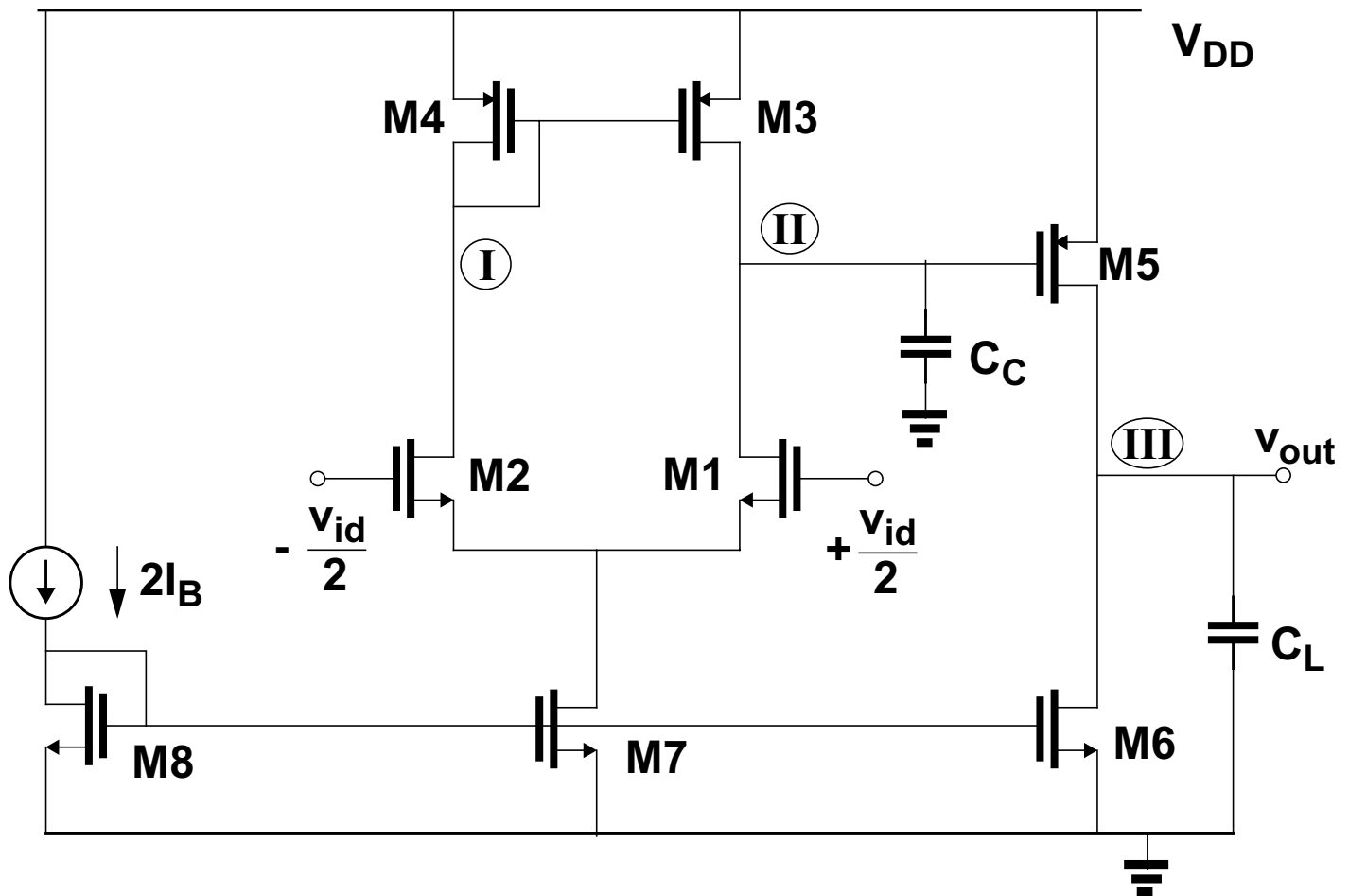


Bode plot



Compensation of two stage differential amplifier (contd.)

9.3.1 2-stage amplifier: dominant pole compensation

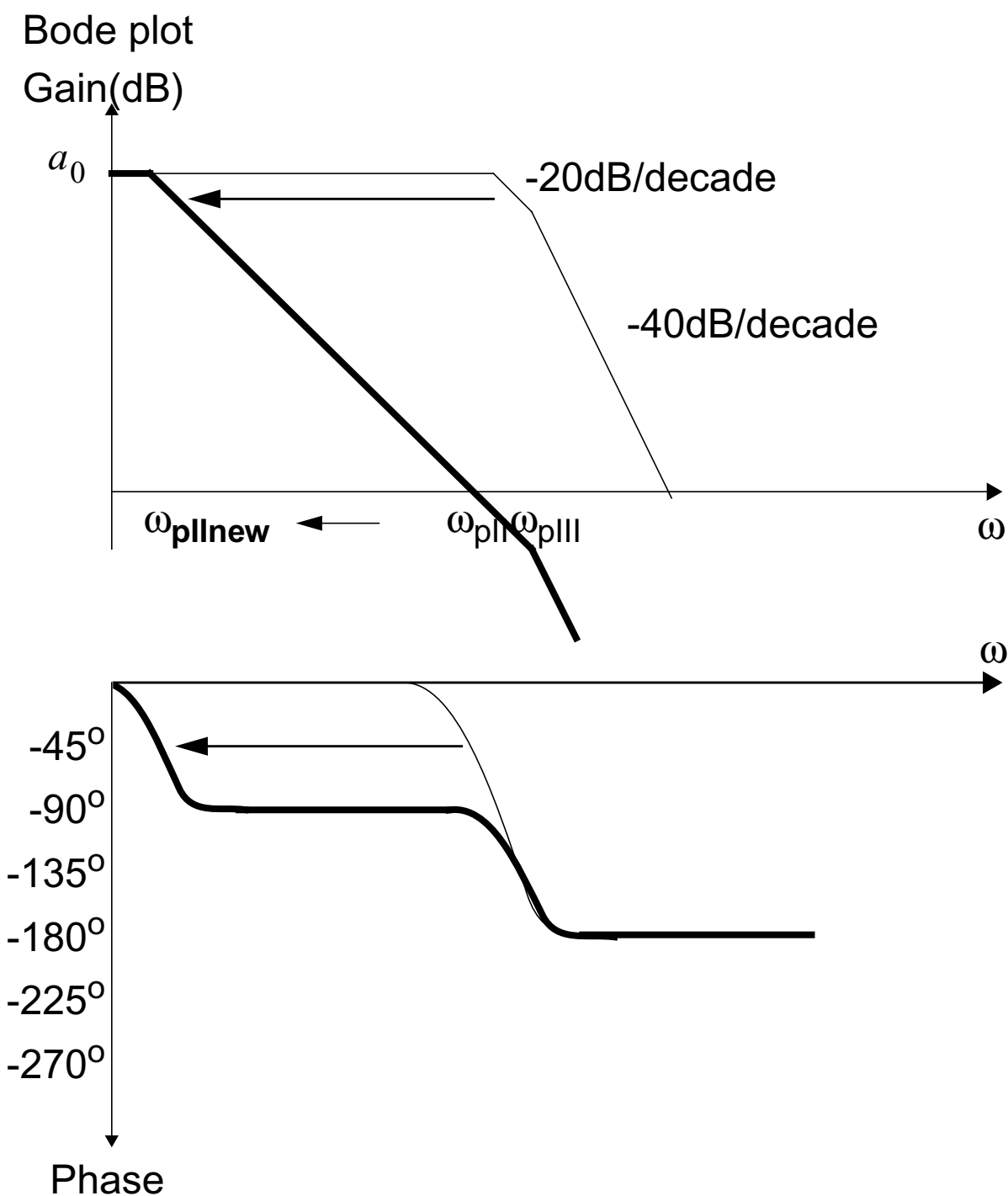
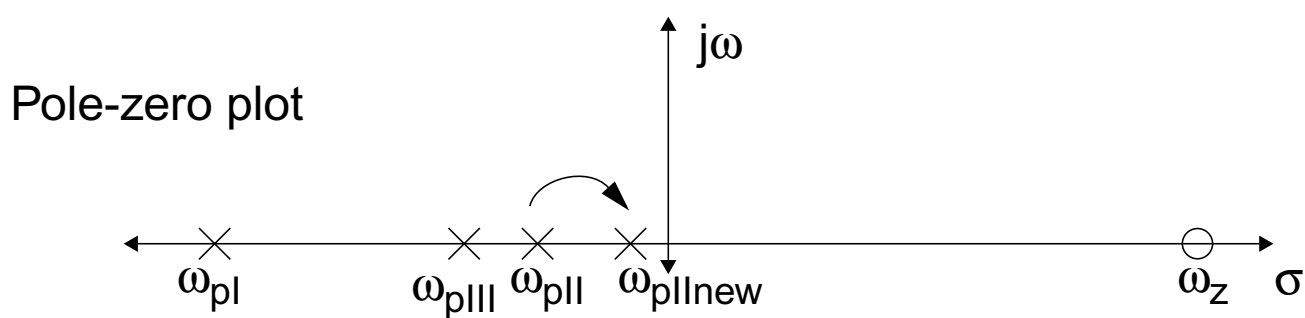


Add large compensation capacitance C_C to node II to make pole at this node dominant

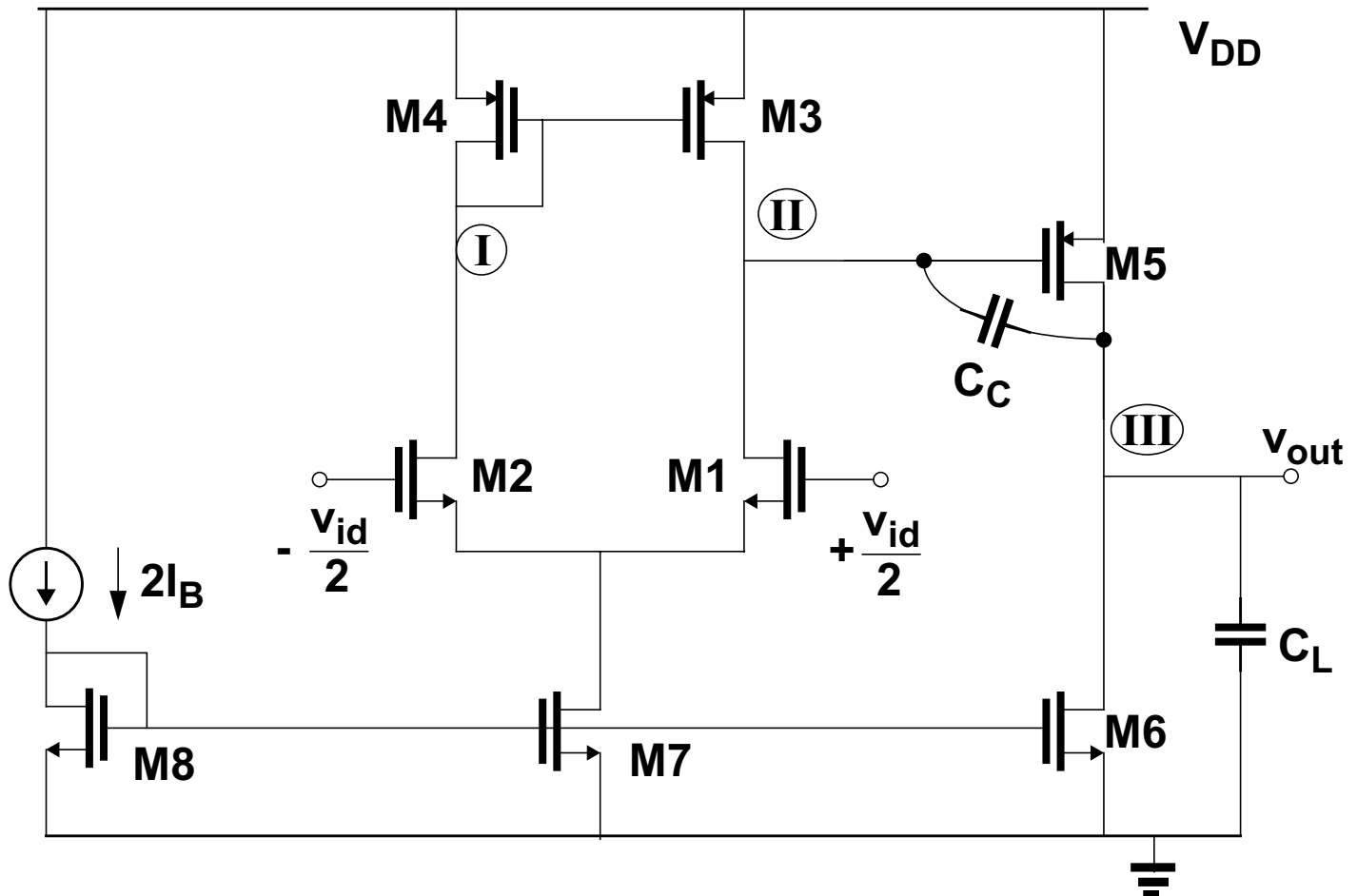
$$\omega_{pII} = -\frac{g_{ds1} + g_{ds3}}{C_{II} + C_C}$$

This requires a very large capacitor.

2-stage amplifier: dominant pole compensation



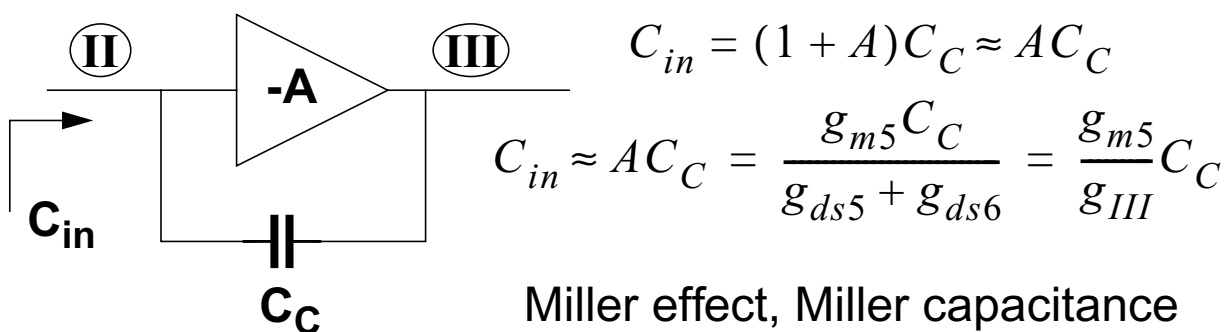
9.3.2 2-stage amplifier: Compensation by pole-splitting (intuitive analysis)



Add large compensation capacitance between node II and III

What is the capacitive loading at node II?

i.e. What effective capacitance does node II see looking into C_C ?

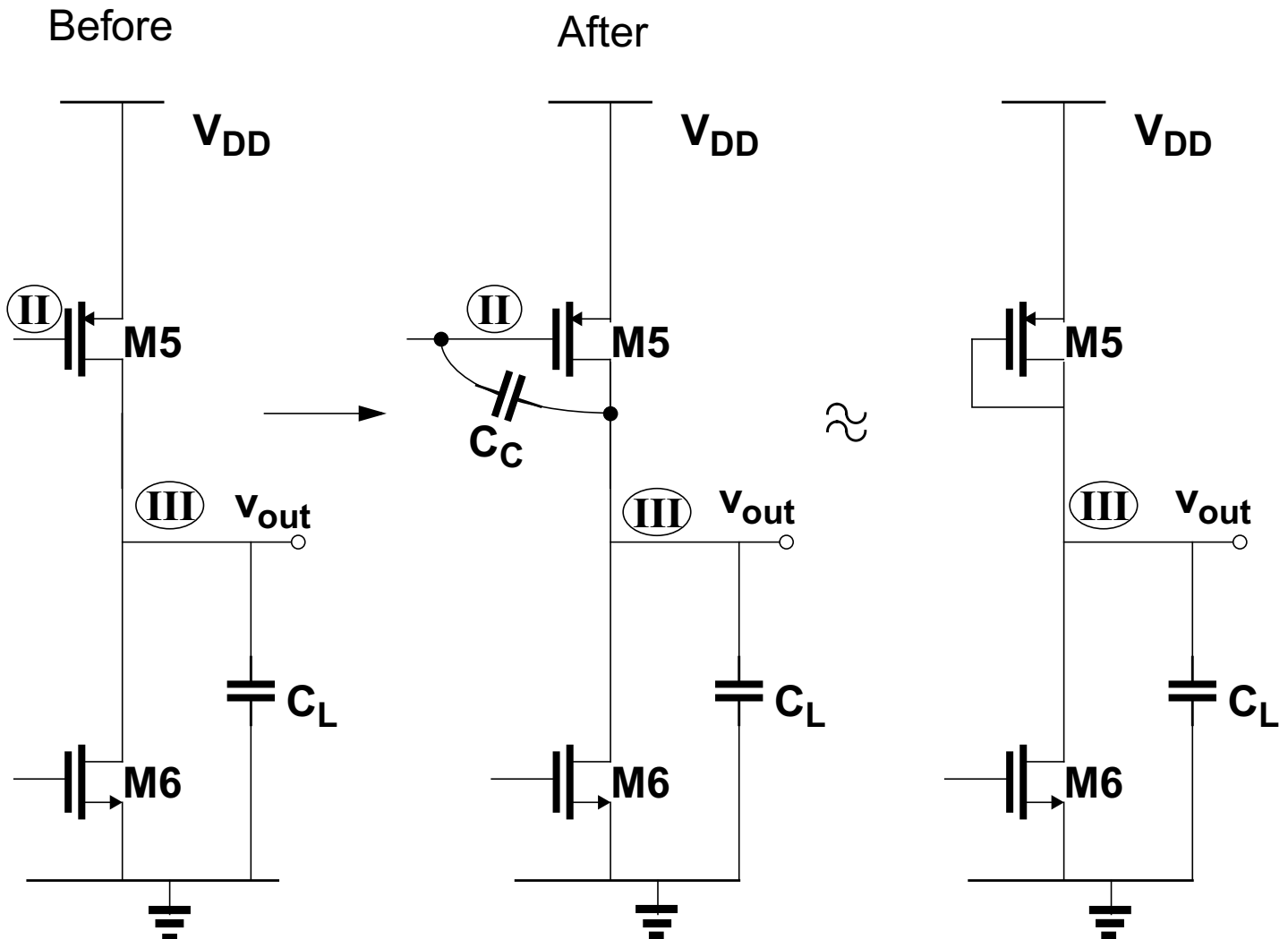


$$\omega_{pII} = -\frac{g_{II}}{C_{II}} = -\frac{g_{II}}{\frac{g_{m5}}{g_{III}}C_C} = -\frac{g_{ds1} + g_{ds3}}{\frac{g_{m5}C_C}{g_{ds5} + g_{ds6}}}$$

=> ω_{pII} goes down to a lower frequency (becomes dominant pole)

Compensation of two stage differential amplifier

What happens the pole at the output node ω_{pIII} ?



$$\omega_{pIII} = -\frac{g_{III}}{C_L}$$

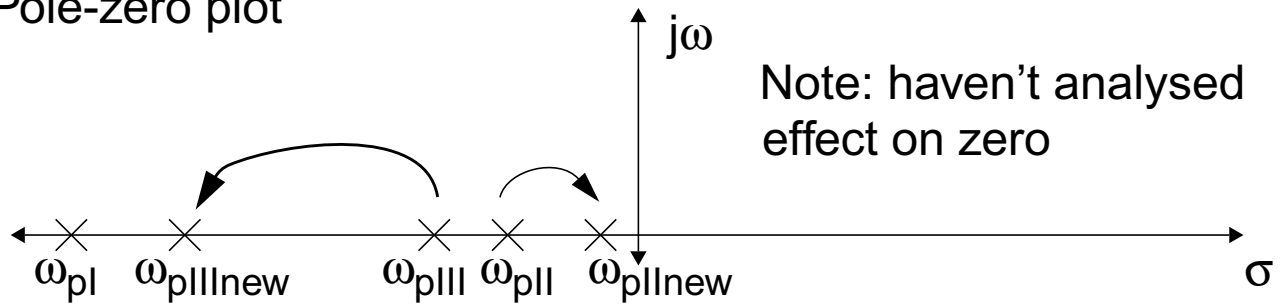
$$\omega_{pIII} = -\frac{g_{ds5} + g_{ds6}}{C_L}$$

C_C looks like a short at high frequencies

$$\omega_{pIII} \approx -\frac{g_{m5}}{C_L}$$

$\Rightarrow \omega_{pIII}$ goes up

Pole-zero plot



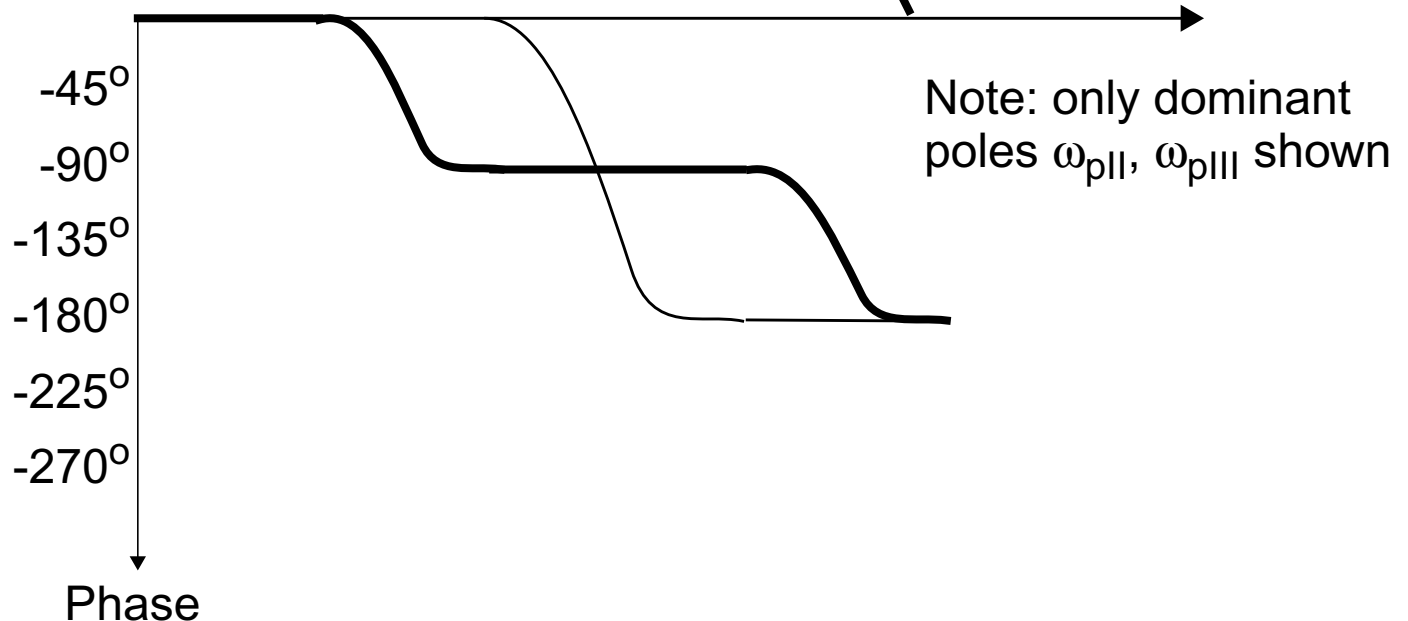
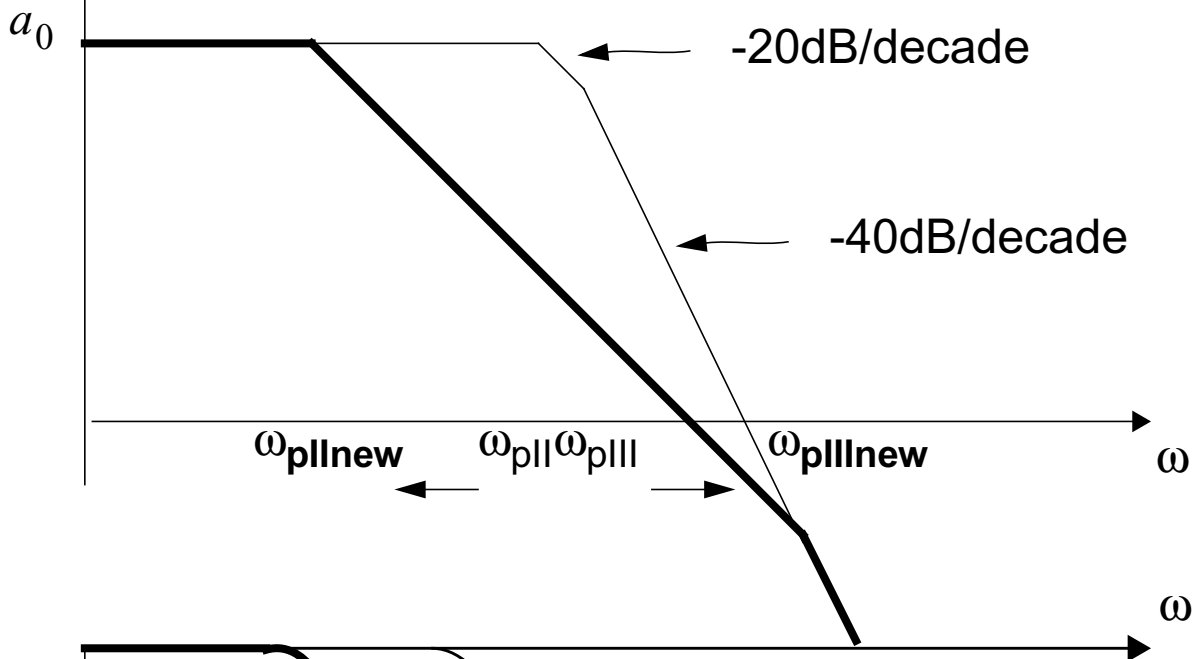
ω_{pII} becomes the dominant pole

ω_{pIII} is pushed to a higher frequency

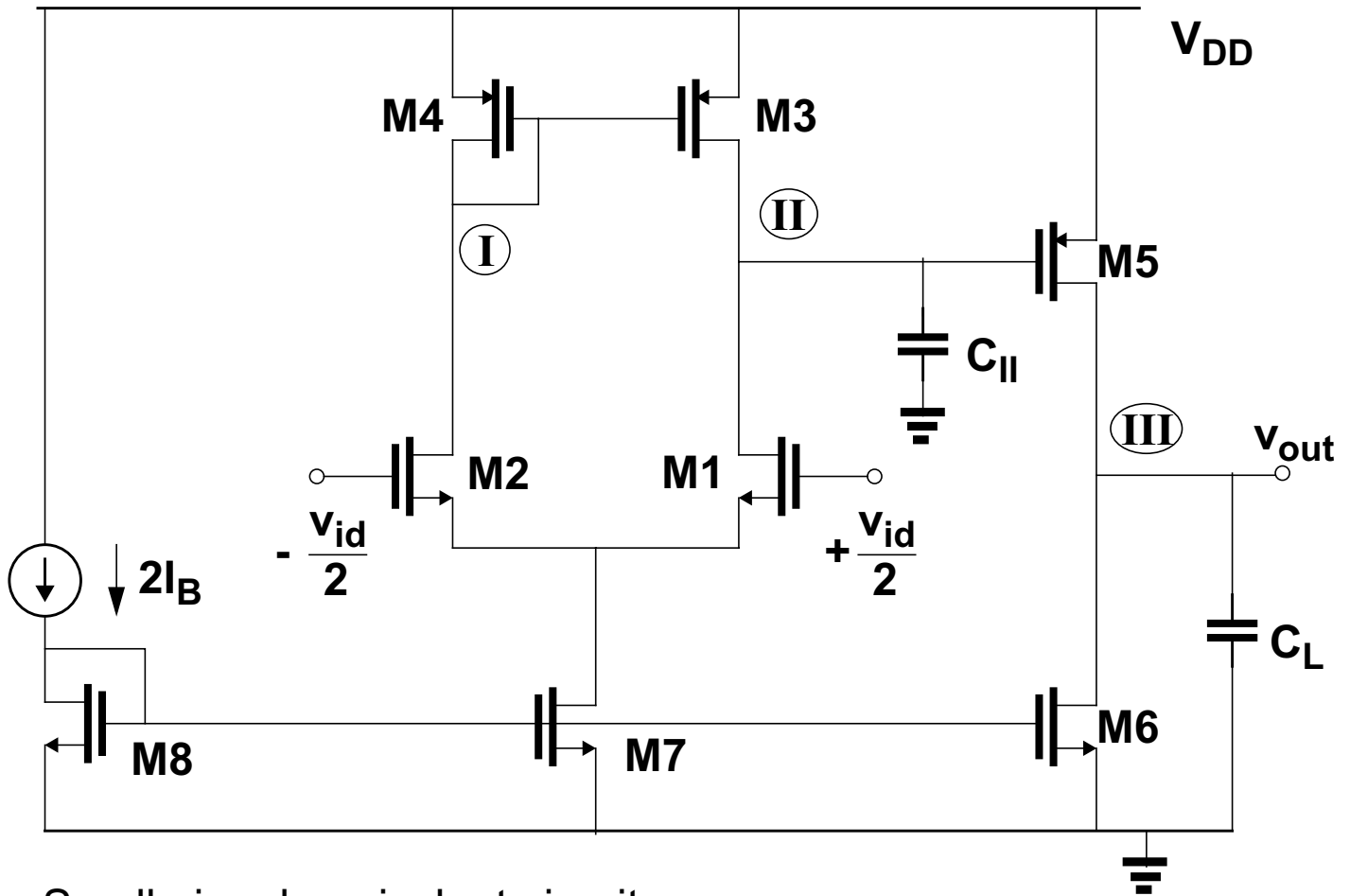
'pole splitting'

Bode plot

Gain(dB)

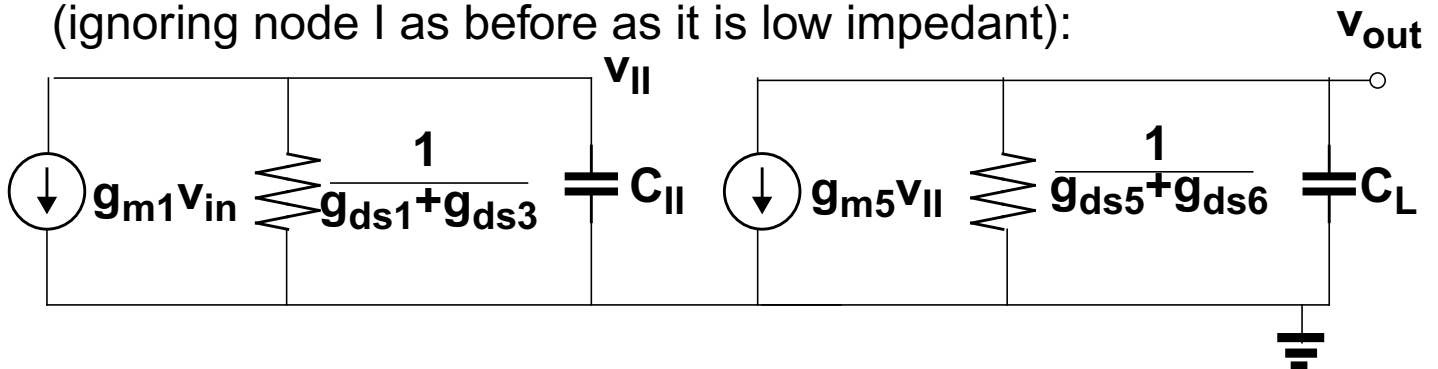


9.3.3 2-stage amplifier: Dominant-pole compensation (mathematical analysis)



Small-signal equivalent circuit

(ignoring node I as before as it is low impedant):



$$\frac{v_{out}}{v_{in}}(s) = \frac{g_{m1}}{g_{ds1} + g_{ds3} + sC_{II}} \cdot \frac{g_{m5}}{g_{ds5} + g_{ds6} + sC_L}$$

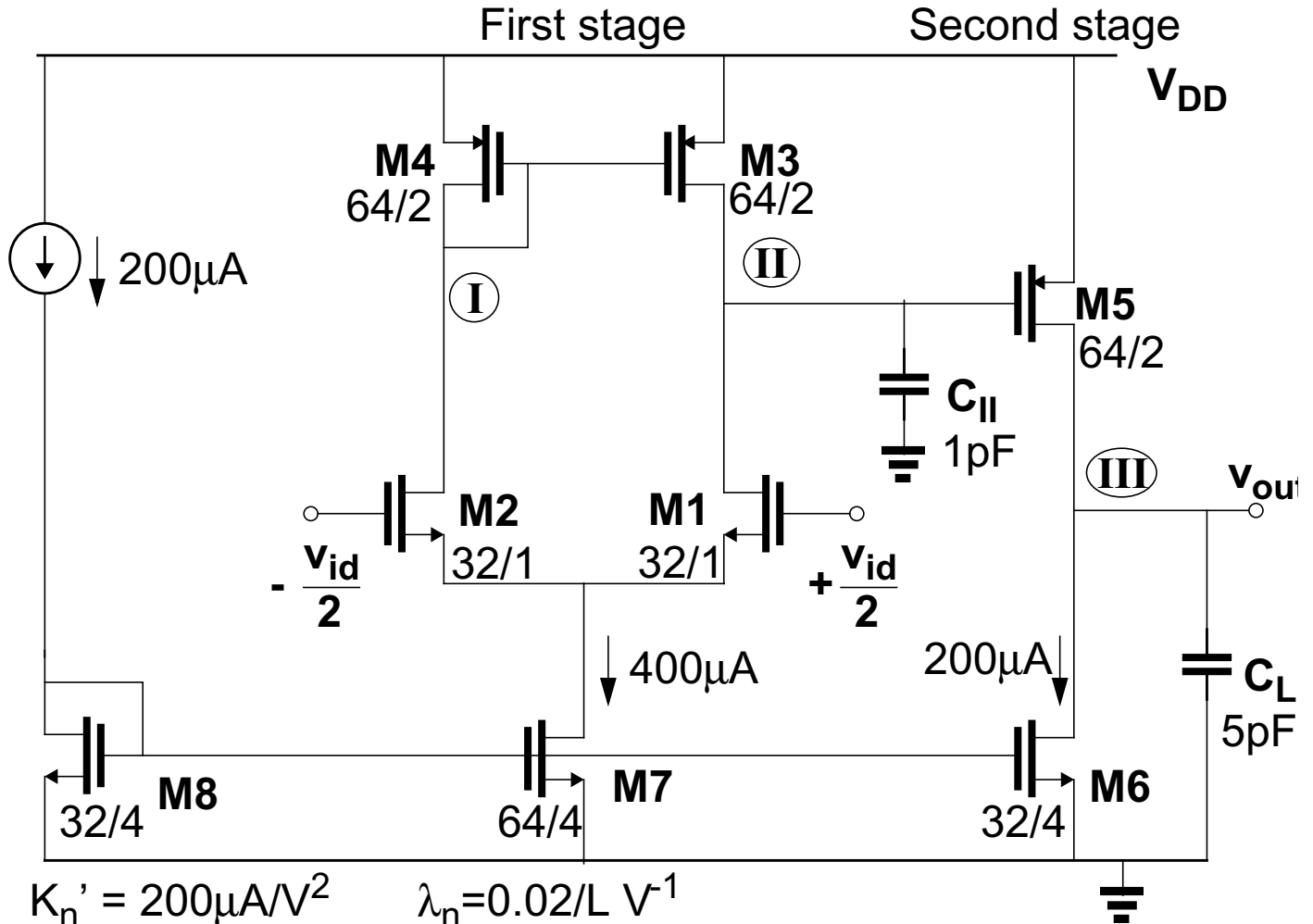
$$\frac{v_{out}}{v_{in}}(s) = \frac{g_{m1}}{g_{ds1} + g_{ds3}} \cdot \frac{g_{m5}}{g_{ds5} + g_{ds6}} \cdot \frac{1}{1 + \frac{sC_{II}}{g_{ds1} + g_{ds3}}} \cdot \frac{1}{1 + \frac{sC_L}{g_{ds5} + g_{ds6}}}$$

$$\frac{v_{out}}{v_{in}}(s) = a_0 \cdot \frac{1}{1 - \frac{s}{\omega_{pII}}} \cdot \frac{1}{1 - \frac{s}{\omega_{pIII}}}$$

$$\omega_{pII} = -(g_{ds1} + g_{ds3})/C_{II}$$

$$\omega_{pIII} = -(g_{ds5} + g_{ds6})/C_L$$

9.3.4 2-stage amplifier: Dominant-pole compensation (numerical example)



$$K_n' = 200\mu A/V^2 \quad \lambda_n = 0.02/L \text{ V}^{-1}$$

$$K_p' = 50\mu A/V^2 \quad \lambda_p = 0.04/L \text{ V}^{-1}$$

Ignore all capacitances except C_{II} and C_L

$$g_{m1} = \sqrt{2K_n' \left(\frac{W}{L}\right)_1 I_{D1}} = \sqrt{2 \times 200\mu A/V \times \frac{32}{1} \times 200\mu A} = 1.6mA/V$$

$$g_{ds1} = \lambda_n I_{D1} = \frac{0.02}{1} \times 200\mu A = 4\mu A/V$$

$$g_{ds3} = \lambda_p I_{D4} = \frac{0.04}{2} \times 200\mu A = 4\mu A/V$$

$$g_{m5} = \sqrt{2K_p' \left(\frac{W}{L}\right)_5 I_{D5}} = \sqrt{2 \times 50\mu A/V \times \frac{64}{2} \times 200\mu A} = 800\mu A/V$$

$$g_{ds6} = \lambda_n I_{D6} = \frac{0.02}{4} \times 200\mu A = 1\mu A/V$$

$$g_{ds5} = \lambda_p I_{D4} = \frac{0.04}{2} \times 200\mu A = 4\mu A/V$$

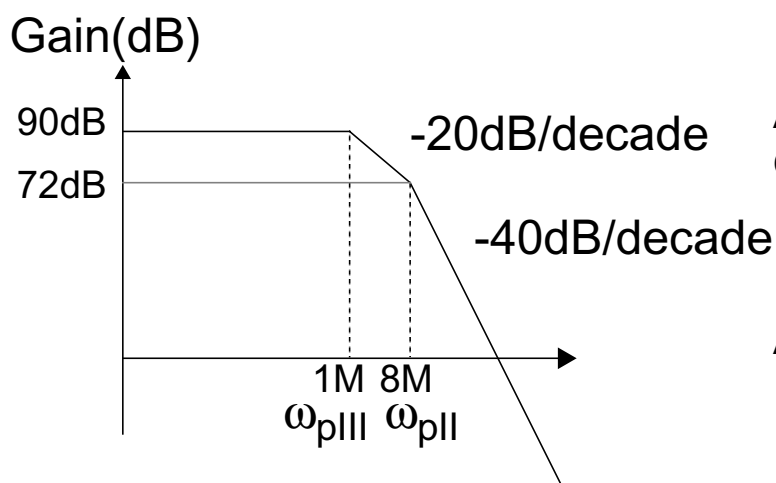
Low-frequency small-signal gain

$$a_0 = \frac{g_{m1}}{g_{ds1} + g_{ds3}} \cdot \frac{g_{m5}}{g_{ds5} + g_{ds6}}$$

$$= \frac{1600\mu A/V}{4\mu A/V + 4\mu A/V} \cdot \frac{800\mu A/V}{4\mu A/V + 1\mu A/V} = 32000 = 90dB$$

$$|\omega_{pII}| = \frac{g_{ds1} + g_{ds3}}{C_{II}} = \frac{4\mu A/V + 4\mu A/V}{1pF} = 8Mrad/s$$

$$|\omega_{pIII}| = \frac{g_{ds6} + g_{ds5}}{C_L} = \frac{1\mu A/V + 4\mu A/V}{5pF} = 1Mrad/s$$



$$a_0 = 90dB$$

First pole at $1Mrads^{-1}$

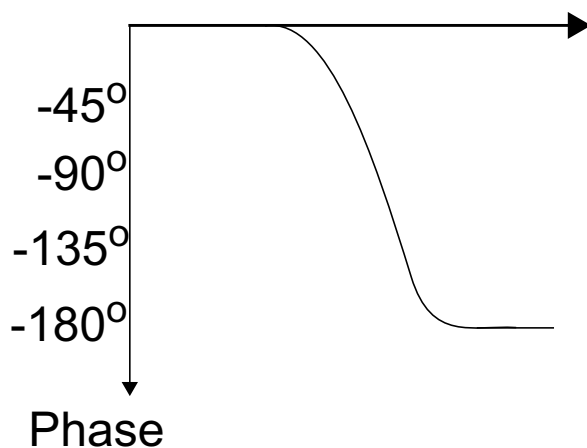
At second pole gain has dropped to 72dB (6dB/octave)

After this 40dB/decade roll-off

When gain falls to 1 (0dB)
phase shift is 180°

=> phase margin = 0°

=> amplifier needs
compensation if used in
feedback configuration.



Dominant pole compensation

Reduce frequency of first pole so than gain has dropped to 0dB at frequency of second pole

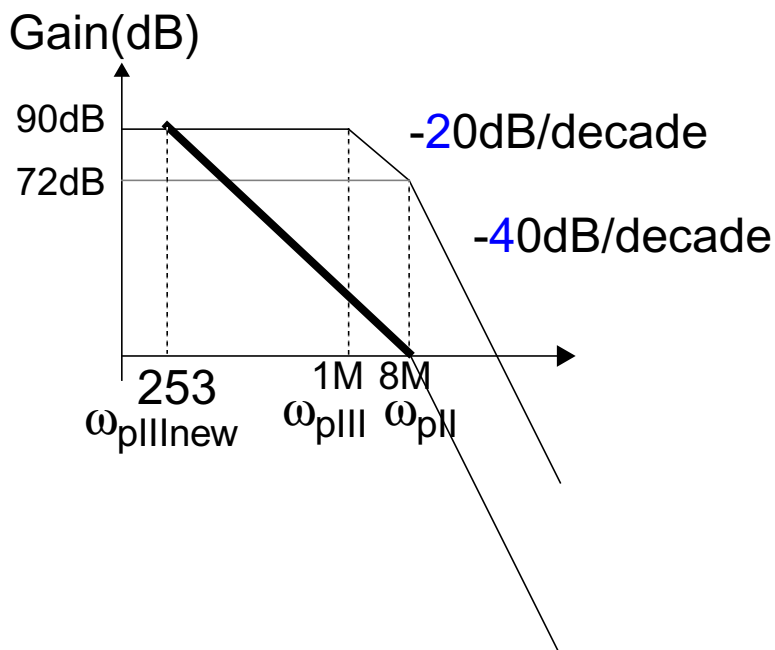
This gives 45° phase margin

For 0dB at 8M gain will have to drop 90dB i.e ~15 octaves, or 4.5 decades

$$|\omega_{pIIInew}| a_0 = |\omega_{pIII}|$$

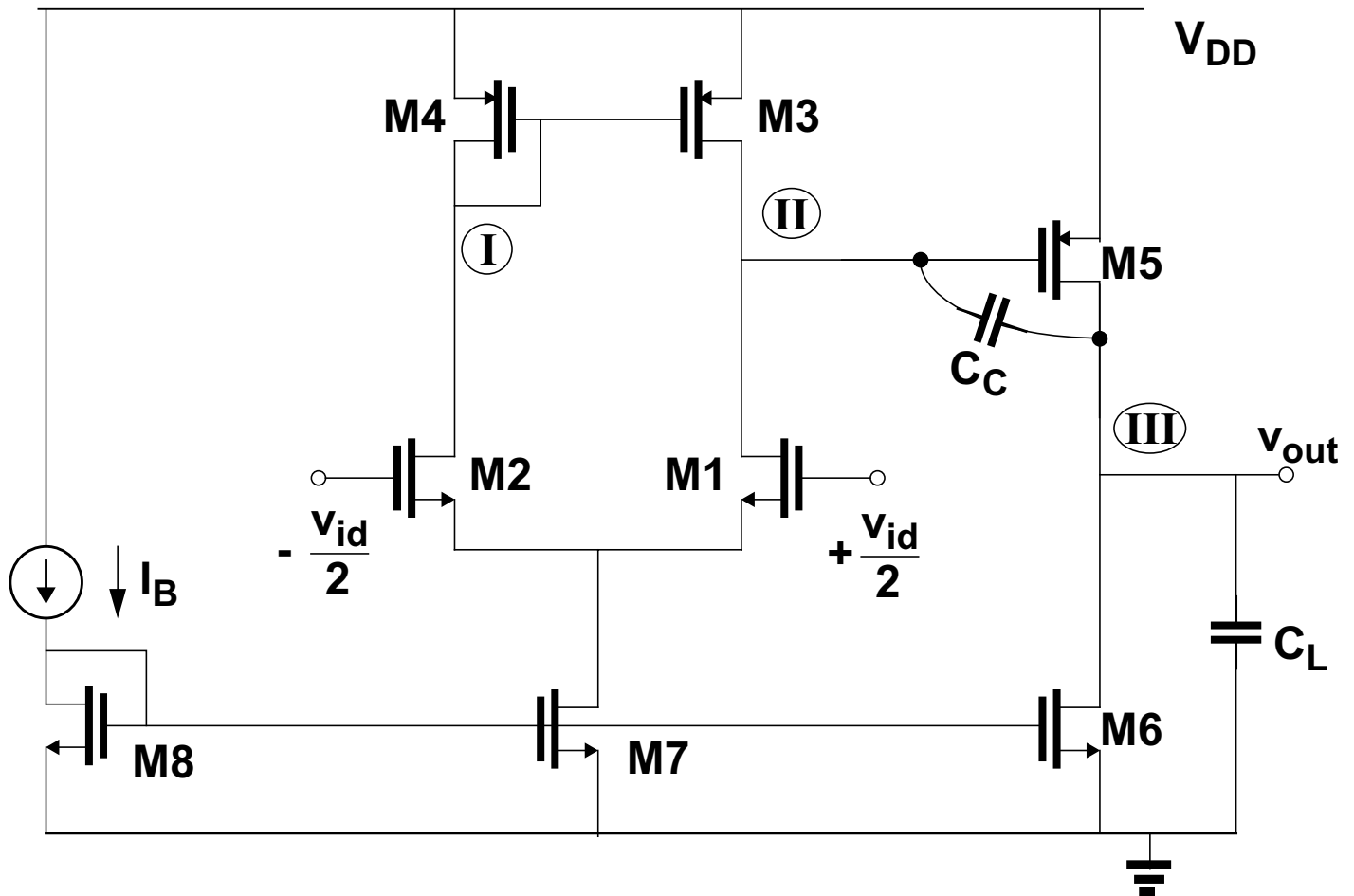
$$|\omega_{pIIInew}| = \frac{8M}{\frac{90}{2^{6.02}}} = \frac{8M}{10^{\frac{90}{20}}} = 253$$

$$|\omega_{pIIInew}| = \frac{g_{ds6} + g_{ds5}}{C_L} \Rightarrow C_L = \frac{g_{ds6} + g_{ds5}}{|\omega_{pIIInew}|} = \frac{5\mu A/V}{253 rad/s} \cong 20nF$$



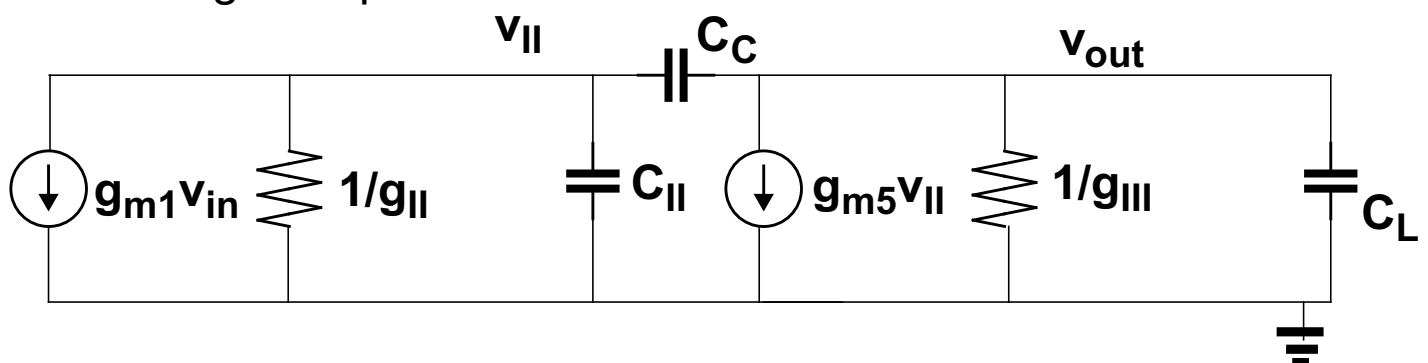
This amount of capacitance cannot economically be integrated.

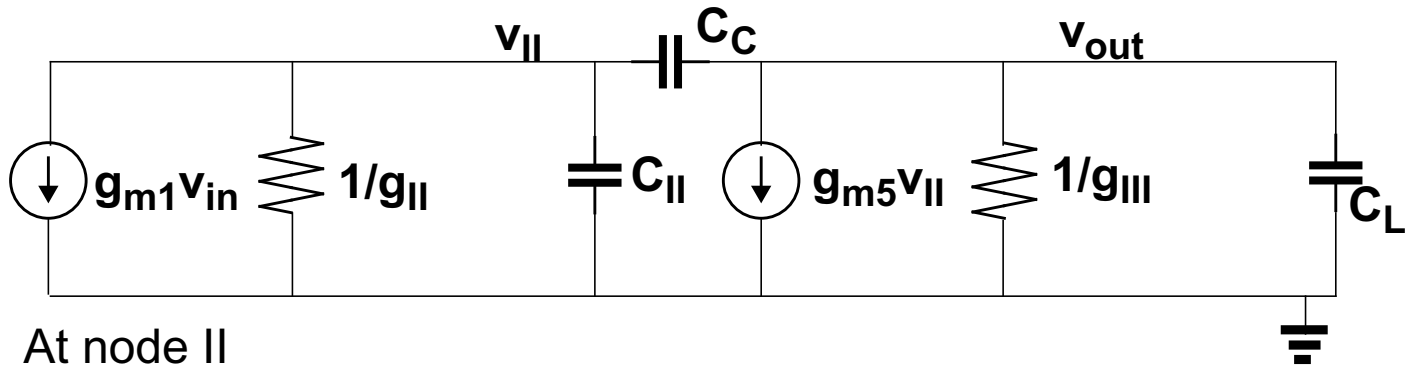
9.3.5 2-stage amplifier: pole-splitting compensation: mathematical approach



Add large compensation capacitance across M5
 Reduces frequency of first-stage pole
 Increase frequency of second-stage pole } Pole splitting

Small-signal equivalent circuit





At node II

$$g_{m1}v_{in} + g_{II}v_{II} + sC_{II}v_{II} + sC_c(v_{II} - v_{out}) = 0 \quad (1)$$

At node III

$$g_{m5}v_{II} + g_{III}v_{out} + sC_Lv_{out} + sC_C(v_{out} - v_{II}) = 0 \quad (2)$$

Rewrite (2) for v_{II}

$$v_{II} = v_{out} \frac{(g_{III} + sC_L + sC_C)}{-g_{m5} + sC_C}$$

Substitute for v_{II} in (1)

$$g_{m1}v_{in} + (g_{II} + sC_{II} + sC_C) \frac{(g_{III} + sC_L + sC_C)}{-g_{m5} + sC_C} v_{out} - sC_C v_{out} = 0$$

$$g_{m1}v_{in} = \left(sC_C - \frac{(g_{II} + sC_{II} + sC_C)(g_{III} + sC_L + sC_C)}{-g_{m5} + sC_C} \right) v_{out}$$

$$\begin{aligned} \frac{v_{out}}{v_{in}}(s) &= \frac{g_{m1}(g_{m5} - sC_C)}{g_{II}g_{III} + s(g_{m5}C_C + g_{II}(C_L + C_C) + g_{III}(C_{II} + C_C)) + s^2(C_{II}C_L + C_{II}C_C + C_C C_L)} \\ &= \frac{g_{m1}g_{m5}}{a_0} \frac{\left(1 - \frac{sC_C}{g_{m5}}\right)}{\left(1 + s\left(\frac{g_{m5}C_C}{g_{II}g_{III}} + \frac{C_L + C_C}{g_{III}} + \frac{C_{II} + C_C}{g_{II}}\right) + s^2\left(\frac{C_{II}C_L + C_{II}C_C + C_C C_L}{g_{II}g_{III}}\right)\right)} \\ &\quad \text{dominant } s \text{ term since } g_m/g_{ds} \gg 1 \end{aligned}$$

$$\frac{v_{out}}{v_{in}}(s) = a(s) = a_0 \frac{\left(1 - \frac{sC_C}{g_{m5}}\right)}{1 + s\left(\frac{g_{m5}C_C}{g_{II}g_{III}}\right) + s^2\left(\frac{C_{II}C_L + C_{II}C_C + C_C C_L}{g_{II}g_{III}}\right)}$$

We know this to be a 2 pole system with poles at $-\omega_{pII}$, $-\omega_{pIII}$ so denominator is of the form

$$\begin{aligned} & \left(1 - \frac{s}{\omega_{pII}}\right)\left(1 - \frac{s}{\omega_{pIII}}\right) \\ &= 1 - \frac{s}{\omega_{pII}} - \frac{s}{\omega_{pIII}} + \frac{s^2}{\omega_{pII}\omega_{pIII}} \end{aligned}$$

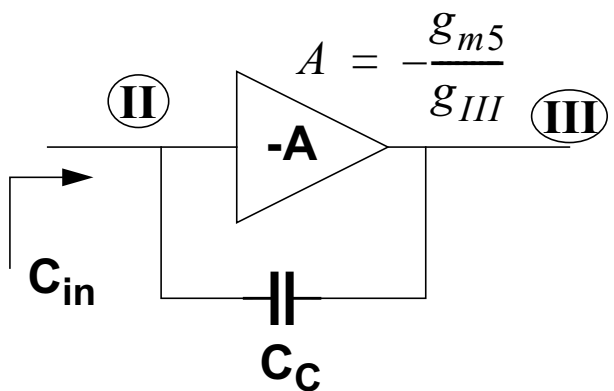
Assume ω_{pII} is the dominant pole i.e. $\omega_{pII} \ll \omega_{pIII}$ so we ignore the s/ω_{pIII} term

The denominator now becomes

$$1 - \frac{s}{\omega_{pII}} + \frac{s^2}{\omega_{pII}\omega_{pIII}}$$

Equating with denominator of above (for s term) we get

$$\begin{aligned} \omega_{pII} &= -\frac{g_{II}g_{III}}{g_{m5}C_C} \\ &= -\frac{g_{II}}{\frac{g_{m5}}{g_{III}}C_C} \end{aligned}$$



$A = -\frac{g_{m5}}{g_{III}}$

$$C_{in} \approx AC_C = \frac{g_{m5}C_C}{g_{ds5} + g_{ds6}} = \frac{g_{m5}}{g_{III}}C_C$$

i.e value of C_C has been multiplied by gain of second stage Miller capacitance

Equate s^2 term to get ω_{pIII}

$$\frac{s^2}{\omega_{pII}\omega_{pIII}} = s^2 \left(\frac{C_{II}C_L + C_{II}C_C + C_C C_L}{g_{II}g_{III}} \right)$$

$$\omega_{pII}\omega_{pIII} = \frac{g_{II}g_{III}}{C_{II}C_L + C_{II}C_C + C_C C_L}$$

$$\omega_{pIII} = \frac{1}{\omega_{pII}} \cdot \frac{g_{II}g_{III}}{C_{II}C_L + C_C(C_{II} + C_L)}$$

$$\omega_{pIII} = -\frac{g_{m5}C_C}{g_{II}g_{III}} \cdot \frac{g_{II}g_{III}}{C_{II}C_L + C_C(C_{II} + C_L)} = -\frac{g_{m5}C_C}{C_{II}C_L + C_C(C_{II} + C_L)}$$

If $C_L \gg C_{II}$ this reduces to $\omega_{pIII} = -\frac{g_{m5}C_C}{C_{II}C_L + C_C C_L}$

If also $C_C \gg C_{II}$ this then reduces to $\omega_{pIII} = -\frac{g_{m5}}{C_L}$

Poles:

$$\omega_{pII} = -\frac{g_{II}}{\frac{g_{m5}}{g_{III}}C_C}$$

Zero:

$$\omega_z = \frac{g_{m5}}{C_C}$$

$$\omega_{pIII} = -\frac{g_{m5}}{C_L} \quad \text{if } C_C \text{ and } C_L \text{ are } \gg C_{II}$$

9.3.6 2-stage amplifier: pole-splitting compensation: (numerical example)

Pick $C_C = 20\text{pF}$

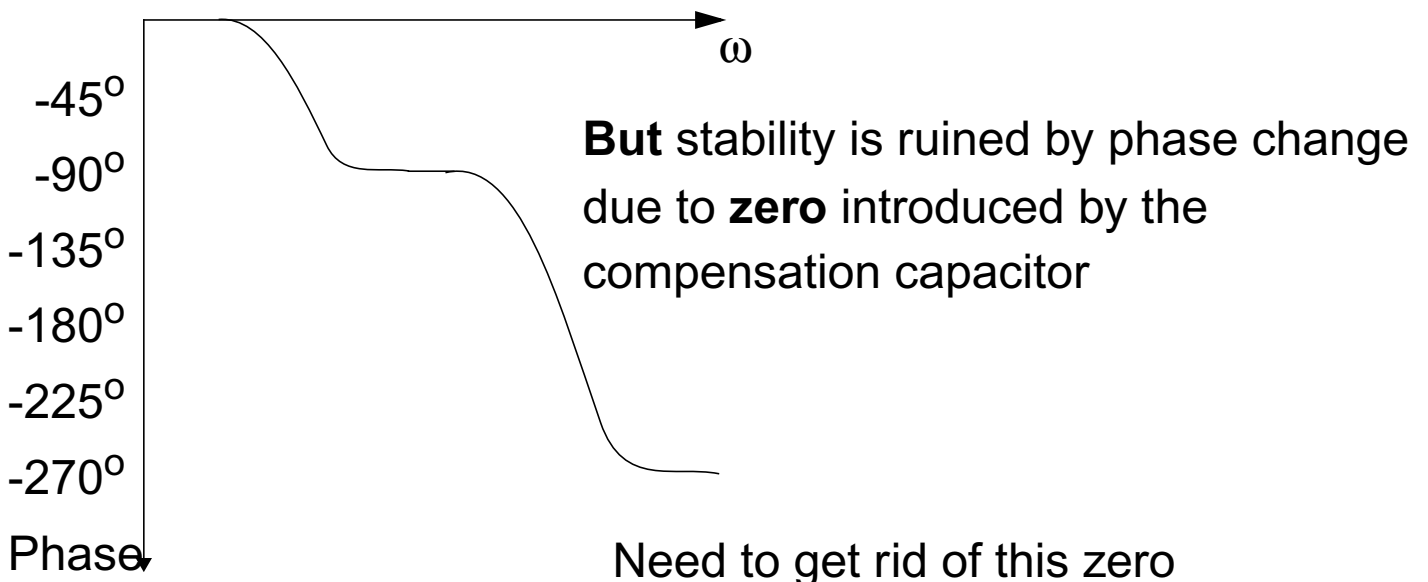
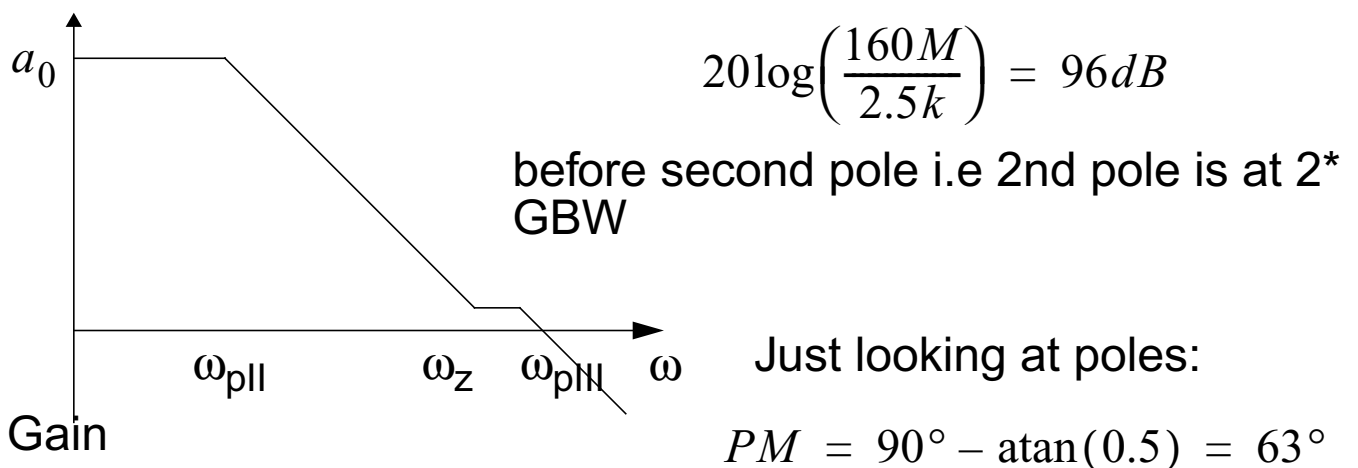
$$|\omega_{pII}| = \frac{g_{II}}{\frac{g_{m5}}{g_{III}} C_C} = \frac{g_{ds1} + g_{ds3}}{\frac{g_{m5}}{g_{ds6} + g_{ds5}} C_C} = \frac{4\mu\text{A}/V + 4\mu\text{A}/V}{\frac{800\mu\text{A}/V}{1\mu\text{A}/V + 4\mu\text{A}/V} 20\text{pF}}$$

$$|\omega_{pII}| = 2.5\text{krad/s}$$

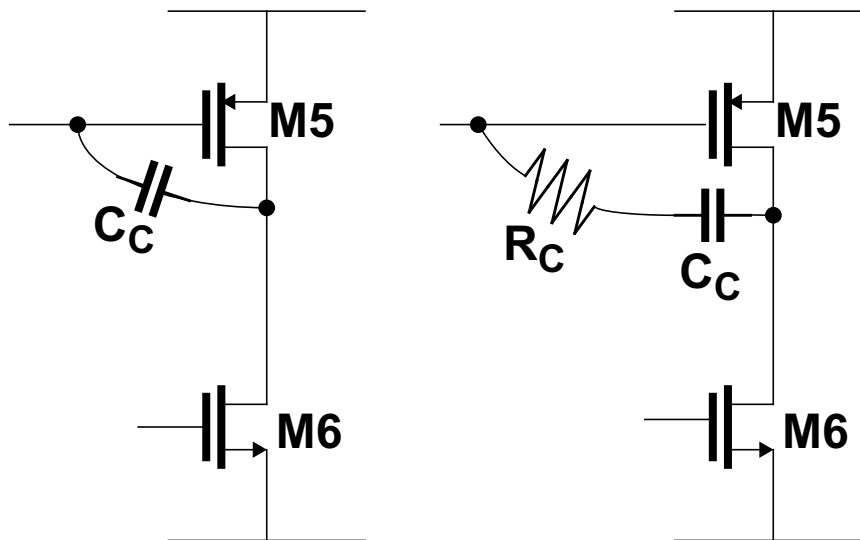
$$|\omega_{pIII}| = \frac{g_{m5}}{C_L} = -\frac{800\mu\text{A}/V}{5\text{pF}} = 160\text{Mrad/s}$$

$$\omega_z = \frac{g_{m5}}{C_C} = \frac{800\mu\text{A}/V}{20\text{pF}} = 40\text{Mrad/s}$$

Pole -splitting has made one pole (ω_{pII}) dominant and pushed out the other pole (ω_{pIII}). Gain will have dropped by



Get rid of zero by putting resistor in series with C_C



It can be shown that
$$\omega_z = \frac{1}{\frac{C_C}{g_{m5}} - R_C C_C}$$

i.e. as R_C is increased from zero ω_z is pushed further out

If you set $R_C = 1/g_{m5}$ then theoretically $\omega_z = \infty$

It can be shown that the positions of ω_{pII} , ω_{pIII} are only slightly affected by the addition of R_C

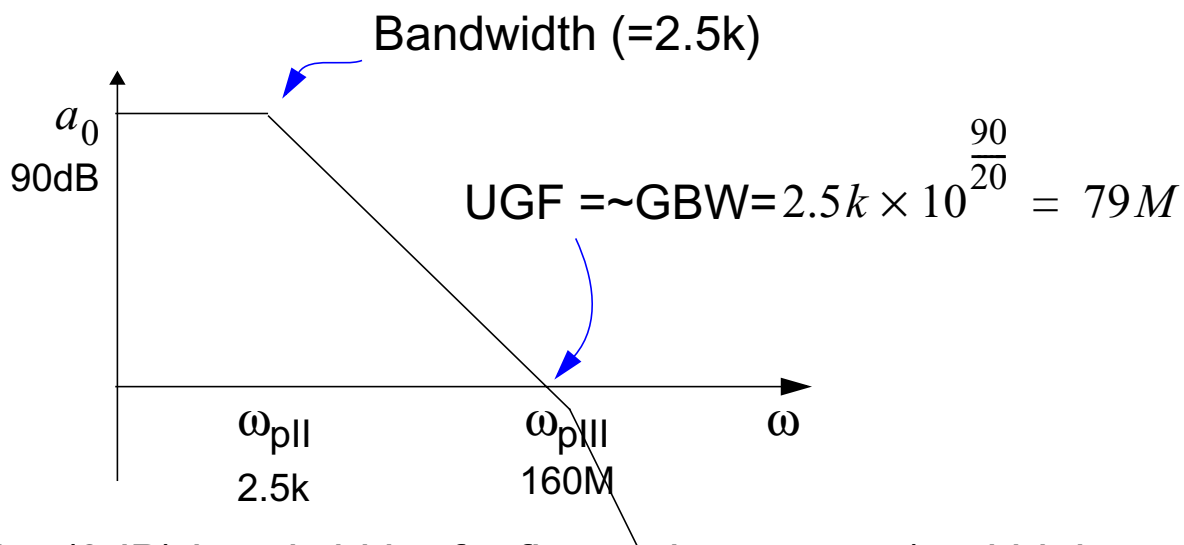
so still valid:
$$|\omega_{pII}| = \frac{g_{II}}{\frac{g_{m5}}{g_{III}} C_C} \quad |\omega_{pIII}| = \frac{g_{m5}}{C_L}$$

Do get extra pole due to R_C at

$$|\omega_{pRc}| = \frac{1}{R_C C_{II}}$$

With $C_{II} \ll C_C$, $C_L \Rightarrow$ this pole not dominant

Note on Gain Bandwidth (GBW):



The (3dB) bandwidth of a first-order system (and higher order systems with a dominant pole) is given by the frequency of the dominant pole, ω_{pII} in this case.

Recall that the Gain Bandwidth (GBW) is the product of the DC gain and the (3dB) bandwidth.

For a first order system this is equal to the unity gain frequency (UGF).

For higher order systems, if $\omega_{pIII} > \text{GBW}$, the same is approximately true, and a phase margin of least 45° is guaranteed.

In this case:

$$GBW = \overbrace{\frac{g_{m1}g_{m5}}{g_{II}g_{III}}}^{a_0} \cdot \overbrace{\frac{g_{II}}{\frac{g_{m5}}{g_{III}}C_C}}^{\omega_{pII}} = \frac{g_{m1}}{C_C}$$

Require: $|\omega_{pIII}| > GBW$

$$\frac{g_{m5}}{C_L} > \frac{g_{m1}}{C_C}$$

$$\frac{g_{m5}}{g_{m1}} > \frac{C_L}{C_C}$$

This can be a useful guide

Note that the preceding analysis contains a number of assumptions e.g. regarding loading, which will not hold true in all cases.

In particular, driving a resistive load can alter the situation significantly as it represents both a different load and reduces the gain of the output stage (and so reduces the Miller effect).

A general approach is to estimate the value of the compensation capacitor required, then tweak the value of the zeroing resistor (aka Miller resistor) R_C by iterative simulations.

10 Noise

There are two types of noise in ICs

1. Interference noise i.e. noise due to disturbances through power supply, ground or substrate.
2. Inherent noise in the devices

Here we deal with type 2.

Noise is a fundamental physical phenomenon and is generated by all active devices and by resistors.

It is therefore present in all circuits and is processed along with the desired signal.

The presence of noise degrades the quality of a signal and determines the smallest signal that can be distinguished.

10.1 Signal-to-Noise ratio

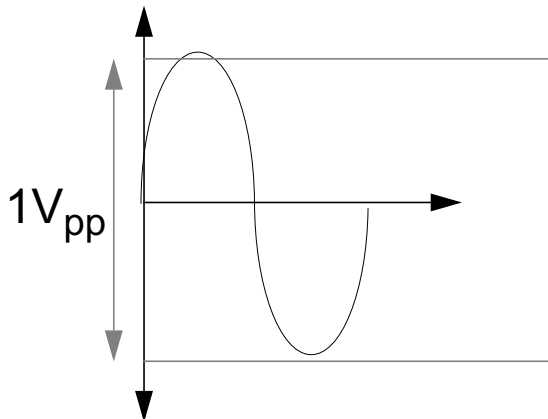
The quality of a signal in the presence of noise is specified by the signal-to-noise ratio (SNR).

$$SNR = 10 \log \left[\frac{\text{signal power}}{\text{noise power}} \right]$$

For a given signal $v(t)$ with a normalised signal power of v_{rms}^2 and a normalised noise power v_{nrms}^2

$$SNR = 10 \log \left[\frac{v_{rms}^2}{v_{nrms}^2} \right] = 20 \log \left[\frac{v_{rms}}{v_{nrms}} \right]$$

Example: If a circuit produces an output sine-wave of 1V peak-peak and has an output noise voltage of 1mVrms, what is the SNR?



For sine wave:

$$RMSvalue = \frac{V_{pp}}{2\sqrt{2}}$$

$$SNR = 20 \log \left(\frac{\frac{1}{2\sqrt{2}}}{1mV} \right) = 51dB$$

Dynamic range of a circuit is the maximum signal divided by the noise level i.e the maximum SNR

10.2 Average Power of Noise

Noise is a random process -> the amplitude of the noise at any one time (instantaneous value) cannot be predicted.

However for most circuit noise the average power over a long time can be predicted.

The average power delivered by a periodic voltage $v(t)$ of period T into a load resistance R_L is given by

$$P_{av} = \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} \frac{v^2(t)}{R_L} dt$$

The average power of a noise voltage source $x(t)$ over a load resistance R_L is given by

$$P_{av} = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} \frac{x^2(t)}{R_L} dt$$

which is usually normalised to the power over a resistor of 1Ω

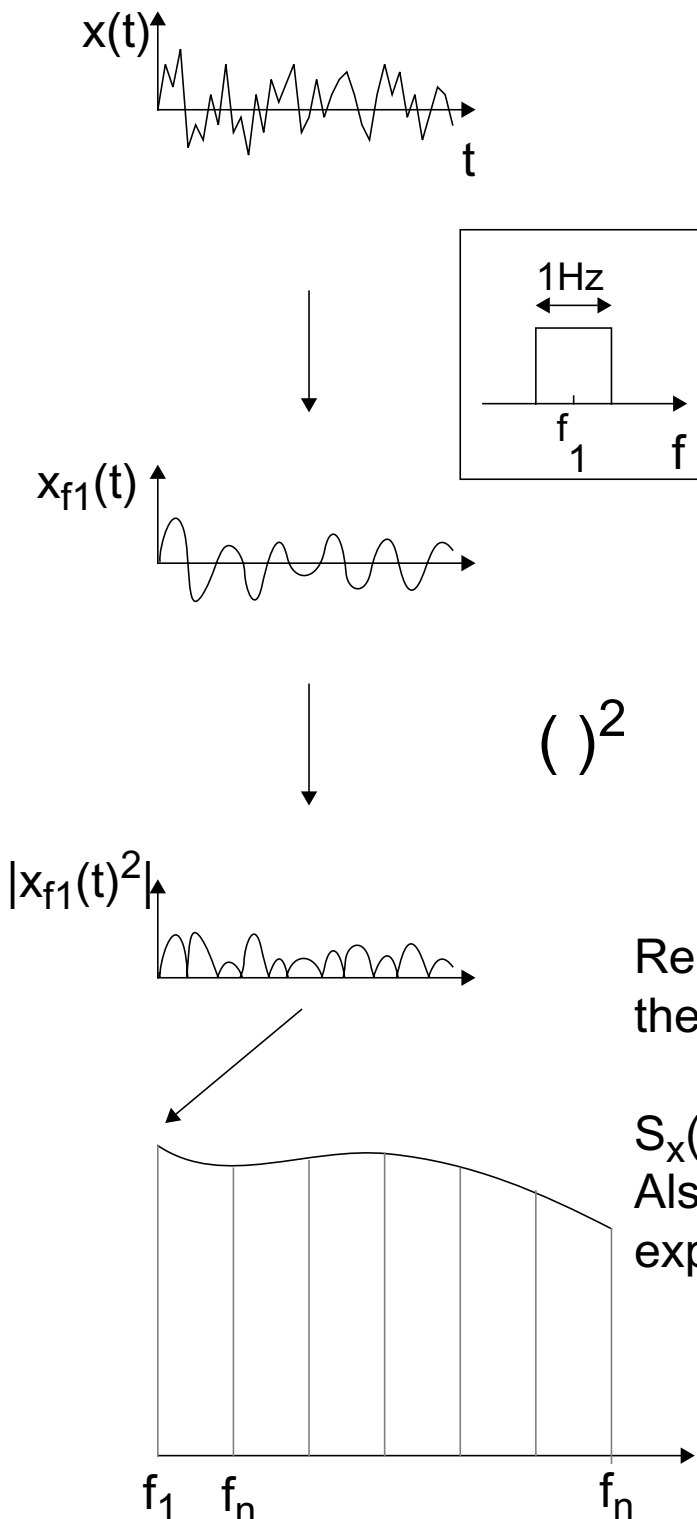
$$P_{av} = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} x^2(t) dt \quad \text{expressed in } V^2$$

The root-mean-square (rms) value ie $\sqrt{P_{av}}$ is also commonly used and is expressed in Volts

10.3 Spectrum of noise (frequency content of noise)

Spectrum or 'Power Spectral Density' PSD of a signal shows how much power a signal contains at each frequency.

For a noise signal the PSD, $S_x(f)$, of $x(t)$ is the average power of $x(t)$ in a bandwidth of 1Hz around f .



Noise signal $x(t)$

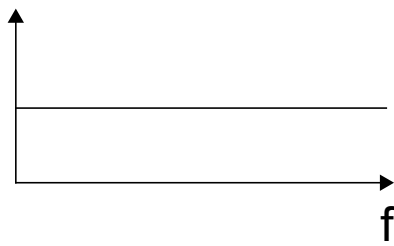
Calculate the PSD at a single frequency f_1 by putting the signal through a bandpass filter of bandwidth 1Hz and squaring the output, and calculating the average over a long time.
This gives $S_x(f_1)$

$()^2$

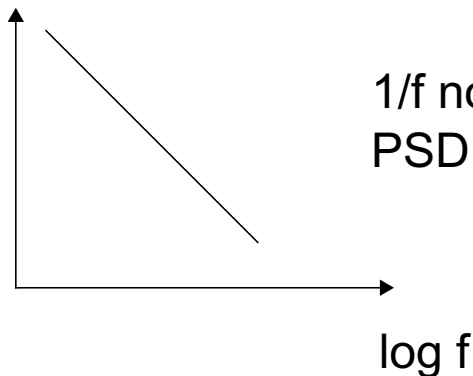
Repeat this for all frequencies to give the overall PSD $S_x(f)$

$S_x(f)$ often expressed in V^2/Hz
Also common to take the sq root and express in V/\sqrt{Hz}

10.3.1 Common Noise Spectra



White noise:
PSD is constant over all frequencies



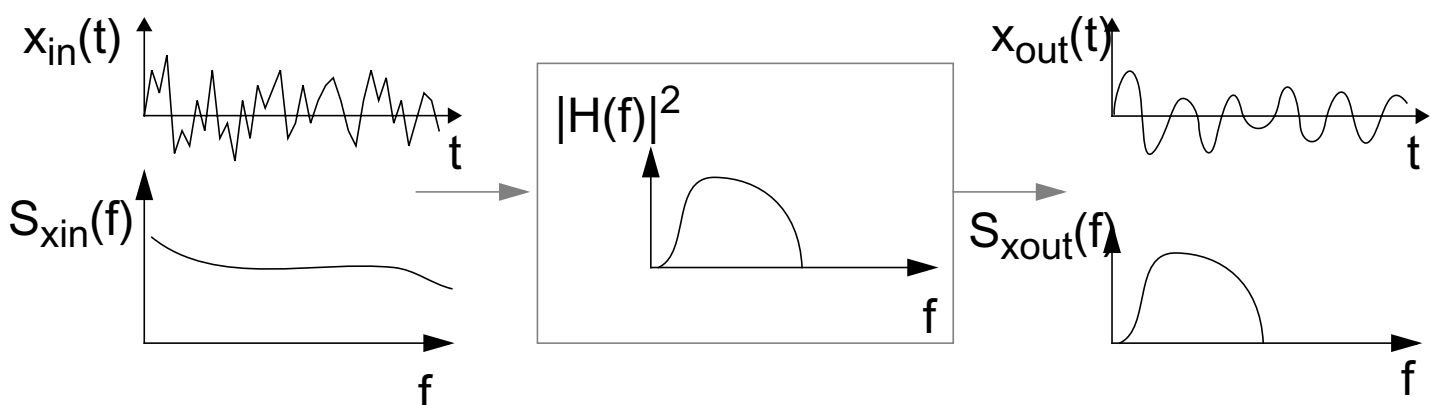
1/f noise (a.k.a. flicker noise)
PSD is inversely proportional to frequency

10.3.2 Spectrum Shaping

If a signal with spectrum $S_x(f)$ is applied to a system with transfer function $H(s)$ then the output spectrum $S_y(f)$ is given by

$$S_y(f) = S_x(f)|H(f)|^2$$

Example: noise spectrum input to an audio filter



Spectrum is shaped by bandwidth of filter

10.4 Amplitude distribution of noise

Cannot predict the instantaneous amplitude of noise

But can predict the distribution of the amplitude

Probability Density Function PDF of $x(t)$

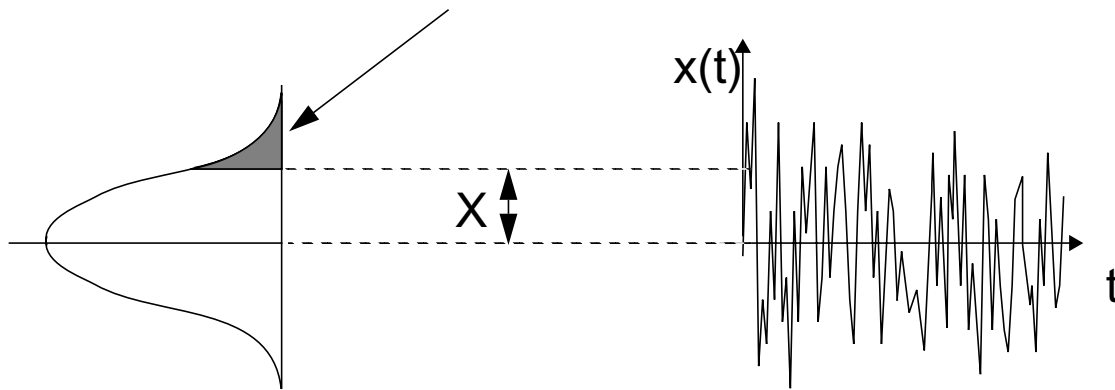
$p(x)dx$ = probability of $x < X < x+dx$

where X is the value of $x(t)$ measured at some point in time.

The PDF of many noise phenomena e.g. thermal noise have the Gaussian (normal) distribution

$$p_x(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-m)^2}{2\sigma^2}} \quad \begin{array}{l} s = \text{standard deviation} \\ m = \text{mean} \end{array}$$

Probability that instantaneous amplitude of $x(t)$ exceeds X .



For Gaussian noise rms value = standard deviation

Probability of instantaneous noise amplitude exceeding rms value is 32%.

Probability of instantaneous noise amplitude exceeding 3 x rms value = 0.3%.

Peak values of noise important in A/D converters, comparators.

10.5 Noise summation

In circuits each device is a source of noise.

To determine overall circuit noise need to sum the individual noise sources

Power of the sum of two noise sources $x_1(t)$ and $x_2(t)$ is given by

$$P_{av} = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} [x_1(t) + x_2(t)]^2 dt$$

$$P_{av} = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} x_1^2(t) dt + \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} x_2^2(t) dt + \lim_{T \rightarrow \infty} \frac{1}{T} 2 \int_{-\frac{T}{2}}^{\frac{T}{2}} x_1(t) x_2(t) dt$$

$$P_{av} = P_{av1} + P_{av2} + \lim_{T \rightarrow \infty} \frac{1}{T} 2 \int_{-\frac{T}{2}}^{\frac{T}{2}} x_1^2(t) x_2^2(t) dt$$

The third term depends on the correlation of the two signals $x_1(t)$ and $x_2(t)$ i.e. how similar they are.

In most circuits, each device generates noise independently, i.e. there is no correlation between the individual noise sources, so the product term is zero.

For these uncorrelated noise sources

$$P_{av} = P_{av1} + P_{av2}$$

or expressed as noise voltages:

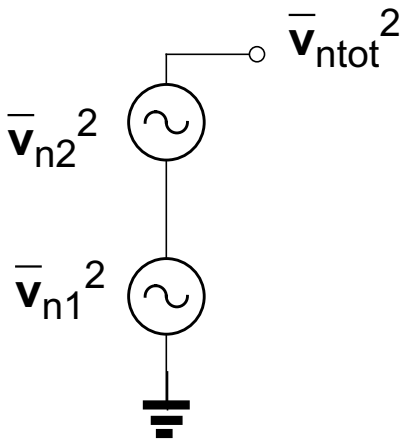
$$\overline{v_{ntot}^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2}$$

$$\overline{v_{ntot}} = \sqrt{\overline{v_{n1}^2} + \overline{v_{n2}^2}}$$

i.e. r.m.s. sum

10.5.1 Uncorrelated and dominant noise sources

For uncorrelated noise sources



$$\overline{v_{ntot}^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2}$$

$$\overline{v_{ntot}} = \sqrt{\overline{v_{n1}^2} + \overline{v_{n2}^2}}$$

i.e. r.m.s. sum

Example

$$\overline{v_{n1}} = 10\mu V$$

$$\overline{v_{n2}} = 5\mu V$$

1. What is the total rms value?

$$\overline{v_{ntot}} = \sqrt{10^2 + 5^2} = 11.2\mu V$$

2. How to keep the total value below $10\mu V$?

Either eliminate $\overline{v_{n2}}$

or reduce $\overline{v_{n1}}$ to

$$\overline{v_{n1}} = \sqrt{10^2 - 5^2} = 8.7\mu V$$

i.e. concentrate on the largest or **dominant** noise source

10.6 Types of Noise

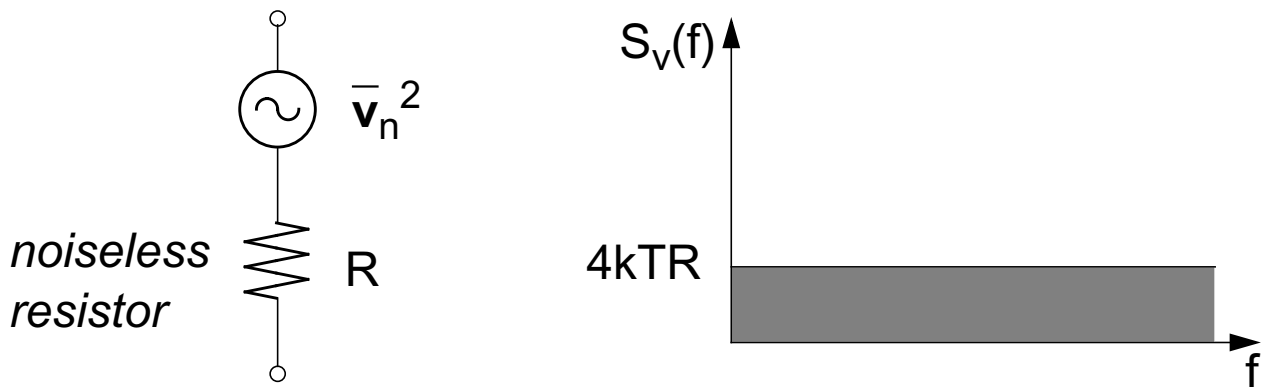
10.6.1 Thermal noise

Thermal noise is generated by the thermal excitation of charge carriers in a conductor.

The spectrum (PSD) of thermal noise is white and is proportional to absolute temperature.

10.6.2 Resistor thermal noise

Resistor noise can be modelled by a noiseless resistor in series with a noise voltage source



Noise spectral density (in V^2/Hz)

$$S_v(f) = 4kTR$$

or $\overline{v_n^2} = 4kTR$

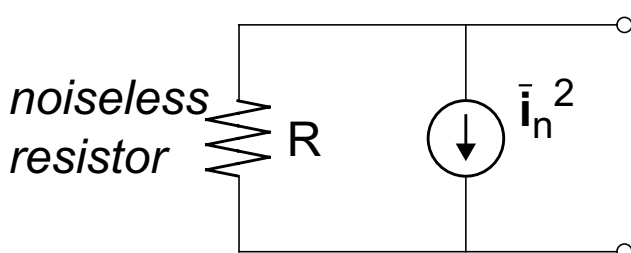
or $\overline{v_n} = \sqrt{4kTR} \quad V / \sqrt{Hz}$

$k = \text{Boltzmann constant} = 1.38 \times 10^{-23} \text{ J/K}$
 $T = \text{absolute temperature}$

$$1k\Omega \text{ resistor: } \overline{V_n} = 4nV/\sqrt{Hz} \text{ at } 300^\circ K$$

$$100k\Omega \text{ resistor: } \overline{V_n} = 40nV/\sqrt{Hz} \text{ at } 300^\circ K$$

Equivalently it can be modelled by a noise current source in parallel with the resistor:

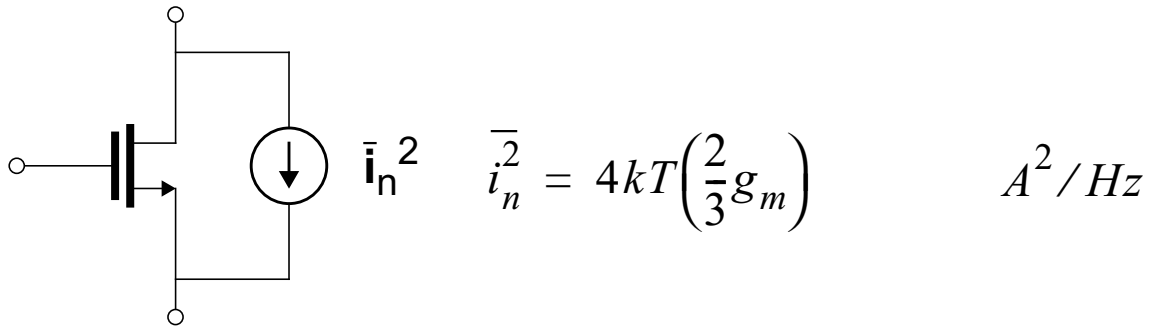


$$\overline{i_n^2} = \frac{4kT}{R} \quad A^2 / Hz$$

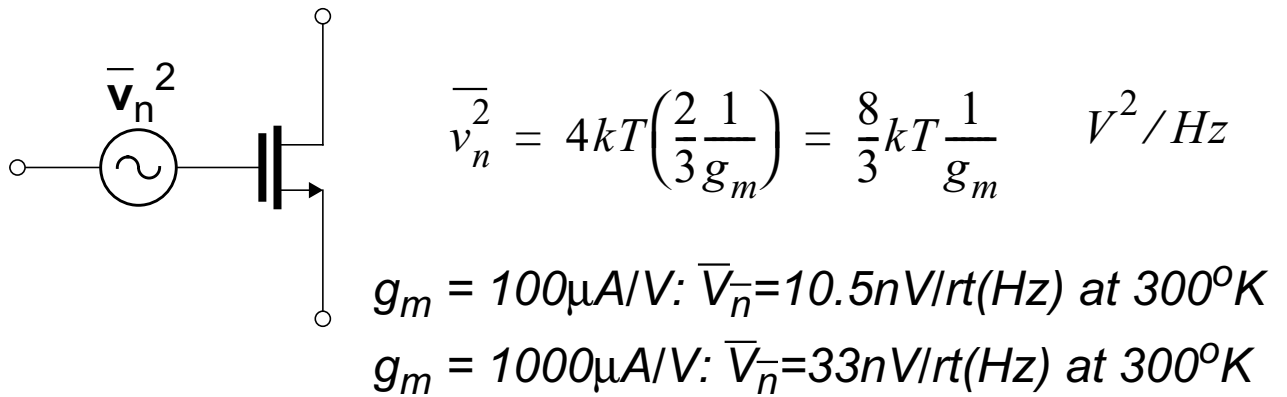
$$\overline{i_n} = \sqrt{\frac{4kT}{R}} \quad A / \sqrt{Hz}$$

10.6.3 MOSFET thermal noise

Thermal noise is generated in the channel of a MOS transistor
Can be modelled by a current source between drain and source



This noise current source at the output can be referred to the input as a noise voltage source (divide by g_m)

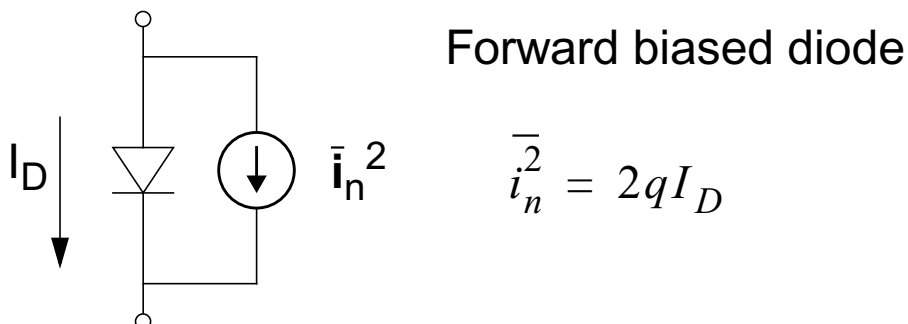


10.6.4 Shot noise

Occurs when dc current is not a continuous smooth flow of carriers, but is a result of pulses of current caused by the individual flow of carriers. Occurs whenever charge crosses a potential barrier e.g. in pn junctions

PSD of shot noise is white

10.6.5 Diode Shot noise



10.6.6 Flicker noise (1/f noise)

Is present in all active devices (and some passive ones).

In active devices is associated with traps which, when dc current flows capture and release charge carriers randomly causing random fluctuations in the current.

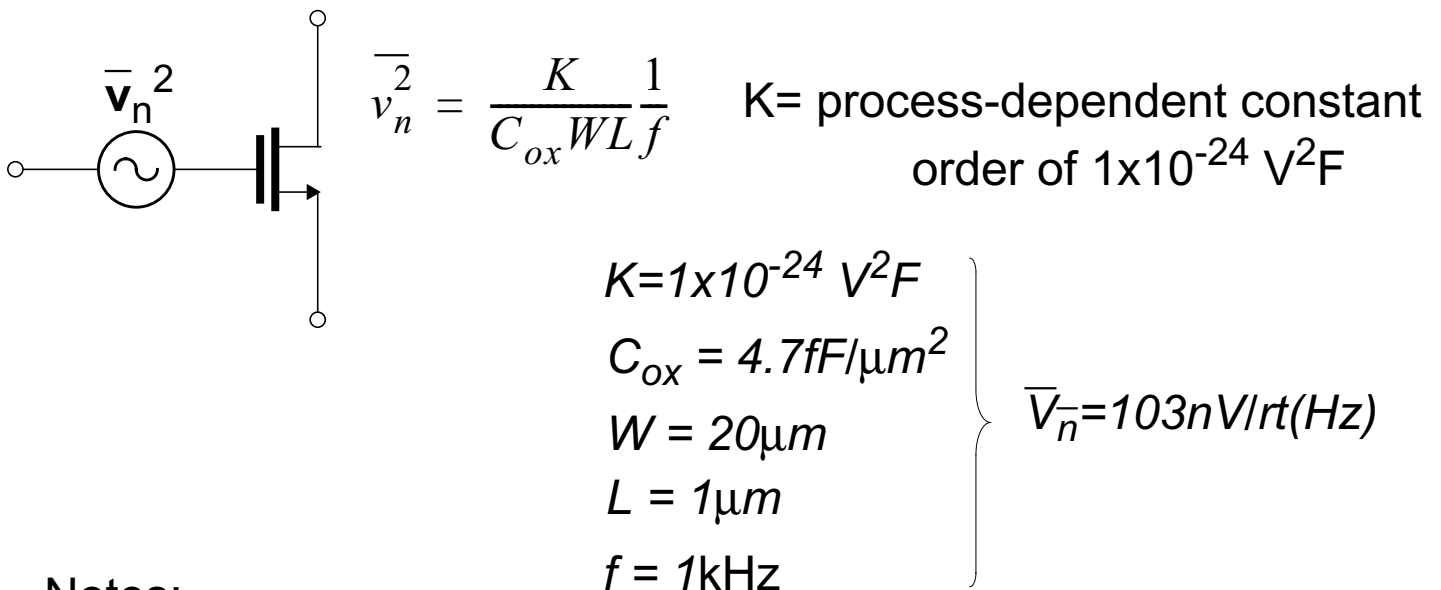
The PSD of flicker noise is inversely proportional to frequency, hence the alternative name 1/f noise

10.6.7 MOSFET-Flicker noise (1/f noise)

Due to interface states between Silicon surface and gate oxide which capture and release charge carriers randomly introducing noise in the drain current.

Very process-dependent.

Usually modelled by a noise voltage source in series with the gate



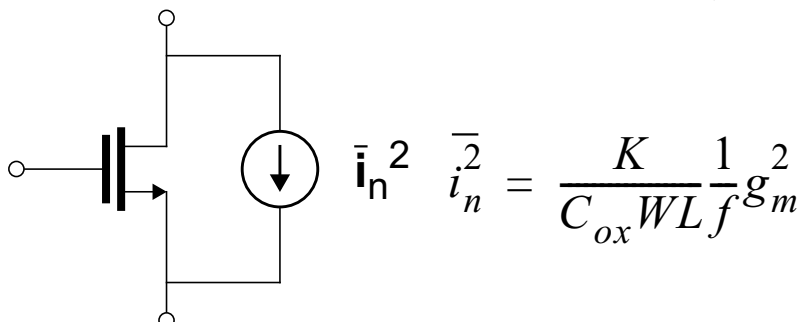
Notes:

Not dependent on bias current

Not dependent on temperature

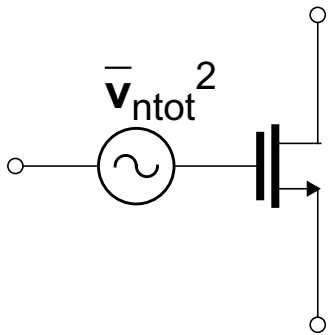
Inversely proportional to area of device

Can also be transferred to the output by multiplying by g_m^2



10.6.8 Corner frequency

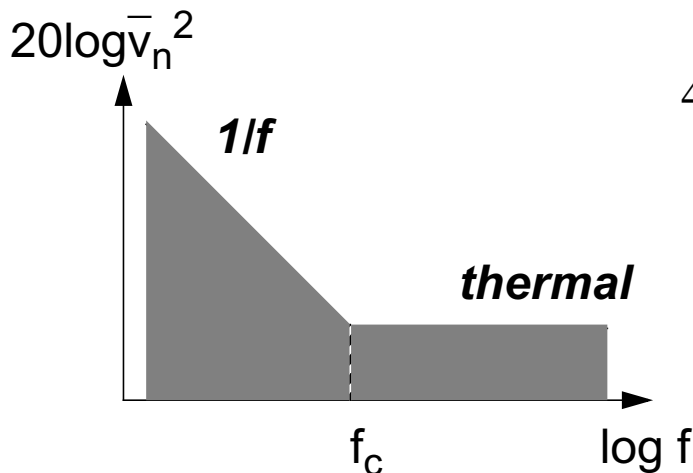
Noise in MOSFET consists of 2 components: $1/f$ and thermal



$$\overline{v_{ntot}^2} = \underbrace{\frac{K}{C_{ox}WL} \frac{1}{f}}_{1/f} + \underbrace{4kT \left(\frac{2}{3} \frac{1}{g_m} \right)}_{\text{thermal}}$$

At low frequencies $1/f$ noise is usually dominant, at high frequencies thermal noise is dominant

Frequency at which $1/f$ noise is equal to thermal noise is called the **corner frequency f_c**



thermal = $1/f$

$$4kT \left(\frac{2}{3} \frac{1}{g_m} \right) = \frac{K}{C_{ox}WL} \frac{1}{f}$$

$$f_c \equiv \frac{K}{C_{ox}WL} g_m \frac{3}{8kT}$$

often order 100kHz..1MHz

Corner frequency for case on previous page, $g_m = 100 \mu A/V$

$$4kT \left(\frac{2}{3} \frac{1}{g_m} \right) = \frac{K}{C_{ox}WL} \frac{1}{f_c} = (10.5 nV / \sqrt{Hz})^2$$

$$f_c = \frac{K}{C_{ox}WL (10.5 nV / \sqrt{Hz})^2} = 97 kHz$$

Note: Total noise at 97kHz = : 14.8 nV/rt(Hz)

10.7 Noise Bandwidth

Noise is present at all frequencies.

The thermal noise generated by devices for example has equal power at all frequencies

=> unbounded noise energy => infinite noise?

Noise is however filtered in the same way as a signal

Each node in a circuit has a pole associated with it.

In other words each node has a certain bandwidth.

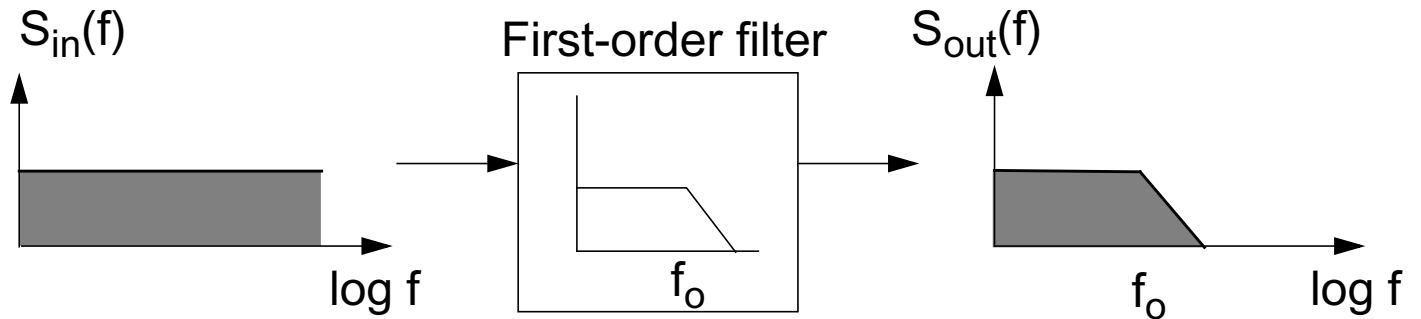
Noise at frequencies above this bandwidth is attenuated, i.e. filtered

This limits the noise and enables us to maintain a SNR

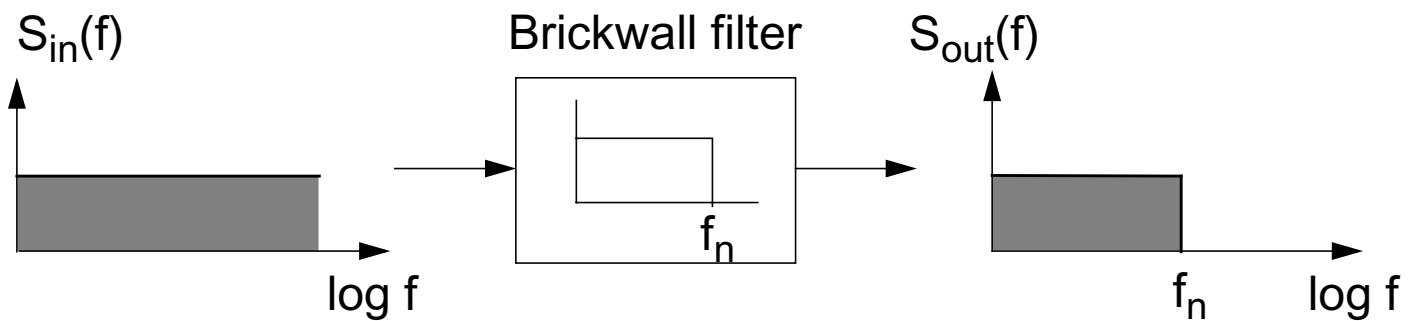
The noise bandwidth of a given filter or node is defined as the bandwidth of a brickwall filter (with the same passband gain) that would give the same output noise when white noise is applied to both filters

10.7.1 Noise bandwidth of a first-order filter

White noise spectrum filtered by a first-order filter with pole frequency f_o

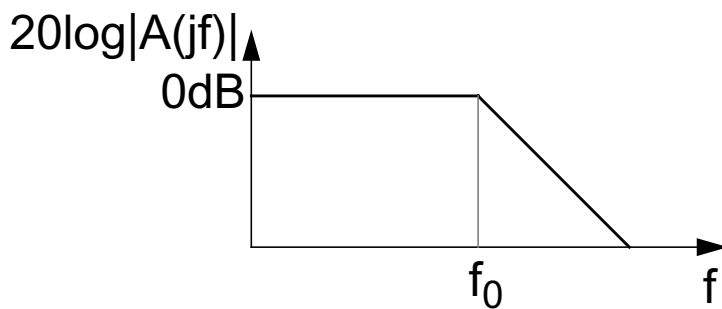


The noise bandwidth f_n is the cut-off frequency of a brickwall filter which gives the same total integrated noise as the first-order filter i.e. for which the area under the two curves is the same



Noise bandwidth of a first-order filter

Example: First-order filter with 3dB bandwidth of f_o



$$A(s) = \frac{1}{1 + \frac{s}{2\pi f_o}}$$

$$|A(jf)| = \sqrt{\frac{1}{1 + \left(\frac{f}{f_o}\right)^2}}$$

If the input to the first-order filter $v_{ni}(f)$ is a white noise source given by

$$S_i(f) = v_{ni}^2(f) = v_{nw}^2 \text{ i.e. constant over frequency}$$

Output noise spectrum is given by

$$S_o(f) = S_i(f)|A(jf)|^2$$

Total output noise from filter over all frequencies is given by

$$v_{no}^2 = \int_0^\infty \frac{v_{nw}^2}{1 + \left(\frac{f}{f_o}\right)^2} df$$

$$v_{no}^2 = v_{nw}^2 \int_0^\infty \frac{1}{1 + \frac{f^2}{f_o^2}} df$$

$$v_{no}^2 = v_{nw}^2 \left. \text{atan} \frac{f}{f_o} \right|_0^\infty$$

$$v_{no}^2 = \frac{v_{nw}^2 \pi f_o}{2}$$

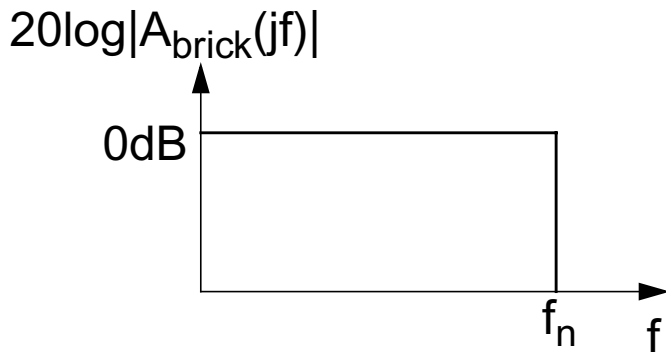
N.B.

$$\int \frac{1}{1 + a^2 x^2} dx = \frac{1}{a} \text{atan} ax$$

$$\int_0^\infty \frac{1}{1 + a^2 x^2} dx = \frac{1}{a} \text{atan} ax \Big|_0^\infty = \frac{\pi}{2a}$$

Noise bandwidth of a first-order filter (contd.)

Compare with a brick wall filter:



Total output noise from brick wall filter:

$$v_{n\text{obrick}}^2 = \int_0^{f_n} v_{nw}^2 df = v_{nw}^2 f_n$$

Equating the 2 equations gives

$$v_{no}^2 = v_{n\text{obrick}}^2$$

$$\frac{v_{nw}^2 \pi f_o}{2} = v_{nw}^2 f_n$$

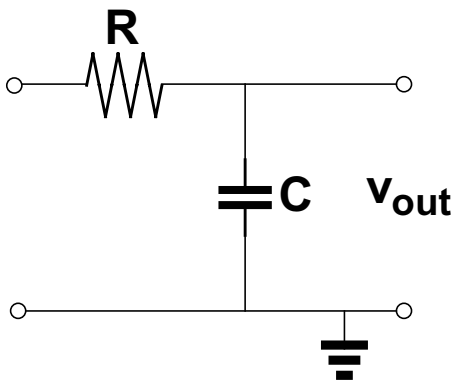
$$f_n = \frac{\pi}{2} f_o$$

i.e Noise bandwidth of a first-order filter with a -3 dB bandwidth of f_o equals $(\pi/2)f_o$.

If you integrate all the noise power at the output of the first-order filter it is the same as multiplying the noise power by $(\pi/2)f_o$

Example: Noise bandwidth of a first-order filter.

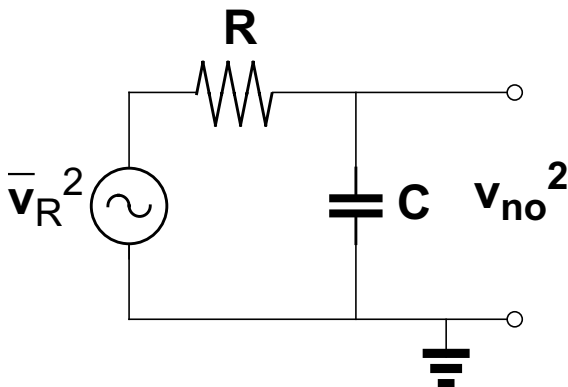
What is the noise voltage at the output of the following circuit?



The resistor R generates a noise voltage $v_r^2 = 4kTR$

The noise from the resistor is filtered by the pole formed by R,C

$$\text{Pole frequency: } f_o = \frac{1}{2\pi RC}$$

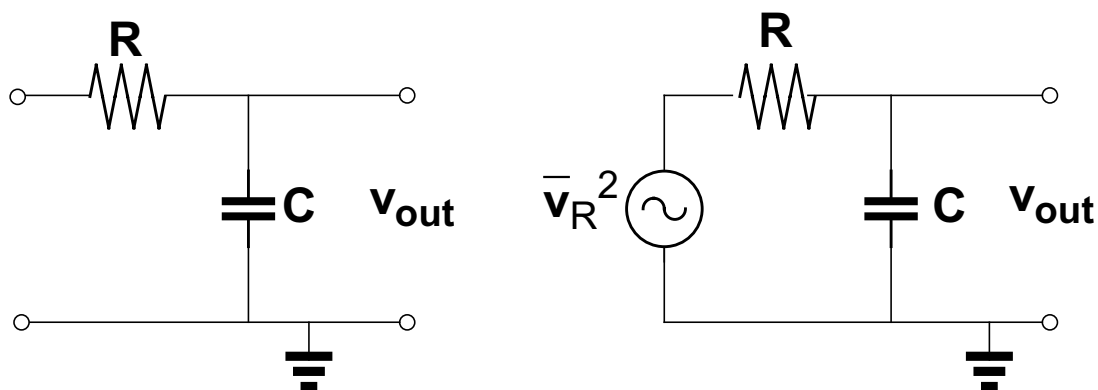


Total output noise power:

$$v_{no}^2 = v_r^2 \cdot \frac{\pi}{2} \cdot f_o = 4kTR \cdot \frac{\pi}{2} \cdot \frac{1}{2\pi RC} = \frac{kT}{C}$$

Total output noise power is independent of value of R

Equivalent derivation



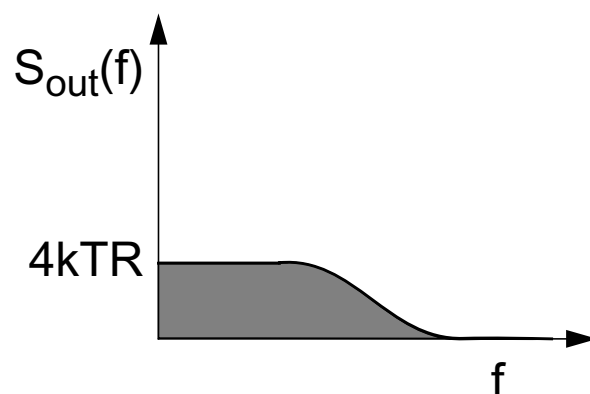
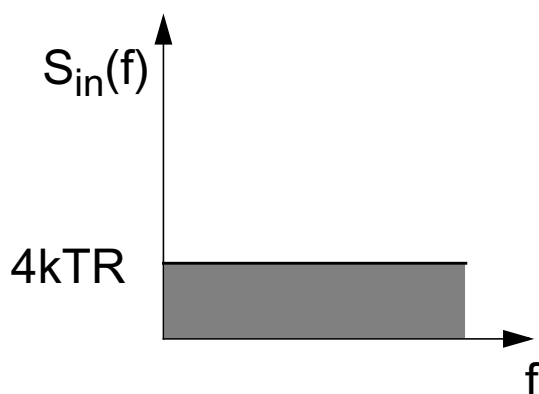
$$\frac{v_{out}}{v_R}(s) = \frac{1}{1 + sRC}$$

$$S_{out}(f) = S_R(f) \left| \frac{v_{out}}{v_R}(j\omega) \right|^2$$

$$= 4kTR \left| \frac{1}{(2\pi fRC)^2 + 1} \right|^2$$

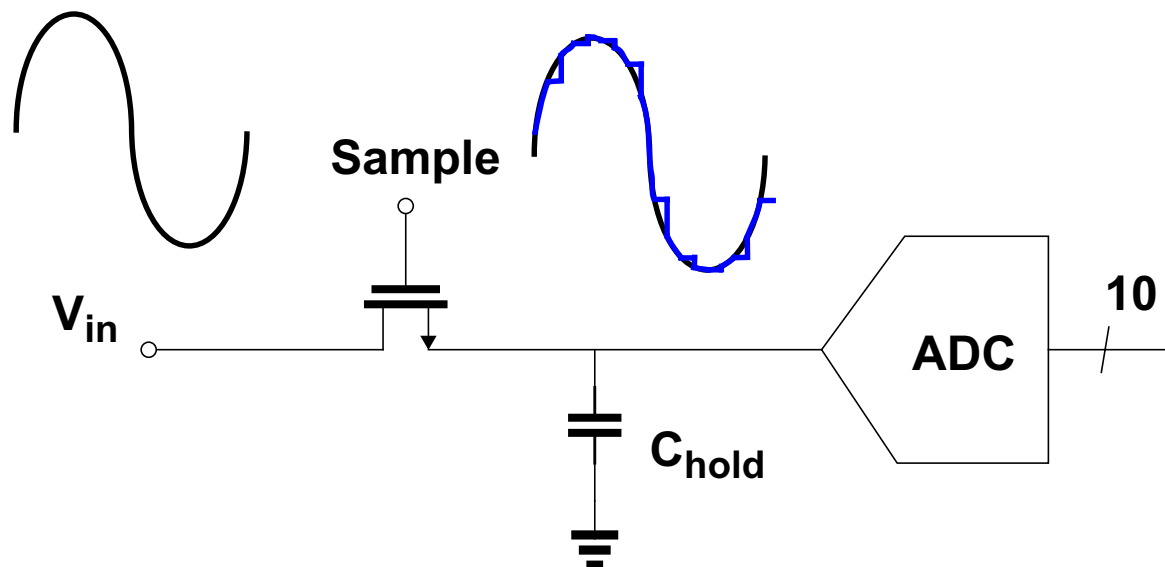
$$P_n = \int_0^\infty \frac{4kTR}{(2\pi fRC)^2 + 1} df$$

$$P_n = \frac{4kTR}{2\pi fRC} \operatorname{atan} 2\pi fRC \Big|_0^{\frac{\pi}{2}} = \frac{kT}{C}$$



Example: Sample and Hold circuit

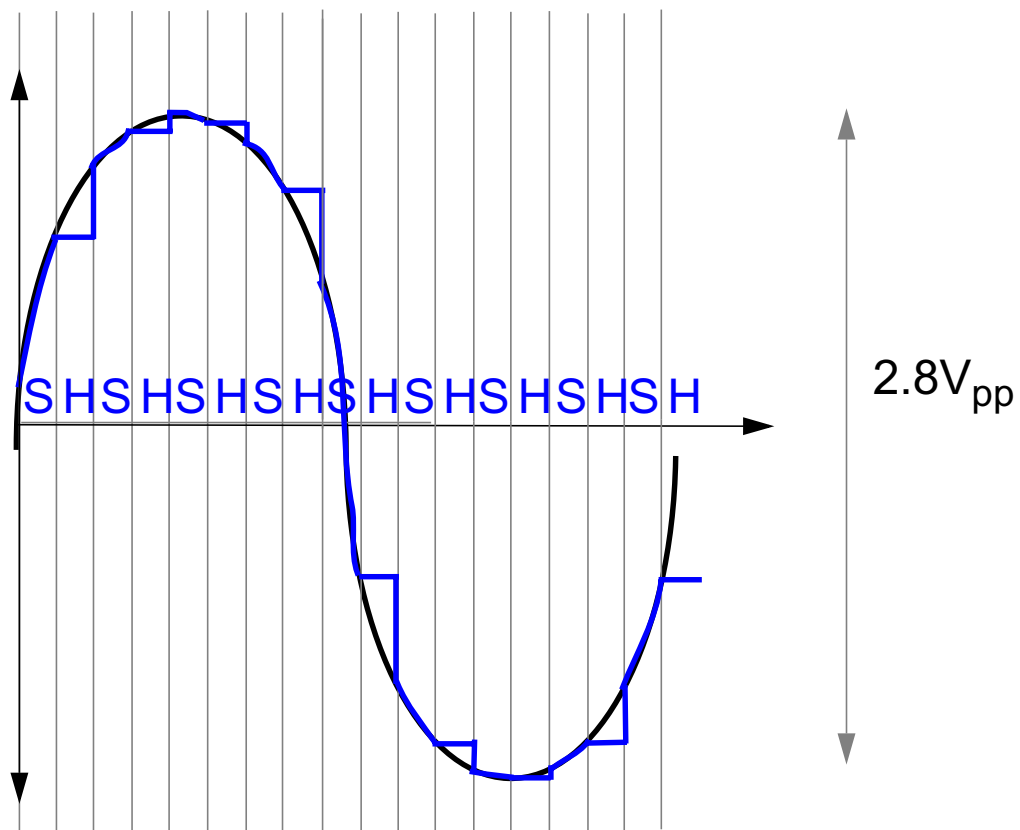
A 10-bit A/D converter with 1V_{rms} input range is preceded by a Sample-and-Hold circuit. What is the minimum required value of the hold capacitor if the noise error budget for the sample-and-hold circuit is 0.1 LSB



An A/D converter usually has a Sample-and-Hold (S/H) circuit at its input to keep the value of the signal being converted constant while the conversion is taking place. This enables the ADC reach higher signal and sampling frequencies.

A simple implementation is a MOS sampling switch and a hold capacitor.

The switch has a certain on resistance which generates noise. This noise is sampled on the capacitor along with the signal.



The switch has a certain on-resistance which generates noise. At the moment the switch is closed this noise is sampled on the capacitor along with the signal, and then converted by the ADC. So this noise is one of the limit to the ADC SNR

10-bit ADC full-scale input range = $1V_{rms}$

ADC LSB = $1V/2^{10} = 1mV$

During the sampling phase the sample-and-hold circuit is a first-order circuit => noise is

$$v_n^2 = \frac{kT}{C}$$

For error budget want $\bar{v}_n < \text{LSB}/10 = 0.1mV$

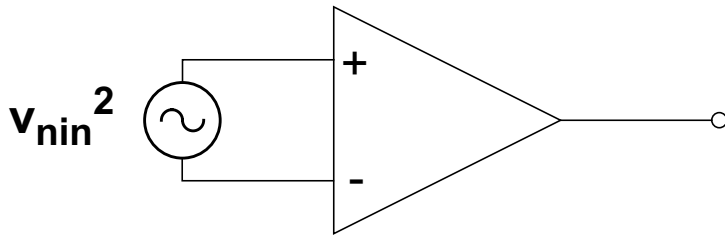
$$\sqrt{\frac{kT}{C}} < 0.1mV \Rightarrow C > \frac{kT}{(0.1mV)^2} \Rightarrow C > \frac{1.38 \times 10^{-23} \times 300}{(0.1mV)^2} = 0.4pF$$

10.8 Input-referred noise

It is usual in the case of voltage amplifiers to refer all noise sources to the input of the amplifier, and quote the 'input-referred noise' of the amplifier.

This allows for easier comparison of noise performance.

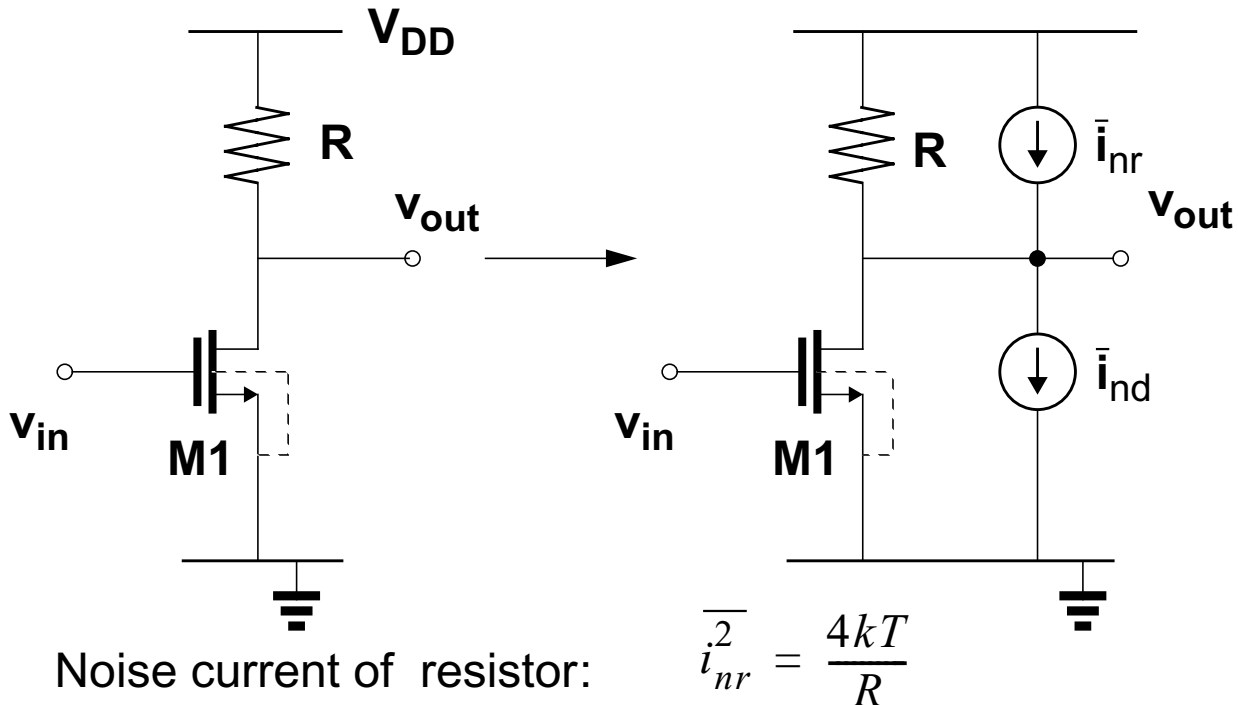
To input-refer a noise source: divide the source by the gain from the input to the source.



10.9 Circuit noise analysis examples

Example: CS stage with resistive load, noise analysis

What is the input-referred thermal noise voltage density of the circuit shown?



Noise current of MOS: $\overline{i_{nd}^2} = 4kT\left(\frac{2}{3}g_m\right)$

Noise sources uncorrelated => total noise is the sum of squares

$$\overline{i_{nt}^2} = \overline{i_{nr}^2} + \overline{i_{nd}^2} \quad \text{or} \quad \overline{i_{nt}} = \sqrt{\overline{i_{nr}^2} + \overline{i_{nd}^2}} \quad \text{rms value}$$

To get input-referred noise divide current noise at output by g_m

$$\overline{v_{nin}} = \frac{\overline{i_{nt}}}{g_m} = \frac{\sqrt{\frac{4kT}{R} + 4kT\left(\frac{2}{3}g_m\right)}}{g_m} \quad \text{rms noise} \quad V/\sqrt{Hz}$$

What is the thermal noise voltage density at the output of the circuit?

Two possible approaches:

1. Multiply input-referred noise voltage by the small-signal voltage gain

$$\begin{aligned}\overline{v_{nout}} &= \overline{v_{nin}} \cdot \frac{g_m}{R + \frac{1}{g_{ds}}} \approx \overline{v_{nin}} \cdot g_m R = \frac{\sqrt{\frac{4kT}{R} + 4kT\left(\frac{2}{3}g_m\right)}}{g_m} \cdot g_m R \\ &= \sqrt{\frac{4kT}{R} + 4kT\left(\frac{2}{3}g_m\right)} \cdot R \quad V / \sqrt{Hz}\end{aligned}$$

2. Divide output noise current by the small-signal conductance at the output

$$\overline{v_{nout}} = \frac{\overline{i_{nt}}}{g_{ds} + \frac{1}{R}} \approx \overline{i_{nt}} \cdot R = \sqrt{\frac{4kT}{R} + 4kT\left(\frac{2}{3}g_m\right)} \cdot R \quad V / \sqrt{Hz}$$

What is the SNR at the output if the signal is a 100mVrms sine wave and the noise is measured over a bandwidth of 1MHz?

Use $R=10k\Omega$, $W/L=16/1$, $K_n'=200\mu A/V^2$, $I_{D1}=100\mu A$

Take Boltzmann's constant $k=1.38 \times 10^{-23} J/^{\circ}K$, temperature $T=300^{\circ}K$. Consider only thermal noise.

Total noise over bandwidth Δf given by

$$\overline{v_{nout\Delta f}} = \sqrt{\frac{4kT}{R} + 4kT\left(\frac{2}{3}g_m\right)} \cdot R \cdot \sqrt{\Delta f}$$

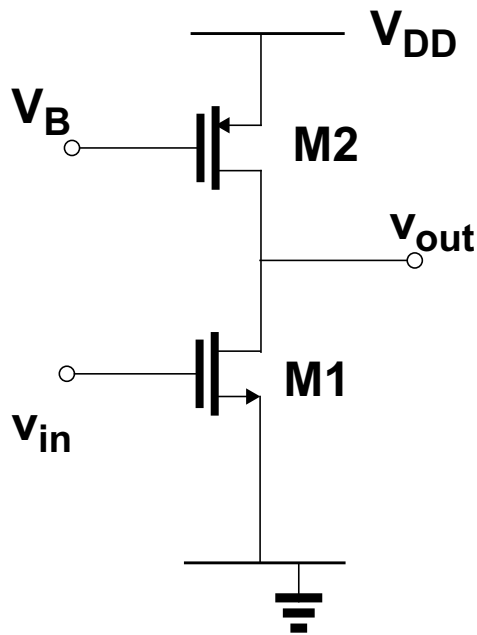
$$SNR_{out} = \frac{100mV}{\sqrt{\frac{4kT}{R} + 4kT\left(\frac{2}{3}g_m\right)} \cdot R \cdot \sqrt{\Delta f}}$$

$$g_{m1} = \sqrt{2K_n'\left(\frac{W}{L}\right)_1 I_{D1}} = \sqrt{2 \times 200\mu A/V \times \frac{16}{1} \times 100\mu A} = 800\mu A/V$$

$$SNR_{out} = \frac{100mV}{\sqrt{1.66 \times 10^{-24} + 8.84 \times 10^{-24}} \cdot 10k \cdot \sqrt{1M}}$$

$$SNR_{out} = 3068 = 70dB$$

Example: CS stage with active load, noise analysis

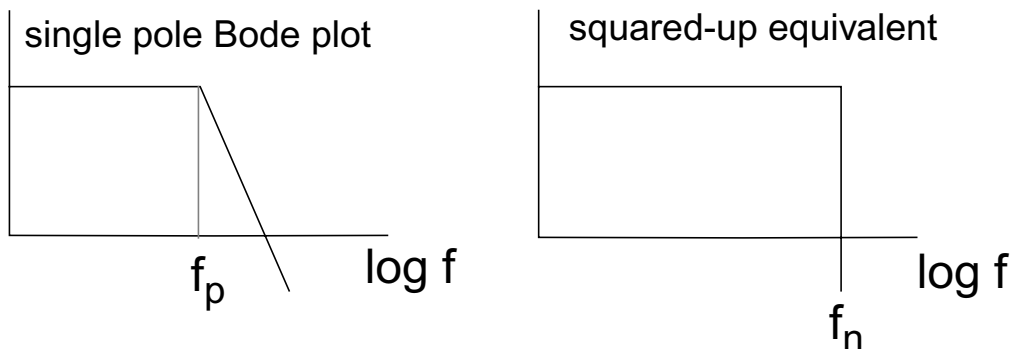


Assume all devices are biased in saturation.

Consider only thermal noise.

- (i) What is the input-referred thermal noise of the circuit shown?
- (ii) If the output drives a load capacitance C_L calculate the total output thermal noise?

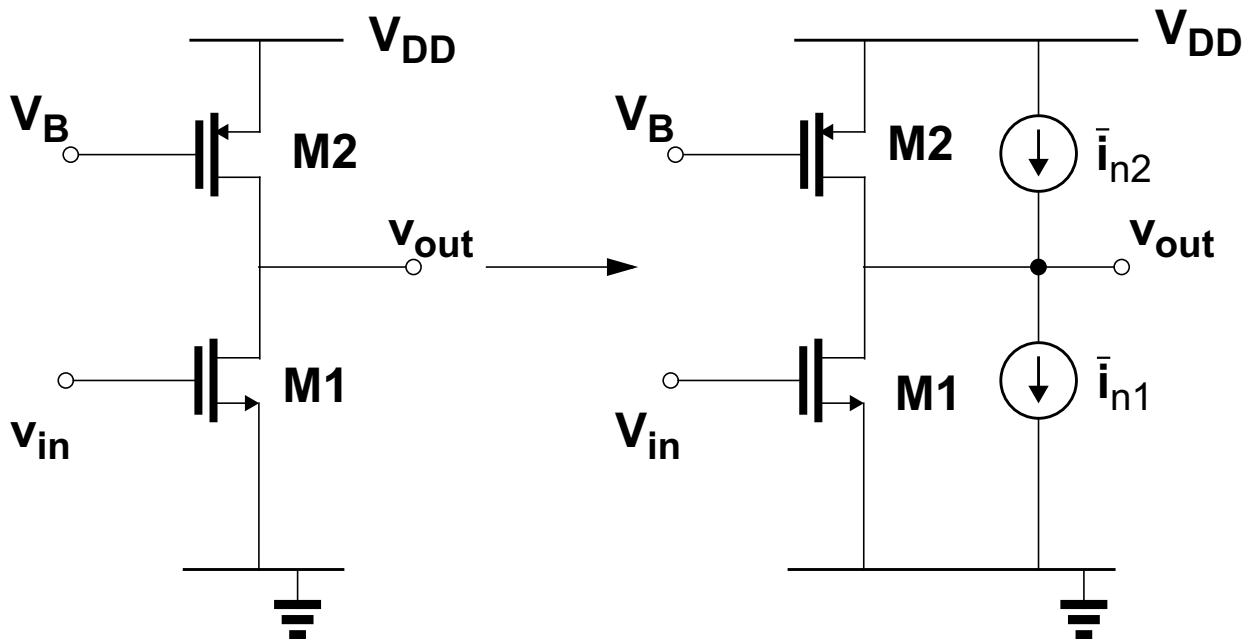
You may assume the following:



For the area underneath the curves to be the same then $f_n = (\pi/2) * f_p$

- (iii) What is the signal-to-noise ratio at the output if the input signal v_{in} is a low-frequency (i.e much lower than the pole frequency) sine-wave with amplitude V_m . Consider only thermal noise.

Solution (i)



Noise current of MOS: $\bar{i}_n^2 = 4kT\left(\frac{2}{3}g_m\right)$

Noise sources uncorrelated \Rightarrow total noise is the sum of squares

$$\bar{i}_{nt}^2 = i_{n1}^2 + i_{n2}^2 \quad \text{or} \quad \bar{i}_{nt} = \sqrt{i_{n1}^2 + i_{n2}^2} \quad \text{rms value}$$

$$\bar{v}_{ni} = \frac{\bar{i}_{nt}}{g_{m1}} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}}{g_{m1}} \quad \text{rms noise } V/\sqrt{Hz}$$

$$\bar{v}_{ni} = \frac{\bar{i}_{nt}}{g_{m1}} = \sqrt{4kT \cdot \frac{2}{3} \left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2} \right)}$$

\Rightarrow for low noise need to minimise g_{m2}

Solution (ii)

To get voltage noise at output multiply input-referred noise by the small-signal voltage gain of circuit

$$\overline{v_{no}} = \overline{v_{ni}} \frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

$$\overline{v_{no}} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}}{g_{ds1} + g_{ds2}}$$

To get total noise voltage at output need to integrate this over all frequencies

The circuit is first-order circuit with a pole at

$$\omega_o = -\frac{g_{ds1} + g_{ds2}}{C_L}$$

$$\overline{v_{nototal}^2} = \int_0^\infty \left(\frac{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}{(g_{ds1} + g_{ds2})^2} \cdot \frac{1}{1 + \frac{C_L^2}{(g_{ds1} + g_{ds2})^2} \cdot (2\pi f)^2} \right) df$$

This is equal to multiplying by the noise bandwidth

$$v_{nototal}^2 = v_{no}^2 \cdot \frac{\pi}{2} \cdot f_o = \left(\frac{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}{(g_{ds1} + g_{ds2})^2} \right) \cdot \frac{\pi}{2} \cdot \left(\frac{g_{ds1} + g_{ds2}}{2\pi C_L} \right)$$

$$= \left(\frac{\frac{2}{3}(g_{m1} + g_{m2})}{g_{ds1} + g_{ds2}} \cdot \frac{kT}{C_L} \right)$$

Solution (iii)

$$SNR = 10 \log \left[\frac{\text{signal power}}{\text{noise power}} \right] = 10 \log \left[\frac{V_{rms}^2}{V_{nrms}^2} \right]$$

Input signal is a sine-wave of amplitude V_m

rms value is $\left(\frac{V_m}{\sqrt{2}} \right)$

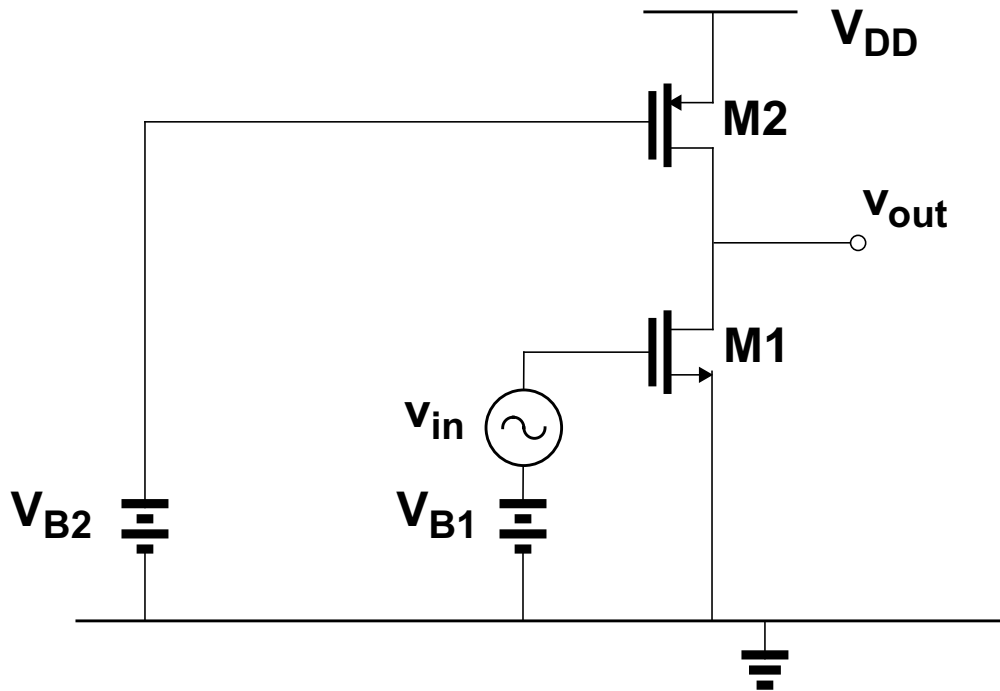
$$SNR_{out} = \frac{\left(\frac{V_m}{\sqrt{2}} \right)^2 \left(\frac{g_{m1}}{g_{ds1} + g_{ds2}} \right)^2}{\frac{\frac{2}{3}(g_{m1} + g_{m2})}{g_{ds1} + g_{ds2}} \cdot \frac{kT}{C_L}}$$

$$SNR_{out} = \frac{3C_L}{4kT} \cdot \frac{g_{m1}^2}{(g_{m1} + g_{m2})(g_{ds1} + g_{ds2})} V_m^2$$

=> to maximise SNR increase C_L , i.e. reduce bandwidth

But input signal spectrum determines the required bandwidth

Problem: CS with active load noise analysis



Assume M1 and M2 are operating in saturation. Only thermal noise sources need be considered.

For calculations take Boltzmann's constant $k=1.38 \times 10^{-23} \text{ J/}^\circ\text{K}$, temperature $T=300^\circ\text{K}$.

(i) Draw the small-signal model for the circuit shown.

What is the low-frequency small-signal voltage gain ($v_{\text{out}}/v_{\text{in}}$) in terms of the small-signal parameters of M1 and M2?

(ii) What is the input-referred thermal noise voltage density of M1?

What is the input-referred thermal noise voltage density of M2?

Answers should be in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T .

(iii) Calculate the input-referred thermal noise voltage density of M1

and the input-referred thermal noise voltage density of M2 if

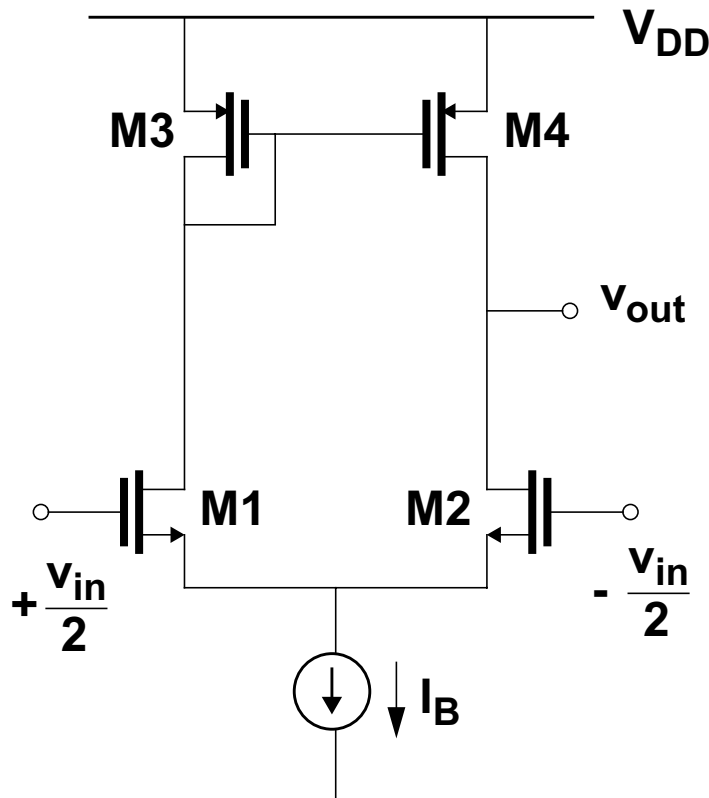
$V_{B1}=1.0\text{V}$, $V_{B2}=1.25\text{V}$, $V_{DD}=3\text{V}$, $V_{tn} = 0.75\text{V}$, $V_{tp} = -0.75\text{V}$,

$\lambda_n=\lambda_p=0.04\text{V}^{-1}$. The drain current of M1 is $100\mu\text{A}$.

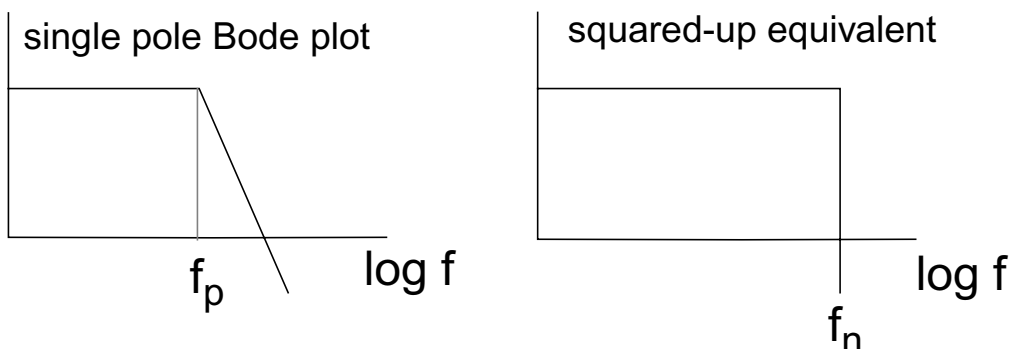
Which is the dominant noise source?

(iv) Calculate the total noise voltage at the output over a bandwidth of 1MHz. If the input signal v_{in} is a 1mV_{rms} sine wave, calculate the signal-to-noise ratio in dB at the output over a bandwidth of 1MHz.

Problem: Differential pair noise analysis



- (i) What is the input-referred thermal noise voltage density of the circuit shown, in terms of the small signal parameters g_m and g_{ds} ?
 - (ii) Calculate the total noise voltage at the output over a bandwidth of 20kHz. Use $g_{mn}=g_{mp}=100\mu\text{A/V}$, $g_{dsn}=g_{dsp}=2\mu\text{A/V}$
 - (iii) Calculate the total noise voltage at the output if the output is loaded by a capacitor $C_L=1\text{pF}$
- You may assume the following:

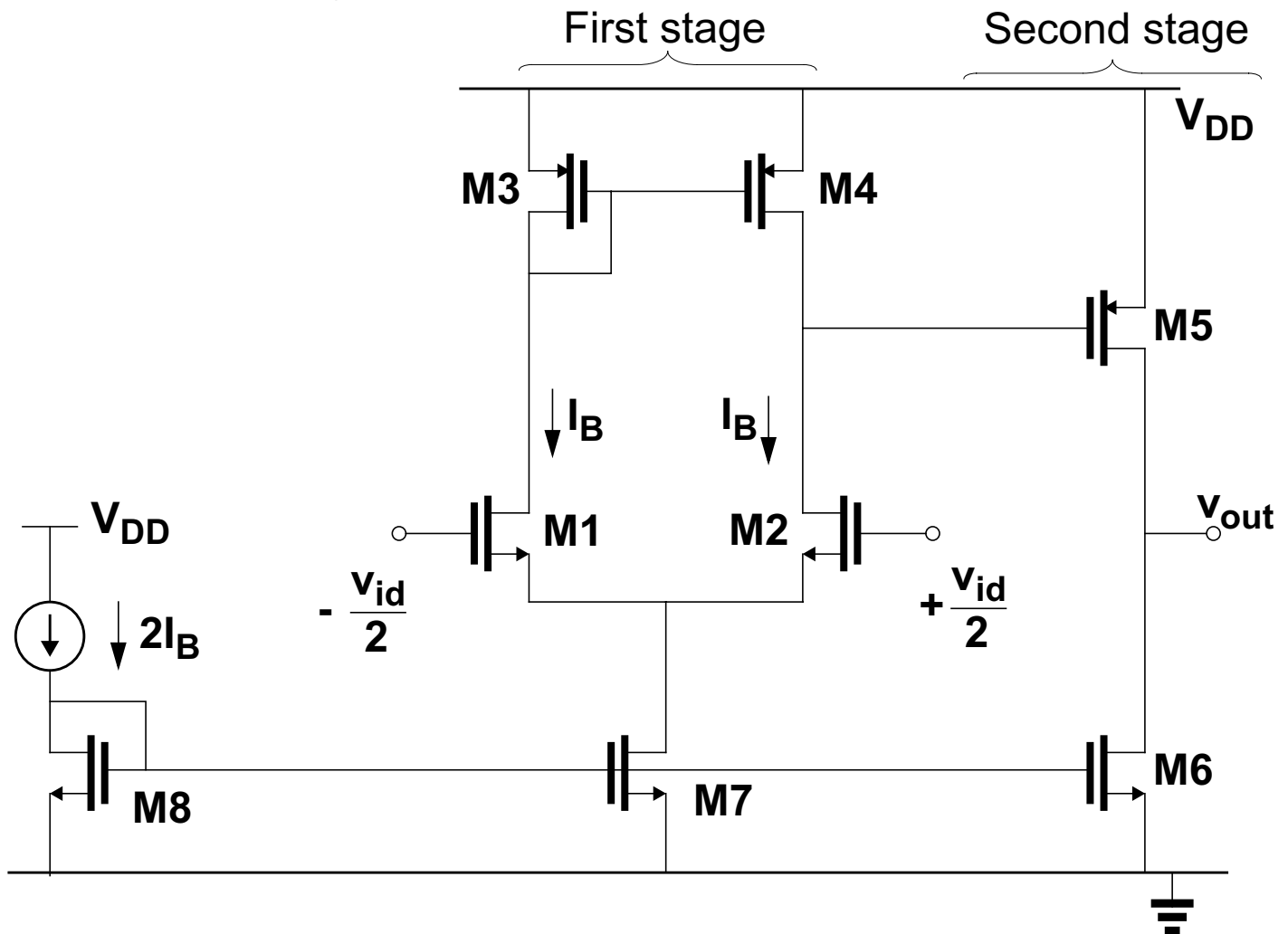


For the area underneath the curves to be the same then $f_n=(\pi/2)*f_p$

- (iv) What is the SNR at the output if the input to the circuit is a differential sine wave of 10mVrms? Assume the frequency of the sine-wave is much less than the pole frequency.

10.10 Opamp gain stage noise

10.10.1 Two-stage opamp



1. Contribution of second stage

The output stage transistors M5 and M6 generate current noise in the output stage. To refer this to the input:

- divide by g_{m5} to refer the noise back to a voltage noise at the output of the first stage.
- Then divide by the voltage gain of the first stage to refer back to the opamp input.

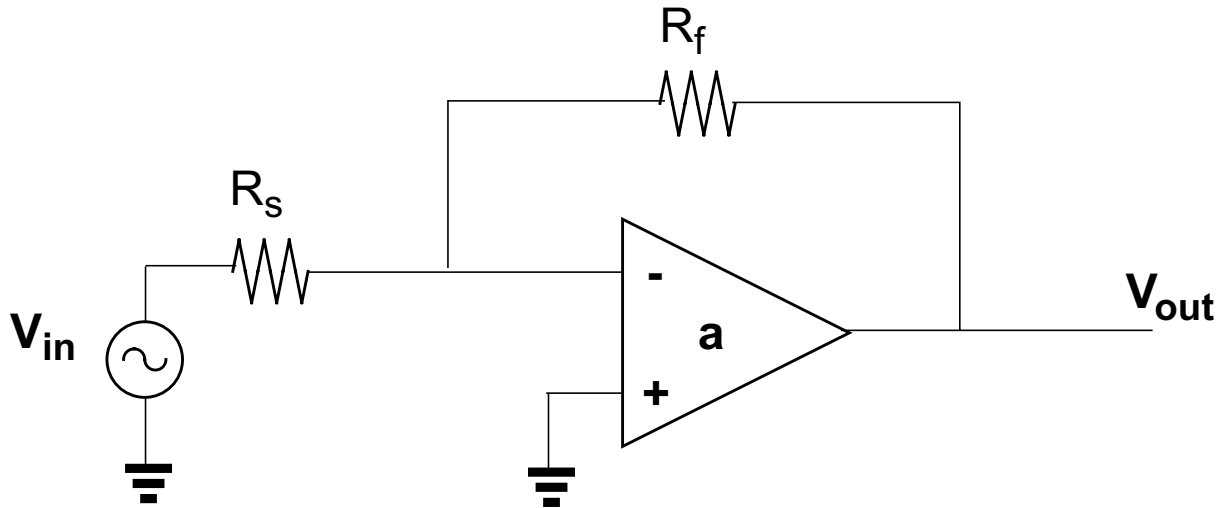
So the noise of M5 and M6 is usually negligible compared to the noise of M1, M2, M3 and M4.

2. Contribution of M8 and M7

The noise of M8 and M7 adds to the tail current, splits between M1 and M2, and approximately cancels at the output node (correlated noise, at least in the quiescent case and with good matching).

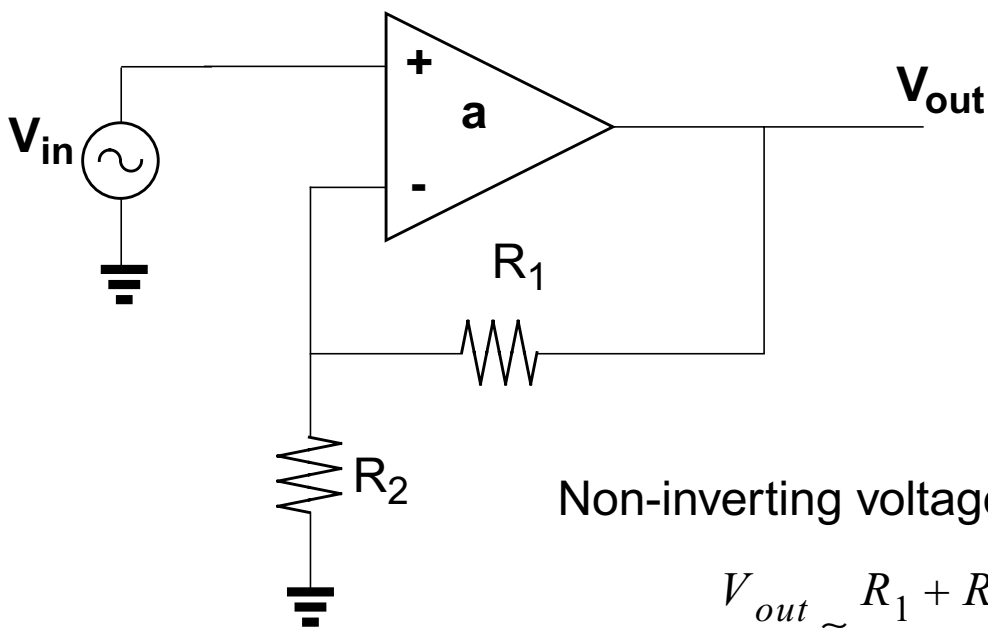
So this can usually be ignored.

10.10.2 Input-referred noise of opamp gain stages



Inverting voltage amplifier (for large opamp gain):

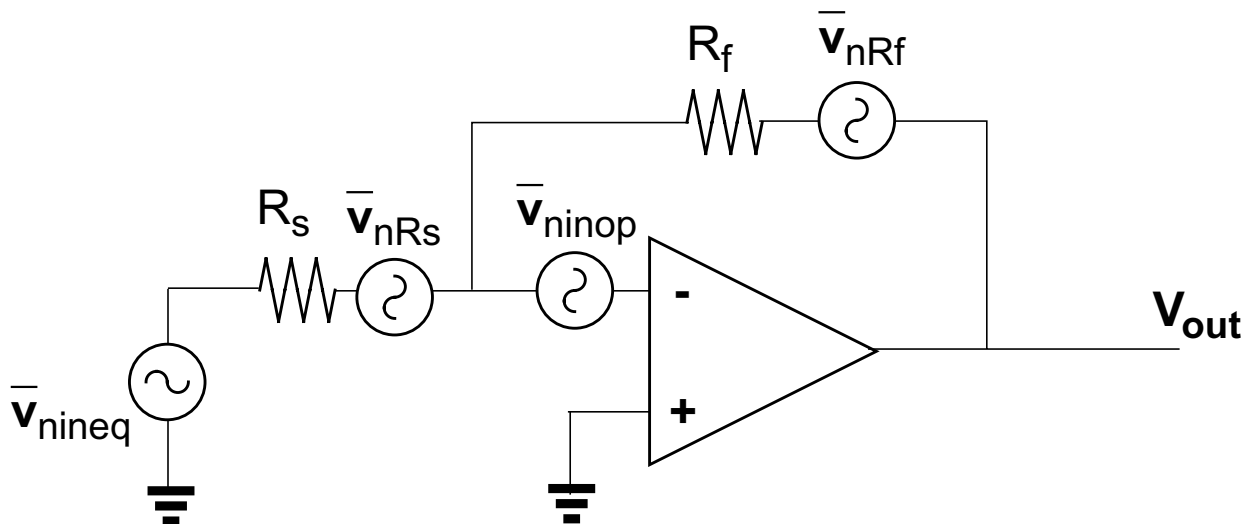
$$\frac{V_{out}}{V_{in}} \cong -\frac{R_{fb}}{R_s}$$



Non-inverting voltage amplifier:

$$\frac{V_{out}}{V_{in}} \cong \frac{R_1 + R_2}{R_2} = 1 + \frac{R_1}{R_2}$$

Inverting amplifier noise sources and input-referred noise:



\bar{v}_{ninop} is the input-referred voltage noise of the opamp

\bar{v}_{nRs} is the voltage noise of R_s $\overline{v_{nRs}} = \sqrt{4kTR_s}$

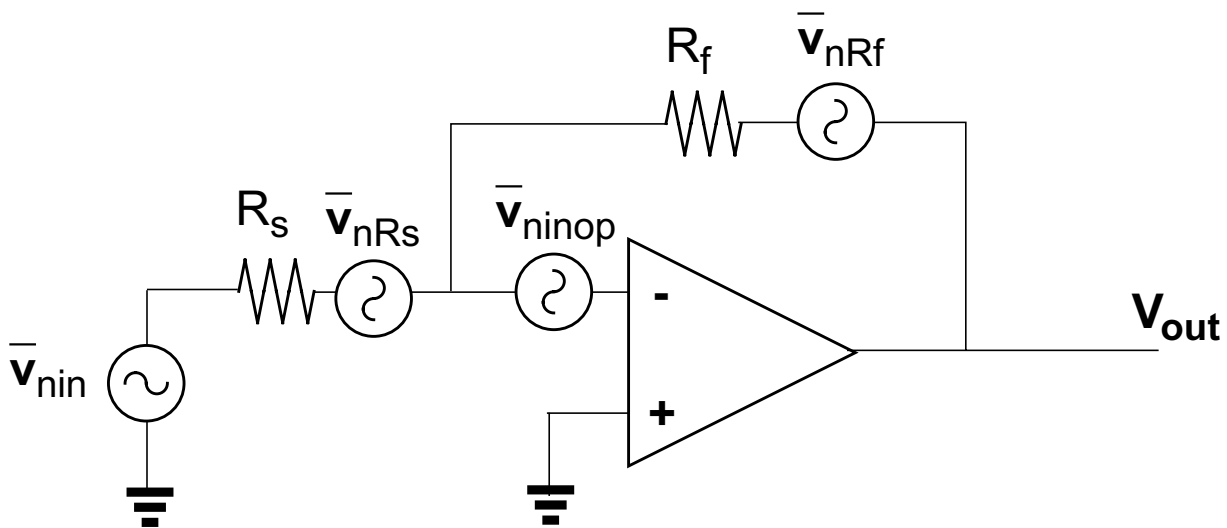
\bar{v}_{nRf} is the voltage noise of R_f $\overline{v_{nRf}} = \sqrt{4kTR_f}$

These each contribute to the total equivalent input-referred noise of the stage, $\bar{v}_{n_{ineq}}$

To calculate this consider

1. The noise of R_f appears at the output and can be referred to the input by dividing by the closed-loop gain R_f/R_s
2. The noise of R_s appears at the input of the stage
3. The input-referred opamp noise is gained up to the output by the gain of a non-inverting gain stage $1+R_f/R_s$, and then referred back to the input by dividing by the closed loop gain R_f/R_s

These noise sources are uncorrelated, so rms sum

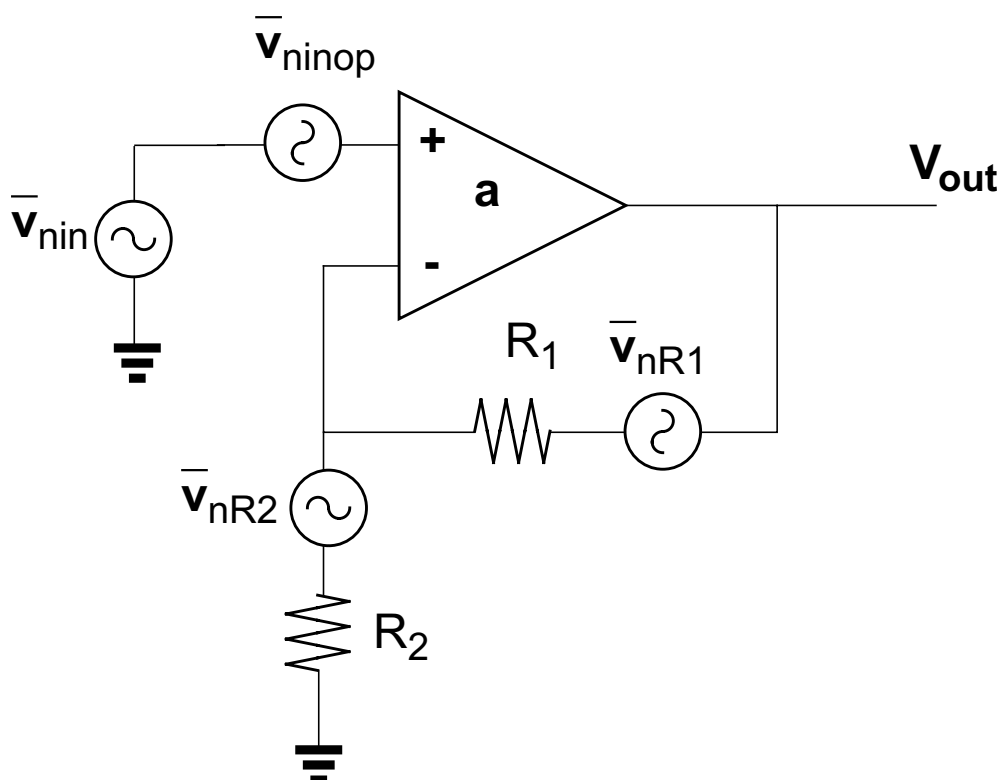


$$\overline{v_{n_{ineq}}} = \sqrt{\left(\frac{\overline{v_{ninop}} \left(1 + \frac{R_f}{R_s} \right)}{\frac{R_f}{R_s}} \right)^2 + v_{nRs}^2 + \left(\frac{v_{nRf}}{\frac{R_f}{R_s}} \right)^2}$$

Note that the noise at the output is the input-referred noise multiplied by the *closed-loop* gain

$$\overline{v_{nout}} = \overline{v_{nin}} \cdot \frac{R_f}{R_s}$$

Non-Inverting amplifier noise sources and input-referred noise



\bar{v}_{ninop} is the input-referred voltage noise of the opamp

\bar{v}_{nR1} is the voltage noise of R_1 $\overline{v_{nR1}} = \sqrt{4kTR_1}$

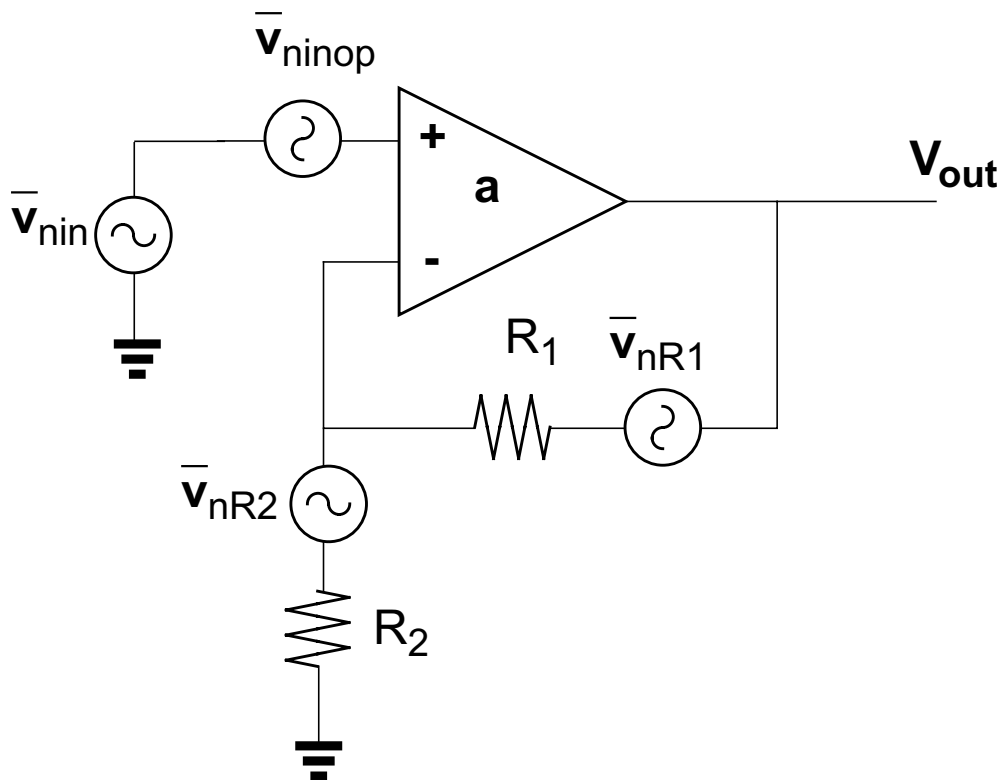
\bar{v}_{nR2} is the voltage noise of R_2 $\overline{v_{nR2}} = \sqrt{4kTR_2}$

These each contribute to the equivalent total input-referred noise of the stage, \bar{v}_{nineq}

To calculate this consider

1. The noise of R_1 appears at the output and can be referred to the input by dividing by the closed-loop gain $(1+R_1/R_2)$
2. The noise of R_2 is gained up to the output by the gain of an inverting gain stage R_1/R_2 , and then referred back to the input by dividing by the closed loop gain $(1+R_1/R_2)$
3. The input-referred opamp noise appears at the input

These noise sources are uncorrelated, so rms sum



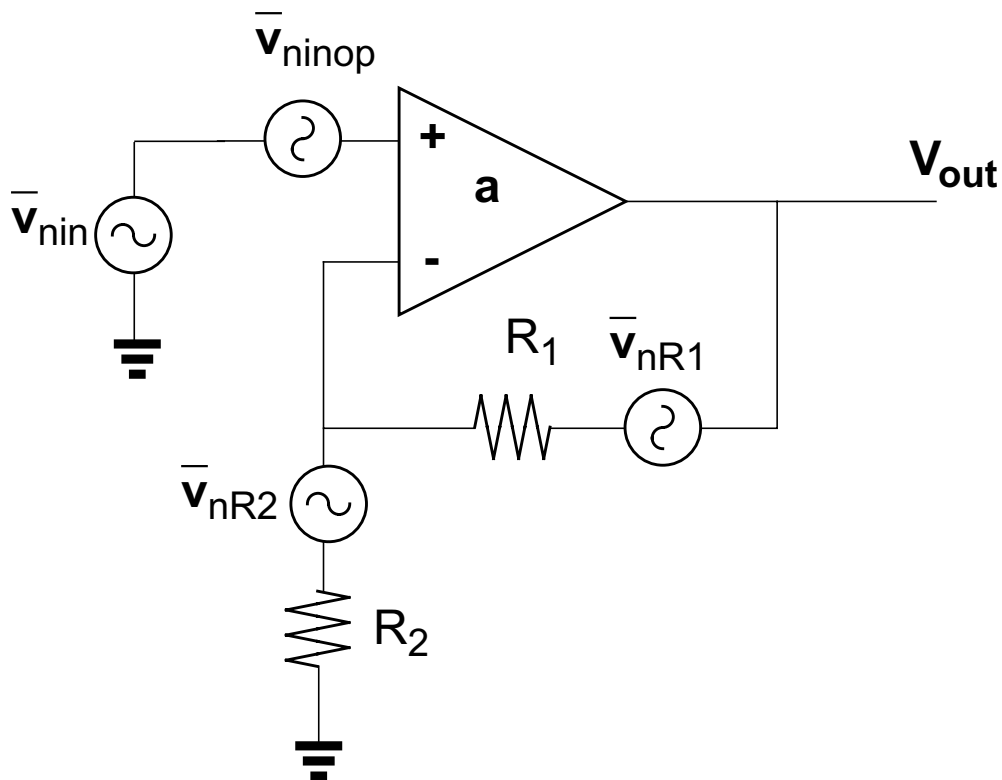
Consider first the equivalent resistor noise at the output

$$\overline{v_{noutReq}} = \sqrt{(\overline{v_{nR1}})^2 + \left(v_{nR2}\left(\frac{R_1}{R_2}\right)\right)^2}$$

$$\overline{v_{noutReq}} = \sqrt{4kTR_1 + 4kTR_2\left(\frac{R_1}{R_2}\right)^2}$$

Refer this back to the input

$$\overline{v_{ninReq}} = \frac{\sqrt{4kTR_1 + 4kTR_2\left(\frac{R_1}{R_2}\right)^2}}{\frac{R_1 + R_2}{R_2}}$$

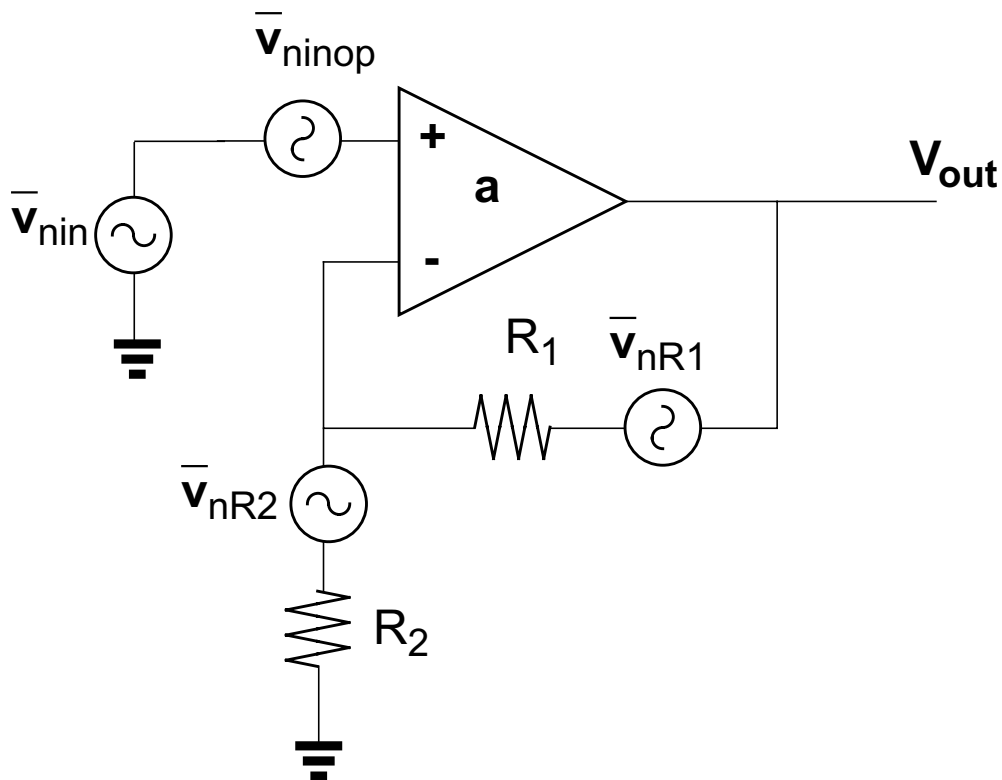


$$\overline{v_{ninReq}} = \frac{\sqrt{4kTR_1 + 4kTR_2\left(\frac{R_1}{R_2}\right)^2}}{\frac{R_1 + R_2}{R_2}}$$

$$\overline{v_{ninReq}} = \sqrt{\frac{4kTR_1R_2^2 + 4kTR_1^2R_2}{(R_1 + R_2)^2}}$$

$$\overline{v_{ninReq}} = \sqrt{\frac{4kTR_1R_2(R_1 + R_2)}{(R_1 + R_2)^2}} = \sqrt{\frac{4kTR_1R_2}{(R_1 + R_2)}}$$

$$\overline{v_{ninReq}} = \sqrt{4kT(R_1 \parallel R_2)}$$



Considering the opamp noise as well, the total equivalent input-referred noise is given by

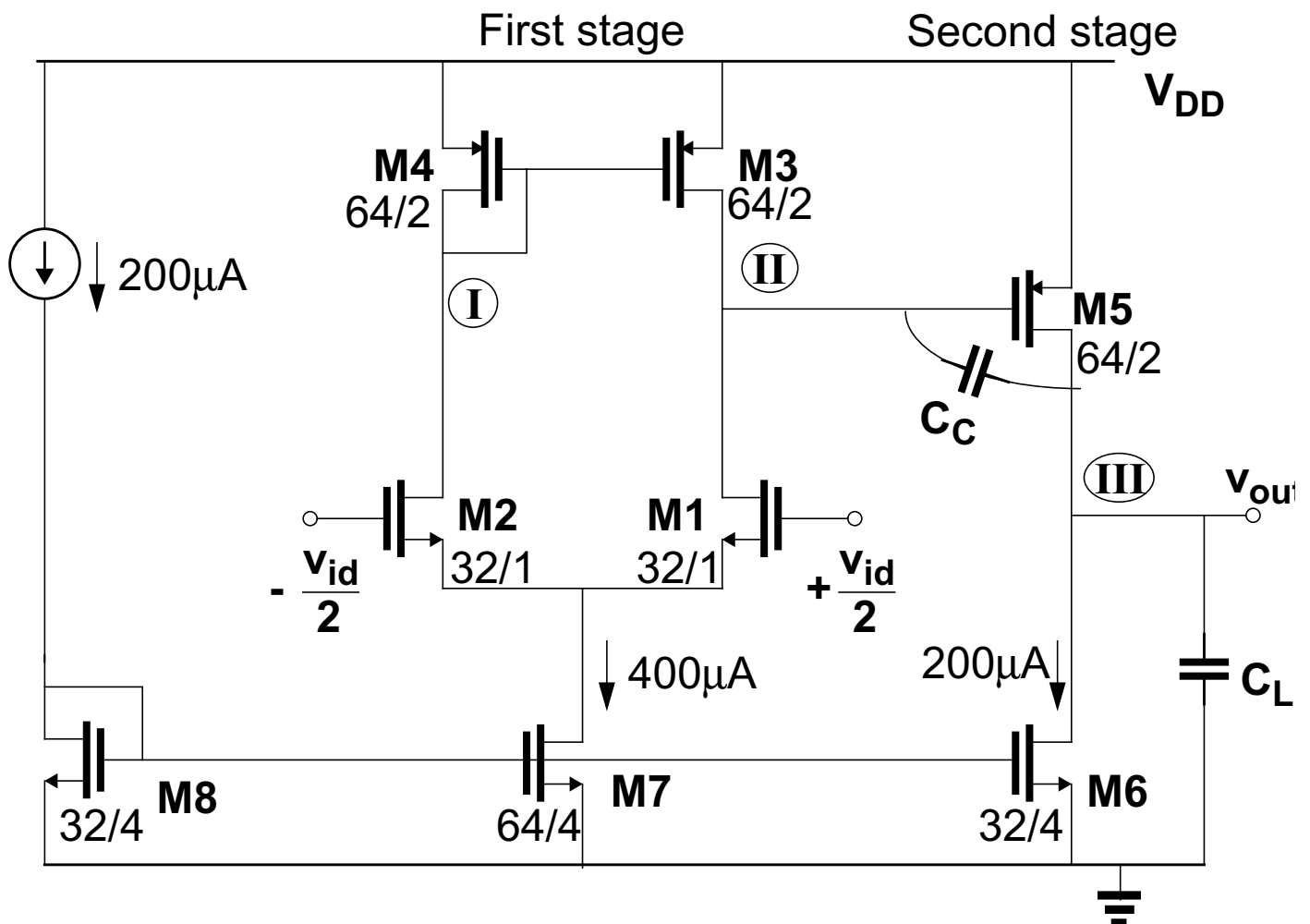
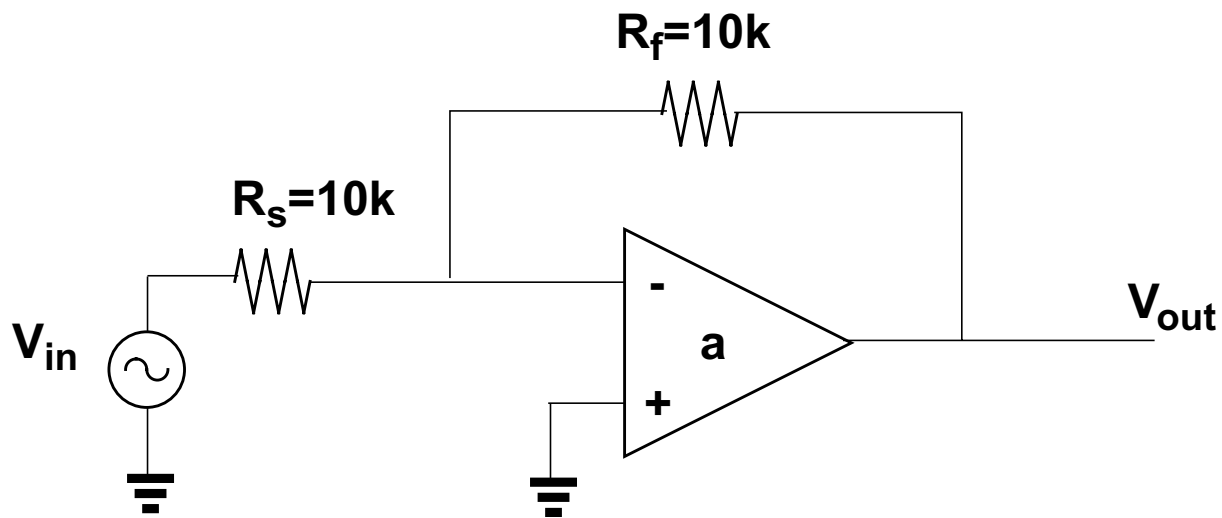
$$\overline{v_{nineq}} = \sqrt{\overline{v_{ninop}}^2 + \overline{v_{ninReq}}^2}$$

$$\overline{v_{nineq}} = \sqrt{\overline{v_{ninop}}^2 + 4kT(R_1 \parallel R_2)}$$

Again, the noise at the output is the input-referred noise multiplied by the *closed-loop* gain

$$\overline{v_{nouteq}} = \overline{v_{nineq}} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

Problem: What is the input-referred noise voltage density of the inverting amplifier stage shown below, if the opamp shown below is used (from P. 293)?



11 Opamp circuits

11.1 Miscellaneous Opamp Non-idealities

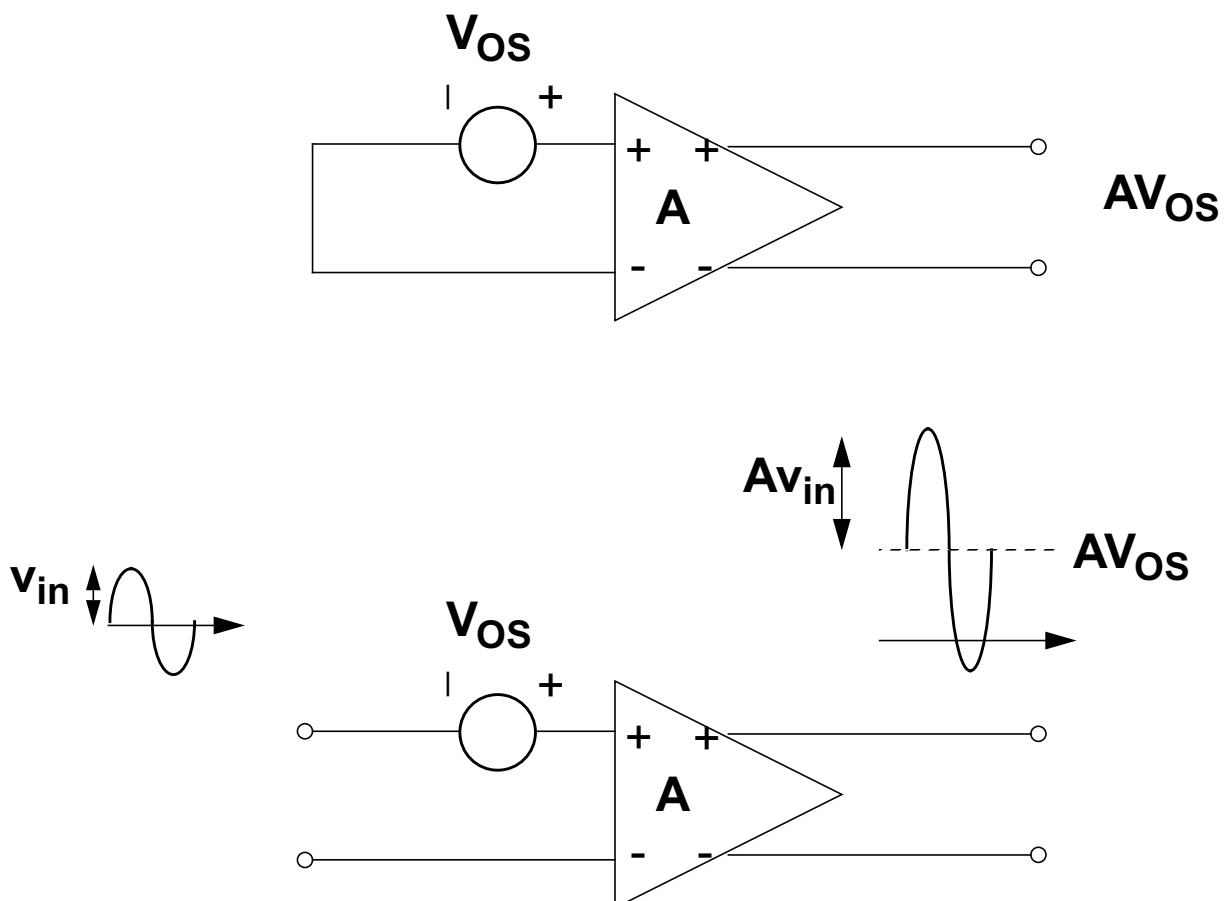
11.1.1 DC Offset

Asymmetries and mismatches contribute to offsets in amplifiers.

These DC offsets are usually modelled by the input-referred offset of the opamp.

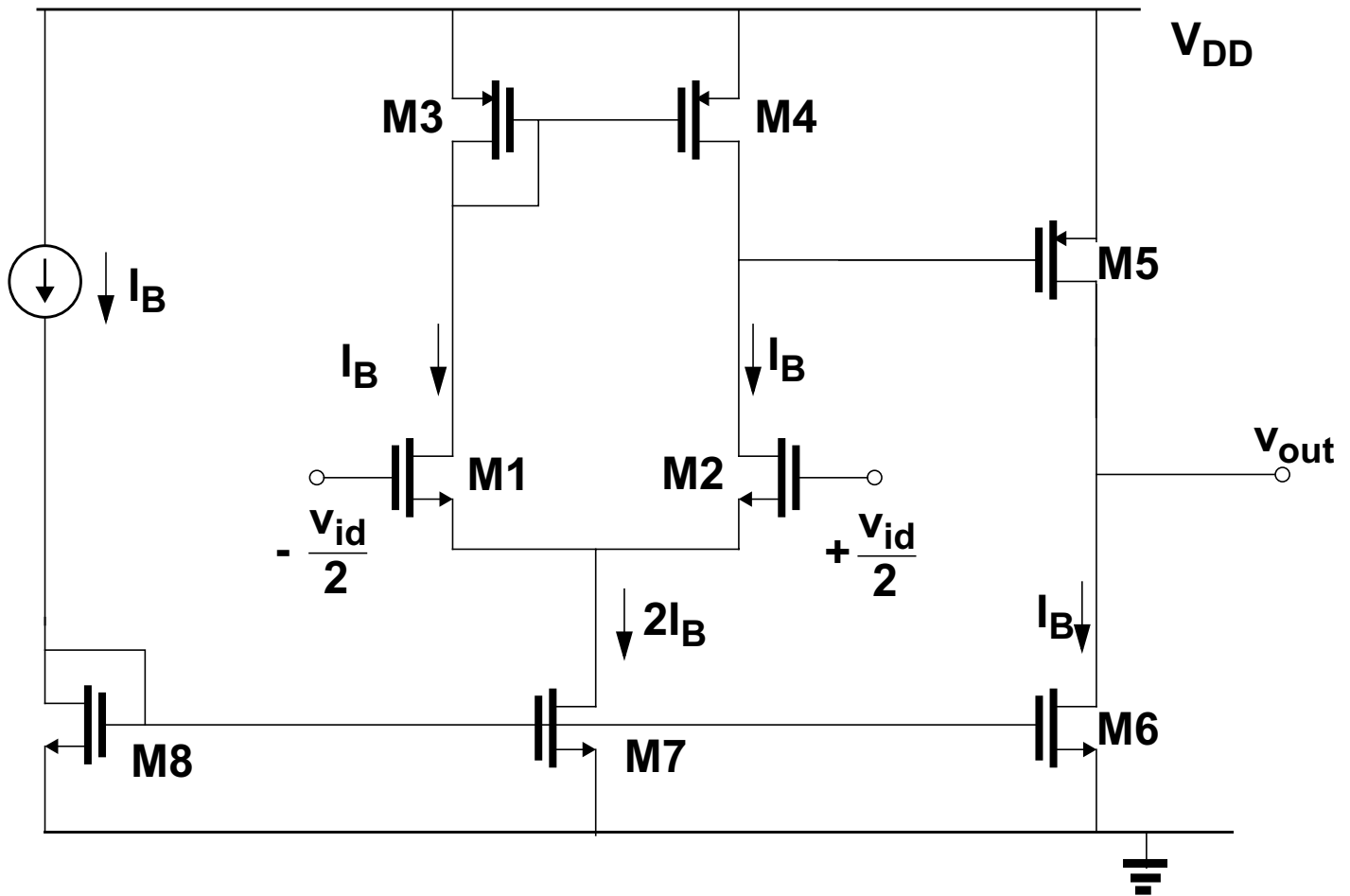
The input-referred DC offset voltage is amplified by the voltage gain of the amplifier.

This results in a DC output voltage in the presence of no input signal. When there is an input-signal, both signal and offset voltage are amplified



Systematic Offset

Systematic offsets result from asymmetries in the biasing of the amplifier



As a minimum requirement for symmetry we need

$$M1=M2; M3=M4; M6=M8; M7=2*M6, M8$$

When $v_{id}=0$ we would like to have equilibrium i.e. $I_{D2}=I_{D4}, I_{D5}=I_{D6}$

If $v_{id}=0$ then I_B nominally flows through M1, M2, and then through M3, M4.

However this is only exactly true if $V_{DS4}=V_{DS3}=V_{GS3}$

But $V_{DS4} = V_{GS5}$ i.e. V_{DS4} is set by V_{GS5}

So V_{GS5} must be set equal to V_{GS3} , i.e.

With I_B flowing through M5

$$\Rightarrow \text{for no systematic offset we need } (W/L)_5=(W/L)_{3,4}$$

If V_{DS4} is not equal to V_{DS3} , then there will be a mismatch between I_{B4} and I_{B2} .

$$\Delta I_{B2,4} = (g_{ds2} + g_{ds4})\Delta V_{DS}$$

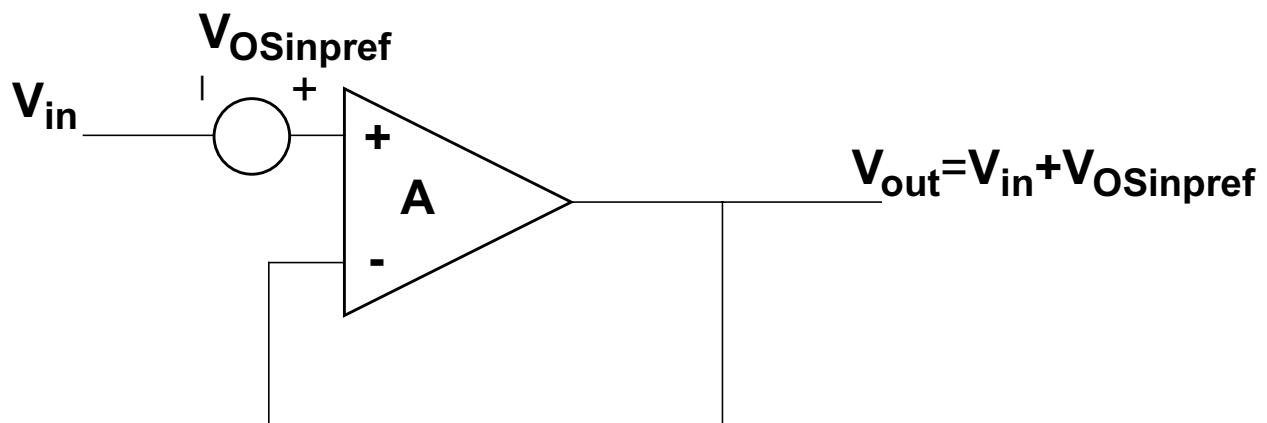
and this can be modelled by an input-referred offset voltage

$$V_{OSinpref} = \frac{\Delta I_{B2,4}}{g_{m1}}$$

i.e. the current mismatch divided by the g_m of the input pair

This is the input voltage that would be required to correct the current imbalance

If, say, the amplifier were connected as a follower, this offset would be present at the output

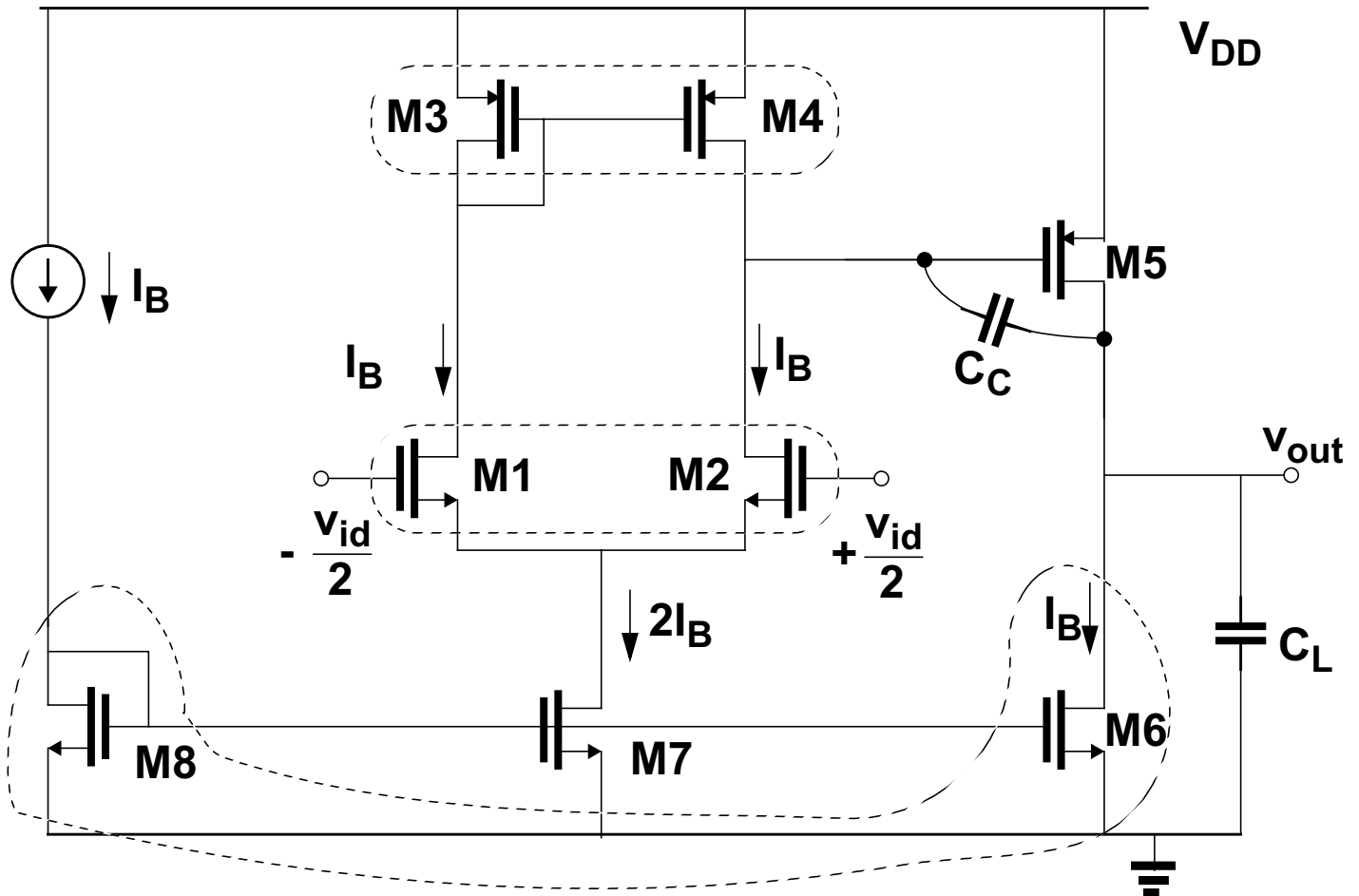


Similarly if the voltage at V_{out} causes an imbalance between I_{D5} and I_{D6} , this will give an additional input-referred offset

$$V_{OSinpref} = \frac{\Delta I_{B5,6}}{g_{m5} \cdot \frac{g_{m1}}{g_{ds2} + g_{ds4}}}$$

As in the case of noise, this is usually less than the previous source

Random Offset



$M1=M2$; $M3=M4$; $M6=M8$ i.e have same W/L . $M7=2*M6$

$$g_{m1}=g_{m2}, g_{m3}=g_{m4}$$

However random mismatches between nominally identical transistors lead V_t mismatch and so current mismatches. These cause offsets in the opamp, which for characterisation are usually referred to the opamp input (as in the case of noise).

What is the input-referred offset voltage due to random mismatch?

1. Contribution of input pair.

Input pair have offset voltage mismatch given by

$$\Delta V_{t1} = \frac{A_{Vt}}{\sqrt{(WL)_1}}$$

Random Offset (contd)

2. Contribution of mirror pair M3 M4.

Mirror pair have offset voltage given by

$$\Delta V_{t3} = \frac{A_{Vt}}{\sqrt{(WL)_3}}$$

These cause a mismatch in drain currents ΔI between M3 and M4

$$I_{D4} - I_{D3} = \Delta I = g_{m3} \Delta V_{t3}$$

To refer this to input divide by g_m of input pair

Input-referred offset voltage from mirror pair then given by

$$\Delta V_{t3inpref} = \frac{g_{m3} \Delta V_{t3}}{g_{m1}}$$

3. Contribution output stage

Suppose there is a mismatch between M6 and M8

$$\Delta V_{t6} = \frac{A_{Vt}}{\sqrt{(WL)_6}}$$

These cause a mismatch in drain currents ΔI between M8 and M6

$$I_{D6} - I_{D8} = \Delta I = g_{m6} \Delta V_{t6}$$

To refer this to input divide by voltage to current gain of amplifier

Input pair have offset voltage given by

$$\Delta V_{t6inpref} = \frac{g_{m6} \Delta V_{t6}}{\frac{g_{m1}}{g_{ds1} + g_{ds3}} \cdot g_{m5}}$$

If all g_m s in same order of magnitude then this will be much less than other two offsets.

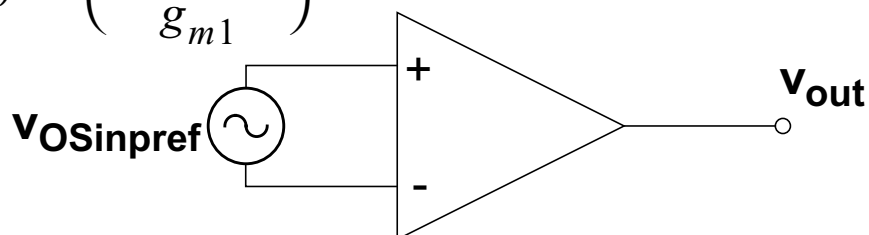
Similarly can neglect any offset from M5

Random Offset (contd)

4. Total input referred offset

Sum contributions from input pair and mirror pair quadratically as offset is a random effect

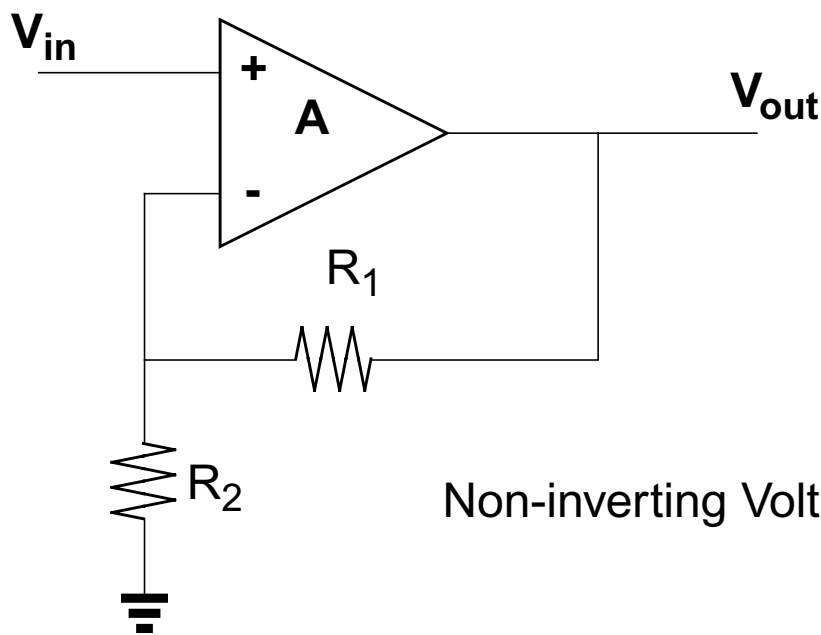
$$V_{OSinpref} = \sqrt{(\Delta V_{t1})^2 + \left(\frac{g_{m3}\Delta V_{t3}}{g_{m1}}\right)^2}$$



=> maximise g_m of input pair, minimise g_m of load pair

Offset of opamp gain stages

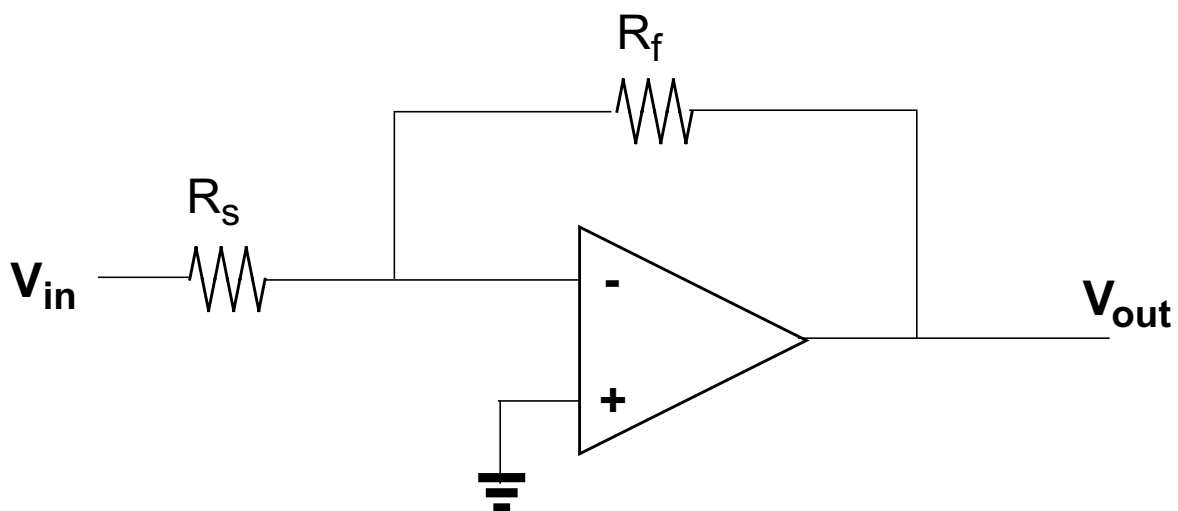
Non-inverting Voltage amplifier:



Non-inverting Voltage amplifier:

$$V_{out} \cong \frac{R_1 + R_2}{R_2}(V_{in}) + \frac{R_1 + R_2}{R_2}(V_{OSinpref})$$

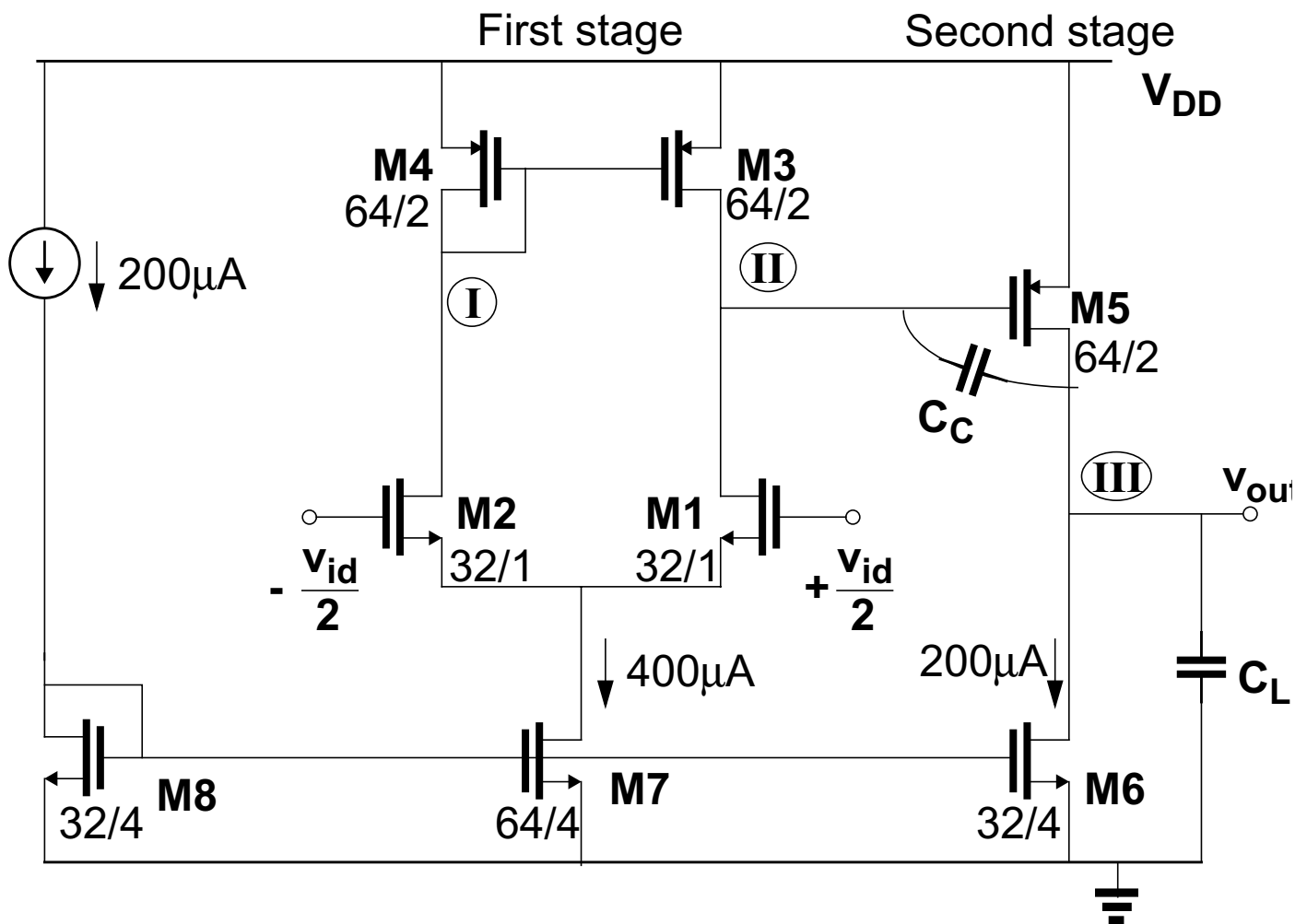
Inverting Voltage amplifier:



$$V_{out} \cong -\frac{R_f}{R_s}(V_{in}) + \frac{R_f + R_s}{R_s}(V_{OSinpref})$$

Problem: What is the input-referred random offset of the amplifier shown below (from P. 293).

Take $A_{Vt}=10\text{mV}\mu\text{m}$.

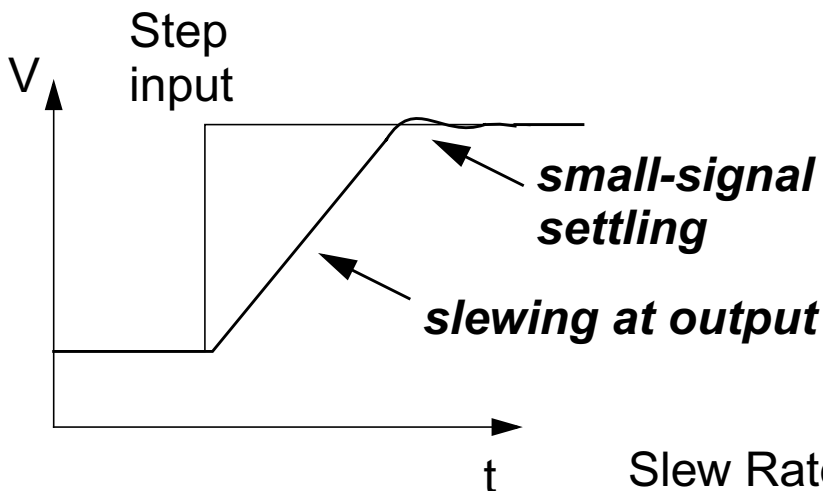
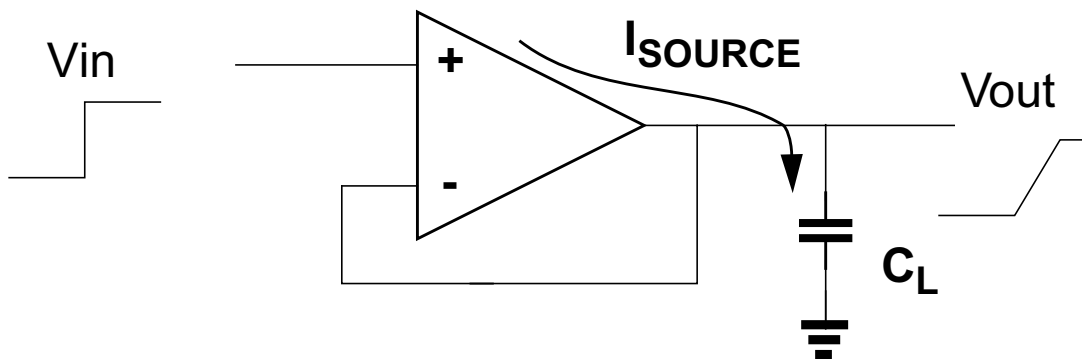


11.1.2 Slew Rate

Slew rate = maximum rate at which the output can change when a fast large signal input (e.g. a step) is applied.

For example a unity gain amplifier with a capacitive load.

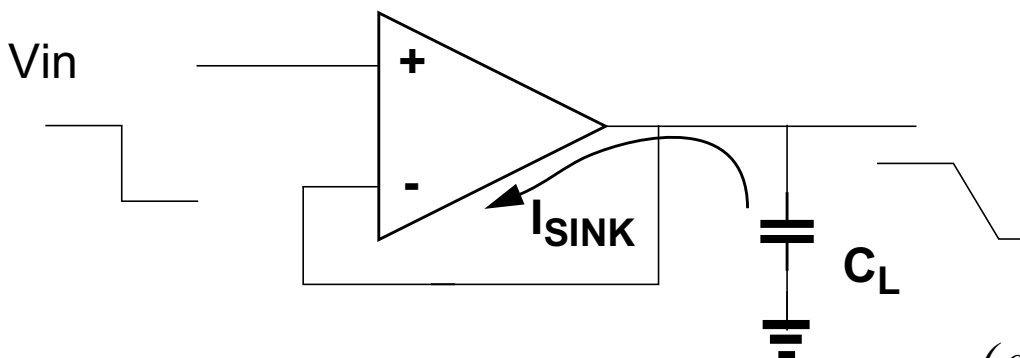
If a large step is applied at the input then the amplifier will have to source a large current into the capacitor. There is a limit to the current the amplifier can source => output 'slews'



Recall:

$$I = C \frac{dv}{dt}$$

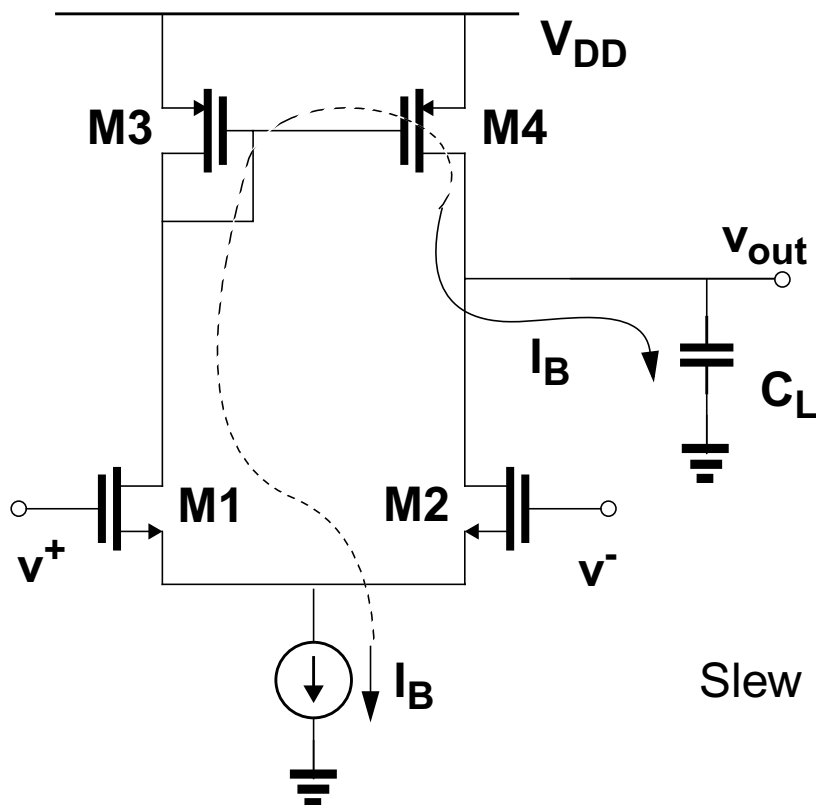
$$\text{Slew Rate} = \left(\frac{dv}{dt} \right)_{max} = \frac{I_{SOURCE}}{C}$$



Similarly for a negative step at input: $\text{Slew Rate} = \left(\frac{dv}{dt} \right)_{max} = \frac{I_{SINK}}{C}$

Slew rate of single stage amplifier

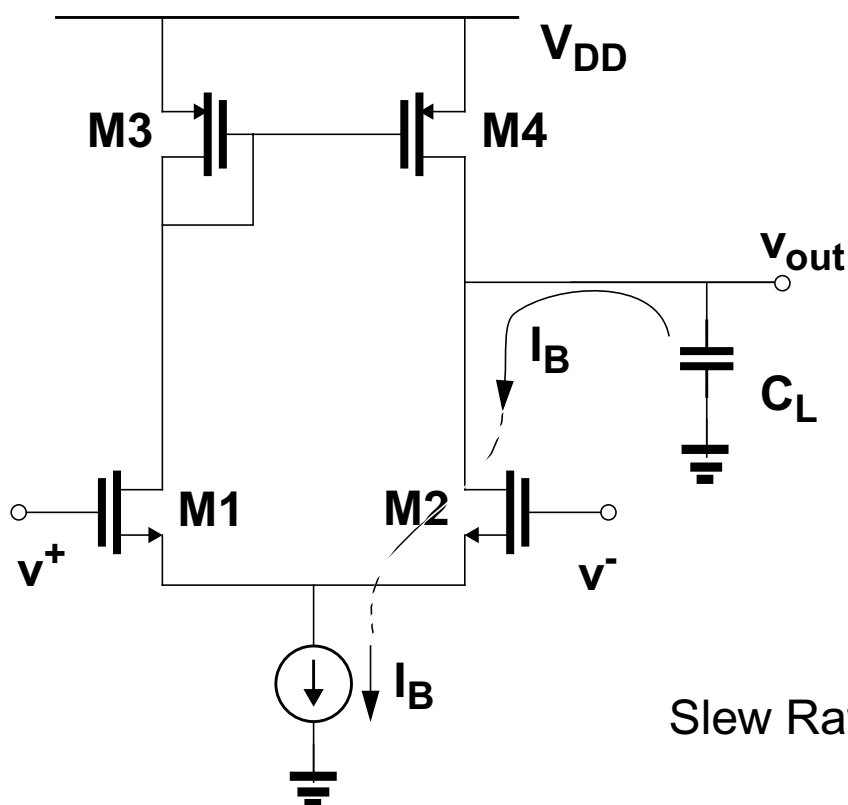
1. Charging C_L



If a positive step is applied at the input with $V^+ \gg V^-$ then all of I_B flows through M1 and is mirrored via M3 and M4 so that M4 supplies a charging current of I_B to C_L

$$\text{Slew Rate} = \left(\frac{dv_{out}}{dt} \right)_{max} = \frac{I_B}{C_L}$$

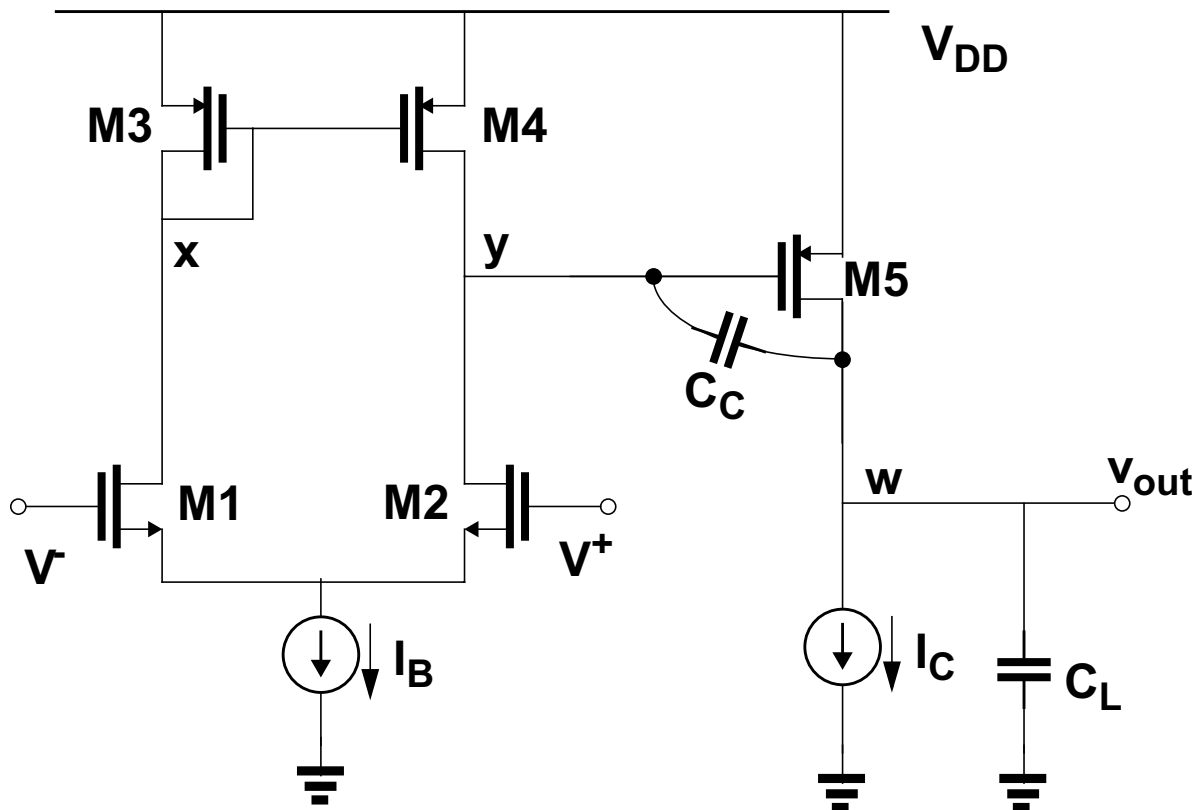
2. Discharging C_L



If a negative step is applied at the input with $V^- \gg V^+$ then all of I_B flows through M2 and discharges C_L

$$\text{Slew Rate} = \left(\frac{dv_{out}}{dt} \right)_{max} = -\frac{I_B}{C_L}$$

Slew Rate of two-stage amplifier



In two-stage amplifier there are two capacitors to be charged i.e. need to supply current to both C_C and C_L if V_{out} is changing

For C_C : charging and discharging current is supplied by first stage

$$\text{Slew Rate} = \frac{I_B}{C_C} \quad (1)$$

For C_L the situation is slightly more complicated

If the bias current of the second stage is I_C (this might be but does not have to be equal to I_B) then:

Discharging C_L i.e. when $V^+ \ll V^- \Rightarrow V_y$ is high so all of I_C is available to discharge C_L .

$$\text{Slew Rate} = \frac{I_C}{C_L} \quad (2)$$

Charging C_L i.e. when $V^+ \gg V^- \Rightarrow V_y$ is low so V_{GS5} is very large \Rightarrow large charging current available through M5 (i.e. $\gg I_C$) \Rightarrow not really a slew rate limitation at output node

Slew rate of amplifier usually taken as the smaller of (1) and (2)

Note on slew rate with Sine-wave

$$V = A \sin \omega t$$

$$\frac{dV}{dt} = A \omega \cos \omega t$$

$$\left(\frac{dV}{dt} \right)_{max} = A \omega$$

If slew rate is less than this get slew-rate distortion

Example: If the amplifier on P291 has a 1Vpp sine wave signal at the output what is the maximum frequency before slewing occurs

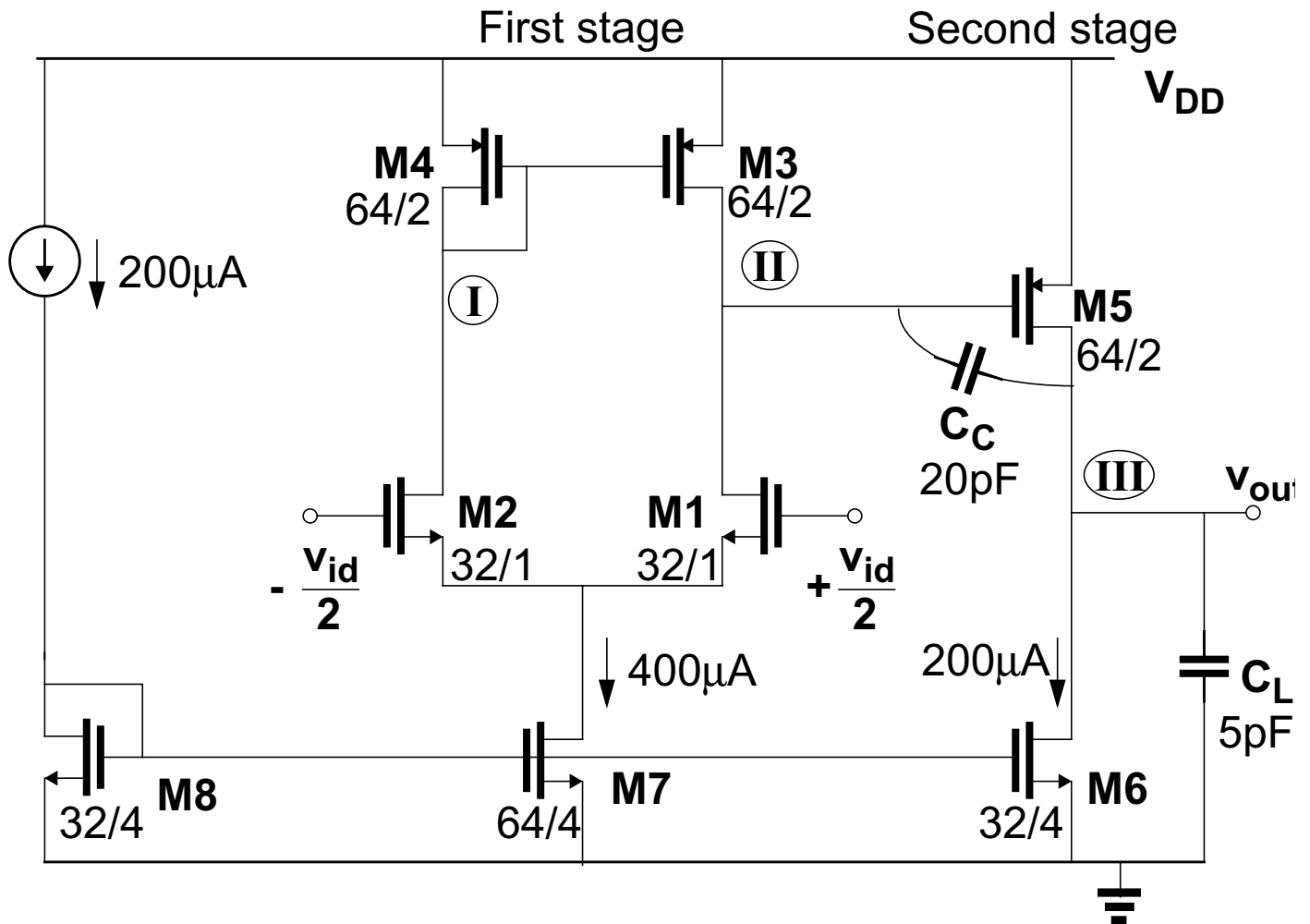
$$A \omega < \frac{I}{C}$$

$$f < \frac{I}{2\pi C A}$$

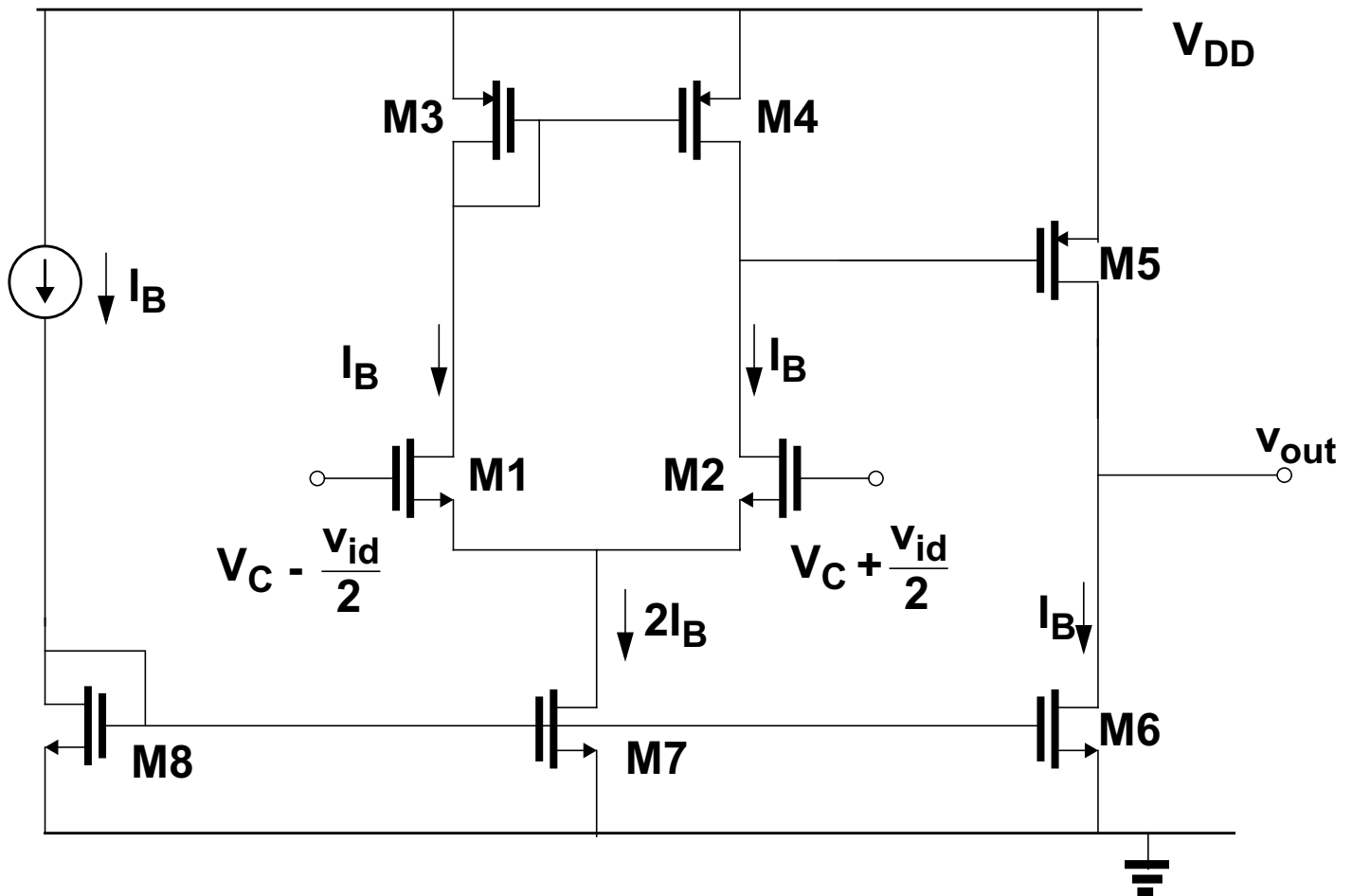
$$f < \frac{200\mu A}{2\pi 5 pF 0.5}$$

$$f < 12 MHz$$

Problem: What is the slew rate of the amplifier shown on P. 293
Assume a Miller compensation capacitor of 20pF has been used to guarantee stability.

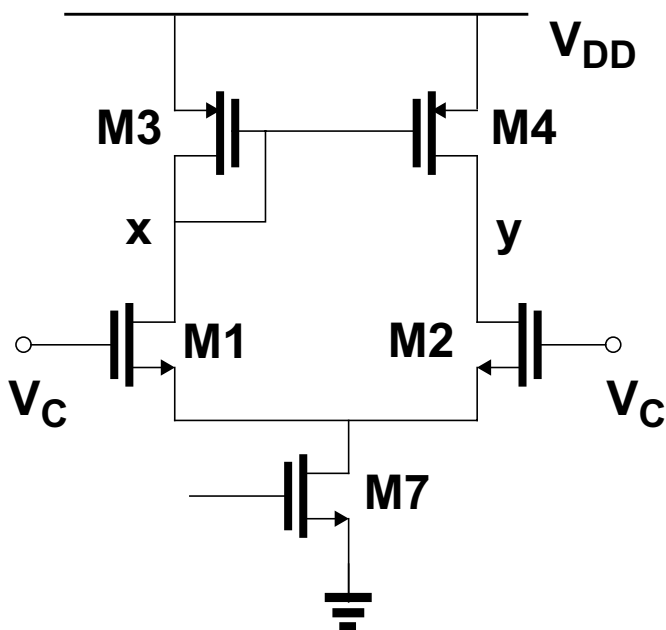


11.1.3 Common-mode input range



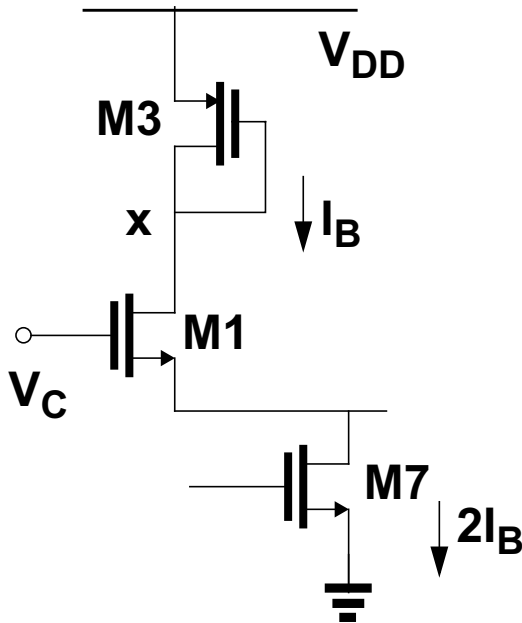
The input is a small-signal v_{id} sitting on a DC bias voltage V_C . Assuming good common mode rejection, V_C can vary without changing the output.

However for normal operation all transistors must remain in saturation which limits how much V_C can vary
i.e. limits the common-mode input range



Only need to look at first stage
Common mode input range is a large signal characteristic, so ignore v_{id}
With the same voltage at the gates of M1 and M2, by symmetry $V_x = V_y$
So just look at LHS

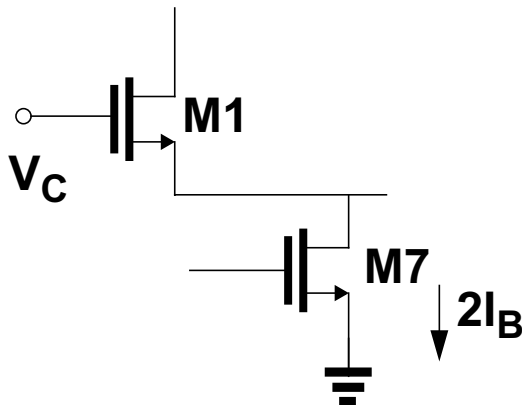
Common-mode input range



There is an upper limit and a lower limit to the common mode input range.

So need to consider what determines the upper and lower limits

Lower limit (looking towards ground):

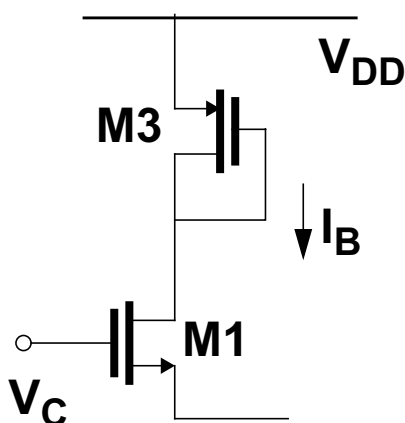


Lower limit: As V_C decreases so does voltage at source of M1 (drain of M7) but M7 must remain in saturation

$$\Rightarrow V_C > V_{GS1} + V_{SAT7}$$

$$\Rightarrow V_C > V_{GS1} + V_{GS7} - V_{tn}$$

Upper limit: looking towards V_{DD}



Upper limit: As V_C increases so does source of M1 but drain-source voltage of M1 must not go less than V_{SAT}

$$V_{D1} = V_{DD} - V_{GS3}, \quad V_{S1} = V_C - V_{GS1}$$

For M1 to remain in saturation

$$V_{D1} - V_{S1} > V_{GS1} - |V_{tp}|$$

$$V_{D1} - (V_C - V_{GS1}) > V_{GS1} - |V_{tp}|$$

$$V_{D1} > V_C - |V_{tp}| \Rightarrow V_C < V_{D1} + |V_{tp}|$$

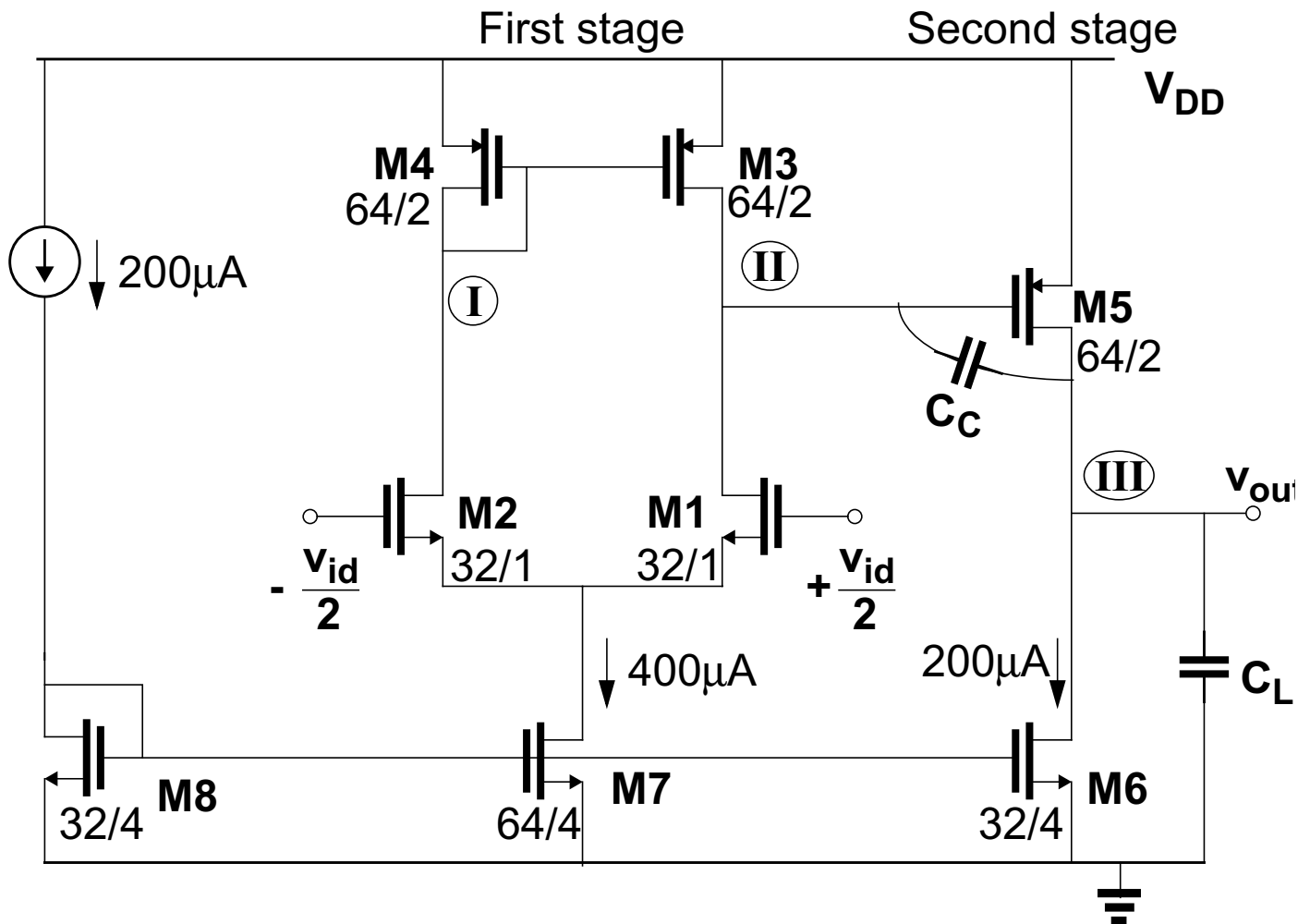
$$\Rightarrow V_C < V_{DD} - V_{GS3} + |V_{tp}|$$

$$\text{Common-mode range: } V_{GS1} + V_{GS7} - V_{tn} < V_C < V_{DD} - V_{GS3} + |V_{tp}|$$

Problem- Common-mode range:

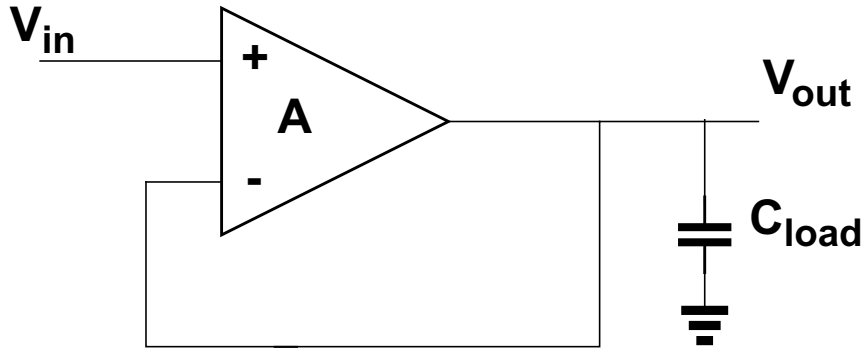
What is the Common-mode input range of the amplifier shown on P. 293?

Take $V_{DD}=5V$, $V_{tn}=V_{tp}=0.8V$



11.2 Opamp applications

11.2.1 Capacitive loads



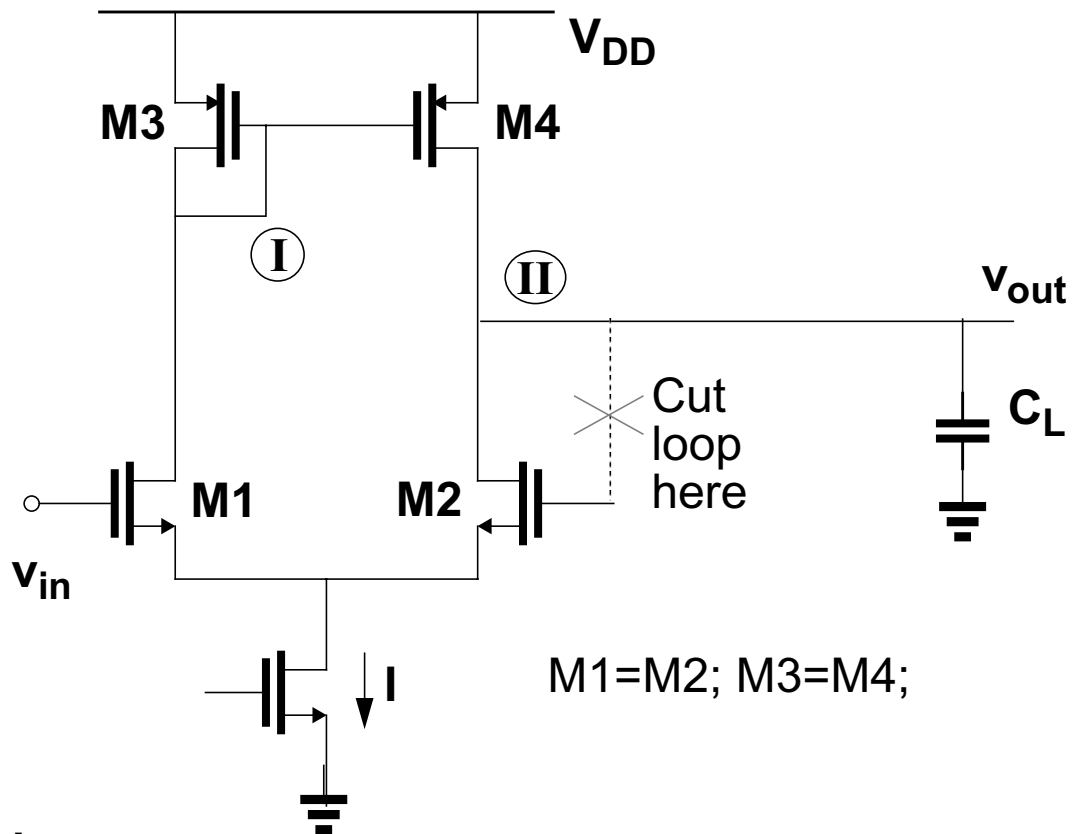
Opamp choice depends on gain requirement.

For a high-gain requirement e.g. ADC front-end stages, need a high gain amplifier to reduce static error between input and output

Some applications, e.g. buffering a reference voltage may only need a moderate gain.

The following pages consider various capacitively-loaded opamps in a unity gain buffer configuration, i.e. with feedback factor =1

Capacitive load buffer-moderate gain.



Loop Gain

$$\text{LoopGain} = \frac{g_{m1}}{g_{ds2} + g_{ds4}}$$

Stability

Identify poles

$$\text{Node I} \quad |\omega_{pI}| = \frac{g_I}{C_I} \approx -\frac{g_{m3}}{C_I}$$

$$\text{Node II} \quad |\omega_{pII}| = \frac{g_{II}}{C_{II}} \approx -\frac{g_{ds2} + g_{ds4}}{C_L}$$

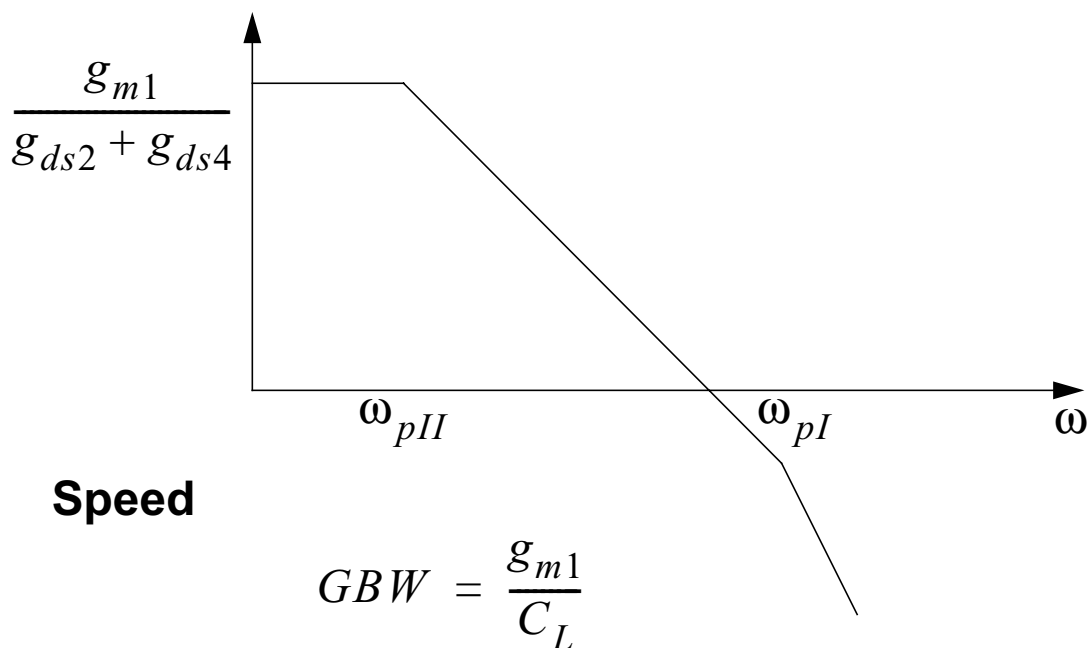
As $g_{ds} \ll g_m$, then ω_{pII} will be dominant (unless $C_L \ll C_I$)
So the load capacitance does the compensation i.e. sets the dominant pole

For $>45^\circ$ PM C_L needs to be large enough such that $GBW < \omega_{pI}$

$$GBW = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \cdot \frac{g_{ds2} + g_{ds4}}{C_L} = \frac{g_{m1}}{C_L}$$

$$\text{For } 45^\circ \text{ PM: } \frac{g_{m1}}{C_L} < \frac{g_{m3}}{C_I} \Rightarrow C_L > \frac{g_{m1}}{g_{m3}} C_I$$

This form of stability compensation is called load compensation. Can be used when the dominant pole is at the output node. Usually restricted to single-stage opamps (one dominant pole)

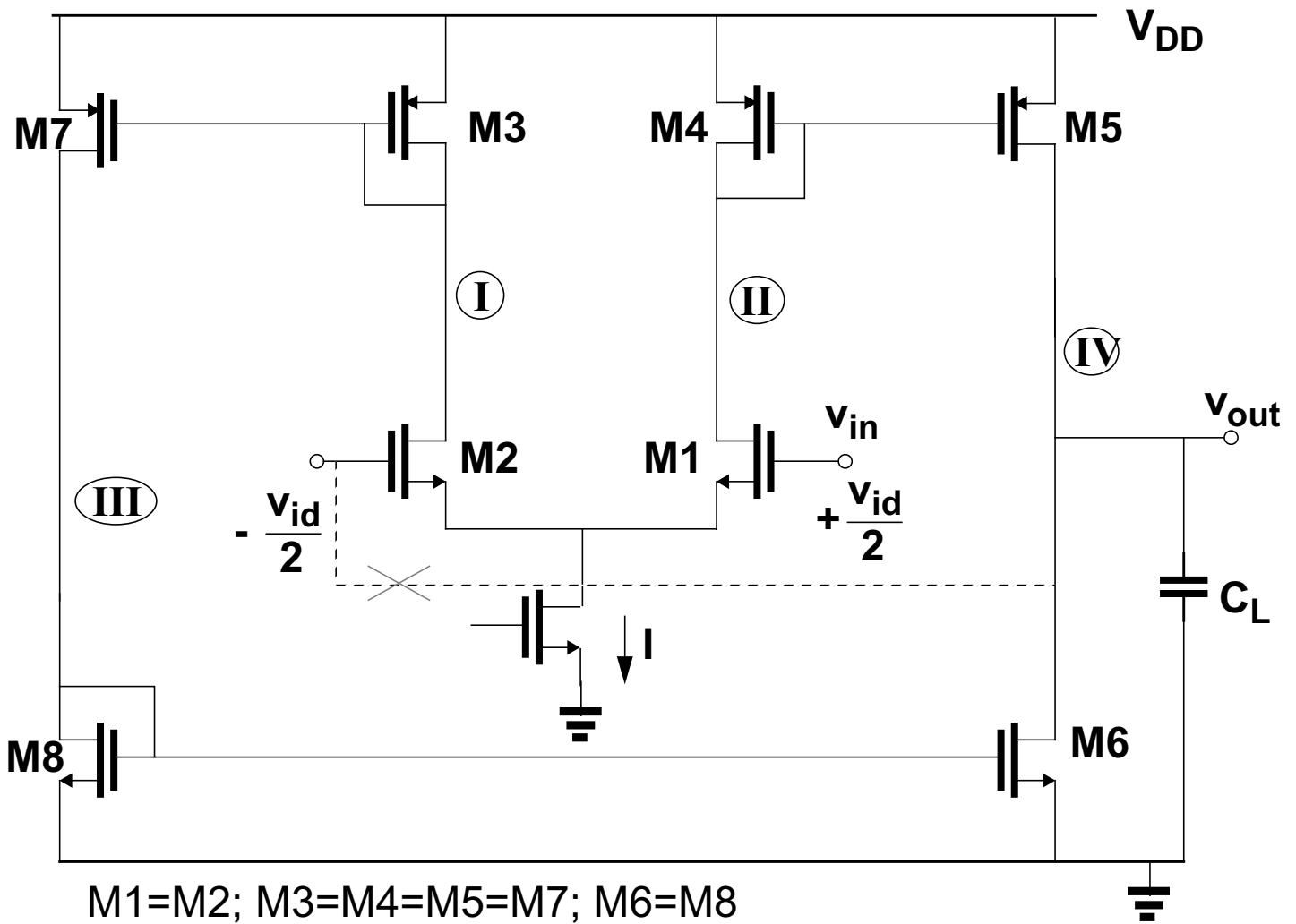


So for a given C_L , then need to increase g_{m1} , i.e. increase W/L until you hit weak inversion, then need to increase **current**
=> power

But be careful with effect on stability

Noise: See earlier analysis. M1, M2, M3, M4 dominant

Capacitive load buffer, moderate gain (symmetric buffer)



Loop Gain

Input signal $+v_{id}/2$ at gate of M1 causes increase in drain current in M1 ($=g_{m1}v_{id}/2$).

This is mirrored to output node via M4, M5.

Similarly signal $-v_{id}/2$ at gate of M2 causes decrease in drain current in M2 ($=g_{m2}v_{id}/2$).

This is mirrored to output node via M3, M7,M8,M6

Total change in current at output node = $g_{m1}v_{id}$

$$LoopGain = \frac{g_{m1}}{g_{ds5} + g_{ds6}}$$

Stability

Identify poles

$$\text{Node I} \quad |\omega_{pI}| = \frac{g_I}{C_I} \approx -\frac{g_{m3}}{C_I}$$

$$\text{Node II} \quad |\omega_{pII}| = \frac{g_{II}}{C_{II}} \approx -\frac{g_{m3}}{C_{II}}$$

$$\text{Node III} \quad |\omega_{pIII}| = \frac{g_{III}}{C_{III}} \approx -\frac{g_{m8}}{C_{III}}$$

$$\text{Node IV} \quad |\omega_{pIV}| = \frac{g_{IV}}{C_{IV}} \approx -\frac{g_{ds5} + g_{ds6}}{C_L}$$

As $g_{ds} \ll g_m$, then ω_{pIV} will be dominant (unless $C_L \ll C_{I,II,III}$)

If say ω_{pIII} is the next dominant, then

For $>45^\circ$ PM C_L needs to be large enough such that $GBW < \omega_{pIII}$

$$GBW = \frac{g_{m1}}{g_{ds5} + g_{ds6}} \cdot \frac{g_{ds5} + g_{ds6}}{C_L} = \frac{g_{m1}}{C_L}$$

$$\text{For } 45^\circ \text{ PM: } \frac{g_{m1}}{C_L} < \frac{g_{m8}}{C_{III}} \Rightarrow C_L > \frac{g_{m1}}{g_{m8}} C_{III}$$

Other non-dominant poles need to be well above GBW in order not to degrade the PM.

So again the load capacitance does the compensation

Notes on Symmetrical OTA and on load compensation

1. Because C_L is the compensation capacitor it has a minimum value below which the opamp goes unstable.

If C_L is removed then opamp may go unstable.

2. Gain is low - same as for single stage. In fact this is a single stage amplifier

For more gain could increase mirror ratios $M4:M5$, $M3:M7$ (but be careful with pole movement due to extra capacitance at mirror gates)

Or use cascodes at output stage

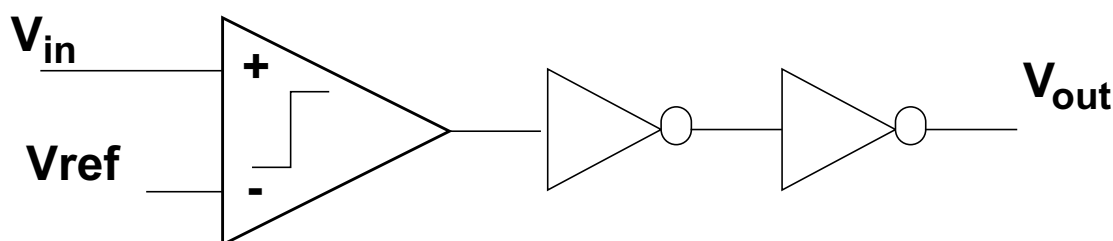
Speed

$$GBW = \frac{g_{m1}}{C_L}$$

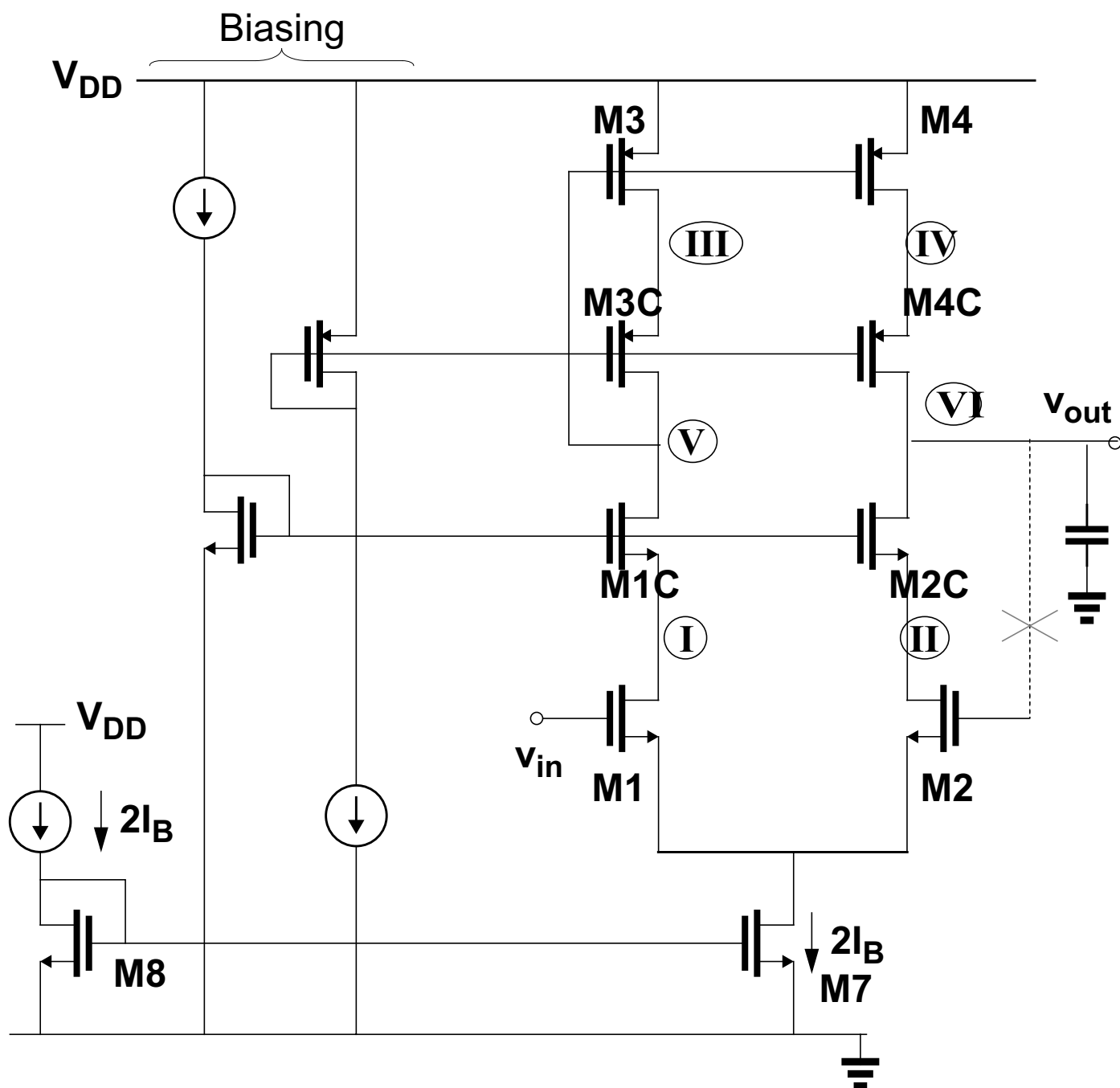
Same trade-off of GBW v. power

Noise: $M1$, $M2$, $M3$, $M4$ dominant

Note that the symmetric OTA is often used as a comparator, with extra inverter stages added



Capacitive load buffer-high gain. Cascode or telescopic amplifier



Loop Gain

$$M1=M2, M1C=M2C, M3=M4, M3C=M4C, M7=M8$$

$$LoopGain = \frac{g_{m1}}{\frac{g_{ds2}}{g_{m2C}/g_{ds2C}} + \frac{g_{ds4}}{g_{m4C}/g_{ds4C}}}$$

Stability Identify poles

$$\text{Node I} \quad |\omega_{pI}| = \frac{g_I}{C_I} \approx -\frac{g_{m1}C}{C_I}$$

$$\text{Node II} \quad |\omega_{pII}| = \frac{g_{II}}{C_{II}} \approx -\frac{g_{m2}C}{C_{II}}$$

$$\text{Node III} \quad |\omega_{pIII}| = \frac{g_{III}}{C_{III}} \approx -\frac{g_{m3}C}{C_{III}}$$

$$\text{Node IV} \quad |\omega_{pIV}| = \frac{g_{IV}}{C_{IV}} \approx -\frac{g_{m4}C}{C_{IV}}$$

$$\text{Node V} \quad |\omega_{pV}| = \frac{g_V}{C_V} \approx -\frac{g_{m3}}{C_V}$$

$$\text{Node VI} \quad |\omega_{pVI}| = \frac{g_{VI}}{C_{VI}} \approx -\frac{\frac{g_{ds2}}{g_{m2}C/g_{ds2}C} + \frac{g_{ds4}}{g_{m4}C/g_{ds4}C}}{C_L}$$

With very low conductance (high resistance) at node VI
 ω_{pVI} will be dominant (unless $C_L \ll$ capacitance on other nodes)

So again the load capacitance does the compensation

If say ω_{pV} is the next most dominant pole, then

For $>45^\circ$ PM C_L needs to be large enough such that $GBW < \omega_{pV}$

$$GBW = \frac{g_{m1}}{\frac{g_{ds2}}{g_{m2}C/g_{ds2}C} + \frac{g_{ds4}}{g_{m4}C/g_{ds4}C}} \cdot \frac{\frac{g_{ds2}}{g_{m2}C/g_{ds2}C} + \frac{g_{ds4}}{g_{m4}C/g_{ds4}C}}{C_L} = \frac{g_{m1}}{C_L}$$

$$\text{For stability: } \frac{g_{m1}}{C_L} < \frac{g_{m3}}{C_V} \Rightarrow C_L > \frac{g_{m1}}{g_{m3}} C_V$$

Other non-dominant poles need to be well above GBW in order not to degrade the PM.

Speed

$$GBW = \frac{g_{m1}}{C_L}$$

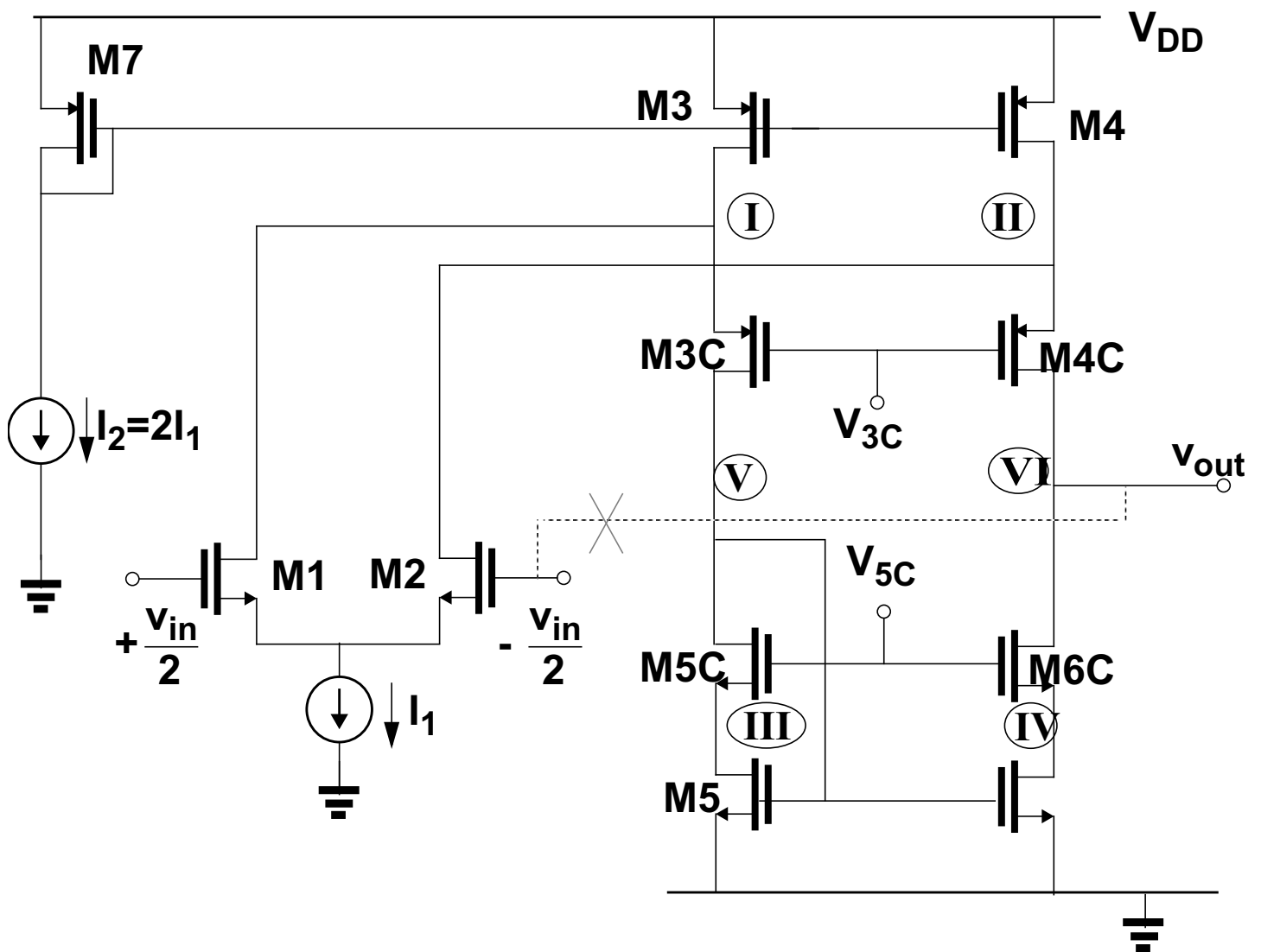
Same trade-off of GBW v. power

Noise: M1, M2, M3 , M4 dominant. In general, cascodes are non-dominant noise contributors

For low noise, increase g_{m1} , decrease g_{m3} , g_{m4} ,
i.e. increase their $V_{GS}-V_t$

This may affect stability -> trade-off

Capacitive load buffer-high gain. Folded-Cascode amplifier



M1=M2, M3=M4, M3C=M4C, M5=M6, M5C=M6C

Loop Gain

$$Gain = -\frac{g_{m1}}{\frac{g_{ds2} + g_{ds4}}{g_{m4C}/g_{ds4C}} + \frac{g_{ds6}}{g_{m6C}/g_{ds6C}}}$$

Stability Identify poles

$$\text{Node I} \quad |\omega_{pI}| = \frac{g_I}{C_I} \approx -\frac{g_{m3}C}{C_I}$$

$$\text{Node II} \quad |\omega_{pII}| = \frac{g_{II}}{C_{II}} \approx -\frac{g_{m4}C}{C_{II}}$$

$$\text{Node III} \quad |\omega_{pIII}| = \frac{g_{III}}{C_{III}} \approx -\frac{g_{m5}C}{C_{III}}$$

$$\text{Node IV} \quad |\omega_{pIV}| = \frac{g_{IV}}{C_{IV}} \approx -\frac{g_{m6}C}{C_{IV}}$$

$$\text{Node V} \quad |\omega_{pV}| = \frac{g_V}{C_V} \approx -\frac{g_{m5}}{C_V}$$

$$\text{Node VI} \quad |\omega_{pVI}| = \frac{g_{VI}}{C_{VI}} \approx -\frac{\frac{g_{ds2} + g_{ds4}}{g_{m4}C/g_{ds4}C} + \frac{g_{ds6}}{g_{m6}C/g_{ds6}C}}{C_L}$$

With very low conductance (high resistance) at node VI
 ω_{pVI} will be dominant (unless $C_L \ll$ capacitance on other nodes)

So again the load capacitance does the compensation

If say ω_{pV} is the next most dominant pole, then

For $>45^\circ$ PM C_L needs to be large enough such that $GBW < \omega_{pV}$

$$GBW = \frac{g_{m1}}{\frac{g_{ds2} + g_{ds4}}{g_{m4}C/g_{ds4}C} + \frac{g_{ds6}}{g_{m6}C/g_{ds6}C}} \cdot \frac{\frac{g_{ds2} + g_{ds4}}{g_{m4}C/g_{ds4}C} + \frac{g_{ds6}}{g_{m6}C/g_{ds6}C}}{C_L} = \frac{g_{m1}}{C_L}$$

$$\text{For stability: } \frac{g_{m1}}{C_L} < \frac{g_{m5}}{C_V} \Rightarrow C_L > \frac{g_{m1}}{g_{m5}} C_V$$

Other non-dominant poles need to be well above GBW in order not to degrade the PM.

Speed

$$GBW = \frac{g_{m1}}{C_L}$$

Same trade-off of GBW v. power

Noise: M1, M2, M3, M4, M5, M6 dominant.

In general, cascodes are non-dominant noise contributors

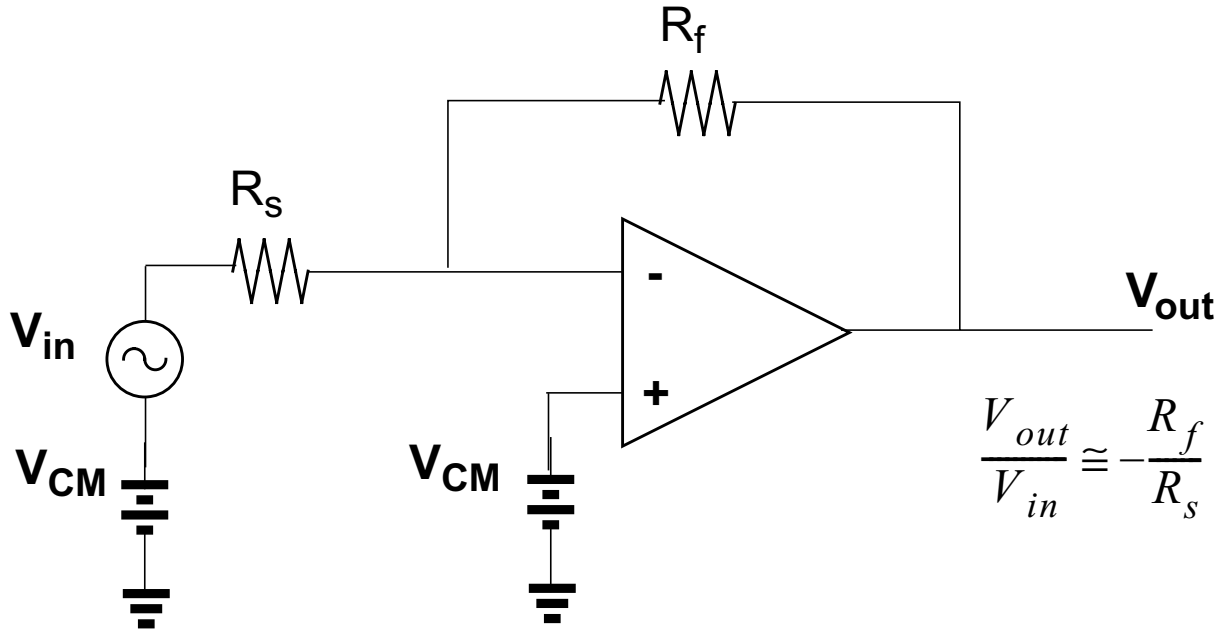
For low noise, increase g_{m1} , decrease g_{m3} , g_{m4} , g_{m5} , g_{m6} ,
i.e. increase their $V_{GS} - V_t$

This may affect stability -> trade-off

11.2.2 Resistive loads

Inverting voltage amplifier

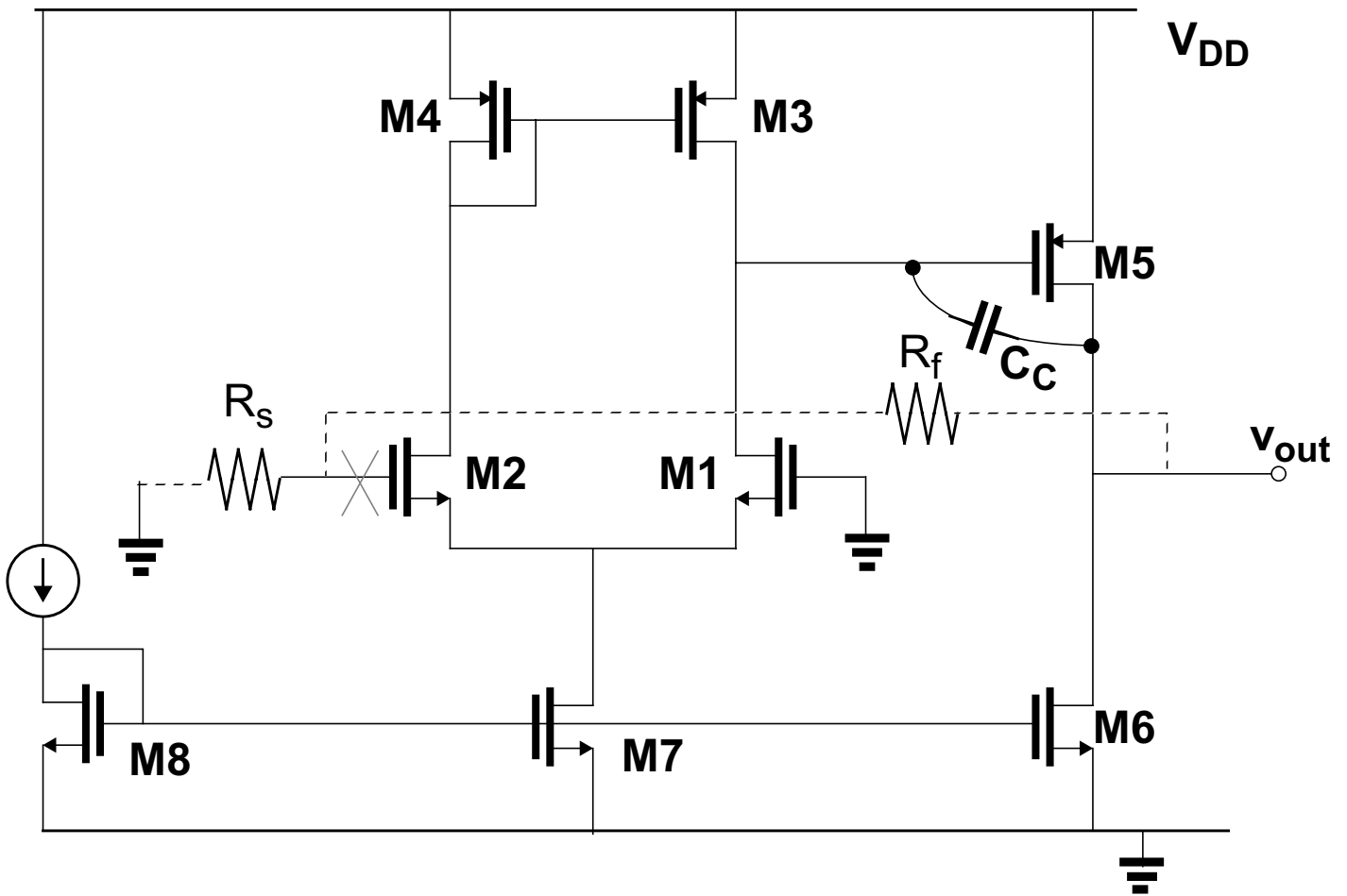
This is the configuration of choice for most basband gain stages, as the opamp input is at a fixed common-mode voltage



The feedback network forms a resistive load for the opamp.

The gain of the output stage of the opamp will be dominated by the load resistance.

For reasonable values of opamp gain, at least 2 stages are required in the opamp.



Loop Gain

The unloaded opamp gain is

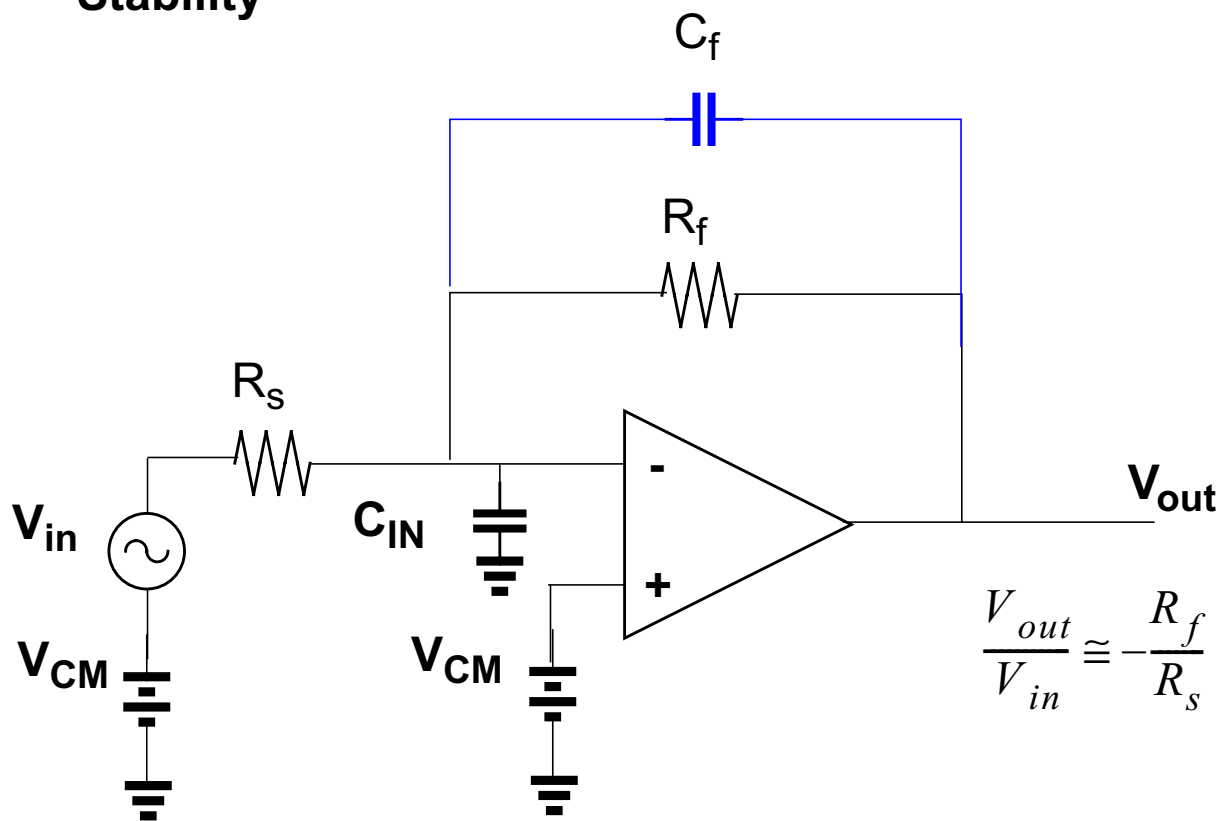
$$UnloadedGain = \frac{g_{m1}}{g_{ds1} + g_{ds3}} \cdot \frac{g_{m5}}{g_{ds5} + g_{ds6}}$$

However in the inverting amp the loop gain becomes

$$LoopGain = \frac{g_{m1}}{g_{ds1} + g_{ds3}} \cdot g_{m5}(R_f + R_s) \cdot \frac{R_s}{R_f + R_s}$$

$$LoopGain = \frac{g_{m1}}{g_{ds1} + g_{ds3}} \cdot g_{m5}R_s$$

Stability



The stability is complicated by:

1. Miller effect is weaker due to low gain of output stage

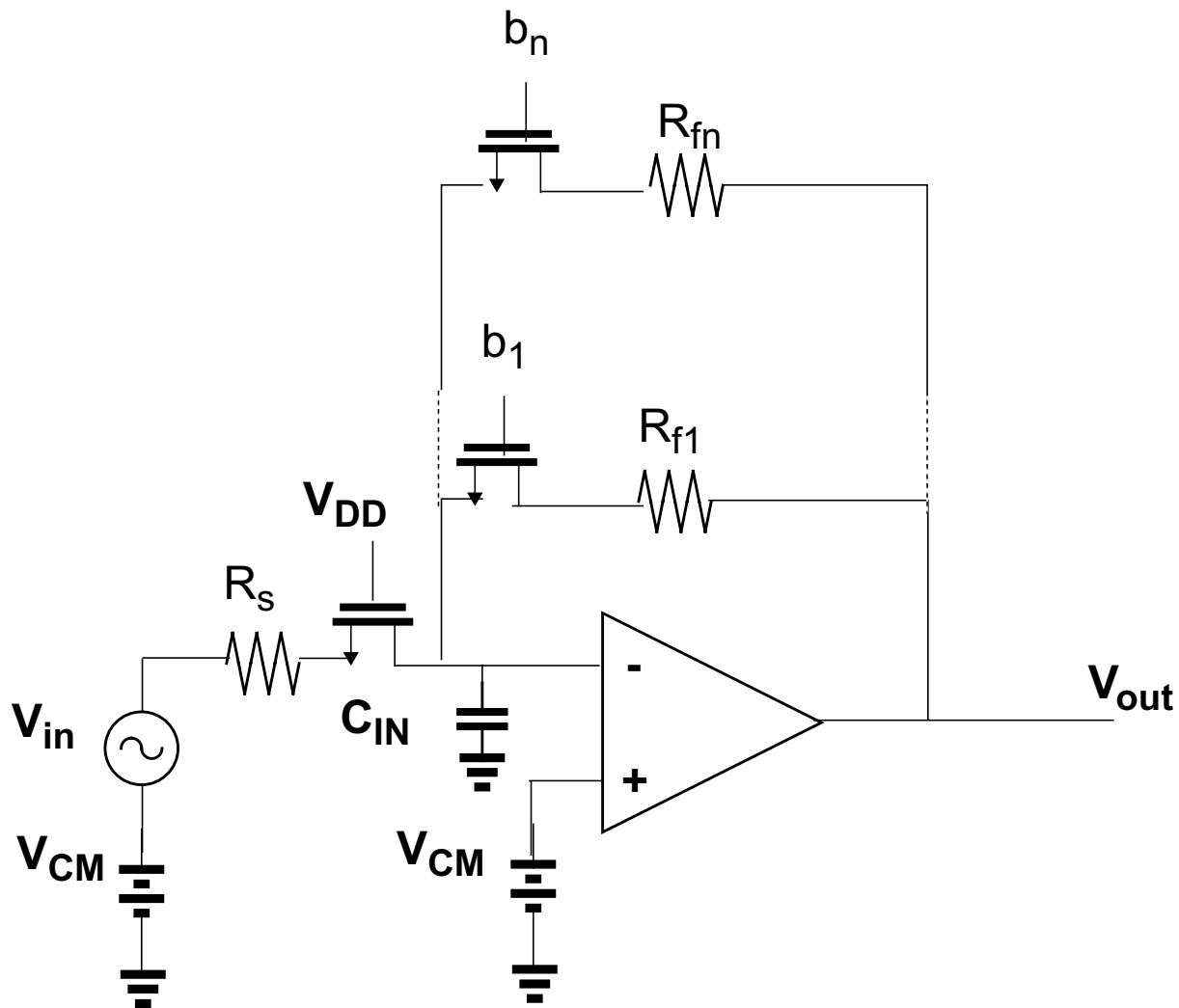
2. There is an additional pole in the loop due at $(R_s // R_f)C_{in}$, where C_{in} is the input capacitance of the opamp.

This pole is usually compensated by putting a capacitance in parallel with the feedback resistor.

This introduces a zero in the loop gain which cancels the pole at the input node.

However, this produces a pole in the closed-loop forward gain

$$\frac{V_{out}}{V_{in}} \cong -\frac{R_f}{R_s(1 + sR_fC_f)}$$



In addition variable gain is usually required

This is usually implemented by switching feedback resistance (keeps input resistance constant)

This changes the feedback factor and so the loop gain.

Lower gain makes stability more difficult.

As gain is switched it may also be necessary to change opamp Miller cap, and feedback cap for stability

Noise

Resistor noise contribution can be significant

In general, make resistors as high-value as you can get away with (from noise and stability point of view)

Low resistance => more power required.

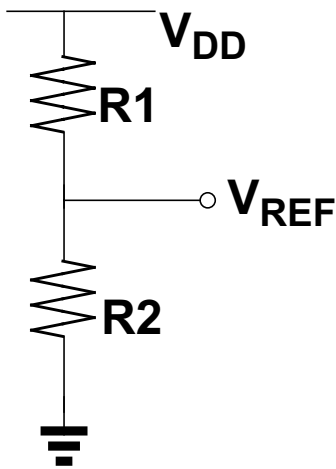
Recall also: high gain- R_s dominates input-referred noise.

12 Voltage and Current References

Simplest voltage references are derived from the power supply

12.1 Supply-dependent references

12.1.1 Resistive Voltage divider



$$V_{REF} = \frac{R_2}{R_1 + R_2} \cdot V_{DD}$$

Supply-dependent

Temperature-independent

Process-independent

Static Power consumption

Reduce power: increase R

=>increase area, output impedance

12.1.2 Resistor MOS Diode Voltage divider

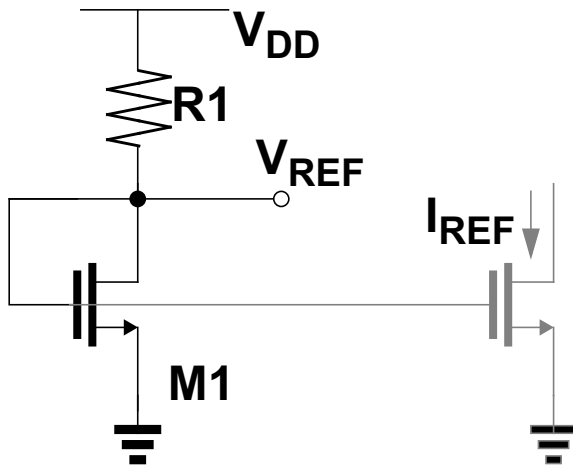
Voltage given by V_{gs} of M1

$$V_{REF} = V_t + \sqrt{\frac{2I_{D1}}{K'_n \frac{W}{L}}}$$

Decide on $I_{D1} \Rightarrow$ gives W/L , R_1

$$V_{REF} = V_t + \sqrt{\frac{2(V_{DD} - V_{REF})}{R_1 K'_n \frac{W}{L}}}$$

i.e Supply-dependent

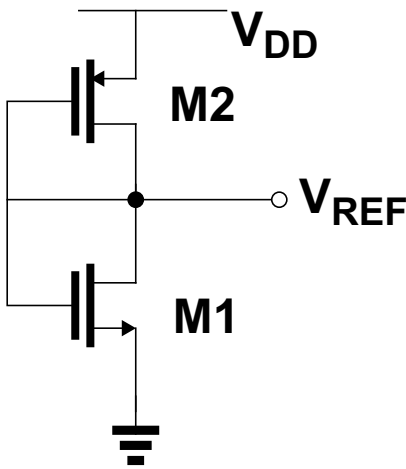


Temperature-dependent (V_t , K'_n , R_1)

Also used as current reference

12.1.3 MOS Diode Voltage divider

MOS Diode Voltage divider



Same current flows through M1, M2

$$\frac{K'_n \left(\frac{W}{L}\right)_1}{2} (V_{REF} - V_{tn})^2 = \frac{K'_p \left(\frac{W}{L}\right)_1}{2} (V_{DD} - V_{REF} - V_{tp})^2$$

$$\text{Let } \frac{K'_n \left(\frac{W}{L}\right)_1}{2} = \beta_n \quad \frac{K'_p \left(\frac{W}{L}\right)_2}{2} = \beta_p$$

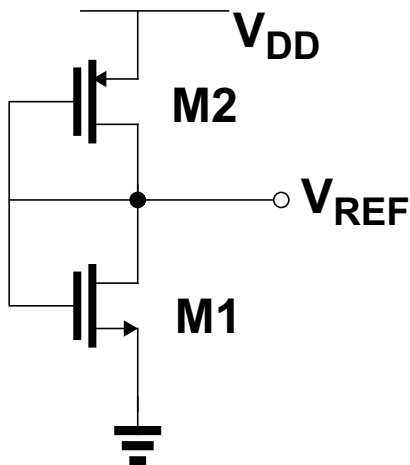
$$\frac{\beta_n}{2} (V_{REF} - V_{tn})^2 = \frac{\beta_p}{2} (V_{DD} - V_{REF} - V_{tp})^2$$

$$V_{REF} \left(\sqrt{\frac{\beta_n}{2}} + \sqrt{\frac{\beta_p}{2}} \right) = \sqrt{\frac{\beta_p}{2}} (V_{DD} - V_{tp}) + \sqrt{\frac{\beta_n}{2}} V_{tn}$$

$$V_{REF} \left(\sqrt{\frac{\beta_n}{2}} + \sqrt{\frac{\beta_p}{2}} \right) = \sqrt{\frac{\beta_p}{2}} (V_{DD} - V_{tp}) + \sqrt{\frac{\beta_n}{2}} V_{tn}$$

$$V_{REF} = \frac{\sqrt{\frac{\beta_p}{2}} (V_{DD} - V_{tp}) + \sqrt{\frac{\beta_n}{2}} V_{tn}}{\left(\sqrt{\frac{\beta_n}{2}} + \sqrt{\frac{\beta_p}{2}} \right)}$$

MOS Diode Voltage divider



$$V_{REF} = \frac{\sqrt{\frac{\beta_p}{2}}(V_{DD} - V_{tp}) + \sqrt{\frac{\beta_n}{2}}V_{tn}}{\left(\sqrt{\frac{\beta_n}{2}} + \sqrt{\frac{\beta_p}{2}}\right)}$$

$$V_{REF} = \frac{(V_{DD} - V_{tp}) + \sqrt{\frac{\beta_n}{\beta_p}}V_{tn}}{\left(\sqrt{\frac{\beta_n}{\beta_p}} + 1\right)}$$

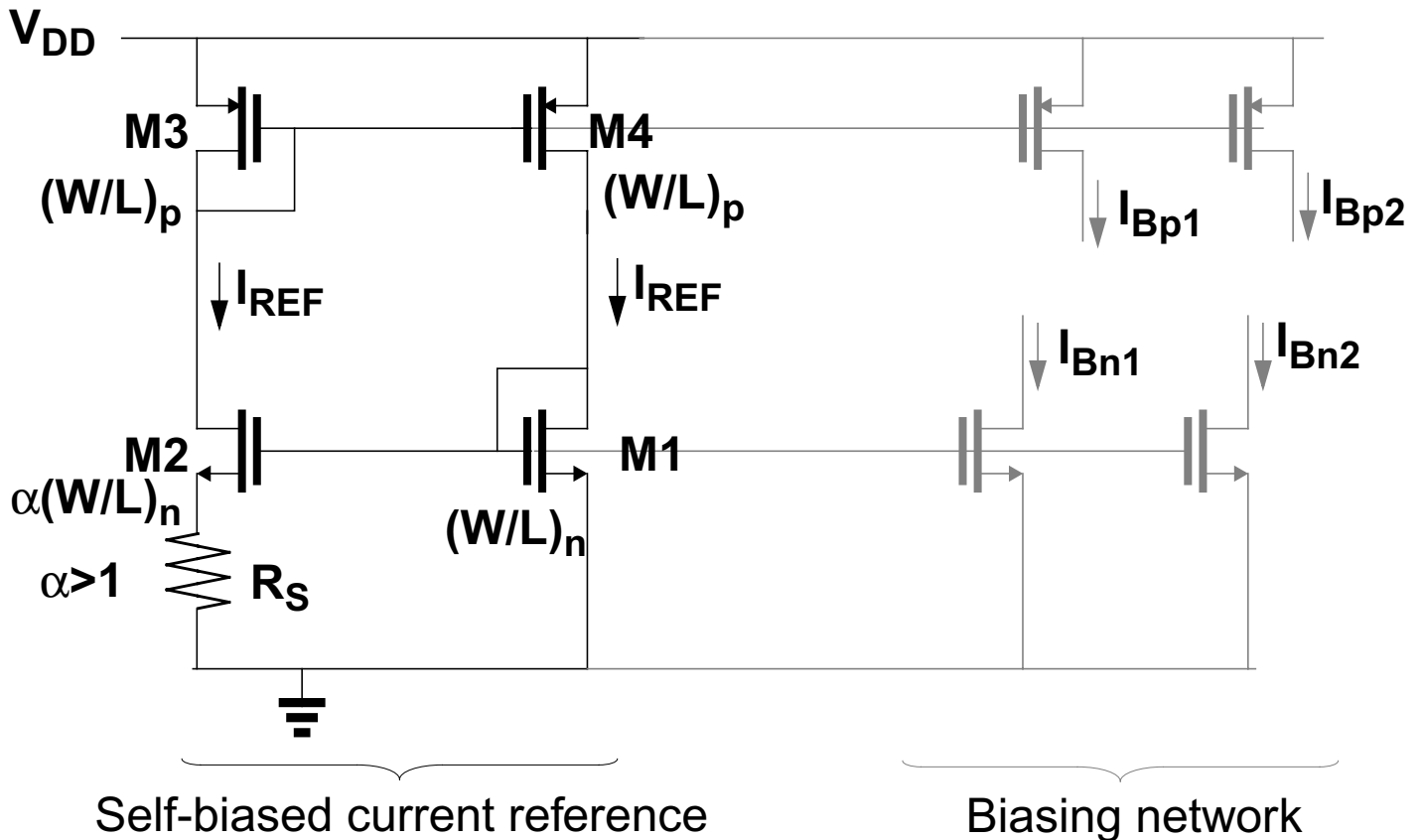
Or knowing required V_{REF} (and V_{tp} , V_{tn} , K_n' , K_p'),
can dimension W/L of M1 and M2

$$\sqrt{\frac{\beta_n}{\beta_p}}(V_{REF} - V_{tn}) = V_{DD} - V_{tp} - V_{REF}$$

$$\sqrt{\frac{\beta_n}{\beta_p}} = \frac{V_{DD} - V_{tp} - V_{REF}}{V_{REF} - V_{tn}}$$

12.2 Supply-independent references

12.2.1 Self-biased current reference



Neglecting body effect and output conductance:
pmos current mirror forces same current in left and right branches

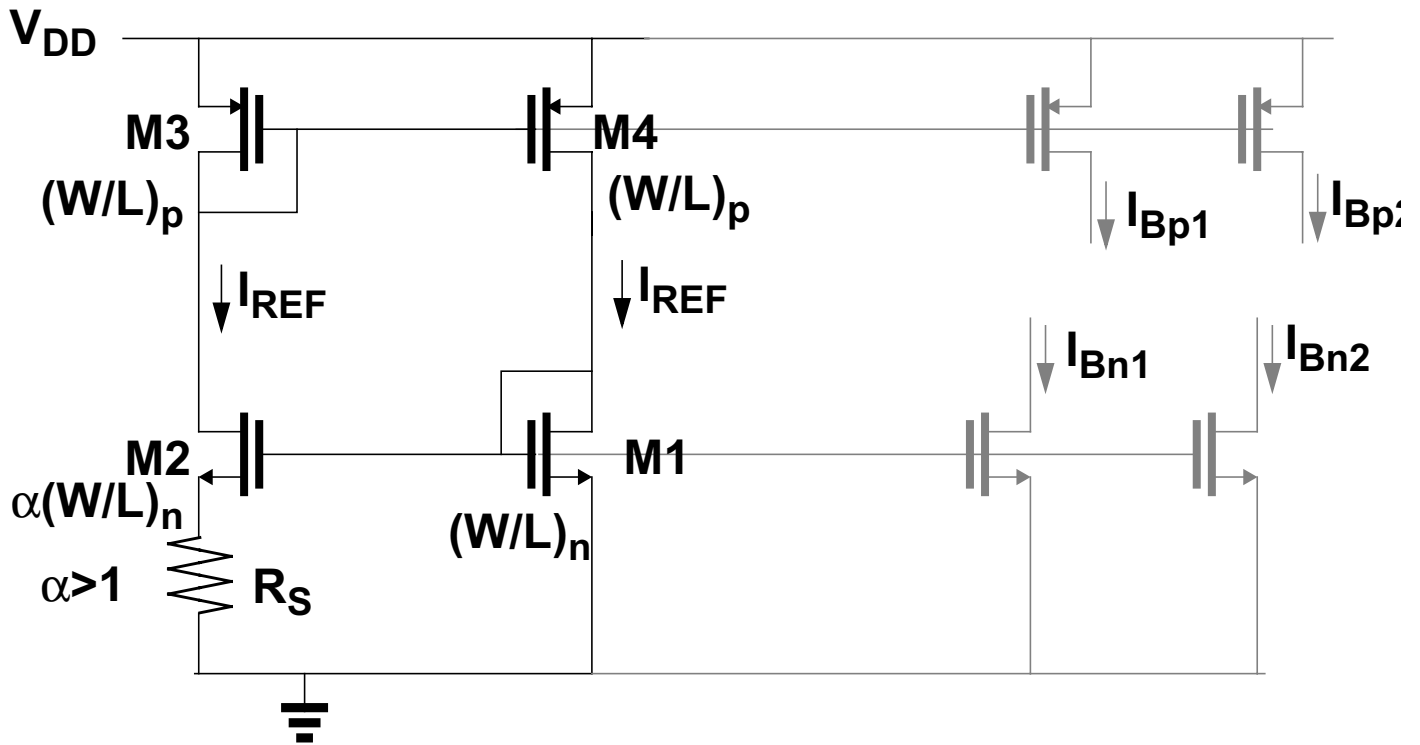
$$V_{GS1} = V_{GS2} + I_{REF}R_S$$

$$V_{tn} + \sqrt{\frac{2I_{REF}}{K'_n\left(\frac{W}{L}\right)_n}} = V_{tn} + \sqrt{\frac{2I_{REF}}{K'_n\alpha\left(\frac{W}{L}\right)_n}} + I_{REF}R_S$$

$$\sqrt{\frac{2I_{REF}}{K'_n\left(\frac{W}{L}\right)_n}}\left(1 - \frac{1}{\sqrt{\alpha}}\right) = I_{REF}R_S$$

$$I_{REF} = \frac{2}{K'_n\left(\frac{W}{L}\right)_n} \cdot \frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{\alpha}}\right)^2$$

12.2.2 Constant g_m biasing



$$\sqrt{\frac{2I_{REF}}{K'_n\left(\frac{W}{L}\right)_n}} \left(1 - \frac{1}{\sqrt{\alpha}}\right) = I_{REF}R_S$$

Re-writing :

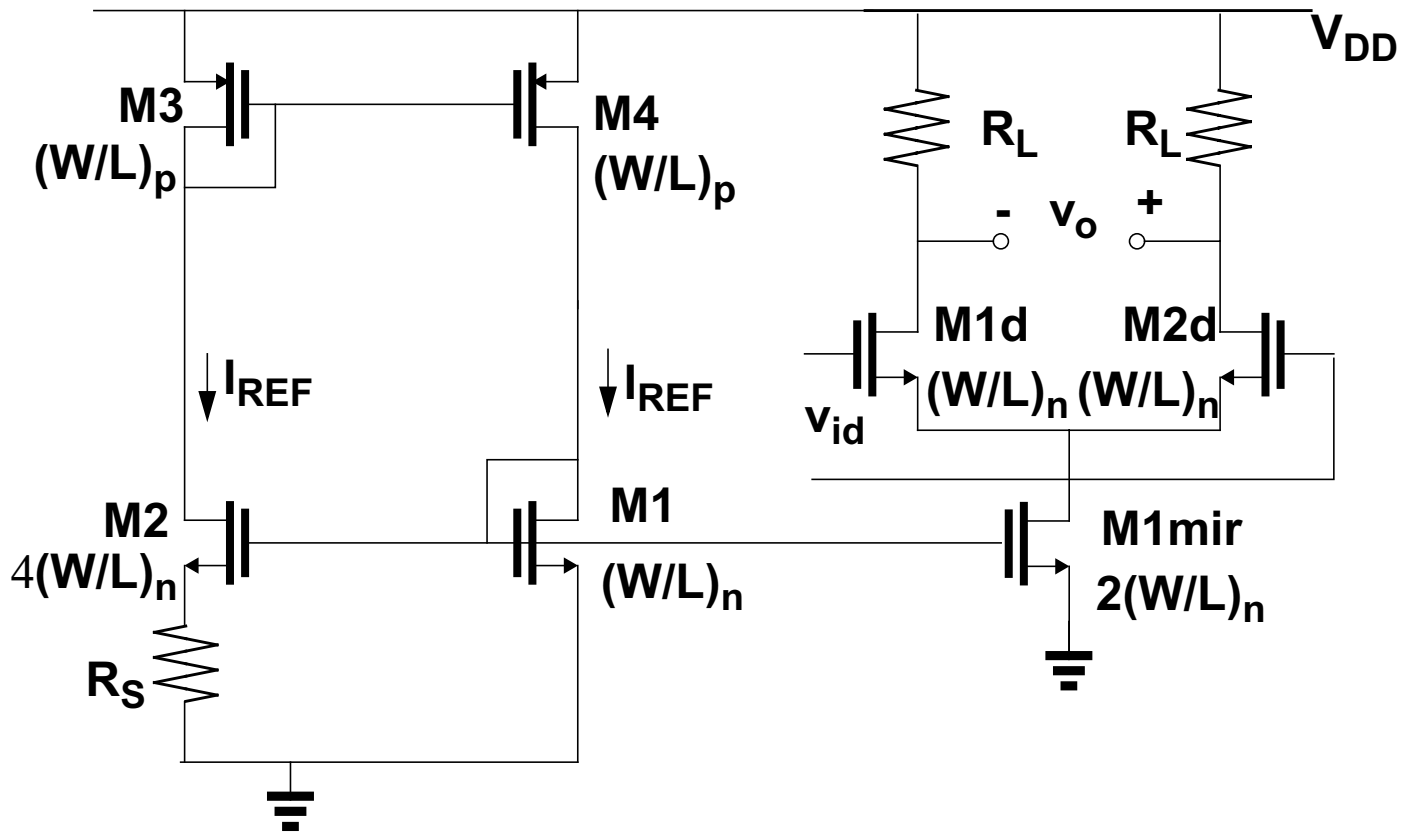
$$\frac{2\left(1 - \frac{1}{\sqrt{\alpha}}\right)}{R_S} = \underbrace{\sqrt{2K'_n\left(\frac{W}{L}\right)_n I_{REF}}}_{g_{m1}}$$

i.e. transconductance of M1 set by geometric ratio and R_S .

For the special case of $\alpha=4$ then

$$g_{m1} = \frac{1}{R_S}$$

Differential pair biased by constant g_m current



Set up tail current to be twice current through M1

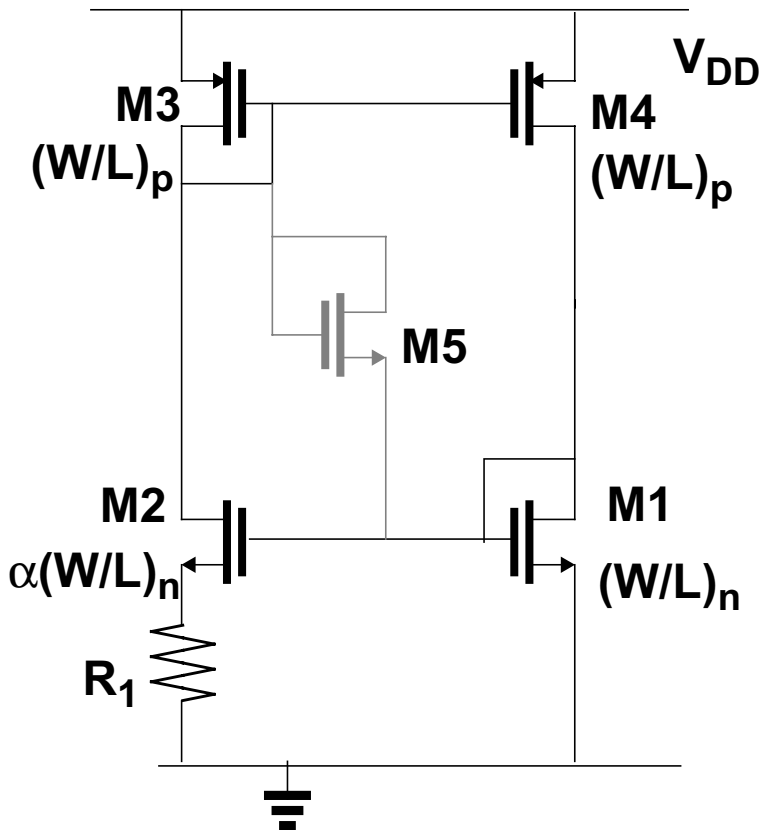
Gain of differential pair given (first order) by

$$Gain = g_{m1d} R_L$$

With M1d and M2d having same W/L, current as M1

$$Gain = \frac{1}{R_s} R_L = \frac{R_L}{R_s}$$

This technique is often used to reduce the spread of a gain stage over process, voltage and temperature



In general self-biased circuits have two possible operating currents- the desired value of I_{REF} and zero

Need to have a start-up circuit that will force the circuit to the desired operating point.

In the bias circuit above it is possible for the circuit to start up with the gates of M1 and M2 at ground potential and the gates of the PMOS transistors M3 and M4 at V_{DD} , so no current flows.

Various possibilities exist to force correct start-up e.g. using M5 as shown.

Now M3, M5 and M2 are 3 diodes in series from V_{DD} to ground and will pull down the gates of M3 and M4 and force the gate of M2 to a potential higher than ground, so M1 and M2 (and so also M3 and M4) cannot remain off.

Note M5 must be dimensioned carefully

To ensure proper start-up: $V_{t1} + V_{t5} + |V_{t3}| < V_{DD}$

Start-up circuit must turn off after circuit has reached proper bias point

$$V_{DD} - V_{GS1} - V_{GS3} < V_{t5}$$

12.3 Bandgap Voltage Reference

Often need to generate an accurate absolute voltage reference
e.g. to define an A/D converter range
or a specified output voltage signal.

Need to be (relatively) independent of temperature

However most process parameters are temperature-dependent.

To generate a temperature-independent reference:

Add a quantity with a positive temperature coefficient (TC) to a
quantity with a negative temperature coefficient.

Though MOS transistor parameters have both TC's which are both
positive (μ_n) and negative (V_t), bipolar transistors have proven to
give more reproducible and easily-defined positive and negative
TC's.

12.3.1 Negative Temperature coefficient Voltage

Recall: for bipolar transistors in active region

$$I_C = I_S \exp\left(\frac{V_{BE}}{\frac{kT}{q}}\right) \Rightarrow V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right)$$
$$\frac{kT}{q} \equiv V_T = 26mV \quad \text{at room temperature}$$

k = Boltzmann's constant = 1.38×10^{-23} J/K
 T = absolute temperature

I_S = scale current

$$I_S = \mu k T n_i^2 \quad \mu = \text{mobility of minority carriers}$$

n_i = intrinsic minority carrier concentration of Si

Temperature coefficient of these quantities:

$$\mu \propto \mu_0 T^m \quad m = -1.5$$

$$n_i^2 \propto T^3 \exp\left(\frac{-E_g}{kT}\right) \quad E_g = \text{bandgap energy of Silicon} = 1.12 \text{ eV}$$

$$I_S = b T^{m+4} \exp\left(\frac{E_g}{kT}\right)$$

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right) \equiv V_T \ln\left(\frac{I_C}{I_S}\right) = V_T [\ln(I_C) - \ln(I_S)]$$

$$\frac{\delta V_{BE}}{\delta V_T} = \frac{\delta V_T}{\delta T} \ln\left(\frac{I_C}{I_S}\right) + V_T \left(\frac{1}{I_C} \cdot \frac{\delta I_C}{\delta T} + \frac{1}{I_S} \cdot \frac{\delta I_S}{\delta T} \right)$$

Assumption: I_C constant with temperature

$$\frac{\delta V_{BE}}{\delta V_T} = \frac{\delta V_T}{\delta T} \ln\left(\frac{I_C}{I_S}\right) - \frac{V_T}{I_S} \cdot \frac{\delta I_S}{\delta T}$$

$$I_S = bT^{m+4} \exp\left(\frac{-E_g}{kT}\right)$$

$$\frac{\delta I_S}{\delta T} = b(m+4)T^{m+3} \exp\left(\frac{-E_g}{kT}\right) + bT^{m+4} \exp\left(\frac{-E_g}{kT}\right) \left(\frac{E_g}{kT^2}\right)$$

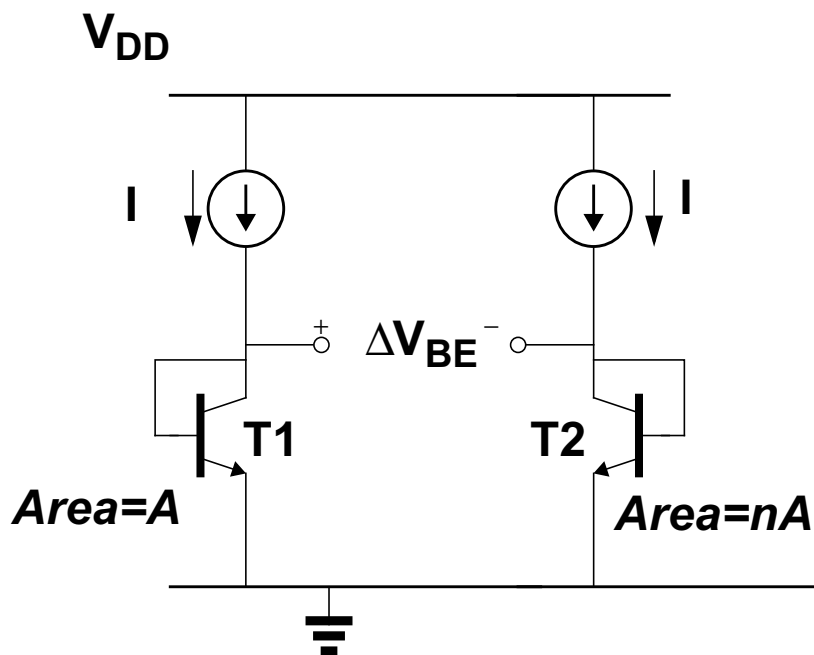
$$\frac{\delta I_S}{\delta T} = (m+4) \frac{I_S}{T} + I_S \left(\frac{E_g}{kT^2} \right)$$

$$\frac{\delta V_{BE}}{\delta V_T} = \frac{\delta V_T}{\delta T} \ln\left(\frac{I_C}{I_S}\right) - (m+4) \frac{V_T}{T} - V_T \left(\frac{E_g}{kT^2} \right)$$

$$= \frac{V_{BE} - (m+4)V_T - \frac{E_g}{q}}{T}$$

For $V_{BE} = 750\text{mV}$, $T=300^\circ\text{K}$: $\delta V_{BE}/\delta T = -1.5\text{mV}/^\circ\text{K}$

12.3.2 Positive Temperature coefficient Voltage



If two transistors have different current densities then difference in their V_{BE} s is proportional to absolute temperature

$$V_{BE1} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right) \quad V_{BE2} = \frac{kT}{q} \ln\left(\frac{I_C}{nI_S}\right)$$

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right) - \frac{kT}{q} \ln\left(\frac{I_C}{nI_S}\right)$$

$$\Delta V_{BE} = \frac{kT}{q} \ln(n)$$

$$\frac{\delta \Delta V_{BE}}{\delta T} = \frac{k}{q} \ln(n) \quad \text{positive temperature coefficient}$$

$$= 0.087 \text{ mV}/^\circ\text{K} \times \ln(n)$$

12.3.3 Zero Temperature-Coefficient Voltage

Want to develop a voltage reference with zero TC.
Find a way to balance the positive and negative TCs.

$$V_{REF} = V_{BE} + \alpha \frac{kT}{q} \ln(n)$$

Negative TC $\frac{\delta V_{BE}}{\delta V_T} = -1.5 mV/^{\circ}K$

Positive TC $\frac{\delta \left(\frac{kT}{q} \right)}{\delta T} \ln(n) = 0.087 mV/^{\circ}K \times \ln(n)$

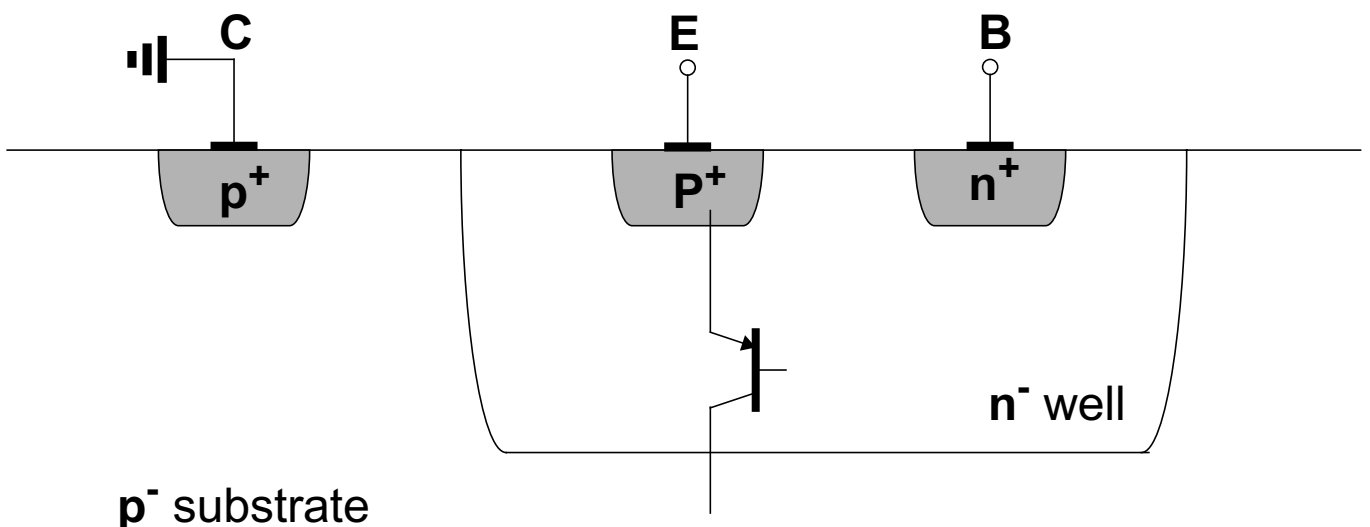
For zero TC V_{REF} need

$$\alpha \ln(n) \approx 17.2$$

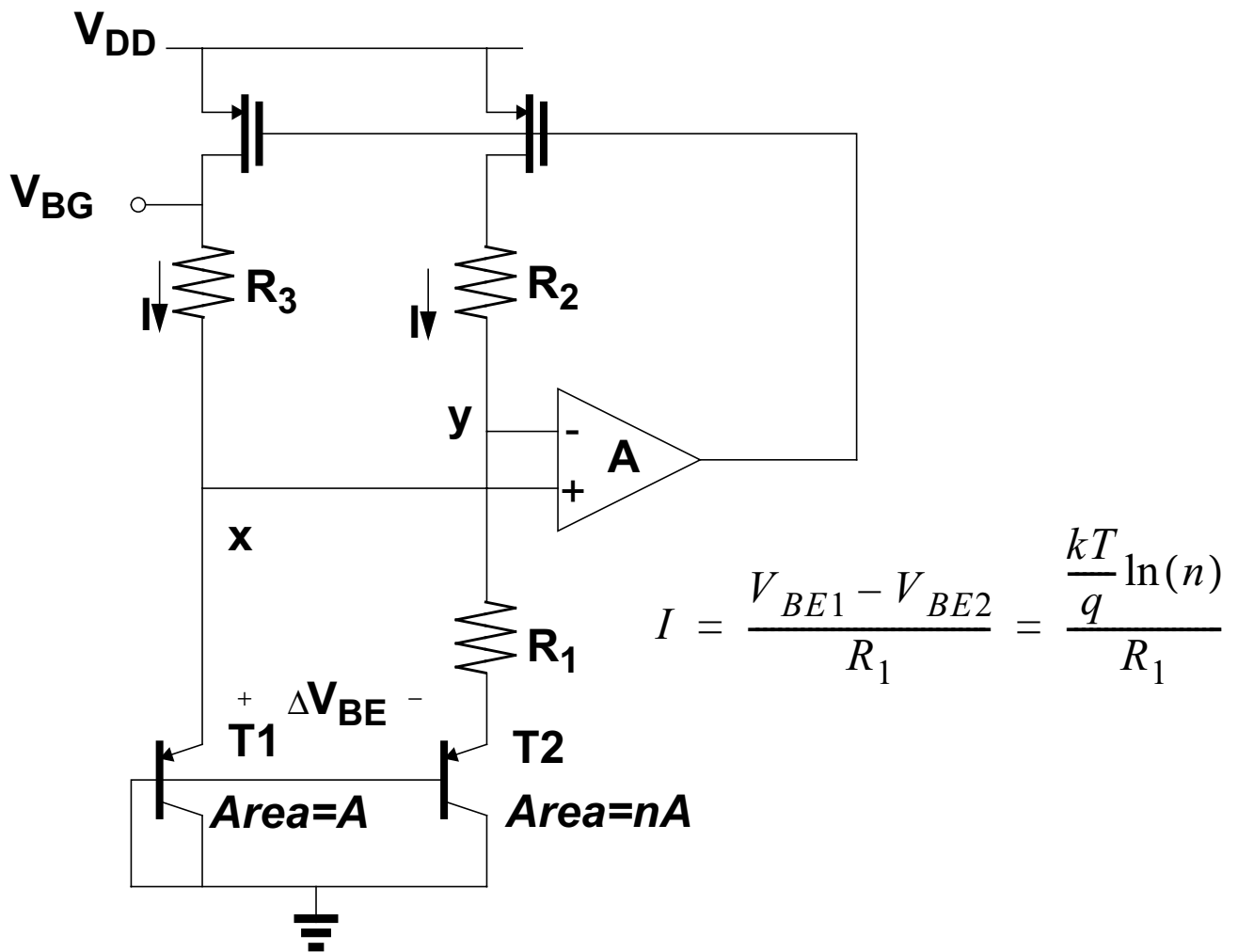
This gives

$$V_{REF} = V_{BE} + 17.2 \frac{kT}{q} \approx 1.25 V$$

Recall that standard CMOS has a bipolar transistor available - a pnp with the collector tied to the substrate.



12.3.4 Bandgap Voltage Reference circuit



$$V_x = V_y$$

$$V_{BG} = V_{BE1} + IR_3 = V_{BE1} + \left(\frac{\Delta V_{BE}}{R_1} \right) R_3$$

$$V_{BG} = V_{BE1} + \frac{kT}{q} \ln(n) \frac{R_3}{R_1}$$

For zero TC V_{REF} need $\left(\frac{R_3}{R_1} \right) \ln(n) \approx 17.2$

e.g $n=24 \Rightarrow R_3/R_1=5.4$

or $n=35 \Rightarrow R_3/R_1=4.8$

12.3.5 Bandgap design issues

1. Opamp

Differential to single-ended folded cascode would be suitable

2. Stability

Opamp output node has relatively high impedance, so dominant pole is at output of opamp.

May need to add some capacitance at this node to guarantee stability.

3. Offset

Offset is important as the input-referred offset of the opamp is gained up by the ratio of R_3/R_1 . A large random offset would add to the variation in bandgap output voltage over process.

$$V_{BG} = V_{BE1} + IR_3 = V_{BE1} + \left(\frac{\Delta V_{BE} + V_{OS}}{R_1} \right) R_3$$

Similarly for the current mismatch from the PMOS mirror and the pnp mismatch.

4. Noise

May be critical, depending on the application.

The input-referred offset of the opamp is also gained up by the ratio of R_3/R_1 .

5. Start-up

The circuit could start up with zero current through the pnps, and a start-up circuit may need to be added e.g. to pull the output of the opamp low to get current flowing through the pnps

6. Temperature dependence of collector current

Our derivation of $\delta V_{BE}/\delta T$ assumed collector current I_C independent of temperature

But in previous circuit
$$I_C = \frac{\frac{kT}{q} \ln(n)}{R_2} \equiv \frac{V_T \ln(n)}{R_2}$$

$$\frac{\delta I_C}{\delta T} = \frac{V_T}{T} \cdot \frac{\ln(n)}{R_2} = \frac{I_C}{T}$$

$$\frac{\delta V_{BE}}{\delta V_T} = \frac{\delta V_T}{\delta T} \ln\left(\frac{I_C}{I_S}\right) + V_T \left(\frac{1}{I_C} \cdot \frac{\delta I_C}{\delta T} + \frac{1}{I_S} \cdot \frac{\delta I_S}{\delta T} \right)$$

$$\frac{\delta V_{BE}}{\delta V_T} = \frac{\delta V_T}{\delta T} \ln\left(\frac{I_C}{I_S}\right) + \frac{V_T}{T} - \frac{V_T}{I_S} \cdot \frac{\delta I_S}{\delta T}$$

$$\frac{\delta V_{BE}}{\delta V_T} = \frac{V_{BE} - (m+3)V_T - \frac{E_g}{q}}{T}$$

$$\Rightarrow : \delta V_{BE}/\delta T$$

slightly less than $-1.5\text{mV}/^\circ\text{K}$

In general pnp temperature model accuracy can be an issue.

Note: Over temperature, process can achieve $\pm 1\text{-}2\%$ accuracy, neglecting random offset (which will add another $1\text{-}2\%$).

Appendix A Bipolar-Junction Transistors (BJT)

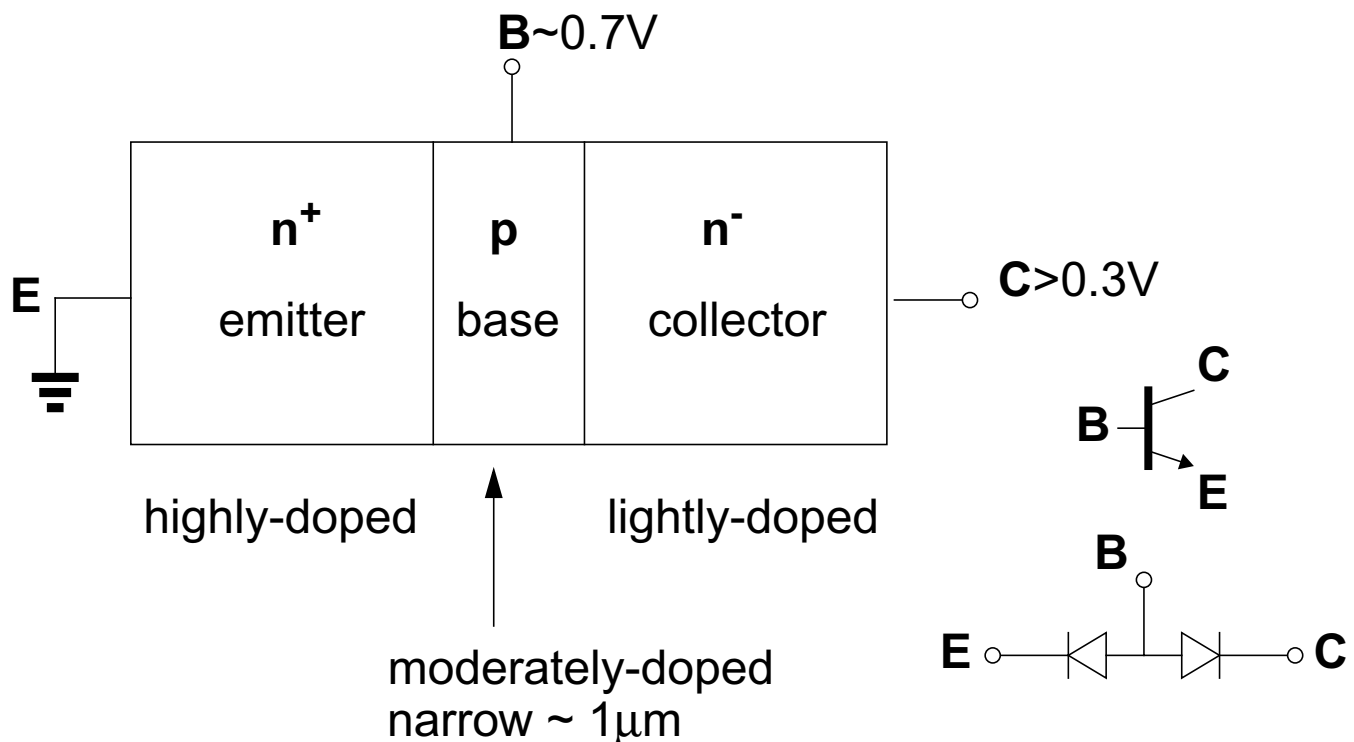
Dominant technology in electronics up to 1970's

Dominant analog technology into 1980's

Still used for high-speed applications (factor 10 higher speed than CMOS of similar resolution).

BiCMOS often preferred for mixed-signal designs.

nnp transistor



In normal operation

Base-emitter diode is forward biased

Base-collector diode is reverse biased

With forward biased base-emitter junction:

+ve majority carriers (holes) in base flow to emitter

-ve majority carriers (electrons) in emitter flow to base

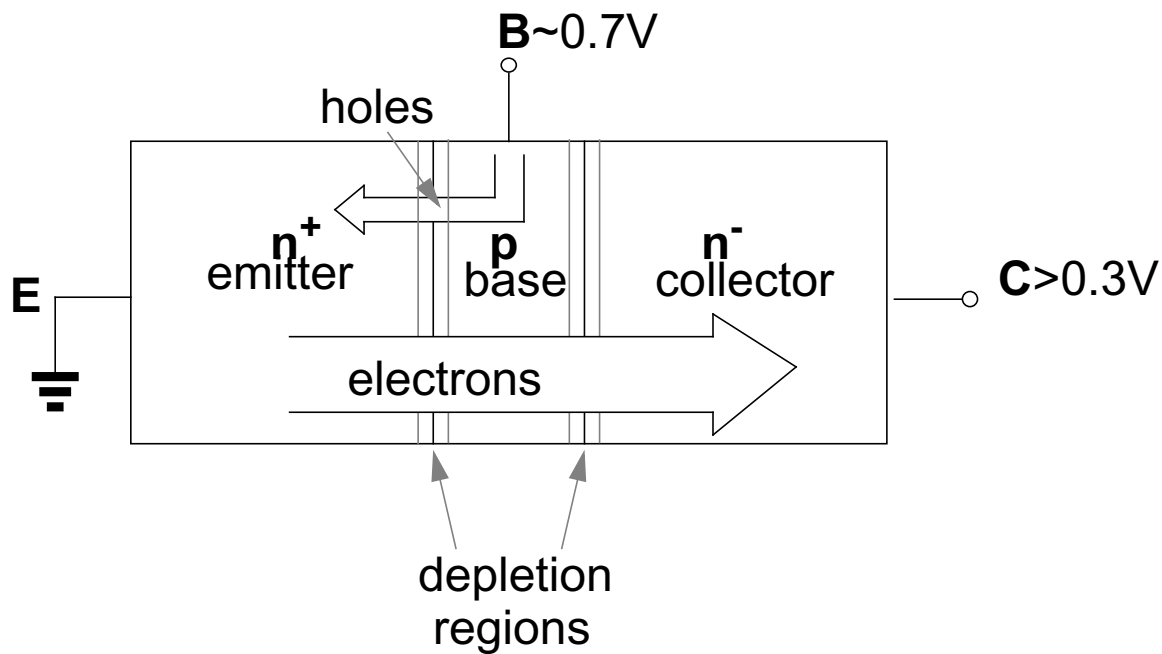
Emitter is more heavily doped than base so

electron flow to base is stronger than flow of holes from base

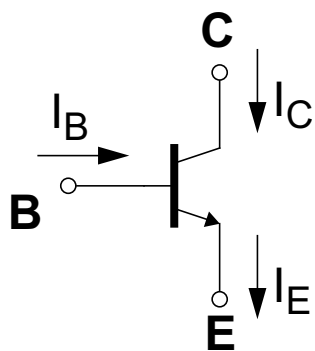
electrons (minority carriers) in base diffuse across base

If they get close to positively charged collector they are swept across reverse-biased base-collector junction.

$$I_E = I_B(\text{small}) + I_C(\text{large})$$



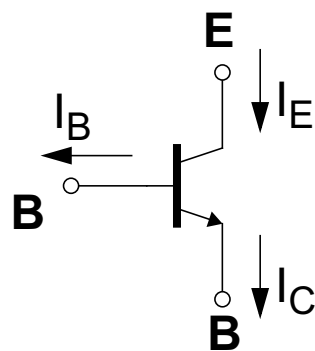
Symbols



npn

$$I_C = \beta I_B$$

$$\beta = 100 \text{ typical}$$

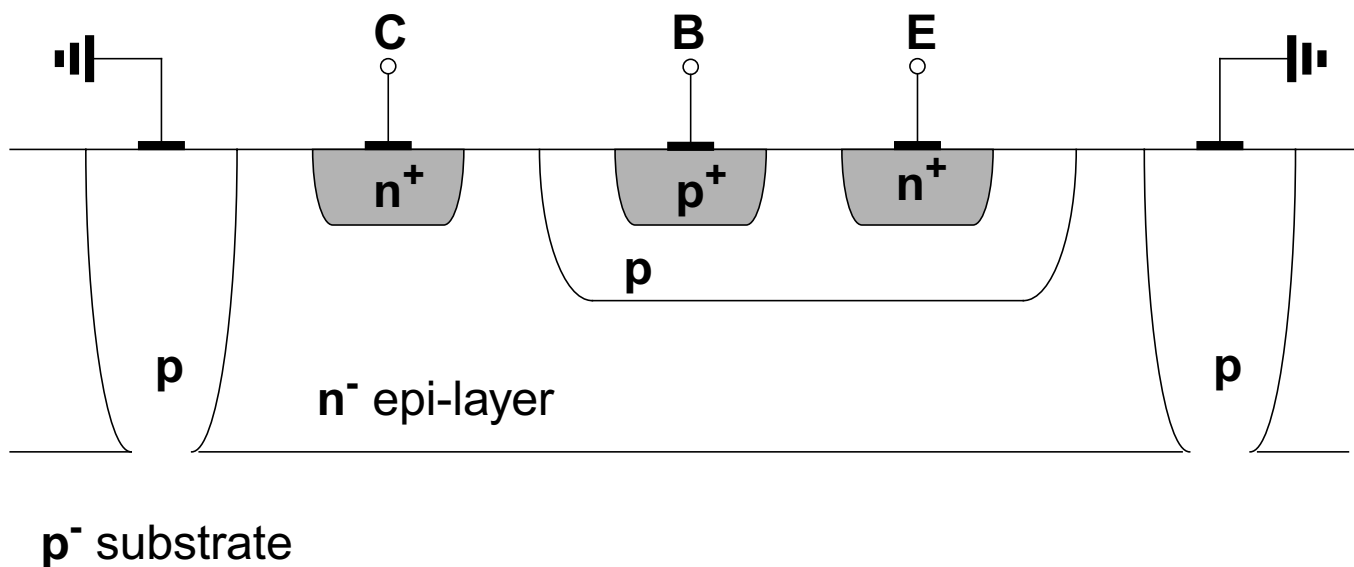


pnp

$$I_C = \beta I_B$$

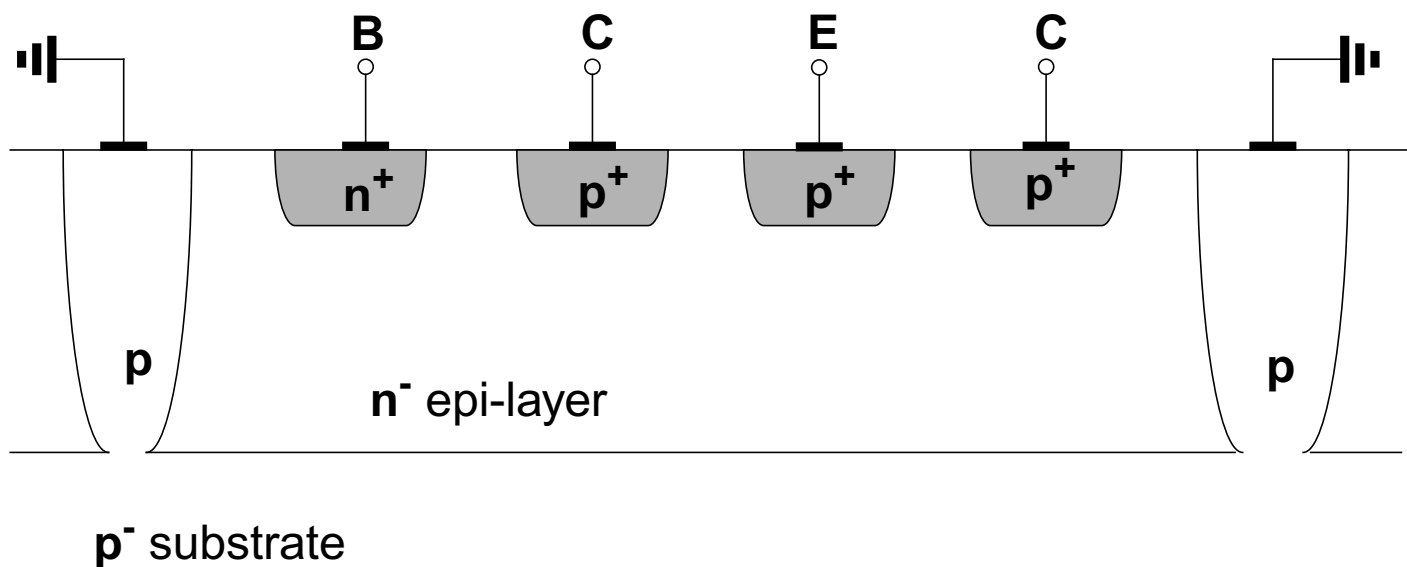
$$\beta = 20 \text{ typical}$$

Standard bipolar process: npn



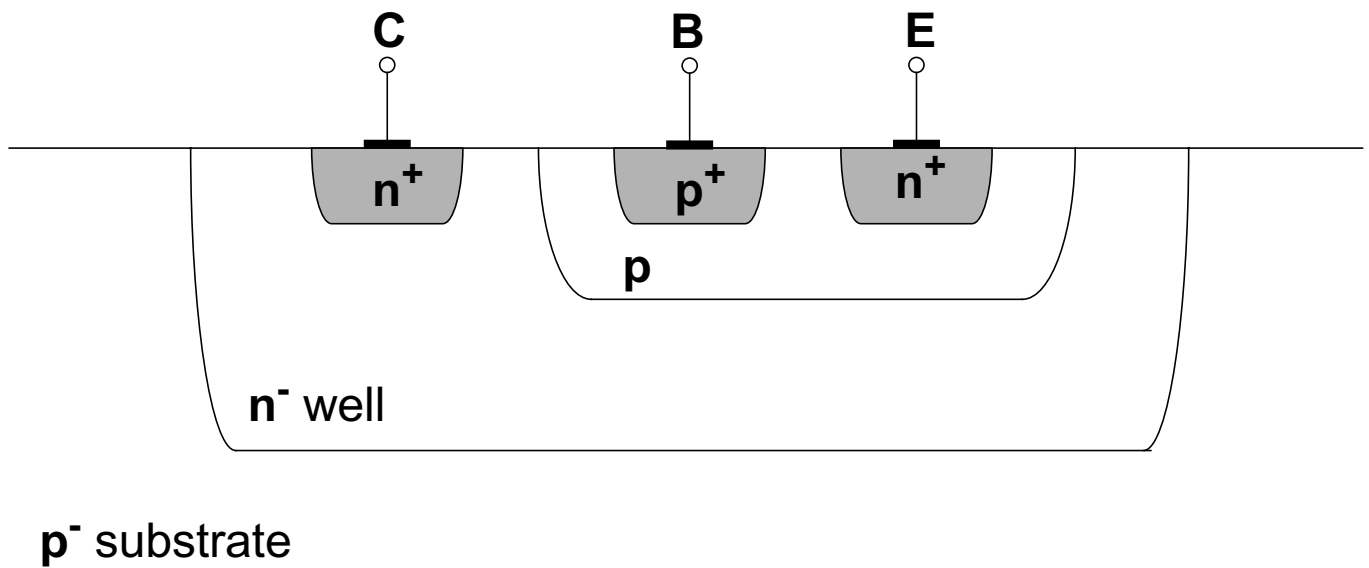
Note difficulty in isolating components

lateral pnp

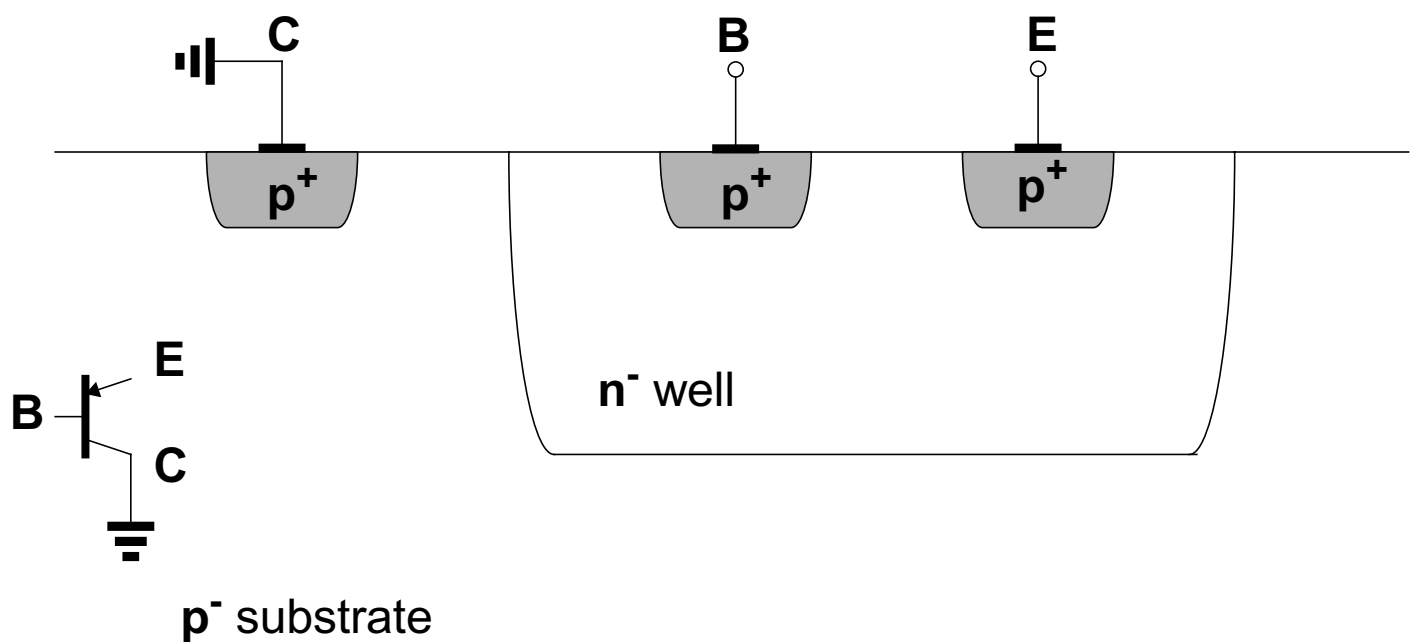


Bipolar in CMOS processes

Bipolar can be added to standard CMOS (one extra layer)



Standard CMOS does have a bipolar (pnp) available without any modifications



In this construction collector is connected to most negative supply

Large-signal behaviour of BJT

Device equations

$$I_C = I_{CS} \exp\left(\frac{V_{BE}}{\frac{kT}{q}}\right) \quad \frac{kT}{q} \equiv V_T = 26mV \text{ at room temperature}$$

k = Boltzmann's constant

T = absolute temperature

q = electron charge

I_{CS} = scale current (prop. to BE junction)

$$I_C = I_{CS} \exp\left(\frac{V_{BE}}{V_T}\right)$$

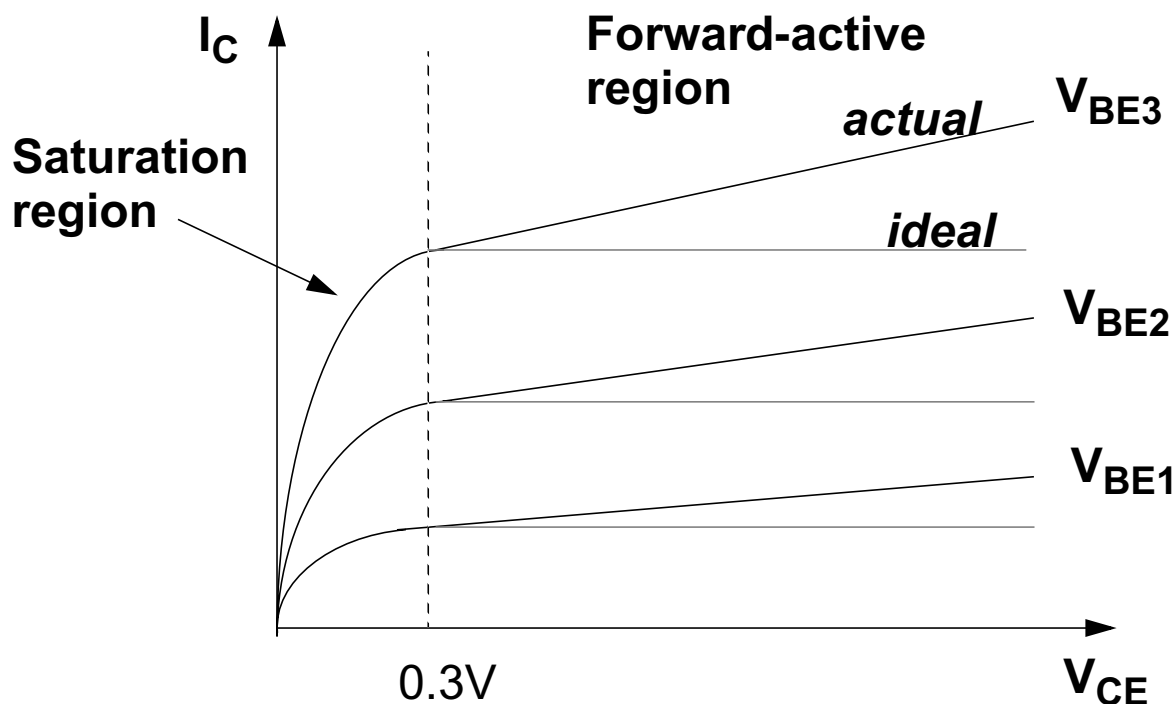
$$I_C = \beta I_B$$

Note exponential increase in I_C with I_B .

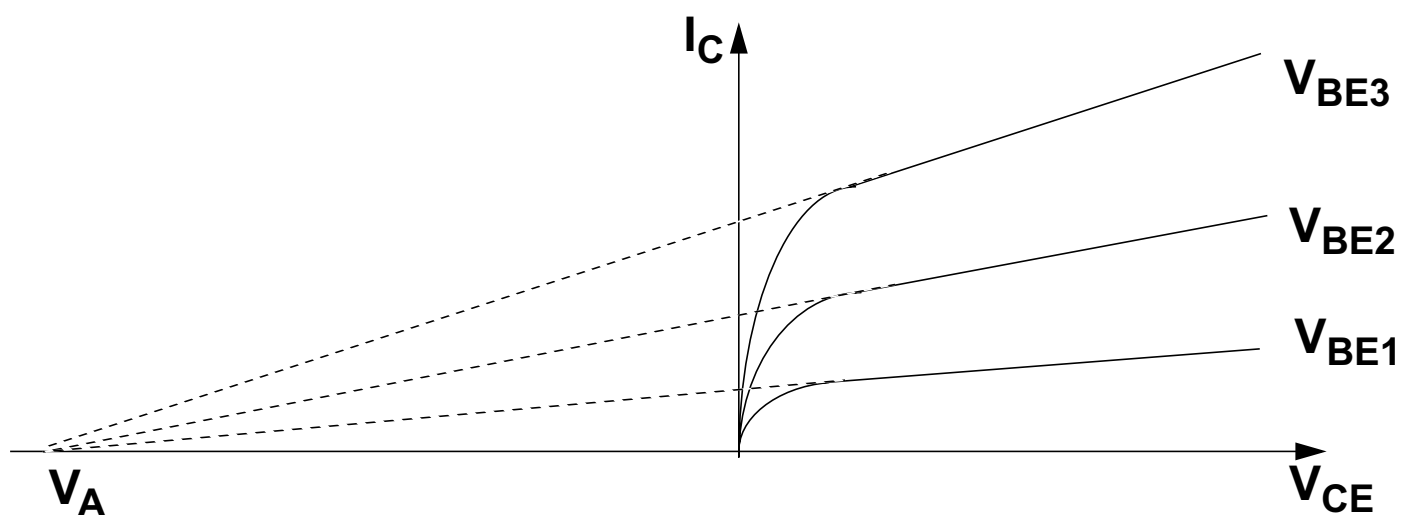
Equation implies a collector current is independent of the collector voltage.

But as collector voltage increases, collector-base depletion area increases, decreasing the effective base width and causing an increase in I_C

=> finite output impedance(as in MOS). Also known as Early effect.



$$I_C = I_{CS} \exp\left(\frac{V_{BE}}{V_T}\right) \left(1 + \frac{V_{CE}}{V_A}\right) \quad V_A = \text{Early voltage } (\sim 50V)$$



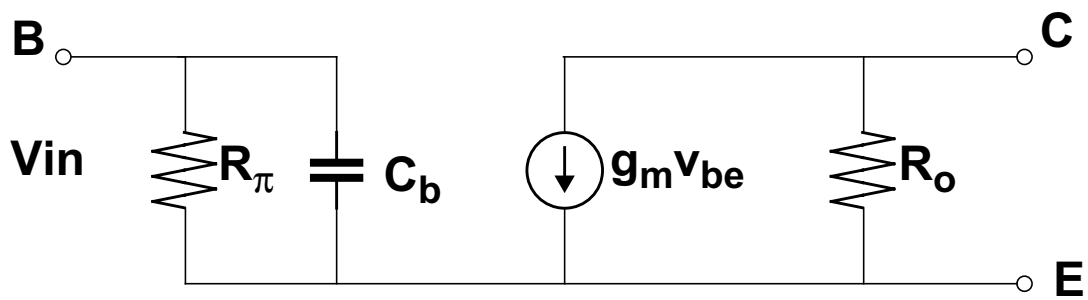
Normally operated in forward-active region

If the collector voltage is lowered such that the base-collector diode starts to turn on the transistor is said to enter saturation

This happens once V_{BC} goes above 0.4V (i.e. with $V_{BE}=0.7V$ when V_{CE} is goes under 0.3V)

In practice try to keep $V_{BC} < 0.2V$

Small Signal model of BJT



Transconductance g_m

Change in collector current when base-emitter voltage is changed

$$\begin{aligned} g_m &= \frac{\delta I_C}{\delta V_{BE}} \\ &= \frac{\delta I_{CS} e^{V_{BE}/V_T}}{\delta V_{BE}} \\ &= \frac{1}{V_T} I_{CS} e^{V_{BE}/V_T} \equiv \frac{I_C}{V_T} \quad V_T = \frac{kT}{q} = 26mV \text{ at room temperature} \\ g_m &= \frac{I_C}{V_T} \end{aligned}$$

Output resistance r_o

Change in collector current when collector-emitter voltage is changed

$$\frac{1}{r_o} = \frac{\delta I_C}{\delta V_{CE}} \quad \text{Use } I_C = I_{CS} e^{V_{BE}/V_T} \left(1 + \frac{V_{CE}}{V_A} \right)$$

$$\frac{\delta I_C}{\delta V_{CE}} = I_{CS} e^{V_{BE}/V_T} \left(\frac{1}{V_A} \right) = \frac{I_C}{V_A}$$

$$r_o = \frac{V_A}{I_C}$$

Input resistance r_π

Input resistance due to base current:

Change in base current when base-emitter voltage is change

Base-charge storage capacitance

When BJT in forward-active region: many minority carriers in base

These carriers are in transit to the collector (responsible for I_C)

For a transistor to turn off this charge must be removed via the base contact.

Can be modelled as a capacitance:

$$\frac{1}{r_{\pi}} = \frac{\delta I_B}{\delta V_{BE}}$$

$$I_B = \frac{I_C}{\beta} = \frac{I_{CS}}{\beta} e^{V_{BE}/V_T}$$

$$\frac{\delta I_B}{\delta V_{BE}} = \frac{1}{V_T} \frac{I_{CS}}{\beta} e^{V_{BE}/V_T} = \frac{I_B}{V_T}$$

$$r_{\pi} = \frac{V_T}{I_B}$$

$$r_{\pi} = \frac{\beta V_T}{I_C}$$

$$r_{\pi} = \beta g_m$$

$$c_b = \tau_b \frac{I_C}{V_T} \quad \tau_b = \text{base-transit-time constant}$$

proportional to square of diffusion length

inv. proportional doping level

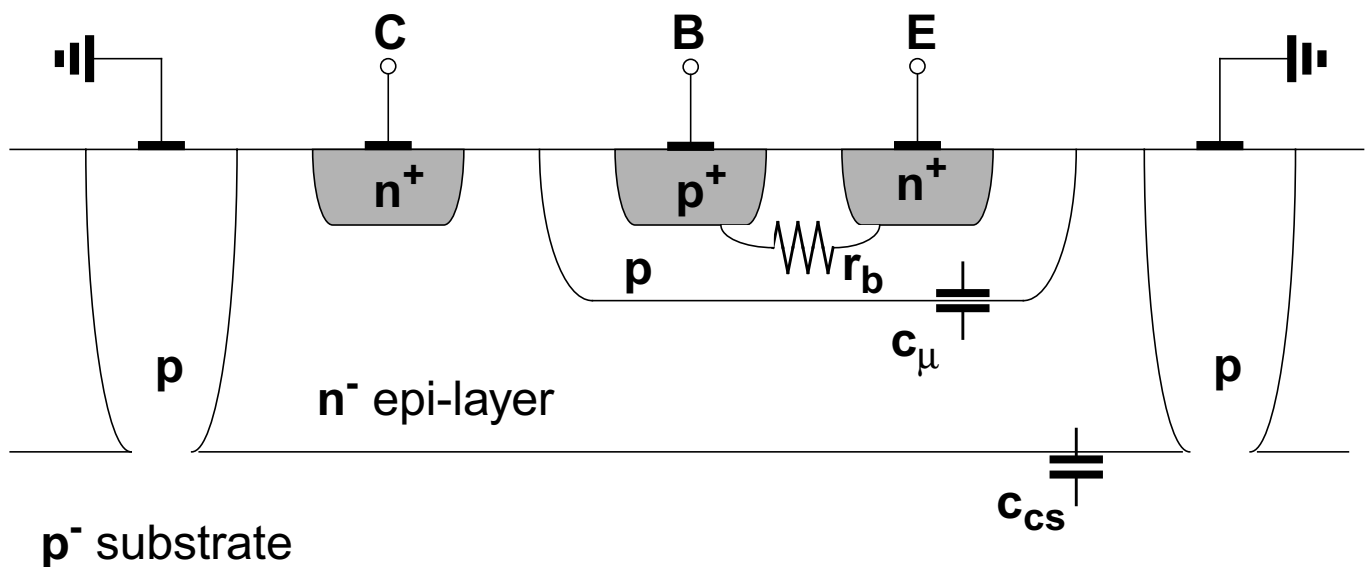
= 10-500ps for a good npn

Note that when a BJT enters saturation i.e. when the base-collector junction become forward biased, carriers from the base diffuse into the lightly doped collector.

Removing this charge takes orders of magnitude longer than removing base charge

High speed bipolar design - never allow transistors to saturate.

Parasitics

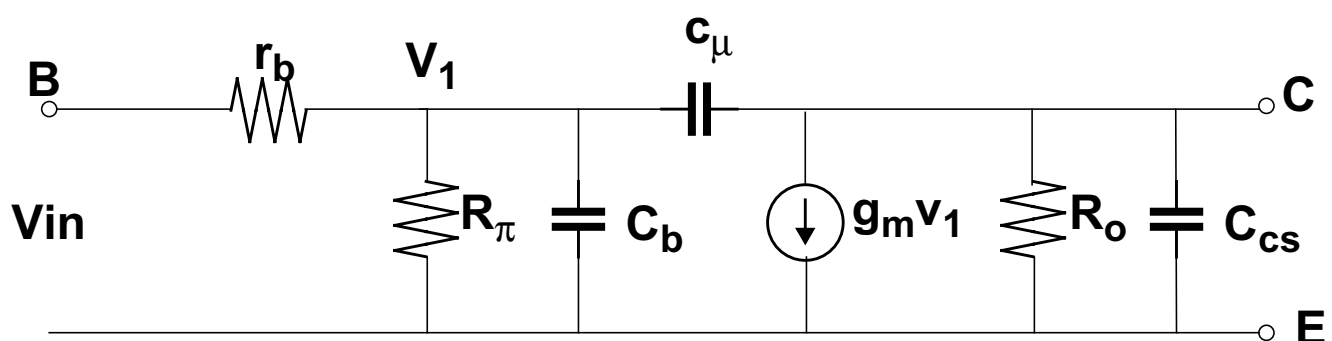


r_b = base series resistance ($\sim 1\text{k}\Omega$)

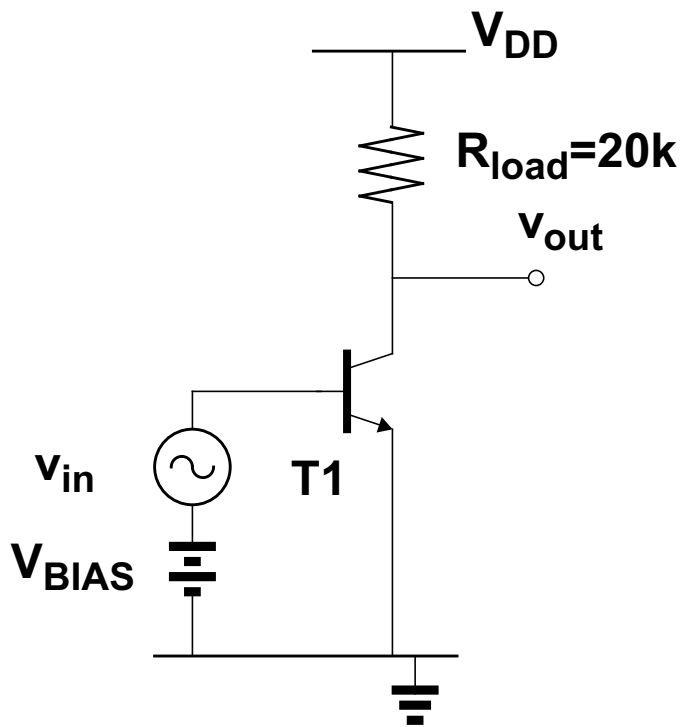
c_μ = basecollector capacitance

c_{cs} = collector-substrate capacitance

Small-signal equivalent circuit with capacitances



Example

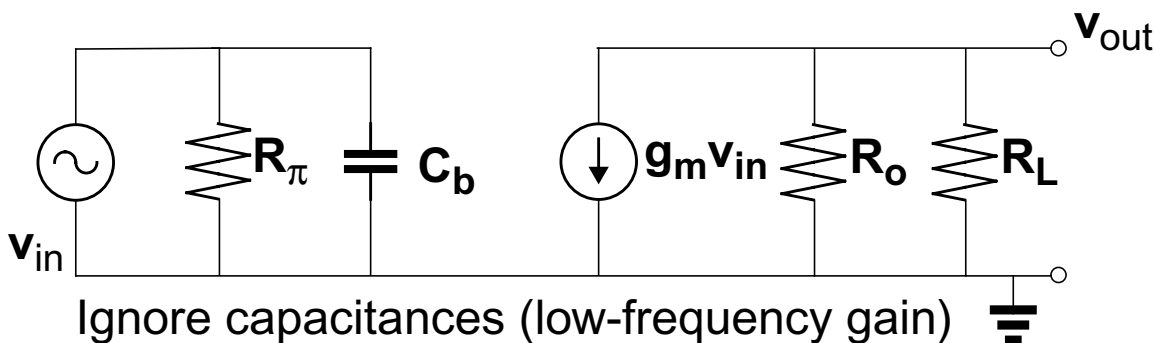


Assume V_{BIAS} sets up a quiescent current of $100\mu A$ through collector

$V_A = 50V$.
Neglect r_b

What is the small-signal low-frequency gain?

Small signal equivalent circuit



Ignore capacitances (low-frequency gain)

Assume v_{in} is ideal $\Rightarrow r_\pi$ has no effect

$$g_m v_{in} = -v_{out} (R_L \parallel r_o)$$

$$g_m = \frac{I_C}{V_T} = \frac{100\mu A}{26mV} = 3.8mA/V$$

$$r_o = \frac{V_A}{I_C} = \frac{50V}{100\mu A} = 500k\Omega$$

$$\frac{v_{out}}{v_{in}} \approx -g_m R_L = -3.8mA/V \times 20k\Omega = -76$$

Compare with MOS version running of the same current
Gain of -8