UE4002 Autumn 2006

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an NMOS in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.
In each question, capacitances other than those mentioned may be ignored.

Question 1

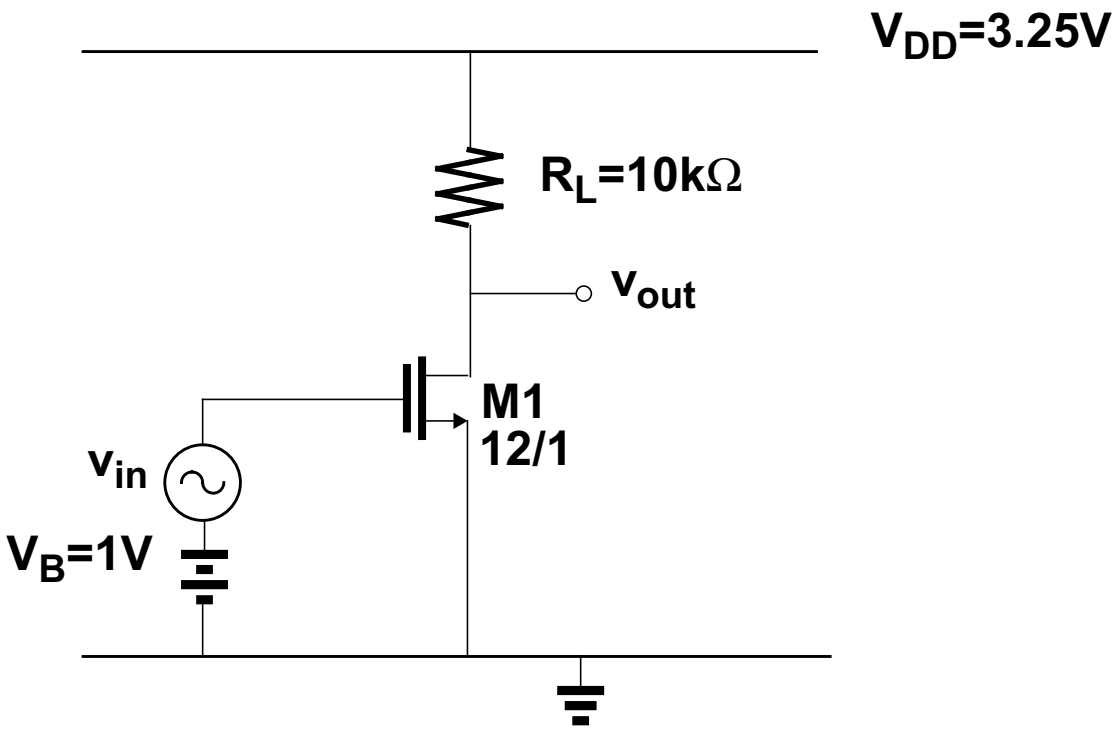

Figure 1

Figure 1 shows a common-source stage with a resistive load.
Biasing and component values are as shown in Figure 1.
Take $K_n'=200\mu A/V^2$, V_{tn} = 0.75V.

(i) Draw the small-signal equivalent circuit for the circuit shown in Figure 1.

(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) in terms of R_L and the small-signal transistor parameters of M1.

(iii) Show that M1 is in saturation.
What is the headroom of M1 (i.e. the amount by which V_{DS} of M1 exceeds the minimum value of V_{DS} required by M1 to be in saturation)?
Calculate the small-signal voltage gain in dB.
Assume $g_{ds1} << 1/R_L$.

(iv) The gain of the circuit is increased by changing only the W/L ratio of M1.
What is the maximum value of W/L such that M1 is still in saturation?
What is the small-signal voltage gain in dB with this value of W/L?

(i) Draw the small-signal equivalent circuit for the circuit shown in Figure 1.

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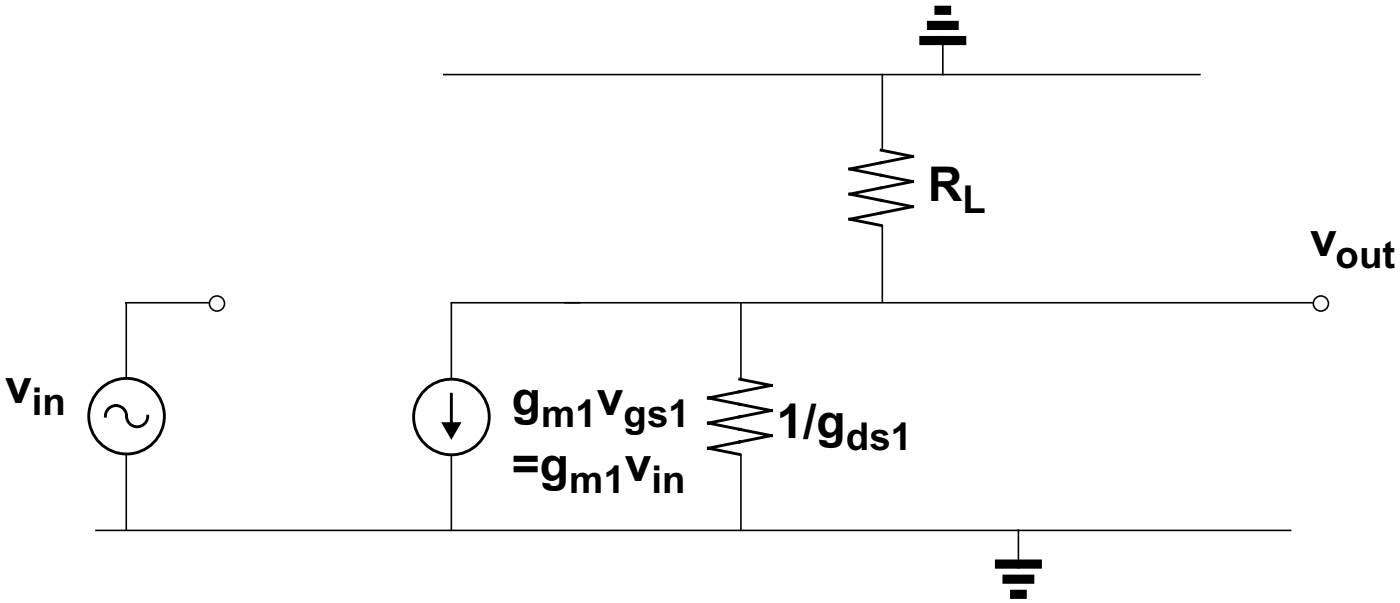

(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) in terms of R_L and the small-signal transistor parameters of M1.

$$g_{m1}v_{in} + v_{out}g_{ds1} + \frac{v_{out}}{R_L} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + \frac{1}{R_L}} \approx -g_{m1}R_L$$

(iii) Show that M1 is in saturation.
What is the headroom of M1 (i.e. the amount by which V_{DS} of M1 exceeds the minimum value of V_{DS} required by M1 to be in saturation)?Calculate the small-signal voltage gain in dB.
Assume $g_{ds1} << 1/R_L$.

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For M1 to be in saturation the $V_{DS1} >= V_{GS1} - V_{tn}$

$$V_{DS1min} = V_{GS1} - V_{tn} = 1 - 0.75V = 0.25V$$

$$V_{DS1} = V_{DD} - I_{D1} R_L$$

$$I_{D1} = \frac{K_n'}{2}\frac{W}{L}(V_{GS1} - V_{tn})^2 = \frac{200\mu A/V^2}{2} \cdot \frac{12}{1} \cdot (1 - 0.75)^2 = 75\mu A$$

$$V_{DS1}' = V_{DD} - I_{D1} \times R_L = 3.25 - 75\mu A \times 10k\Omega = 2.5V$$

$$V_{DS1} > V_{DS1min} \Rightarrow saturation$$

Headroom: $V_{DS1} - V_{DS1min} = 2.5 - 0.25 = 2.25V$

$$g_{m1} = \sqrt{2K_n'\frac{W}{L}I_{D1}} = \sqrt{2 \times 200\mu A/V^2 \times \frac{12}{1} \times 75\mu A} = 600\mu A/V$$

$$\frac{v_{out}}{v_{in}} \approx -g_{m1} R_L = 600\mu A/V \times 10k\Omega = 6$$

$$20\log\left|\frac{v_{out}}{v_{in}}\right| = 15.6dB$$

(iv) The gain of the circuit is increased by changing the W/L ratio of M1.
What is the maximum value of W/L such that M1 is still in saturation.?
What is the small-signal voltage gain in dB with this value of W/L?

$$I_{D1} = \frac{K_n' W}{2 L}(V_{GS1} - V_{tn})^2$$

If W/L increases, then I_{D1} increases proportionally

This increases the voltage drop across R_L

M1 remains in saturation as longs as V_{DS1}>= 0.25V, i.e as longs as

$$V_{DD} - I_{D1} R_L \geq 0.25V$$

$$I_{D1} \leq \frac{V_{DD} - 0.25V}{R_L} = \frac{3.25V - 0.25V}{10k\Omega} = 300\mu A$$

i.e. M1 remains in saturation until I_{D1} increases by 4 times ie W1/L1=48/1

=> Gain increases by 12 dB, or by calculation:

$$g_{m1} = \sqrt{2K_n' \frac{W}{L} I_{D1}} = \sqrt{2 \times 200\mu A/V^2 \times \frac{48}{1} \times 300\mu A} = 2400\mu A/V$$

$$\frac{v_{out}}{v_{in}} \approx -g_{m1} R_L = 2400\mu A/V \times 10k\Omega = 24$$

$$20\log\left|\frac{v_{out}}{v_{in}}\right| = 27.6dB$$

Question 2

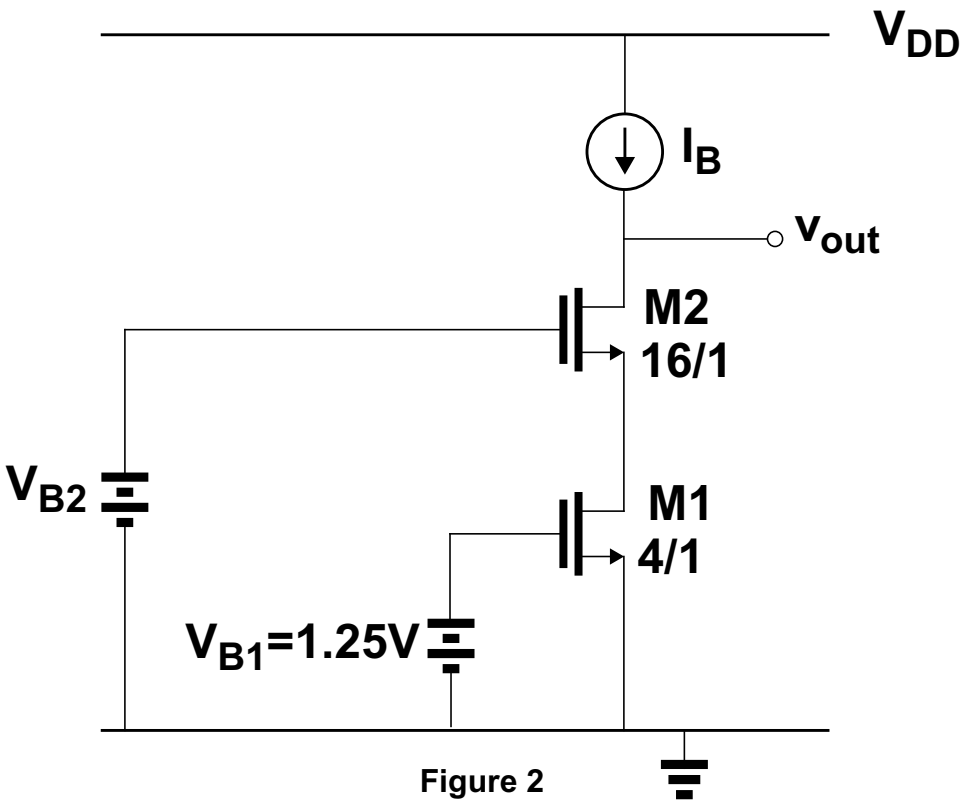

Figure 2

Figure 2 shows a cascode stage with a current source load.
Biasing and transistor dimensions are as shown in Figure 2.
Take K_n'=200μA/V^2, V_{tn}= 0.75V.

(i) What is the minimum value of V_{B2} such that M1 is in saturation? (Assume M2 is in saturation for this calculation). What is then the minimum voltage at the output node (v_{out}) such that M2 is in saturation?

(ii) Draw a small-signal equivalent circuit of the cascode stage, showing how to measure the small-signal output resistance i.e. the resistance looking into the node v_{out}.

(iii) Derive an expression for the small-signal output resistance in terms of the small-signal parameters of M1 and M2. Simplify the expression assuming $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$.

(iv) Calculate the small-signal output resistance assuming all transistors are in saturation. Take λ_n=0.04/L V^{-1} with L in microns.

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(i) What is the minimum value of V_{B2} such that M1 is in saturation? (Assume M2 is in saturation for this calculation). What is then the minimum voltage at the output node (v_{out}) such that M2 is in saturation?

For M1 to be in saturation then

$$V_{DS1} \geq V_{GS1} - V_{tn}$$

$$(V_{DS1})_{min} = V_{GS1} - V_{tn} = 1.25V - 0.75V = 500mV$$

As

$$V_{GS2} - V_t = \sqrt{\frac{2I_{D2}}{K_n' \frac{W_2}{L_2}}} = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V^2 \frac{16}{1}}} = 250mV$$

$$V_{B2} = V_{GS2} + (V_{DS1})_{min}$$

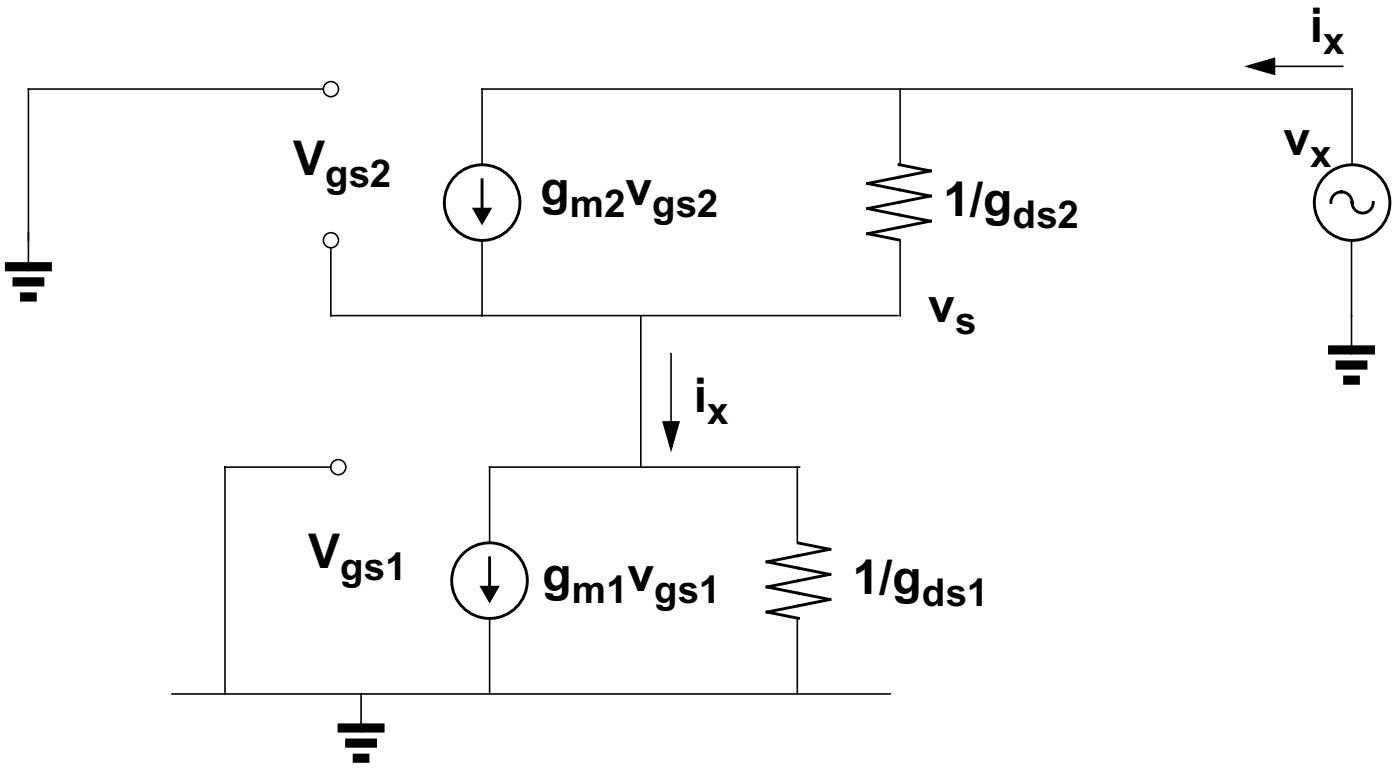
$$V_{BIAS2} = (V_{GS2} - V_{tn}) + V_{tn} + (V_{DS1})_{min} = 0.25V + 0.75V + 0.5V = 1.5V$$

$$V_{DS2} \geq V_{GS2} - V_{tn} = 0.25V$$

so minimum voltage at the output for both transistors to be in saturation is given by

$$V_{outmin} = (V_{DS1})_{min} + (V_{DS2})_{min} = 0.25V + 0.5V = 0.75V$$

(ii) Draw a small-signal equivalent circuit of of the cascode stage, showing how to measure the small-signal output resistance i.e. the resistance looking into the node v_{out}.



(iii) Derive an expression for the small-signal output resistance in terms of the small-signal parameters of M1 and M2. Simplify the expression assuming $g_{m1},g_{m2},>>g_{ds1},g_{ds2},$.

Note: $v_{gs1} = 0 \Rightarrow g_{m1}v_{gs1} = 0$

$$i_x = g_{m2}v_{gs2} + (v_x - v_s)g_{ds2}$$

Since $v_{gs2} = -v_s$ and $v_s = \dfrac{i_x}{g_{ds1}}$

$$i_x = -(g_{m2})\frac{i_x}{g_{ds1}} + \left(v_x - \frac{i_x}{g_{ds1}}\right)g_{ds2}$$

$$r_{out} = \frac{v_x}{i_x} = \frac{1 + \dfrac{g_{m2}}{g_{ds1}} + \dfrac{g_{ds2}}{g_{ds1}}}{g_{ds2}}$$

Since $g_{m1},g_{m2} >> g_{ds1},g_{ds2}$ this can be reduced to

$$r_{out} = \frac{g_{m2}}{g_{ds2}} \cdot \frac{1}{g_{ds1}}$$

(iv) Calculate the small-signal output resistance assuming all transistors are in saturation. Take λ_n=0.04/L V^{-1} with L in microns.

$$r_{out} = \frac{g_{m2}}{g_{ds2}} \cdot \frac{1}{g_{ds1}}$$

$$g_{m2} = \frac{2I_{D2}}{(V_{GS2} - V_{tn})} = \frac{2 \times 100\mu A}{0.25V} = 800\mu A/V$$

$$g_{ds1} = \lambda I_{D1} = \frac{0.04}{L_1} I_{D1} = \frac{0.04}{1} 100\mu A = 4\mu A/V$$

$$g_{ds1} = \lambda I_{D1} = \frac{0.04}{L_1} I_{D1} = \frac{0.04}{1} 100\mu A = 4\mu A/V$$

$$r_{out1} = \frac{g_{m2}}{g_{ds2}} \cdot \frac{1}{g_{ds1}} = \frac{800\mu A/V}{4\mu A/V} \cdot \frac{1}{4\mu A/V} = \underline{\underline{50M\Omega}}$$

Question 3

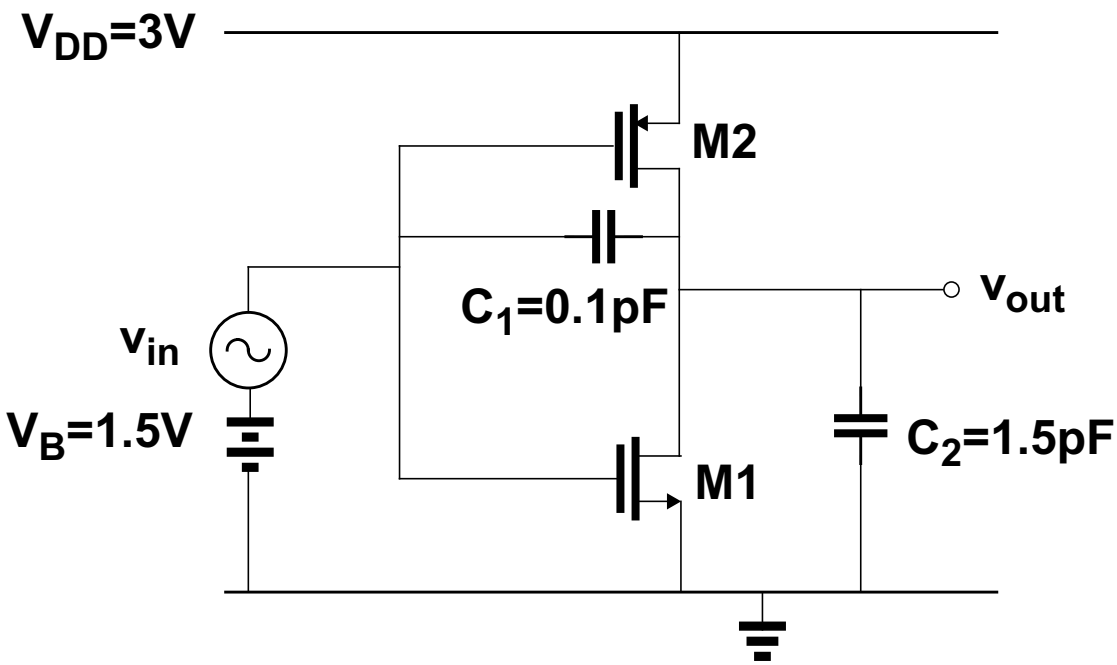
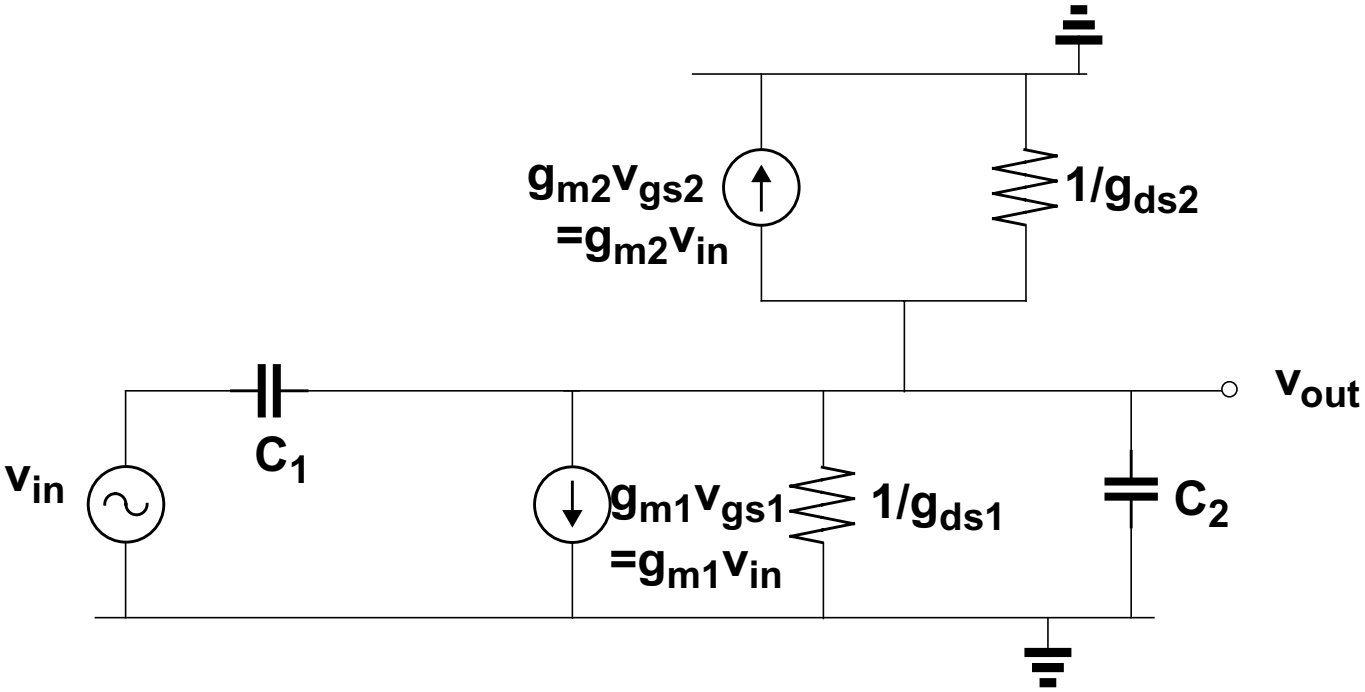


Figure 3

Figure 3 shows a CMOS inverter stage.
Biasing and component values are as shown in Figure 3.
Take V_{tn}=0.7V, V_{tp}=-0.7V, $\lambda_n=\lambda_p$=0.04V^{-1}.

(i) Draw the small-signal equivalent circuit for the CMOS inverter stage shown in Figure 3.
(ii) Derive an expression for the high-frequency transfer function.
(iii) Calculate the dc gain in dB, and the break frequencies (i.e. pole and/or zero frequencies).
Assume both transistors are in saturation with a drain current of 200μA.
(iv) Draw a Bode diagram of the gain response.
What is the value of gain at frequencies well above the break frequencies?

(i) Draw the small-signal equivalent circuit for the CMOS inverter stage shown in Figure 3.



(ii) Derive an expression for the high-frequency transfer function.

KCL at output node

$$(v_{out}-v_{in})sC_1 + g_{m1}v_{in} + g_{m2}v_{in} + v_{out}g_{ds1} + v_{out}g_{ds2} + v_{out}sC_2 = 0$$

$$(g_{m1} + g_{m1} - sC_1)v_{in} = -(g_{ds1} + g_{ds2} + sC_{gs1} + sC_L)v_{out}$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} + g_{m2} - sC_1}{g_{ds1} + g_{ds2} + sC_1 + sC_2}$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}} \frac{\left(1 - \frac{sC_1}{g_{m1} + g_{m2}}\right)}{\left(1 + \frac{s(C_1 + C_2)}{g_{ds1} + g_{ds2}}\right)}$$

(iii) Calculate the dc gain in dB, and the break frequencies (i.e. pole and/or zero frequencies). Assume both transistors are in saturation with a drain current of 200μA.

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}}\frac{\left(1-\frac{sC_1}{g_{m1}+g_{m2}}\right)}{\left(1+\frac{s(C_1+C_2)}{g_{ds1}+g_{ds2}}\right)}$$

$$g_{m1} = \frac{2I_D}{(V_{GS1}-V_{tn})} = \frac{2\times 200\mu A}{1.5-0.7} = 500\mu A/V$$

$$g_{m2} = \frac{2I_D}{(|V_{GS2}|-|V_{tp}|)} = \frac{2\times 200\mu A}{1.5V-0.7V} = 500\mu A/V$$

$$g_{ds1} = \lambda I_D = 0.04V^{-1}\times 200\mu A = 8\mu A/V$$

$$g_{ds2} = \lambda I_D = 0.04V^{-1}\times 200\mu A = 8\mu A/V$$

DC gain given by

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}} = -\frac{500\mu A/V+500\mu A/V}{8\mu A/V+8\mu A/V} = -62.5$$

$$20\log\left|\frac{v_{out}}{v_{in}}\right| = 36dB$$

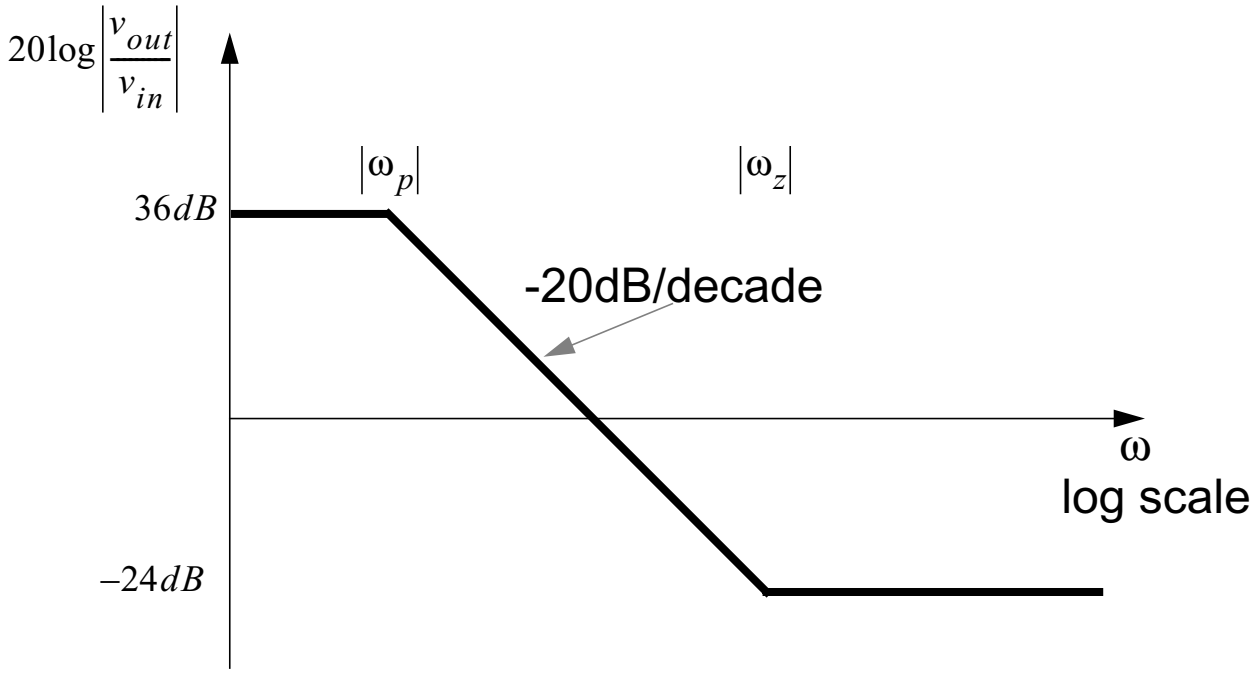
Pole frequency given by

$$|\omega_p| = \frac{g_{ds1}+g_{ds2}}{(C_1+C_2)} = \frac{16\mu A/V}{0.1pF+1.5pF} = 10Mrad/s$$

Zero frequency given by

$$|\omega_Z| = \frac{g_{m1}+g_{m2}}{C_1} = \frac{1000\mu A/V}{0.1pF} = 10Grad/s$$

(iv) Draw a Bode diagram of the gain response.
What is the value of gain at frequencies well above the break frequencies?



Zero is 3 decades up gives HF gain = -24dB.

Question 4

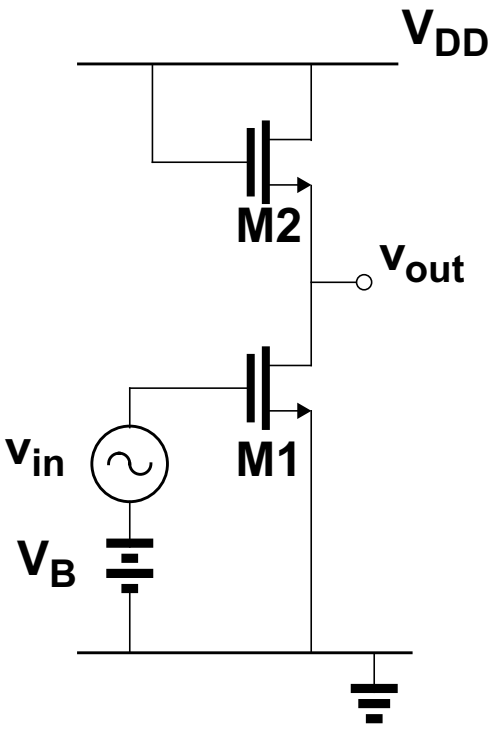


Figure 4a

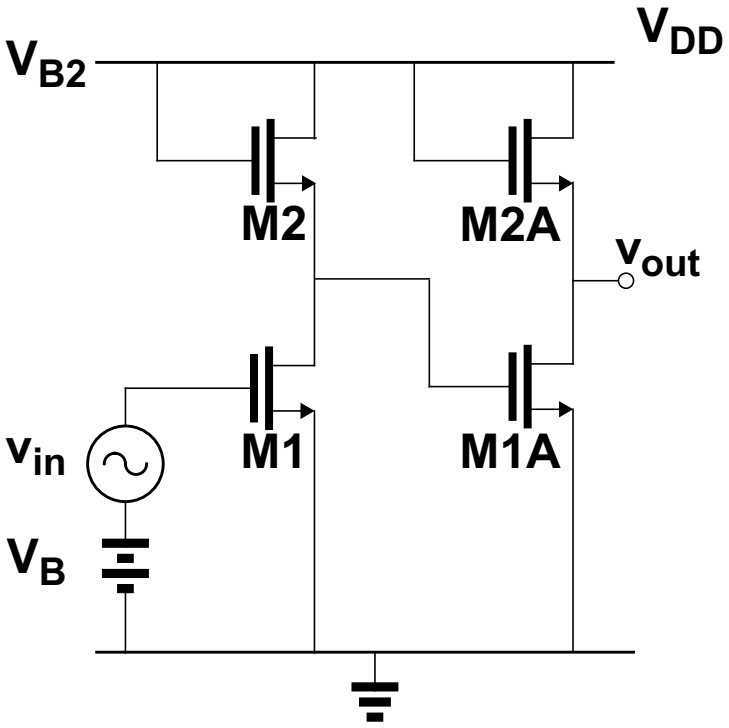


Figure 4b

For the circuits shown in Figure 4a and 4b, assume all transistors are operating in saturation and $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$. Only thermal noise sources need be considered.

Take Boltzmann's constant $k=13.8X10^{-24}$ J/^{o}K, temperature T=300^{o}K.

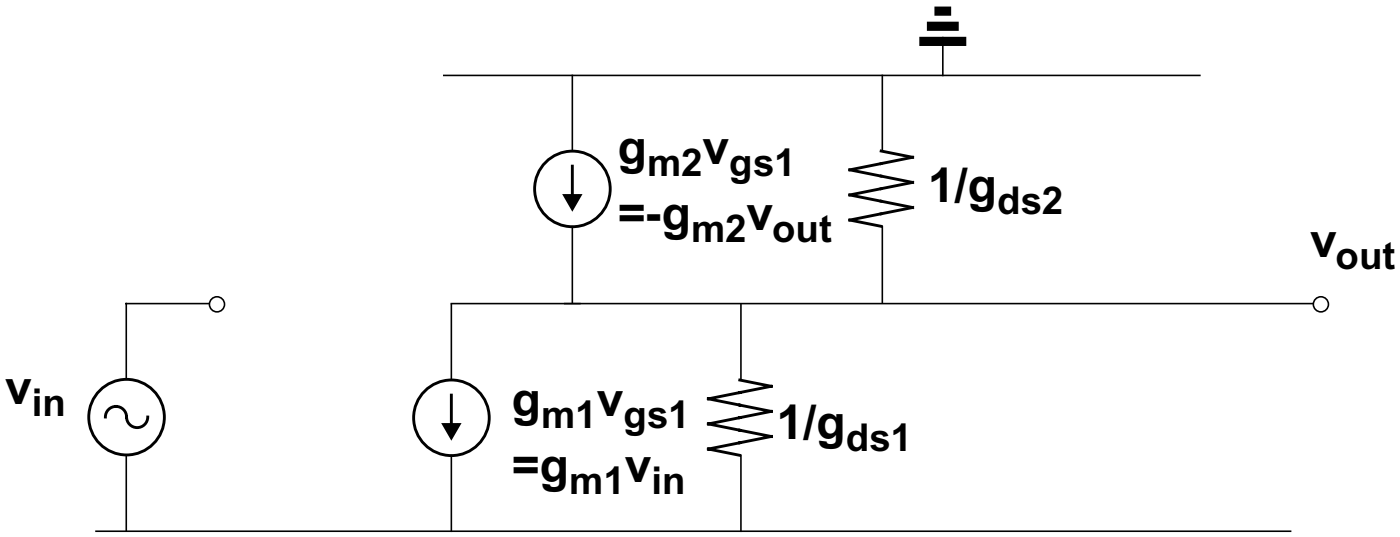
(i) Draw the small-signal model for the circuit shown in Figure 4a.
What is the small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters of M1 and M2?

(ii) What is the input-referred noise voltage density in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T?

(iii) Calculate the input-referred noise voltage density if g_{m1}=400μA/V, g_{m2}=100μA/V.
What is the noise voltage density at the output?
(Note: the units μA/V are equivalent to μS).

(iv) The gain stage shown in Figure 4a is cascaded with an identical gain stage, with identical transistor dimensions, as shown in Figure 4b. Assume also that M1A has the same biasing conditions as M1.
Calculate the input-referred noise voltage density of the circuit shown in Figure 4b.
What is the total input-referred noise in a bandwidth of 1MHz to 10MHz?

(i) Draw the small-signal model for the circuit shown in Figure 4a.
What is the small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters of M1 and M2?

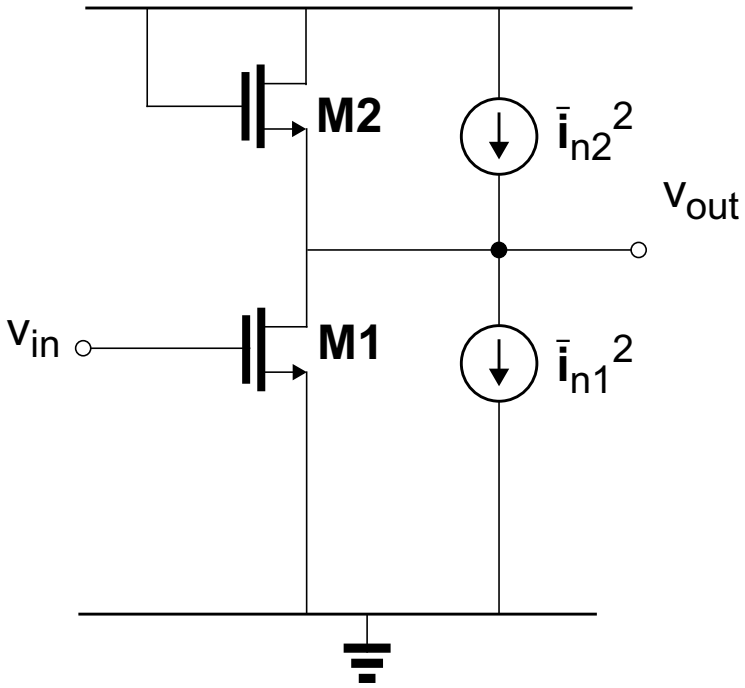


$$g_{m1}v_{in} + v_{out}g_{ds1} + g_{m2}v_{out} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \approx -\frac{g_{m1}}{g_{m2}}$$

Alternatively recognise that M2 is equivalent to a small-signal resistance $1/g_{m2}$ and write result directly

(ii) What is the input-referred noise voltage density in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T?



Total noise current at output is square root of the individual noise currents

$$\overline{i_{nt}} = \sqrt{i_{n1}^2 + i_{n2}^2} = \sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}$$

Input-referred noise voltage given by

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}}{g_{m1}} \qquad V/\sqrt{Hz}$$

(iii) Calculate the input-referred noise voltage density if g_{m1}=400μA/V, g_{m2}=100μA/V.
What is the noise voltage density at the output?
(Note: the units μA/V are equivalent to μS).

Noise density at input

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \sqrt{4kT \cdot \frac{2}{3}\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2}\right)} = \sqrt{4kT \cdot \frac{2}{3}\left(\frac{1}{400\mu A/V} + \frac{100\mu A/V}{(400\mu A/V)^2}\right)} = 5.87nV/(\sqrt{Hz})$$

To get voltage noise at output multiply input-referred noise by gain of circuit

$$\overline{v_{no}} = \overline{v_{ni}}\frac{g_{m1}}{g_{m2}}$$

$$Gain = \frac{g_{m1}}{g_{m2}} = \frac{400\mu A/V}{100\mu A/V} = 4$$

$$\overline{v_{no}} = 5.87nV/\sqrt{Hz} \times 4 = 23.5nV/\sqrt{Hz}$$

(iv) The gain stage shown in Figure 4a is cascaded with an identical gain stage, with identical transistor dimensions, as shown in Figure 4b. Assume also that M1A has the same biasing conditions as M1.
Calculate the input-referred noise voltage density of the circuit shown in Figure 4b.
What is the total input-referred noise in a bandwidth of 1MHz to 10MHz?

Input Noise density of second stage is divided by gain of second stage and added quadratically to noise of first stage

$$\overline{v_{nitot}} = \sqrt{v_{ni1}^2 + \left(\frac{v_{ni2}}{Gain}\right)^2} = \sqrt{5.87^2 + \left(\frac{5.87}{4}\right)^2} \approx 6.05nV/\sqrt{Hz}$$

$$\overline{v_{nitot1to10MHz}} = v_{nitot}\sqrt{9MHz} = 6.05nV/\sqrt{Hz} \times \sqrt{9MHz} \approx 18.2\mu V$$