UE4010 Autumn 2006 Part A

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an NMOS in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS} - V_{tn})^2(1 + \lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n = \lambda_p = 0$.
In each question, capacitances other than those mentioned may be ignored.

Question 1

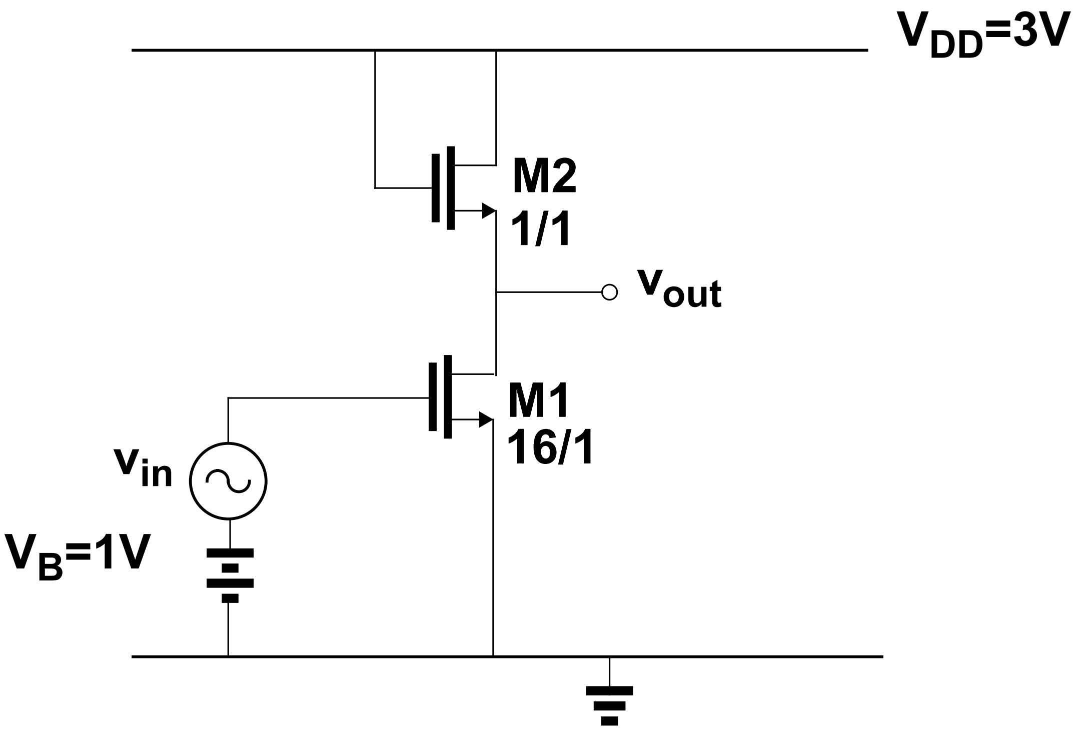


Figure 1

Figure 1 shows a common-source stage with an NMOS diode load.
Biasing and transistor dimensions are as shown in Figure 1. Take $K_n' = 200\mu A/V^2$, V_{tn} = 0.75V.

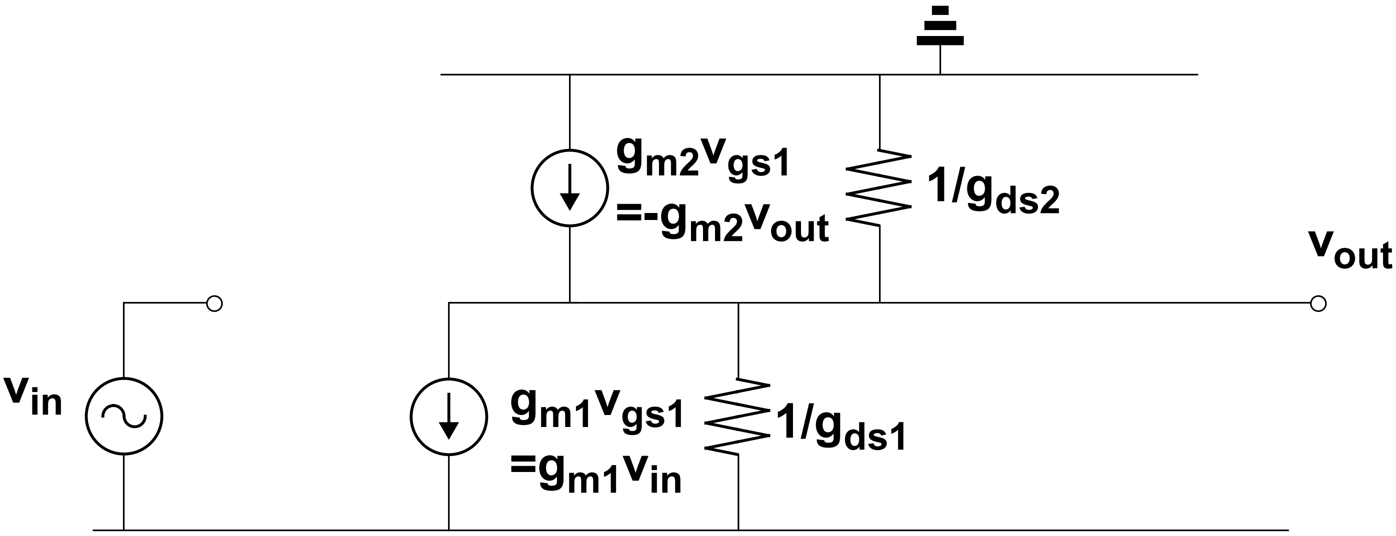
(i) Draw the small-signal equivalent circuit for the circuit shown in Figure 1.

(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal transistor parameters of M1 and M2.

(iii) Show that M1 is in saturation.
What is the headroom of M1 (i.e. the amount by which V_{DS} of M1 exceeds the minimum value of V_{DS} required by M1 to be in saturation)?
Calculate the small-signal voltage gain in dB.
Assume $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$.

(iv) The gain of the circuit is increased by changing the W/L ratio of M1.
What is the maximum value of W/L such that M1 is still in saturation?
What is the small-signal voltage gain in dB with this value of W/L?

(i) Draw the small-signal equivalent circuit for the circuit shown in Figure 1.



(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal transistor parameters of M1 and M2.

$$g_{m1}v_{in} + v_{out}g_{ds1} + g_{m2}v_{out} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \approx -\frac{g_{m1}}{g_{m2}}$$

Alternatively recognise that M2 is equivalent to a small-signal resistance $1/g_{m2}$ and write result directly

(i) Show that M1 is in saturation.
What is the headroom of M1 (i.e. the amount by which V_{DS} of M1 exceeds the minimum value of V_{DS} required by M1 to be in saturation)?
Calculate the small-signal voltage gain in dB.
Assume $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$

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For M1 to be in saturation the $V_{DS1} >= V_{GS1} - V_{tn}$

$$V_{DS1min} = V_{GS1} - V_{tn} = 1 - 0.75V = 0.25V$$

$$V_{DS1} = V_{DD} - V_{GS2}$$

$$I_{D1} = \frac{K'_n}{2}\frac{W}{L}(V_{GS1} - V_{tn})^2 = \frac{200\mu A/V^2}{2} \cdot \frac{16}{1} \cdot (1 - 0.75)^2 = 100\mu A$$

$$V_{GS2} = \sqrt{\frac{2I_{D1}}{K'_n\frac{W}{L}}} + V_{tn} = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V^2\frac{1}{1}}} + 0.75 = 1 + 0.75 = 1.75V$$

$$V_{DS1} = V_{DD} - V_{GS2} = 3 - 1.75 = 1.25$$

$$V_{DS1} > V_{DS1min} \Rightarrow saturation$$

Headroom: $V_{DS1} - V_{DS1min} = 1.25 - 0.25 = 1V$

$$g_{m1} = \sqrt{2K'_n\frac{W_1}{L_1}I_{D1}}$$

$$g_{m2} = \sqrt{2K'_n\frac{W_2}{L_2}I_{D2}}$$

$I_{D1} = I_{D2} =>$ $$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}}{g_{m2}} = -\frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}} = -\frac{16}{1}$$

$$20\log\left|\frac{v_{out}}{v_{in}}\right| = 24dB$$

(ii) The gain of the circuit is increased by changing the W/L ratio of M1.
What is the maximum value of W/L such that M1 is still in saturation.?
What is the small-signal voltage gain in dB with this value of W/L.

$$I_{D1} = \frac{K'_n}{2}\frac{W}{L}(V_{GS1} - V_{tn})^2$$

If W/L increases, then I_{D1} increases

This increases the voltage drop across M2 (i.e. V_{GS2})

M1 remains in saturation as longs as V_{DS1}>= 0.25V, i.e as longs as

$$V_{DD} - V_{GS2} \geq 0.25V$$

$$V_{DD} - (V_{GS2} - V_{tn} + V_{tn}) > 0.25V$$

$$V_{GS2} - V_{tn} \leq V_{DD} - V_{tn} - 0.25V$$

$$V_{GS2} - V_{tn} \leq 2V$$

From (iii), original V_{GS2}-V_{tn}=1V

i.e. M1 remains in saturation until I_{D2}=I_{D1} doubles ie W1/L1=32/1

Gain then given by

$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}}{g_{m2}} = -\frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}} = -\frac{32}{1}$$

$$20\log\left|\frac{v_{out}}{v_{in}}\right| = 30dB$$

Question 2

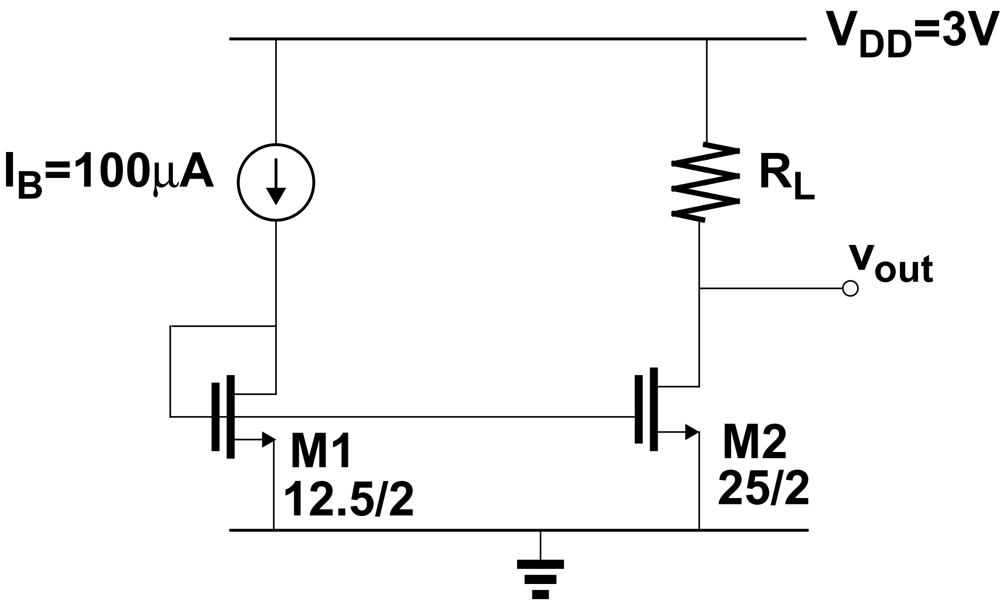

Figure 2

Figure 2 shows an NMOS current mirror (M1, M2) with the output connected via a resistor R_L to V_{DD}.
Take $K_n' = 200\mu A/V^2$, $V_{tn} = 0.75V$.
Biasing and transistor dimensions are as shown in Figure 2.

(i) What is the minimum value of the voltage at the output node (i.e the drain of M2) such that M2 is in saturation? What is the maximum value of R_L such that M2 is in saturation?

(ii) Draw a small-signal equivalent circuit showing how to measure the small-signal output resistance of the circuit i.e. the resistance looking into the node v_{out}?

(iii) Derive an expression for the small-signal output resistance in terms of R_L and the small-signal transistor parameters.

(iv) Calculate the small-signal output resistance if R_L is equal to the maximum value calculated in (i). Take $\lambda_n = 0.04/L\ V^{-1}$ with L in microns.

(i) What is the minimum value of the voltage at the output node (i.e the drain of M2) such that M2 is in saturation? What is the maximum value of R_L such that M2 is in saturation?

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For M1 to be in saturation the $V_{DS2}>=V_{GS2}-V_{tn}$

Note: $V_{GS2}-V_{tn} = V_{GS1}-V_{tn}$

$$V_{GS1} - V_{tn} = \sqrt{\frac{2I_{D1}}{K_n^{'}\frac{W_1}{L_1}}} = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V^2 \frac{12.5}{2}}} = 0.4V$$

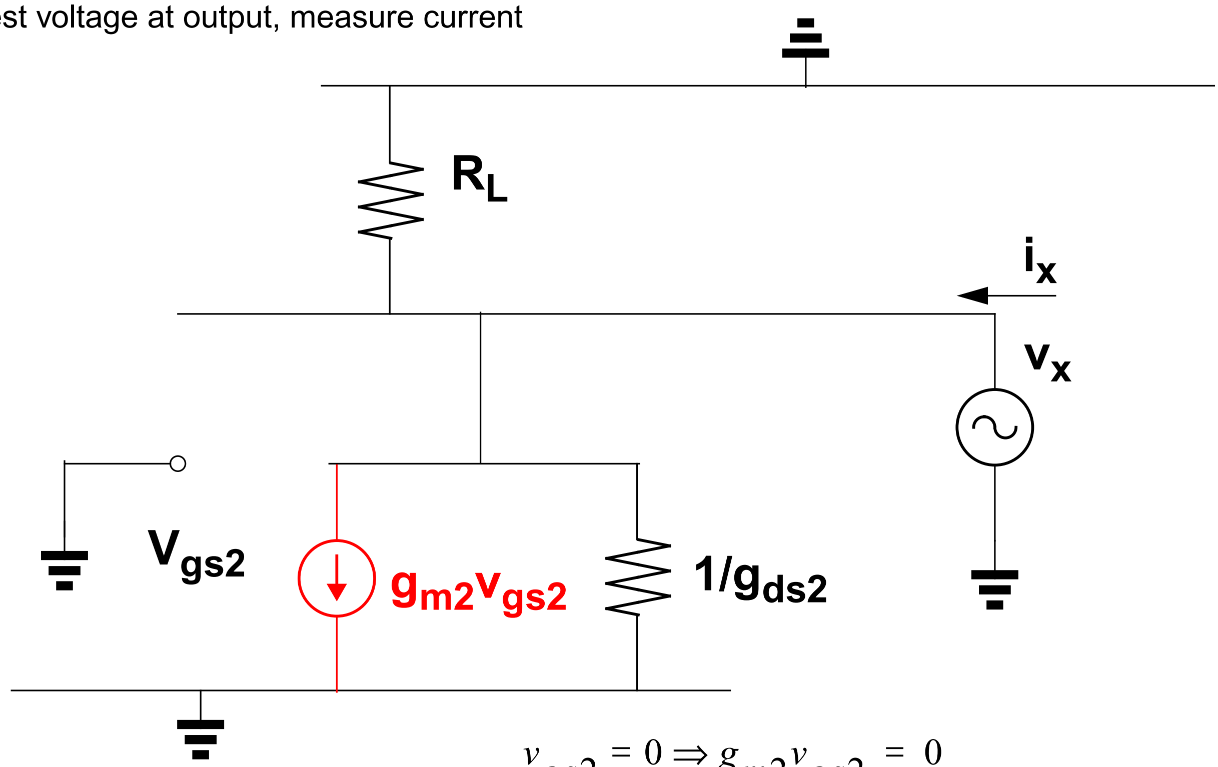
M2 has same $V_{GS}-V_{tn}$ as M1 i.e. 0.4V => V_{DS2min}=0.4V

$W_2/L_2=2W_1/L_1 => I_{D2}=2I_{D1}$

$$R_{Lmax} = \frac{V_{DD} - V_{DS1min}}{I_{D2}} = \frac{V_{DD} - V_{DS1min}}{2I_{D1}} = \frac{3 - 0.4}{2 \cdot 100\mu A} = 13k\Omega$$

(ii) Draw a small-signal equivalent circuit showing how to measure the small-signal output resistance i.e. the resistance looking into the node v_{out}?

Apply test voltage at output, measure current



$$v_{gs2} = 0 \Rightarrow g_{m2}v_{gs2} = 0$$

As no small-signal flows through M1, the gate of M2 can be considered grounded, so $v_{gs2}=0$
Current source $g_{m2}v_{gs2}=0$ shown in red is open circuit may be omitted from circuit.

(iii) Derive an expression for the small-signal output resistance in terms of R_L and the small-signal transistor parameters.

$$i_x = \frac{v_x}{R_L} + v_x g_{ds2}$$

$$r_{out} = \frac{v_x}{i_x} = \frac{1}{g_{ds2} + \frac{1}{R_L}}$$

(iv) Calculate the small-signal output resistance if R_L is equal to the maximum value calculated in (i). Take λ_n=0.04/L V^{-1} with L in microns.

$$g_{ds2} = \lambda I_D = \frac{0.04V^{-1}}{2} \times 200\mu A = 8\mu A/V$$

$$r_{out} = \frac{1}{g_{ds2} + \frac{1}{R_L}} = \frac{1}{4\mu A/V + \frac{1}{13k\Omega}} = 12.4k\Omega$$

Question 3

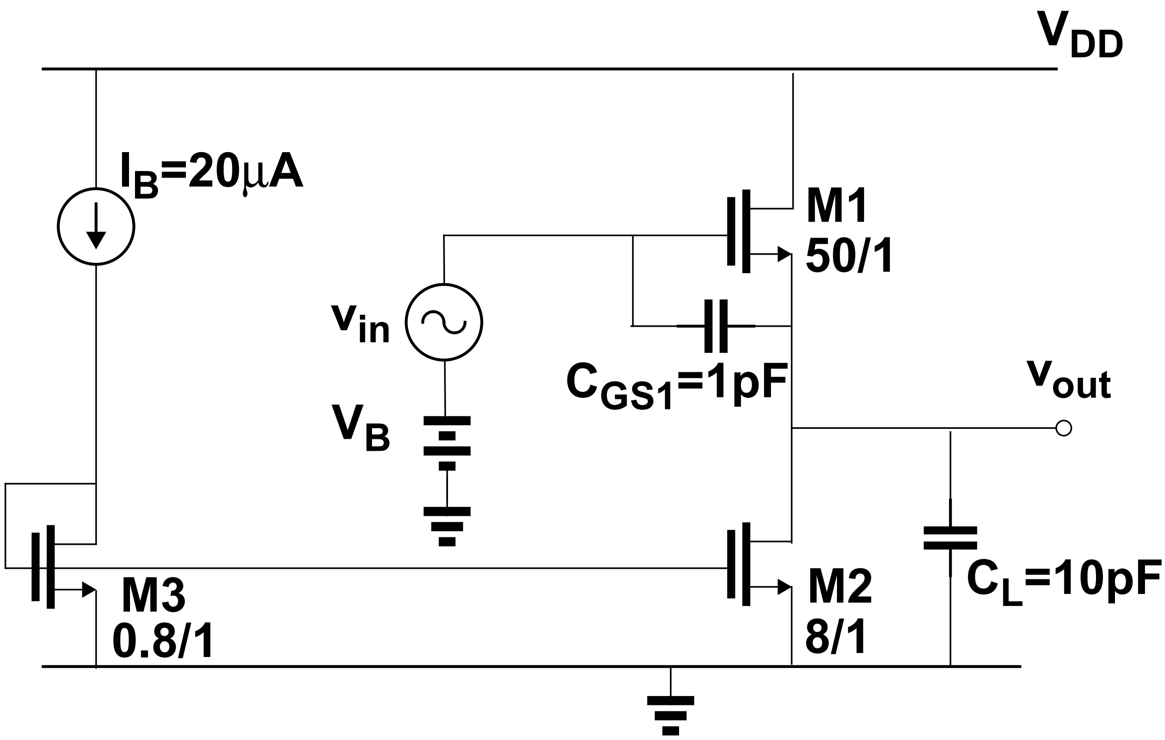


Figure 3

Figure 3 shows an NMOS source follower.

Biasing and transistor dimensions are as shown in Figure 3. Take $K_n'=200\mu A/V^2$.

Assume all transistors are in saturation and $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$.

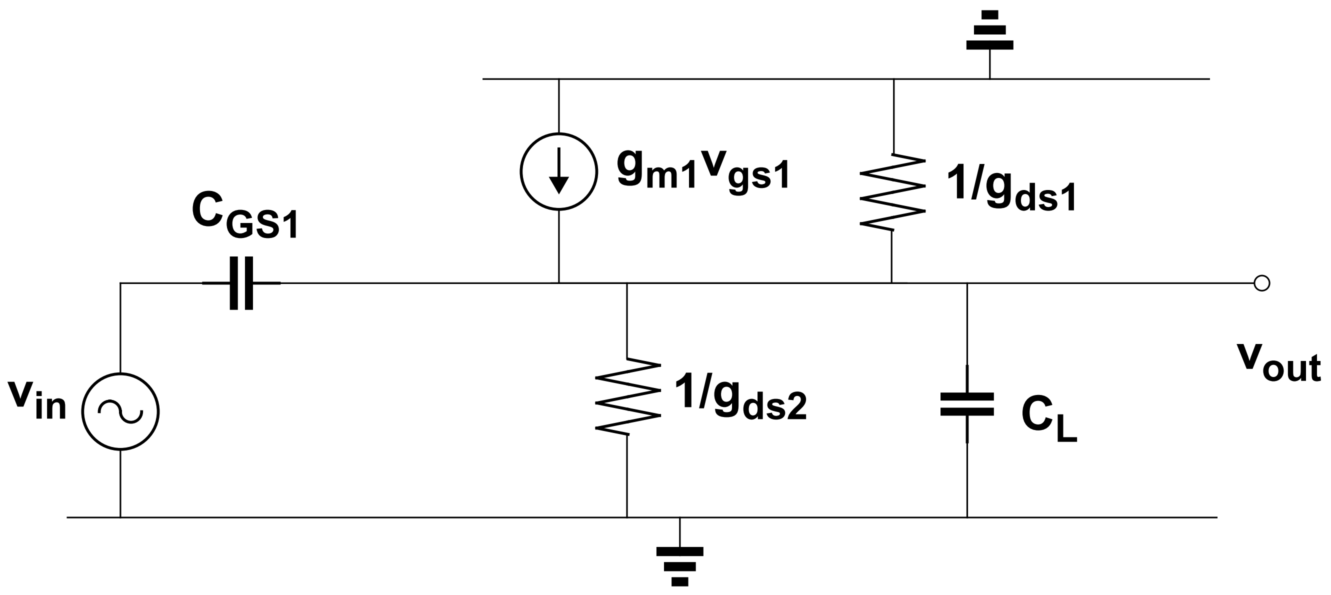
(i) Draw the small-signal equivalent circuit for the source follower stage shown in Figure 3.

(ii) Derive an expression for the high frequency transfer function.

(iii) Calculate the dc gain in dB, and the break frequencies (i.e. pole and/or zero frequencies).

(iv) Draw a Bode diagram of the gain response.
What is the value of gain at frequencies well above the break frequencies?

(i) Draw the small-signal equivalent circuit for the source follower stage shown in Figure 3.



(ii) Derive an expression for the high frequency transfer function.

$$v_{gs1} = v_{in} - v_{out}$$

KCL at output node

$$(v_{in} - v_{out})sC_{gs1} + g_{m1}(v_{in} - v_{out}) - (v_{out}g_{ds1}) - (v_{out}g_{ds2}) - v_{out}sC_L = 0$$

$$(g_{m1} + sC_{gs1})v_{in} = (g_{m1} + g_{ds1} + g_{ds2} + sC_{gs1} + sC_L)v_{out}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1} + sC_{gs1}}{g_{m1} + g_{ds1} + g_{ds2} + sC_{gs1} + sC_L}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1} + g_{ds2}} \frac{\left(1 + \frac{sC_{gs1}}{g_{m1}}\right)}{\left(1 + \frac{s(C_{gs1} + C_L)}{g_{m1} + g_{ds1} + g_{ds2}}\right)}$$

(iii) Calculate the dc gain in dB, and the break frequencies (i.e. pole and/or zero frequencies).

DC gain given by

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1} + g_{ds2}} \approx 1 = \underline{\underline{0dB}}$$

Pole frequency given by

$$|\omega_p| = \frac{g_{m1} + g_{ds1} + g_{ds2}}{(C_{gs1} + C_L)} \approx \frac{g_{m1}}{(C_{gs1} + C_L)}$$

$W_3/L_3 = 10W_2/L_2 \Rightarrow I_{D2} = 10I_{D1}$

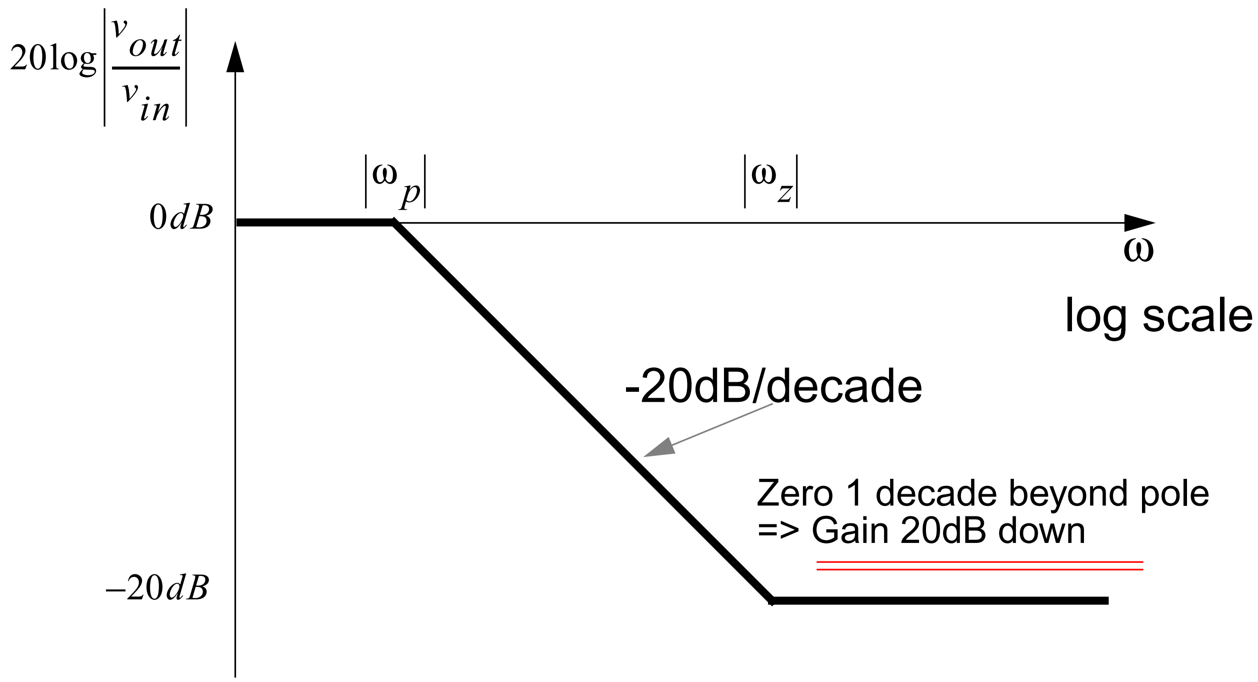
$$g_{m1} = \sqrt{2K'_p \frac{W}{L} I_D} = \sqrt{2 \times 200\mu A/V \times \frac{50}{1} \times 200\mu A} = 2000\mu A/V$$

$$|\omega_p| \approx \frac{2000\mu A/V}{1pF + 9pF} = \underline{\underline{200Mrad/s}}$$

Zero frequency given by

$$|\omega_z| = \frac{g_{m1}}{C_{gs1}} = \frac{2000\mu A/V}{1pF} = \underline{\underline{2Grad/s}}$$

(iv) Draw a Bode diagram of the gain response.
What is the value of gain at frequencies well above the break frequencies?



Question 4

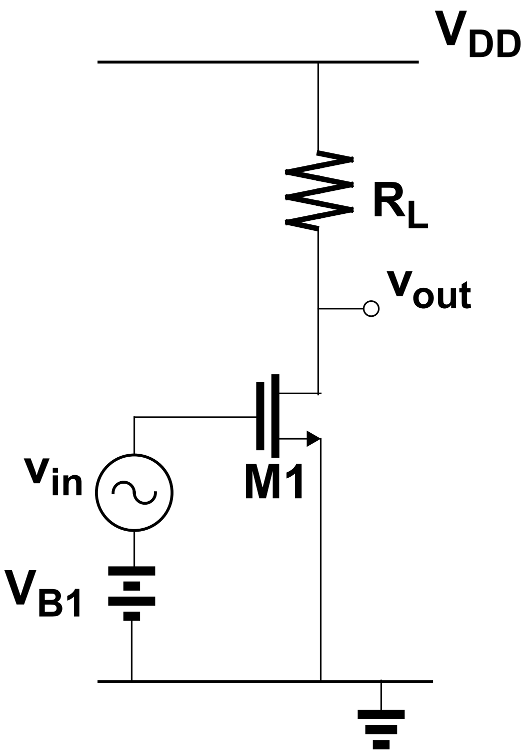


Figure 4a

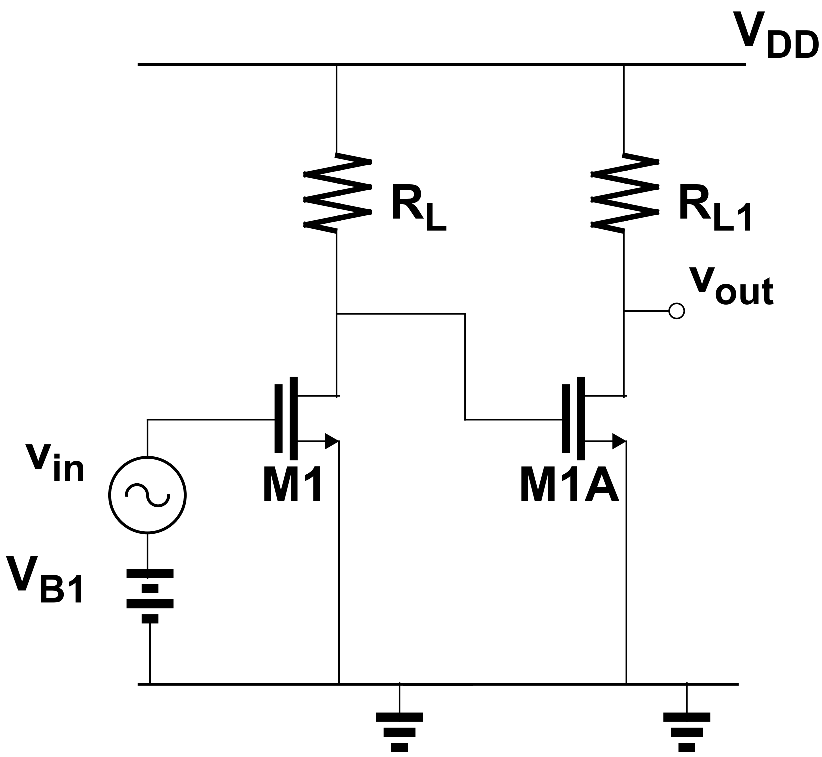


Figure 4b

For the circuits shown in Figure 4a and 4b, assume all transistors are operating in saturation.
Only thermal noise sources need be considered.
Take Boltzmann's constant $k=13.8X10^{-24}J/^oK$, temperature $T=300^oK$.

(i) Draw the small-signal model for the circuit shown in Figure 4a.
What is the low-frequency small-signal voltage gain (v_{out}/v_{in}) in terms of R_L and the small-signal parameters of M1?

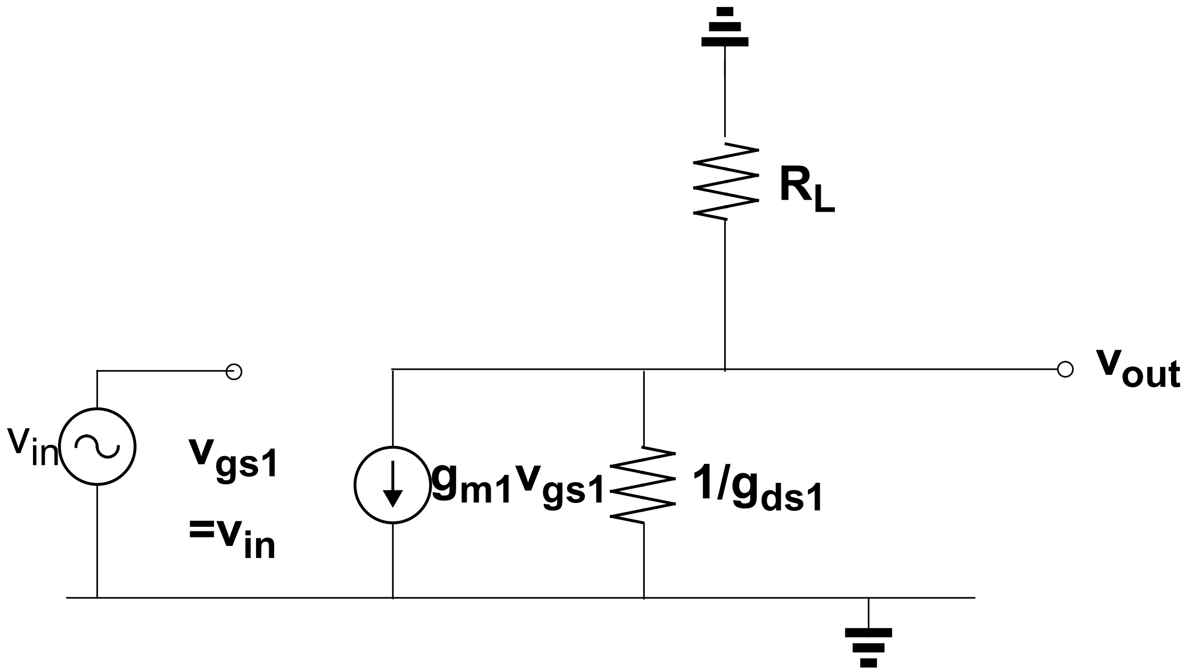
(ii) What is the input-referred noise voltage density in terms of the small-signal parameters of M1, R_L, Boltzmann's constant k and temperature T?

(iii) Calculate the input-referred noise voltage density if $g_{m1}=400\mu A/V$, $R_L=10k\Omega$.
What is the noise voltage density at the output? Assume $g_{ds1} << 1/R_L$.
(Note: the units $\mu A/V$ are equivalent to μS).

(iv) The gain stage shown in Figure 4a is cascaded with an identical gain stage, with identical transistor dimensions and load resistance as shown in Figure 4b. Assume also that M1A has the same biasing conditions as M1.
Calculate the input-referred noise voltage density of the circuit shown in Figure 4b.
What is the total input-referred noise in a bandwidth of 1MHz to 10MHz?

Solution

(i) Draw the small-signal model for the circuit shown in Figure 4a.
What is the low-frequency small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters of M1 and R_L?

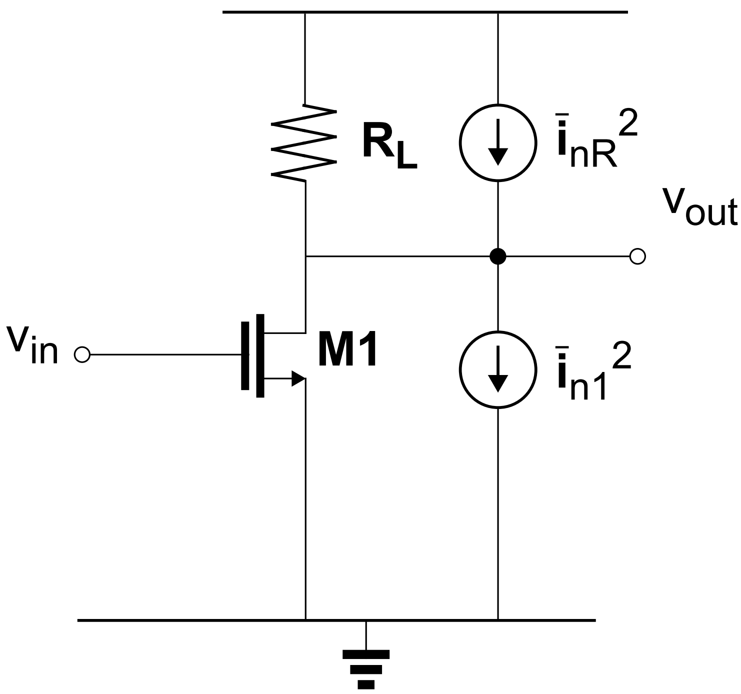


Current at output node

$$g_{m1}v_{in} + v_{out}g_{ds1} + \frac{v_{out}}{R_L} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + \frac{1}{R_L}} \cong -g_{m1}R_L$$

(ii) What is the input-referred noise voltage density in terms of the small-signal parameters of M, R_L, Boltzmann's constant k and temperature T?



Total noise current at output is square root of the individual noise currents

$$\overline{i_{nt}} = \sqrt{i_{n1}^2 + i_{n2}^2} = \sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + \frac{4kT}{R_L}}$$

Input-referred noise voltage given by

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_{m1}} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + \frac{4kT}{R_L}}}{g_{m1}} = \sqrt{4kT\left(\frac{2}{3}\frac{1}{g_{m1}} + \frac{1}{g_{m1}^2 R_L}\right)} \qquad V/\sqrt{Hz}$$

(iii) Calculate the input-referred noise voltage density if g_{m1}=400µA/V, RL=10kΩ.
What is the noise voltage density at the output? Assume $g_{ds1} << 1/R_L$.
(Note: the units µA/V are equivalent to µS).

Noise density at input

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_m} = \sqrt{4kT\left(\frac{2}{3}\frac{1}{g_{m1}} + \frac{1}{g_{m1}^2 R_L}\right)} = \sqrt{4kT\cdot\frac{2}{3}\left(\frac{1}{400\mu A/V} + \frac{1}{(400\mu A/V)^2 10k\Omega}\right)} = 5.9nV/(\sqrt{Hz})$$

To get noise voltage density at output multiply input-referred noise voltage density by gain of circuit

$$\overline{v_{no}} = \overline{v_{ni}}g_{m1}R_L$$

$$Gain = g_{m1}R_L = 400\mu A/V \times 10k\Omega = 4$$

$$\overline{v_{no}} = 5.9nV/\sqrt{Hz} \times 4 = 23.5nV/\sqrt{Hz}$$

(iv) The gain stage shown in Figure 4a is cascaded with an identical gain stage, with identical transistor dimensions and load resistance as shown in Figure 4b. Assume also that M1A has the same biasing conditions as M1.
Calculate the input-referred noise voltage density of the circuit shown in Figure 4b.
What is the total input-referred noise in a bandwidth of 1MHz to 10MHz?

Input Noise density of second stage is divided by gain of second stage and added quadratically to noise of first stage

$$\overline{v_{nitot}} = \sqrt{v_{ni1}^2 + \left(\frac{v_{ni2}}{Gain}\right)^2} = \sqrt{5.9^2 + \left(\frac{5.9}{4}\right)^2} \approx 6.1nV/\sqrt{Hz}$$

Alternatively point out that noise of second stage divided by gain of first stage makes it negligible.

$$\overline{v_{nitot1to10MHz}} = v_{nitot}\sqrt{9MHz} = 6.1nV/\sqrt{Hz} \times \sqrt{9MHz} \approx 18.3\mu V$$