Solutions UE4002 Summer 2009

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an NMOS in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.
In each question, capacitances other than those mentioned may be ignored.

Question 1

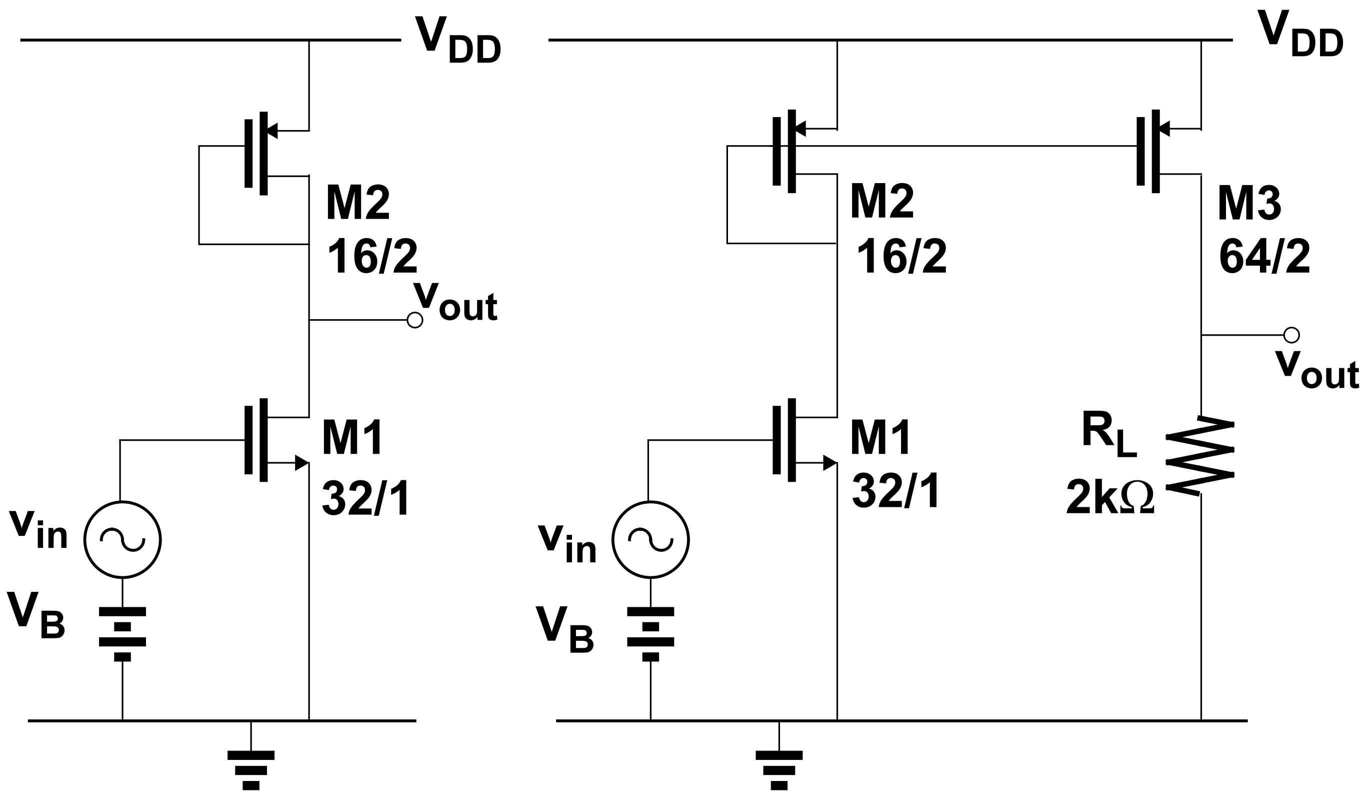
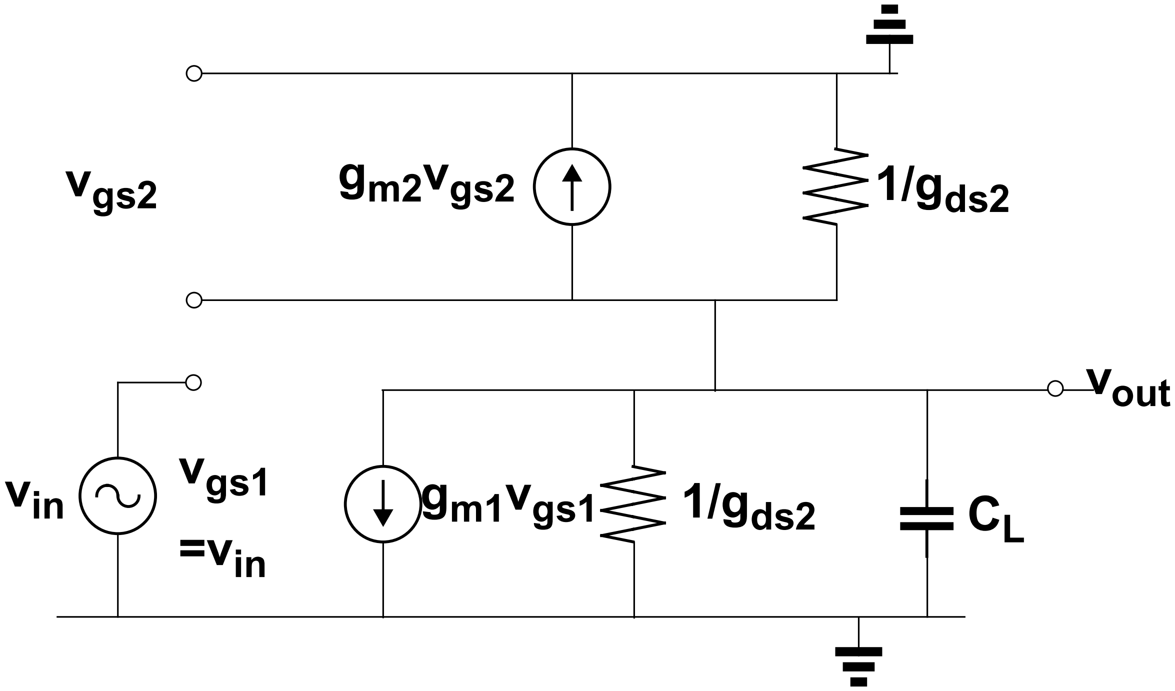


Figure 1a　　Figure 1b

For the questions below you may assume $g_{m1},g_{m2} \gg g_{ds1},g_{ds2}$ and that all devices are biased in saturation.

(i) Figure 1a shows a gain stage with a diode-connected load.
Draw the small-signal model for this circuit.
(ii) Derive an expression for the small signal voltage gain (v_{out}/v_{in}).
(iii) Calculate the drain current of M1 and the small-signal voltage gain (v_{out}/v_{in}) in dB if
V_B=1V, $V_{tn}=|V_{tp}|$=0.75V, $K_n'=200\mu A/V^2$, $K_p'=50\mu A/V$.
Transistor dimensions in microns are as shown in Figure 1a.
(iv) Calculate the small-signal voltage gain (v_{out}/v_{in}) of the circuit shown in Figure 1b.
Assume $g_{ds3} \ll 1/R_L$.

(i) Figure 1a shows a gain stage with a diode-connected load.
Draw the small-signal model for this circuit.



(ii) Derive an expression for the low-frequency small signal voltage gain (v_{out}/v_{in}).

Current at output node

$$g_{m1}v_{gs1} + g_{m2}v_{gs2} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$g_{m1}v_{in} + g_{m2}v_{out} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \cong -\frac{g_{m1}}{g_{m2}}$$

Alternatively recognise that the current of the current-source $g_{m2}v_{gs2}$ is determined by voltage across its terminals i.e. is equivalent to a resistance $1/g_{m2}$.
Since $1/g_{m2} << 1/g_{ds2}$, $1/g_{m2} << 1/g_{ds1}$, can write directly

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2}}$$

(iii) Calculate the drain current of M1 and the small-signal voltage gain (v_{out}/v_{in}) in dB if V_B=1V, V_{tn}=$|V_{tp}|$=0.75V, K_n'=200µA/V^2 , K_p'=50µA/V.
Transistor dimensions in microns are as shown in Figure 1a.

$$I_{D1} = \frac{K_n'}{2}\frac{W}{L}(V_{GS1}-V_{tn})^2 = \frac{200\mu A/V^2}{2}\cdot\frac{32}{1}\cdot(1-0.75)^2 = 200\mu A$$

$$g_{m1} = \sqrt{2K_n'\frac{W}{L}I_D} = \sqrt{2\times 200\mu A/V\times\frac{32}{1}\times 200\mu A} = 1600\mu A/V$$

$$g_{m2} = \sqrt{2K_p'\frac{W}{L}I_D} = \sqrt{2\times 50\mu A/V\times\frac{16}{2}\times 200\mu A} = 400\mu A/V$$

Low-frequency gain given by

$$\frac{v_{out}}{v_{in}} \cong -\frac{g_{m1}}{g_{m2}} = \frac{1600\mu A/V}{400\mu A/V} = -4 = \underline{\underline{12dB}}$$

(iv) Calculate the small-signal voltage gain (v_{out}/v_{in}) of the circuit shown in Figure 1b.
Assume g_{ds3}<<1/R_L.

In Figure 1b the current out of M1 is mirrored with 1:4 ratio to the output, so that the gain becomes g_m times the mirroring ratio times the resistance at the output node.

$$\frac{v_{out}}{v_{in}} \cong -g_{m1}\times 4\times R_L = -1600\mu A/V\times 4\times \underline{\underline{2k\Omega = 12.8}} = 22dB$$

Question 2

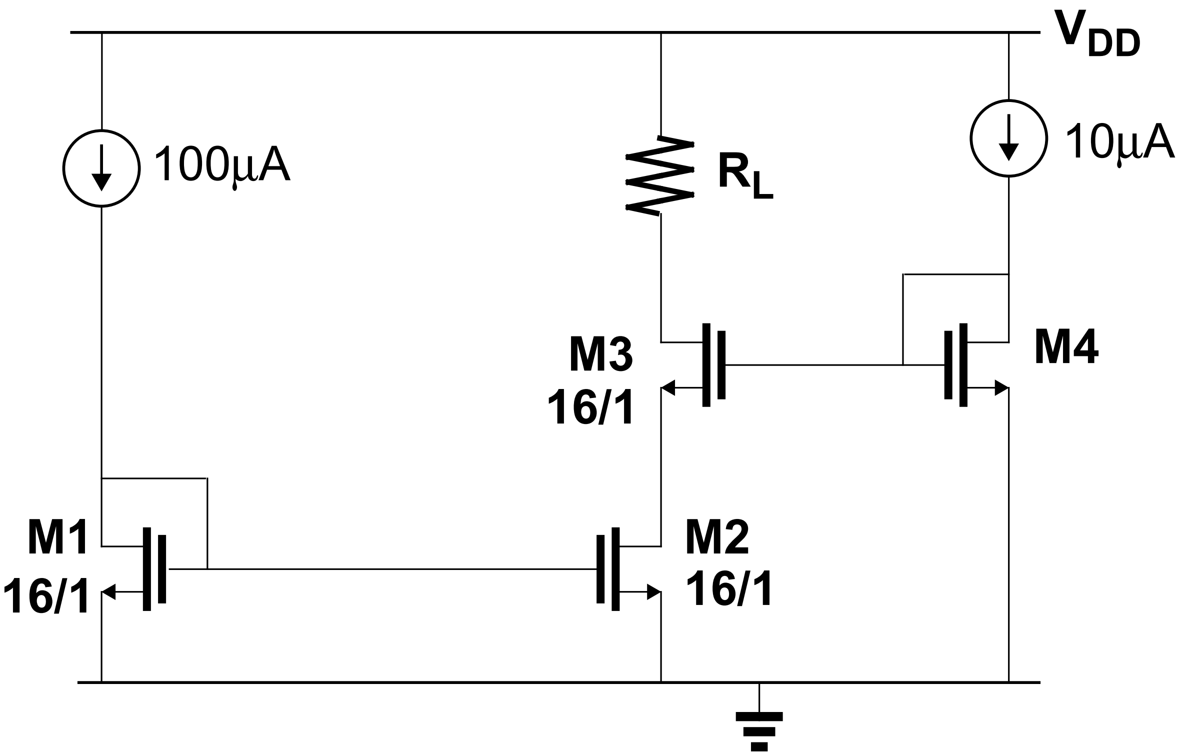


Figure 2

Figure 2 shows an nmos current mirror (M1, M2) with cascoded output. The bias voltage for the cascode is generated by the diode-connected nmos M4 which is biased by a current source as shown.

For this question $K_n' = 200\mu A/V^2$, $V_{tn} = 750mV$, $V_{DD} = 5V$.

The device sizes of M1, M2 and M3 in microns are as indicated in Figure 2.

All devices are biased in saturation.

(i) What is the minimum voltage at the drain of M2 such that M2 is just biased in saturation?
If M4 has L=10, what is the required value of W for M4 such that M2 is just biased in saturation, assuming M3 is in saturation?

(ii) What is then the maximum value of R_L such that M3 is also biased in saturation?

(iii) With M2 just biased in saturation, estimate the percentage inaccuracy of the current mirror due to the finite output conductance of M1 and M2.
For this calculation take $\lambda_n = 0.04V^{-1}$.

(iv) Estimate the 3 sigma percentage inaccuracy of the current mirror due to transistor V_{tn} mismatch.
Note: Assume the mismatch is normally distributed and that the 1 sigma V_{tn} mismatch of a transistor pair (in mV) is given by

$$\sigma_{Vtn} = \frac{A_{Vtn}}{\sqrt{WL}}$$

Take $A_{Vtn} = 10mV\mu m$.

(i) What is the minimum voltage at the drain of M2 such that M2 is just biased in saturation?
If M4 has L=10, what is the required value of W for M4 such that M2 is just biased in saturation, assuming M3 is in saturation?

For M1,M2

$$|V_{GS} - V_t| = \sqrt{\frac{2I_D}{K_n' \frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V^2 \frac{16}{1}}} = 250mV$$

This is the minimum source drain voltage required for M2 to be in saturation.

$$V_{D2min} = \underline{\underline{0.25V}}$$

For M4

As M3 has same dimensions, same current as M1, M2 it has the same V_{GS}

$$V_{GS3} = V_{GS1} = (V_{GS1} - V_t) + V_t = 0.25V + 0.75V = 1V$$

$$V_{GS4} = V_{GS3} + V_{D2min}$$

$$= 1 + 0.25V$$

$$= 1.25V$$

$$I_{D4} = \frac{K_n'}{2}\frac{W}{L}(V_{GS4} - V_t)^2 \Rightarrow W = \frac{2I_{D4}}{K_n' \frac{1}{L}(V_{GS4} - V_t)^2}$$

$$\underline{\underline{W = \frac{2 \cdot 10\mu A}{200\mu A/V^2 \frac{1}{10}(0.5)^2} = 4}}$$

(ii) What is then the maximum value of R_L such that M3 is also biased in saturation?

Maximum voltage at drain of M3

$$V_{D3max} = V_{D2max} + (V_{GS3} - V_t) = 0.25V + 0.25V = 0.5V$$

Maximum value of R_L is then given by

$$R_{Lmax} = \frac{V_{DD} - V_{D3max}}{I_{D3}} = \frac{5V - 0.5V}{100\mu A} = \underline{\underline{45k\Omega}}$$

(iii) With M2 just biased in saturation, estimate the percentage inaccuracy of the current mirror due to the finite output conductance of M1 and M2.
For this calculation take λ_n=0.04V^{-1}.

$$I_{D1} = \frac{K_n'}{2}\frac{W}{L}(V_{GS1} - V_{tn})^2(1 + \lambda_n V_{DS1})$$

$$I_{D2} = \frac{K_n'}{2}\frac{W}{L}(V_{GS2} - V_{tn})^2(1 + \lambda_n V_{DS2})$$

$$\frac{I_{D2}}{I_{D1}} = \frac{1 + \lambda_n|V_{DS2}|}{1 + \lambda_n|V_{DS1}|} = \frac{1 + 0.04 \cdot 0.25}{1 + 0.04 \cdot 1.00} = 0.971$$

Percentage inaccuracy = $\underline{\underline{-2.9\%}}$

(iv) Estimate the 3 sigma percentage inaccuracy of the current mirror due to transistor V_t mismatch.
Note: The 1 sigma V_t mismatch of a transistor pair in mV is given by

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{WL}}$$

Take A_{Vt} = 10mVμm.

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{WL}} = \frac{10mV\mu m}{\sqrt{16\mu m \cdot 1\mu m}} = 2.5mV$$

This is the 1σ mismatch in V_t of M1 and M2

This value is small compared to the overdrive voltage V_{GS}-V_t

=> Use small-signal analysis to calculate inaccuracy

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2 \times 100\mu A}{0.25V} = 0.8mA/V = 0.8\mu A/mV$$

$$\sigma_{I_D} = g_m\sigma_{Vt} = 2.5mV \cdot 0.8\mu A/mV = 2\mu A$$

i.e. 1σ sigma mismatch in drain currents of 2%

3σ percentage mismatch is +/-6%

Question 3

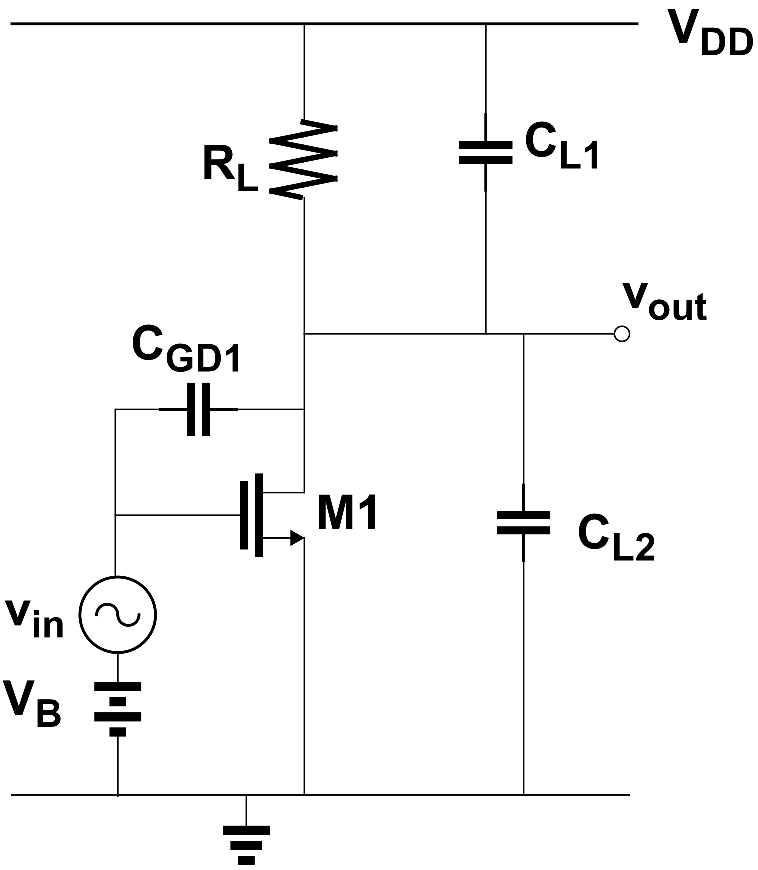


Figure 3

For the questions below you may assume $g_{ds1} << 1/R_L$ and that M1 is biased in saturation.

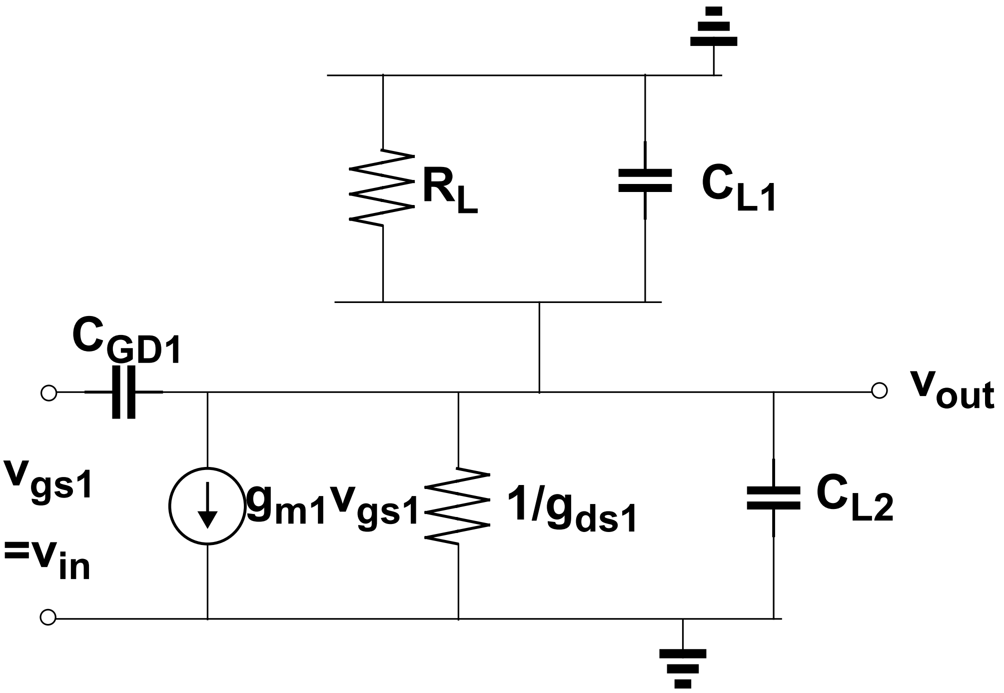
(i) Figure 3 shows a gain stage with an RC load. Draw the small-signal model for this circuit.

(ii) Ignoring all capacitances except C_{GD1}, C_{L1} and C_{L2}, derive an expression for the high-frequency transfer function from v_{in} to v_{out}.

(iii) Calculate the low-frequency gain (v_{out}/v_{in}) and the break frequencies (i.e. pole and/or zero frequencies) if V_B=1V, V_{tn}=0.75V, I_{D1}=250µA, C_{GD1}=0.2pF, C_{L1}=4pF, C_{L2}=5.8pF, R_L=10kΩ.

(iv) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the pole and/or zero frequencies.

(i) Figure 2 shows a gain stage with an RC load. Draw the small-signal model for this circuit.



(ii) Ignoring all capacitances except C_{GD1}, C_{L1} and C_{L2}, derive an expression for the high-frequency transfer function from v_{in} to v_{out}.

KCL at output node:

$$(v_{out} - v_{in})sC_{GD1} + g_m v_{in} + v_{out}g_{ds} + v_{out}/R_L + v_{out}sC_{L1} + v_{out}sC_{L2} = 0$$

$$v_{in}(g_m - sC_{GD1}) + v_{out}(g_{ds} + 1/R_L + s(C_{GD1} + C_{L1} + C_{L2})) = 0$$

$$a(s) = \frac{v_{out}}{v_{in}}(s) = -\frac{g_m - sC_{GD1}}{g_{ds} + 1/R_L + s(C_{GD1} + C_{L1} + C_{L2})}$$

$$a(s) = \frac{v_{out}}{v_{in}}(s) = -\frac{g_m}{g_{ds} + 1/R_L}\left(\frac{1 - s\dfrac{C_{GD1}}{g_m}}{1 + \dfrac{s(C_{GD1} + C_{L1} + C_{L2})}{g_{ds} + 1/R_L}}\right)$$

(iii) Calculate the low-frequency gain (v_{out}/v_{in}) and the break frequencies (i.e. pole and/or zero frequencies) if V_B=1V, V_{tn}=0.75V, I_{D1}=250μA, C_{GD1}=0.2pF, C_{L1}=4pF, C_{L2}=5.8pF, R_L=10kΩ.

$$g_{m1} = \frac{2I_{D1}}{(V_{GS1}-V_{tn})} = \frac{2\times 250\mu A}{1-0.75} = 2000\mu A/V$$

Low-frequency gain given by

$$\frac{v_{out}}{v_{in}} \cong -\frac{g_{m1}}{g_{ds1}+1/R_L} \approx -g_{m1}R_L = -2000\mu A/V\times 10k = -20 \Rightarrow 26dB$$

Zero frequency given by

$$|\omega_z| = \frac{g_{m1}}{C_{GD1}} = \frac{2000\mu A/V}{0.2pF} = 10Grad/s$$

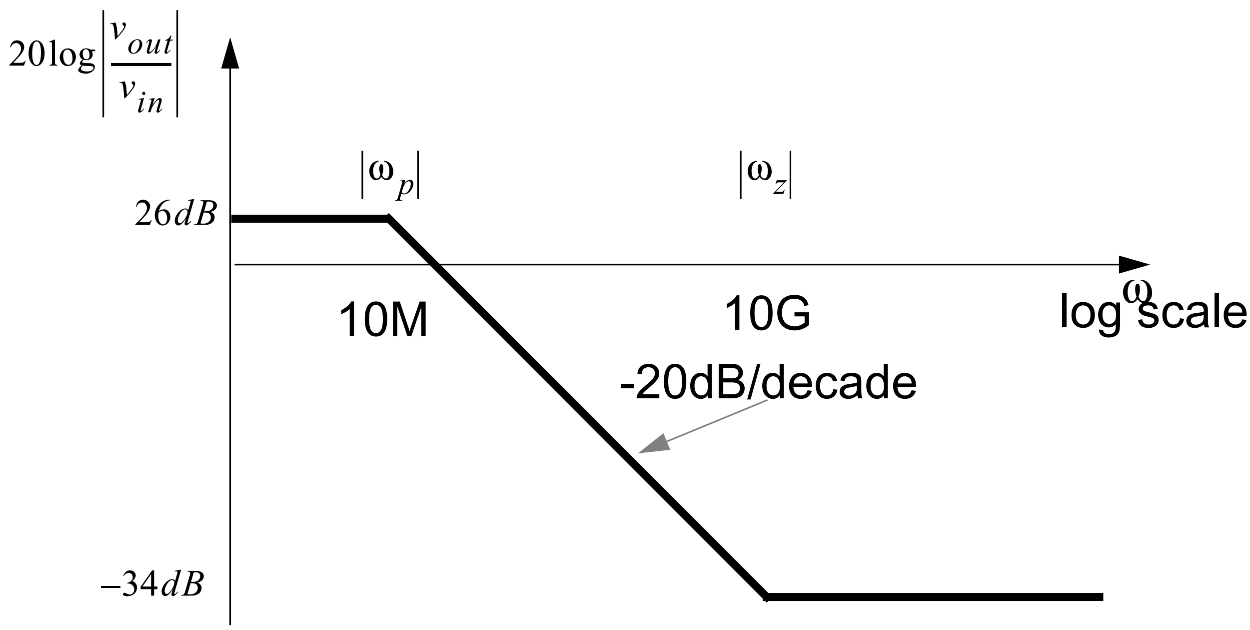
Pole frequency given by

$$|\omega_p| = \frac{g_{ds}+\frac{1}{R_L}}{C_{L1}+C_{L2}+C_{GD1}} \approx \frac{\frac{1}{R_L}}{C_{L1}+C_{L2}+C_{GD1}}$$

$$|\omega_p| = \frac{\frac{1}{10k\Omega}}{4pF+5.8pF+0.2pF} \approx \frac{1}{10k\Omega\times 10pF} = 10Mrad/s$$

(iv) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the pole and zero frequencies.

Zero is 3 decades down, so gain at high frequecies = -34dB



Question 4

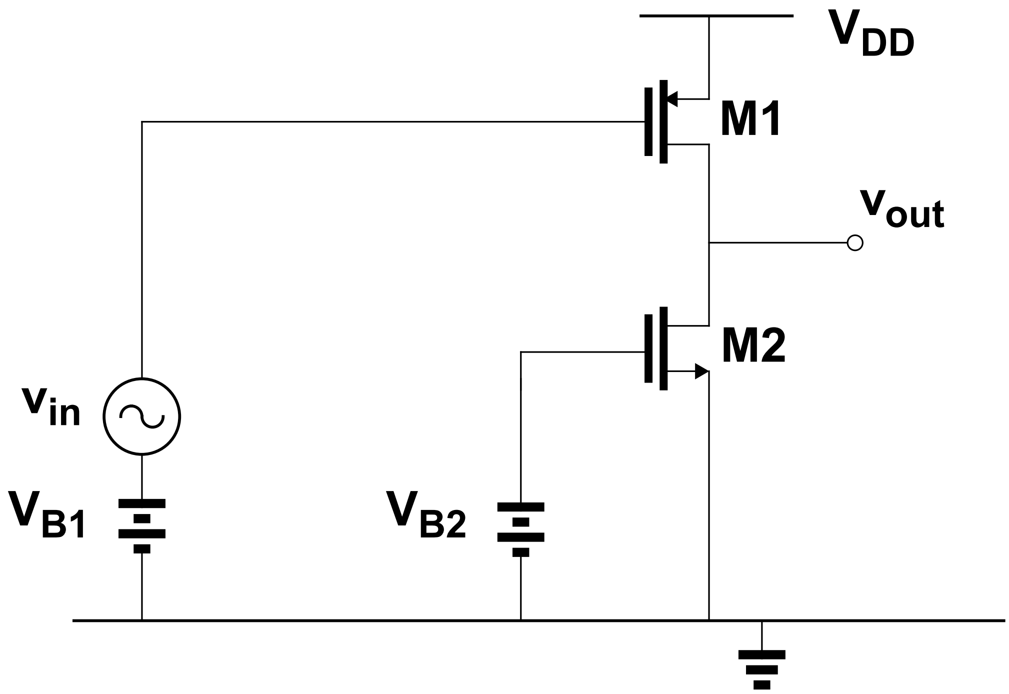


Figure 4

Assume M1 and M2 are operating in saturation. Only thermal noise sources need be considered.

For calculations take Boltzmann's constant $k=1.38X10^{-23}J/^{o}K$, temperature $T=300^{o}K$.

(i) Draw the small-signal model for the circuit shown in Figure 4.
What is the low-frequency small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters of M1 and M2?

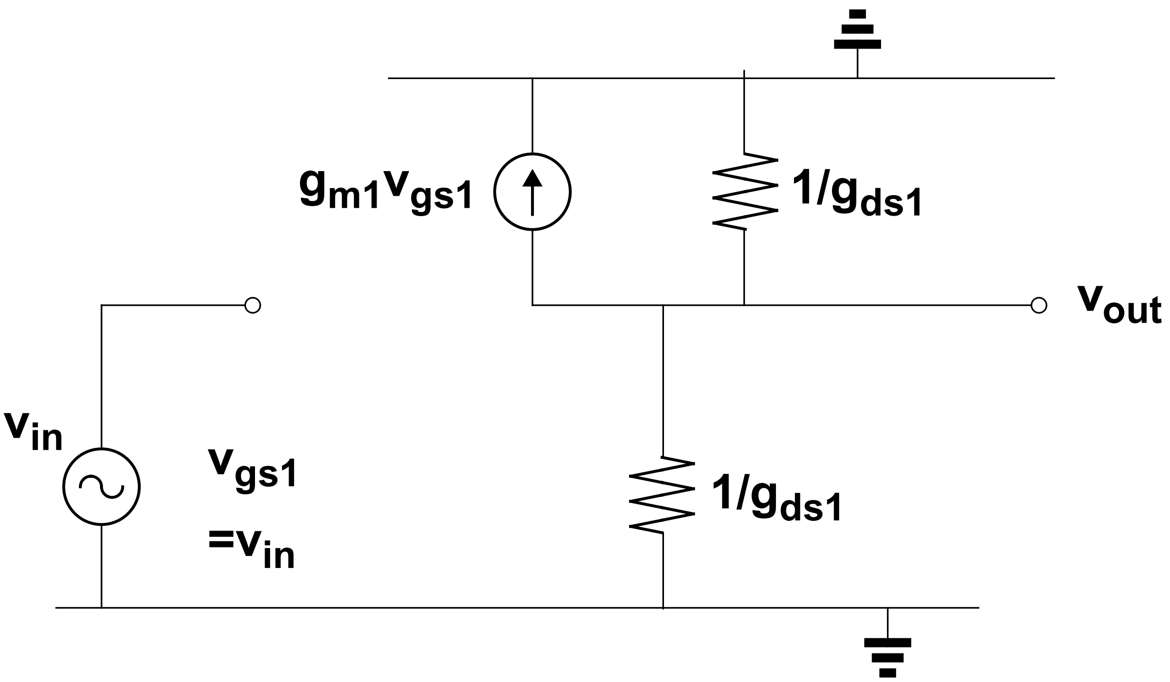
(ii) What is the input-referred thermal noise voltage density of the circuit shown in Figure 4?
The answer should be in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T.

(iii) Calculate the input-referred thermal noise voltage density of the circuit if
V_{B1}=2.0V, V_{B2}=1.75V, V_{DD}=3V, V_{tn} = 0.75V, V_{tp} = -0.75V, $\lambda_n=\lambda_p=0.04V^{-1}$.
The drain current of M2 is 200µA.
What is the thermal noise voltage density at the output of the circuit?

(iv) If the input signal v_{in} is a $1mV_{rms}$ sine wave with negligible noise, calculate the maximum bandwidth for which the signal-to-noise ratio at the output is 60dB.

Solution

(i) Draw the small-signal model for the circuit shown in Figure 4.
What is the low-frequency small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters of M1 and M2?

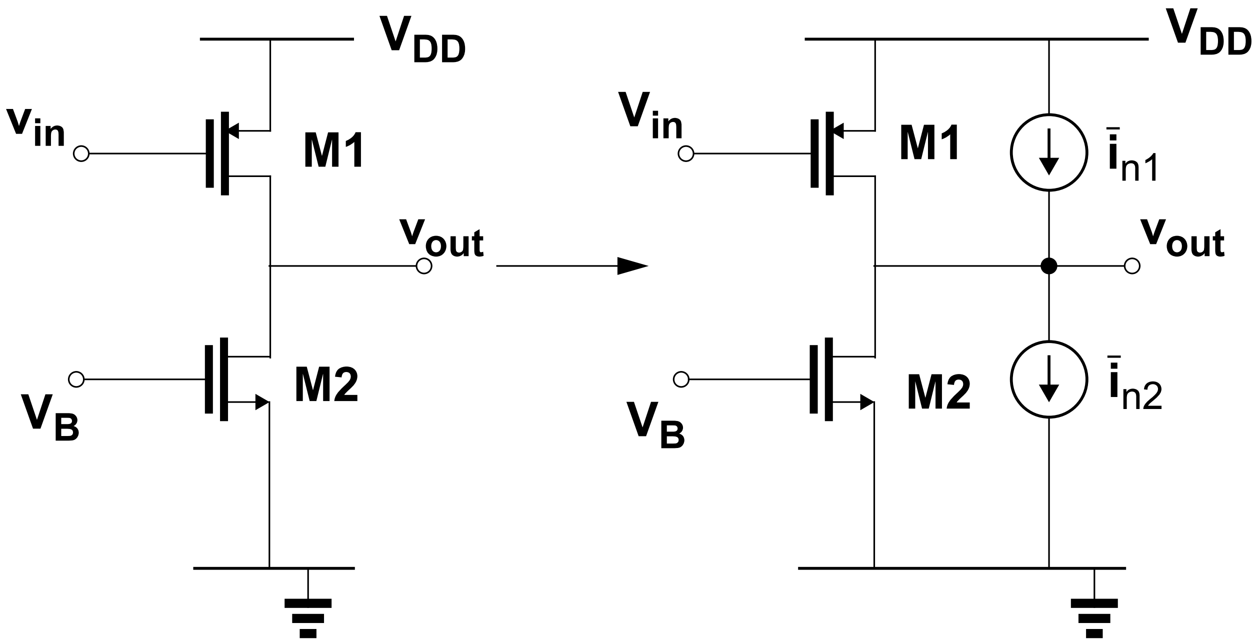


Current at output node

$$g_{m1}v_{in} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

(ii) What is the input-referred thermal noise voltage density of the circuit shown in Figure 4? The answer should be in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T.?



Noise current density of MOS:

$$\overline{i_n^2} = 4kT\left(\frac{2}{3}g_m\right) \qquad A^2/Hz$$

$$\overline{i_n} = \sqrt{4kT\left(\frac{2}{3}g_m\right)} \qquad A/\sqrt{Hz}$$

Total noise current at output is square root of the individual noise currents

$$\overline{i_{nt}} = \sqrt{i_{n1}^2 + i_{n2}^2} = \sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}$$

Input-referred noise voltage given by

$$\overline{v_{ni}} = \frac{\overline{i_{nt}}}{g_{m1}} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right) + 4kT\left(\frac{2}{3}g_{m2}\right)}}{g_{m1}} \qquad V/\sqrt{Hz}$$

(iii) Calculate the input-referred thermal noise voltage density of the circuit if V_{B1}=2.0V, V_{B2}=1.75V, V_{DD}=3V, V_{tn} = 0.75V, V_{tp} = -0.75V, $\lambda_n=\lambda_p=0.04V^{-1}$.
The drain current of M2 is 200μA.
What is the thermal noise voltage density at the output of the circuit?

g_m given by

$$g_m = \frac{2I_D}{(|V_{GS}|-|V_{tp}|)}$$

$$g_{m1} = \frac{2 \cdot 200\mu A}{1V - 0.75V} = 1600\mu A/V \qquad g_{m2} = \frac{2 \cdot 200\mu A}{1.75V - 0.75V} = 400\mu A/V$$

$$\overline{v_{ni}} = \frac{\sqrt{4kT\left(\frac{2}{3}(g_{m1} + g_{m2})\right)}}{g_{m1}}$$

$$\overline{v_{nitot}} = \frac{\sqrt{(4 \cdot 1.38\times10^{-23} \cdot 300)\left(\frac{2}{3}\right)(1600\mu A/V + 400\mu A/V)}}{1600\mu A/V} = \underline{\underline{2.94nV/\sqrt{Hz}}}$$

$$g_{ds1} = \lambda_n I_D = 0.04V^{-1}200\mu A = 8\mu A/V$$
$$g_{ds2} = \lambda_n I_D = 0.04V^{-1}200\mu A = 8\mu A/V$$

Gain of stage

$$Gain = -\left(\frac{g_{m1}}{g_{ds1} + g_{ds2}}\right) = -\frac{1600\mu A/V}{16\mu A/V} = -100$$

$$\overline{v_{notot}} = \overline{v_{nitot}} \cdot \left(\frac{g_{m1}}{g_{ds1} + g_{ds2}}\right) = \underline{\underline{294nV/\sqrt{Hz}}}$$

(iv) If the input signal v_{in} is a $1mV_{rms}$ sine wave, calculate the maximum bandwidth for which the signal-to-noise ratio at the output is 60dB.

Total noise at output given by

$$\overline{v_{notot}} = \overline{v_{nitot}} \cdot \left(\frac{g_{m1}}{g_{ds1}+g_{ds2}}\right) \cdot \sqrt{BW}$$

Output signal

$$v_{out} = -\left(\frac{g_{m1}}{g_{ds1}+g_{ds2}}\right) v_{in} = -100 \cdot 1mV_{rms} = 100mV_{rms}$$

Signal-to-Noise ratio given by

$$\frac{S}{N} = \frac{v_{out}}{\overline{v_{nitot}} \cdot \left(\frac{g_{m1}}{g_{ds1}+g_{ds2}}\right) \cdot \sqrt{BW}} = 1000$$

i.e. 60dB

$$BW = \left(\frac{v_{out}}{\overline{v_{nitot}} \cdot \left(\frac{g_{m1}}{g_{ds1}+g_{ds2}}\right) \cdot \frac{S}{N}}\right)^2 = \left(\frac{100mV}{2.94nV/\sqrt{Hz} \cdot (100) \cdot 1000}\right)^2 = \underline{\underline{115.7kHz}}$$