Part A

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an nmos in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.
In each question, capacitances other than those mentioned may be ignored.

Question 1

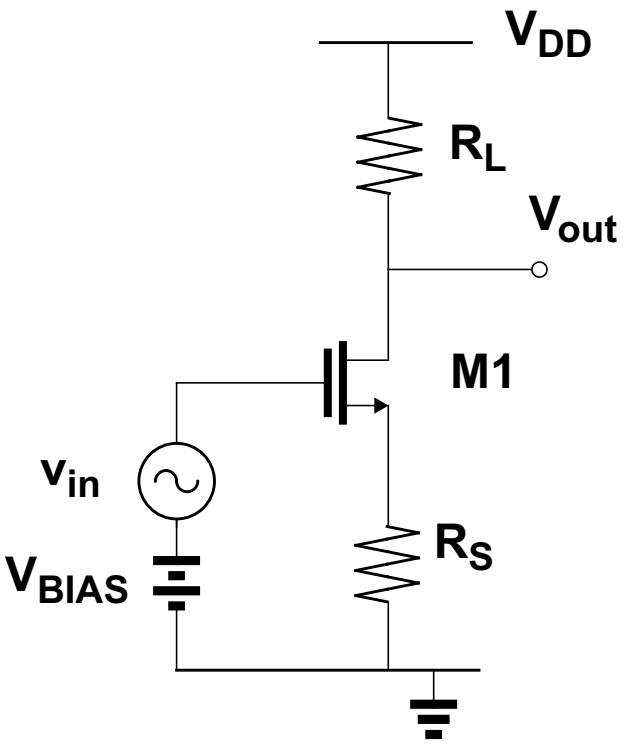


Figure 1

(i) Draw the small-signal equivalent circuit for the gain stage shown in Figure 1.
(ii) Show that (assuming $g_{m1}>>g_{ds1}$, $1/g_{ds1} >> R_L$, $1/g_{ds1} >> R_S$) the small-signal voltage gain is given by

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_L}{1+g_m R_S}$$

(iii) Calculate the small-signal voltage gain with the following conditions:
$K_n'=200\mu A/V^2$, $V_{tn}=0.7V$, $I_{D1}=200\mu A$, $R_L=10k\Omega$, $R_S=1k\Omega$, $V_{DD}=5V$, $W/L_{M1}=12.5/1$
(iv) What is the largest value of gain that can be achieved by increasing R_L?

Question 2

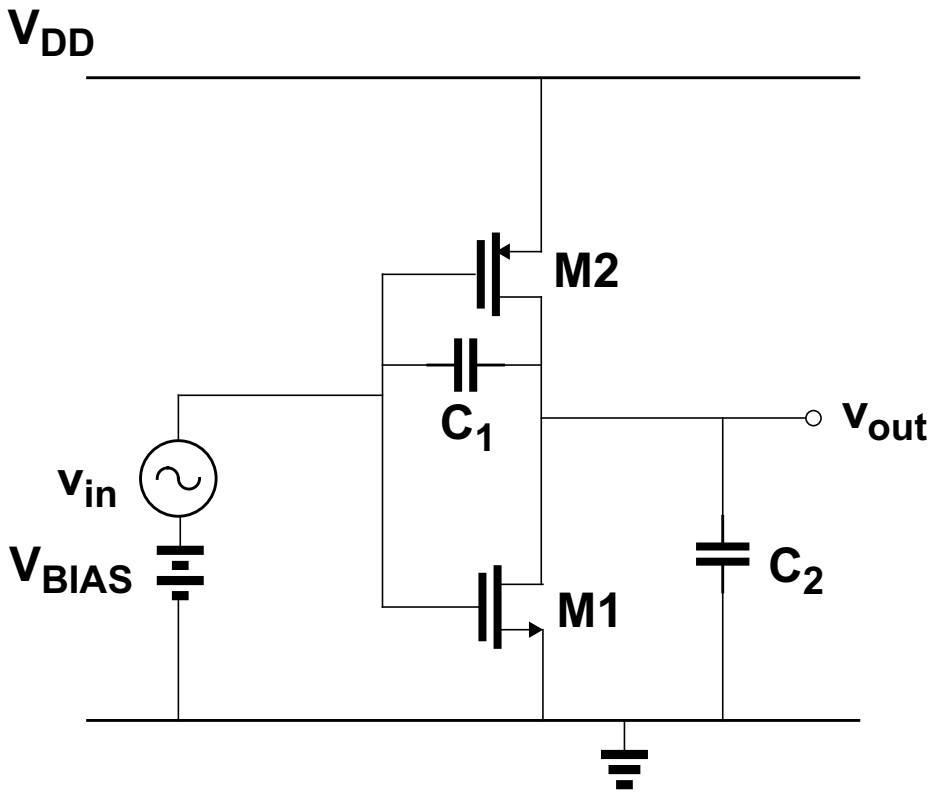


Figure 2

(i) Draw the small-signal equivalent circuit for the CMOS inverter stage shown in Figure 2.
(ii) Ignoring all capacitances except C_1 and C_2 derive an expression for the high frequency transfer function (v_{out}/v_{in})
(iii) Calculate the pole and zero frequencies if
V_{BIAS}=1.5V, V_{tn}=0.7V, V_{tp}=-0.7V, $\lambda_n=\lambda_p=0.04V^{-1}$, C_1=0.1pF, C_2=1.5pF.
Assume both transistors are in saturation with a drain current of 200μA.
(iv) Draw a Bode diagram of the gain. Indicate in dB the dc gain and the gain at frequencies well above the pole and zero frequencies.

Question 3

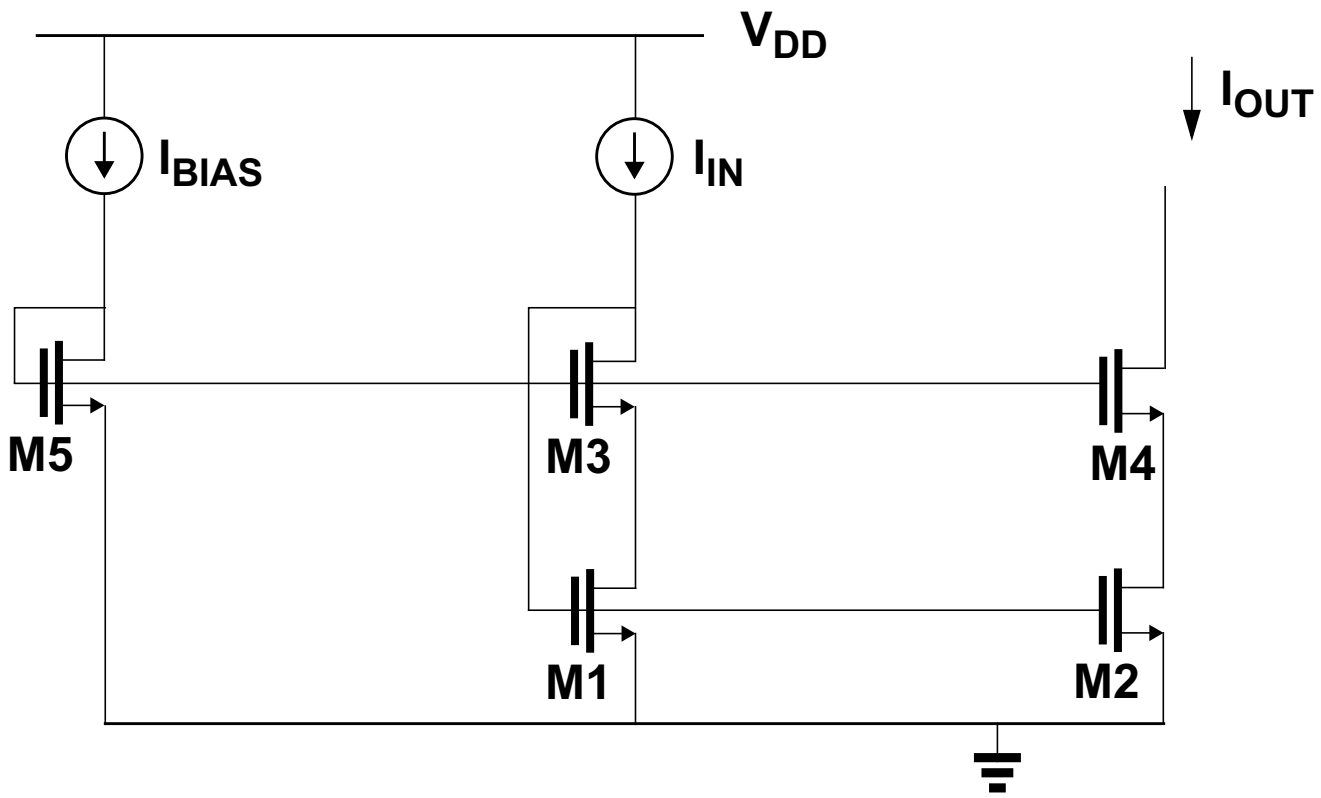


Figure 3

Figure 3 shows a cascode current mirror. Note that the drain of M3 is not connected to the gate of M3. Assume M1, M2, M3 and M4 have equal dimensions.
K_n'=200µA/V^2, V_{tn}=750mV, I_{IN}=250µA.

(i) The current mirror transistors M1 and M2 are to have a gate overdrive voltage (V_{GS}-V_{tn}) of 0.5V.
What is the required W/L for M1 and M2?
What minimum voltage at the gates of M3 and M4 is required such that M1 and M2 are just biased in saturation?

(ii) M5 is to be dimensioned such that M1 and M2 are just biased in saturation.
What is the required W/L of M5 if I_{BIAS} = I_{IN}/10?
What is the minimum voltage at the output such that M4 is also in saturation?

(iii) It is required to calculate the small-signal input resistance of the current mirror (i.e. the resistance looking into the drain of M3). Draw a small-signal model showing how this can be done.

(iv) Derive an expression for the small-signal input resistance of the current mirror. Simplify the expression assuming g_m>>g_{ds} for each transistor.

Question 4

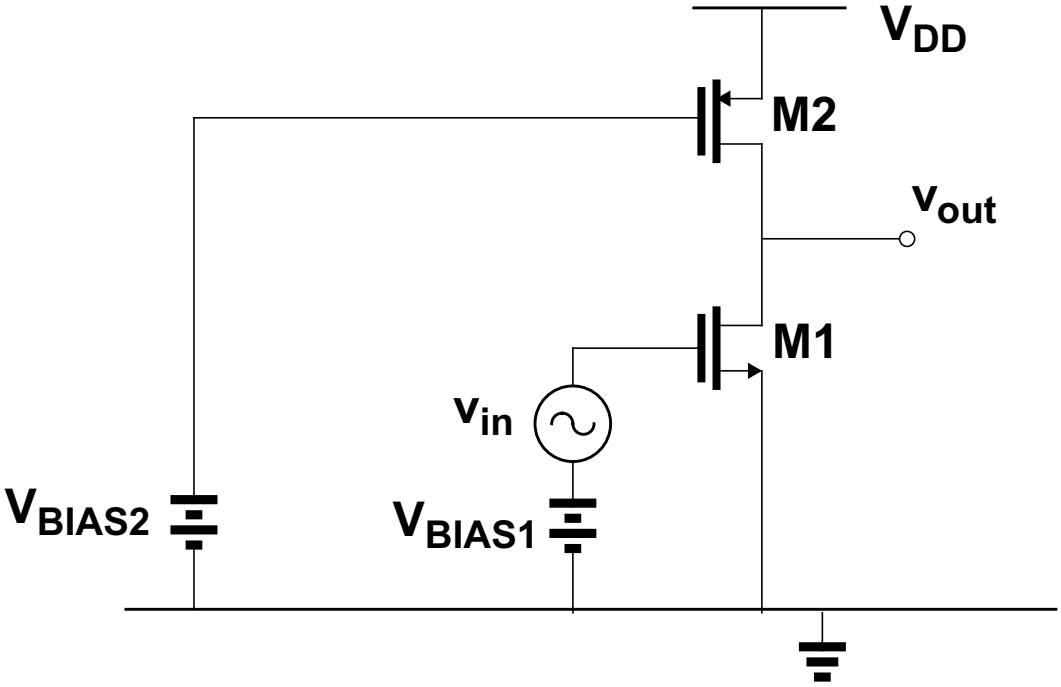


Figure 4

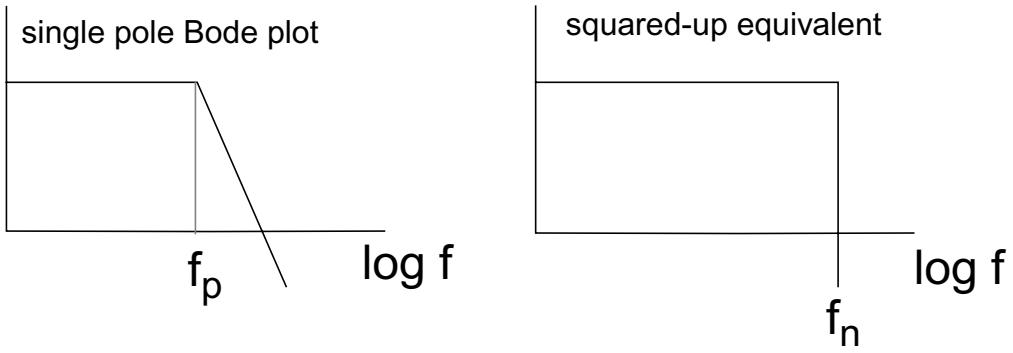
Assume M1 and M2 are operating in saturation. Only thermal noise sources need be considered.

(i) Draw the small-signal model for the circuit shown in Figure 4.
What is the low-frequency small-signal voltage gain (v_{out}/v_{in})?

(ii) What is the input-referred thermal noise voltage in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T?

(iii) If a capacitor C_L is connected between the output node and ground what is the total integrated thermal noise at the output node?

You may assume the following:



For the area underneath the curves to be the same then $f_n=(\pi/2)*f_p$

(iv) Using the result of (iii) calculate the signal-to noise ratio at the output if the input signal v_{in} is a $1mV_{rms}$ sine wave with a frequency much lower than the frequency of the pole at the output node.
For this calculation take V_{BIAS1}=1.0V, V_{BIAS2}=2.0V, V_{DD}=3V, V_{tn} = 0.75V, V_{tp} = -0.75V, $\lambda_n=\lambda_p=0.04V^{-1}$, C_L=10pF.
The drain current of M1 is 100μA.
Assume Boltzmann's constant $k=1.38X10^{-23}J/^oK$, temperature $T=300^oK$.