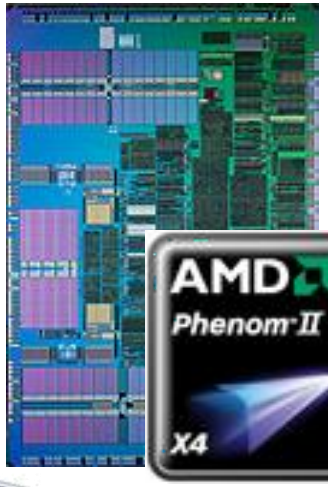
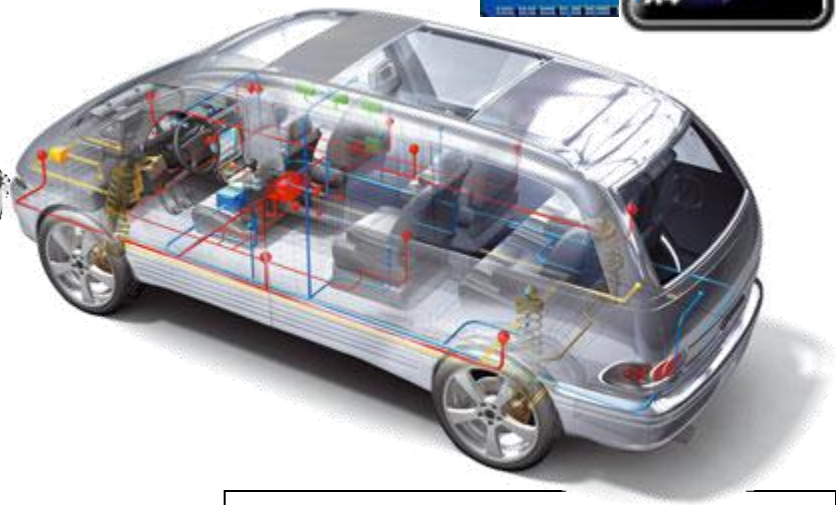
What is SOI?

Do we really need it?

Benefit for Processors, RF and High-Temperature applications





JP Colinge

Tyndall National Institute
University College Cork
Cork, Ireland

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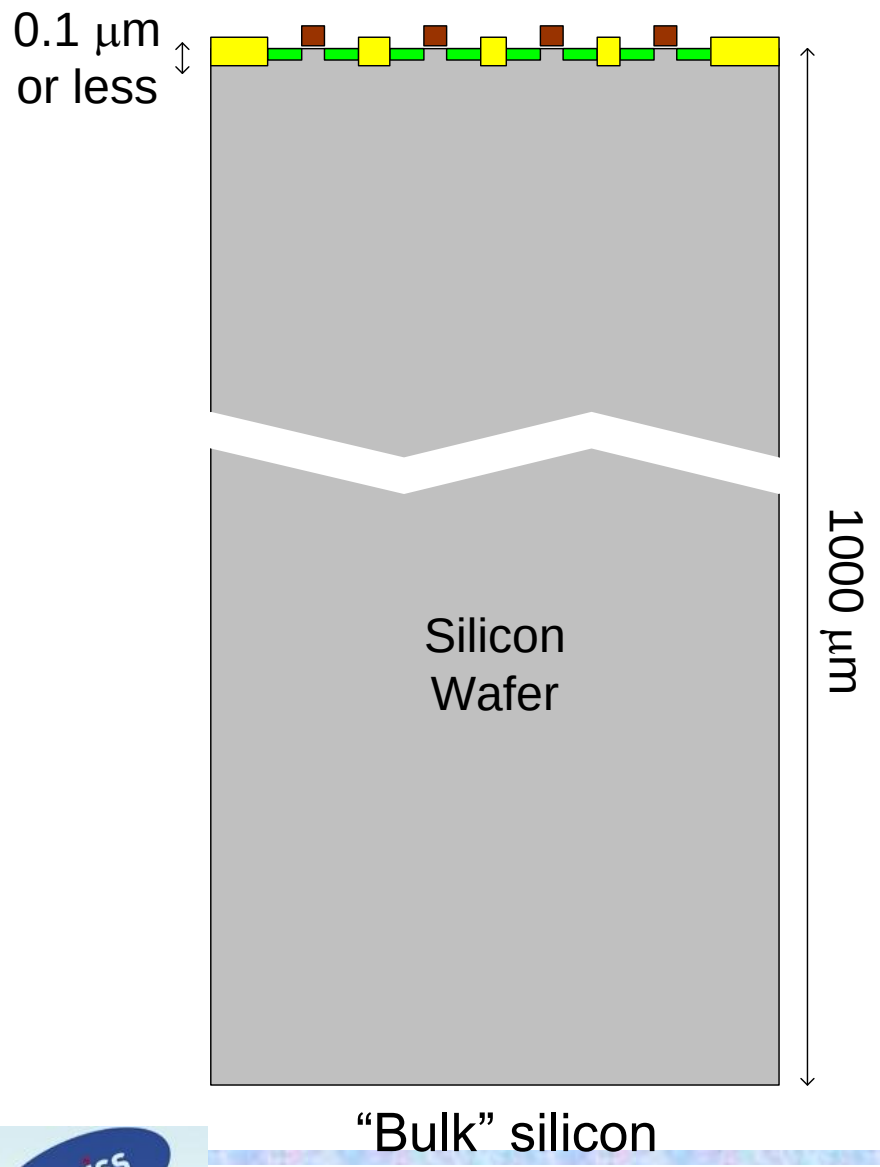
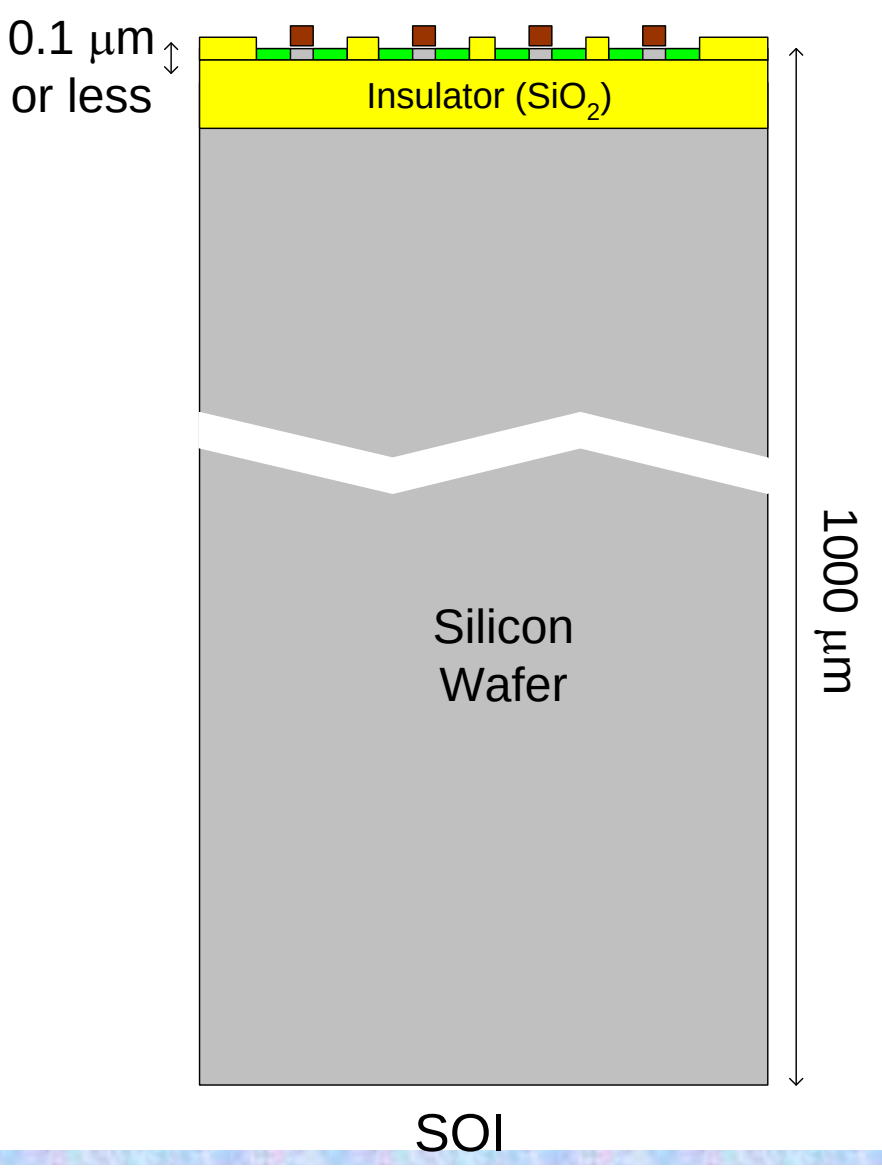
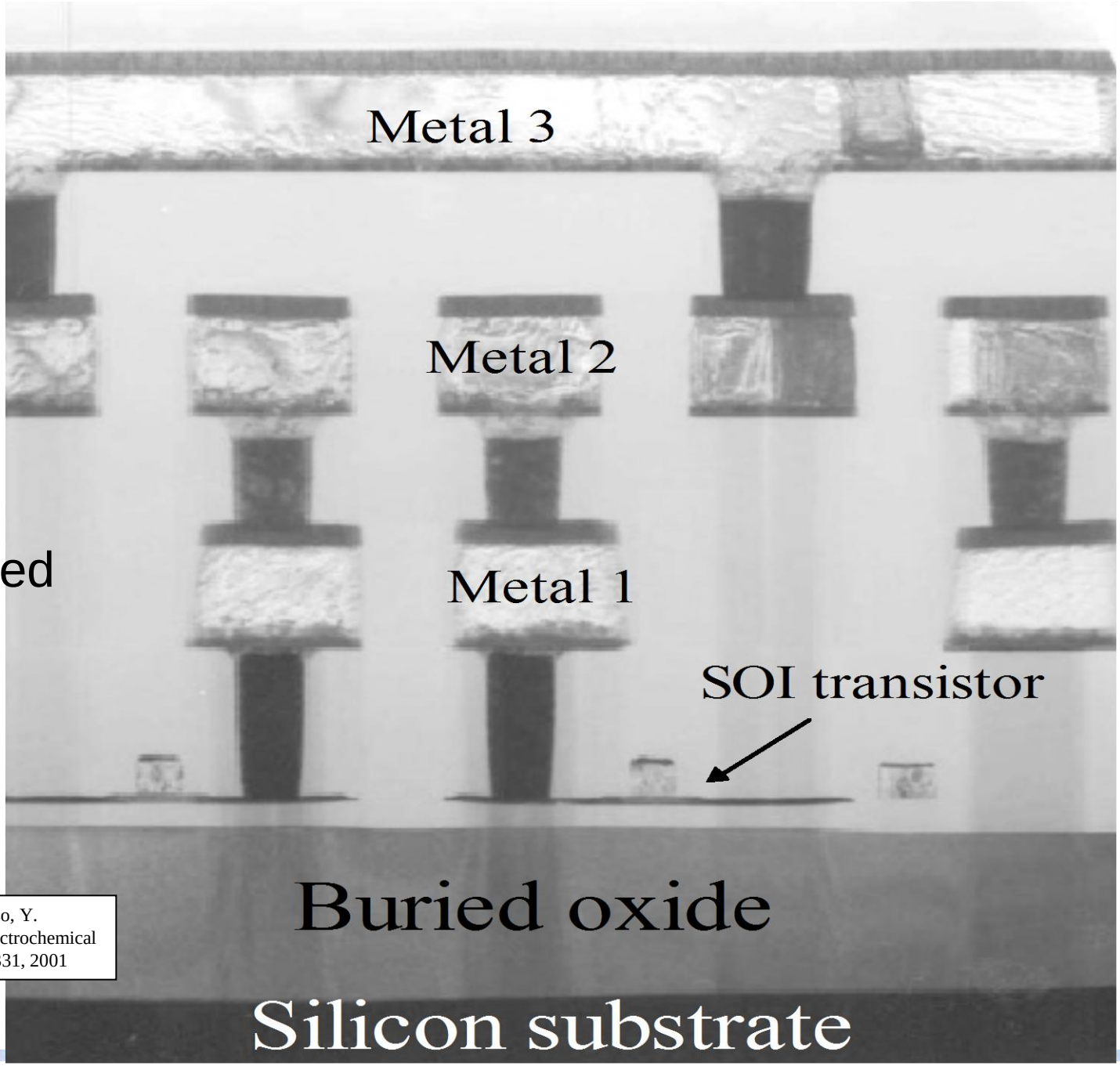
SOI = Silicon On Insulator





OKI, 2001

Fully Depleted



M. Itoh, Y. Kawai, S. Ito, K. Yokomizo, Y. Katakura, Y. Fukuda, F. Ishikawa, Electrochemical Society Proceedings, Vol. 2001-3, p. 331, 2001

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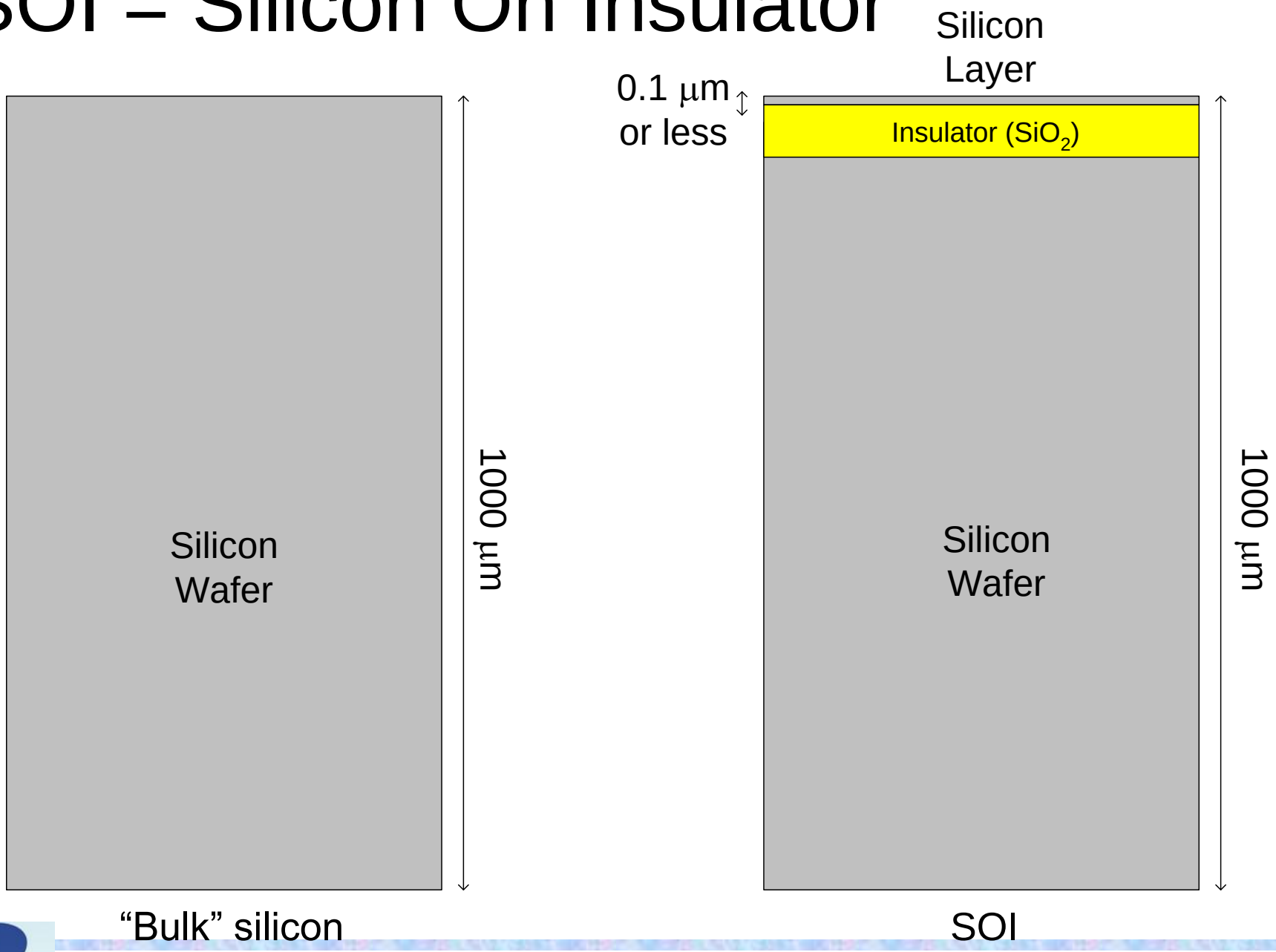
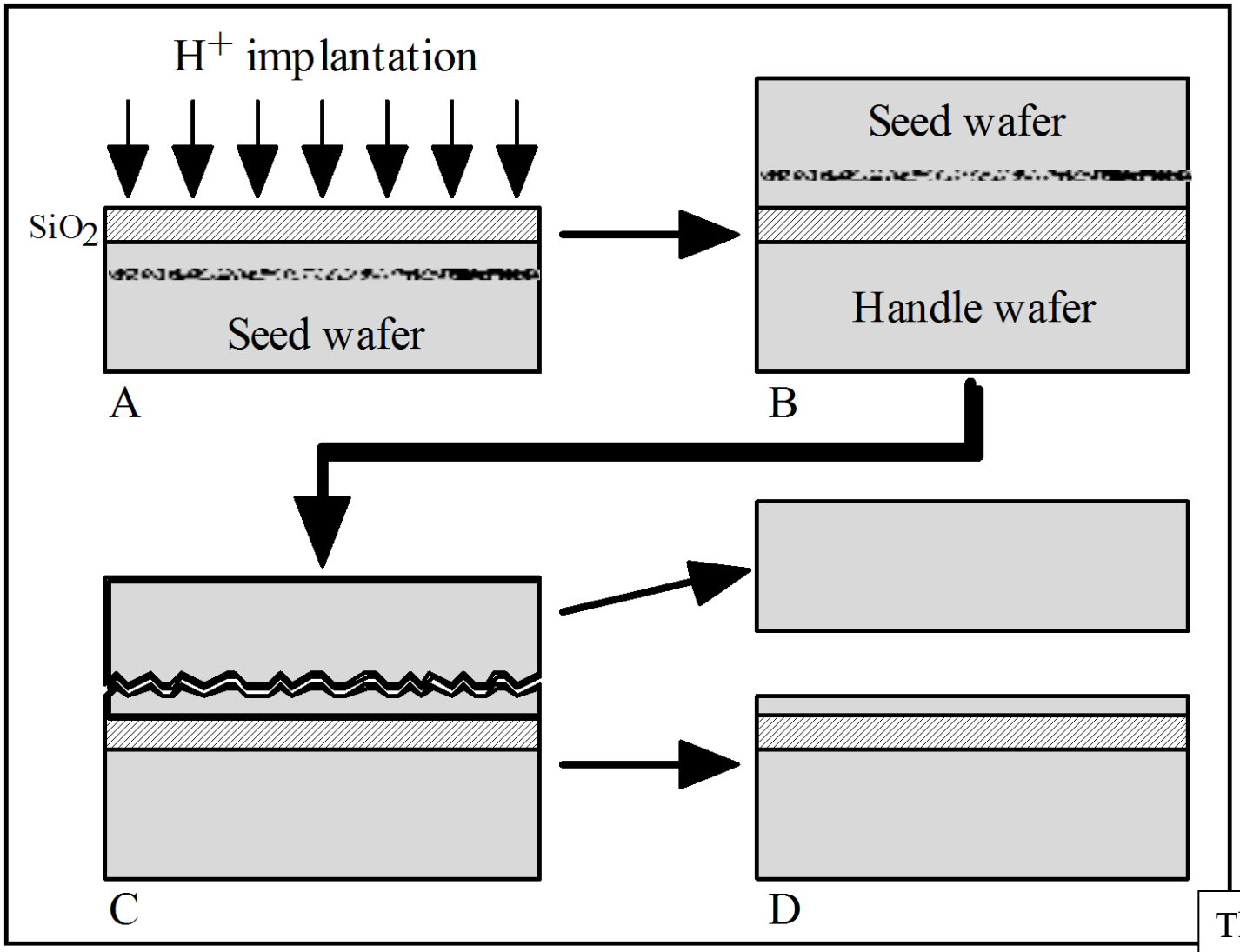
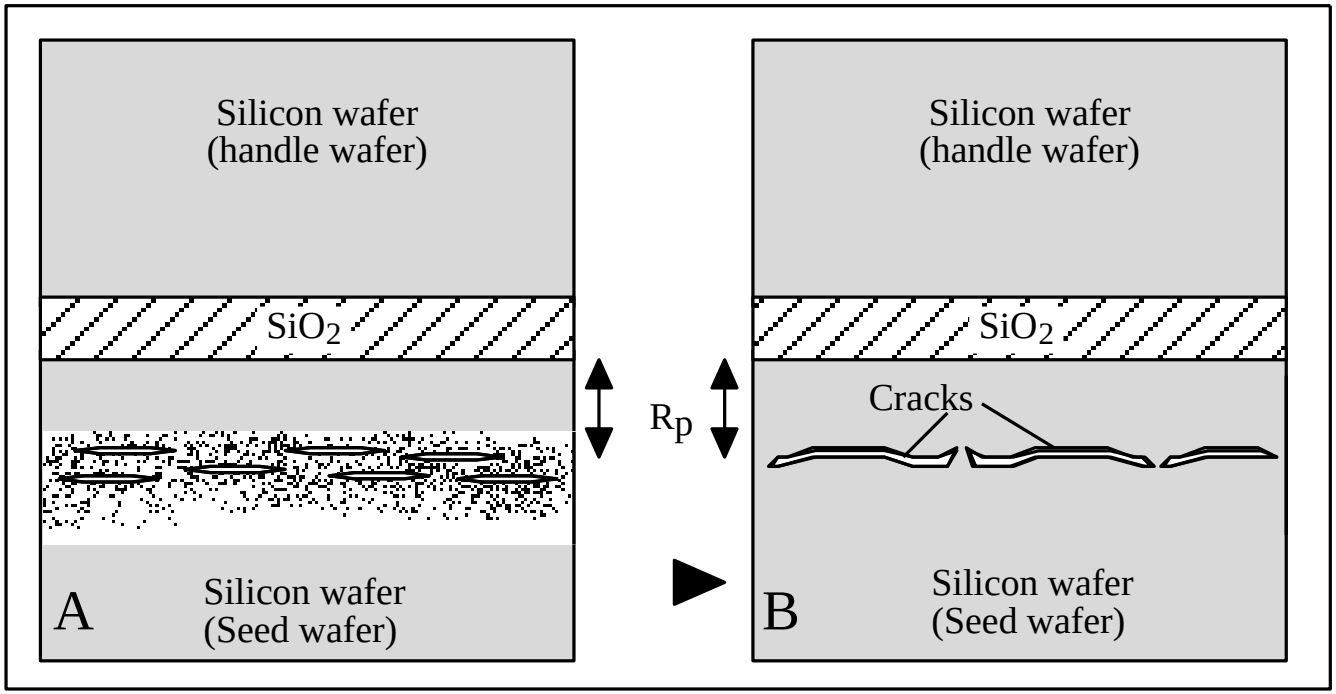


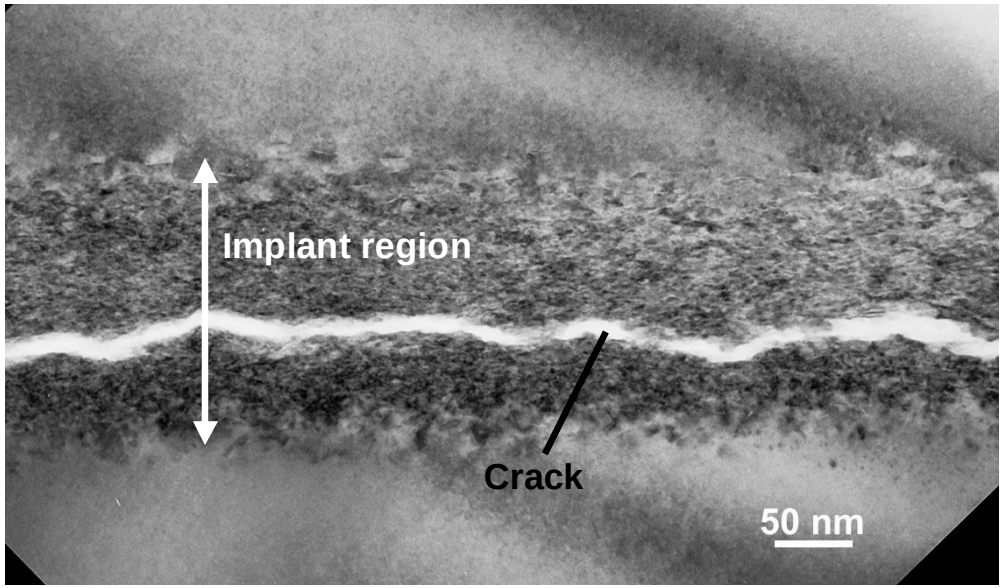


SOI Wafer Fabrication

The Smart-Cut® process:
A: Hydrogen implantation
B: Wafer bonding
C: Splitting of wafer A
D: Polishing



Formation of cracks near the projected range of a silicon wafer implanted with hydrogen.
A: Bonding of the handle wafer to the seed wafer
B: Formation of a crack network near the projected range upon annealing.



TEM micrograph of a crack

Product Family	Thin SOI		HM UNIBOND™	Thick SOI		
Products by Applications	Ultra-Thin UNIBOND™ XUT, XUT+	Ultra-Thin UNIBOND™ UTSOI	sSOI	UNIBOND™	UNIBOND™ + Epi	Engineered BSOI
CMOS logic	●	●	●			
Power management ICs				●	●	●
Analog & mixed signal	●			●	●	●
RF & microwave components	●			●	●	
Discrete power devices					●	●
Radiation hard & high temperature ICs	●			●	●	●
Imaging					●	●
M(0)EMS	●			●	●	●
Memories	●					
Silicon photonics	●					
Solid state lighting						

● Current offering

www.soitec.com

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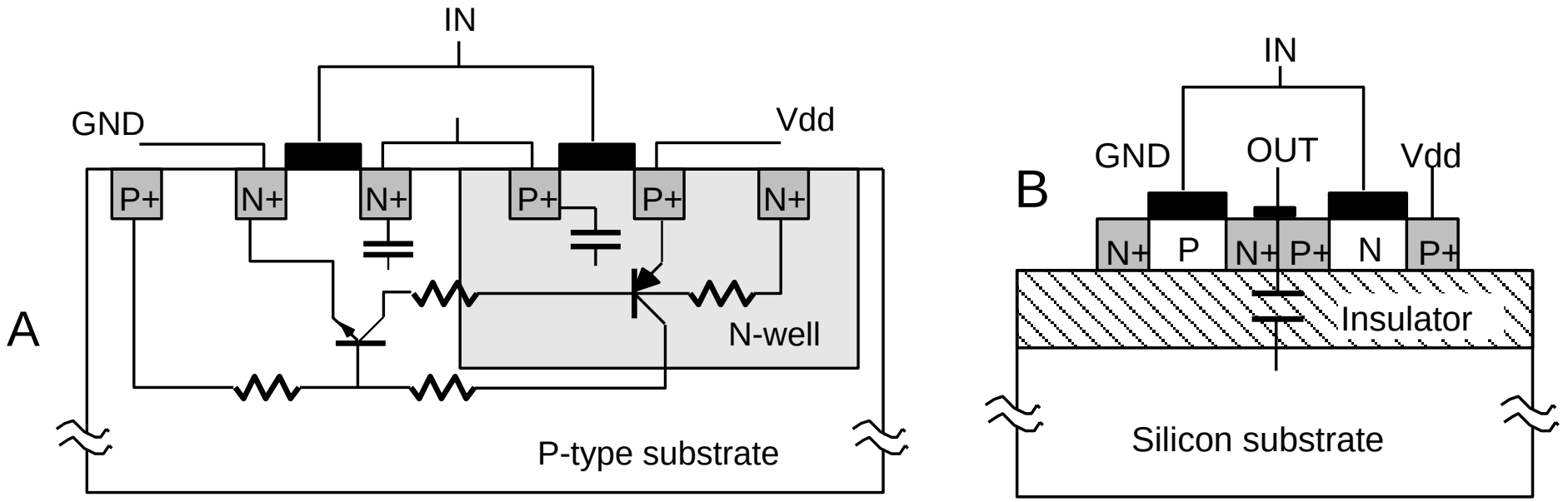
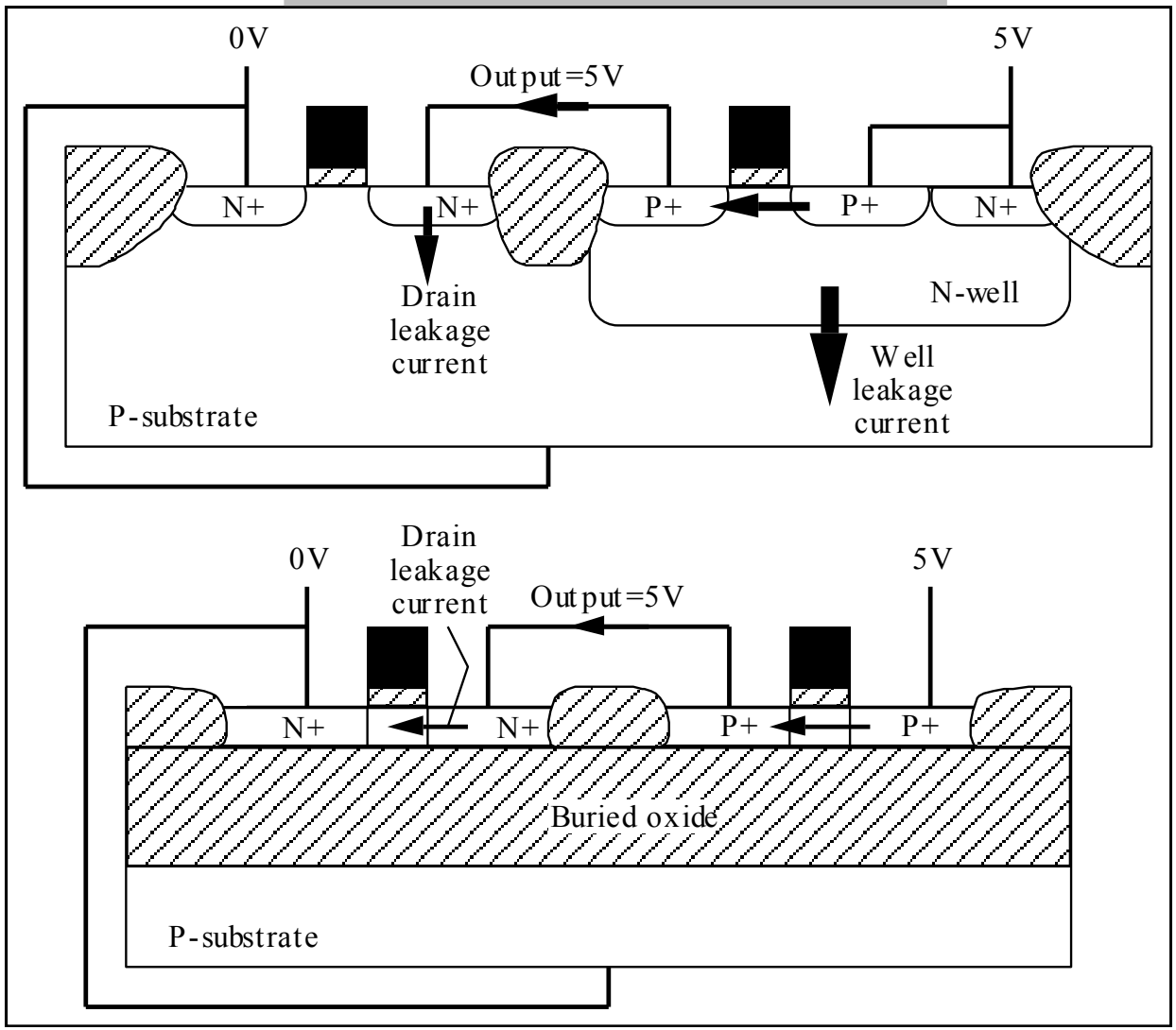
Latch-up and S&D capacitances



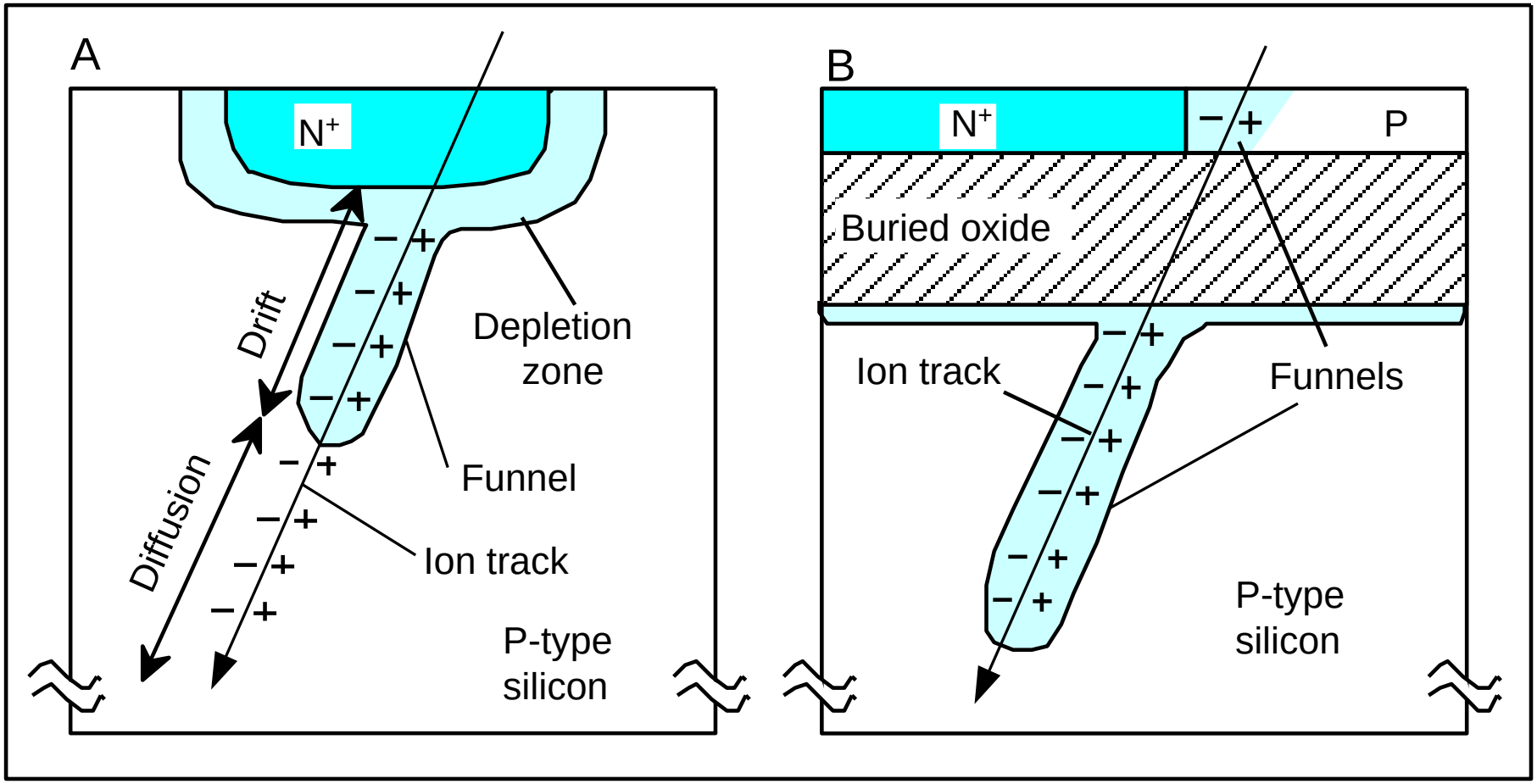
A: Cross section showing the latchup path in a bulk CMOS inverter.
B: Cross section of an SOI CMOS inverter.
The drain parasitic capacitances are also presented.

Leakage currents



Leakage current paths in bulk (top) and SOI (bottom) CMOS inverters.
No current flow to the substrate is allowed in SOI.

Soft Errors



Ion strike on A: a bulk PN junction, and B: an SOI junction.

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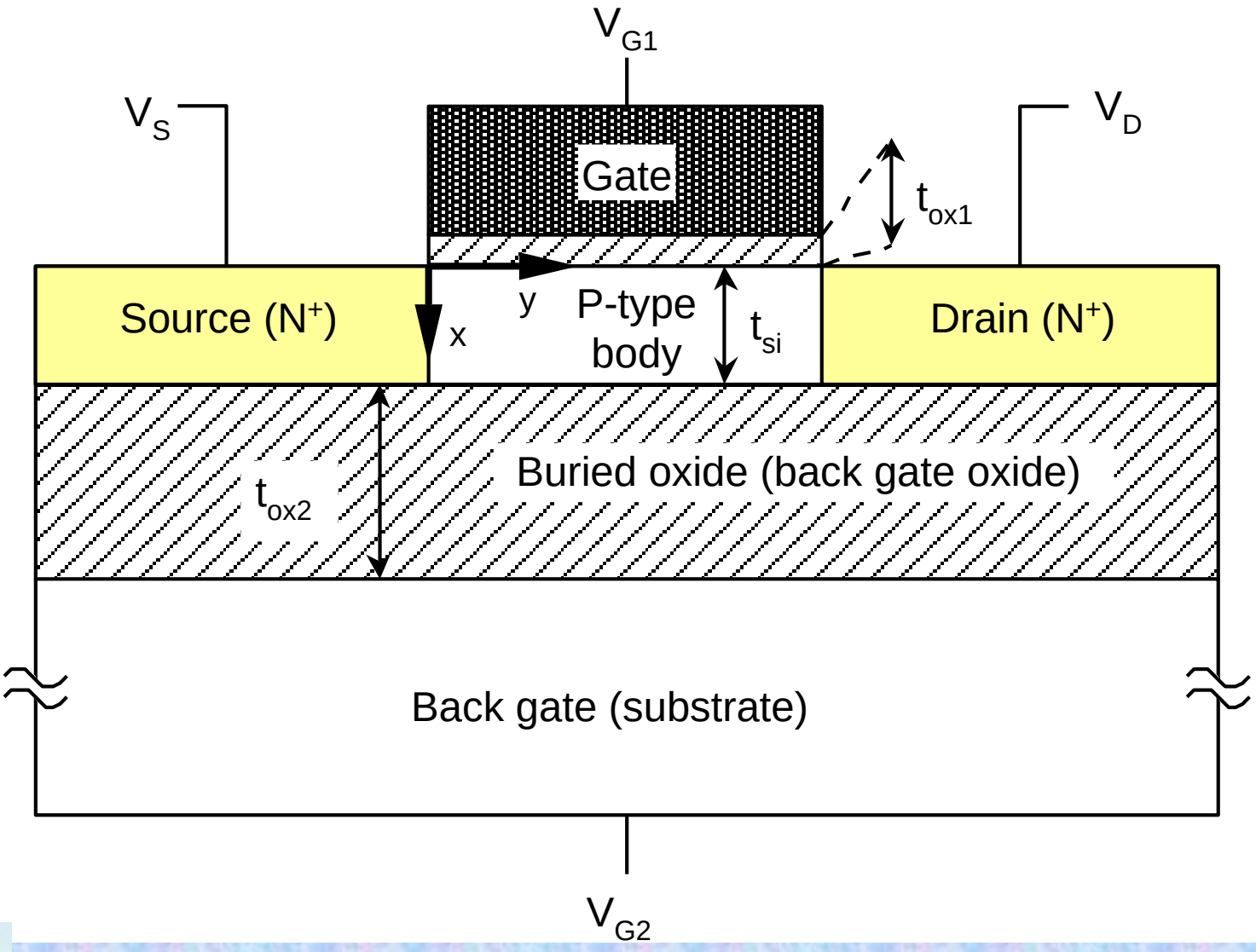
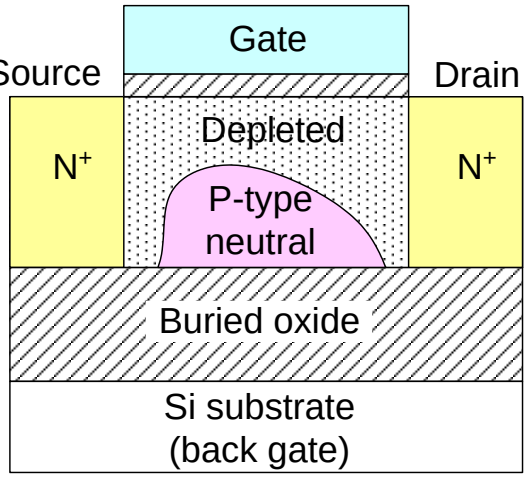
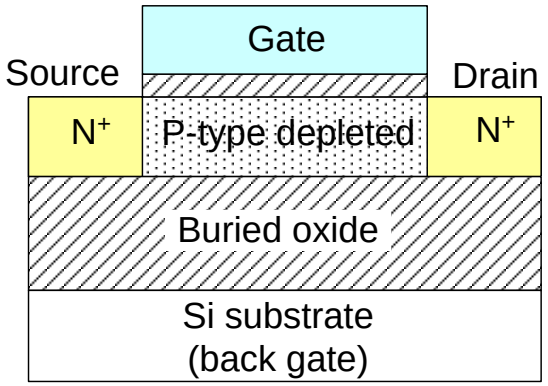
A few definitions….



Types of (single-gate) SOI MOSFETs

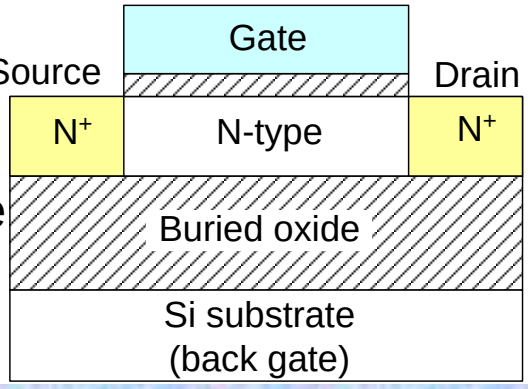
Partially depleted SOI MOSFET

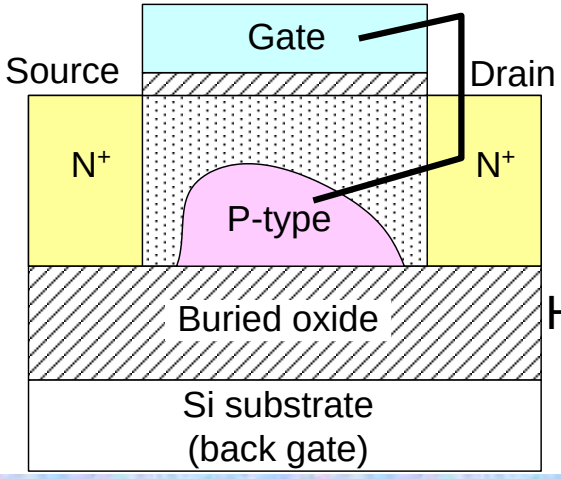




Fully depleted SOI MOSFET

Accumulation-mode SOI MOSFET





Hybrid/MTCMOS/ DTMOS FET

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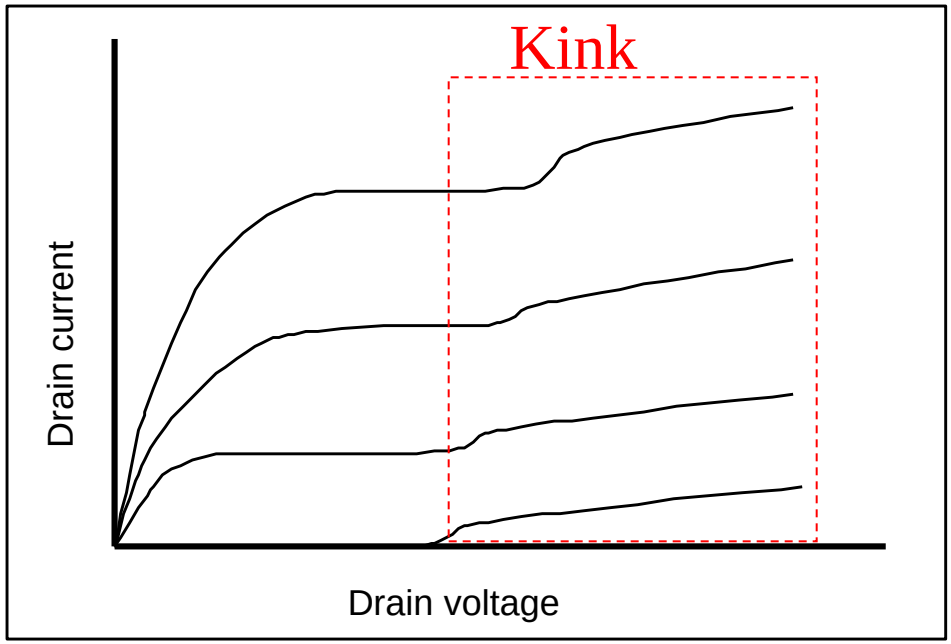
Kink Effect: Implications



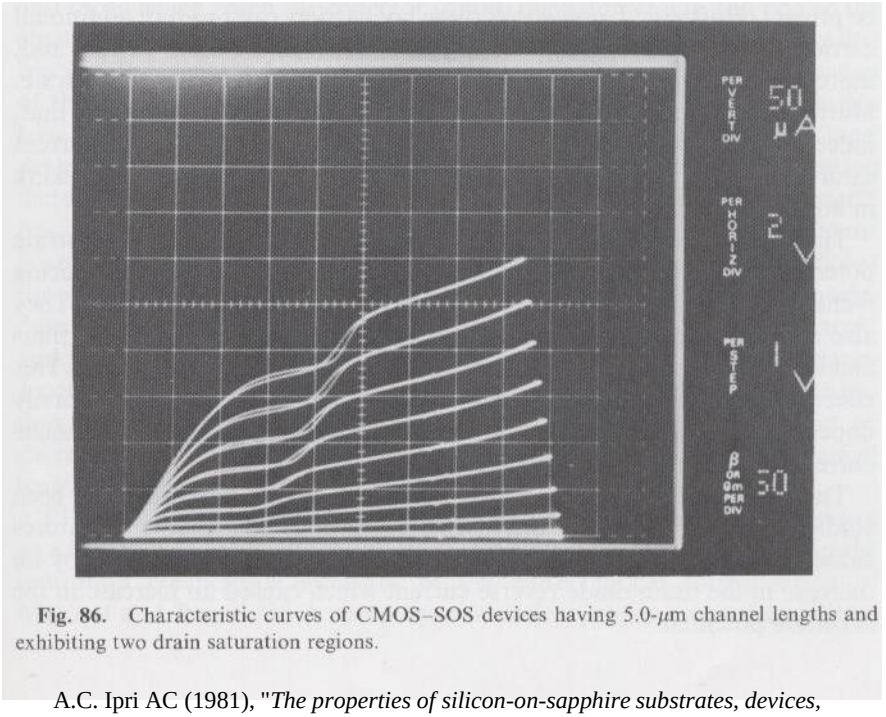


Fig. 86. Characteristic curves of CMOS–SOS devices having 5.0-μm channel lengths and exhibiting two drain saturation regions.

A.C. Ipri AC (1981), "*The properties of silicon-on-sapphire substrates, devices, and integrated circuits*", Applied Solid-State Sciences, Supplement 2, Silicon Integrated Circuits, Part A, Ed. by. D. Kahng, Academic Press, pp. 253-395, 1981

Good: - increased drain current

Bad: - poor output conductance, low Early voltage

- kink effect generates noise *

* Simoen E, Magnusson U, Rotondaro ALP. The kink-related excess low-frequency noise in silicon-on-insulator MOST's. *IEEE Transactions on Electron Devices, vol.41, no.3, March 1994, pp.330-9*

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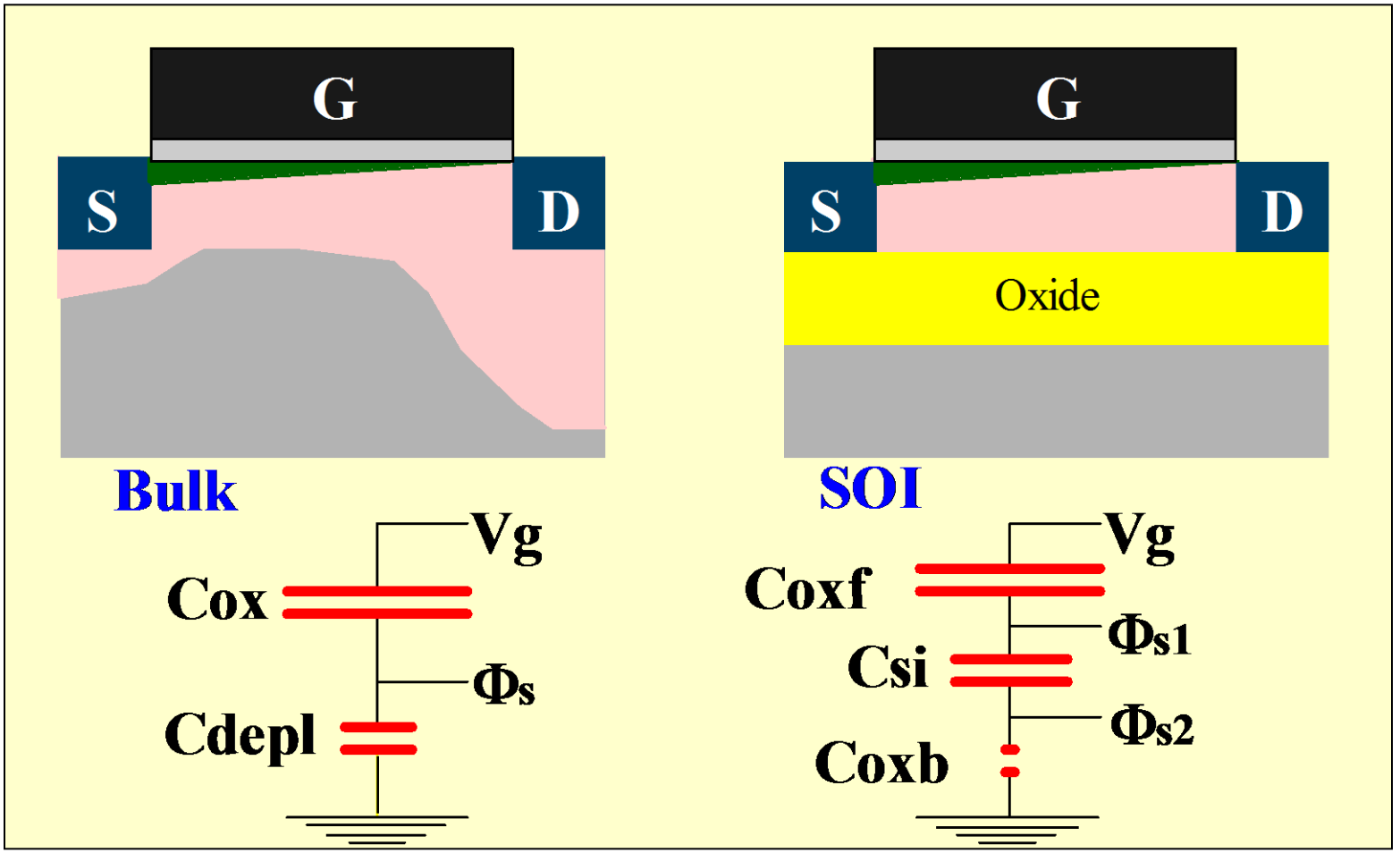
Gate-to-channel coupling; Body Effect



Body factor: n = …1.05… in an FDSOI MOSFET (*vs.* 1.5 in bulk)

Basic MOSFET equations

- Triode $$I_D = \mu C_{ox} \frac{W}{L}\left[(V_G - V_{TH})V_D - \frac{1}{2} n V_D^2\right]$$
- Saturation $$I_{Dsat} = \frac{1}{2n} \mu \ C_{ox} \frac{W}{L}(V_G - V_{TH})^2$$
- Subthreshold swing $$S = n \frac{kT}{q} \ln(10)$$
- Transconductance/current $$\frac{g_m}{I_D} = \sqrt{\frac{2\mu C_{ox} W/L}{n I_D}}$$

"A lower *n* value improves everything"

Gate-to-channel coupling; Body Effect

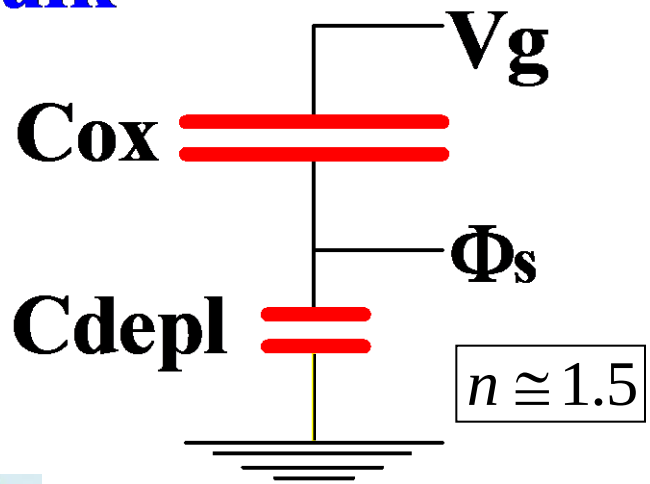
Bulk

$$n \equiv \frac{dV_G}{d\Phi_S} = \frac{C_{ox} + C_{depl}}{C_{ox}} = 1 + \frac{C_{depl}}{C_{ox}} = 1 + \frac{C_{channel\,to\,ground}}{C_{channel\,to\,gate}}$$

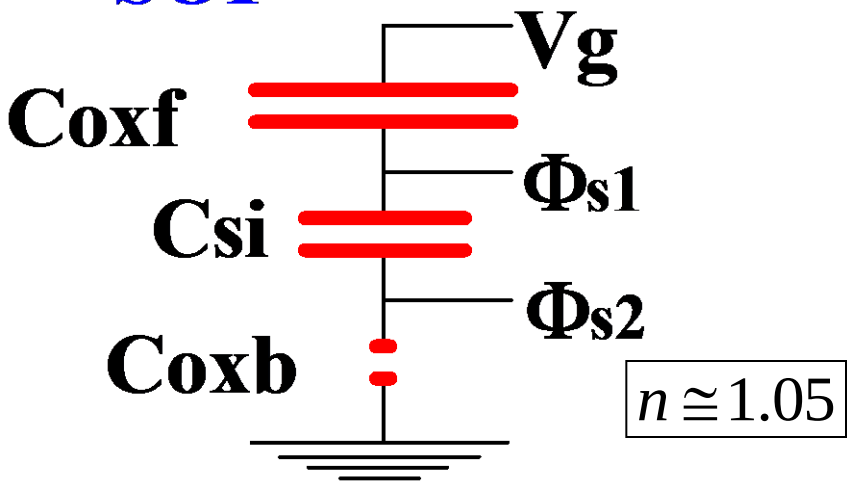
FDSOI

$$n \equiv \frac{dV_G}{d\Phi_S} = \frac{C_{ox} + C_{depl}}{C_{ox}} = 1 + \frac{C_{si}C_{ox2}}{C_{ox1}(C_{si} + C_{ox2})} = 1 + \frac{C_{channel\,to\,ground}}{C_{channel\,to\,gate}}$$

Bulk



SOI



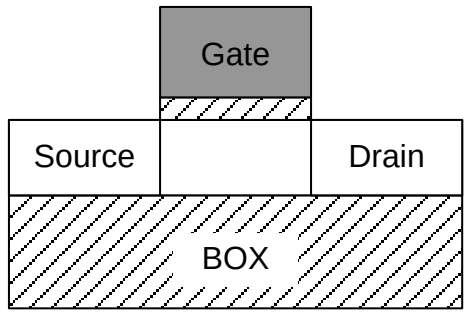
End of Roadmap Research

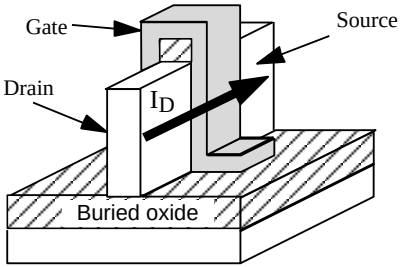
"1 Gate"

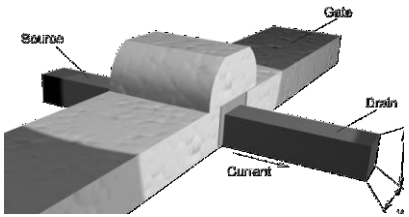
"2 Gates"

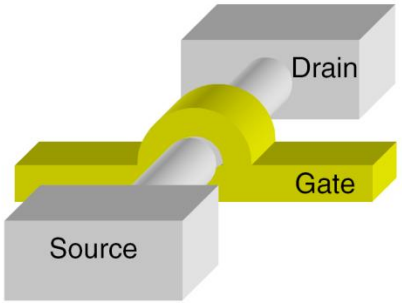
"3 Gates"

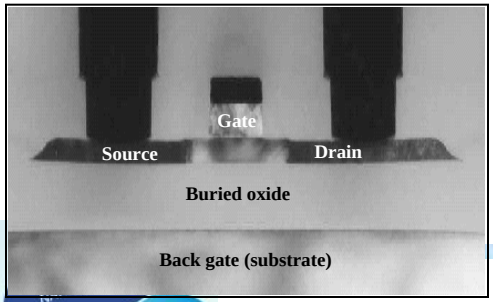
"Gate-all-Around"

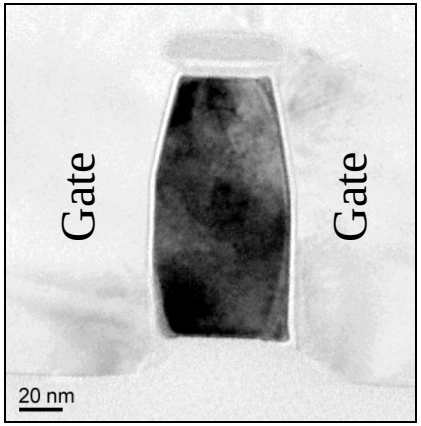


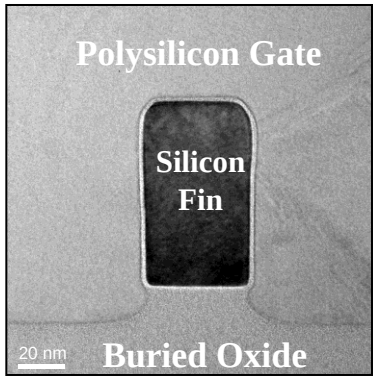


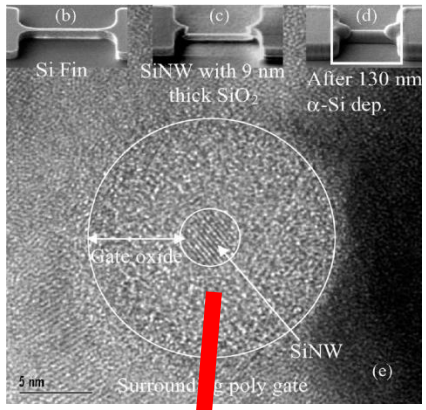


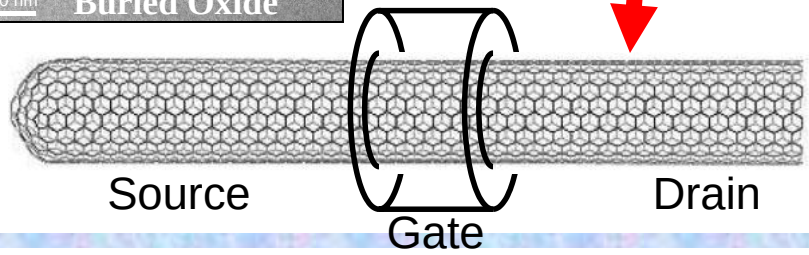




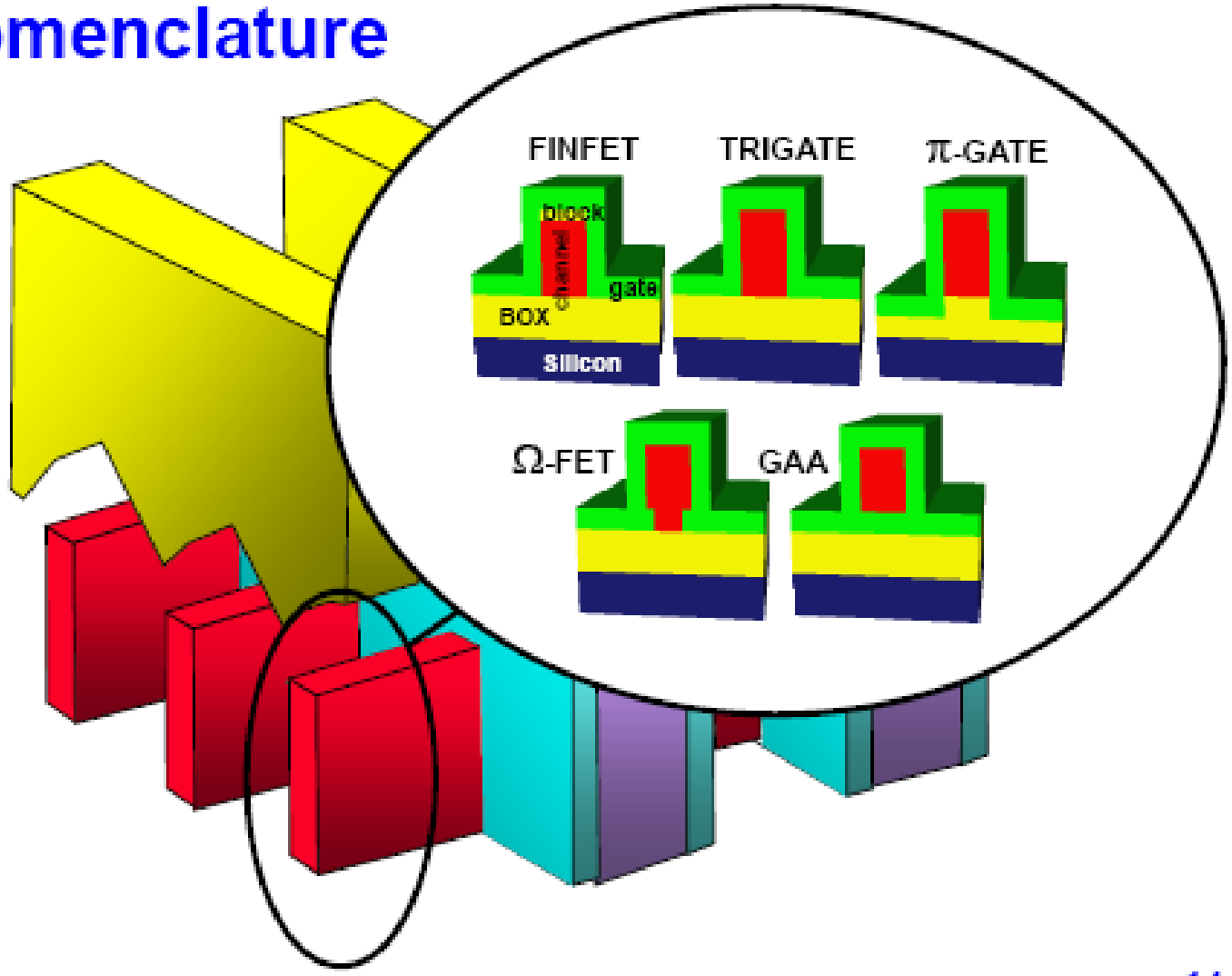








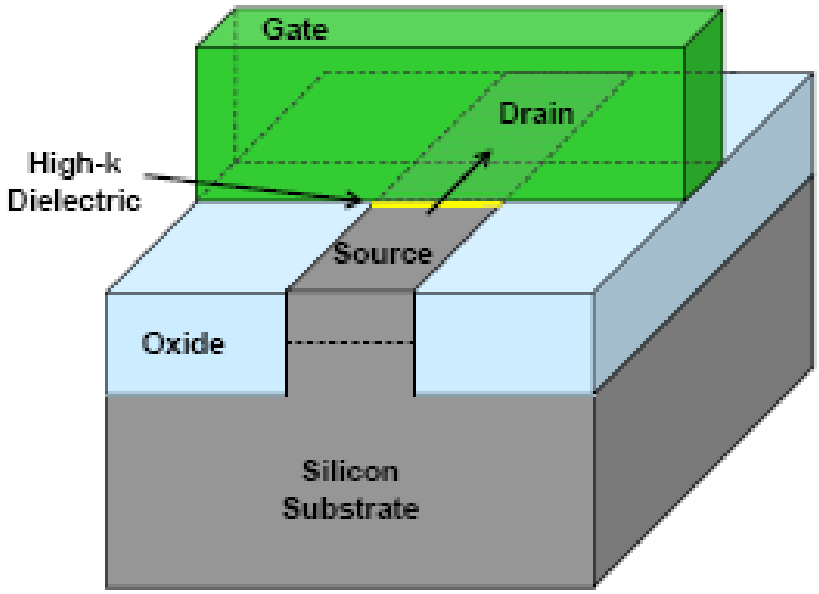
Nomenclature



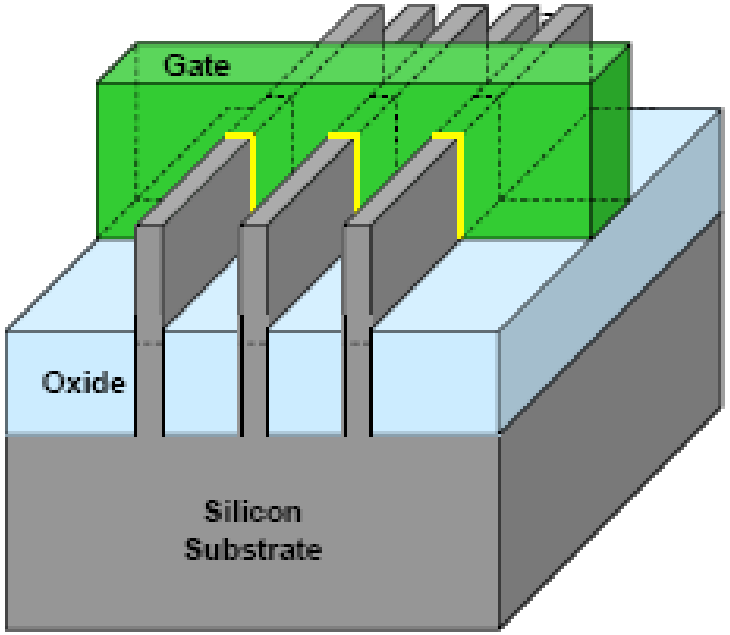
Kuhn: Tyndall 2011

14

Planar

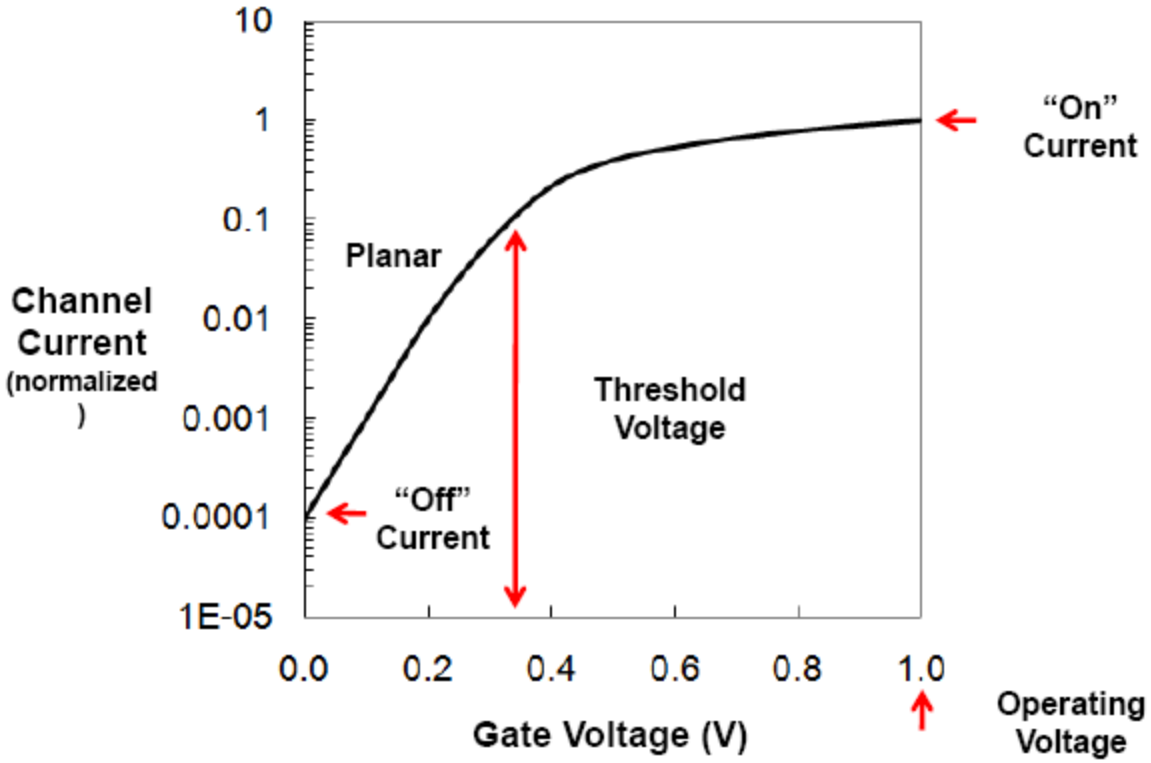

Gate
Drain
High-k
Dielectric
Source
Oxide
Silicon
Substrate

TriGate



Tri-Gate transistors can have multiple fins connected together to increase total drive strength

TriGate Electrostatics Benefits



Basic ID-VG

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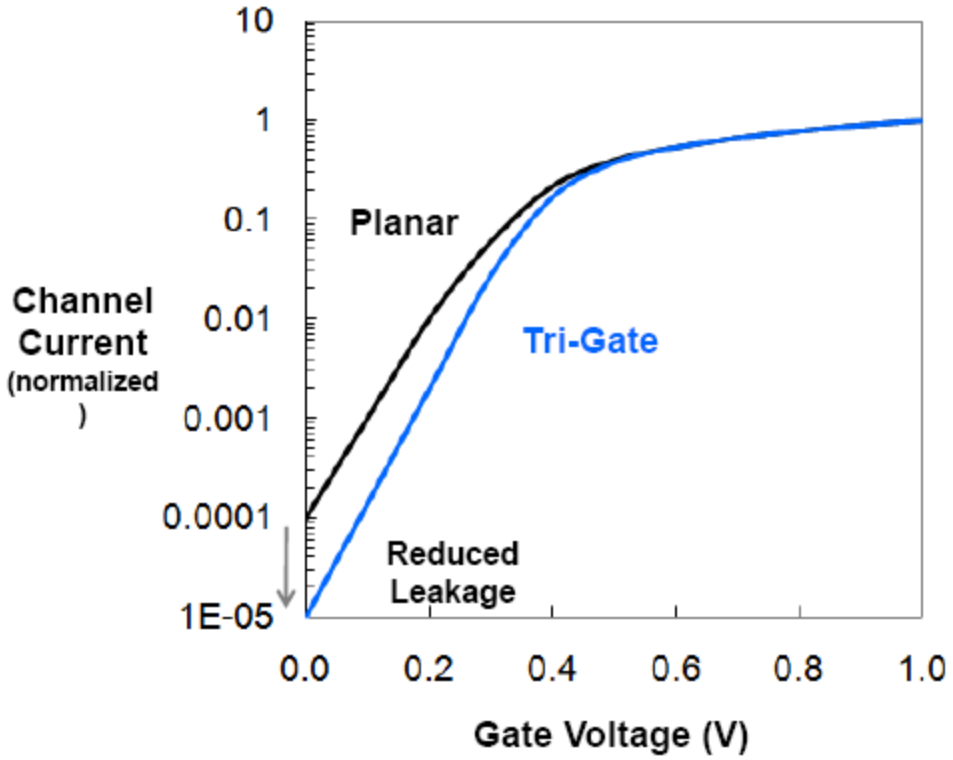

Good news:

Tri-gate short channel improvement → Ioff improvement

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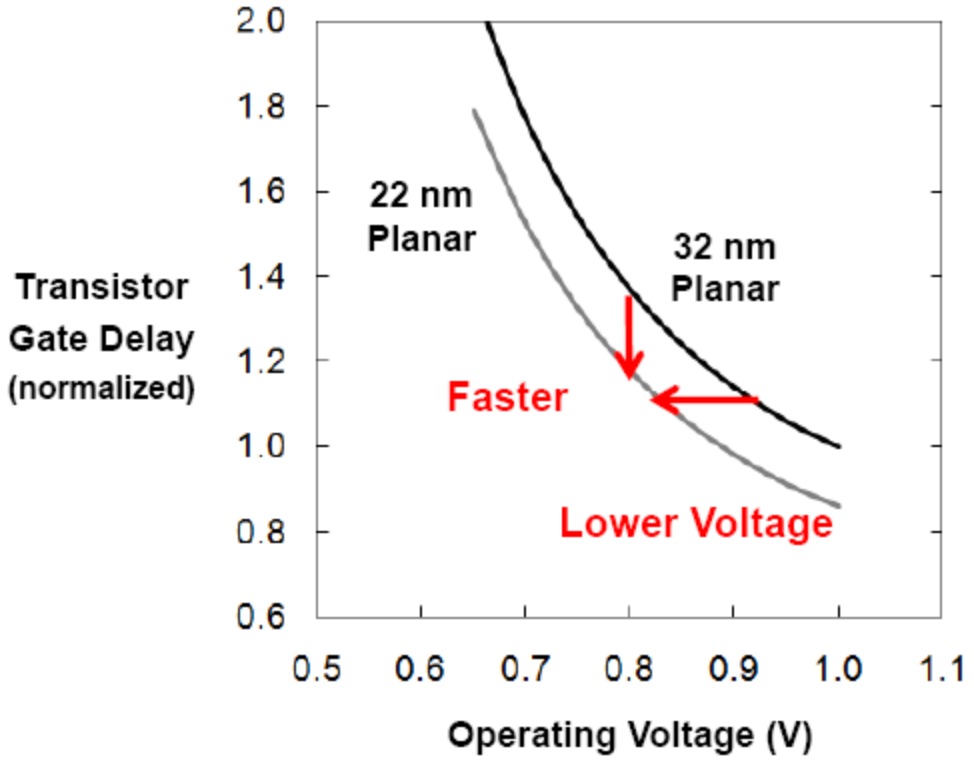
TriGate Electrostatics Benefits



22nm extension → similar ID-VG shape

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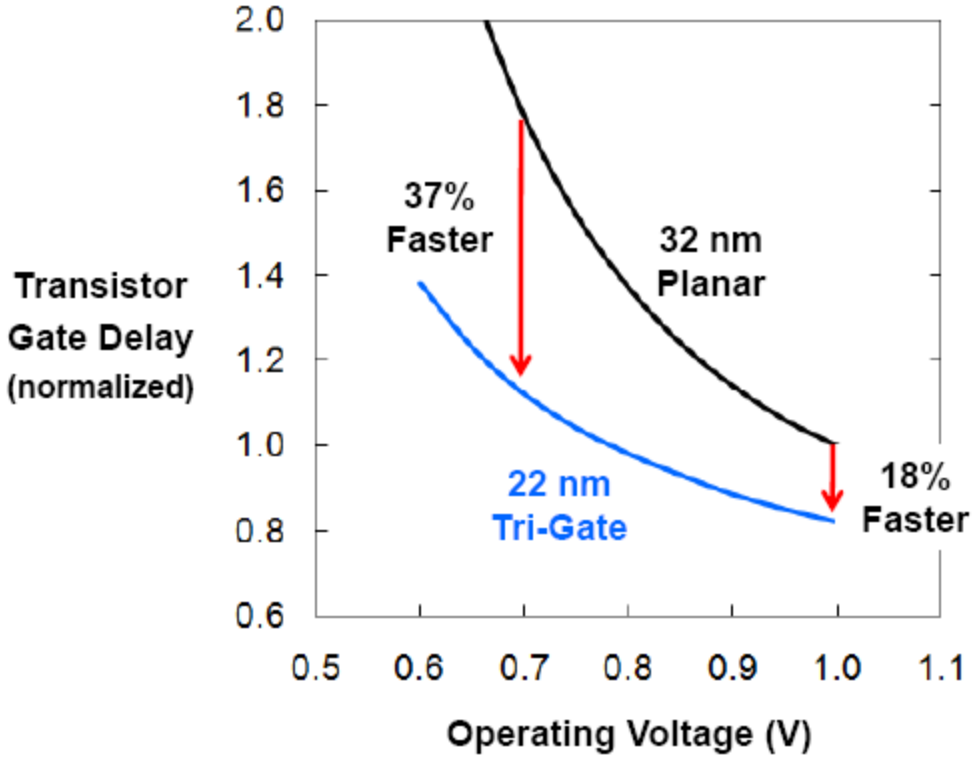
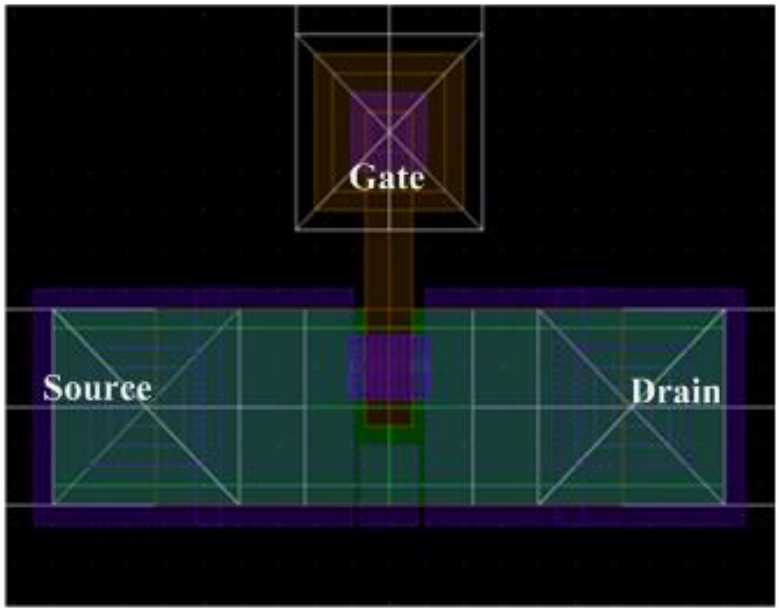
TriGate Electrostatics Benefits



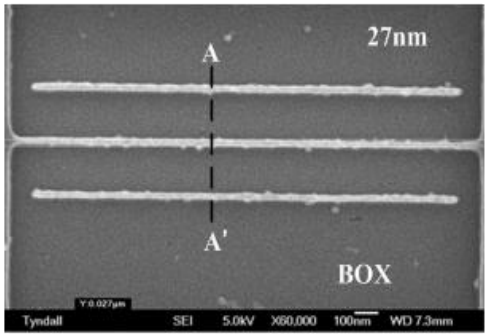
EXCELLENT news: Improved performance at high voltage and an *unprecedented* performance gain at low voltage

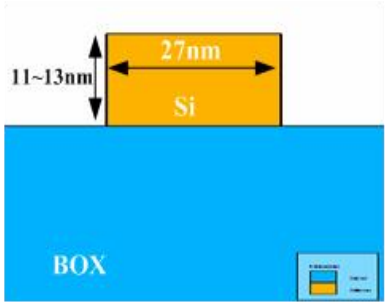
Kuhn: Tyndall 2011

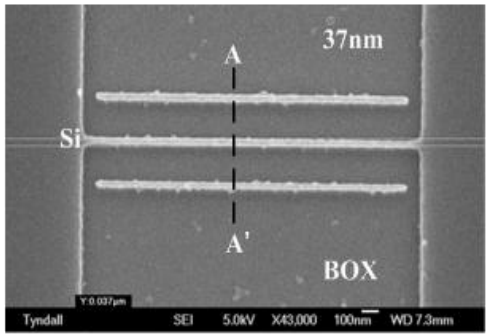
E-beam Lithography and Process

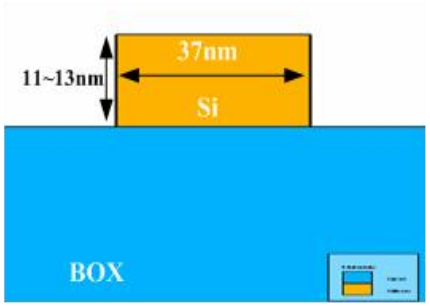


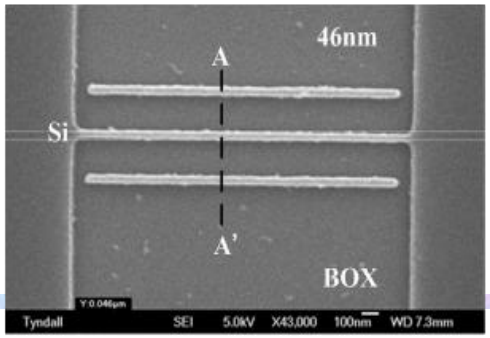
Lay out view of fabricated device

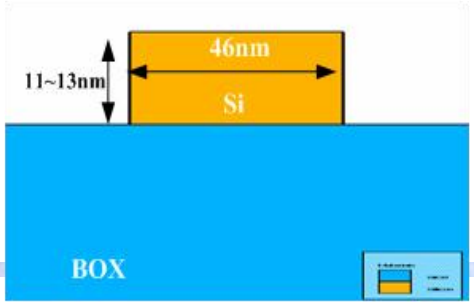




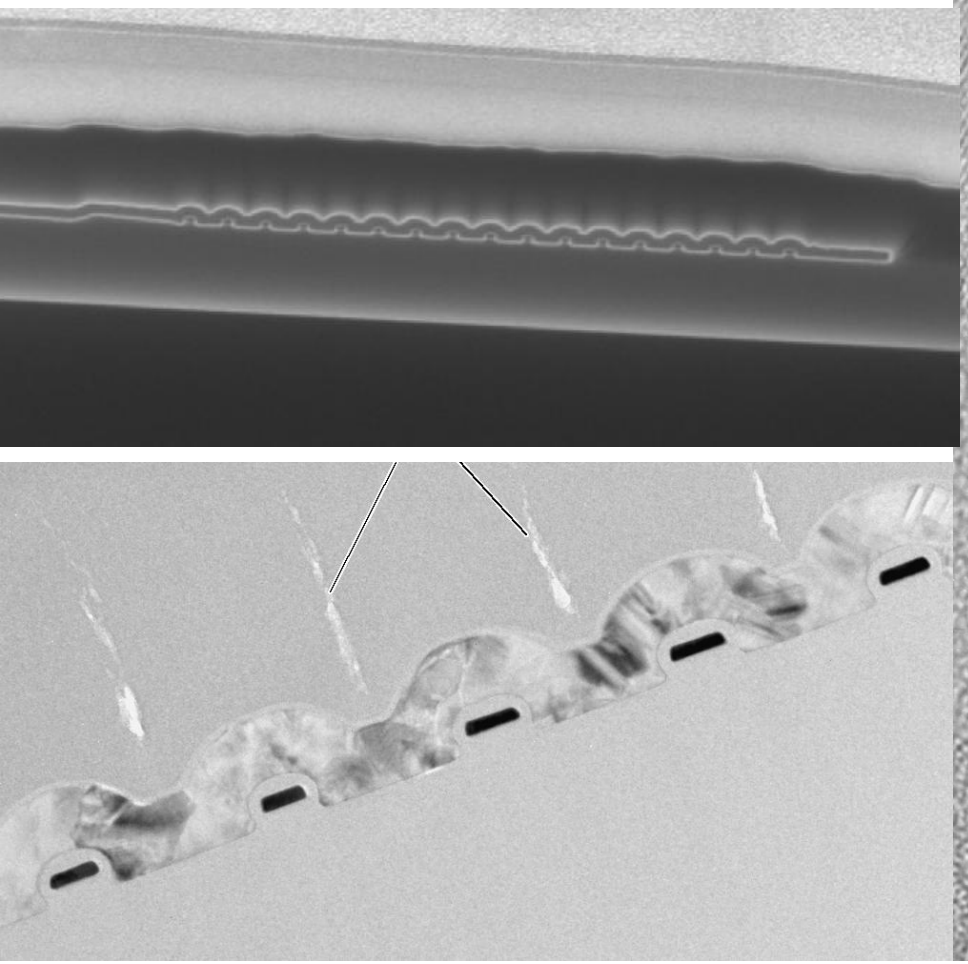


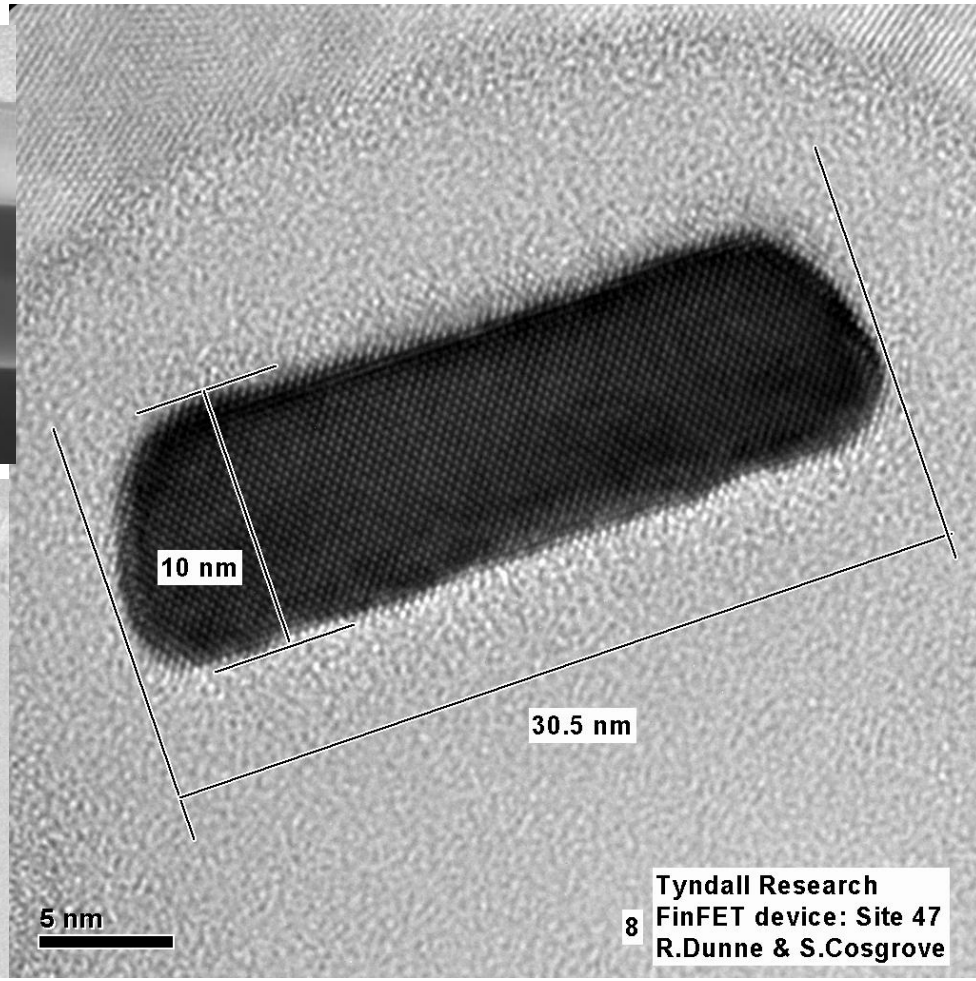






Fabricated Device: TEM

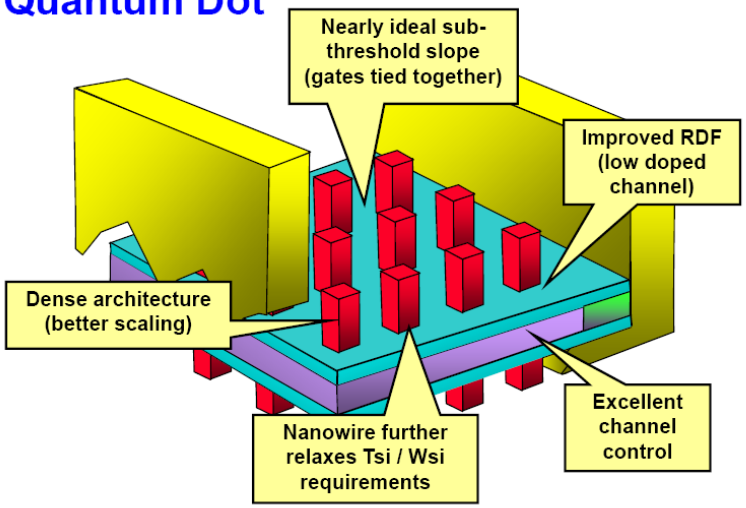




Future?

Nanowires and Quantum Dots

Nanowire / Quantum Dot

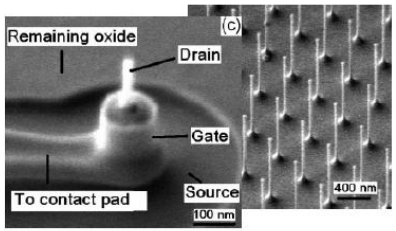


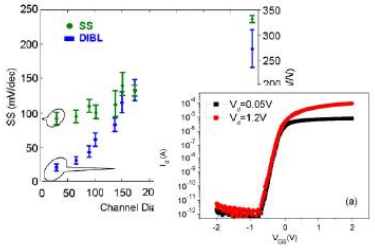
Kuhn: Tyndall 2011

Benefits

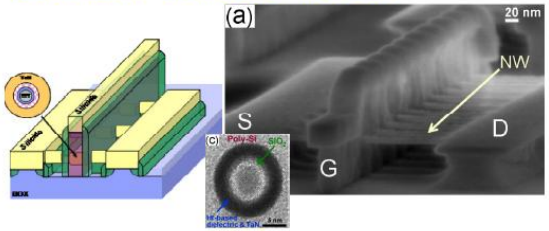
Nanowire FETs

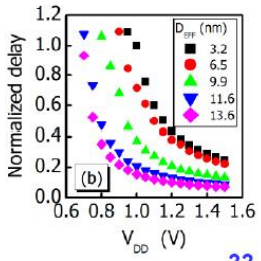
Yang – EDL 2008





Bangsaruntip - IEDM 2009 / VLSI 2010





Kuhn: Tyndall 2011

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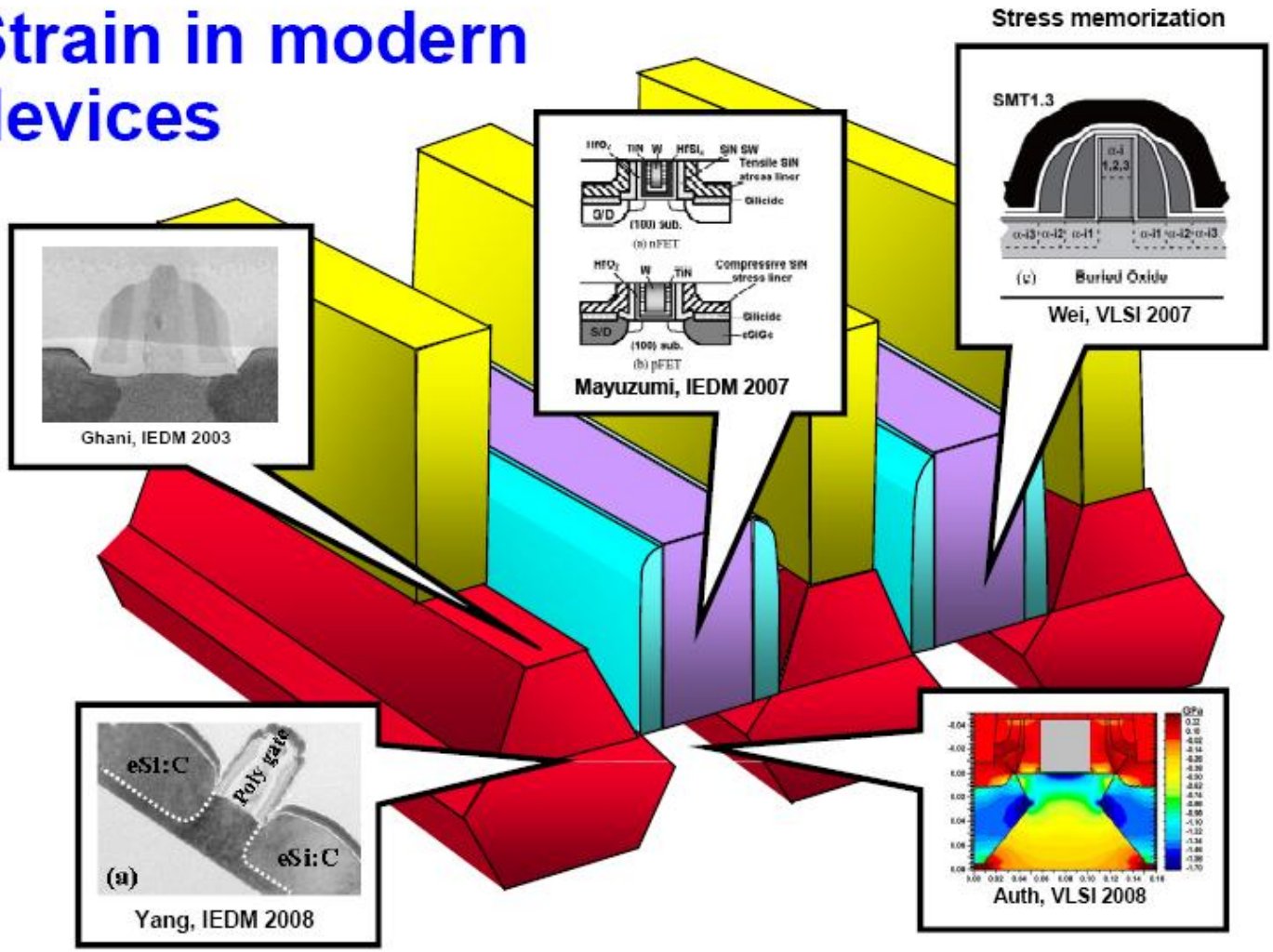
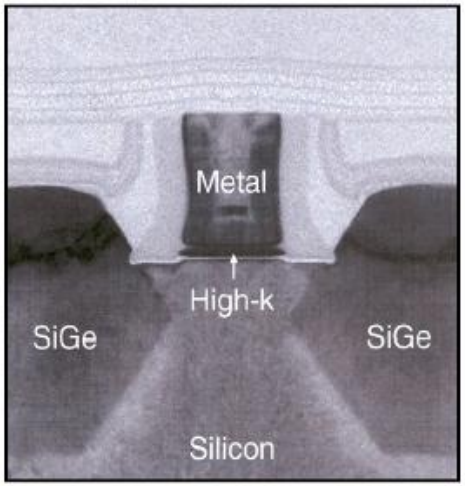
Stress and Strain



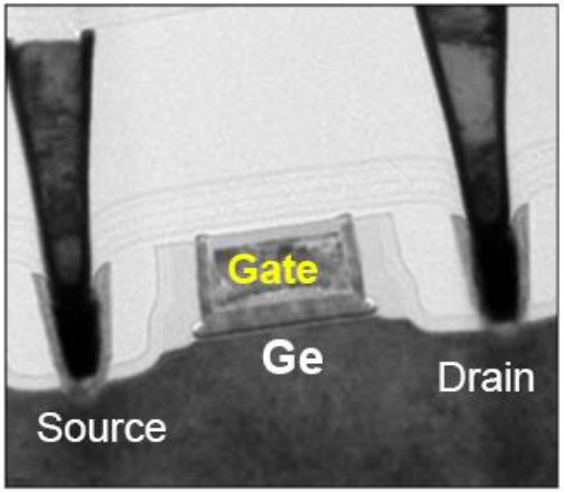
Kuhn: Tyndall 2011

New Materials

Si vs Ge MOSFETs



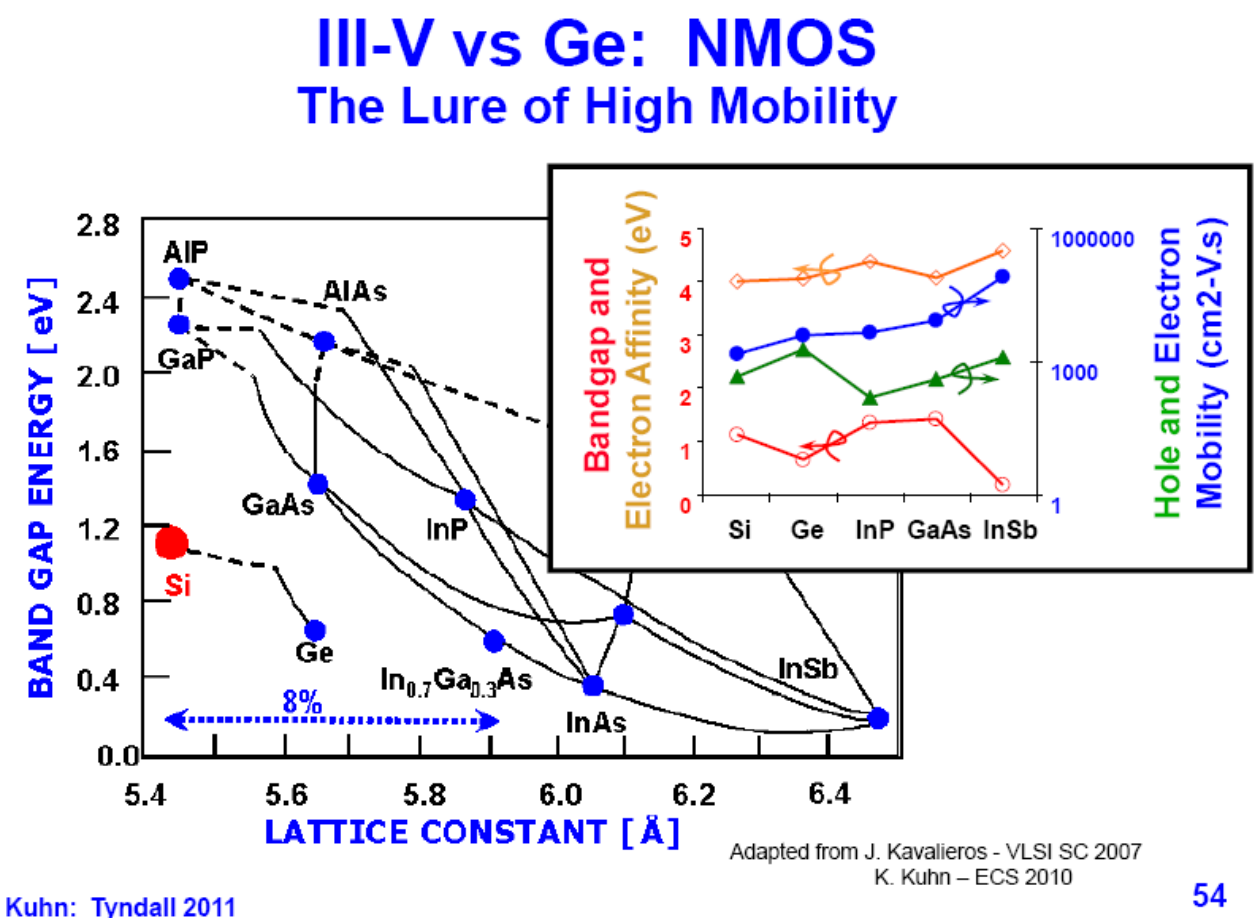
Intel 45nm HiK-MG Si device



Intel HiK-MG Ge device

The introduction of manufacturable HiK-MG transistors has led to the reconsideration of Ge channels

III-V materials



Limit to visibility remains ~ decade