OLLSCOIL NA hÉIREANN, CORCAIGH
THE NATIONAL UNIVERSITY OF IRELAND, CORK

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

SUMMER EXAMINATIONS, 2009

B. E. (ELECTRICAL AND ELECTRONIC)
M.ENG.SC. (MICROELECTRONICS)
VSEU (VISITING EUROPEAN)

RF IC Design
EE4011

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Answer *five* questions.

All questions carry equal marks.
The use of departmental approved non-programmable calculators is permitted.
The use of mathematical/statistical tables is permitted.
Smith Charts are appended to this paper. Detach and use as required. Write your examination number on any charts you use and return them with your examination script.

The following physical constants may be used if necessary:
Boltzmann's Constant: $k = 1.381 \times 10^{-23}$ J/K
Elementary Charge: $q = 1.602 \times 10^{-19}$ C
Vacuum Permittivity: $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m

Time allowed: *3 hours*

1. (a) Show a model of a GaAs MESFET suitable for small-signal analysis and derive expressions for the four y-parameters of the device, assuming that port 1 of the network is at the gate and port 2 is at the drain with the source connected to the common ground. You can neglect the gate-to-drain capacitance in your model.

[*10 marks*]

Question 1 is continued overleaf.

1. (b) The y-parameters of a GaAs MESFET in a common-source amplifier configuration have been measured at 1.5GHz with the following results:

$y_{11} = 0.0071 \angle 87.98°$
$y_{12} = 0$
$y_{21} = 0.1999 \angle -2.02°$
$y_{22} = 0.0173 \angle 15.79°$

From these measurements, determine the values of the elements of the small-signal equivalent circuit for the device at 1.5GHz and also the cut-off frequency of the device.

[*10 marks*]

2. (a) Show a suitable small-signal model for a bipolar transistor and from this derive an expression for the z-parameters of the device assuming that the base is at port 1 and the collector is at port 2 of the two-port network representation, with the emitter connected to the common ground. You need only include capacitance(s) associated with the base-emitter circuit.

[*10 marks*]

(b) Determine the z-parameters for a bipolar transistor configured as described in (a) at a frequency of 1GHz and at a temperature of 300K. The device bias conditions and parameters are as follows, where the symbols have their usual meanings:

$V_{BE} = 0.8V$, $V_{CE} = 3.0V$, $I_S = 1x10^{-15}A$, $V_A = 10V$, $\beta = 100$, $C_{JE} = 0.3pF$, $M_{JE} = 0.5$, $V_{JE} = 1.0V$ and $\tau_F = 0.1ns$.

(Note: if you use the thermal voltage, V_T , in your formulas, be sure to calculate this at the correct temperature.)

[*10 marks*]

3. (a) For an RF amplifier circuit give definitions for (i) the operating power gain, (ii) the transducer power gain and (iii) the available power gain.

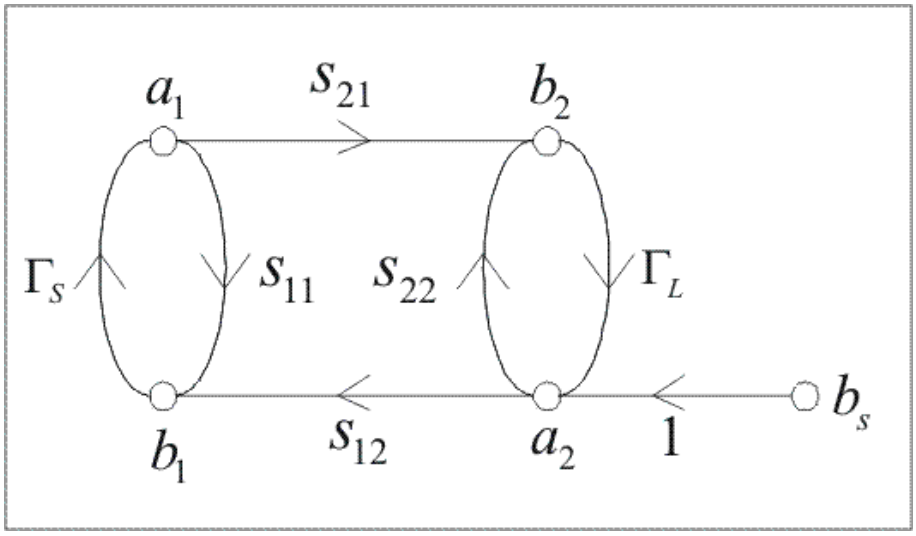
[*3 marks*]

(b) State the conditions that are necessary to achieve maximum unilateral transducer gain from a single transistor amplifier and illustrate how this is usually achieved.

[*3 marks*]

(c) Determine an expression for the output reflection coefficient of a single-transistor amplifier by considering the signal-flow diagram shown below where the symbols have their usual meanings:

[*12 marks*]



(d) A high-frequency transistor has the following characteristics (at 1 GHz with 50Ω reference):

$s_{11} = 0.863 \angle -79.1°$
$s_{12} = 0.072 \angle 36.5°$
$s_{21} = 3.434 \angle 106.2°$
$s_{22} = 0.627 \angle -58.3°$

If this device is used as a single-transistor amplifier at 1 GHz determine the output reflection coefficient of the amplifier if the source reflection coefficient is $0.1 \angle 0°$.

[*2 marks*]

4. (a) A BJT has the following S-parameters and noise parameters (with Z_0=50Ω) at 1GHz:

$$s_{11} = 0.707\angle -155° \quad s_{12} = 0 \quad s_{21} = 5.00\angle 180° \quad s_{22} = 0.51\angle -20°$$

$$F_{\min} = 3\,dB \quad \Gamma_{opt} = 0.45\angle 180° \quad R_N = 4\,\Omega$$

(i) Determine the maximum unilateral transducer gain (in *dB*) for this device.

[*2 marks*]

(ii) On a Smith-Chart, draw the 3.1 *dB* noise circle associated with this device.

[*3 marks*]

Note: The following equations specify the noise circles where the symbols have their usual meanings:

$$N_i = \frac{F_i - F_{\min}}{4R_N / Z_0}\left|1+\Gamma_{opt}\right|^2 \quad C_{Fi} = \frac{\Gamma_{opt}}{N_i+1} \quad R_{Fi} = \frac{\sqrt{N_i\left(N_i+1-\left|\Gamma_{opt}\right|^2\right)}}{\left(N_i+1\right)}$$

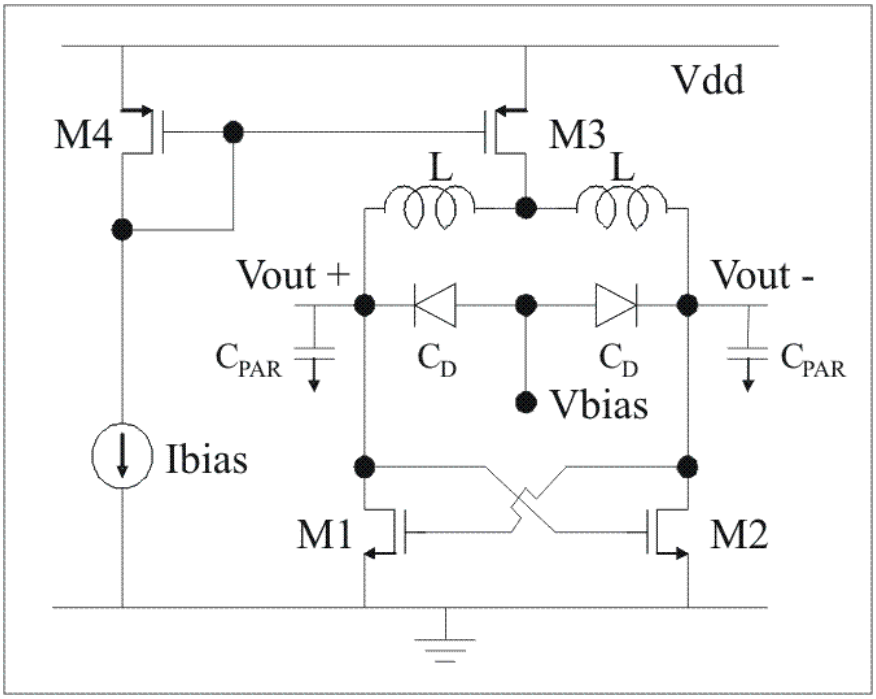
(b) Using Smith-Chart procedures, determine the largest unilateral transducer gain which can be achieved (to the nearest 0.1 *dB*) if the BJT in part (a) is used for a low-noise amplifier at 1GHz, without exceeding a noise figure of 3.1 *dB*, and determine values for the 2-element input and output matching networks needed to achieve this gain (in a 50Ω system).

[*15 marks*]

Note: The following equations specify the source gain circles where the symbols have their usual meanings:

$$\left|C_S\right| = \frac{g_s\left|s_{11}\right|}{1-\left|s_{11}\right|^2\left(1-g_s\right)} \qquad R_S = \frac{\sqrt{1-g_s}\left(1-\left|s_{11}\right|^2\right)}{1-\left|s_{11}\right|^2\left(1-g_s\right)}$$

5. (a) The schematic below shows a typical MOSFET LC Voltage Controlled Oscillator (VCO):



By using a suitable small-signal analysis, derive the equivalent input resistance (r_{in}) of the cross-coupled MOSFET pair above and outline how the cross-coupled MOSFETs are used to sustain oscillation in the circuit.

[*10 marks*]

(b) If the inductors in the circuit of part (a) have a parasitic resistance of 5Ω and a bias current (Ibias) of 5mA is used, determine the width (W) of the MOSFETs M1 and M2 which is required to sustain oscillation assuming both M1 and M2 have the same widths and a length of L=0.25μm (assume all MOSFETs are in saturation).

The following MOSFET parameters should be used for your calculations:

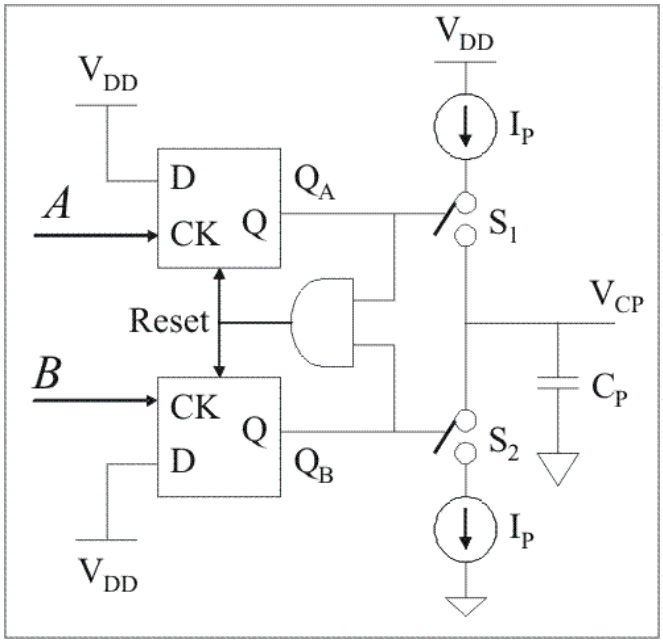
T_{OX}=5nm, μ=400cm^2/Vs, ε_r = 3.9 (dielectric constant of SiO_2).

[*5 marks*]

(c) The VCO in part (a) uses inductors (L) with a value of 4nH and has a parasitic capacitance (C_{PAR}) of 1pF at each of the output nodes (assume this value includes the parasitic MOSFET drain and gate capacitances as well). The diodes have parameters M_J = 0.5, V_J = 0.8V and C_{J0} = 1.5pF. If the average DC level of the Vout lines is 1.5V, determine the oscillation frequency of the circuit when Vbias = 0V.

[*5 marks*]

6. (a) The following topology is frequently used to implement a combined phase-frequency detector/charge-pump (PFD/CP) in Type II phase-locked loops (PLLs):



Illustrate the operation of this circuit using clear timing diagrams for the case where logic waveforms of the same frequency are applied to lines A and B, but where A leads B by a phase angle $\Delta\phi$, assuming that the voltage V_{CP} begins at 0V. Using you diagram as a starting point, derive an expression for the s-domain transfer function of this circuit.

[*5 marks*]

(b) Show the overall block diagram for a full Type II PLL based on the PFD/CP in part (a), with an integer divider and also include any extra component which you think is necessary to improve the stability of the system. Derive an expression for the closed-loop transfer function of the full system.

[6 *marks*]

(c) A Type II PLL has the following parameters:

$$I_P=2mA,\ C_P=100pF,\ R_P=10k\Omega,\ K_{VCO}=100MHz/V,\ M=1000$$

(i) Determine the natural frequency of oscillation of the closed-loop system.

[2 *marks*]

(ii) Determine the damping factor of the closed-loop system.

[2 *marks*]

(d) Illustrate a PLL based on a dual-modulus divider and describe the operation of the dual-modulus divider if the output frequency from the PLL is specified to be 10.1 times the input frequency.

[5 *marks*]

7. (a) Illustrate a detailed block-level architecture for a single-chip CMOS GPS receiver and outline the functions of the main blocks in the receiver including the typical frequencies encountered by each block.

[*10 marks*]

(b) Answer EITHER section (i) OR section (ii) below:

EITHER:

(i) For the GPS receiver in part (a), select one block from the overall architecture and discuss the design of this block in detail. In your discussion, show a more detailed schematic diagram of the block you choose (if necessary) and outline the typical design trade-offs that must be made when designing this block, as well as the typical performance characteristics that can be achieved with a single-chip CMOS approach.

[*10 marks*]

OR:

(ii) Discuss the operation of the GPS system including the frequencies, power levels and the modulation and coding schemes used. Show how the characteristics of the GPS system lead to the specifications for receiver systems such as the single-chip solution discussed in part (a).

[*10 marks*]

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Smith Charts are appended to the paper after this page.