UE4002 Autumn 2005

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an nmos in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.
In each question, capacitances other than those mentioned may be ignored.

Question 1

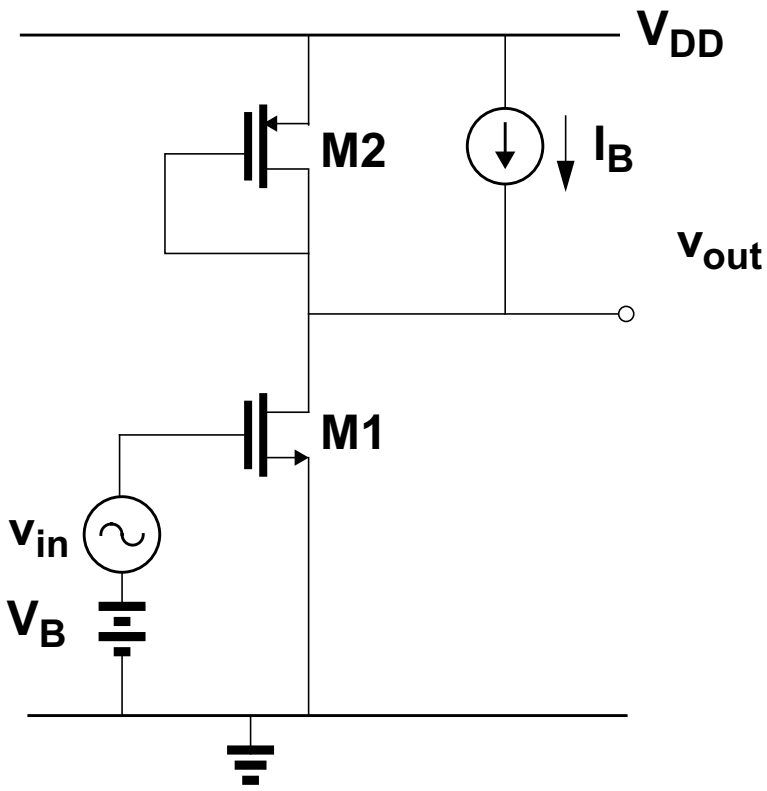


Figure 1

For the questions below you may assume $g_{m1},g_{m2}>>g_{ds1},g_{ds2}$ and that all devices are biased in saturation.

(i) Figure 1 shows a gain stage with a diode-connected load. An additional DC bias current is injected from V_{DD} into the output node. Draw the small-signal model for this circuit.
(ii) Derive an expression for the small signal voltage gain (v_{out}/v_{in}).
(iii) Calculate the small-signal voltage gain (v_{out}/v_{in}) in dB if V_B=1V,$|V_{GS2}|$=1.75V, $V_{tn}=|V_{tp}|$=0.75V, I_{D1}=200μA, I_B= 150μA.
(iv) Calculate the small-signal voltage gain in dB if the additional bias current I_B is reduced to zero. Assume V_B is unchanged.

Question 2

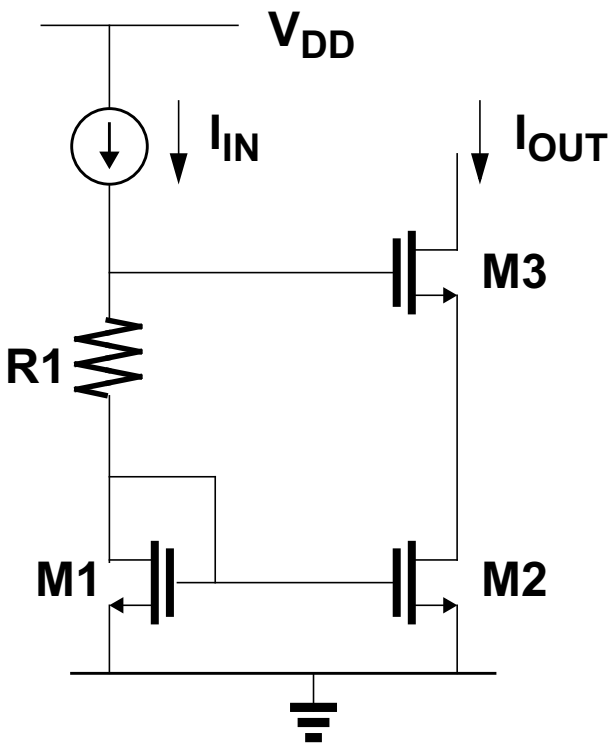


Figure 2

Figure 2 shows a cascoded current mirror.
Assume $K_n'=200\mu A/V^2$, $V_{tn}=800mV$.
All transistors have W/L=12.5/2.

(i) If $I_{IN}=I_{OUT}=100\mu A$, what is the minimum voltage at the output node, i.e. the drain of M3, such that all transistors are biased in saturation?
What minimum value of R1 is required to ensure M2 is in saturation?

(ii) What value of R1, and W/L of M2 would be required to increase the output current to 400μA and still ensure all transistors are in saturation?

(iii) It is required to measure the small-signal output resistance of the current mirror (i.e. the small-signal resistance looking into the drain of M3). Draw a small signal model showing how this can be done.

(iv) Derive an expression for the small-signal output resistance. Reduce this to its simplest form assuming $g_{m1}, g_{m2}, g_{m3} >> g_{ds1}, g_{ds2}, g_{ds3}$.

Question 3

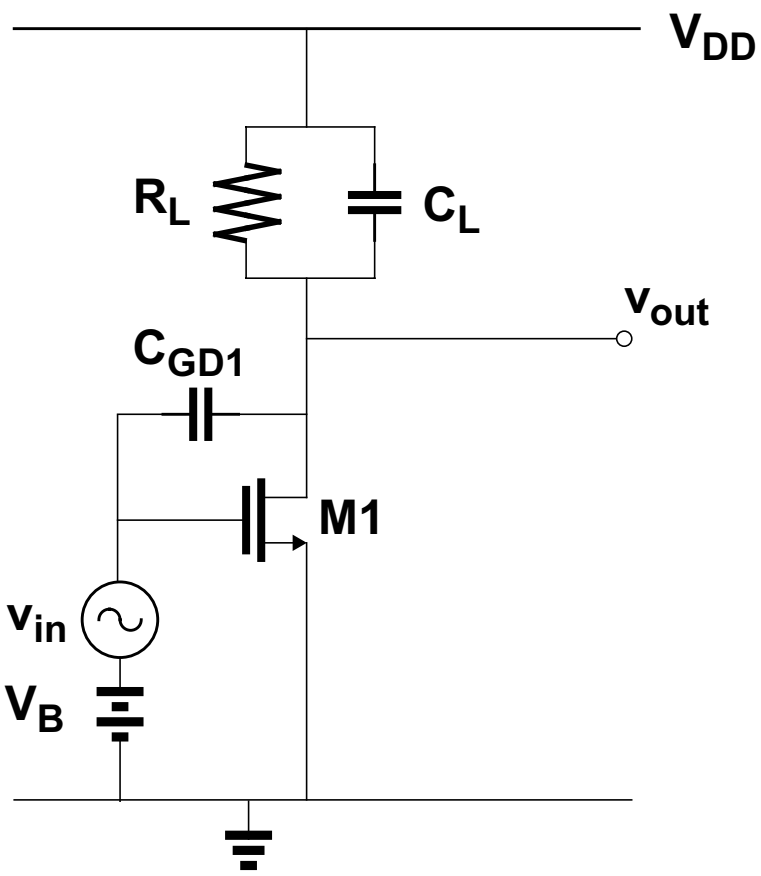


Figure 3

For the questions below you may assume $g_{m1} >> g_{ds1}$, $g_{ds1} << 1/R_L$ and that M1 is biased in saturation.

(i) Figure 3 shows a gain stage with an RC load. Draw the small-signal model for this circuit.
(ii) Ignoring all capacitances except C_{GD1} and C_L, derive an expression for the high-frequency transfer function.
(iii) Calculate the low-frequency gain (v_{out}/v_{in}) and the pole and zero frequencies if V_B=1V,V_{GS2}=1.75V, V_{tn}=0.75V, I_{D1}=250μA, C_{GD1}=0.1pF, C_L=4.9pF,R_L=10kΩ.
(iv) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the pole and zero frequencies.

Question 4

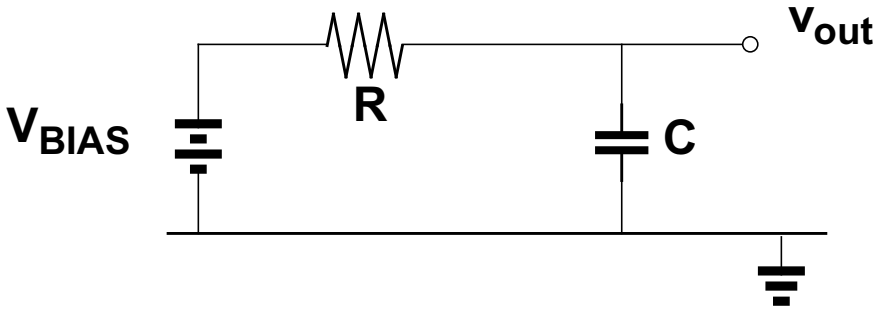


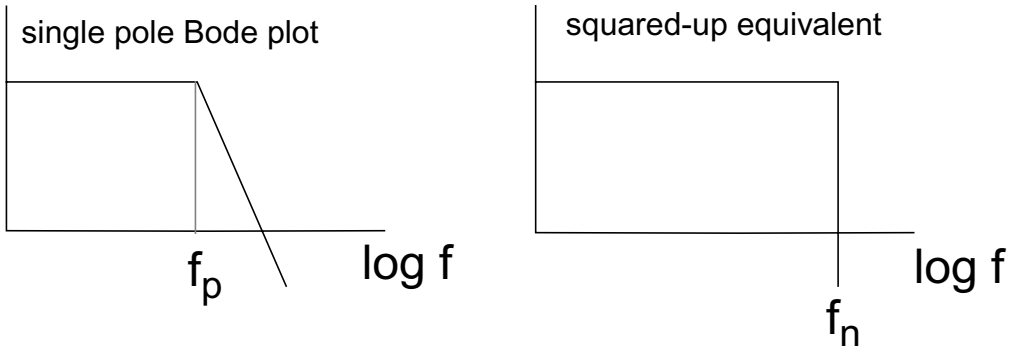
Figure 4

For numerical calculations take Boltzmann's constant k=1.38X10^{-23}J/^{o}K, temperature T=300^{o}K.

(i) Show that the total integrated thermal noise voltage at node v_{out} in Figure 4 is

$$v_{nout}^2 = \frac{kT}{C}$$

where k is Boltzmann's constant, and T is the temperature.
You may assume the following:



For the area underneath the curves to be the same then $f_n=(\pi/2)*f_p$

(ii) If R= 1kΩ and C=1pF calculate the total thermal noise in V_{rms} at node v_{out} in Figure 4?

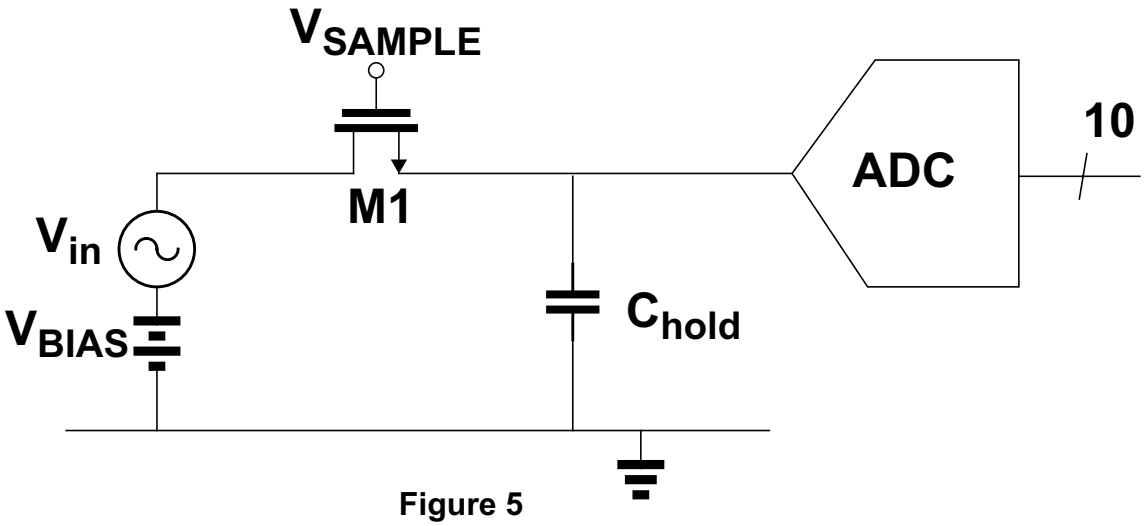


Figure 5

(iii) Figure 5 shows a sampling circuit preceding a 10-bit A/D converter. The sampling switch M1 is turned on.If the A/D converter has an input range of 1Vrms, and the noise budget for the sampling circuit is 0.1 LSB, what is the minimum value required for C_{hold}?

(iv) If a 12-bit A/D converter is used with the same input range, and the noise budget for the sampling circuit is kept at 0.1LSB, what is the new minimum value required for C_{hold}?