Solutions UE4002 Summer 2007

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an NMOS in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.
In each question, capacitances other than those mentioned may be ignored.Question 1

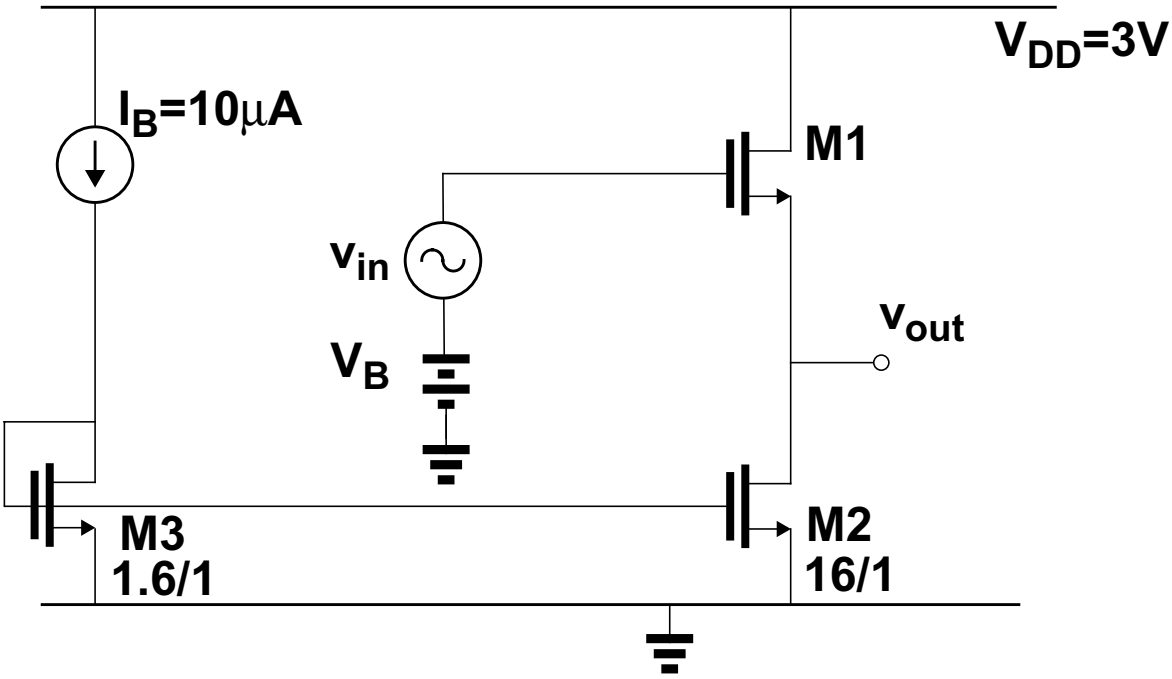
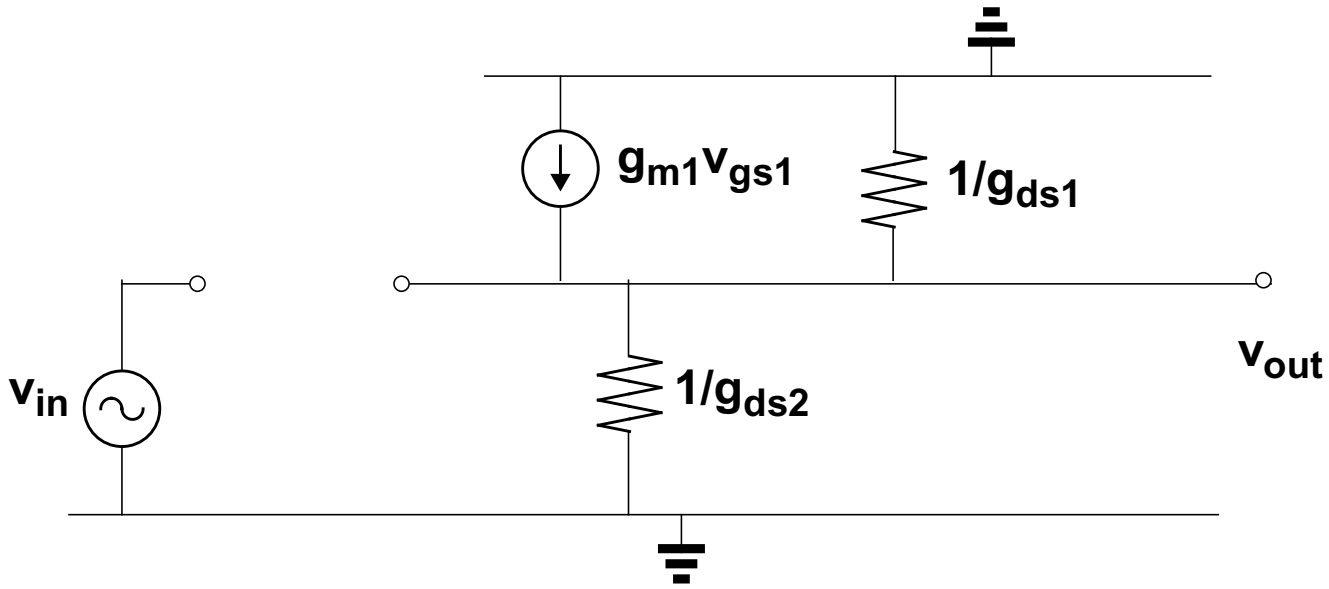


Figure 1

Figure 1 shows an NMOS source follower.
Biasing and transistor dimensions are as shown in Figure 3. Take K_n'=200μA/V^2, V_{tn}=750mV.
Assume all transistors are in saturation.

(i) Draw the small-signal equivalent circuit for the source follower stage shown in Figure 1.
(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}).
(iii) The source follower is to be used as a DC level-shifter, where the DC voltage at the source of M1 is 1V lower than at the gate of M1.
What value of W/L is required for M1 to achieve this?
(iv) What are the minimum and maximum values of V_B for which the levelshifter works as required?

(i) Draw the small-signal equivalent circuit for the source follower stage shown in Figure 1.



(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in})

$$v_{gs1} = v_{in} - v_{out}$$

KCL at output node

$$g_{m1}(v_{in} - v_{out}) - (v_{out}g_{ds1}) - (v_{out}g_{ds2}) = 0$$

$$g_{m1}v_{in} = (g_{m1} + g_{ds1} + g_{ds2})v_{out}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1} + g_{ds2}}$$

(iii) The source follower is to be used as a DC level-shifter, where the DC voltage at the source of M1 is 1V lower than at the gate of M1.
What value of W/L is required for M1 to achieve this?

Require V_{GS} M1 = 1V.

Current mirror ratio 1:10 => I_{D1}=100µA

$$\frac{W_1}{L_1} = \frac{2I_{D1}}{K_n'(V_{GS1} - V_{tn})} = \frac{2 \cdot 100\mu A}{200\mu A/V^2(1-0.75)^2} = \frac{16}{1}$$

(iv) What are the minimum and maximum values of V_B for which the levelshifter works as required?

Lower limit given by requirement than M2 stay in saturation

$$V_{B1} > V_{GS1} + (V_{GS2} - V_{tn})$$

$$V_{GS2} - V_{tn} = \sqrt{\frac{2I_{D2}}{K_n' \frac{W_2}{L_2}}} = \sqrt{\frac{2 \cdot 100\mu A}{200\mu A/V^2 \frac{16}{1}}} = 0.25V$$

$$V_{B1} > 1V + 0.25V = 1.25V$$

Upper limit given by requirement that M1 stay in saturation

$$V_{DD} - V_{S1} > V_{GS1} - V_{tn}$$

$$V_{DD} - (V_{B1} - V_{GS1}) > V_{GS1} - V_{tn}$$

$$V_{B1} < V_{DD} + V_{tn}$$

$$V_{B1} < 3 + 0.75$$

$$3.75V > V_{B1} > 1.25V$$

Question 2

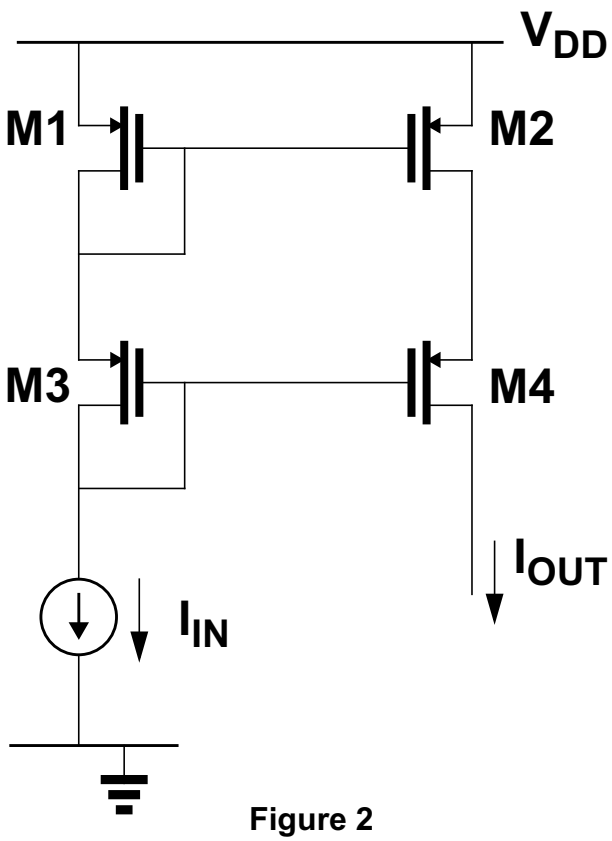


Figure 2

Figure 2 shows a cascoded current mirror.

Assume $I_{IN}=I_{OUT}=100\mu A$, $V_{DD}=3V$, $K_p'=50\mu A/V^2$, $V_{tp}=-750mV$.

All transistors have W/L=64/1.

(i) It is required to measure the small-signal output resistance of the current mirror (i.e. the small-signal resistance looking into the drain of M4). Draw a small-signal model showing how this can be done.

(ii) Derive an expression for the small-signal output resistance.
Reduce this to its simplest form assuming $g_{m1}, g_{m2}, g_{m3}, g_{m4} >> g_{ds1}, g_{ds2}, g_{ds3}, g_{ds4}$.

(iii) What is the maximum voltage at the output node, i.e. the drain of M4, such that all transistors are biased in saturation?

(iv) It is desired to increase the mirroring ratio by increasing the width of M2 only. What is the largest value of output current I_{OUT} such that M2 remains in saturation?

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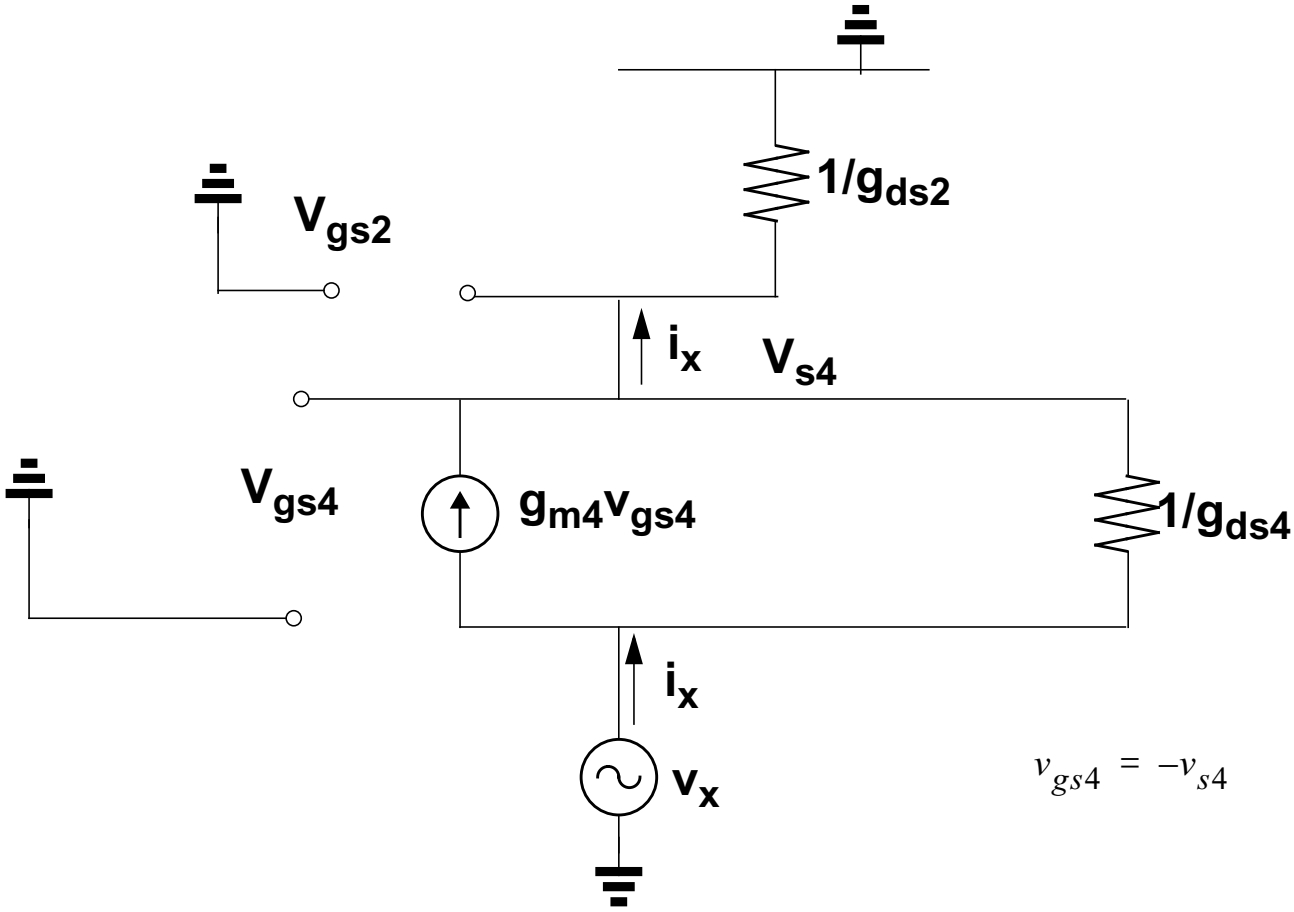
(i) It is required to measure the small-signal output resistance of the current mirror (i.e. the small-signal resistance looking into the drain of M4). Draw a small signal model showing how this can be done.

Can consider the gates of M1, M3 to be grounded in the small-signal sense.
Apply test voltage at output, measure current



(ii) Derive an expression for the small-signal output resistance.

$$i_x = g_{m4}v_{gs4} + (v_x - v_{s4})g_{ds4}$$

$$i_x = -g_{m4}v_{s4} + v_x g_{ds4} - v_{s4}g_{ds4}$$

Since $v_{s4} = \dfrac{i_x}{g_{ds2}}$

$$i_x = -g_{m4}\frac{i_x}{g_{ds2}} + v_x g_{ds4} - \frac{i_x}{g_{ds2}}g_{ds4}$$

$$r_{out} = \frac{v_x}{i_x} = \frac{1}{g_{ds4}}\left(1 + \frac{g_{m4}}{g_{ds2}} + \frac{g_{ds4}}{g_{ds2}}\right) \approx \frac{1}{g_{ds2}}\left(\frac{g_{m4}}{g_{ds4}}\right)$$

(iii) What is the maximum voltage at the output node, i.e. the drain of M4, such that all transistors are biased in saturation?

The maximum voltage at the output is given by the voltage at the drain of M2 plus the required V_{DS} across M4 for it to be in saturation i.e. V_{GS4}-V_t

For all transistors

$$\left|\left|V_{GS}\right| - \left|V_t\right|\right| = \sqrt{\frac{2I_D}{K_n' \frac{W}{L}}} = \sqrt{\frac{2 \cdot 100\mu A}{50\mu A/V^2 \frac{64}{1}}} = 250mV \Rightarrow \left|V_{GS}\right| = 1V$$

$$V_{OUTmax} = V_{DD} - \left|V_{GS1}\right| - \left|V_{GS3}\right| + \left|V_{GS4}\right| - \left|V_{GS4} - V_t\right|$$

$$V_{OUTmax} = 3V - 1V - 1V + 1V - 0.25V = 1.75V$$

(iv) It is desired to increase the mirroring ratio by increasing the width of M2 only. What is the largest value of output current such that M2 remains in saturation?

If the current of M2 is increased by increasing the width of M2 only, then its V_{GS}-Vt will remain the same.
However V_{GS4} will increase, increasing V_{D4}, until M2 goes out of saturation
This determines V_{GS4max} which determines the max. current.

$$V_{S4max} = V_{D2max} = V_{DD} - (\left|V_{GS2}\right| - \left|V_{tp}\right|) = 3 - 0.25V = 2.75V$$

$$V_{G4} = V_{DD} - \left|V_{GS1}\right| - \left|V_{GS3}\right| = 3V - 1V - 1V = 1V$$

$$\left|V_{GS4max}\right| = V_{S4max} - V_{G4} = 2.75V - 1V = 1.75V$$

$$I_{D4max} = \frac{K_p'}{2}\frac{W}{L}(\left|V_{GS4}\right| - \left|V_t\right|)^2 = \frac{50\mu A/V^2}{2}\frac{64}{1}(1.75 - 0.75)^2 = 1.6mA$$

Question 3

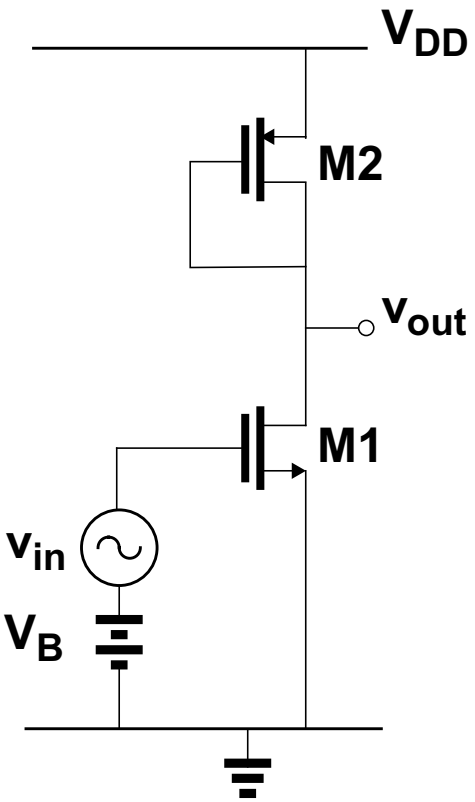


Figure 3a

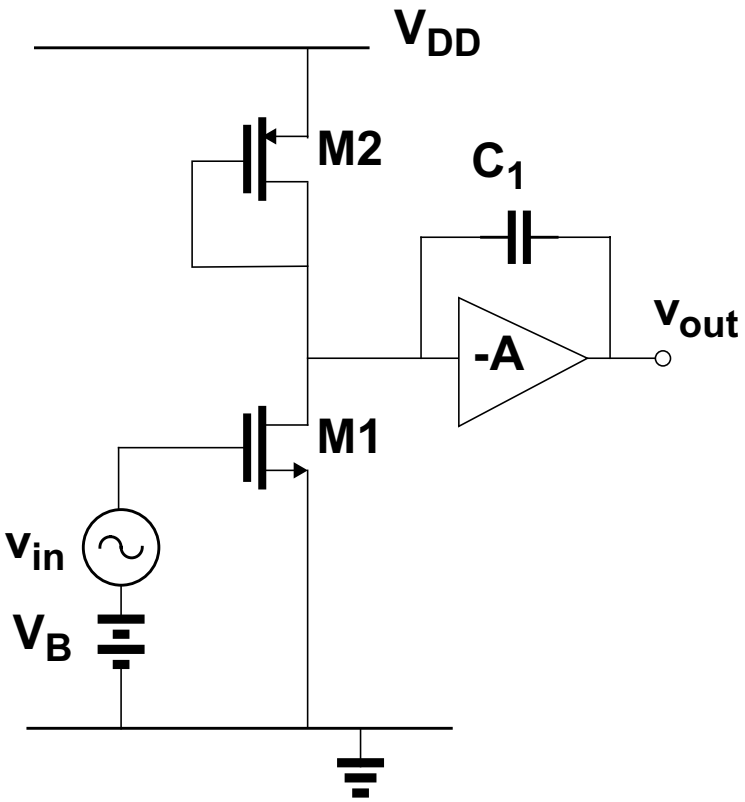


Figure 3b

For the questions below you may assume $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$ and that all devices are biased in saturation.

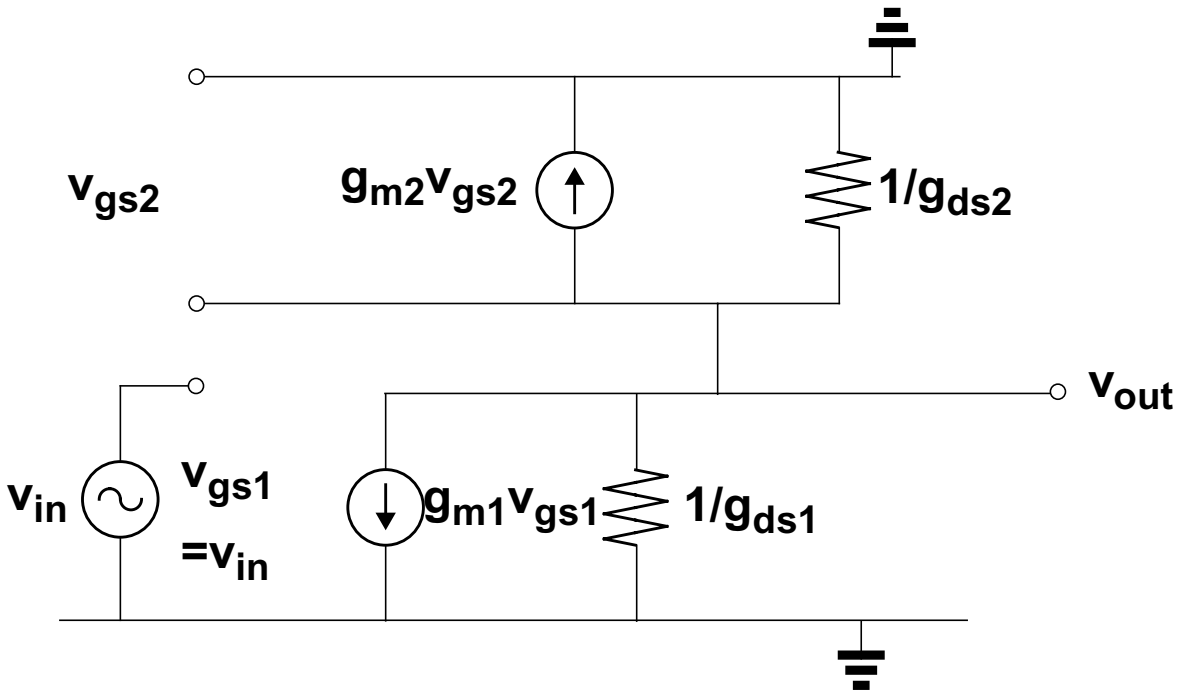
(i) Figure 3a shows a gain stage with a diode-connected load.
Draw the small-signal model for this circuit.
Give an expression for the small-signal voltage gain (v_{out}/v_{in}).

(ii) In Figure 3b the amplifier of Figure 3a is cascaded with an ideal amplifier with a small-signal gain of -A.
Give an expression for the small-signal low-frequency voltage gain (v_{out}/v_{in}) of this circuit.
Give also an expression for the frequency of the dominant pole of the circuit shown in Figure 3b.

(iii) Calculate the small-signal low-frequency voltage gain (v_{out}/v_{in}) in dB, and the dominant pole frequency of the circuit shown in Figure 3b if
V_B=1V,$|V_{GS2}|$=1.75V, $V_{tn}=|V_{tp}|$=0.75V, I_{D1}=200μA, A=-50, C_1=100pF

(iv) Assuming the circuit shown in Figure 3b is first-order, give an expression for its unity gain frequency.
What is the effect on the unity gain frequency if V_B is increased to 1.25V, assuming M1 remains in saturation?

(i) Figure 3a shows a gain stage with a diode-connected load.
Draw the small-signal model for this circuit.
Derive an expression for the small-signal voltage gain (v_{out}/v_{in}).



May write the small-signal voltage gain directly or derive as follows
Current at output node

$$g_{m1}v_{gs1} + g_{m2}v_{gs2} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$g_{m1}v_{in} + g_{m2}v_{out} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \cong -\frac{g_{m1}}{g_{m2}}$$

Alternatively recognise that the current of the current-source $g_{m2}v_{gs2}$ is determined by voltage across its terminals i.e. is equivalent to a resistance $1/g_{m2}$.
Since $1/g_{m2} << 1/g_{ds2}$, $1/g_{m2} << 1/g_{ds1}$, can write directly

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2}}$$

(ii) In Figure 3b the amplifier of Figure 3a is cascaded with an ideal amplifier with a small-signal gain of -A. Write an expression for the small-signal low-frequency voltage gain (v_{out}/v_{in}) of this circuit. Write also an expression for the frequency of the pole of the circuit shown in Figure 3b.

Gain is the product of the gain of the gain stage in Figure3a and the gain of the ideal amplifier

$$Gain = -\frac{g_{m1}}{g_{m2}} \cdot -A = A\frac{g_{m1}}{g_{m2}}$$

Pole frequency given by conductance at the output of the gain stage divided by the capacitance seen at this node.
The conductance is given by

$$g_{m2} + g_{ds1} + g_{ds2} \approx g_{m2}$$

The capacitance seen at this node is (from the Miller approximation)

$$(1 + A)C_1$$

Pole frequency given by

$$|\omega_p| = \frac{g_{m2}}{(1 + A)C_1}$$

(iii) Calculate the small-signal voltage gain (v_{out}/v_{in}) in dB, and the pole frequency if V_B=1V,$|V_{GS2}|$=1.75V, $V_{tn}=|V_{tp}|$=0.75V, I_{D1}=200µA, A=-50, C_1=100pF

$$g_{m1} = \frac{2I_{D1}}{(V_{GS1} - V_{tn})} = \frac{2 \times 200\mu A}{1 - 0.75} = 1600\mu A/V$$

$$g_{m2} = \frac{2|I_{D2}|}{(|V_{GS2}| - |V_{tp}|)} = \frac{2 \times 200\mu A}{1.75 - 0.75} = 400\mu A/V$$

Low-frequency gain given by

$$\frac{v_{out}}{v_{in}} \cong A\frac{g_{m1}}{g_{m2}} = 50\frac{1600\mu A/V}{400\mu A/V} = 200 = 46dB$$

Pole frequency given by

$$|\omega_p| = \frac{g_{m2}}{(1 + A)C_1} = \frac{400\mu A/V}{(1 + 50)100pF} = 78krad/s \approx 80krad/s$$

(iv) Assuming the circuit shown in Figure 3b is first-order, give an expression for its unity gain fequency. What is the effect on the unity gain frequency if V_B is increased to 1.25V, assuming M1 remains in saturation?

Unity gain frequency is the product of the low-frequency gain and the pole frequency

$$|\omega_u| = A\frac{g_{m1}}{g_{m2}} \cdot \frac{g_{m2}}{(1 + A)C_1} \approx \frac{g_{m1}}{C_1}$$

If V_B is increased to 1.25V then V_{GS}-V_t doubled => I_{D1} quadrupled

$$g_{m1} = \sqrt{2K_n'\frac{W}{L}I_{D1}}$$

=> g_{m1} doubled => w_u approximately doubled

Question 4

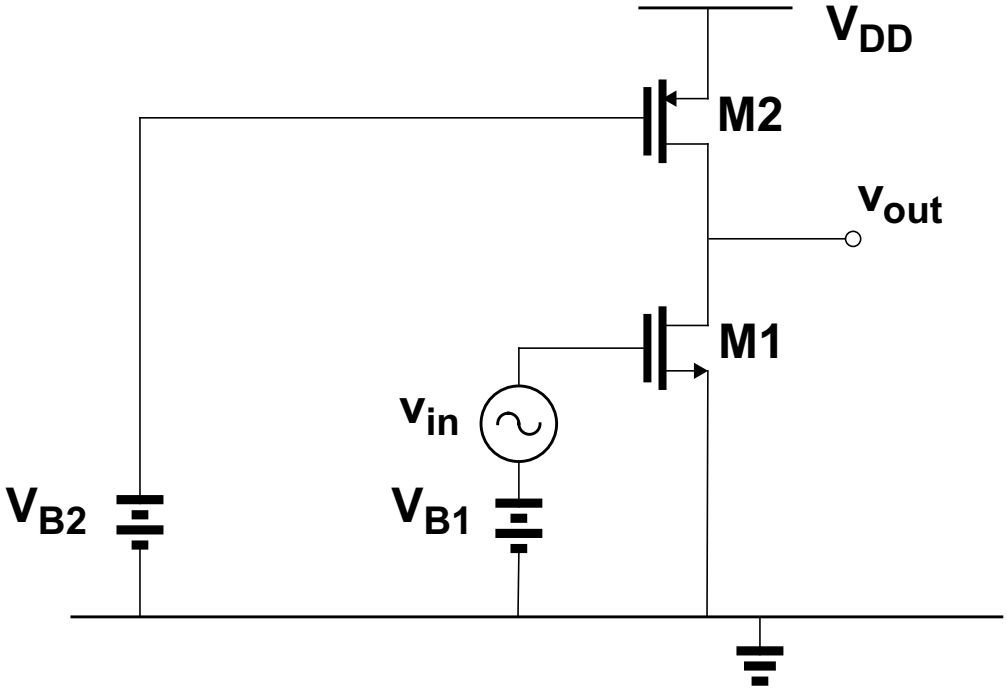


Figure 4

Assume M1 and M2 are operating in saturation. Only thermal noise sources need be considered.

For calculations take Boltzmann's constant $k=1.38X10^{-23}J/^oK$, temperature $T=300^oK$.

(i) Draw the small-signal model for the circuit shown in Figure 4.
What is the low-frequency small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters of M1 and M2?

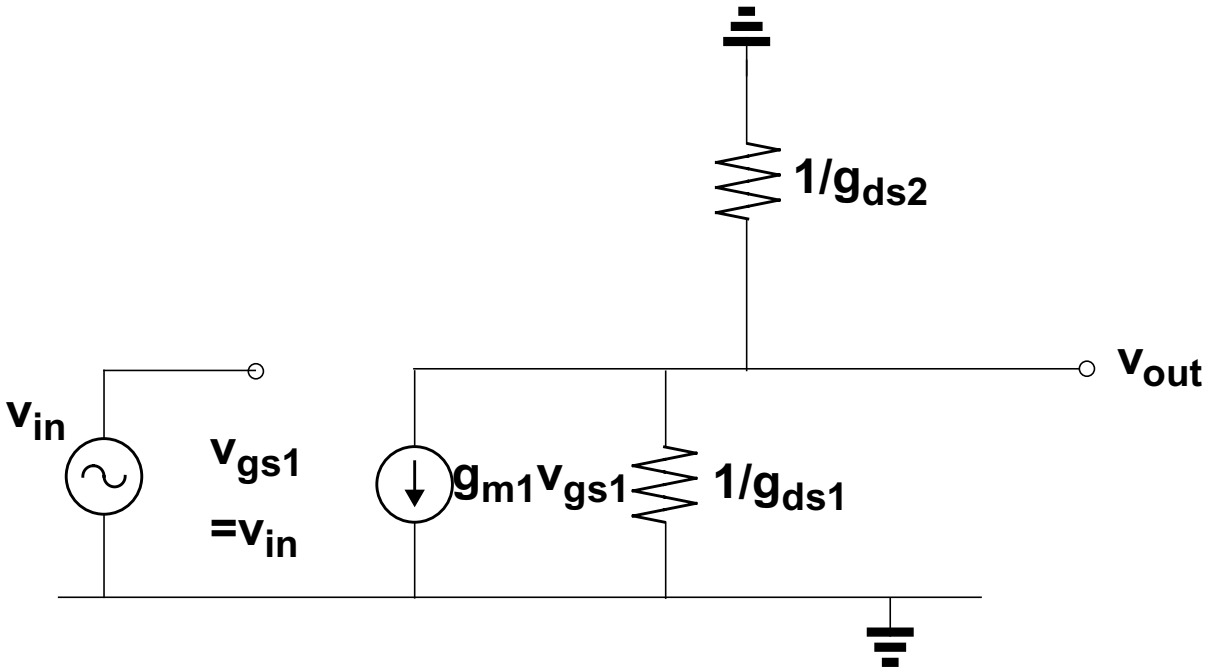
(ii) What is the input-referred thermal noise voltage density of M1?
What is the input-referred thermal noise voltage density of M2?
Answers should be in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T.

(iii) Calculate the input-referred thermal noise voltage density of M1 and the input-referred thermal noise voltage density of M2 if
$V_{B1}=1.0V$, $V_{B2}=1.25V$, $V_{DD}=3V$, $V_{tn} = 0.75V$, $V_{tp} = -0.75V$, $\lambda_n=\lambda_p=0.04V^{-1}$.
The drain current of M1 is 100μA.
Which is the dominant noise source?

(iv) Calculate the total noise voltage at the output over a bandwidth of 1MHz.
If the input signal v_{in} is a $1mV_{rms}$ sine wave, calculate the signal-to-noise ratio in dB at the output over a bandwidth of 1MHz.

Solution

(i) Draw the small-signal model for the circuit shown in Figure 4.
What is the low-frequency small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters of M1 and M2?

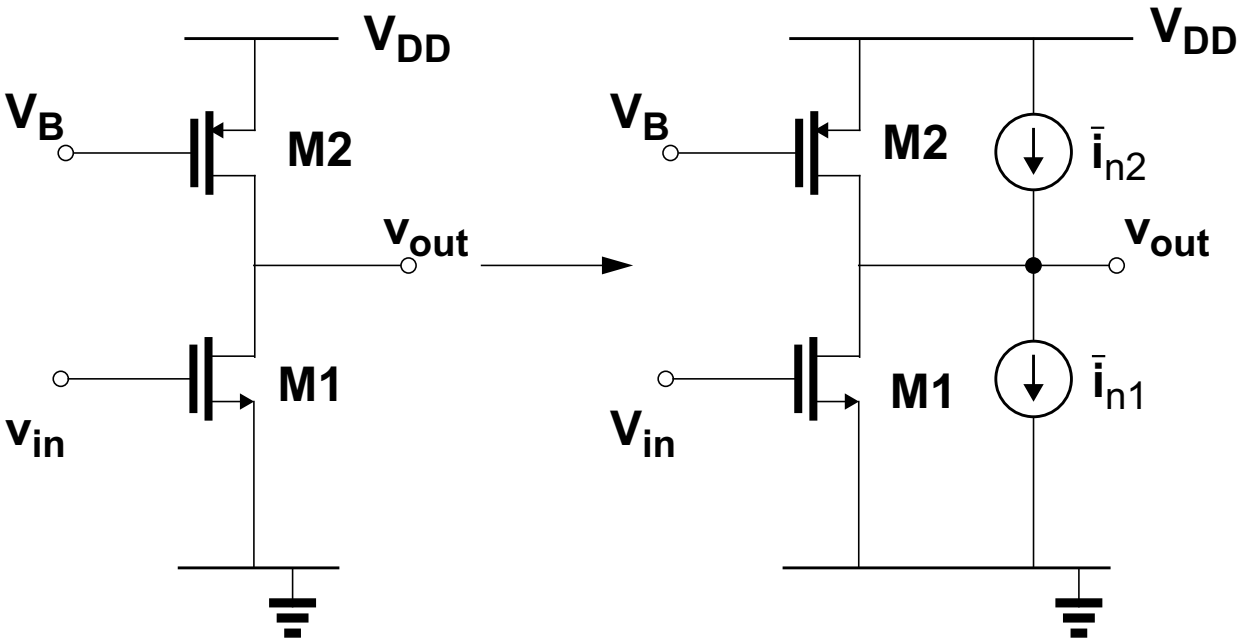


Current at output node

$$g_{m1}v_{in} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

(ii) What is the input-referred thermal noise voltage density of M1?
What is the input-referred thermal noise voltage density of M2?
Answers should be in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T.



Noise current of MOS: $\overline{i_n^2} = 4kT\left(\frac{2}{3}g_m\right)$

Input-referred noise of M1

$$\overline{v_{niM1}} = \frac{\overline{i_{nM1}}}{g_{m1}} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m1}\right)}}{g_{m1}} = \sqrt{\frac{4kT\left(\frac{2}{3}\right)}{g_{m1}}}$$ rms noise $V/\sqrt{Hz}$

Input-referred noise of M2

$$\overline{v_{niM2}} = \frac{\overline{i_{M2}}}{g_{m1}} = \frac{\sqrt{4kT\left(\frac{2}{3}g_{m2}\right)}}{g_{m1}} = \sqrt{4kT\left(\frac{2}{3}\frac{g_{m2}}{g_{m1}^2}\right)}$$ rms noise $V/\sqrt{Hz}$

(iii) Calculate the input-referred thermal noise voltage density of M1 and the input-referred thermal noise voltage density of M2 if
V_{B1}=1.0V, V_{B2}=1.25V, V_{DD}=3V, V_{tn} = 0.75V, V_{tp} = -0.75V, $\lambda_n=\lambda_p=0.04V^{-1}$.
The drain current of M1 is 100μA.
Which is the dominant noise source?

g_m given by

$$g_m = \frac{2I_D}{(V_{GS}-V_T)}$$

$$g_{m1} = \frac{2 \cdot 100\mu A}{1V - 0.75V} = 800\mu A/V \qquad g_{m2} = \frac{2 \cdot 100\mu A}{1.75V - 0.75V} = 200\mu A/V$$

Input-referred noise of M1

$$\overline{v_{niM1}} = \sqrt{\frac{4kT\left(\frac{2}{3}\right)}{g_{m1}}} = \sqrt{\frac{(4 \cdot 1.38\times10^{-23} \cdot 300)\left(\frac{2}{3}\right)}{800\mu A/V}} = 3.71nV/\sqrt{Hz}$$

Input-referred noise of M2

$$\overline{v_{niM2}} = \sqrt{4kT\left(\frac{2}{3}\frac{g_{m2}}{g_{m1}^2}\right)} = \sqrt{(4 \cdot 1.38\times10^{-23} \cdot 300)\left(\frac{2}{3}\right) \cdot \frac{200\mu A/V}{800\mu A/V^2}} = 1.86nV/\sqrt{Hz}$$

M1 is dominant noise source

(iv) Calculate the total noise voltage at the output over a bandwidth of 1MHz.
If the input signal v_{in} is a $1mV_{rms}$ sine wave, calculate the signal-to-noise ratio in dB at the output over a bandwidth of 1MHz.

$$g_{ds1} = \lambda_n I_D = 0.04V^{-1}\,100\mu A = 4\mu A/V$$
$$g_{ds2} = \lambda_n I_D = 0.04V^{-1}\,100\mu A = 4\mu A/V$$

Gain of stage

$$Gain = -\left(\frac{g_{m1}}{g_{ds1}+g_{ds2}}\right) = -\frac{800\mu A/V}{8\mu A/V} = -100$$

Total input-referred noise

$$\overline{v_{nitot}} = \sqrt{\left[\frac{4kT\left(\frac{2}{3}\right)}{g_{m1}}\right]^2 + \left[4kT\left(\frac{2}{3}\frac{g_{m2}}{g_{m1}^2}\right)\right]^2}$$

$$\overline{v_{nitot}} = \sqrt{3.71nV/\sqrt{Hz}^2 + 1.86nV/\sqrt{Hz}^2} = 4.15nV/\sqrt{Hz}$$

Total noise at output given by

$$\overline{v_{notot}} = \overline{v_{nitot}} \cdot \left(\frac{g_{m1}}{g_{ds1}+g_{ds2}}\right) \cdot \sqrt{BW} = 4.15nV/\sqrt{Hz} \cdot 100 \cdot \sqrt{1MHz} = 415\mu V_{rms}$$

Output signal

$$v_{out} = -\left(\frac{g_{m1}}{g_{ds1}+g_{ds2}}\right)v_{in} = -\frac{800\mu A/V}{8\mu A/V} \cdot 1mV_{rms} = 100mV_{rms}$$

Signal-to-Noise ratio given by

$$\frac{S}{N} = \frac{100mV}{415\mu V_{rms}} = 241 \qquad \text{or } 47.6 \text{ dB}$$