OLLSCOIL NA hÉIREANN
THE NATIONAL UNIVERSITY OF IRELAND

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

Summer 2011
Engineering (**Electrical & Electronic**) Examination
Processing of Integrated Circuits (UE4008)

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Time allowed **1 ½ Hours**
Answer three out of four questions

Approved calculator permitted.

Question 1

a) The 90nm node (ITRS Roadmap for Semiconductors) is generally considered to be the end of the "Traditional Scaling Era" describe some of the changes in CMOS devices that occurred between 1µm technology to 90nm.
b) What major changes are being introduced beyond the 65nm node?
c) What are the equivalent oxide thickness and the actual thickness in the gate region of a MOS transistor if hafnium oxide with a dielectric constant of 25 is used as the gate dielectric and the resultant capacitance is 3.46×10^{-7} F/cm^2?

Given:
The permittivity of free space is 8.86×10^{-14} F/cm
The dielectric constant of silicon dioxide is 3.9

Question 2

a) Explain why the thermal oxidation rate of silicon slows down over time
b) How is silicon nitride used to form a semi-recessed field oxide profile in CMOS processing
c) Explain what happens dopant that is close to the silicon /silicon dioxide interface during thermal oxidation of silicon for dopants with a segregation coefficient greater than 1 and for dopants with segregation coefficient less than 1.
d) If a <100> silicon wafer on which some areas have an existing silicon dioxide thickness of 200nm and some areas are etched back to bare silicon is thermally oxidised in steam at 1000°C for 60 minutes, what is the final thickness of the oxide on the previously bare areas and on the areas with the existing oxide?

Wet oxidation graph attached

Question 3

a) In relation to a high energy beam of ions striking the surface of crystalline silicon explain the following terms
   (i) Range
   (ii) Projected range
   (iii) Straggle
b) Explain the function(s) of the high temperature heat treatment given to wafers following ion implantation
c) What energy is needed to place the peak of a phosphorus implant at the silicon/oxide interface if the oxide thickness is 0.07μm, and what thickness of oxide is needed to protect other parts of the silicon from this implant? The implant dose is 1X $10^{16}/cm^2$and the background concentration is 1x $10^{15}/cm^3$.

Given:

$C_{(x)} = C_p.\exp[-(x-R_p)^2/2\Delta R_p^2]$

Projected Range and Projected Standard Deviation Graphs attached.

Question 4

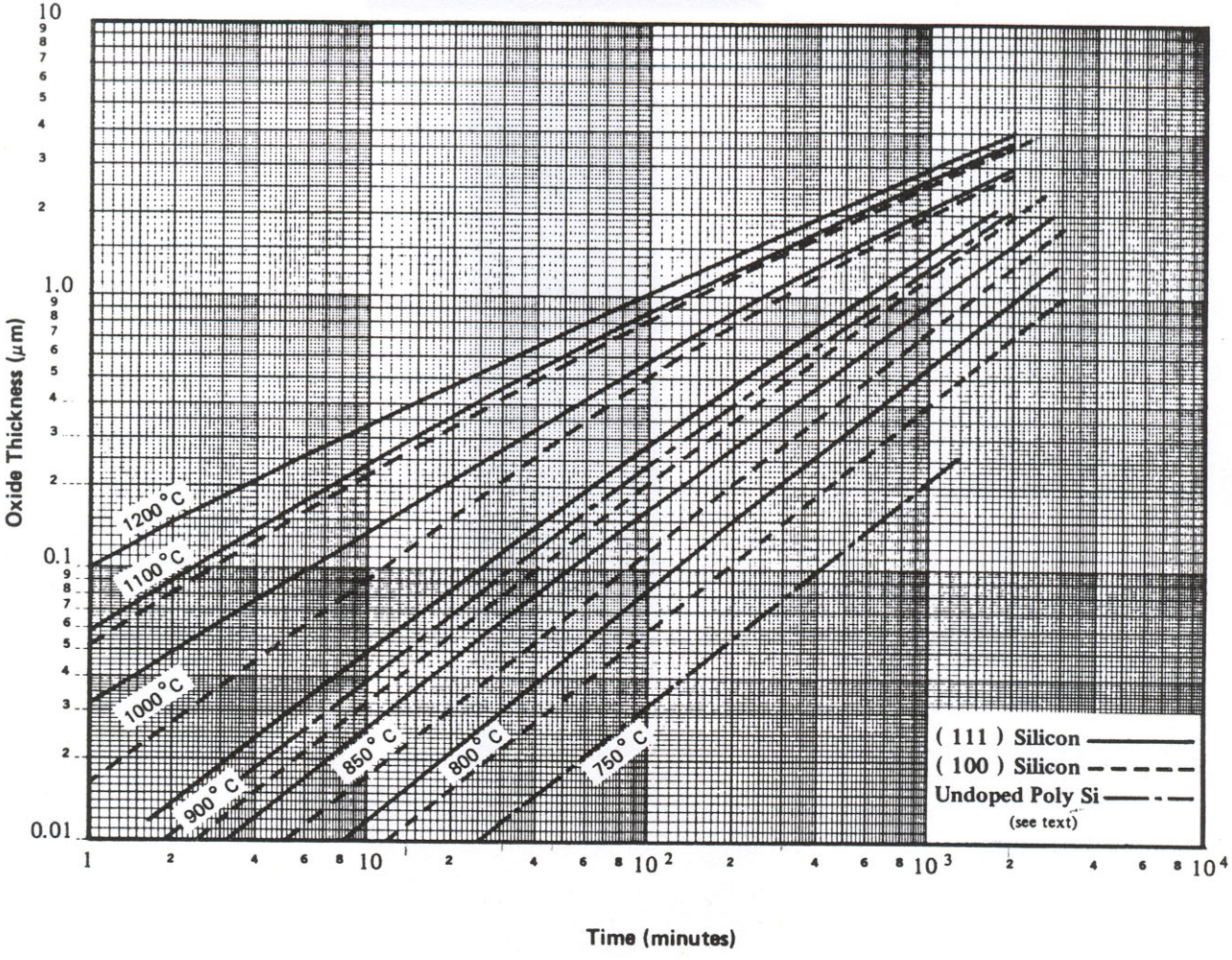
a) Describe how parasitic or field devices can be formed in a CMOS process; what measures can be taken to prevent the turn on of these devices, use diagrams to illustrate the answer.
b) Compare an SOI (Silicon-on-Insulator) CMOS process with a bulk silicon process use cross-sectional diagrams to illustrate the answer. Mention the two principal types of SOI transistor configuration.
c) In an NMOS process with a minimum allowed drawn gate length of 2.0μm, a threshold voltage of 0.8V and a power supply voltage of 10V. What is the smallest device that can be used to deliver a current of 10mA between the source and drain?

Given:

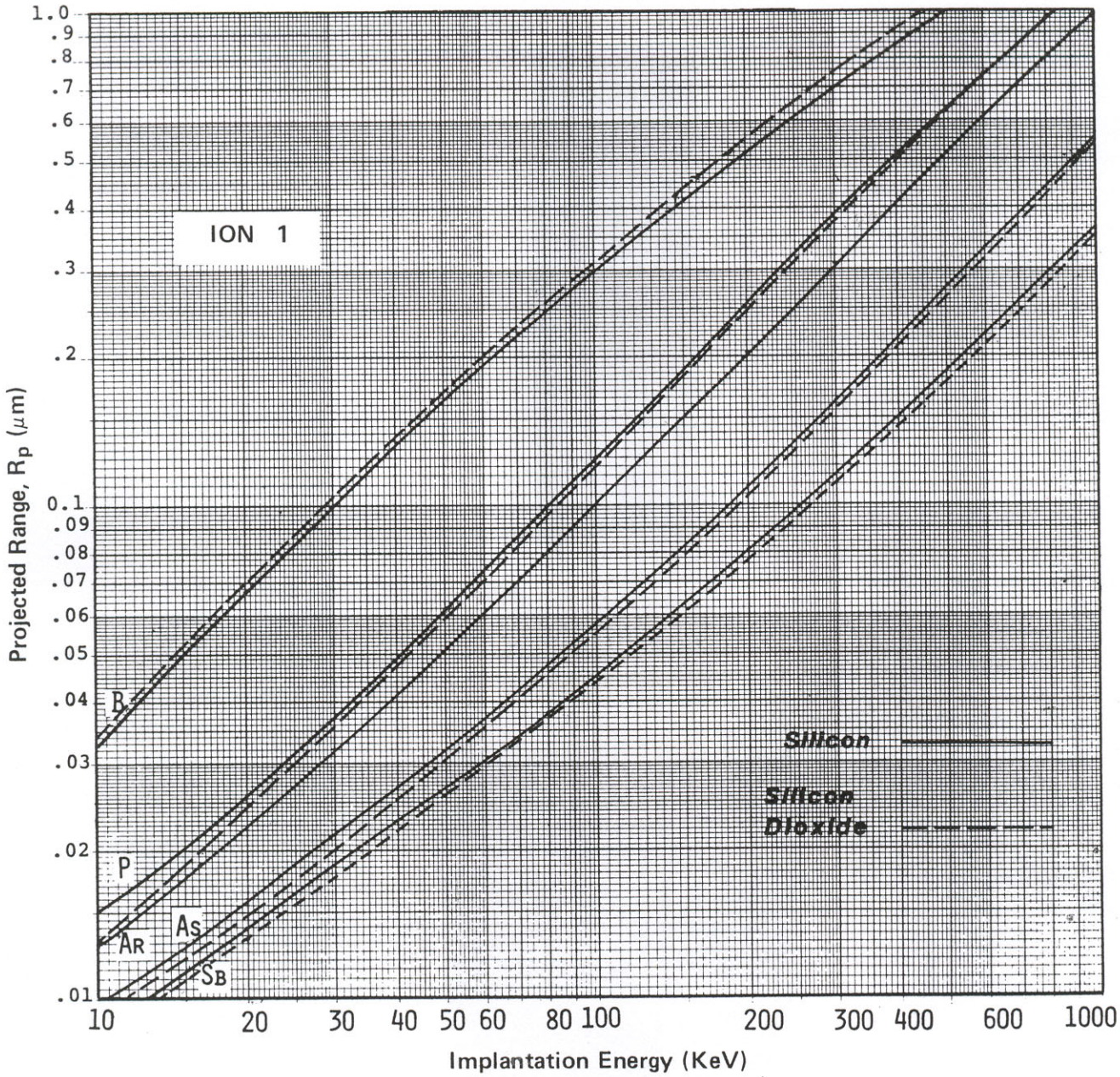
$\mu_n = 1000cm^2/V.s$

$C_{ox} = 5 \text{ X } 10^{-8}$ F/ cm^2

OXIDE GROWTH IN PYROGENIC STEAM (640 Torr) [2,3,4,5]



PROJECTED RANGE IN SILICON & SILICON DIOXIDE[1]



PROJECTED STANDARD DEVIATION IN SILICON & SILICON DIOXIDE[1]