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THE NATIONAL UNIVERSITY OF IRELAND, CORK

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

SUMMER EXAMINATIONS, 2013

B. E. (ELECTRICAL AND ELECTRONIC)
M.ENG.SC. (MICROELECTRONICS)
VSEU (VISITING EUROPEAN)

RF IC Design
EE4011

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Answer *five* questions.

All questions carry equal marks.

Time allowed: *3 hours*

The use of departmental approved non-programmable calculators is permitted.

Smith Charts are appended to this paper. Detach and use as required. Write your examination number on any charts you use and return them with your examination script.

The following physical constants may be used if necessary:

Boltzmann's Constant: $k = 1.381 \times 10^{-23}$ J/K
Elementary Charge: $q = 1.602 \times 10^{-19}$ C
Vacuum Permittivity: $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m
Dielectric Constant of Silicon-Dioxide (SiO_2): $\varepsilon_r = 3.9$

The following trigonometric relationship may be used if necessary:

$$\cos A \sin B = \frac{1}{2}\left[\left(\sin(A+B) - \sin(A-B)\right)\right]$$

The questions begin on the next page.

1. (a) Draw a cross-section of a typical MESA-isolated GaAs MESFET, clearly labeling all the important elements, and briefly describe how device isolation is achieved.

[*4 marks*]

(b) Show a suitable small-signal model for a GaAs MESFET and from this derive expressions for the *y*-parameters of the device in a common source configuration with the gate considered to be port 1 and the drain considered to be port 2. For simplicity, you may ignore the gate-drain capacitance.

[*8 marks*]

(c) The *y*-parameters of a MESFET connected as in part (b) have been measured at a frequency of 2.5GHz giving the following values:

$y_{11} = 0.0377 \angle 73.6°$
$y_{12} = 0.0$
$y_{21} = 0.0959 \angle -16.4°$
$y_{22} = 0.0127 \angle 38.1°$

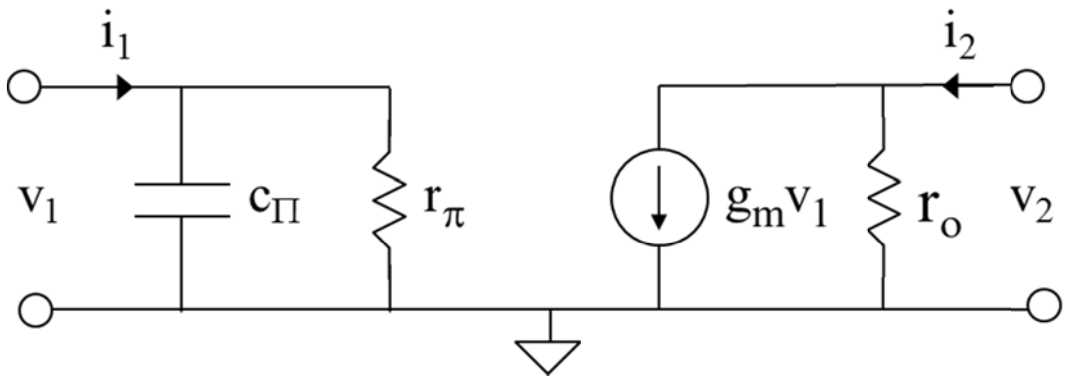
Determine the elements of the small-signal model from these measurements.

[*5 marks*]

(d) A MESFET device has been laid out with a single long and thin gate stripe with W=200 μm and L=0.5μm and with the gate contacted on one side only, giving a gate resistance, R_G, of 10Ω. If the device is laid out as 5 parallel fingers but keeping the same total width, what is the new value of gate resistance if the gate fingers are contacted on both sides?

[*3 marks*]

2. A simplified two-port small-signal model of a BJT configured in a common emitter configuration is shown below. Port 1 is at the base and port 2 is at the collector.



The values of the small-signal elements are as follows:

$$c_\pi = 40\,pF \quad r_\pi = 500\Omega \quad g_m = 0.25S \quad r_o = 200\Omega$$

(a) Determine expressions for i_1 and i_2 in terms of v_1 and v_2.

[*2 marks*]

(b) Determine expressions for the *z*-parameters of the BJT and evaluate the *z*-parameters at a frequency of 0.5*GHz*.

[8 *marks*]

(c) Assuming that the device is configured for measurement of h_{21}, show the following quantities as a function of frequency on a diagram: h_{21}, the currents i_1 and i_2 and the currents in c_π and r_π. Clearly label the important features on this diagram.

[4 *marks*]

Note: graph paper is not required – a diagram in the normal answer book is sufficient.

(d) For this BJT determine:

(i) The output short-circuit current gain, h_{21}, at low frequencies.

[2 *marks*]

(ii) The frequency at which the magnitude of the current flowing through the capacitor c_π is the same as that flowing through the resistor r_π.

[2 *marks*]

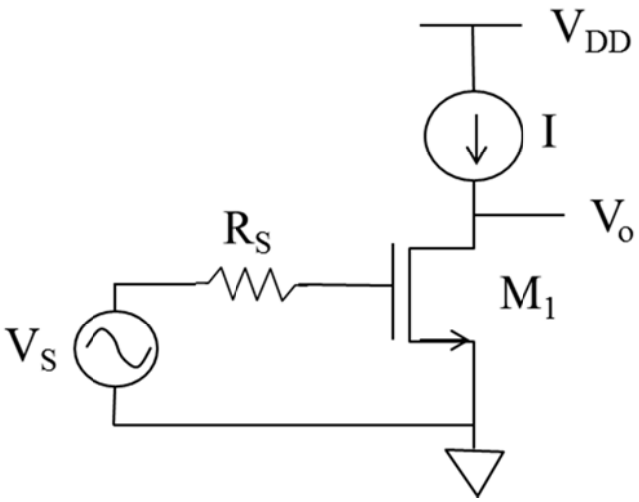
(iii) The cut-off frequency, f_T.

[2 *marks*]

3. (a) State the formula for the noise factor of an amplifier and define all the quantities in the formula.

[2 *marks*]

(b) A common-source amplifier is shown below. It is biased by means of an ideal current source, I, and is driven by a signal-source, V_S, with source resistance, R_S.



The only sources of noise in the circuit are the thermal noise of the source resistance, R_S, and the thermal noise of the MOSFET, M_1, which can be represented as a noise current source between the drain and source as follows (for a bandwidth of 1*Hz*):

$$\overline{i_n^2} = 4kT\gamma g_m$$

where γ is a device-dependent constant.
Determine an expression for the Noise Factor of this amplifier for a bandwidth of 1*Hz*.You may ignore the capacitances of the MOSFET and represent it by a two-element small-signal model with a transconductance, g_m, and an output resistance, r_o.

[*14 marks*]

(c) Determine the noise figure (in *dB*) for an amplifier such as that described in part (b) with the following parameters

$$R_S = 50\Omega \quad \gamma = \frac{2}{3} \quad g_m = 0.01S$$

[*2 marks*]

(d) Illustrate the spectral noise density as a function of frequency for a MOSFET which has both thermal and $1/f$ noise components and illustrate the "corner frequency" typically seen on this type of plot.

[*2 marks*]

4. An RF NPN transistor is used to make a Low Noise Amplifier (LNA). It has the following characteristics at 1GHz in a 50Ω system:

$$s_{11} = 0.65\angle -160° \quad s_{12} = 0.1\angle 30° \quad s_{21} = 4.0\angle 90° \quad s_{22} = 0.4\angle -60°$$

(a) Determine the stability factors for the LNA and whether it is unconditionally stable.

[*2 marks*]

(b) Determine the centre points and the radii of the source and load stability circles and draw these on a Smith Chart. (You need only draw the segments of the circles that are near or inside the unit circle on the Smith Chart). Comment on whether the stability circles indicate any restrictions if the LNA is to be designed for maximum unilateral transducer gain.

[4 *marks*]

The source and load stability circles are described by the following formulas where the symbols have their usual meanings:

$$CS_S = \frac{s_{11}^{\ *} - \Delta^* s_{22}}{|s_{11}|^2 - |\Delta|^2} \quad RS_S = \frac{|s_{12}s_{21}|}{\left||s_{11}|^2 - |\Delta|^2\right|} \quad CS_L = \frac{s_{22}^{\ *} - \Delta^* s_{11}}{|s_{22}|^2 - |\Delta|^2} \quad RS_L = \frac{|s_{12}s_{21}|}{\left||s_{22}|^2 - |\Delta|^2\right|}$$

(c) Design input and output matching networks for the LNA to achieve maximum unilateral transducer gain, if the LNA is to work with source and load impedances of 50Ω.

[*10 marks*]

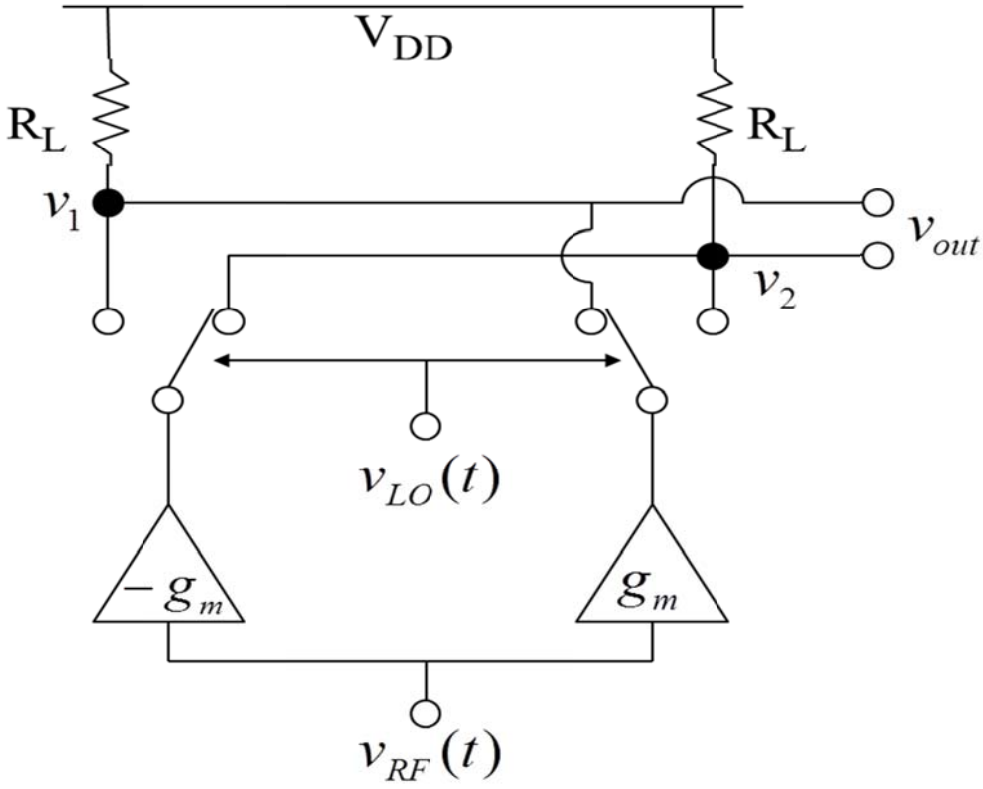
(d) (i) Determine the maximum unilateral transducer gain of the amplifier (in dB) designed in part (c).

[*2 marks*]

(ii) Determine the Unilateral Figure of Merit for this transistor and comment on whether the unilateral assumption is accurate enough when designing an LNA with this transistor.

[*2 marks*]

5. The diagram below shows a simplified schematic of a double-balanced mixer for RF applications. The switches are ideal single-pole, double-throw switches controlled by the LO waveform and they operate 180° out of phase with each other as indicated by the connections on the diagram. Each transconductance stage draws a DC bias current, I_{DC}, through its output terminal.



(a) Assuming the LO waveform is a square wave, and the RF waveform is cosinusoidal with a form $V_{RF}\cos(\omega_{RF}t)$, develop an expression for the output voltage, V_{OUT}, which clearly shows the frequency spectrum of the output waveform.

[12 *marks*]

Note: A square wave which toggles between 0 and 1V at a frequency of ω radians/s has a Fourier expansion as follows:

$$s(t) = \frac{1}{2} + \frac{2}{\pi}\left[\sin(\varpi t) + \frac{1}{3}\sin(3\varpi t) + \frac{1}{5}\sin(5\varpi t) + \cdots\right]$$

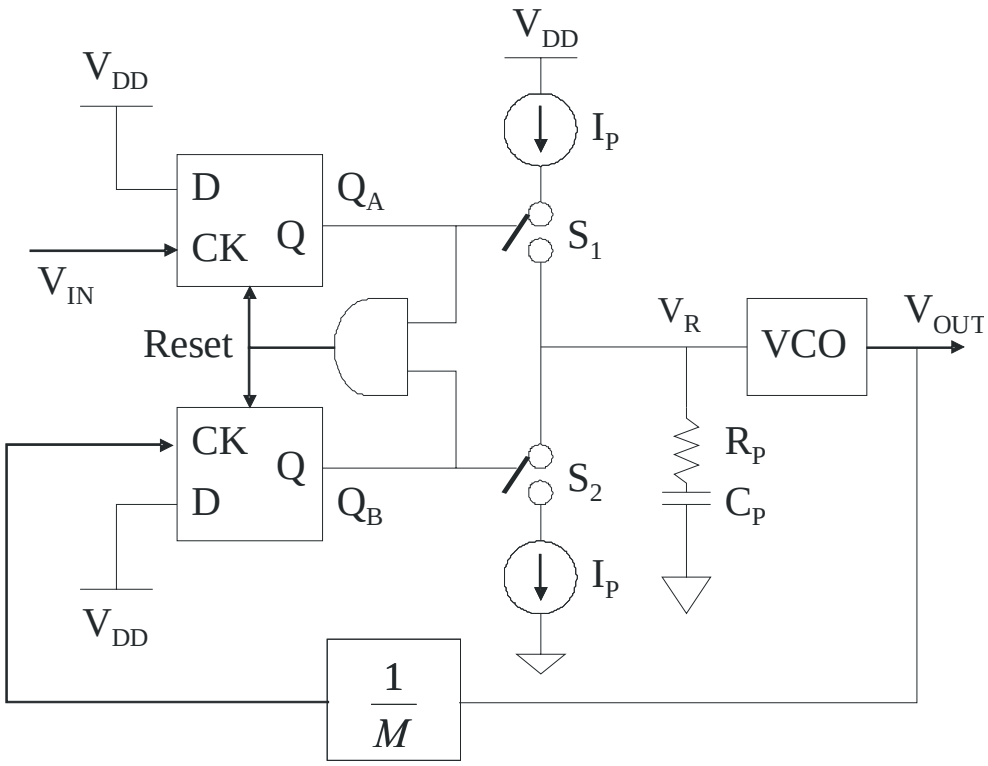
(b) If the transconductance elements are implemented with bipolar transistors connected as emitter coupled pairs with a total tail current of 0.5mA, and the load resistors (R_L) have a value of 2kΩ, determine the voltage conversion gain of the mixer at 300K.

[4 *marks*]

(c) Show a circuit diagram of a Gilbert cell that implements a double-balanced mixer with bipolar transistors. Clearly show all the interconnections and label the inputs and outputs.

[*4 marks*]

6. A Type II PLL is shown below.



(a) Derive an expression for the closed-loop response of the Type II PLL. You may use the "average current" method to determine the transfer function of the PFD/CP circuit.

[10 *marks*]

Note: The denominator of 2nd-order systems is written in standard form as:

$$s^2 + 2\varsigma\omega_n s + \omega_n^2$$

(b) A Type II PLL has the following parameters:

I_P=0.3mA, C_P=50pF, R_P=20kΩ, K_{VCO}=200MHz/V, M=250

(i) Determine the natural frequency of the closed-loop system.

[2 *marks*]

(ii) Determine the damping factor of the closed-loop system.

[2 *marks*]

(c) Show a suitable schematic for a Delay Locked Loop (DLL) to produce eight (8) clock phases with equal delay between the phases and describe the unique elements of the circuit compared to a standard PLL.

[6 *marks*]

7. (a) Draw a detailed block-level architecture of a single-chip GPS/Galileo receiver and outline the functions of the main blocks in the IC providing details of frequencies, bandwidth, gain, noise levels and data rates as appropriate.

[*10 marks*]

(b) Answer EITHER section (i) OR section (ii) below:

EITHER:

(i) For the GPS receiver in part (a), select one block from the overall architecture and discuss the design of this block in detail. In your discussion, show a more detailed schematic diagram of the block you choose (if necessary) and outline the typical design trade-offs that must be made when designing this block, as well as the typical performance characteristics that can be achieved with a single-chip CMOS approach.

[*10 marks*]

OR:

(ii) Discuss the operation of the GPS system including the frequencies, power levels and the modulation and coding schemes used. Show how the characteristics of the GPS system lead to the specifications for receiver systems such as the single-chip solution discussed in part (a).

[*10 marks*]

End of Examination Paper