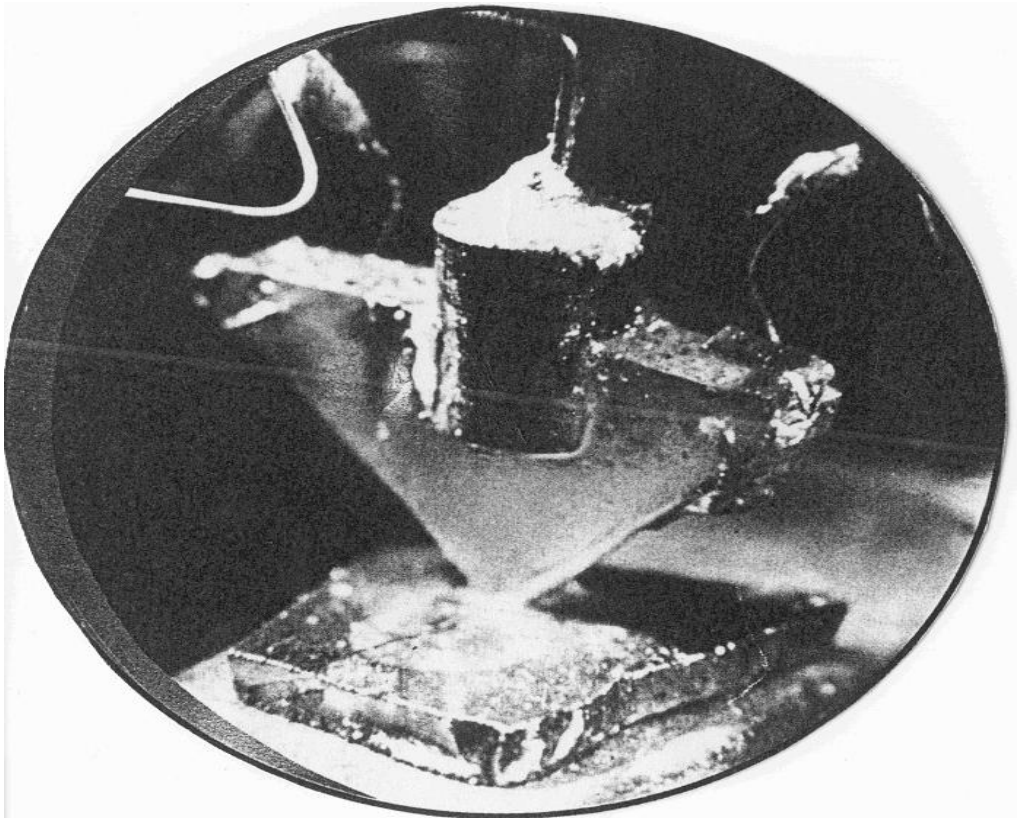
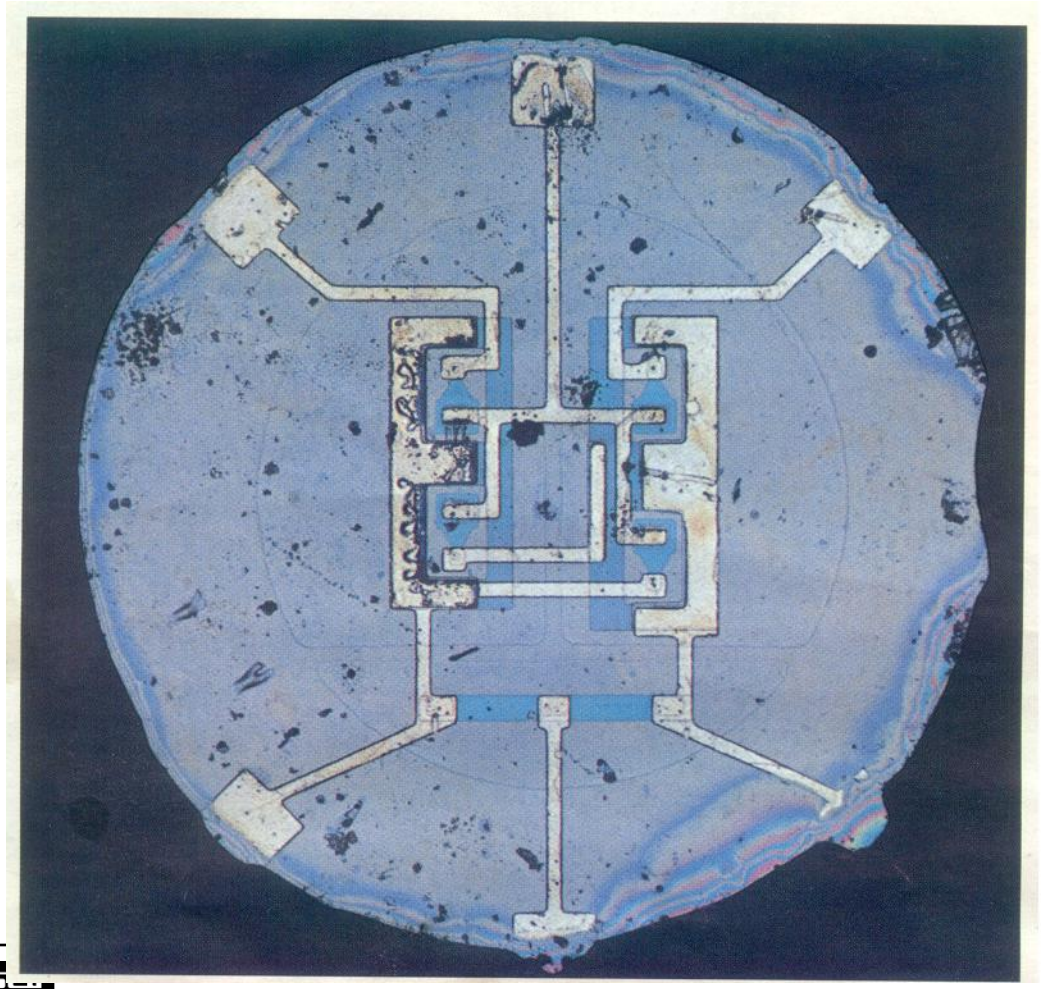
# Introduction to Semiconductor Processing

# The Original



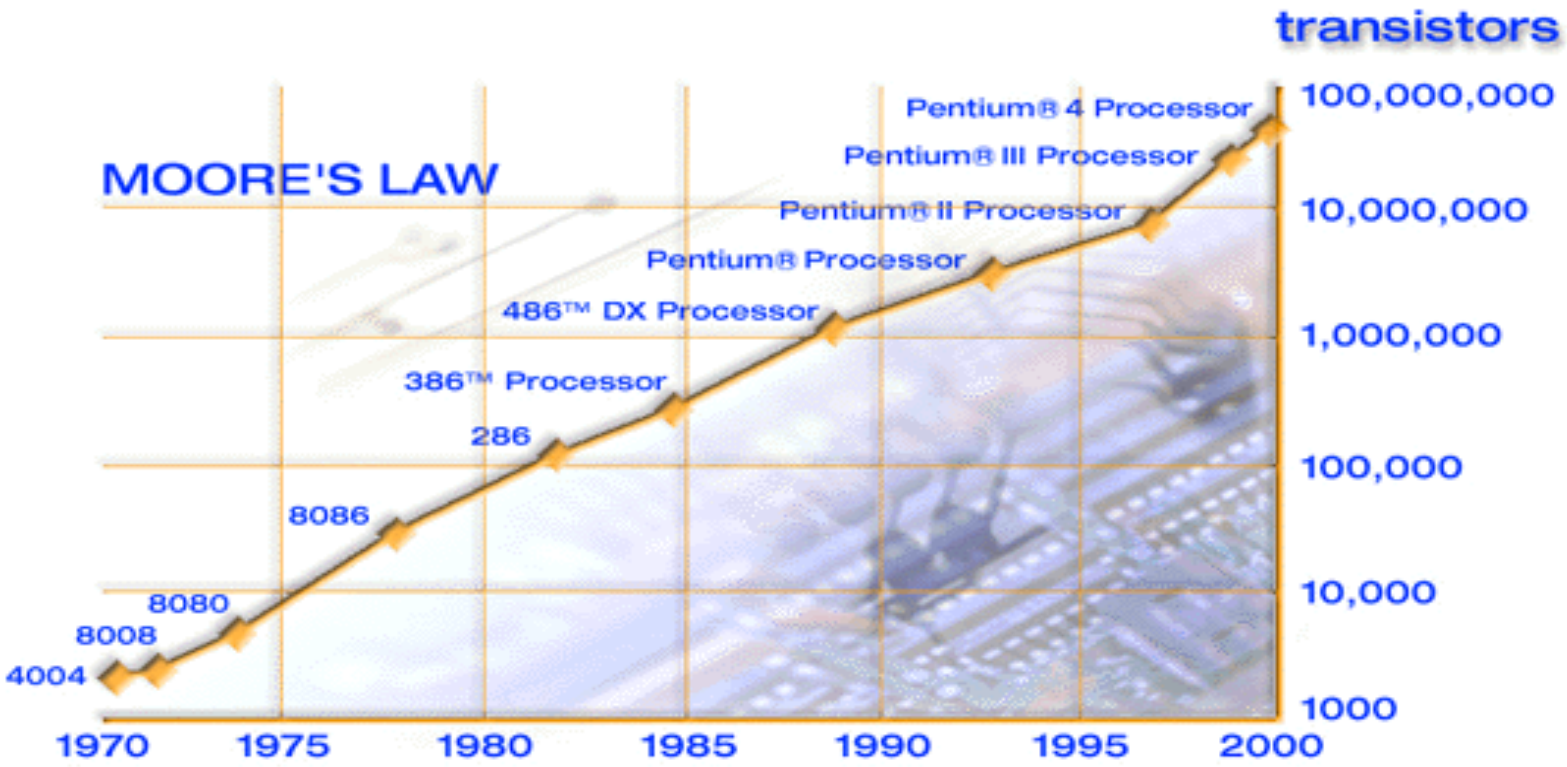
**Bell Labs.**
**24th Dec. 1947**

# First Integrated Circuit

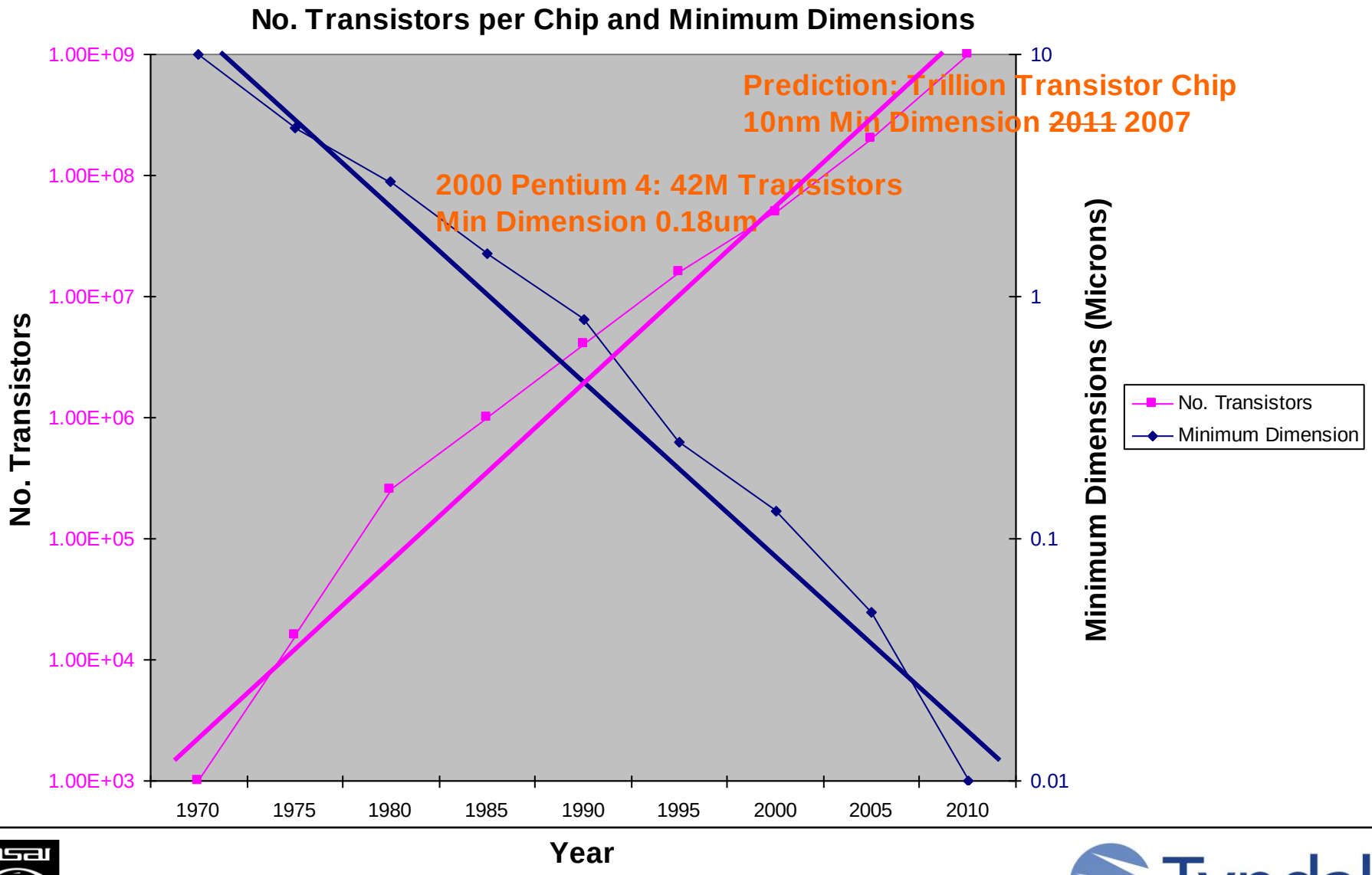


**Fairchild 1961:**
**Flip-flop, world's first monolithic chip**

# Moore's Law



# Trend in circuit size



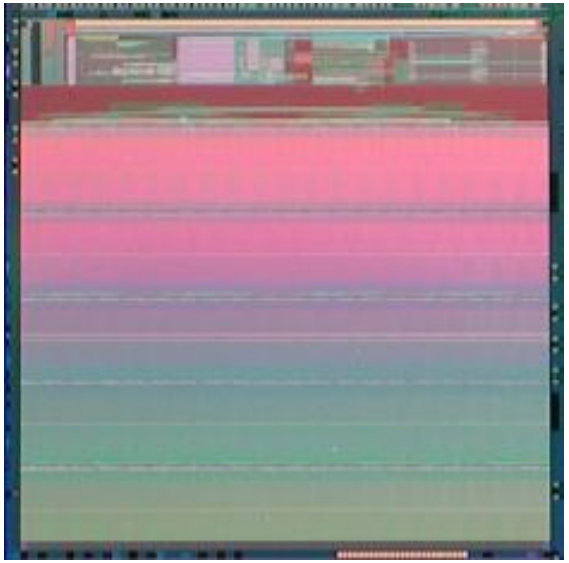
# Intel Pentium 4 Microprocessor

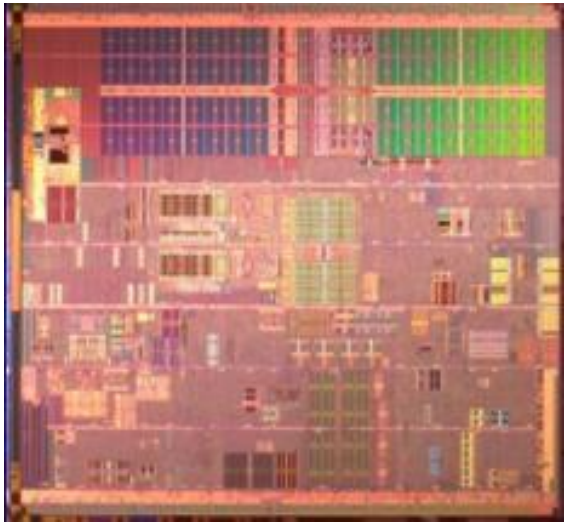
**0.18μm design rules**

**42M Transistors**

**1.5GHz speed of operation**

# 90nm Technology



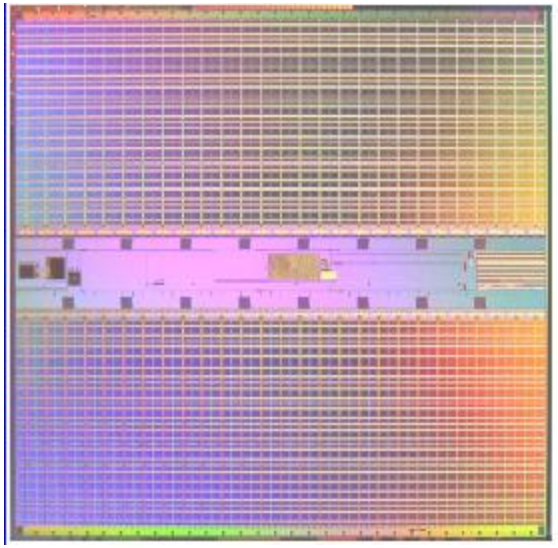


- 52Mbit SRAM Chip
- 130nm Design Rules
- 109mm$^2$ Die Size
- 330 million transistors

- CPU Chip
- 112mm2 Die Size
- 125 Million transistors

# 65nm Technology

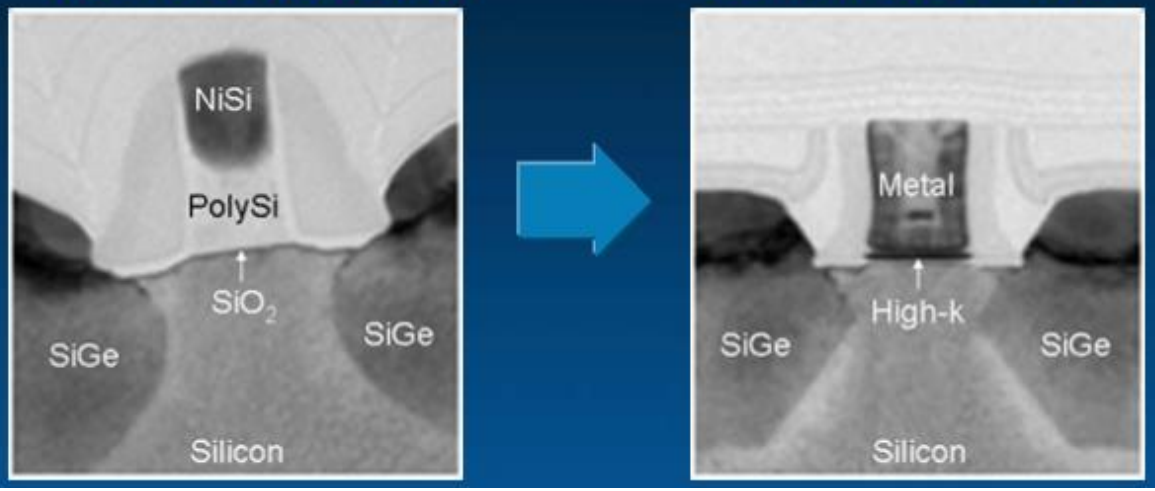
- 0.57 μm2 cell size
- >0.5 billion transistors•
- 110 mm2 chip size•
- Uses all process features
- Capable of supporting Vdd at 0.7V
- Fully functional 70 Mbit SRAM chips have been fabricated.



# High-k + Metal Gate Transistors

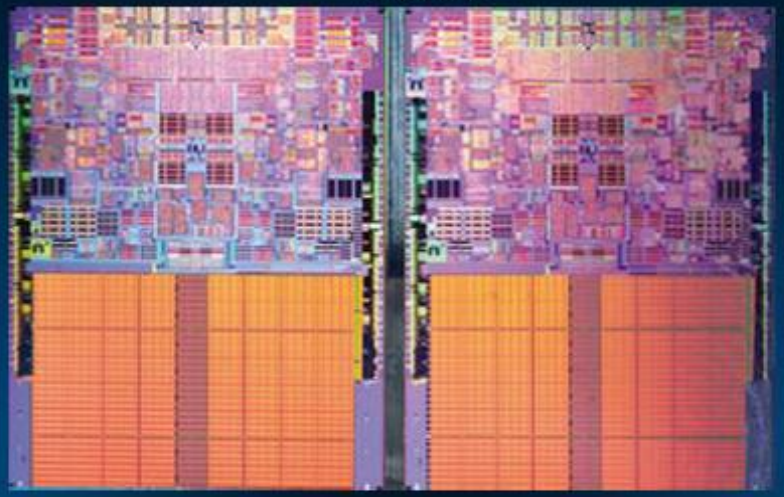
| | |
|---|---|
| Improved Transistor Density | ~2x |
| Improved Transistor Switching Speed | >20% |
| Reduced Transistor Switching Power | ~30% |

**65 nm Transistor** | **45 nm HK + MG**



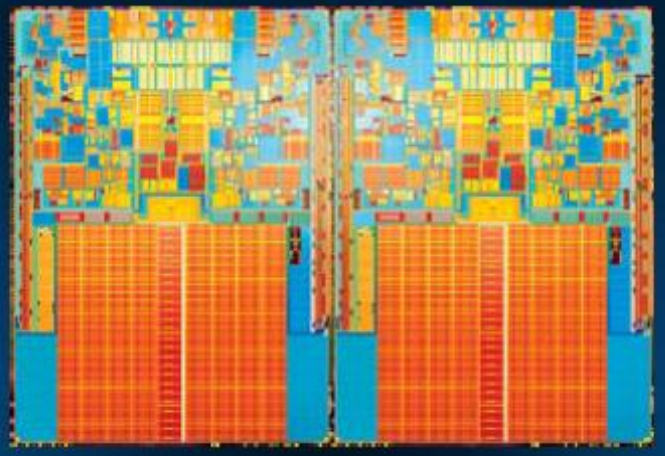
# 45nm Hi-k Processor Advantage

Quad-core Intel® Xeon® 5300 Processor (Clovertown) 65nm



143 $mm^{2*}$ 143 $mm^{2*}$

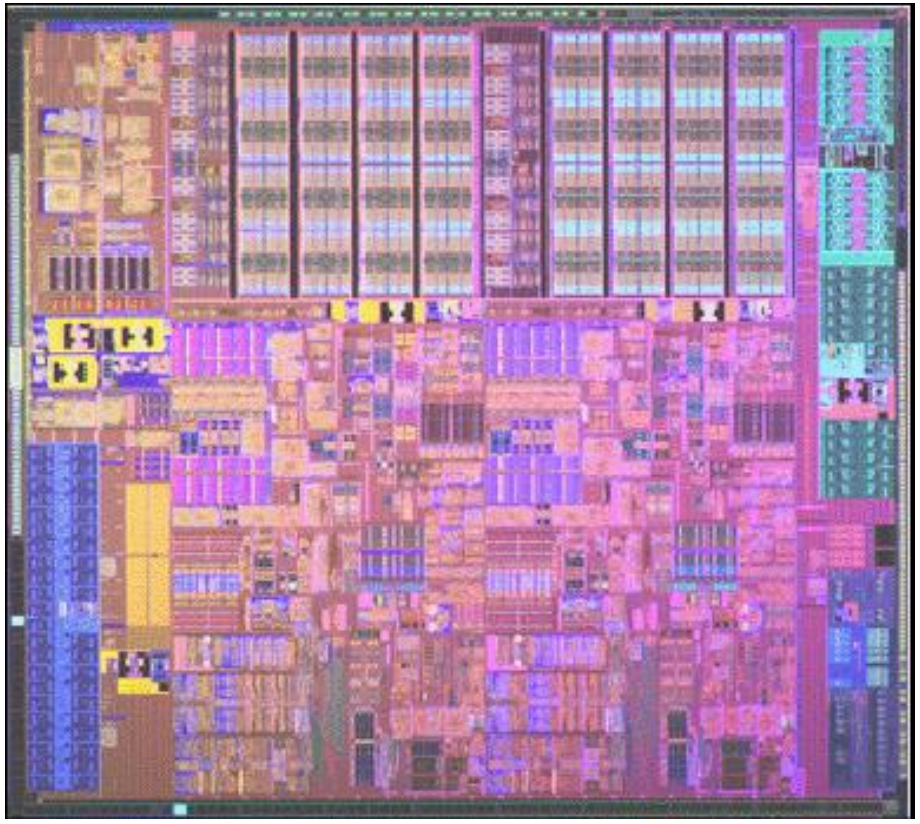
Quad-core Intel® Xeon® 5400 Processor (Harpertown) 45nm Hi-k



107 $mm^{2*}$ 107 $mm^{2*}$

**45nm Processor has 820 million transistors on a single chip**

# 32 nm WestmereMicroprocessor



# Intel's Logic Technology Evolution

| Process Name: | P1262 | P1264 | P1266 | P1268 | P1270 |
|---|---|---|---|---|---|
| Lithography: | 90 nm | 65 nm | 45 nm | 32 nm | 22 nm |
| 1st Production: | 2003 | 2005 | 2007 | 2009 | 2011 |

***Moore's Law continues!***

Intel continues to develop a new technology generation every 2 years

# Intel's 32nm Process

8

**32 nm Technology Features**

- 2ndgeneration high-k + metal gate transistors
- 9 copper + low-k interconnect layers
- Immersion lithography on critical layers
- ~0.7x minimum pitch scaling
- Pb-free and halogen-free packages

Lead is below 1000 PPM per EU RoHSdirective (2002/95/EC, Annex A).Some EU RoHSexemptions for lead may apply to other components used in the product package. Applies only to halogenated flame retardants and PVC in components. Halogens are below 900 PPM bromine and 900 PPM chlorine.*32 nm delivers the promise of Moore's Law: Higher performing, lower power, and lower cost transistors*

# Types of Semiconductors

| | | |
|---|---|---|
| **Elemental.** | **(IV)** | **: Silicon, Germanium** |
| **Compound.** | **(IV:IV)** | **: SiC.** |
| | **(III:V)** | **: AIP, AISb, GaAs, InP.** |
| | **(II:VI)** | **: ZnO, CdTe.** |
| | **(IV:VI)** | **: PbS, PbSe, PbTe.** |
| **Alloys.** | **Ternary** | **: AIGaAs, CdMnTe. GaAsP.** |
| | **Quaternary** | **: AIGaAsSb, GaLnAsP.** |

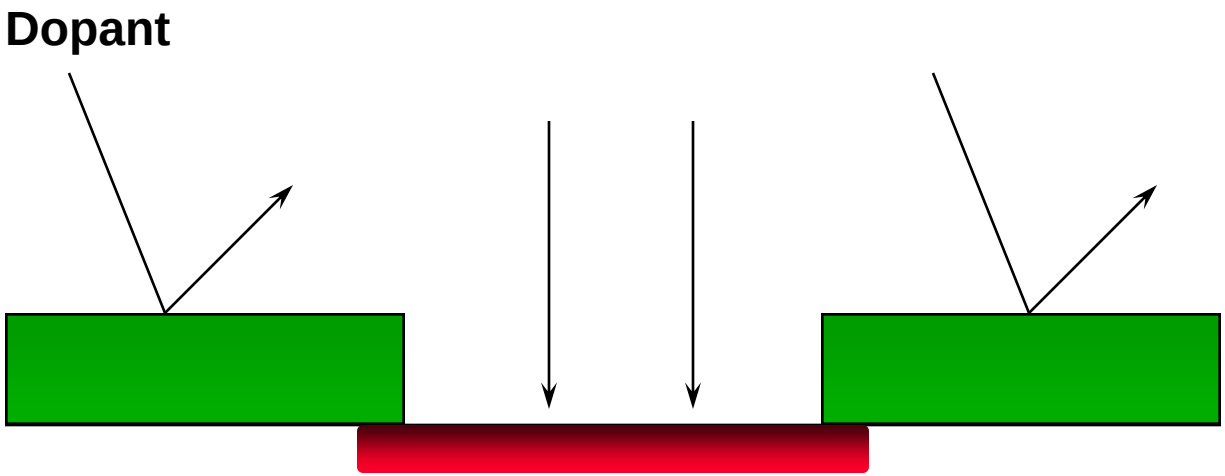
# Why Silicon

| | | |
|---|---|---|
| **Germanium** | **:** | **Original choice**<br>**(unstable/Water soluble oxide)** |
| **Silicon** | **:** | **Most advanced manufacturing status.**<br>**Volume of devices made huge.**<br>**(THE thermal oxide)** |
| **GaAs** | **:** | **Optical and high speed applications**<br>**(Brittle, no oxide)** |
| **Others** | **:** | **Niche areas. eg. Thermal imaging, optics, LED's, flat panel displays** |

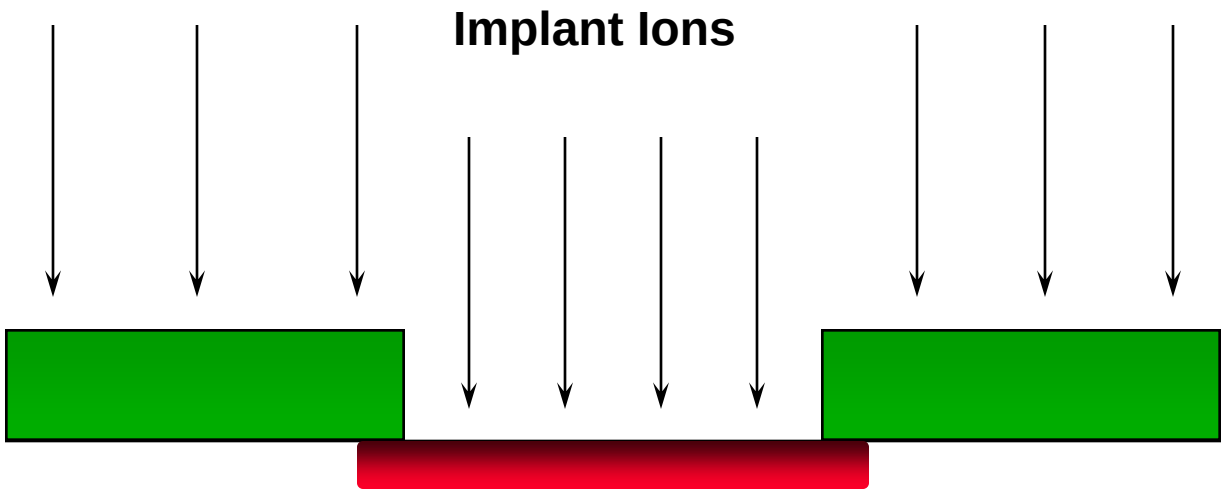
# Silicon Dioxide

- **Good insulator - Breakdown field 10MV/cm**
  - **1000Å oxide will block 100V**
  - **1000Å=100nm=1/100,000 of a cm**
- **Very stable at high temperatures**
  - **up to 1300ºC**
- **A very good diffusion barrier**
- **It is etchable**
  - **Wet in HF**
  - **Dry in Fluorine compounds**

# Oxide as a Diffusion Barrier



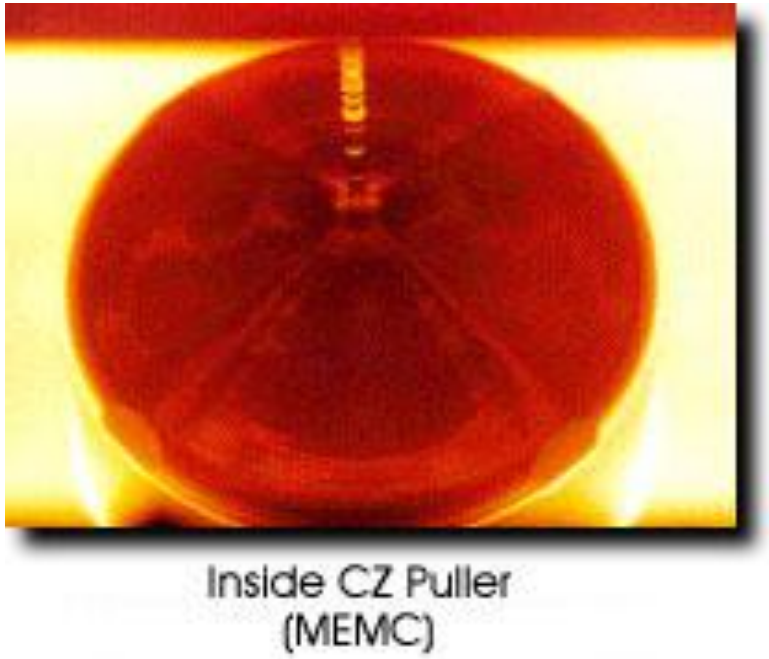
# Oxide as an Implant Barrier



# Polysilicon Ingots

Polysilicon Ingots

# Puller



Inside CZ Puller
(MEMC)

**Cz Crystal Pullers (Mitsubishi Materials Silicon)**

**Inside Cz Puller (MEMC)**

# Single Crystal Silicon Ingot

Single Crystal Silicon Ingot

# Water Lapping Machine

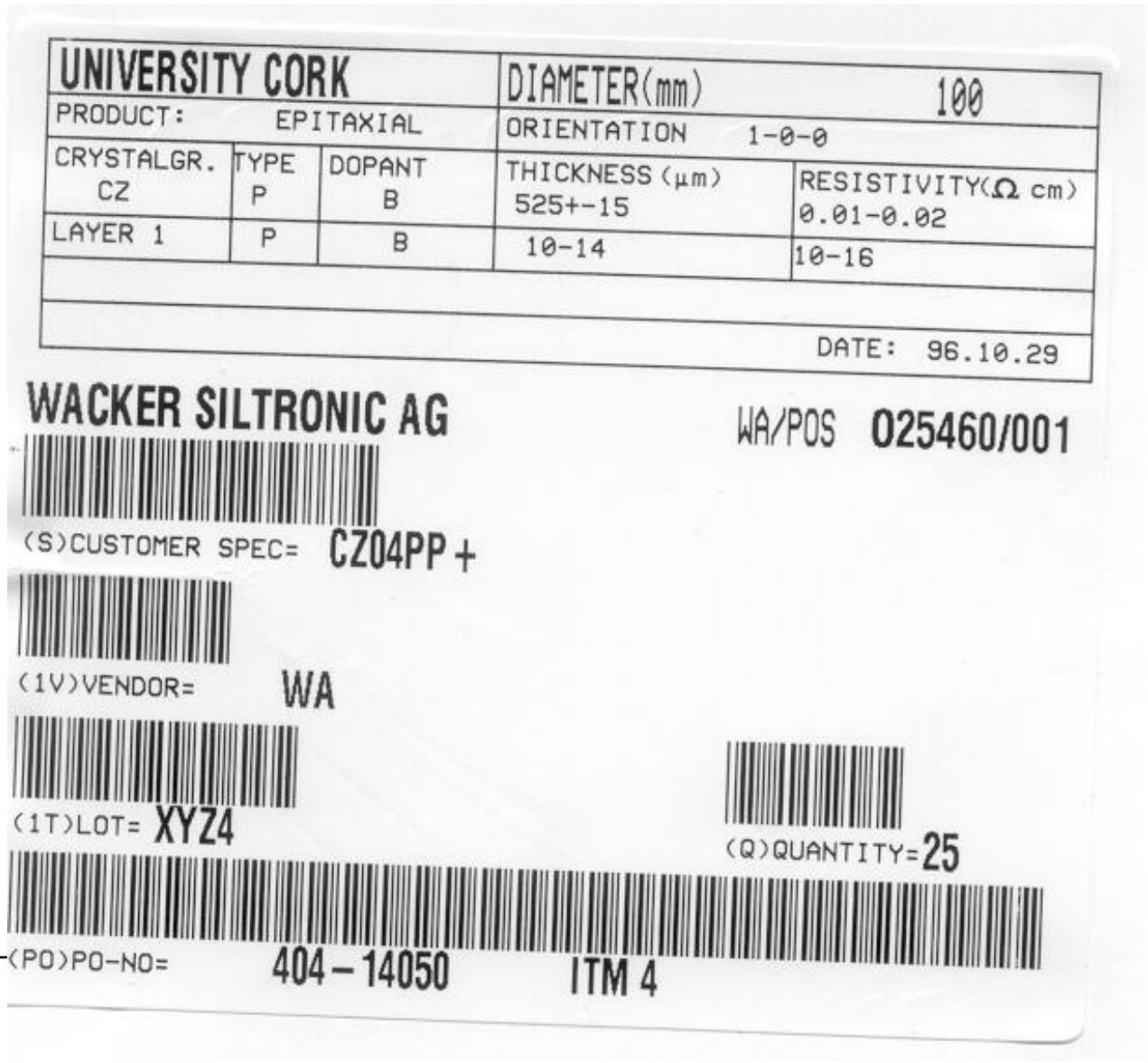
Wafer Lapping Machine
(Mitsubishi Materials Silicon)

# Wafer Parameters -- Label

- **Epitaxial Silicon**
- **Diameter**
- **Orientation**
- **Thickness**
- **Resistivity**
- **Type/Dopant**

# Bulk Wafer Label

# Epitaxial Wafer label



| UNIVERSITY CORK | | | DIAMETER(mm) | 100 |
|---|---|---|---|---|
| PRODUCT: EPITAXIAL | | | ORIENTATION 1-0-0 | |
| CRYSTALGR. CZ | TYPE P | DOPANT B | THICKNESS (µm) 525+-15 | RESISTIVITY(Ω cm) 0.01-0.02 |
| LAYER 1 | P | B | 10-14 | 10-16 |
| | | | | |
| | | | DATE: 96.10.29 | |

WACKER SILTRONIC AG

WA/POS 025460/001

(S)CUSTOMER SPEC= CZ04PP+

(1V)VENDOR= WA

(1T)LOT= XYZ4

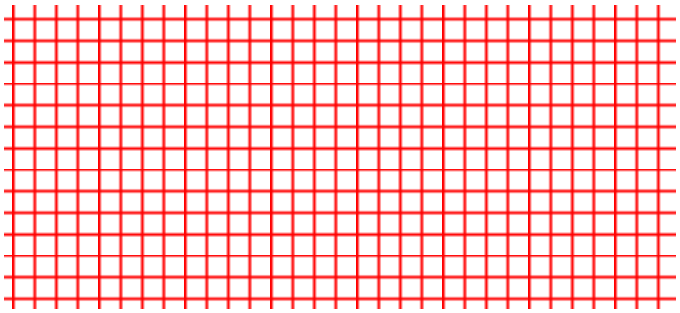
(Q)QUANTITY=25

(PO)PO-NO= 404-14050 ITM 4

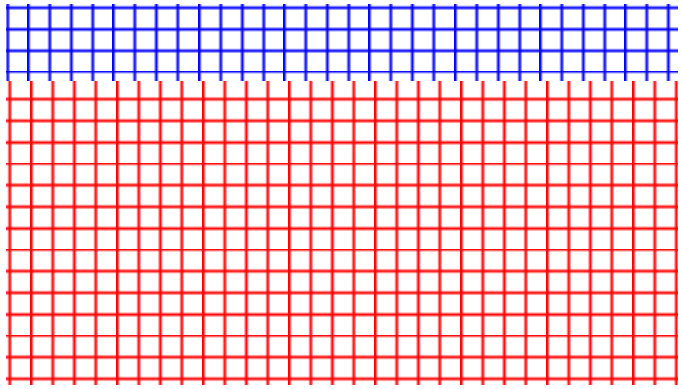
# Epitaxial Silicon

- **Silicon layer either of the same type or different type grown on top of a substrate wafer**
- **Traditionally used for bipolar processes**
- **Now in general use for CMOS processes**

# Epitaxial Growth

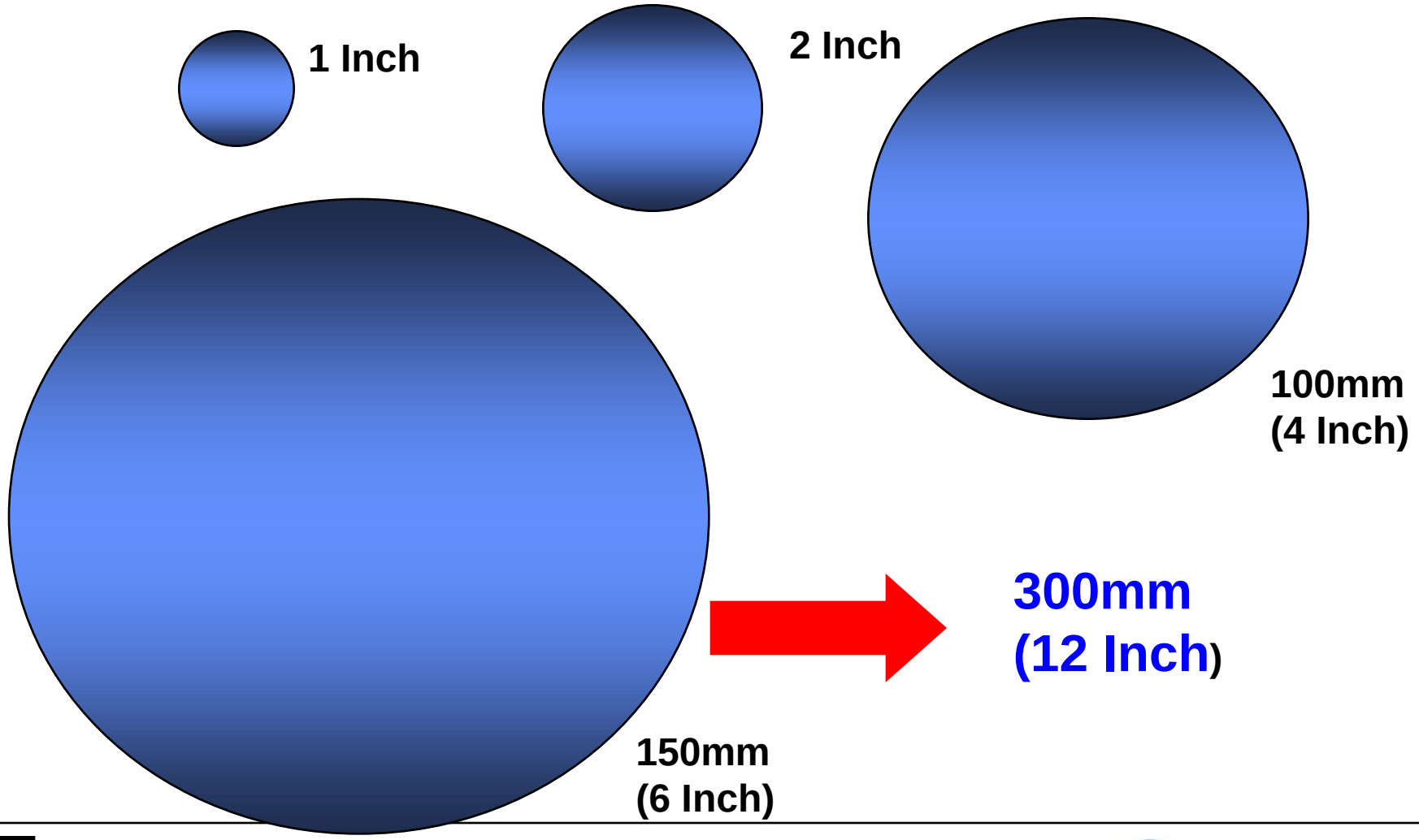


Cross-section of silicon wafer with well defined crystal structure



An epitaxial layer can be grown on top of the existing layer. This layer will have a continuation of the original crystal structure but can have a different doping type and/or a different doping concentration

# Diameter



# Thickness

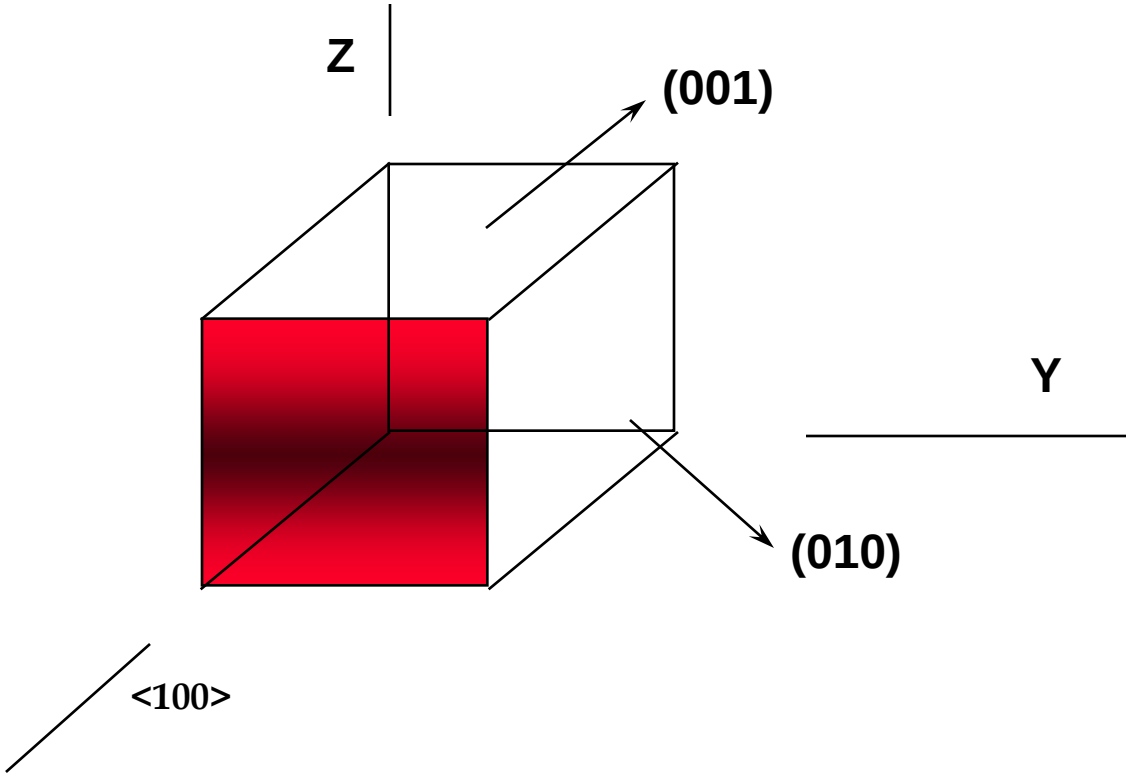
- **Substrate**
  - **100mm wafers typically 525 μm ±15**
- **Layer**
  - **The thickness of the epi layer grown on the substrate**

# Orientation

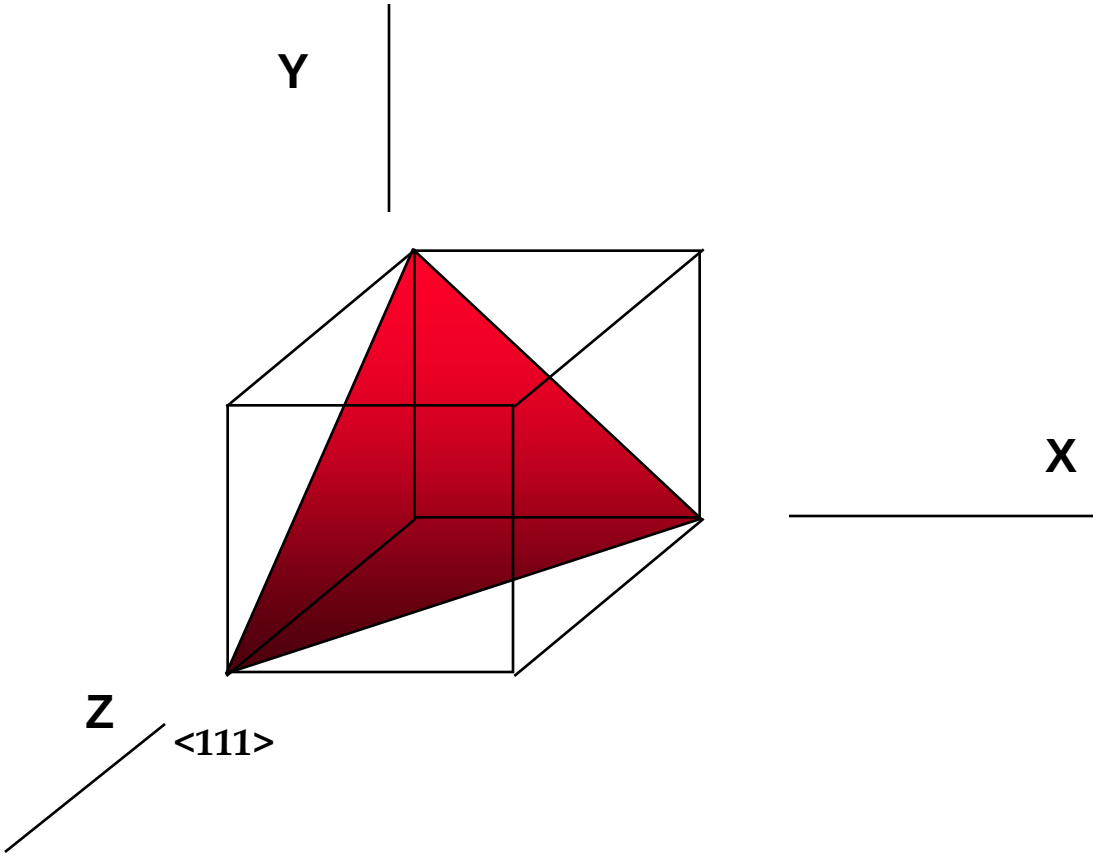
## How the silicon crystal is cut

- **Depends on:**
  - **The process being used**
  - **The applications for the devices**
  - **Historical Reasons**

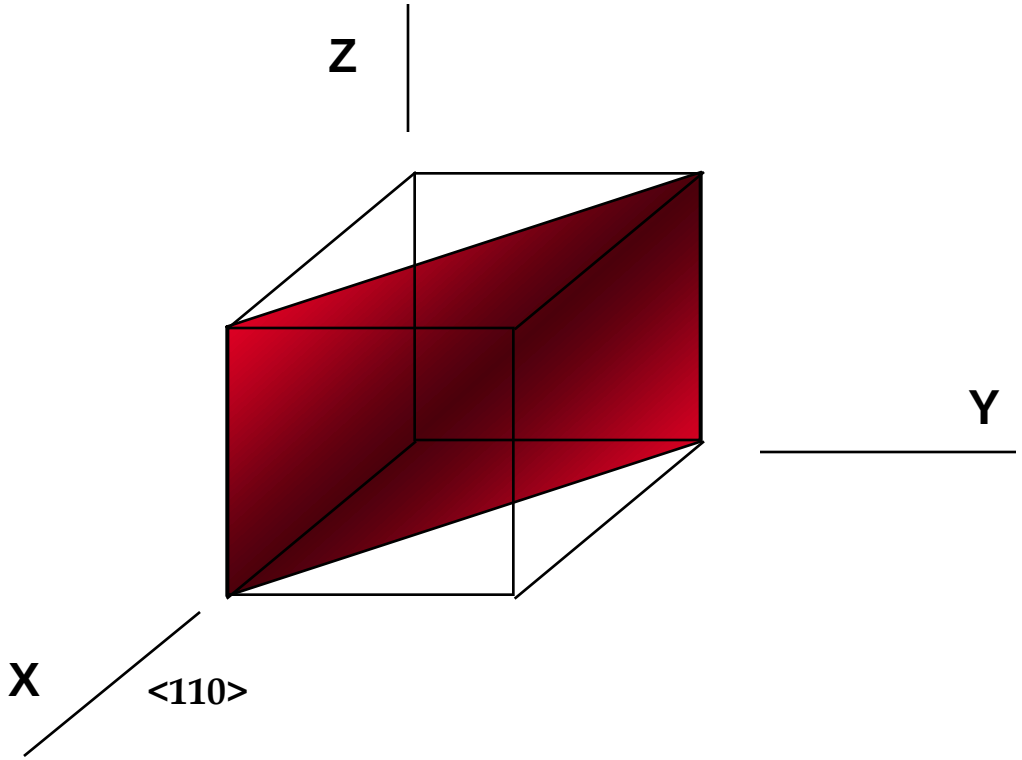
# 100 Orientation



# 111 Orientation



# 110 Orientation



# Resistance

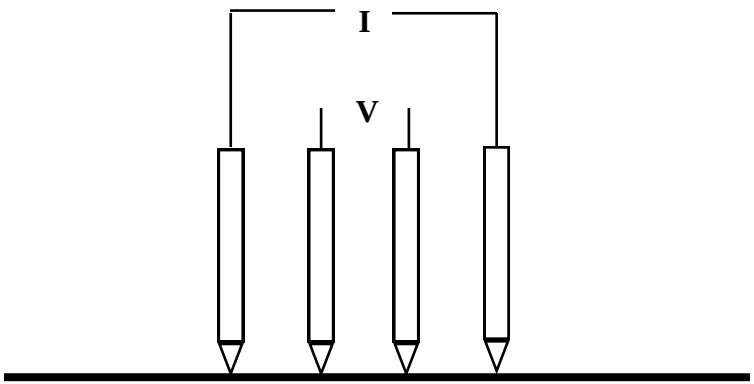
- **Bulk Resistivity -- Units -- Ω.cm**
- **Resistance -- V/I -- Units -- Ω**
- **Sheet Resistance -- Units -- Ω /Sq**

# Resistivity

- **Measured in Ω.cm**
- **Uniform through the substrate**
- **For Epi wafers two numbers**
  - **Substrate resistivity, usually very low i.e high doping**
  - **Layer resistivity**
- **Curves to convert resistivity to doping concentration**

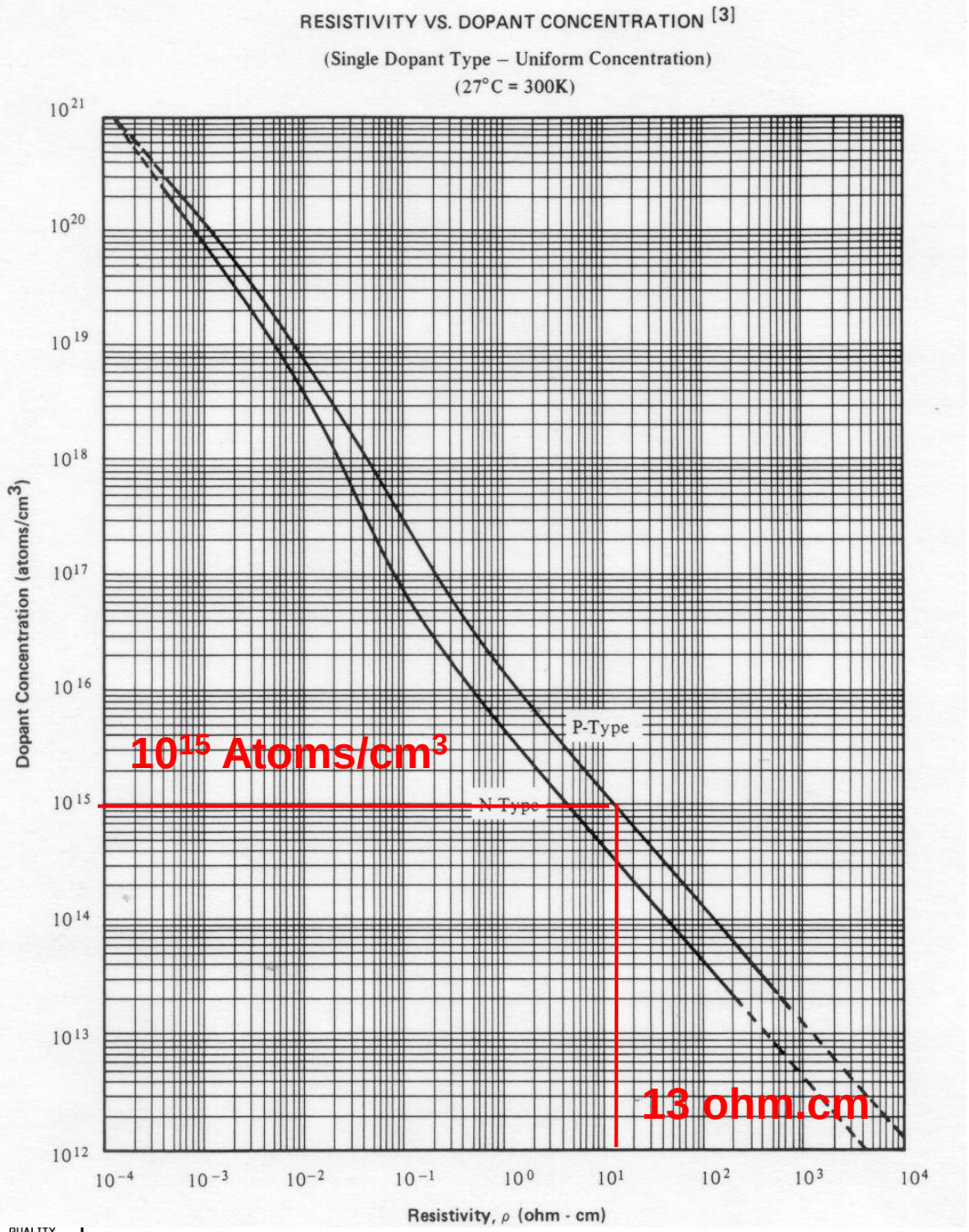
# 4 Point Probe

- **Force current between the outer probes**
- **Measure the voltage difference between the inner probes**
- **Rs = V/I X Geometric factor**
- **Geometric factor depends on a uniform probe spacing = 4.532**
- **Sheet Resistance = Rs = R X 4.532**




**4 Point Probe**

# Resistivity Vs Doping






Tyndall National Institute

# Type -- Dopant

- **For Example:**
  - **N/Sb**
  - **means N type doping with Antimony as the dopant material**

# Type -- Dopant

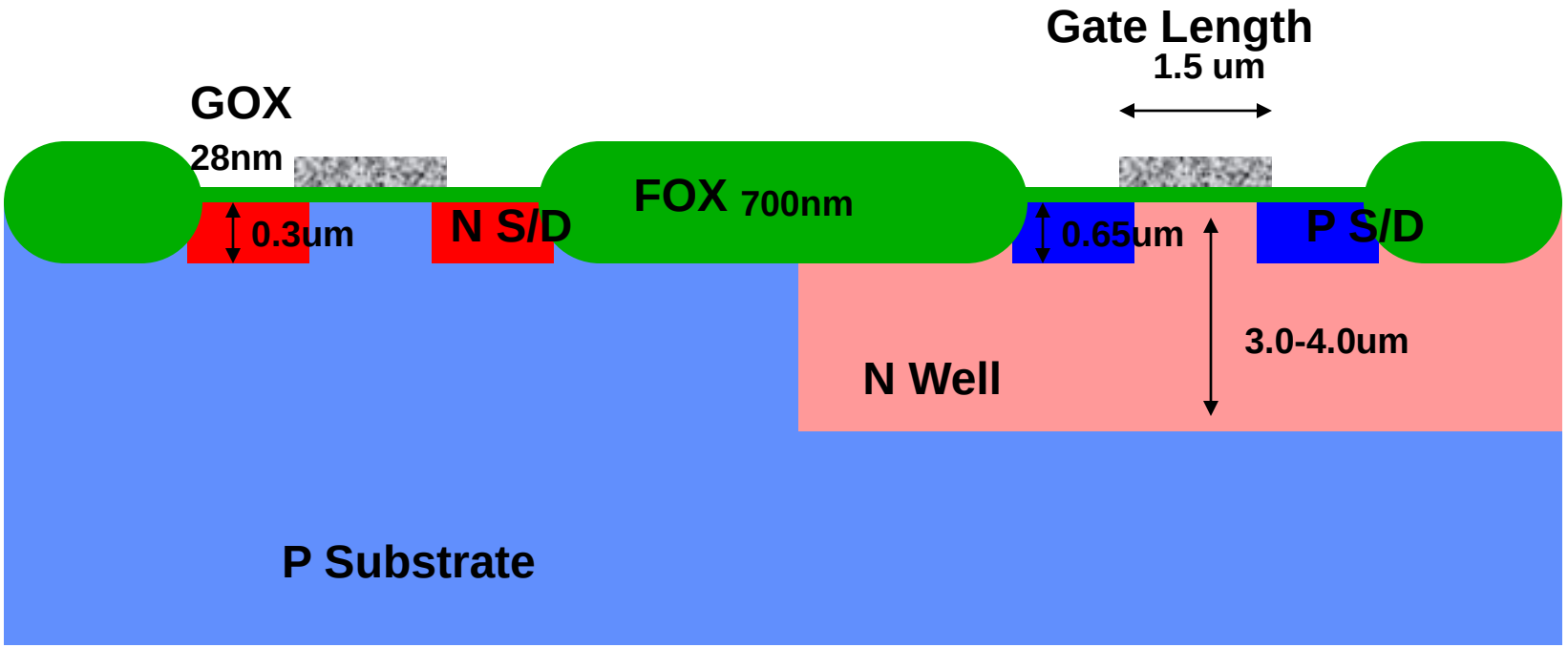
- **N/Ph**
- **means N type doping with phosphorus as the dopant material**
- **P/B**
- **means P type dopant with Boron as the dopant material**

# Dimensions

- **The industry (all industry) is gradually changing to the International System (SI) for measurement units**

- **Some older measurement units still linger on**

# 1.5µm Process Dimensions

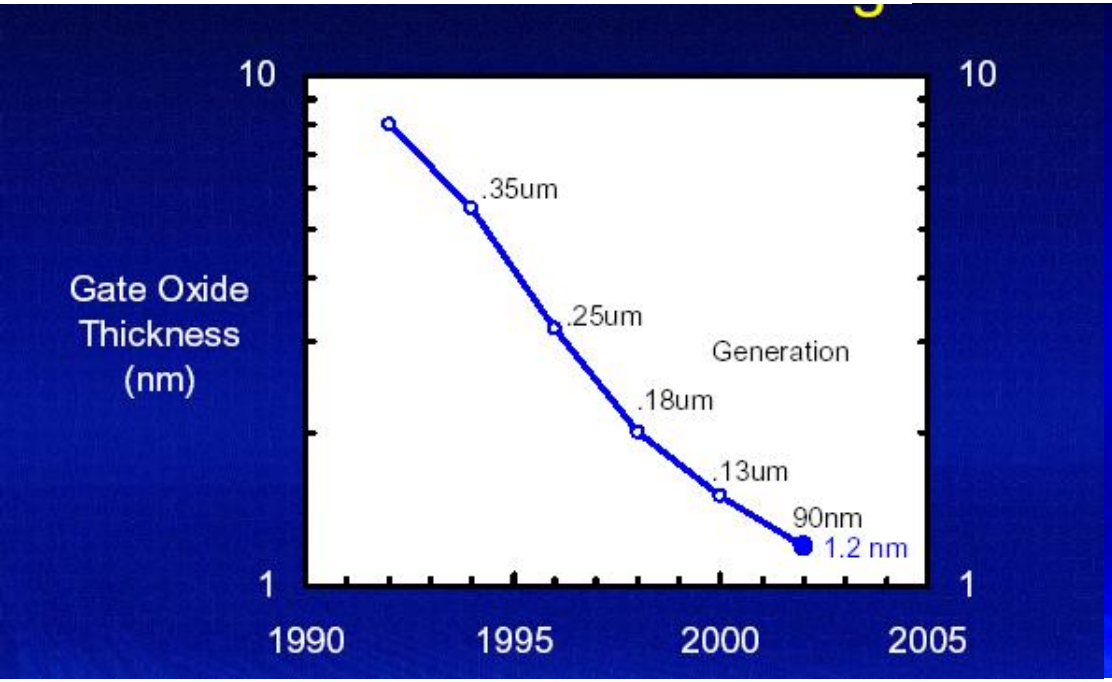


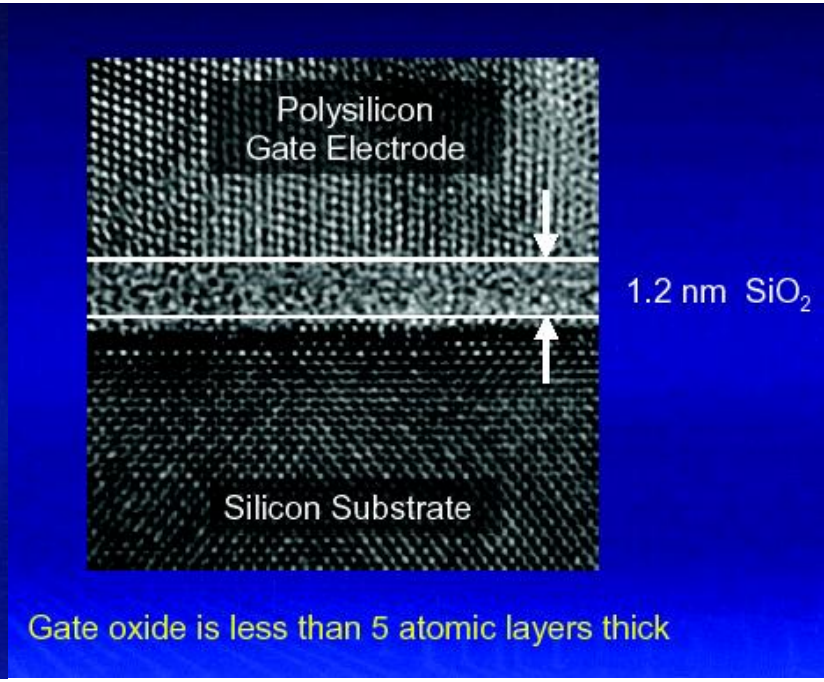
# Everything Scales Down

- Minimum Feature Size
- Film Thicknesses
- Junction Depths
- Power Supply Voltages

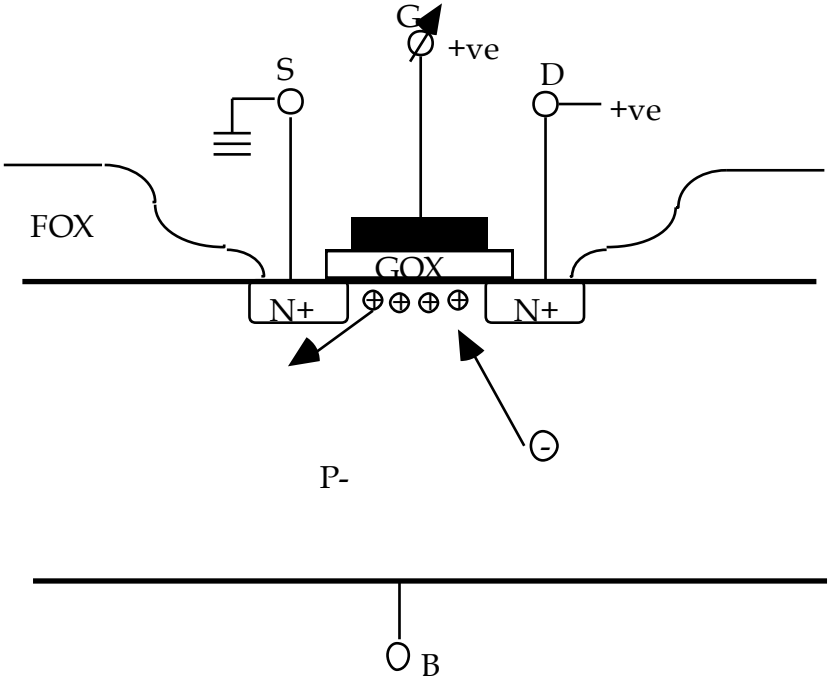
- 90nm Process
- 1.2nm Gate “Oxide
- Junction Depth
- 1.2V Power Supply

# Intel Gate Oxide Scaling



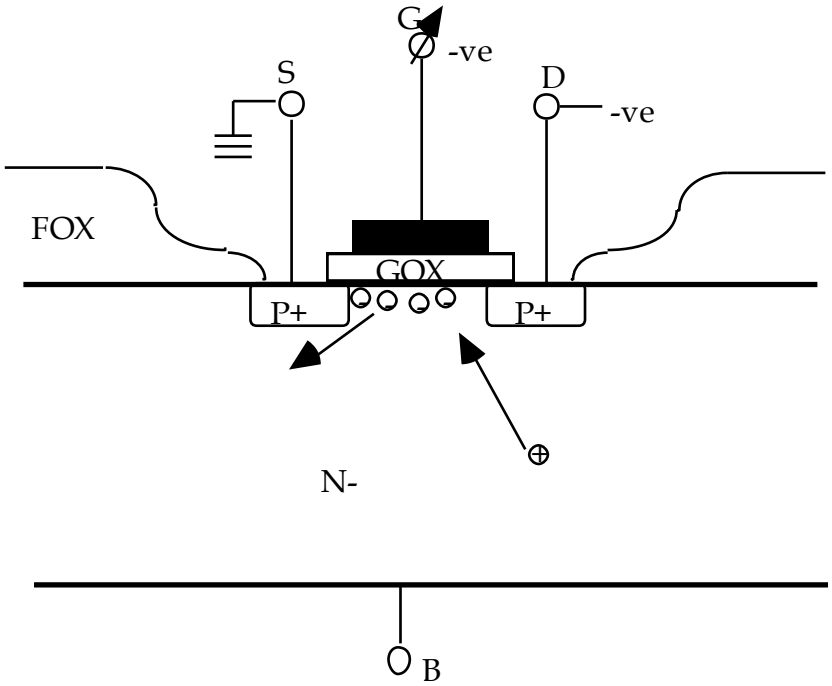



# N-MOS Device



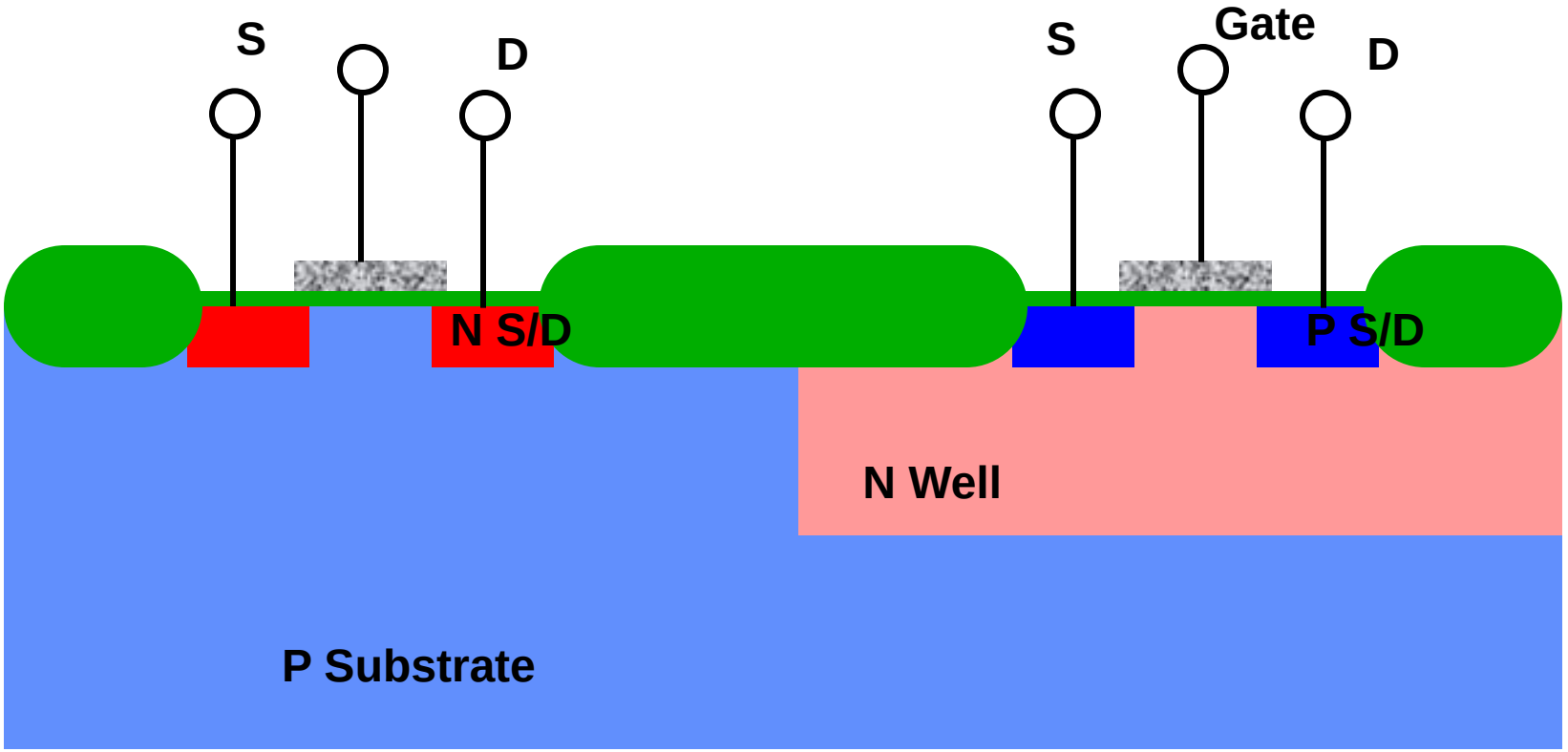

**N-Channel Enhancement Mode Device**

# P-MOS Device

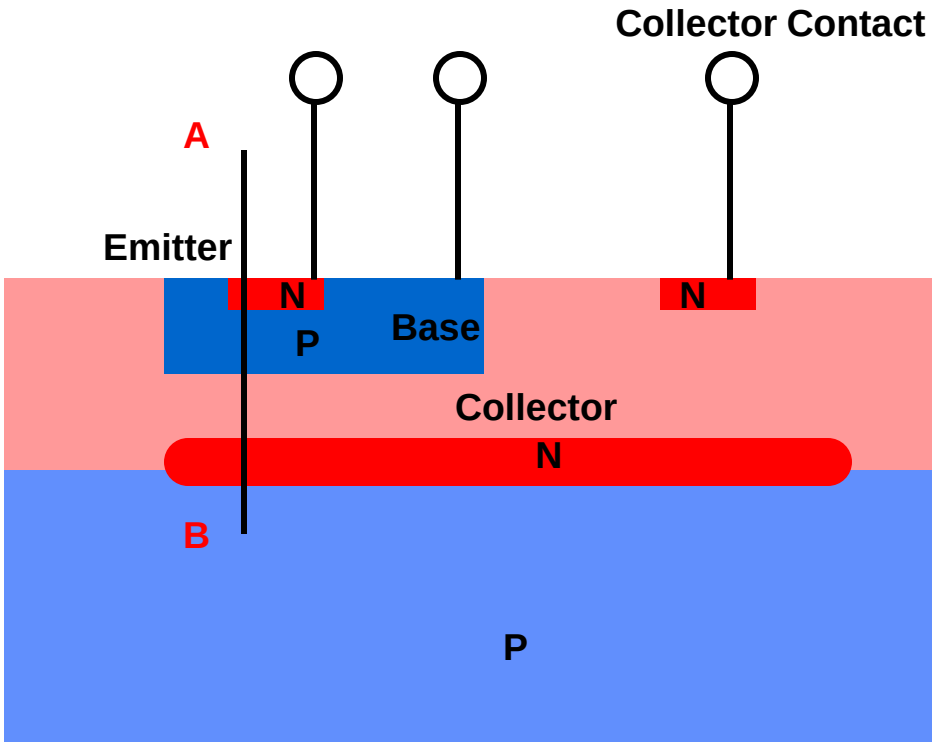


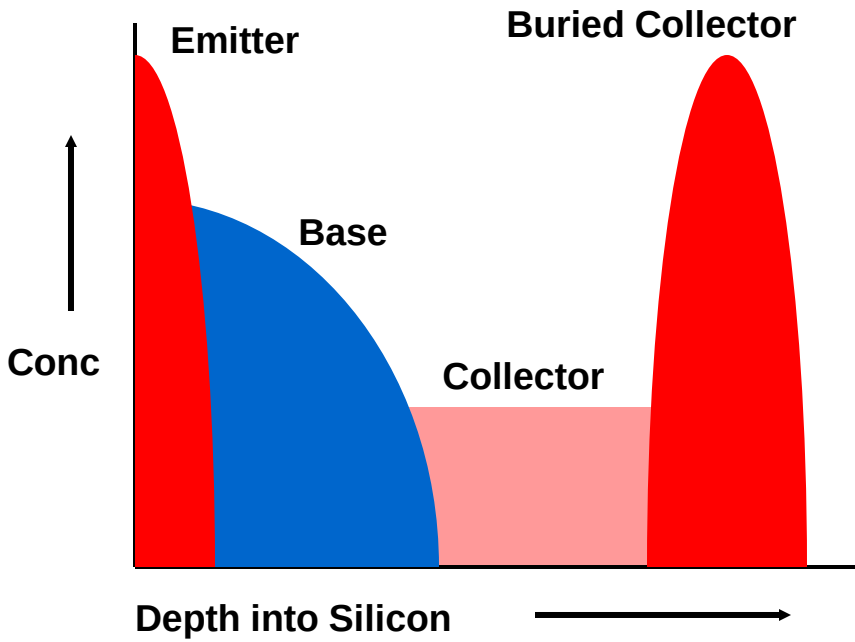

**P-Channel Enhancement Mode Device**

# C-MOS Devices

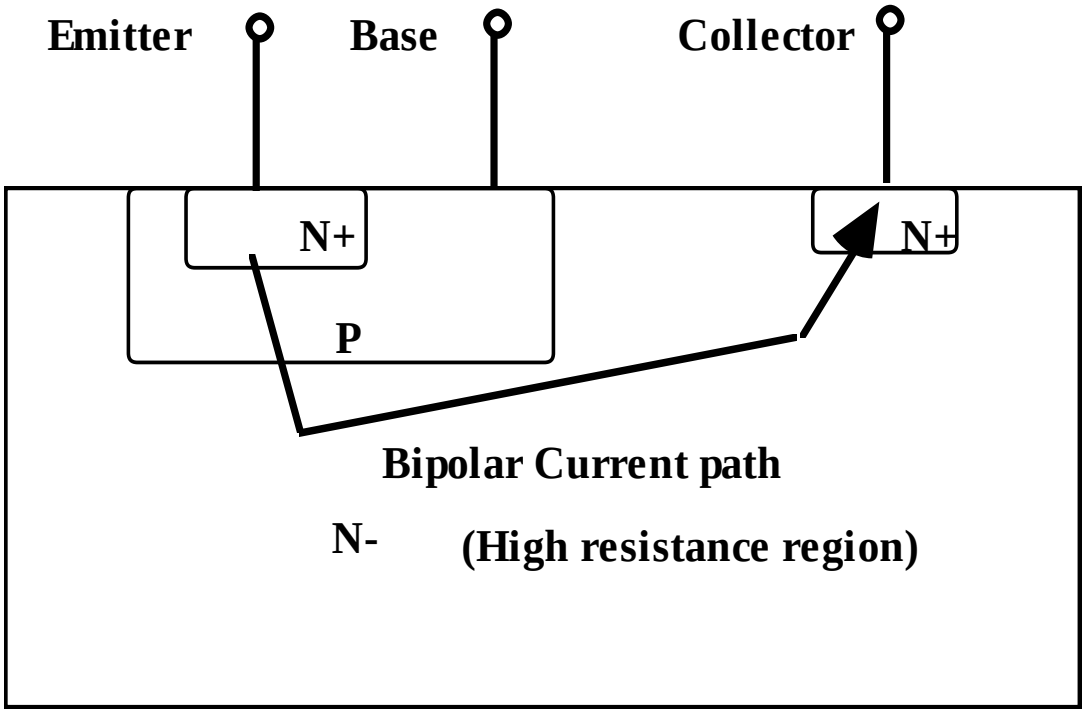


# Bipolar Transistor



# Bipolar Current Path



**Information Only**

# Seven Base Units of SI

| Quantity | Unit Name | Symbol |
|---|---|---|
| Length | Metre | m |
| Mass | Kilogram | kg |
| Time | Second | s |
| Electric Current | Ampere | A |
| Temperature | Kelvin | K |
| Luminous Intensity | Candela | cd |
| Amount of Substance | Mole | mol |

# SI Derived Units with Special Names

- **Frequency - Hertz**
- **Force - Newton**
- **Pressure - Pascal**
- **Energy - joule**
- **Power -Watt**

# SI Derived Units with Special Names II

- **Electric Charge -Coulomb C**
- **Electric Potential -Volt V**
- **Electric Capacitance -Farad F**
- **Electric Resistance -Ohm Ω**
- **Electric Conductance-Siemens S**

# Prefered SI Prefixes

| | Factors by which unit is multiplied | Prefix name | Symbol |
|---|---|---|---|
| Multiples | $10^{12}$ | Terra | T |
| | $10^{9}$ | Giga | G |
| | $10^{6}$ | Mega | M |
| | $10^{3}$ | Kilo | k |
| Submultiples | $10^{-3}$ | Milli | m |
| | $10^{-6}$ | Micro | ? |
| | $10^{-9}$ | Nano | n |
| | $10^{-12}$ | Pico | p |
| | $10^{-15}$ | Femto | f |
| | $10^{-18}$ | Atto | a |

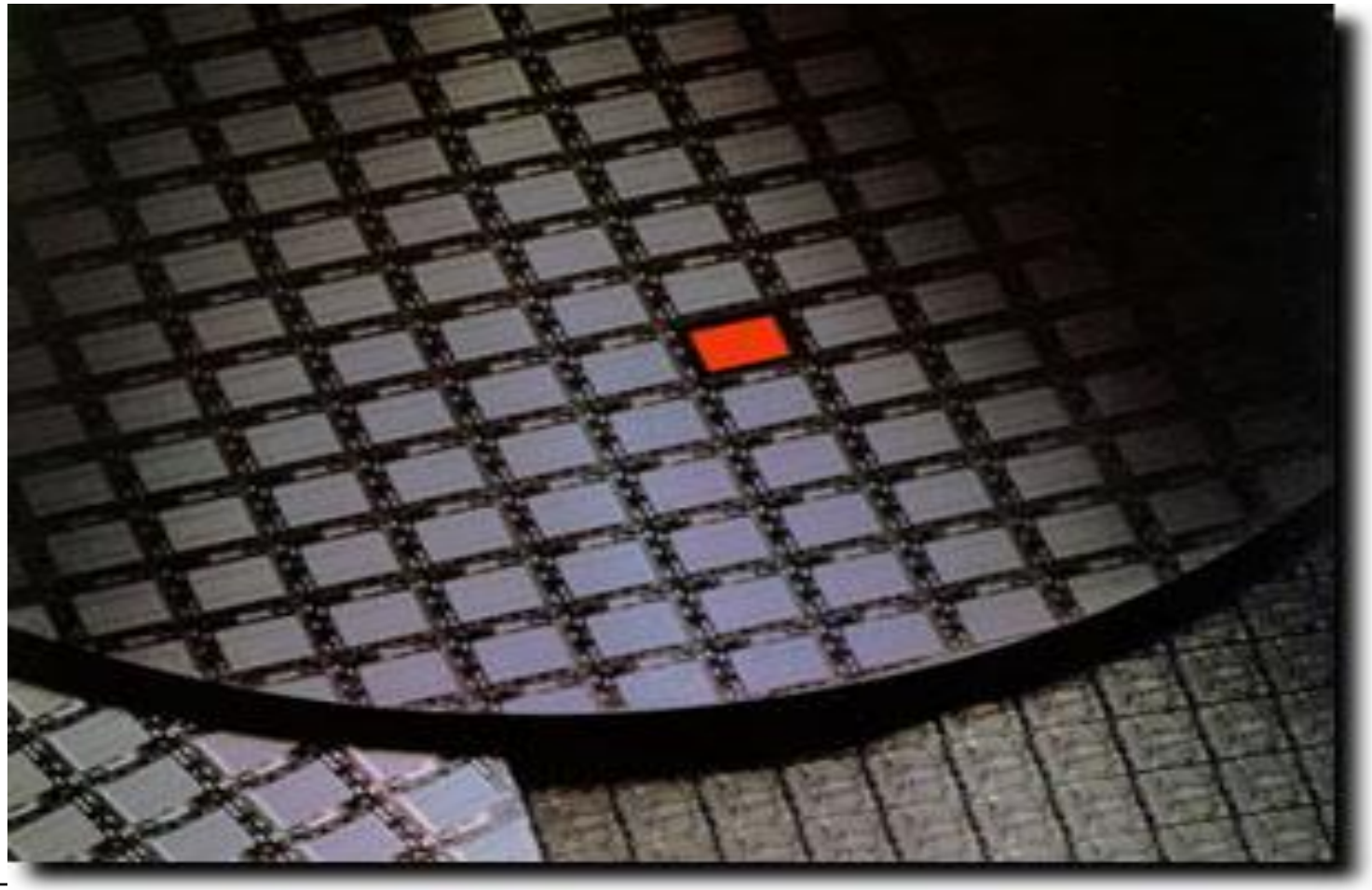
# Non-SI Units which are used

- **Litre, cc,**
- **Tonne**
- **Minutes, hour**
- **Degree celcius**

# Obsolete Units Still Technically Correct

- **Angstrom Å 1Å=0.1nm**
- **Micron µ 1µ=1µm**
- **Bar bar 1bar=100kPa**
- **Torr torr 1Torr=133.322Pa**
- **Revolutions per minute rpm 1rpm=16.666mHz**

# Finished Wafer



# Die Lead Frame Attachment

Die Lead Frame Attachment
(Ablestik)

# Wire Bonding

Wire Bonding
(Kaijo Corporation)

# Terms 1

- **Acceptor**
  - **Impurity that make silicon P-type**
- **Anode**
  - **positive terminal in a device**
- **Backside Damage**
  - **intentional damage to the non-processed side of a wafer, this damage draws impurities away from the front surface or acts as a “getter”**

# Terms 1

- **Bipolar Transistor**
  - **transistor consisting of 2 PN junctions, with 3 terminals emitter, base and collector**

- **Burn-**
  - **in elevated temperature stressing of a device to identify and remove early failures**

# Terms 2

- **CMOS**
  - **Complementary Metal Oxide Semiconductor process -- has PMOS and NMOS devices on the came substrate**

- **Capacitance**
  - **A measure of the amount of charge a device can store between two conductors measured in Farads**

# Terms 3

- **Carriers**
  - **Electrons or holes that are available for conduction of current**
- **Cathode**
  - **Negative terminal of a device**
- **Channel**
  - **the conducting region of a MOS device**
- **Chip**
  - **also called a die**

# Terms 4

- **Contact**
  - **region of exposed silicon covered by metal to provide electrical access to the device**
- **CVD**
  - **Chemical Vapour Deposition**
- **DIP**
  - **Dual In-Line Package  Package with two vertical rows of leads**

# Terms 5

- **Enhancement Mode**
  - **A MOS transistor that is normally off**
- **Extrinsic**
  - **A semiconductor when dopants are introduced**
- **FET**
  - **Field Effect Transistor**

# Terms 6

- **Getter**
  - **A process by which un-wanted impurities are trapped in an in active region**
- **Ion**
  - **An atom that has either gained or lost electrons**
- **Junction**
  - **The interface between two semiconductor regions of opposite carrier type**

# Terms 7

- **LSI -- large Scale Integration**
  - **IC that contains more than1000 gates on a single chip**
- **MOSFET**
  - **Metal Oxide Semiconductor FET**
- **Miller Capacitance**
  - **Capacitance caused by gate overlap of the source/drain regions**

# Terms 8

- **Silicon**
  - **14th element of the periodic table used as the substrate in IC production**
- **N-Type**
  - **Silicon doped with Phos, Arsenic etc**
- **P-Type**
  - **Silicon doped with boron**

# Terms 9

- **Oxidation**
  - **The growth of silicon dioxide on the silicon surface**
- **Oxide Breakdown**
  - **Conduction caused by a voltage which exceeds the dielectric strength of the oxide - usually irreversible**

# Terms 10

- **Polycrystalline Silicon**
  - **A layer of deposited silicon made up of multiples of small crystal structures**
- **Primary Flat**
  - **The longest flat on the wafer parallel to the <110> plane**

# Terms 11

- **Qf**
  - **Fixed charge**
- **Qm**
  - **Mobile charge**
- **Qit**
  - **Interface trapped charge**