Tutorial and Instruction Manual:

Using PSpice in Teaching of Power Electronics

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Goals

1. Overview of how to use PSpice, i.e. the basics of navigating PSpice.

2. Show how PSpice can be used for simulating power electronic circuits, both in the time and frequency domains.

3. Illustrate examples of simulations of several basic converter circuits .

4. Provide a basic library of power electronic circuits and components which users can refine and expand for their own particular needs.

5. Stimulate discussion and sharing of ideas on using simulation as an educational tool.

Outline

* **Introduction**
  * **Overview of the simulation process.**
  * **Unique aspects of simulating power electronics**
* **Pspice basics/navigation**
  * **Loading and configuring Pspice**
  * **Circuit entry, running simulations, and viewing results**
* **Build it yourself guided exercise - switching circuit implementation of buck converter**
  * **Inclusion of detailed MOSFET and diode models**
  * **Realistic simulation of individual switchings and inclusion of other circuit parasitics**
* **Use of Probe capabilities**
* **Use of average circuit models**
  * **Example of buck converter in CCM and DCM**
  * **Converter transfer function (V_o/D) frequency response - buck converter example**
* **Closed loop control of converter output - buck converter with voltage mode control**
  * **Simulation results compared with experimental results from PowerPole lab board**
* **Diode rectification - waveforms, Fourier components, THD**
* **DC to AC inversion - example of single phase full-bridge inverter**
* **Conclusions**

Overview of Simulation Process

* Simulation is a three-step process
  * Input the circuit topology - done with Schematics
  * Setting up simulation and running it
    * Set component values
    * Set simulation parameters - simulation type (transient, etc) and range (time duration, etc).
    * Run simulation - done in Schematics with automatic transfer to Pspice.
  * Examine results in Probe - numerous ways to view results

* Power electronic circuit simulations have two widely disparate time scales
  * Long time scale (hundreds of switching cycles) to see steady-state converter operation
  * Short time scale (one or two switching cycles) to see details of individual switchings
  * Keeping overall simulation times reasonable requires special considerations.

* Inadequate component models for accurate simulation of individual switchings
  * Built-in diode, MOSFET, and BJT models only accurate for logic level circuits
  * User must generate (or obtain from vendors) accurate equivalent circuits for inductors, capacitors, transformers, and semiconductor components.

Why PSpice for Power Electronics Simulation

* Evaluation version free and powerful enough for most power electronics simulations in educational settings.

* Most students have basic familiarity with Pspice from other undergraduate courses. Many have it on their own computers.

* Accurate models for power semiconductor devices available from several manufacturers.
  * Built-in model for IGBT

* Automatic linearization of large signal circuits about a dc operating point.
  * Not necessary to provide small signal equivalent circuit for frequency response simulations.

* Powerful graphics-based post processor (Probe) for viewing simulation results.
  * Extensive macro and mathematical capability for viewing derived results (power dissipation, efficiency, etc.)

* Intuitive schematic entry for construction of circuits.

* Ability to add user-generated models or components to component libraries.

Pspice Installation and Basics of Pspice Navigation

Loading and Configuring of PSpice

* Two separate procedures (automated and manual) for loading and configuring of PSpice

* Automated procedure uses two install programs which are specifically designed for those computers which do not have Pspice.
    * First install program (provided by OrCAD/Cadence) installs Pspice 9.1
    * Second install program (provided by U. of MN) loads power electronic libraries and tutorial circuits and configures the libraries by loading a specific configuration (INI) file.
        * Any existing configuration (INI) file will be overwritten and thus lost.

* Use manual configuration of Pspice if you already have Pspice on your computer. This will avoid the overwriting of your present configuration (INI) file and thus the links to libraries etc. which you have developed.

Automated Loading and Configuration of Pspice

1. Installation of Pspice

   * Activate Setup file for installing Psice. Setup located in the Install Pspice folder on tutorial CD.

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   * When Select Schematic Editor window opens, select Schematics and deselect Capture.

   * Use default selections when other windows request choices during the installation process.

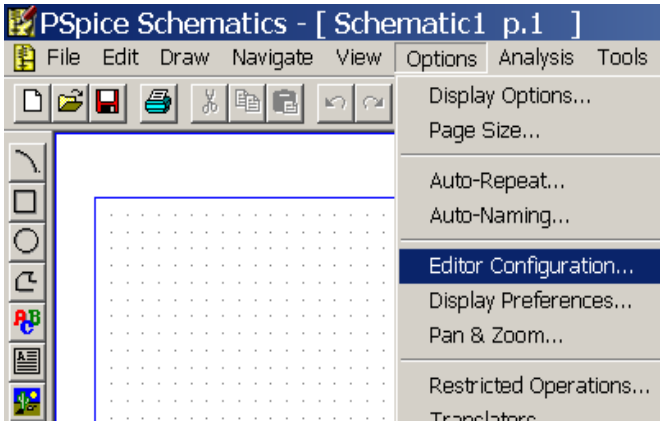
2. Loading and configuring libraries.

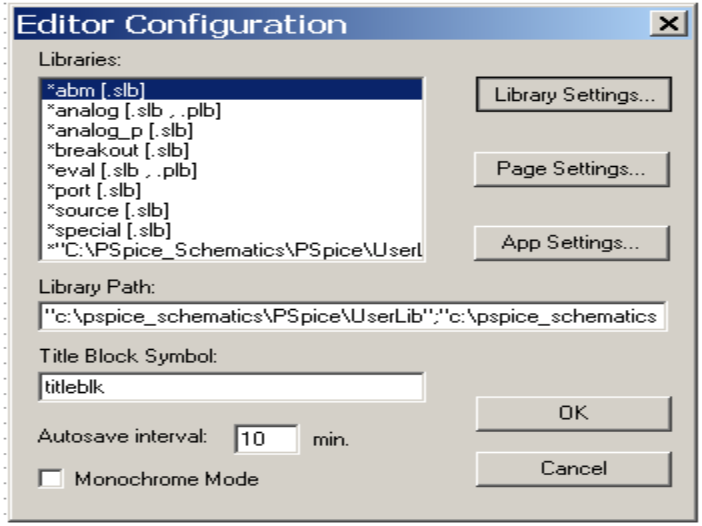
   * Activate Setup file for ConfigurePspicePwrE.

   * Located in Install Pspice folder (on tutorial CD) in subfolder entitled ConfigurePspicePwrE.

Manual Configuration of Pspice

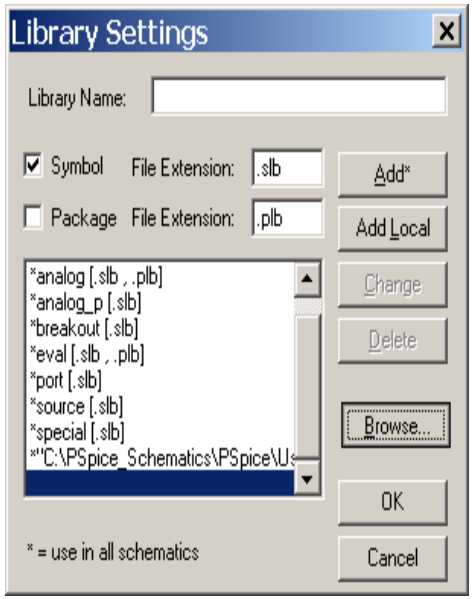
1. Manual loading and configuration of library files assumes that you already have Pspice installed on your computer and that your have some libraries that you have developed and configured that you want to remain linked to Pspice.
2. Copy Pspice Tutorial Circuits folder on CD into the OrCAD_Demo folder on Drive C: Path name: C:\Program files\Orcad_Demo
3. One time setup of power electronics Symbol library (PE_lib1) using files on workshop-supplied CD
   * Open folder Move to PSpice Userlib located in Pspice folder on CD. Select contents of Move to Pspice Userlib folder and copy these contents to the Userlib folder located in the Pspice folder on Drive C. Path name: C:\Program files\OrCAD_Demo\Pspice\Userlib
   * Launch Schematics and open a new page using New in the File menu.
   * In the Options menu, select Editor Configuration. When Editor Configuration window opens, select Library Settings button.

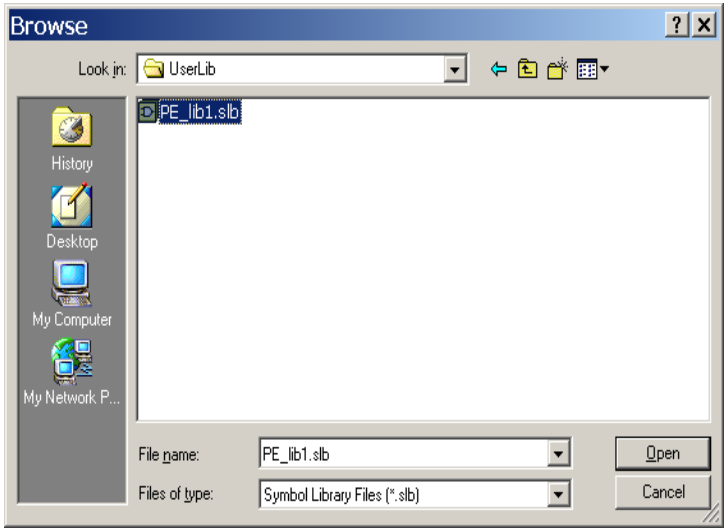


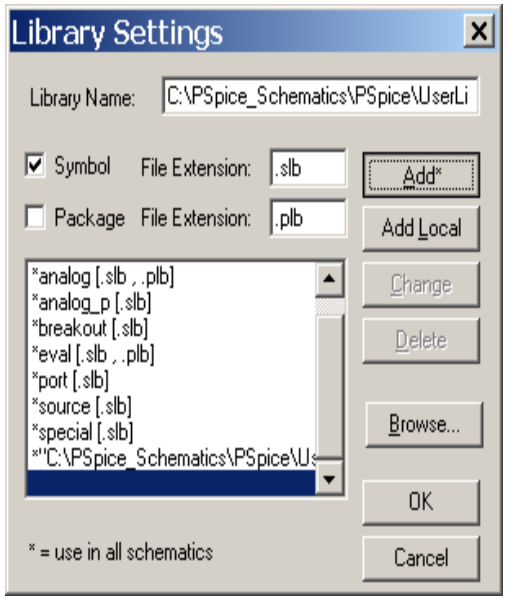


Manual Installation of Pspice (cont.)

* In Library Settings window, select the Browse button. In the Browse window, open the folder in the Userlib folder (C:\Program files\OrCAD_Demo\Pspice\Userlib) and open PE_lib1. Browse window will close.
* In Library Settings window, the path name to PE_lib1 will appear in the Library Name bar. Select Add* to add PE_lib1 to the list of configured libraries. Then click OK to close Library Setting window.
* Click OK in the Editor Configuration window to close it.



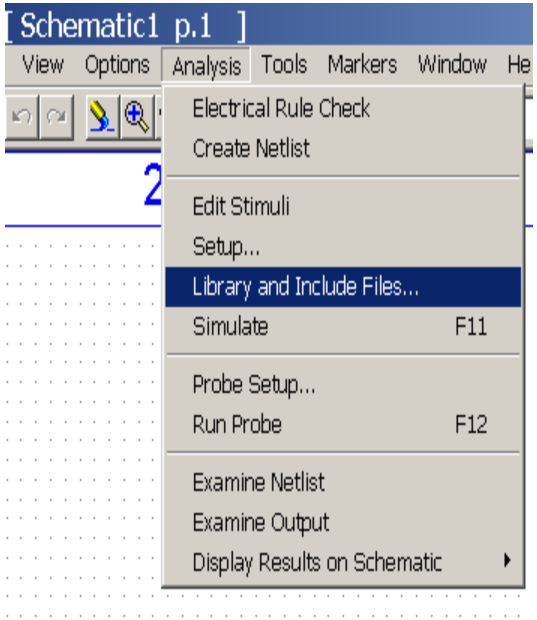


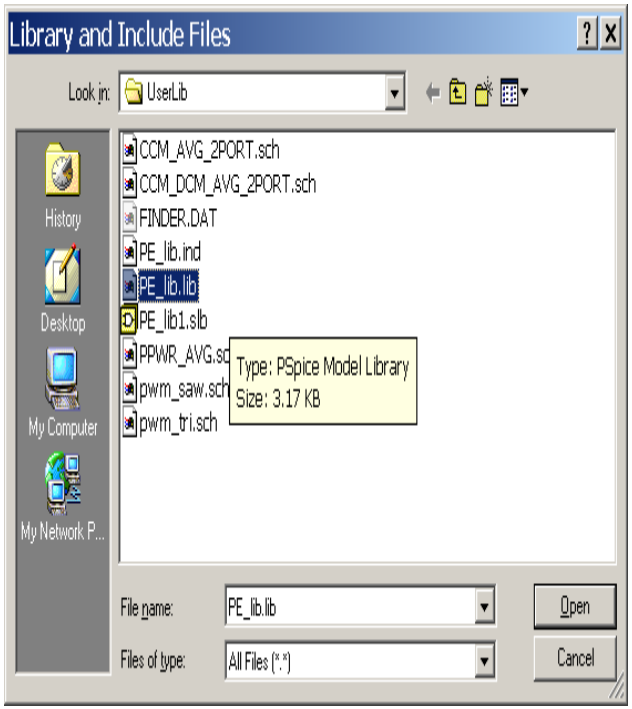


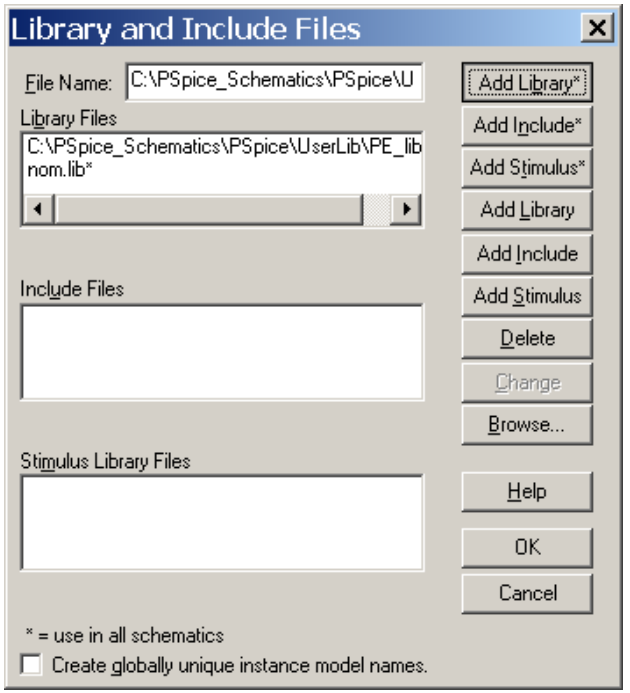
Manual Installation of Pspice (cont.)

4. Configure model library (which contains diode MUR2020 and MOSFET IRF640) PE_lib.lib
   * In Schematics, activate Options pull-down menu and choose Library and Include Files button.
   * In Library and Include Files window, select Browse button.
   * In Browse window, navigate to Userlib folder, and select PE_lib.lib and open it. Be sure to select All Files in Files of type: select slot as shown in figure below. Browse window closes and returns control to Library and Include Files window.
   * In Library and Include Files window, select Add Library*. Then click OK to exit window.

5. Customization is complete.





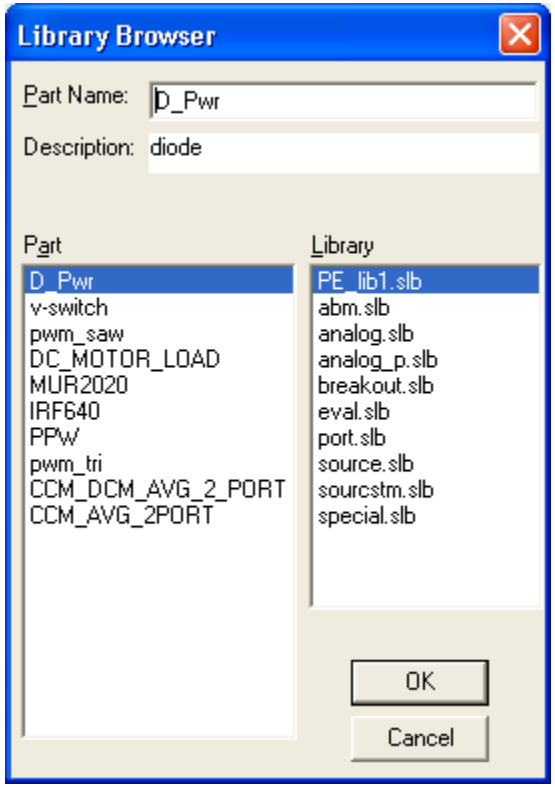


Contents of Pspice Tutorial Circuits

* **BuckConv_Sw_Model** - Buck converter implemented with a voltage-controlled switch. Intended for transient analysis to show ideal converter waveforms.
* **Buck_MOSFET** - Buck converter implemented with vendor-supplied MOSFET and diode models. Intended for transient analysis to show both basic converter waveforms and details of individual switchings of the MOSFET and diode.
* **Buck_Conv_Avg -** Buck converter utilizing average model of the powerpole. Intended for transient analysis to show effects of step load change.
* **Buck_Freq_Response** - Similar to Buck_Conv_Avg except that the circuit also has an ac source to provide a sinusoidal variation to the duty cycle. Intended for swept ac analysis to shown the transfer function versus frequency between the output voltage and the input duty cycle.
* **Buck_conv_avg_fb_ctrl** - Average model of a buck converter with voltage mode feedback control. Intended for transient analysis to show converter response to a step load change.
* **Buck-conv-sw-fb_ctrl** - Buck converter implemented with ideal voltage-controlled switch and voltage mode feedback control. Intended for transient analysis to show response to step load change.
* **DBrdg_Rect** - Full bridge single phase diode rectifier. Intended for transient analysis to show voltage and current waveforms as source inductance is changed and calculation of harmonic components and total harmonic distortion.
* **Inverter_1PH_BP** - Single phase inverter with bipolar switching. Intended for transient analysis showing sinusoidal output current.

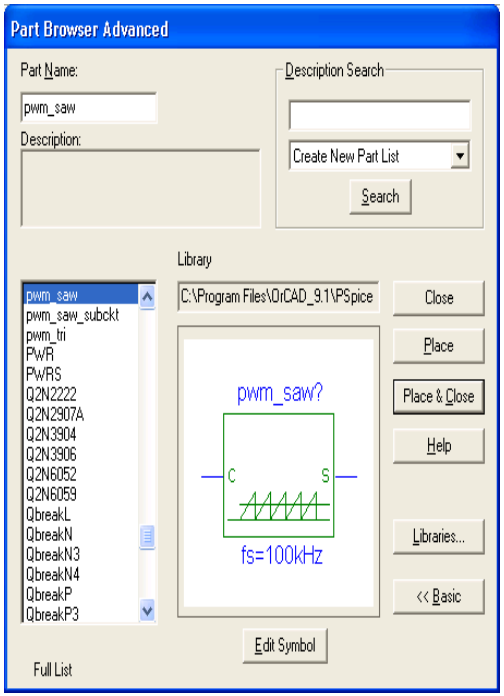
Power Electronic Components in U of M-supplied Libraries

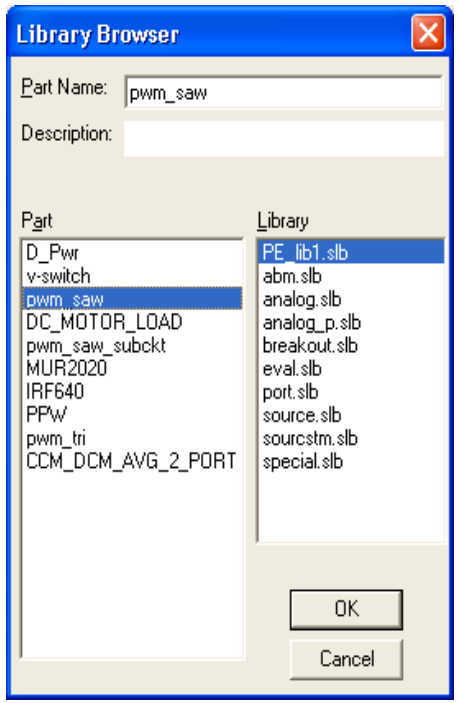
* Specially developed parts for power electronic simulations.
* D_Pwr - diode with 0.001 ohm series resistance.
* V-switch - voltage controlled switch with 0.001ohm series resistance.
* pwm_saw - produces pulse-width modulated unipolar pulse train by comparing input dc voltage against a sawtooth wave. User supplies dc voltage proportional to duty cycle and the sawtooth (switching) frequency.
* MUR2002 (power MOSFET) and IRF640 (power diode) - detailed vendor-developed models of these two components which are on the PowerPole laboratory circuit board.
* PPW - average model of the powerpole valid in both DCM and CCM.
* pwm_tri - same function as pwm_saw except a triangular wave is used instead of a sawtooth. Used for inverter circuits.
* CCM_DCM_AVG_2_PORT - alternative formulation of average model of a powerpole. Use in place of PPW if PPW gives convergence problems.
* CCM_AVG_2PORT - average model of a powerpole valid only in CCM. Simpler model than PPW or CCM_DCM_AVG_2_PORT.

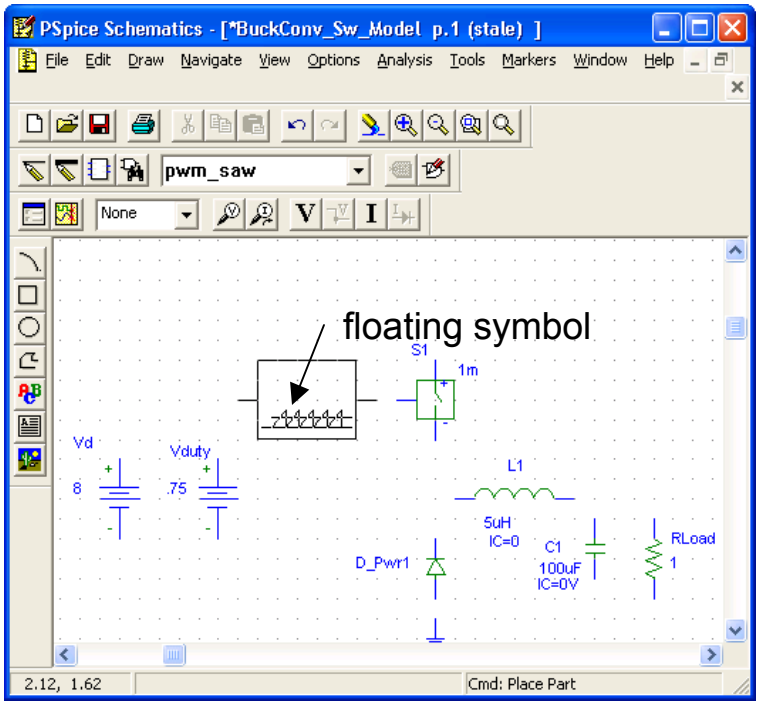


PSpice Navigation: Selecting and Placing Components

* Open a new page or stored file in Schematics. Open Parts Browser window by either selecting the Get New Part button on the Toolbar or by selecting Get New Part in the Draw pull-down menu.
* Shorten Full List by selecting Libraries button in Parts Browser window and selecting desired library in Library Browser window. Click OK button in Library Browser to return to Parts Browser
* Go to Schematics. Move floating component symbol (moves with selection arrow) to desired location on Schematic page and place component on page with a mouse click.
* Continue parts selection/placement until Schematic page has all components needed for circuit.







PSpice-Supplied Component Libraries

* Initial Pspice installation has component library divided into nine parts libraries to simplify finding a particular part.
    * User can add or remove libraries as desired.
    * Maximum of 10 configured (addressable) libraries at a given time in student version.

* Pspice-supplied library contents

    * abm.slb - analog behavior models. Voltage and current sources whose outputs can be controlled by mathematical expressions or tabular data and a Laplace transform block.

    * analog.slb - analog components. Passive components (R, L, C), coupled inductors, and dependent voltage and current sources.

    * analog_p.slb - passive components (R,L,C) with parameterized values.

    * breakout.slb - contains a number of components, passive and active, in a simplified generic or default configuration. Useful for circuits when detailed models, esp. for active devices, not available.

PSpice-Supplied Component Libraries (cont.)

* eval.slb - selection of detailed models (sometimes vendor developed) for specific devices (mostly semiconductor) , e.g. uA741 op amp, IRF150 power MOSFET, etc.

* port.slb - contains a number of different ports and pins for specifying node connections without having to have a directly drawn wire connection. Includes ground connection or symbol.

* source.slb - contains variety of independent current and voltage source models. Different models of a voltage (current) source used depending on type of analysis, e.g. ac sweep, transient analysis, etc.

* sourcstm.slb - specialized models of voltage and current source to be used with Edit Stimulus command in Analysis menu.

* special.slb - contains specialized parts, the most important of which is PARAM (short for Parameters) which is needed for making stepped (parameterized) simulations.

* Recommend removing sourcstm.slb and analog_p.slb libraries if needed to make room for other libraries. We have not used these two libraries.

Connecting Components to Form a Circuit

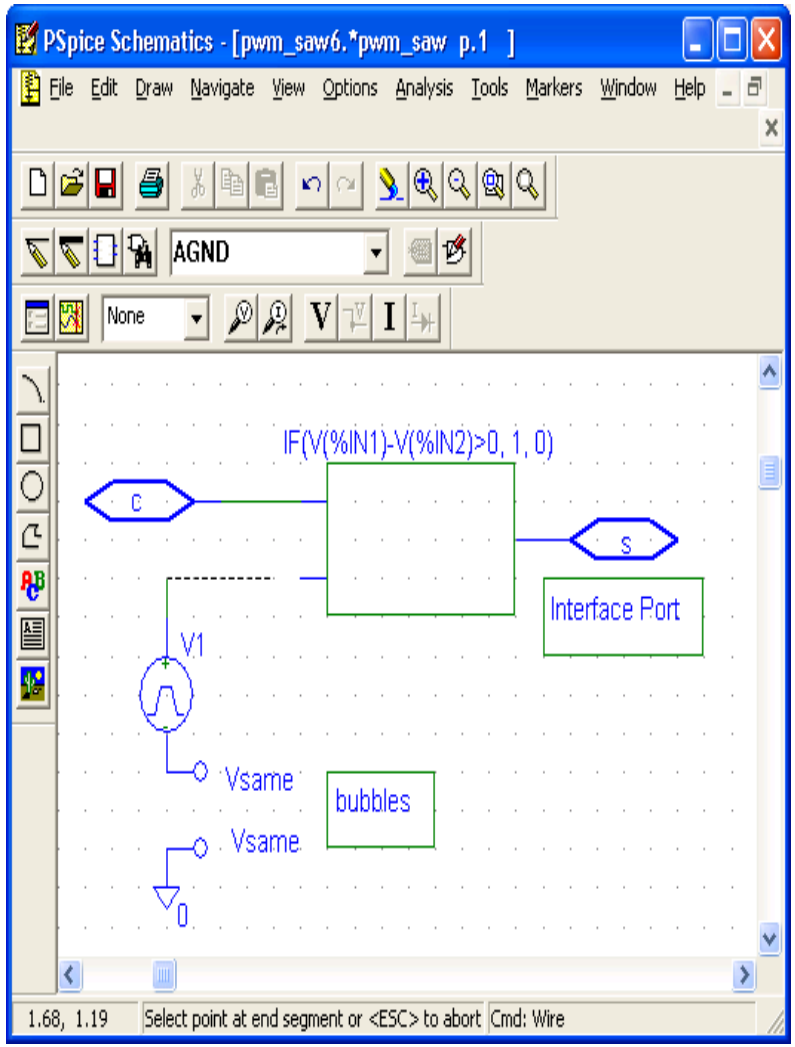
* Connect components using wire tool. Select the Draw Wire button (pencil icon) on Toolbar or select from the Draw pull-down menu.

* Wires can cross each other without being shorted together. Connection of crossed wires indicated by dot at wire intersection.

* Select analog ground (AGND) from port.slb library for the circuit ground.

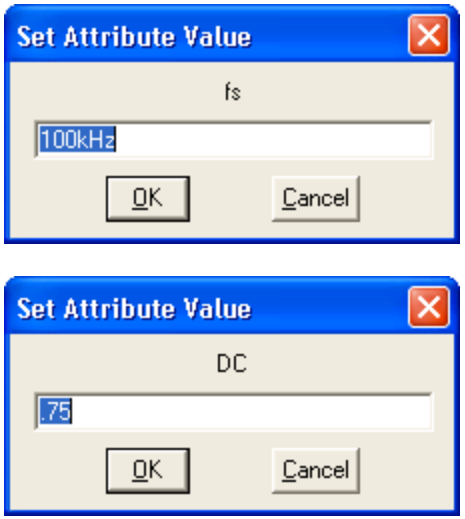
* Use bubbles (found in port.slb library) to connect together nodes without drawing a direct wire connection. Bubbles must have same name in order to be connected together.

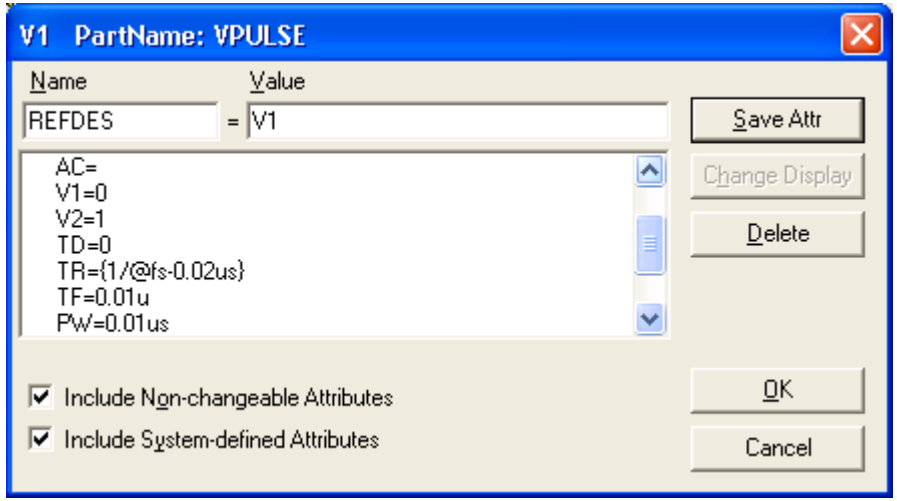
* Use Interface port (port.slb library) to make off-page connections to a circuit on another page (hierarchical circuit).



Specifying Component Values

* Set component values (resistor values, frequency f_s for PWM modulator, dc voltage source, etc.) by one of two methods.
* Open Set Attribute Value window by double clicking on printed value on schematic or selecting the attribute and then clicking on Attrributes in Edit pull-down menu. Best for setting just one or two values per component.
* Open dialog box listing all the attributes of a component by selecting the entire component and either double click on component or click on Attributes in Edit pull-down menu. Best for components which have multiple entries such as Vpulse.





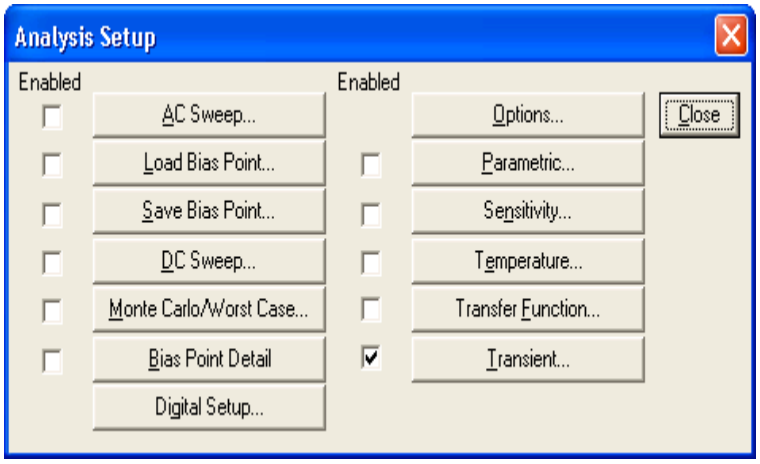
Setting Up Simulation Parameters

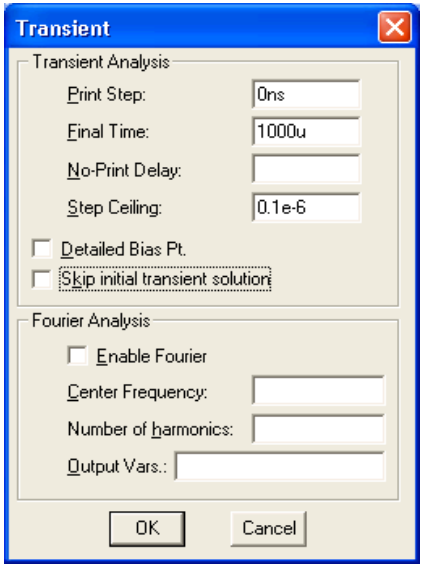
* Specify simulation parameters in Analysis Setup dialog box. Box opened by selecting the Analysis Setup button on toolbar or selecting Analysis Setup on Analysis pull-down menu.

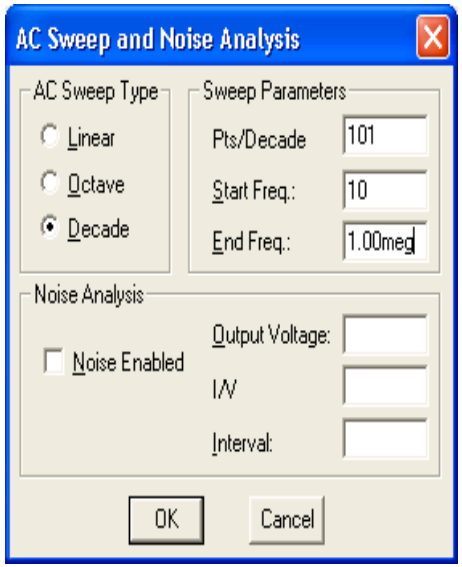
* Several different types of analysis can be done, including parameterized. Types shown in Analysis Setup figure shown below.

* Enter power-of-ten using either scientific notation 1eX where X is the positive or negative exponent or using suffix letters shown below. Pspice is case-insensitive.

  f = 1e-15 ; p = 1e-12 ; n = 1e-9 ; u = 1e-6 ; m = 1e-3 ; k = 1e3 ; meg = 1e6 ; g = 1e9 ; t = 1e12



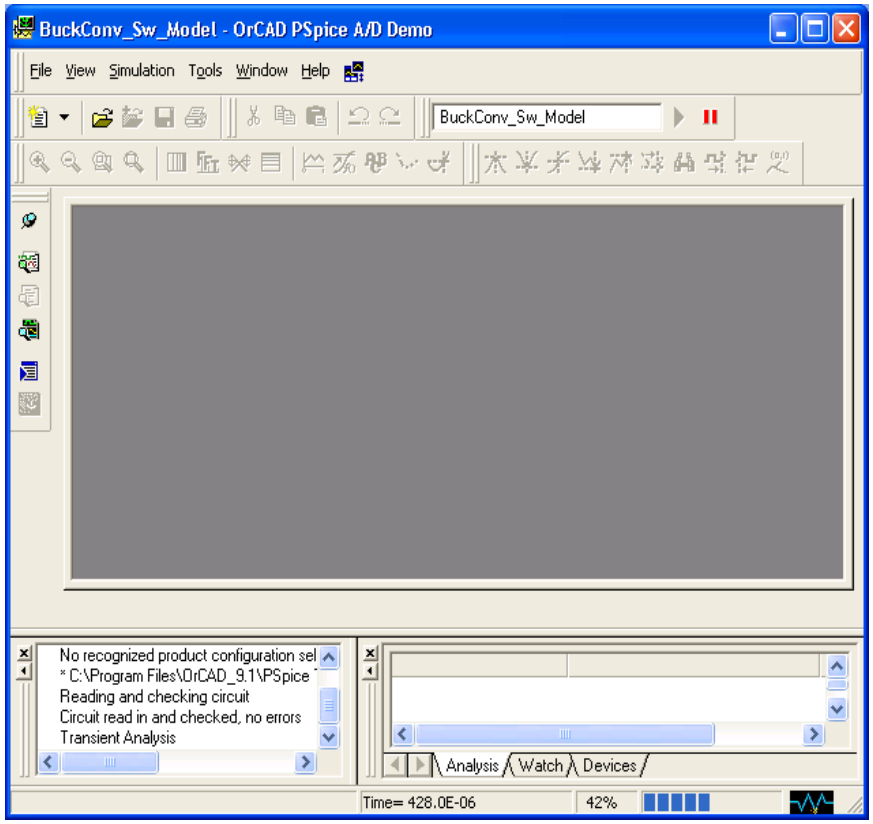




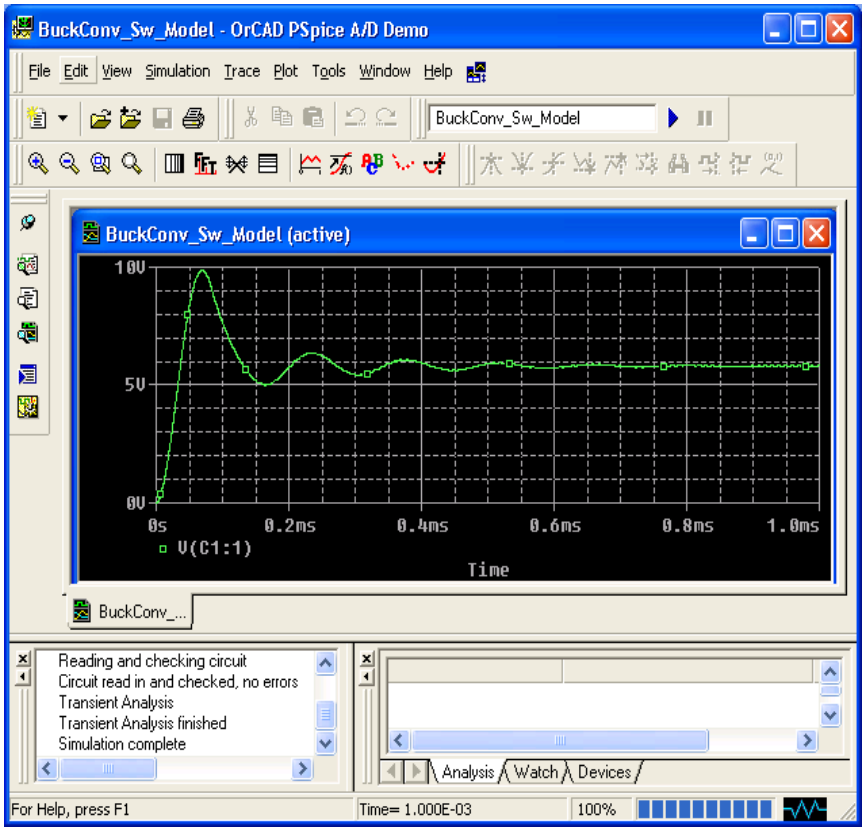
Running the Simulation

* Simulation started by selecting the Simulate button on the Schematic toolbar or selecting Simulate in the Analysis pull-down menu.
* Window shown below opens which indicates status of simulation and the percent completion. Simulation runs automatically to completion or until an error is encountered.

Simulation in progress



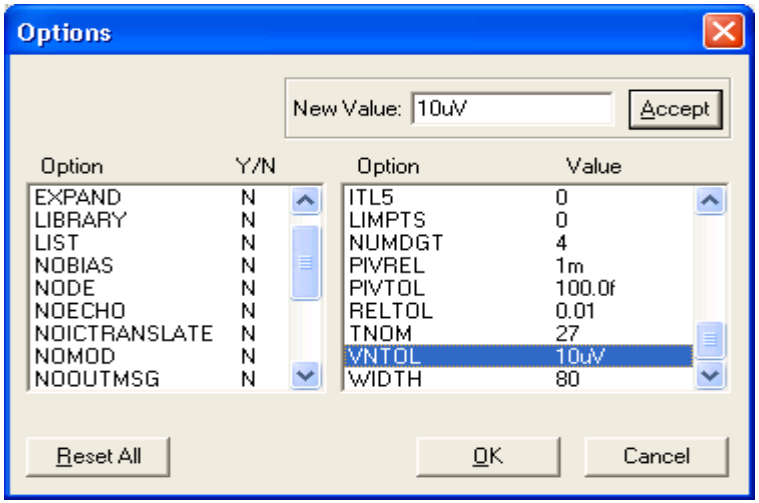
Simulation completed



Convergence Problems and Suggested Solutions

Increase Error Tolerances

* Open Options dialog box by selecting Options in Analysis Setup dialog box.
* Suggested error tolerance settings for power electronics simulations.
  * ABSTOL to 1u
  * GMIN to 1u
  * ITL1 to 400 to 1000
  * ITL4 to 100 to 400
  * RELTOL to .002 to .01
  * VNTOL to 100u



Circuit-based Suggested Solutions

* Use R-C snubbers (time constant small compared to switching period) across diodes, switches, thyristors, and other nonlinear devices.
* Use a large resistor in parallel with an inductor. Resistance much larger than inductive impedance at switching frequency.
* Use a small resistor in series with a capacitor. Resistance much less than capacitive impedance at switching frequency.
* Assign small but finite rise and fall times to pulsed sources (1% of switching period or less).
* In general put a large resistor in parallel with any element suspected of causing convergence problem.
* If error message indicates a floating node, connect node to ground with a large (1megohm) resistor.
* Loops involving only voltage sources and inductors but no series resistance cause errors. Insert a small resistance anywhere in the loop.

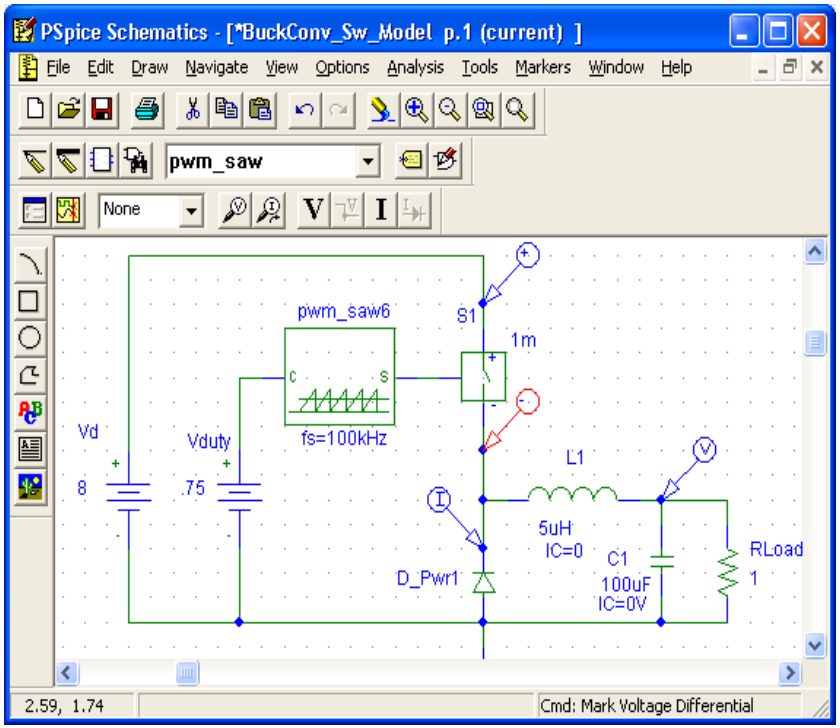
Using Probe - Specifying Desired Data for Display

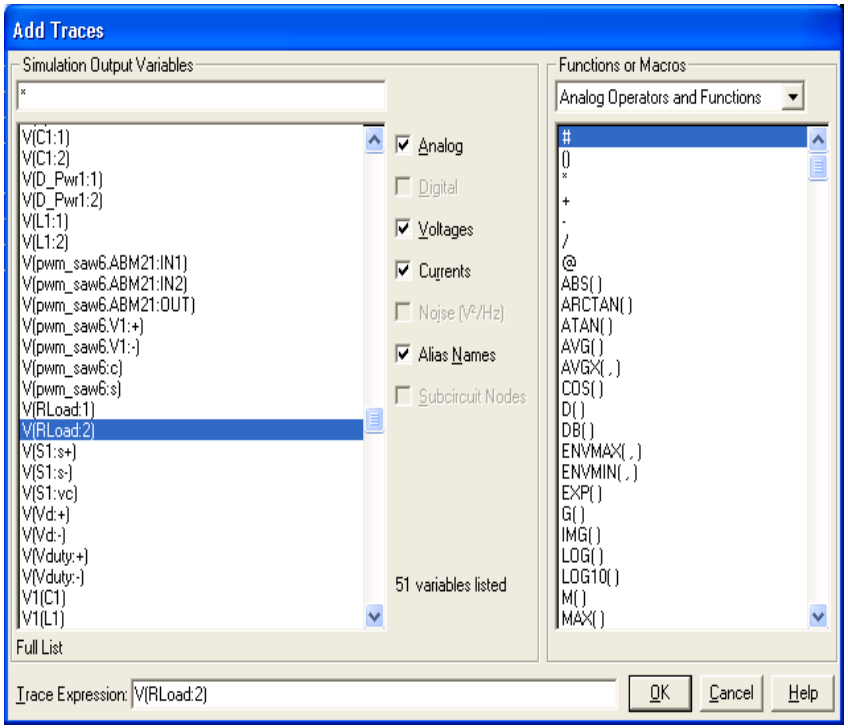
Markers on Circuit Schematic

* Voltage and current markers on Schematic toolbar or Markers pull-down menu.
* Place at desired locations. Can be moved, deleted, added as needed to change displayed data.

Trace Menu in Probe Window

* To add traces, select Add Trace in Trace pull-down menu in Probe window.
* Select desired data in Add Traces dialog box.
* Most useful when using Probe Functions or Macros for more complex analysis.





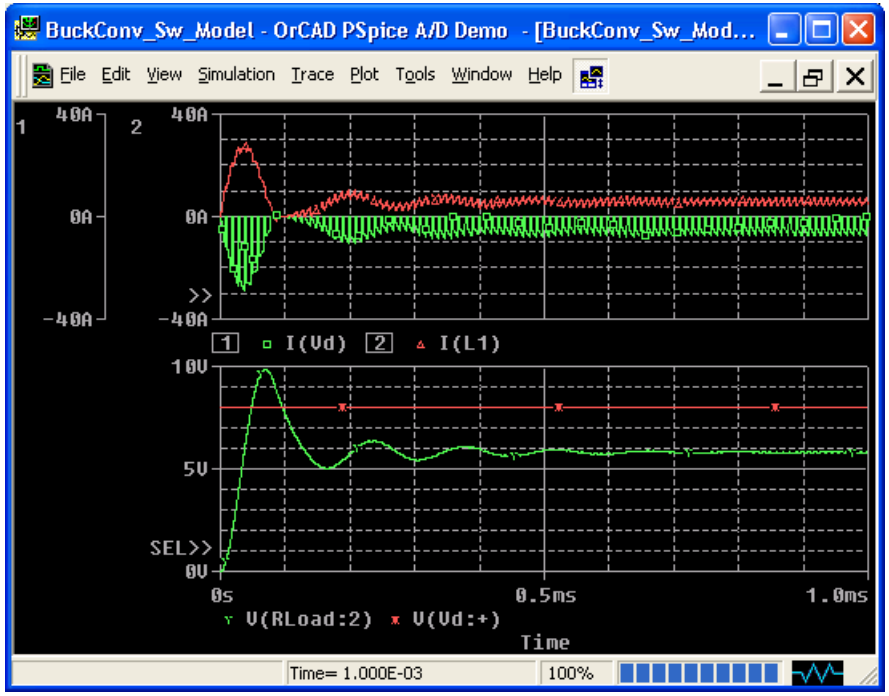
Overview of Probe Capabilities

Multiple Display Options

* Display multiple traces on same plot - Probe Trace Menu
* Multiple axes on plot - Probe Plot menu
* Multiple plots in window - Probe Plot menu
* Append data to existing plot from other simulations - Probe File menu

Extensive Functions/Macros for Analysis

* Numerous mathematical functions/macros for manipulating simulation results to obtain "dependent" data orinformation.
* Example: average power taken from dc supply Vd in buck converter. AVG(I(Vd)*V(Vd:+))
* Example: average power dissipated in Rload of buck converter. AVG(I(Rload)*V(Rload:2))

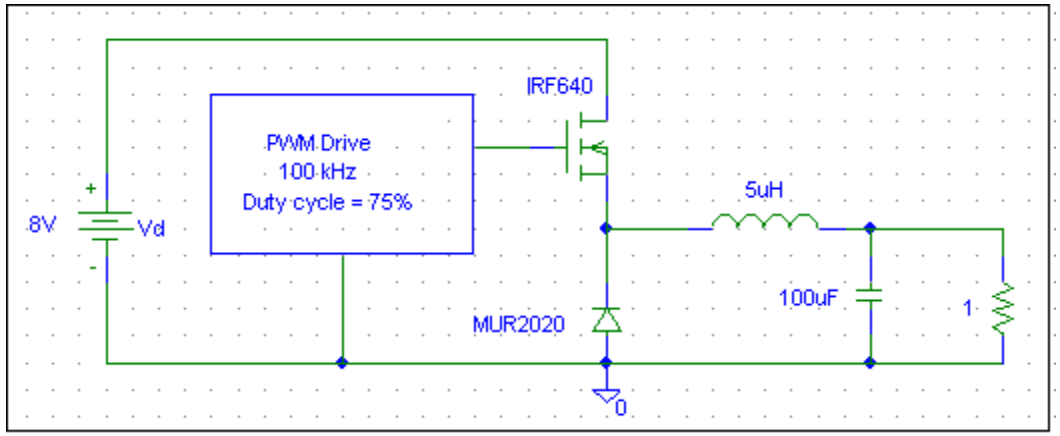


Do-It-Yourself Exercise

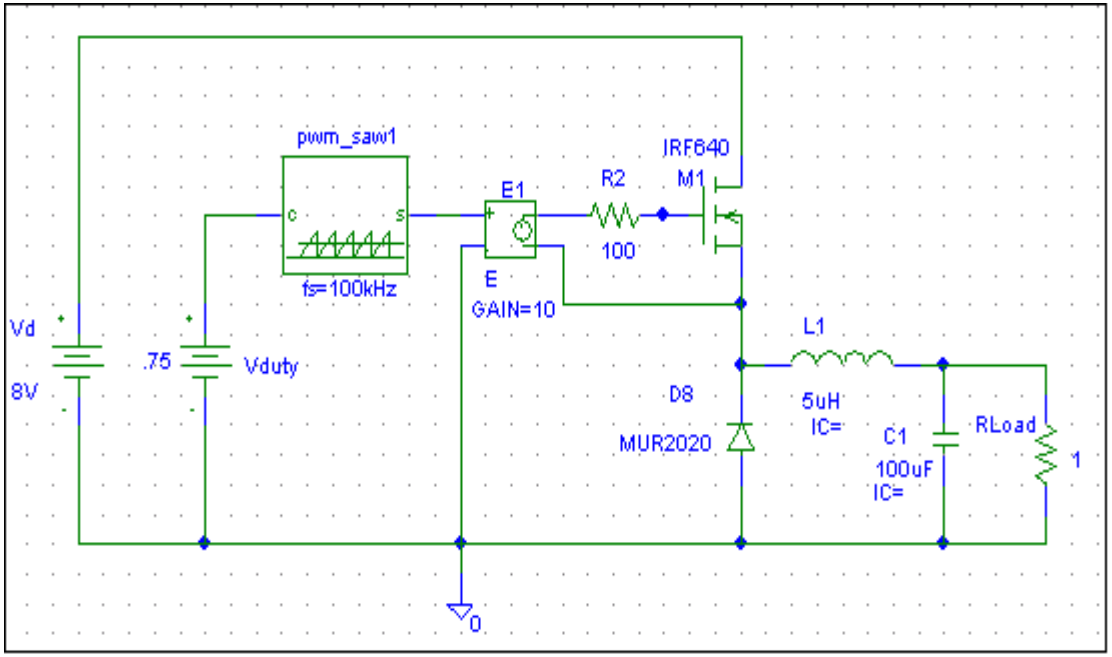
Buck Converter

Guided Do-It-Yourself Exercise - Buck Converter

* Buck converter implemented with realistic MOSFET and diode models.
* Same circuit parameters as buck converter with ideal switch loaded from CD

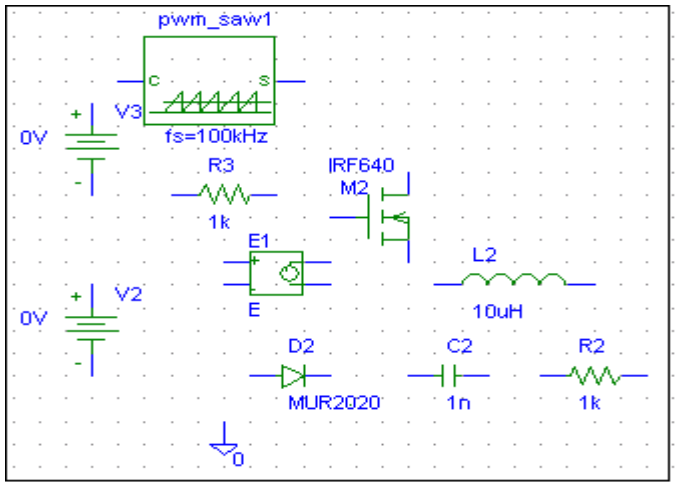


* Buck converter implemented in Pspice.
* Voltage-controlled voltage source E1 needed because pwm_saw output is with respect to ground.
* E1 gain set at 10 so that E1 output is large enough to drive the MOSFET with a 1V input from pwm_saw.
* 100 ohm series gate resistance added so realistic Vgs can be seen.

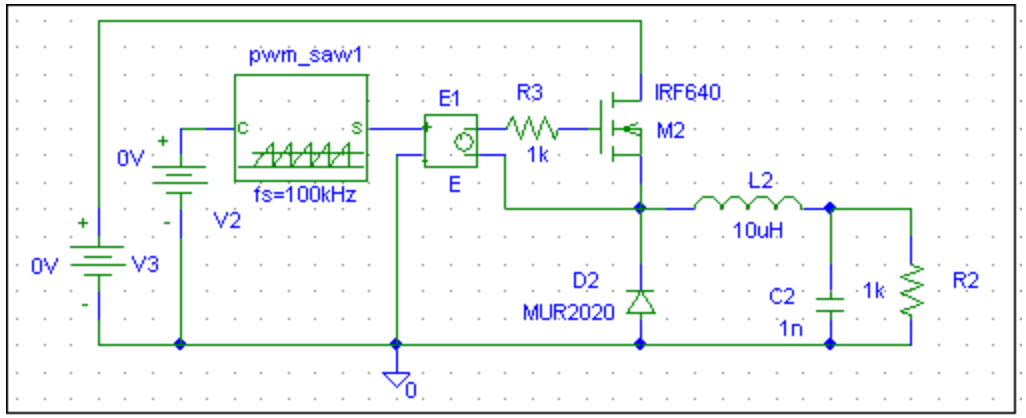


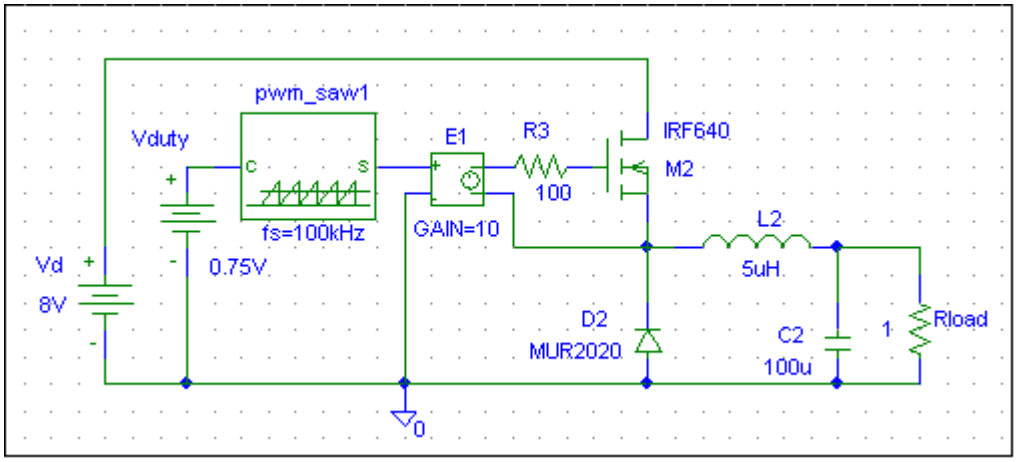
Guided D.I.Y. Exercise - Input the Circuit Topology

1. Get needed components



2. Reorient components, make electrical connections and thus form desired circuit.

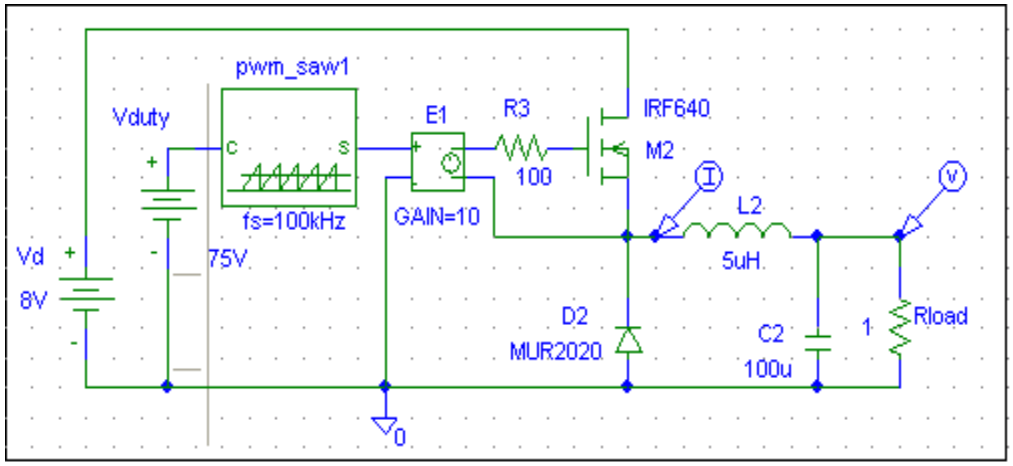




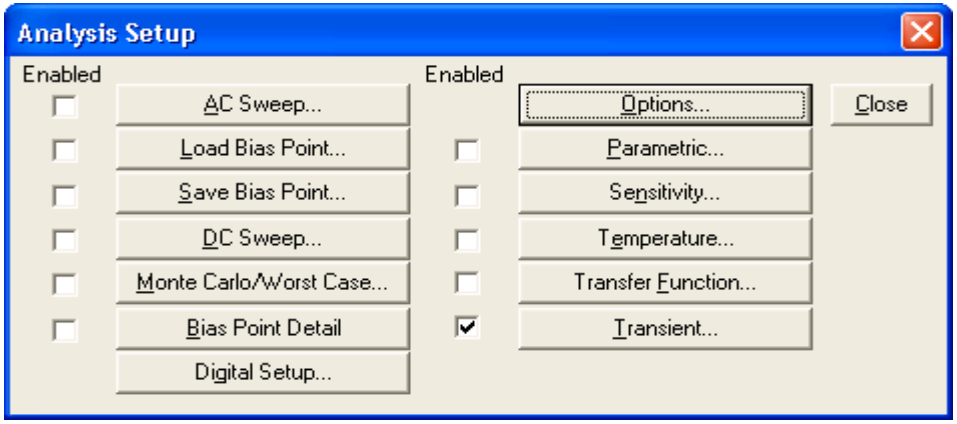
3. Enter component values and change identifying labels as desired.

Guided D.I.Y. Exercise - Simulation Setup

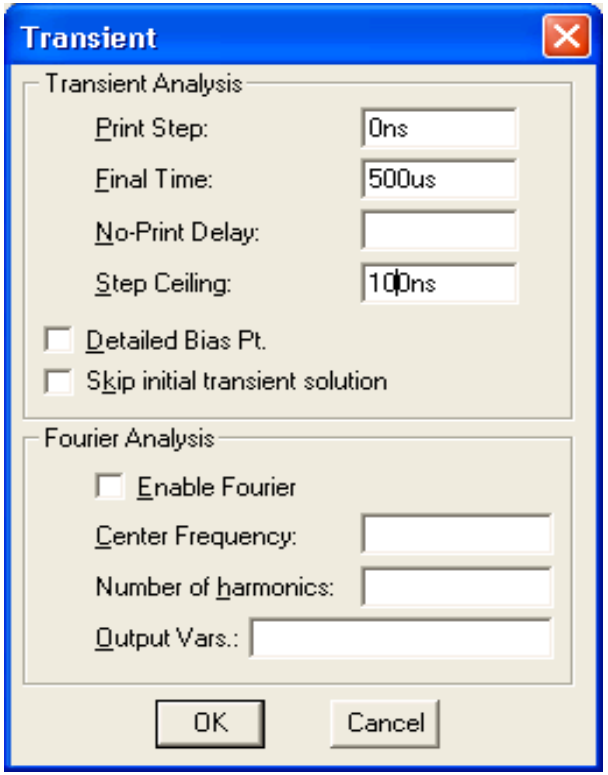
* Pick load voltage (across Rload) and inductor (L2) current for initial display in Probe.



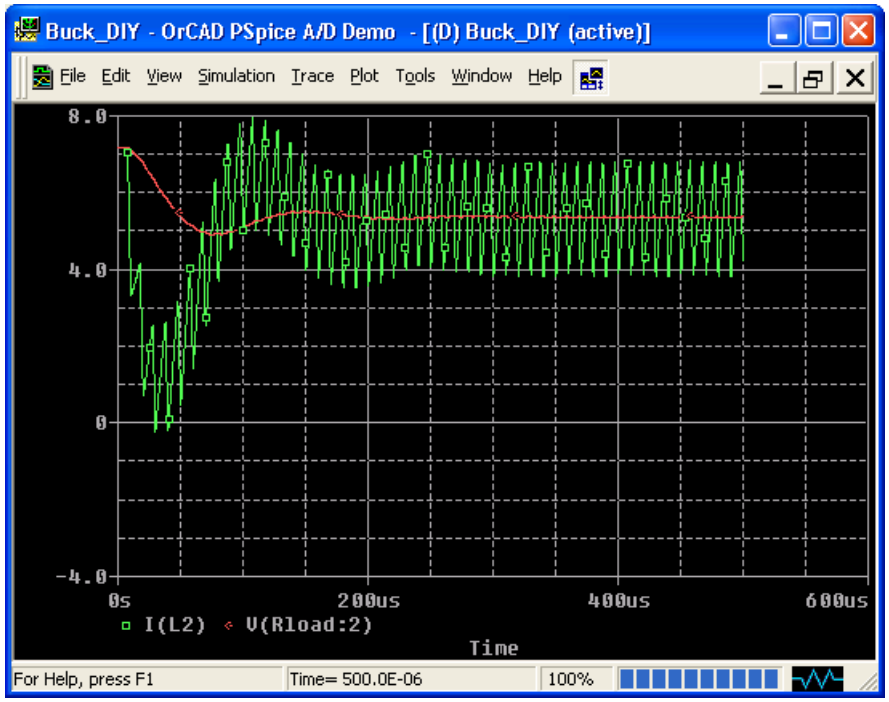
* Choose Transient for analysis to be performed and use default error tolerances in Options.

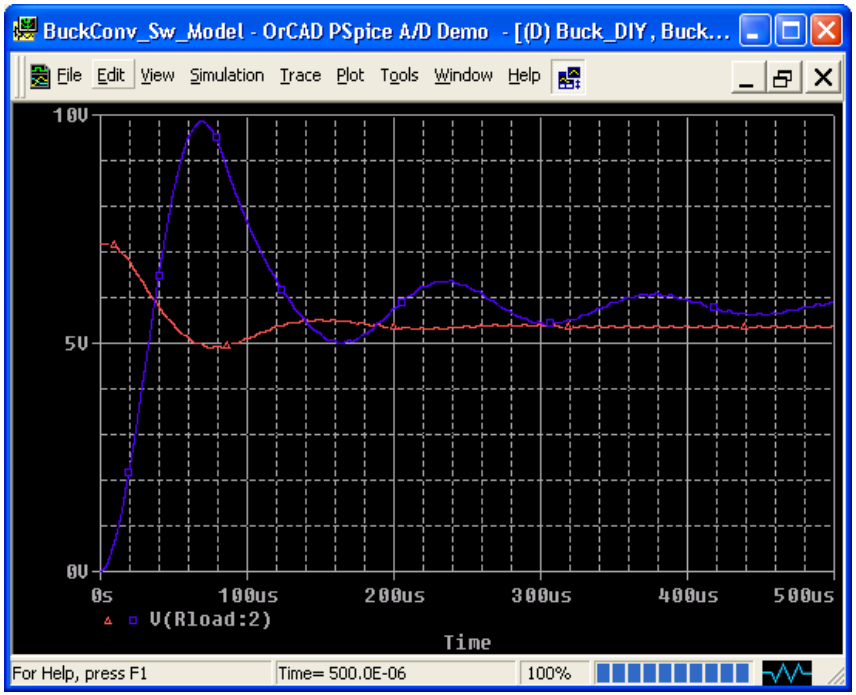


* Transient setup - use 500us for duration of analysis.
* Set Step Ceiling at 1% or less lof switching period - 100ns in this case.
* Rest of options not used for this analysis.



Guided D.I.Y. Exercise - Initial Simulation Results



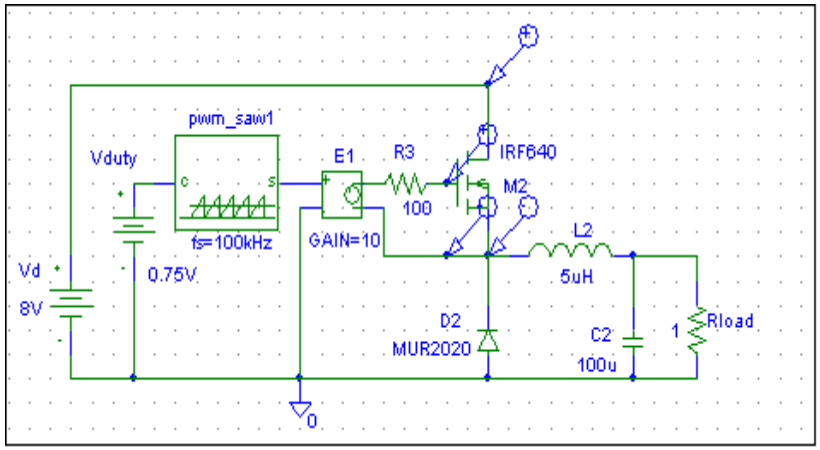


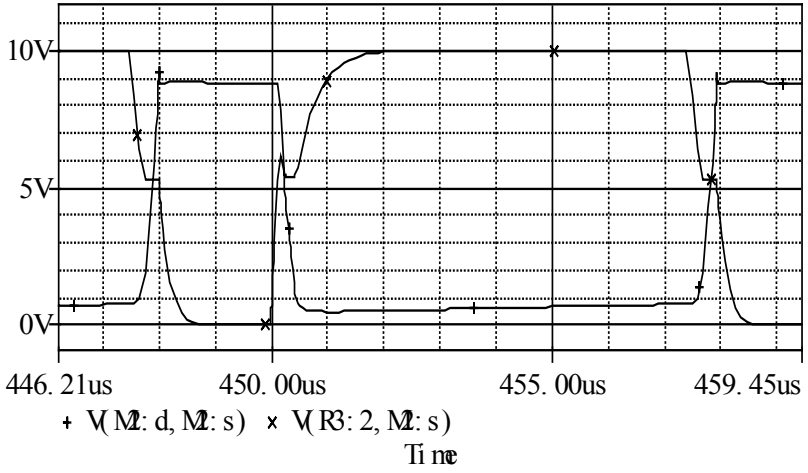
* Green trace, I(L2), inductor (L2) current.
* Red trace, V(Rload:2), load voltage.
* Damped oscillations in first 300 microseconds represent establishment of steady state operating conditions after starting from an initial dc operating point calculated by PSpice.

* Red trace, load voltage for buck with MOSFET as switching element.
* Blue trace, load voltage for buck with voltage-controlled switch and ideal diode.
* Buck with voltage-controlled switch and ideal diode has approximately 0.4V higher output. Due to lower losses in switch and diode.

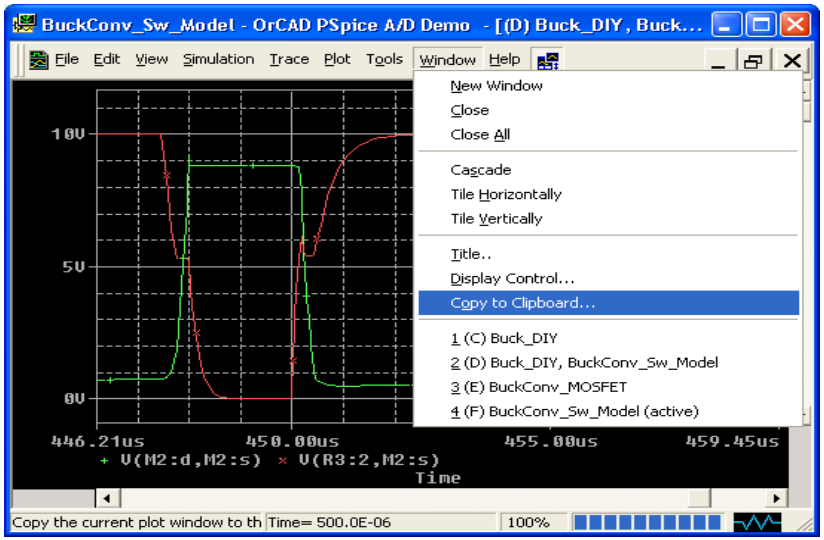
Guided D.I.Y. Exercise - MOSFET Voltages - Single Cycle

* MOSFET gate-source and drain-source voltage selected using differential voltage markers. Available from Marker pull-down menu in Schematics.





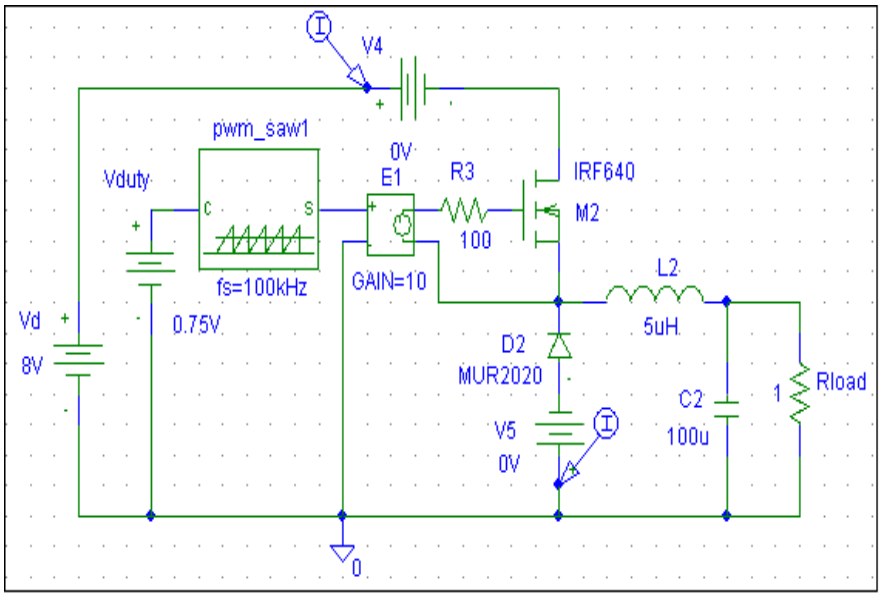
* To view only one or two switching cycles, select Zoom Area button on Probe toolbar. Then with mouse button depressed, draw a rectangle in Probe window which is area tp be displayed in full Probe window.
* To get black trace on white background, choose Copy to Clipboard on Window pull-down menu in Probe.

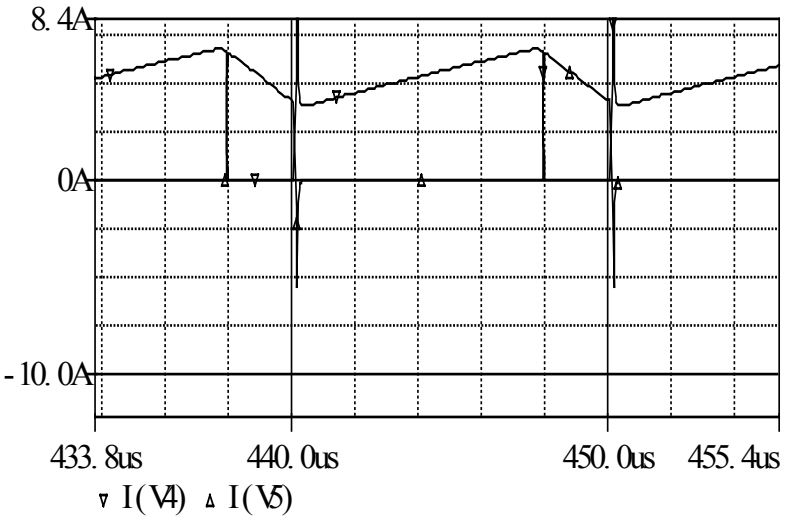


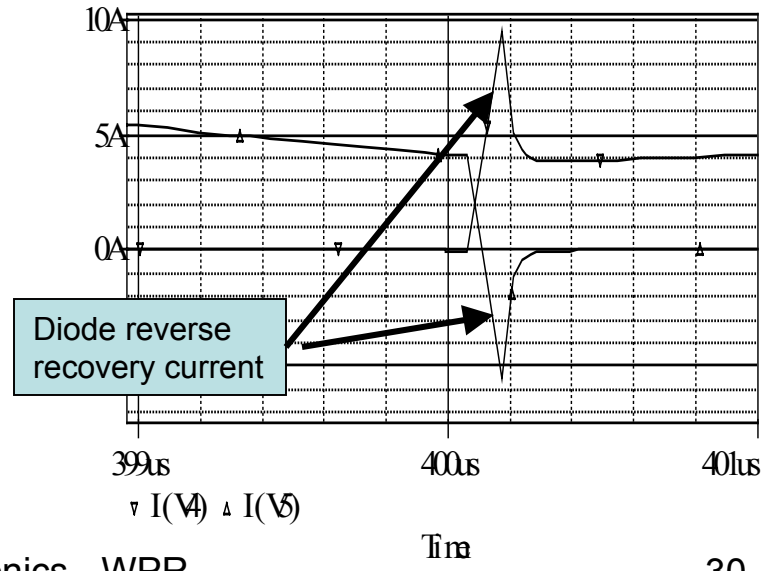
* Select buttons in dialog box shown to the left and click ok. Paste Clipboard into desired document to view.

Guided D.I.Y. Exercise - Dislaying Branch Currents

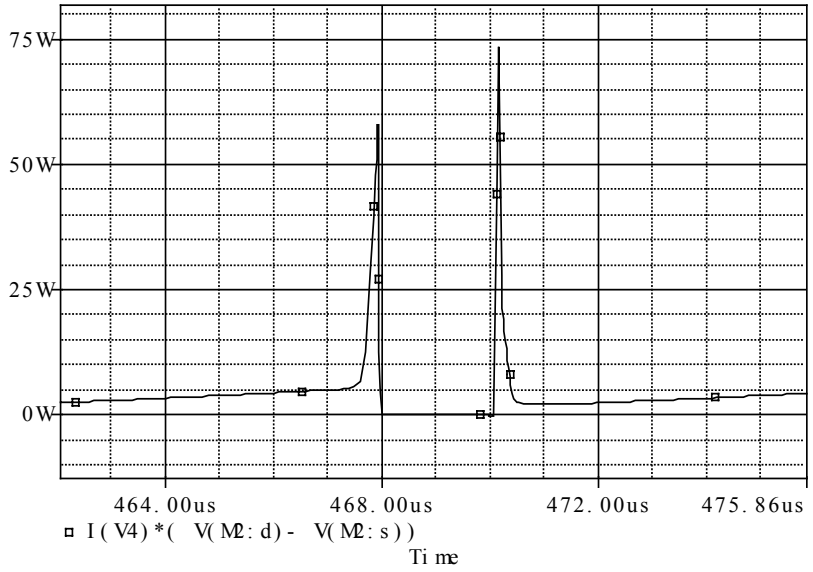
* Current markers only work for PSpice (built-in) components.
  * Do not work for user-defined models (e.g. pwm_saw) or external models (e.g. IRF640)
  * Use of Add Trace window can be confusing if non-Pspice model is comprised of several components.
* Add a zero value dc voltage source in branch where current display is desired. Example shown below for MOSFET drain current and diode current. Current marker will work for voltage source.







Guided D.I.Y. Exercise - Power Dissipation, Efficiency

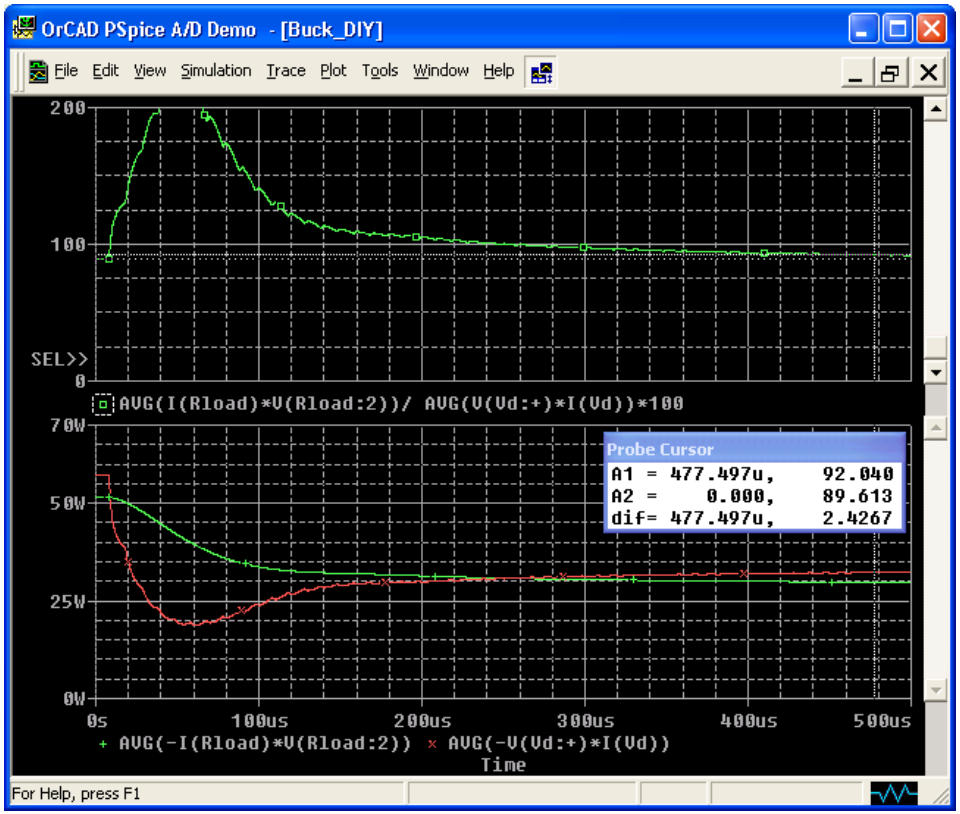


* Instantaneous power dissipation in the MOSFET for a single switching cycle.

* Upper plot - efficiency (<P_o>/<P_{in}>)*100 of buck converter example

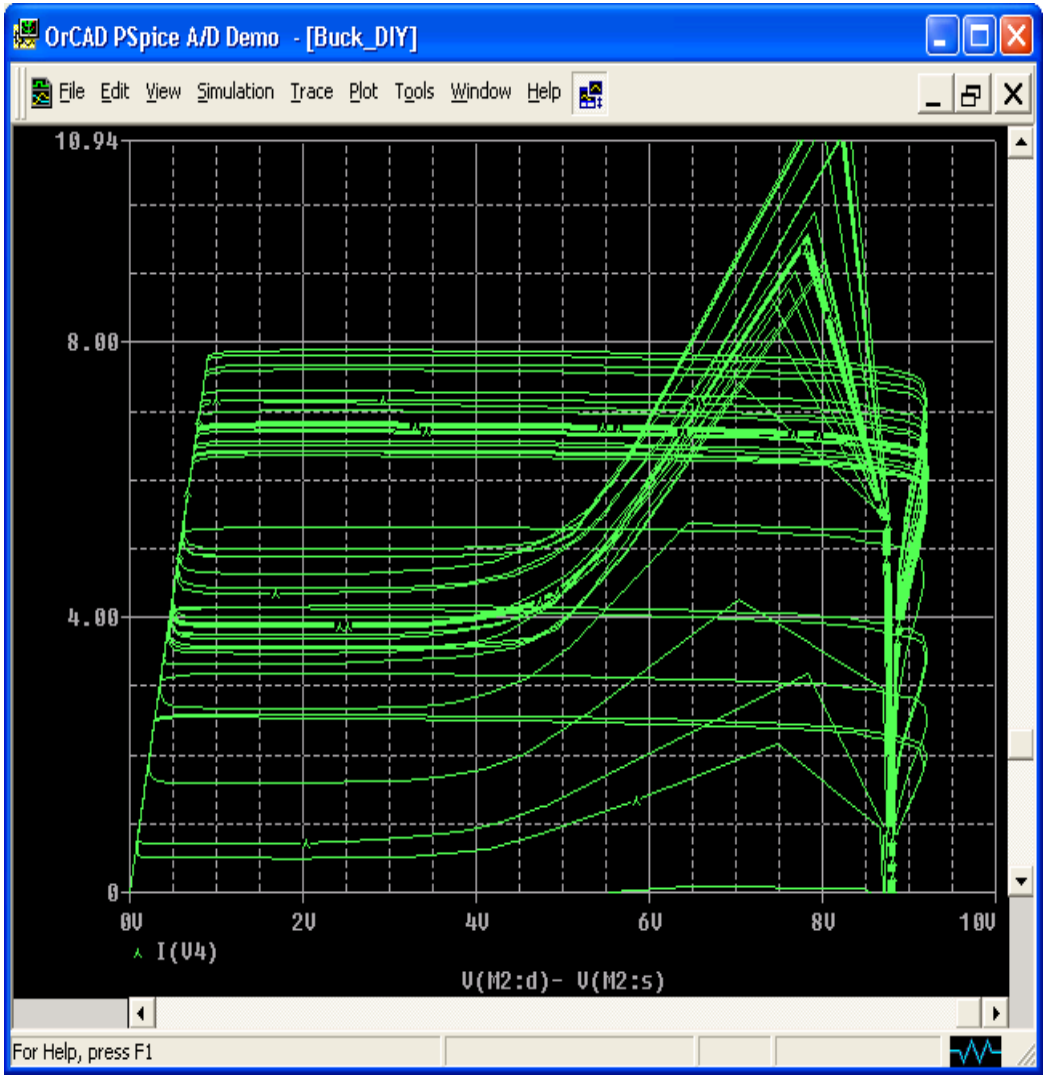
* Lower plot - average input power (<P_{in}>) and average load power (<P_o>)

* Traces are running averages, so values only meaningful at end of simulation where stable constant values are obtained.

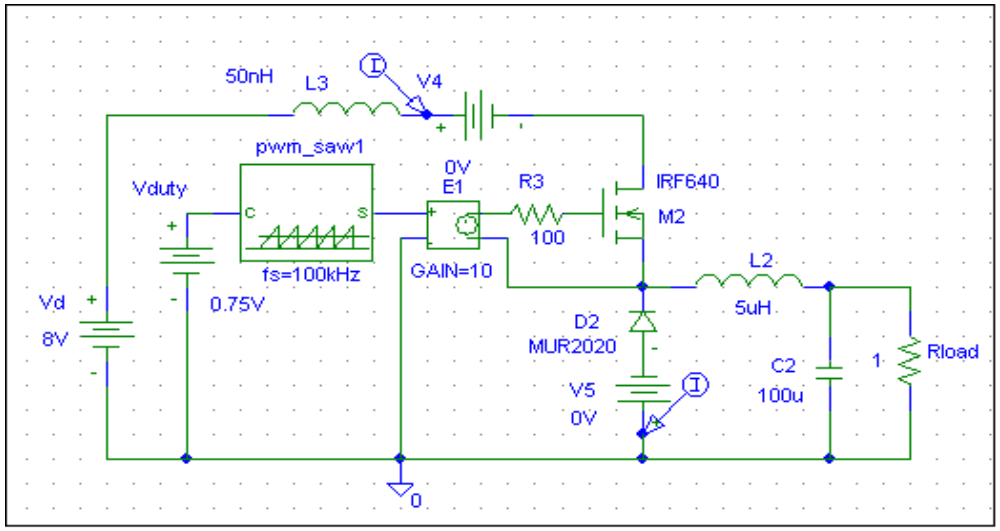


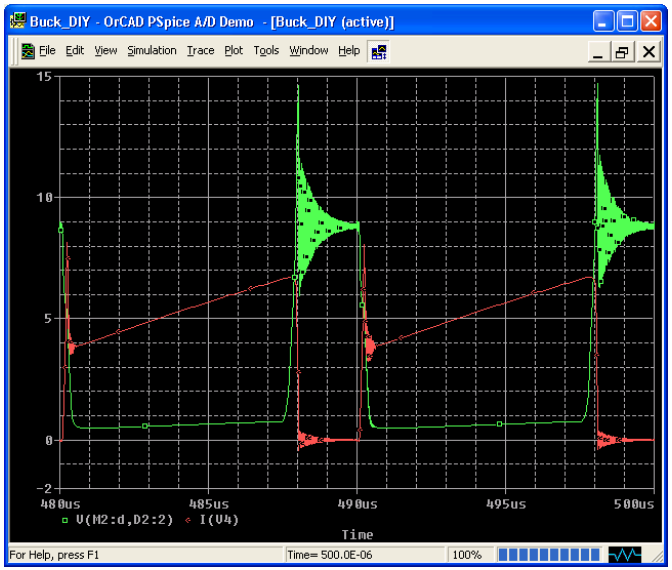
Guided D.I.Y. Exercise - MOSFET Switching Trajectory

* Plot drain current vs time.
* In Plot menu, select Axis Settings, and select Axis Variable button.
* In resulting X Axis Variable dialog box, change variable to the drain-source voltage V(M2:d) - V(M2:s)
* Close open dialog boxes and return to Probe window.
* To show trajectory corresponding to steady state conditions, redo transient analysis with the No_Print Delay set to 480us (for time window of 500us). Only last one or two switching cycles will be displayed.



Guided D.I.Y. Exercise - Effects of Circuit Parasitics





* Upper left: MOSFET switching trajectory with 50 nH of stray series inductance. No_Print Delay of 480 us for 500 us simulation window.
* Drain current and drain-source voltage versus time with 50 nH series inductance corresponding to switching trajectory of upper left window.
* Effects of any other parasitics could also be modeled.
  * C2 effective series resistance or inductance
  * L2 series resistance
  * Supply voltage Vd series resistance

Average Representations

of the PowerPole

Need for Average Model of PowerPole

* Switching circuit implementation of converters not amenable for use in design of control circuits.

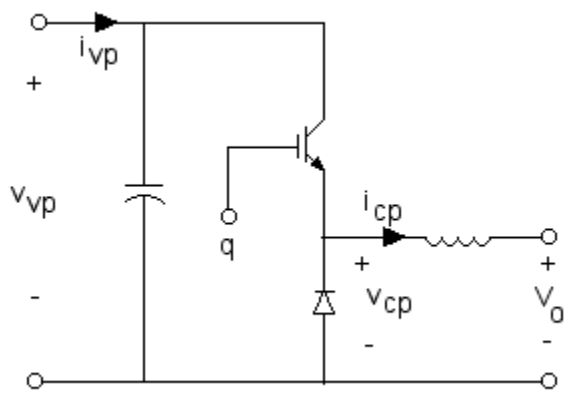
* Average representation of the converter with the switchings removed needed for feedback control design.

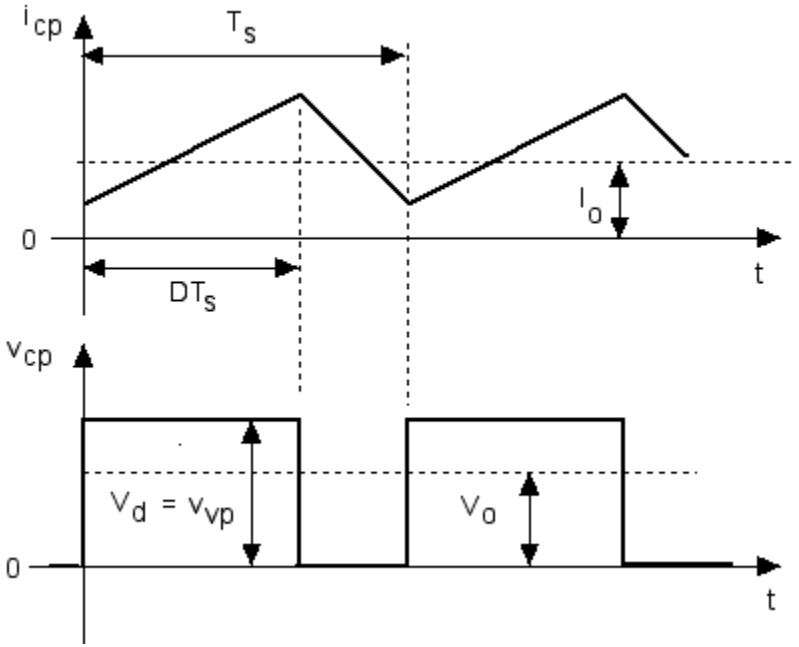
* Space state averaging complex and confusing to students.
  * Non-intuitive and must be repeated for each separate converter topology.
  * Not amenable for use in circuit-oriented simulators such as Pspice.
  * Does not use the unifying concept of the powerpole.

* Advantages of an average representation of the powerpole.
  * Would maintain the unifying concepts in the frequency domain which are found to be so useful in the time domain.
  * Would be a drop-in element in the converter topology just like any other component.
  * Would enable simulators such as Pspice to be used as design tools for feedback controllers using their extensive small signal swept frequency analysis capabilities.
  * Would simplify analytical studies of converter input (duty cycle) to output (output voltage) transfer functions versus frequency.

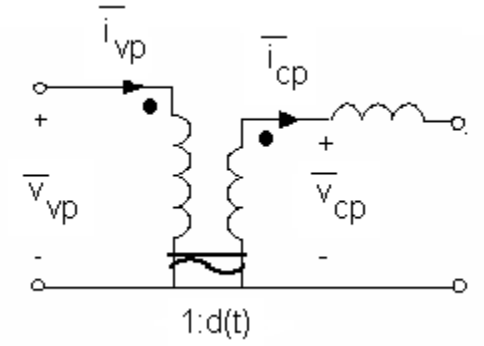
PowerPole Average Model for CCM

PowerPole circuit

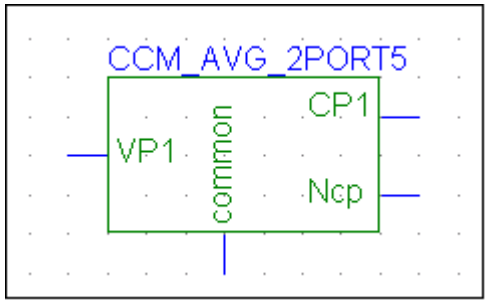




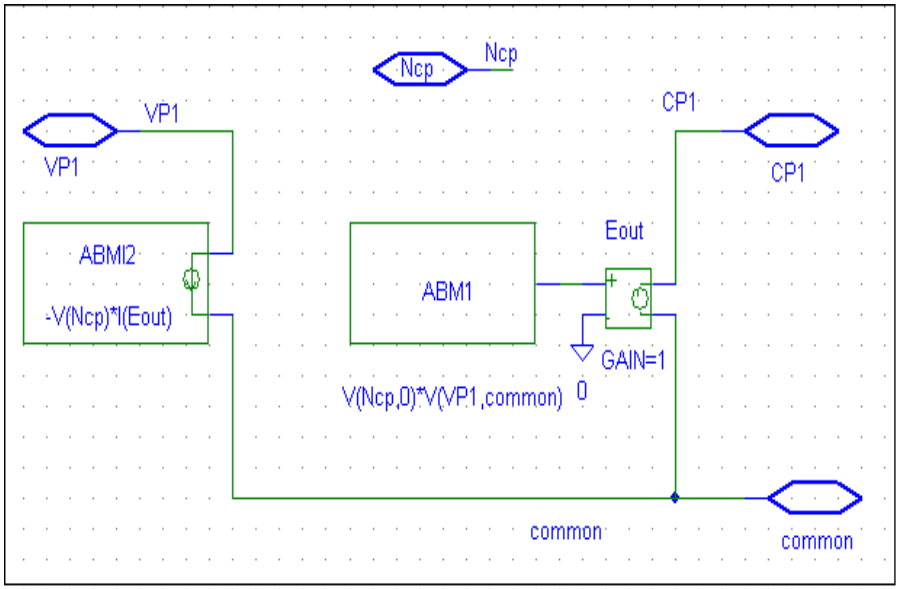
* $\langle v_{cp} \rangle = V_o = DV_d = D\langle v_{vp} \rangle$
* $\langle v_{cp} \rangle \langle i_{cp} \rangle = \langle v_{vp} \rangle \langle i_{vp} \rangle$: power conservation
* $\langle i_{vp} \rangle = D \langle i_{cp} \rangle$
* Assume variations in duty cycle at frequencies less than $0.1f_s$. D becomes d(t) and average quantities can be used to represent slowly varying (compared to switching times) quantities.
* Simplify notation by replacing brackets with a bar. Thus $\overline{v}_{cp} = d(t)\overline{v}_{vp}$ and $\overline{i}_{vp} = d(t)\overline{i}_{cp}$
* Suggests equivalent circuit shown below.



CCM PowerPole Model Implemented in PSpice



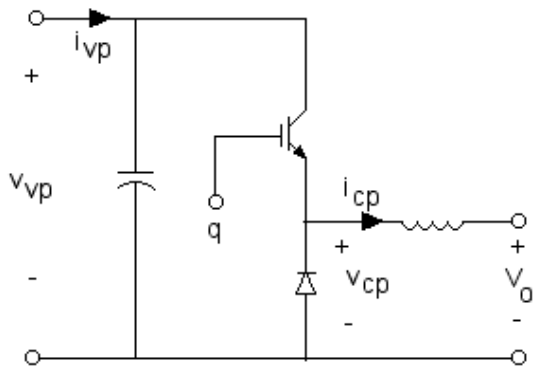
* Pspice circuit symbol for PowerPole average model valid in CCM only.
* Listed in symbol library PE_lib1.slb as CCM_AVG_2PORT

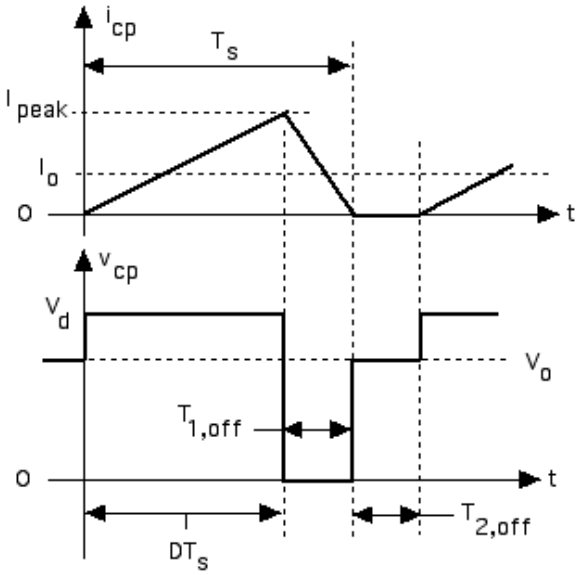


* Implementation of CCM average model of PowerPole.
* Ncp is the duty cycle of the PowerPole. Connected to a voltage source whose value is between 0 and 1. Value of the voltage source is the desired duty cycle.
* Duty cycle voltage source can be DC or time-varying.

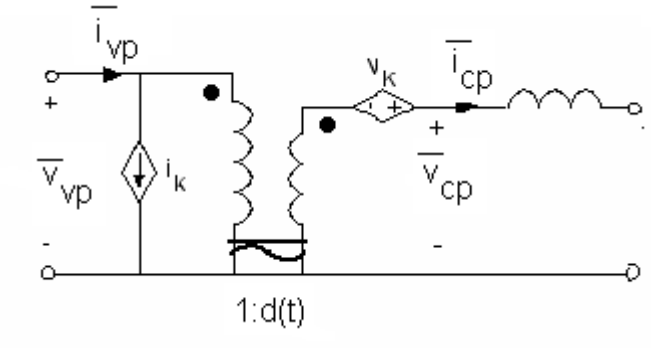
PowerPole Average Model for DCM and CCM

PowerPole circuit

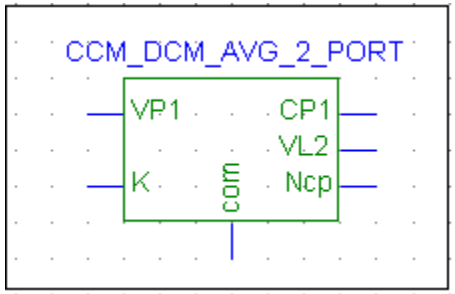




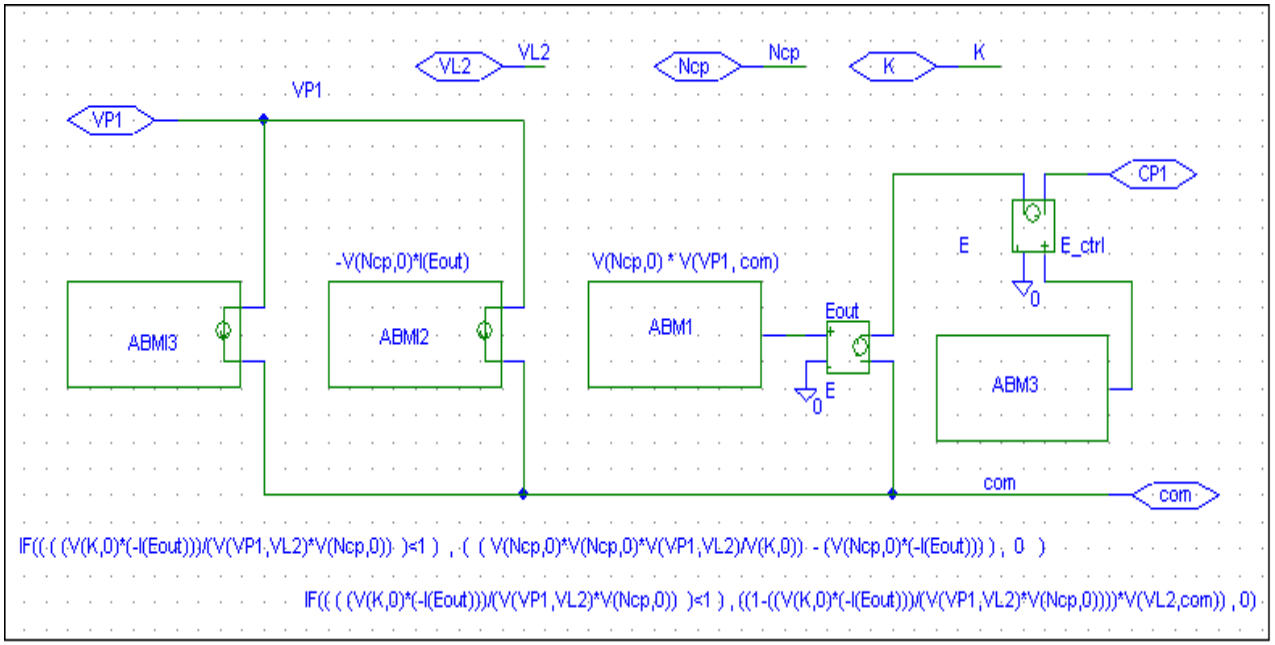
1. $I_{peak} = DT_s(V_{vp} - V_o)/L$; $\langle i_{cp} \rangle = I_o = I_{peak}(D + D_{1,off})T_s/2$; $D_{1,off} = T_{1,off}/T_s$
2. $D + D_{1,off} = kI_o/\{D(V_{vp} - V_o)$; $k = 2*f_s*L$
3. $V_A = \langle v_{vp} \rangle = DV_{vp} + D_{2,off}V_o = DV_{vp} + V_k$; This equation suggests putting a voltage source V_k in series with the CCM output as shown below.
4. $V_k = D_{2,off}V_o = (1 - \{D + D_{1,off}\})V_o = \{1 - kI_o/[D(V_{vp} - V_o)]\}V_o$
5. $\langle i_{vp} \rangle = D\, I_{peak}/2 = D^2T_s\,(V_{vp} - V_o)/(2L)$; Current port side of the DCM model can include CCM model if we express $\langle i_{vp} \rangle = DI_o + I_k$ where DI_o is the CCM portion of the current. I_k current source shown below in equivalent circuit of the powerpole.
6. $I_k = D^2T_s\,(V_{vp} - V_o)/(2L) - DI_o$



DCM-CCM PowerPole Model Implemented in PSpice



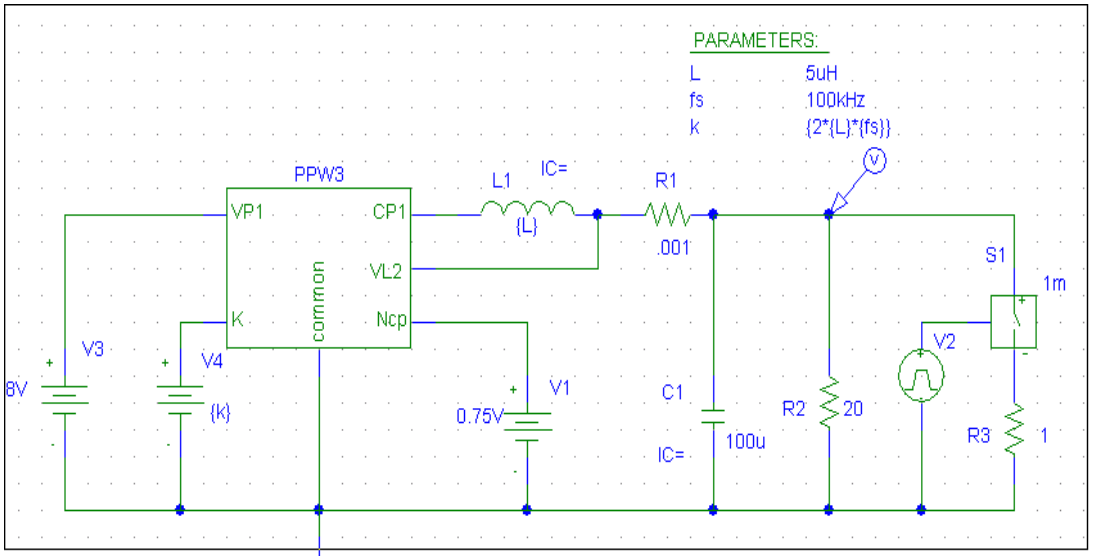
* Pspice circuit symbol for PowerPole average model valid in both DCM and CCM.
* Listed in symbol library PE_lib1.slb as CCM_DCM_AVG_2_PORT

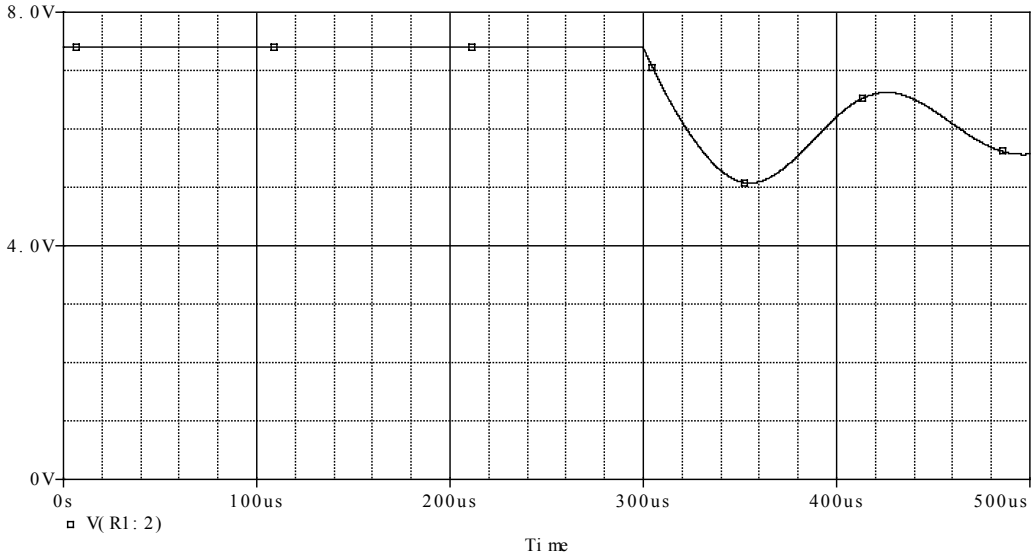


* Implementation of CCM and DCM average PowerPole model.
* Ncp = duty cycle of PowerPole. Connected to a voltage source with value between 0 and 1V. Value is the desired duty cycle.

* Duty cycle voltage source can be DC or time-varying.
* $k = 2*L*f_s$ where L is the inductance in series with the current port and f_s = switching freq.
* VL2 = external connection to load side of inductor in series with current port.
* ABMI3 and ABM3 in conjunction with formulas shown below them implement the dependent sources i_k and v_k.

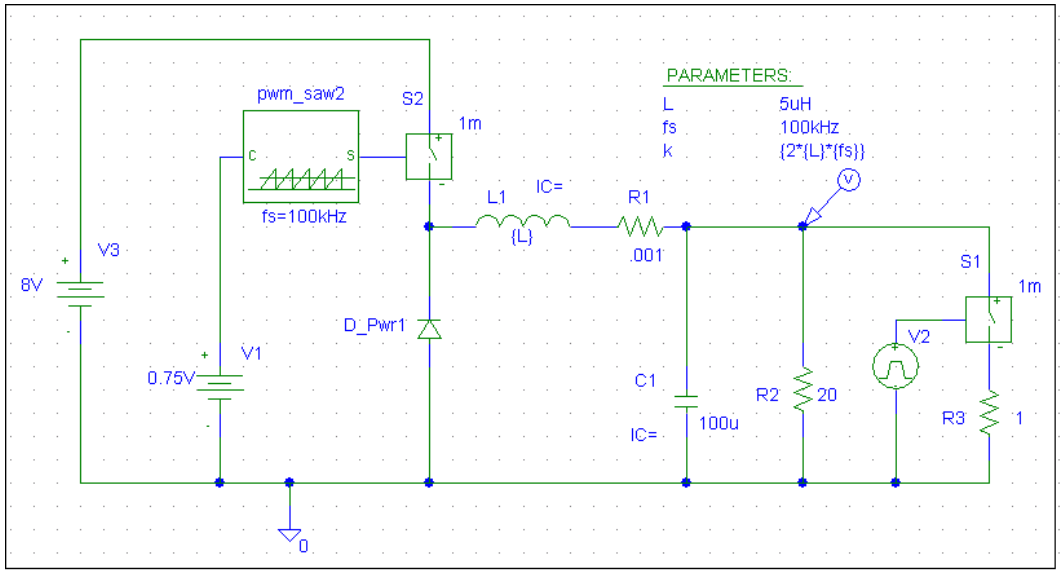
Buck Converter Utilizing Average PowerPole Model



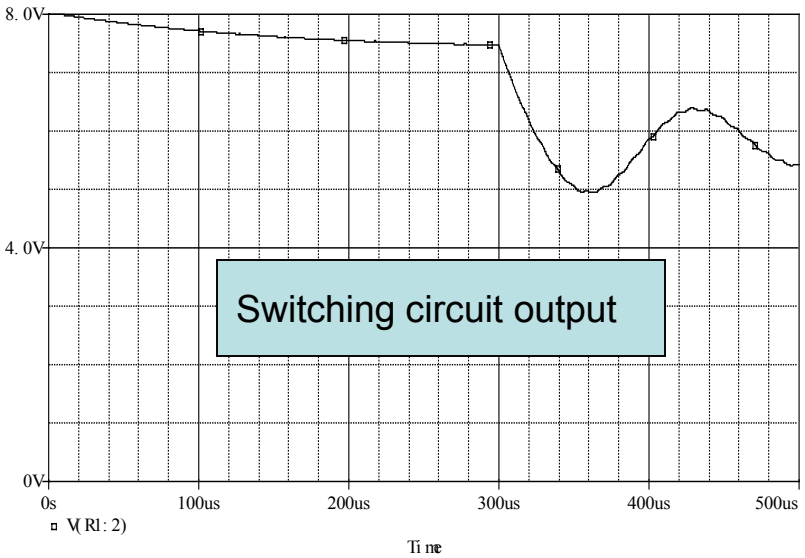


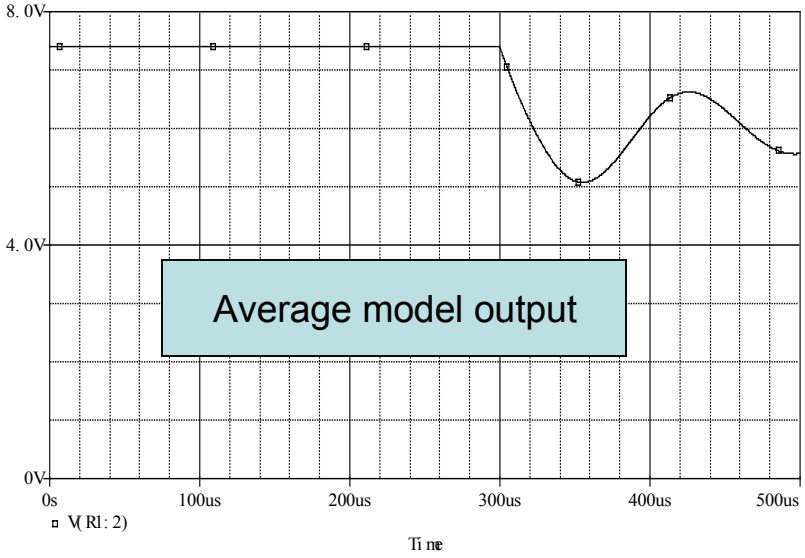
* Buck_Conv_Avg in Pspice Tutorial Circuits folder.
* Transient analysis - 500us window.
* Duty cycle = 75%
* Switch S1 switched on at 300us. Converter goes from DCM to CCM

Buck Average Model Compared with Switching Model



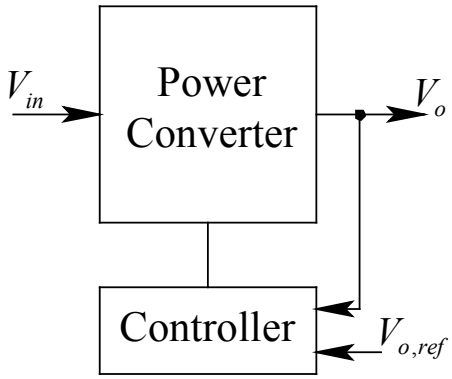
* Buck converter with switched load. Switching circuit implementation of converter.
* All parameters identical to previous average model circuit.
* Lower left waveform is switching circuit output. Lower right is average model output. Nearly identical outputs



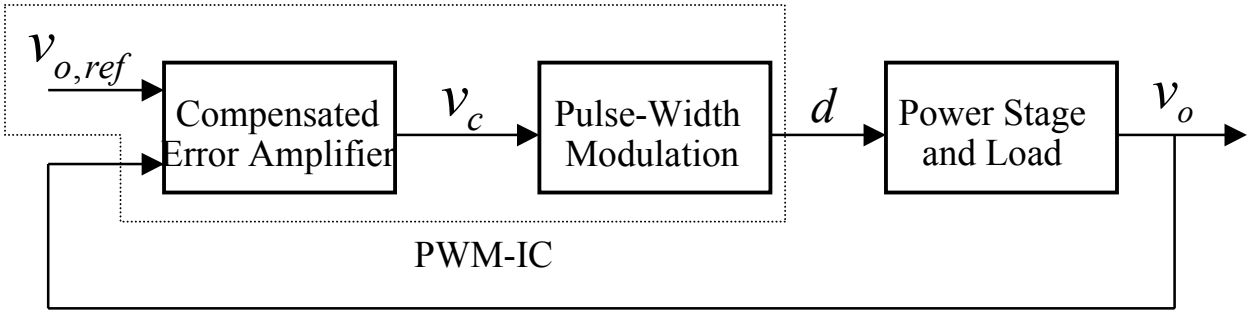


Voltage Mode Control of a Buck Converter

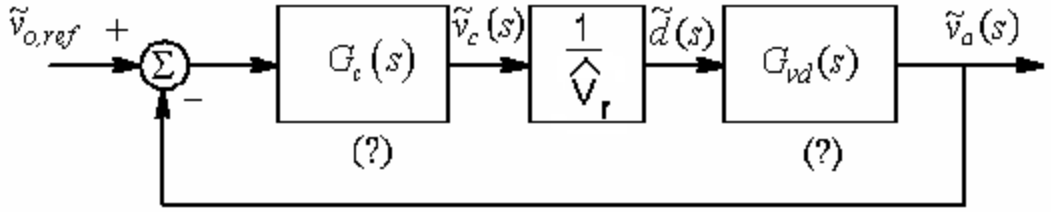
Converter Feedback Control Problem



Power converter with controller



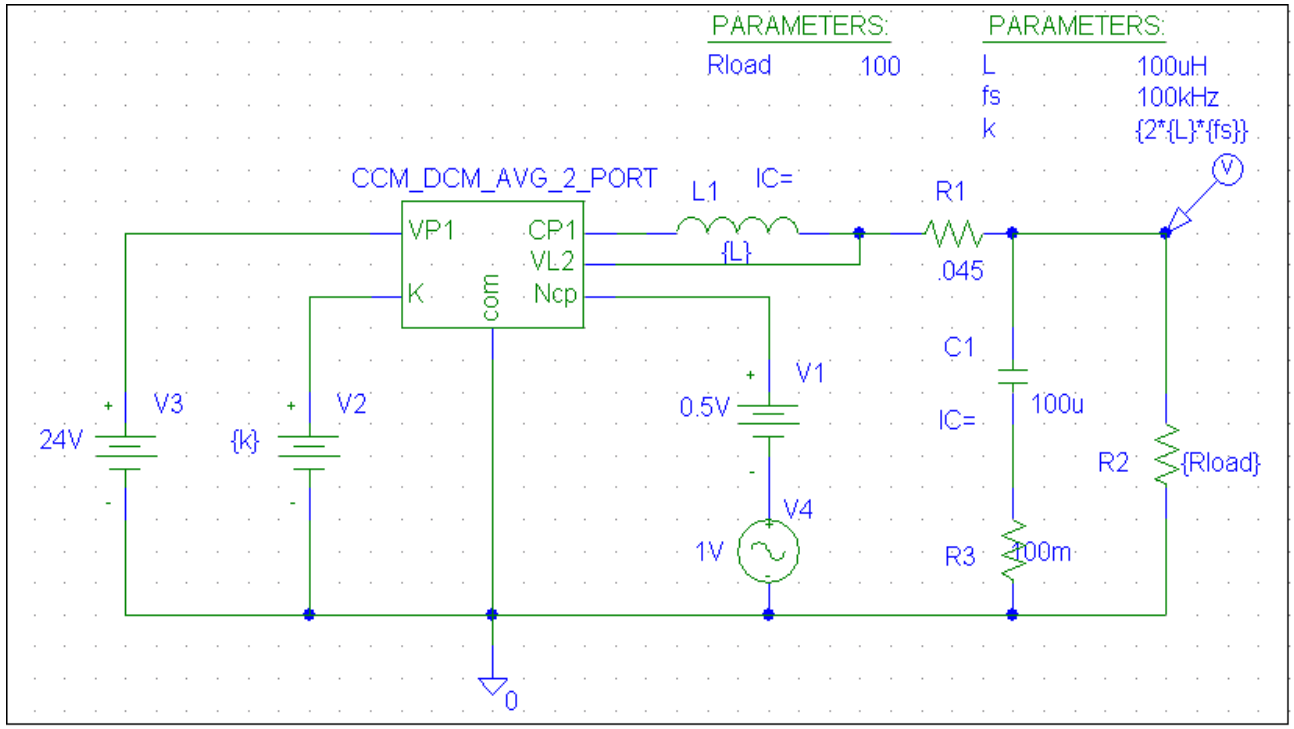
Time domain model



Frequency domain model

- **Power stage transfer function $G_{vd}(s)$ needed in order to design compensated error amplifier.**
- **Pspice using average model of PowerPole can find $G_{vd}(s)$**

Buck Converter Frequency Response - $G_{vd}(s)$



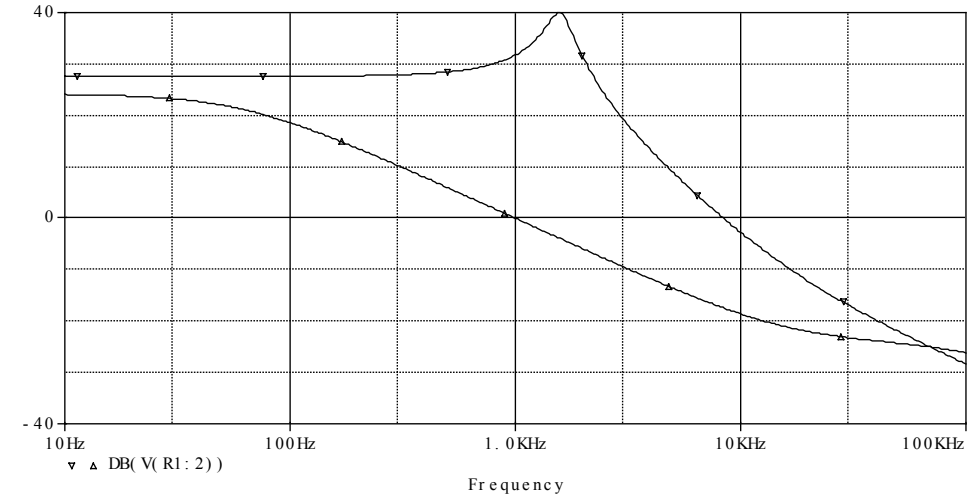
Circuit file name - Buck_Conv_Freq.sch

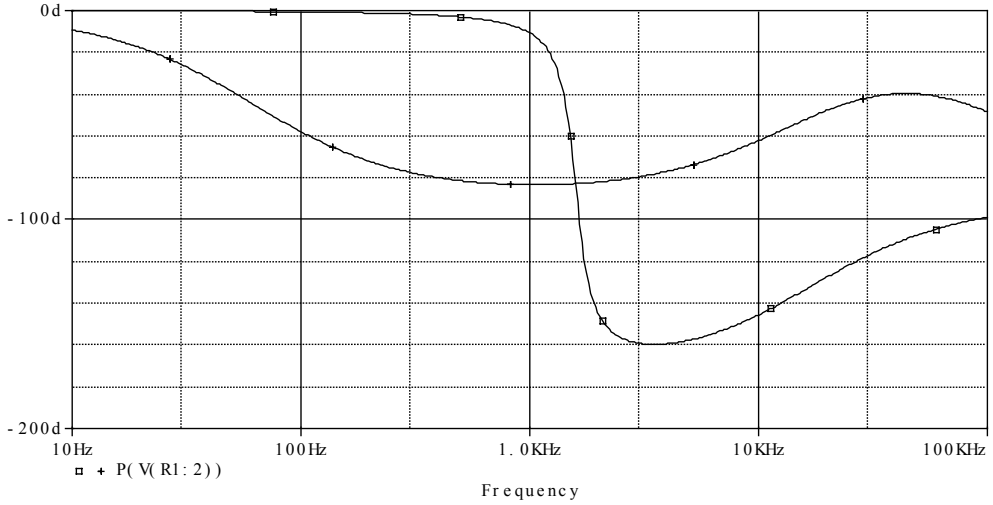
Located in PSpice Tutorial Circuits folder

* AC voltage source V4 provides duty cycle pertubation d(s).
* Swept frequency analysis from 10Hz to 1MHz.
* Parametric analysis with Rload = 10 ohms (CCM) and 100 ohms (DCM)
* Plot output voltage $V_o(s) = G_{v\,d}(s)$ since d(s) = 1 in magnitude.

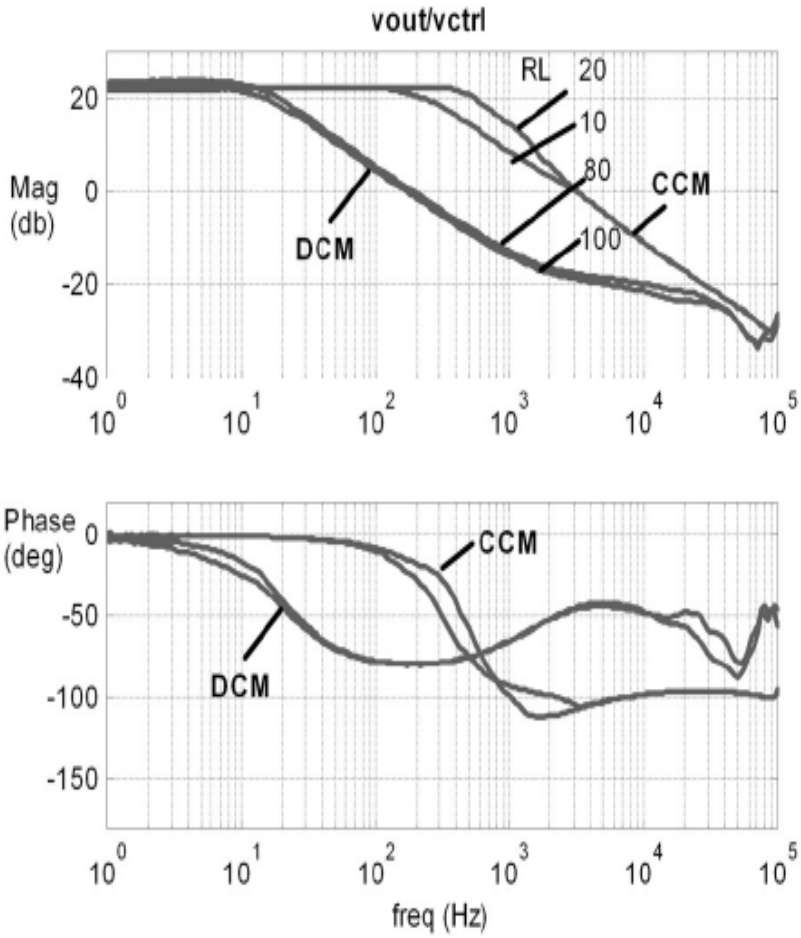
Buck Converter Frequency Response - $G_{vd}(s)$ (cont.)

PSpice Results

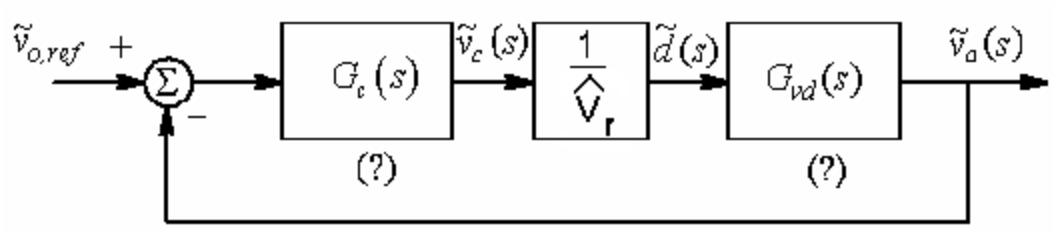




Experimental results using PowerPole board and frequency analyzer

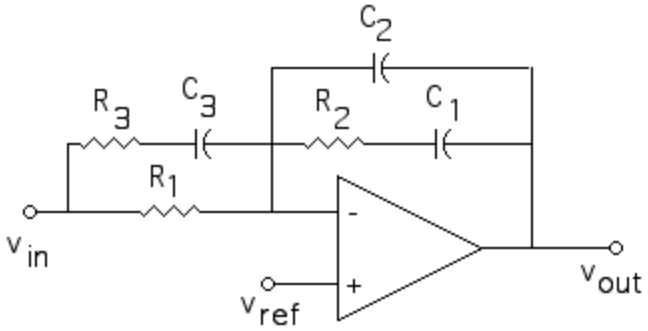


Closed Loop Voltage Mode Control of Buck Converter



Control loop frequency domain model

* Power processor (buck converter) frequency response, $G_{vd}(s)$ known from Pspice analysis.
* PWM block transfer function known.
* Design controller transfer function $G_c(c)$ on basis of desired closed loop response.



Compensated error amplifier

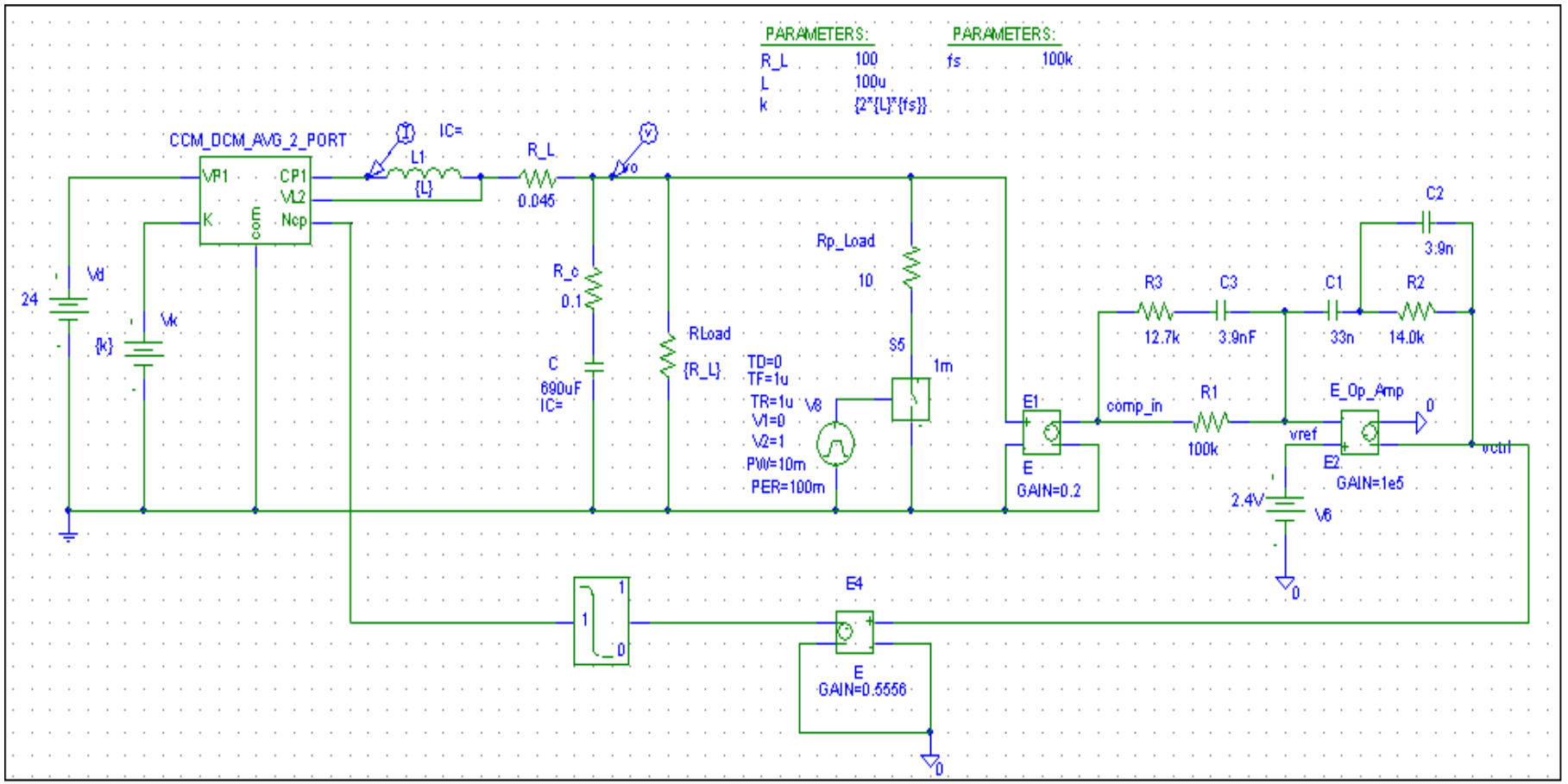
$$G_c(s) = \frac{k_c}{s}\frac{\left(1+\frac{s}{\omega_z}\right)^2}{\left(1+\frac{s}{w_p}\right)^2} \qquad \omega_z < \omega_p$$

Controller design details

* Select crossover frequency of 1 kHz
* Use K-factor approach to design controller. (H. D.Venable, "The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis", Proc. Powercon10, San Diego, USA, 1983.)
* k_c = 146.3, ω_z = 2πx334 rad/sec, ω_p = 2πx2990 rad/sec

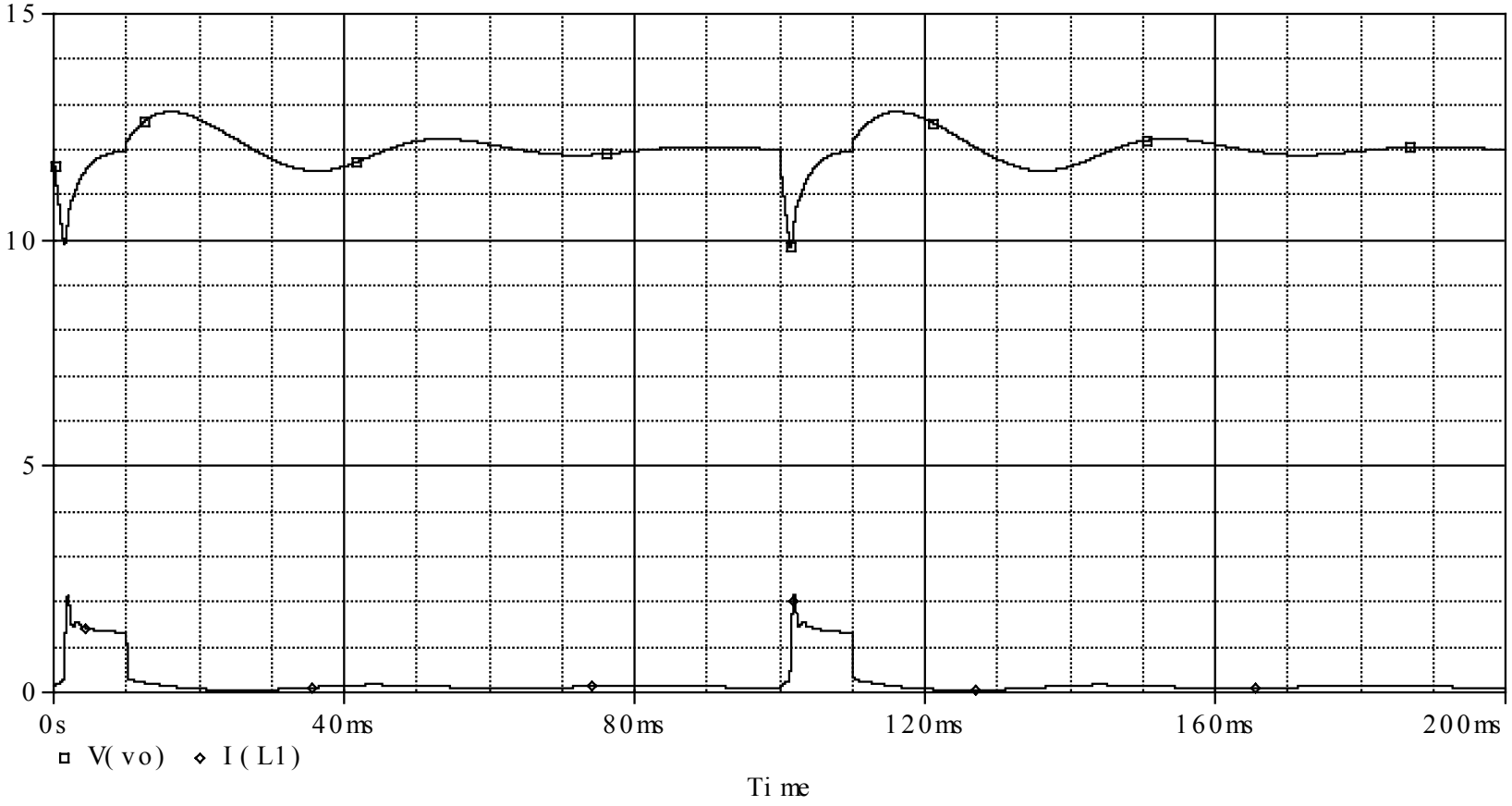
Buck Converter with Voltage Mode Control - Average Model

* Circuit file name: buck_conv_avg_fb_ctrl.sch
* Located in Pspice Tutorial Circuits folder.



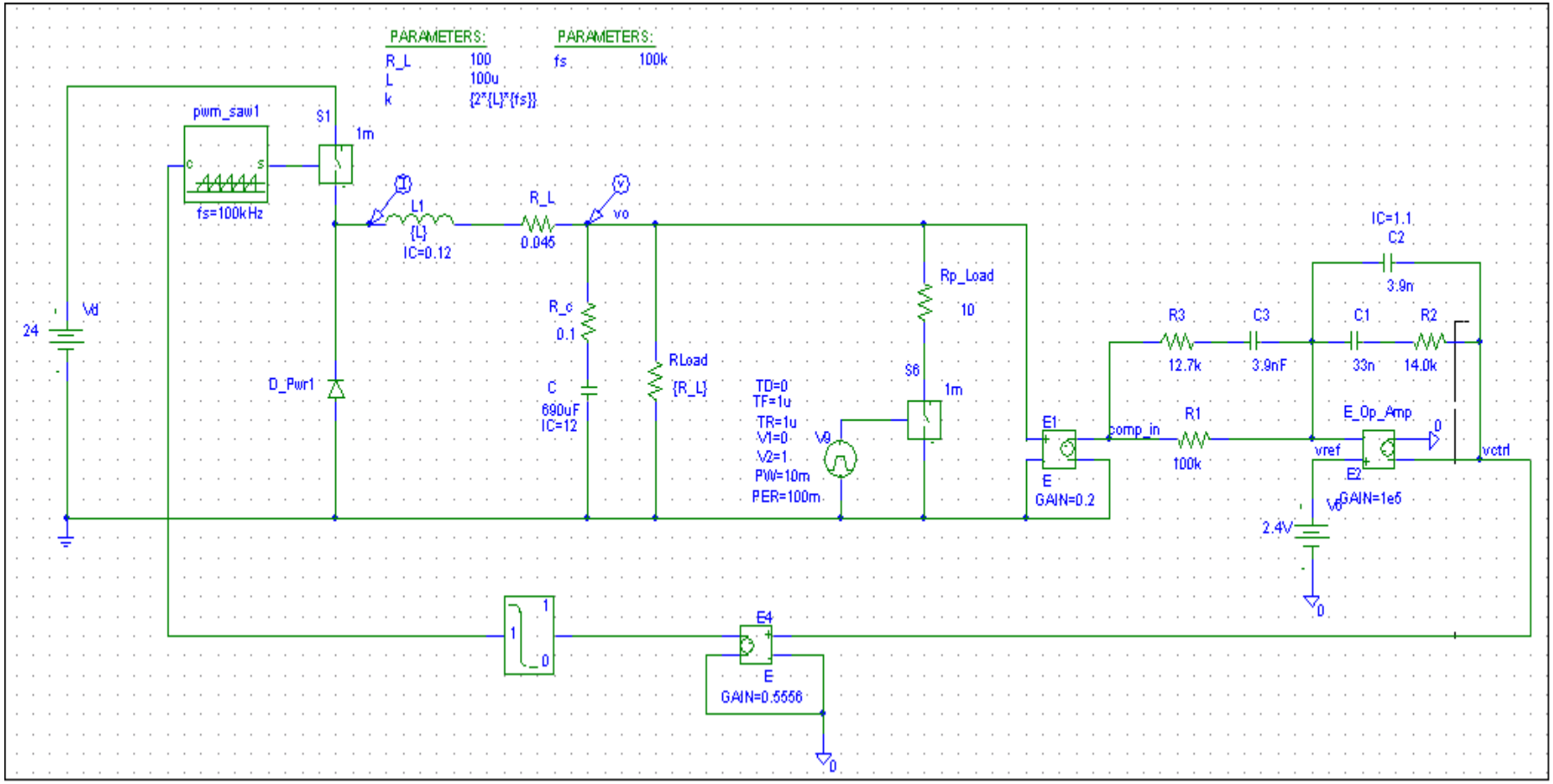
Controlled Buck Converter Dynamic Response

* Transient analysis of using average model of PowerPole. 200 ms time window.
* 10 ohm load switched in parallel with 100 ohm load for 10 milliseconds at t = 0 and t = 100 ms
* Output voltage and inductor current versus time displayed below.



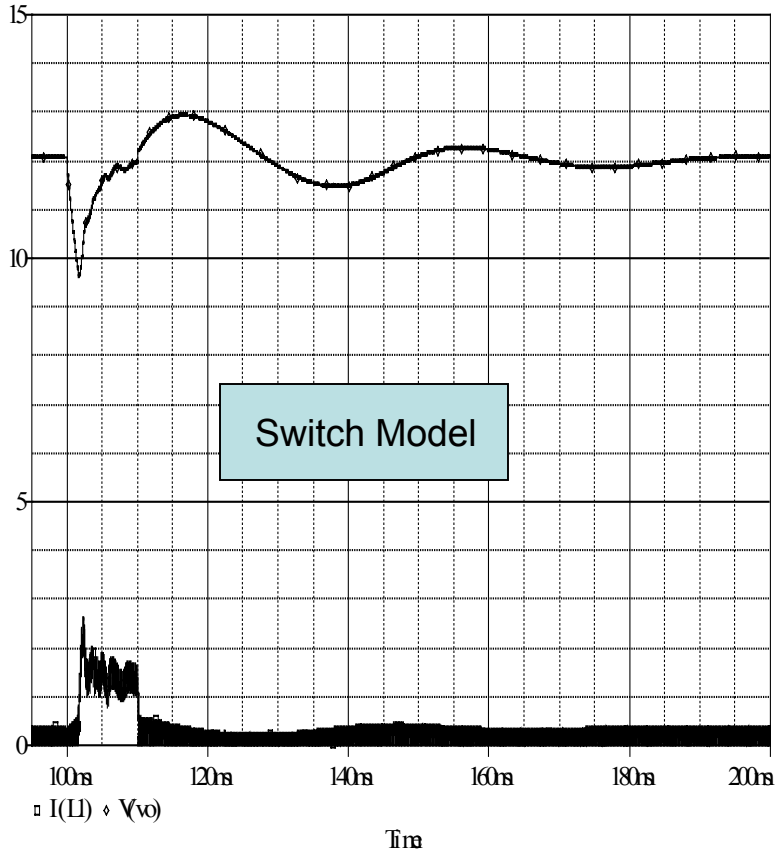
Buck Converter with Voltage Mode Control - Switch Model

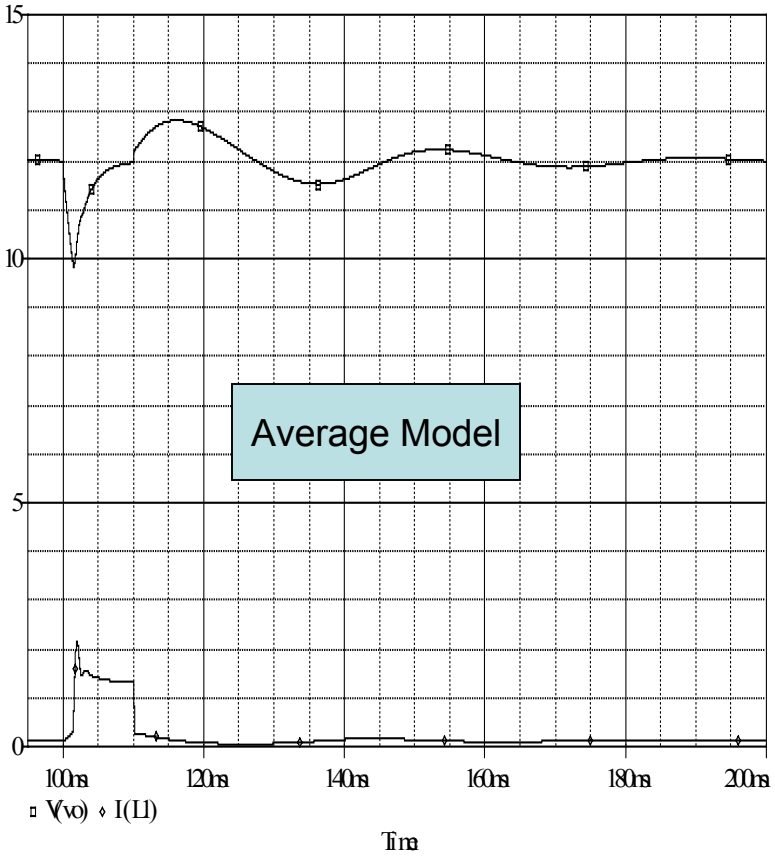
* Circuit file name: buck_conv_sw_fb_ctrl.sch
* Located in Pspice Tutorial Circuits folder.



Controlled Buck Dynamic Response - Average Vs Switch Models

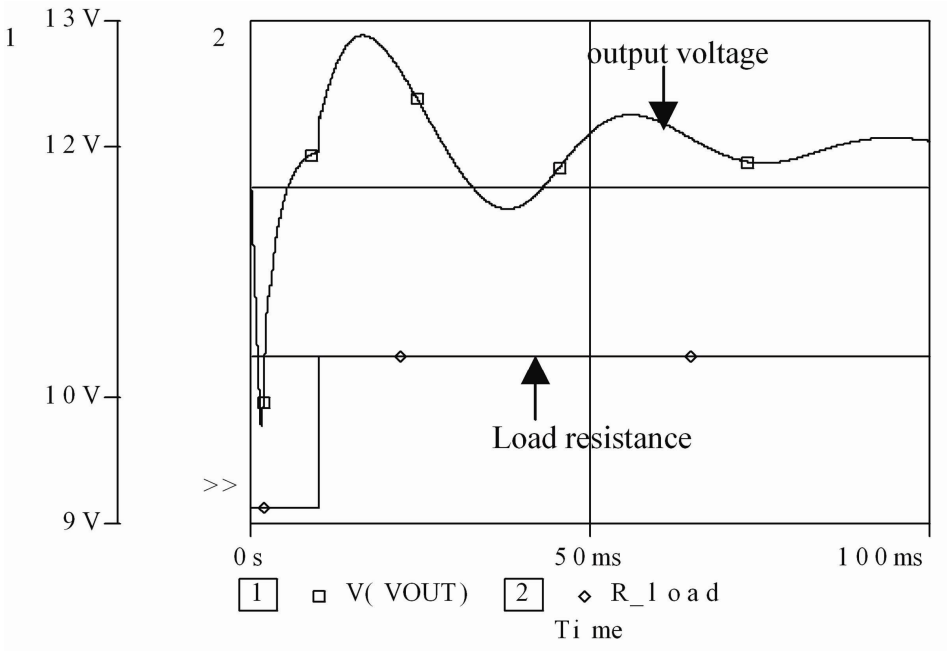
* Transient analysis of using switch model of PowerPole. 200 ms time window, 95 ms No_Print_Delay.
* 10 ohm load switched in parallel with 100 ohm load for 10 milliseconds at t = 0 and t = 100 ms
* Output voltage and inductor current versus time displayed below.



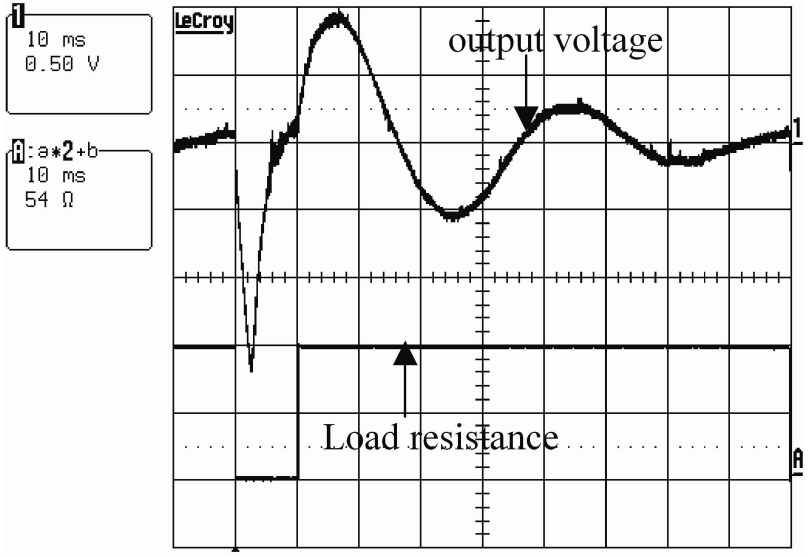


Buck Dynamic Response - Simulation Vs Experiment

Simulation result using average model of PowerPole.



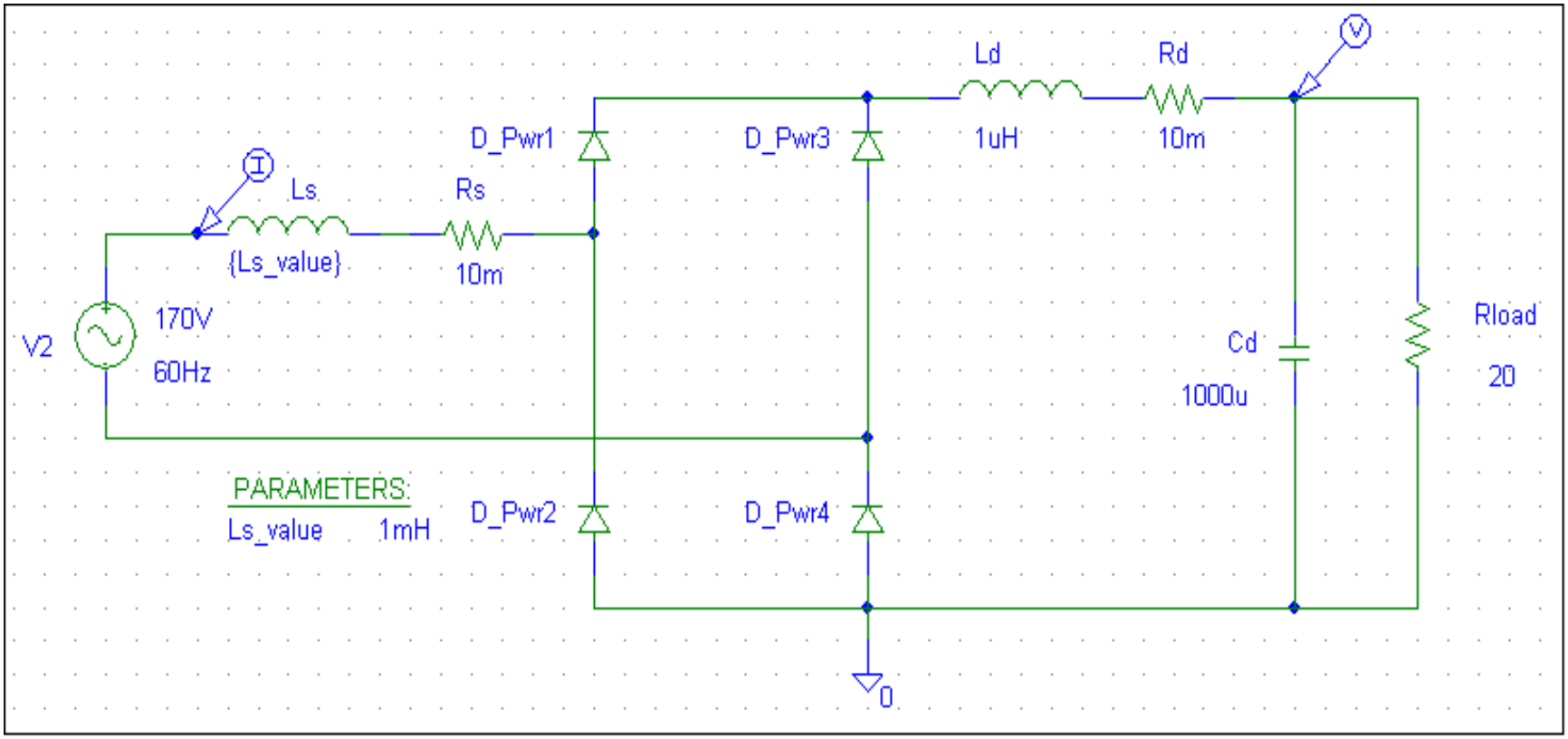
Experimental result using PowerPole circuit board



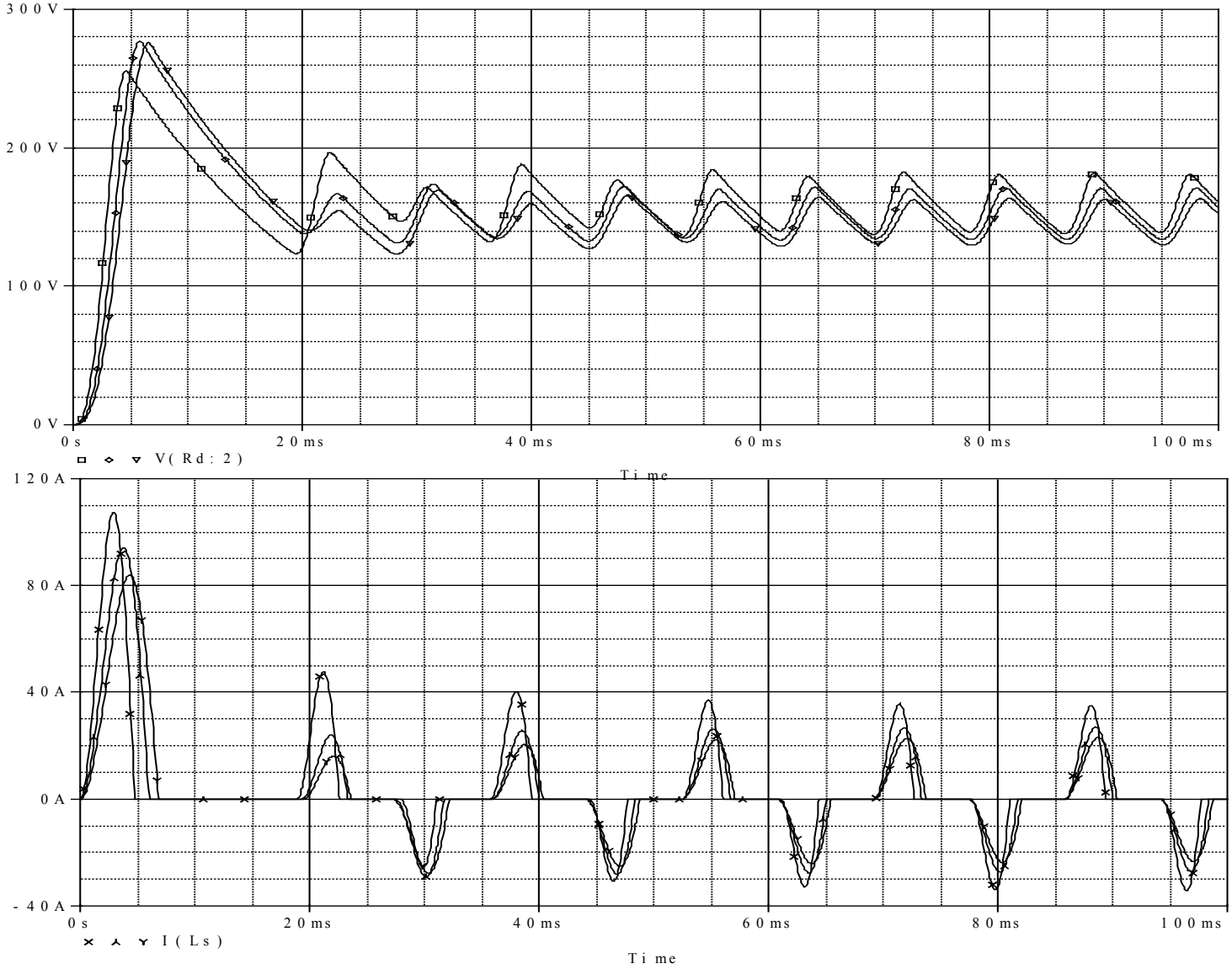
Diode Rectification

Single Phase Diode Rectification

* Circuit file name: DBrdg_Rect.sch. Located in Pspice Tutorial Circuits folder.
* Transient analysis. 100 ms time window.
* Parametric analysis with Ls = 1mH, 2 mH, and 3 mH.



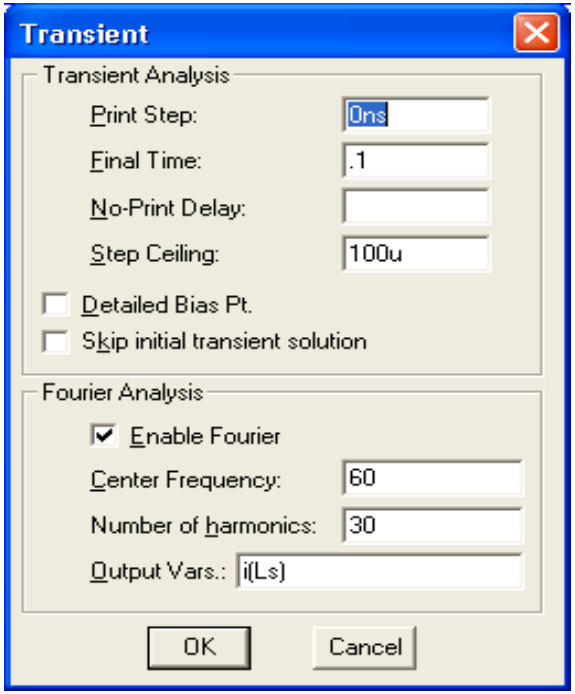
Diode Bridge Rectifier Outputs

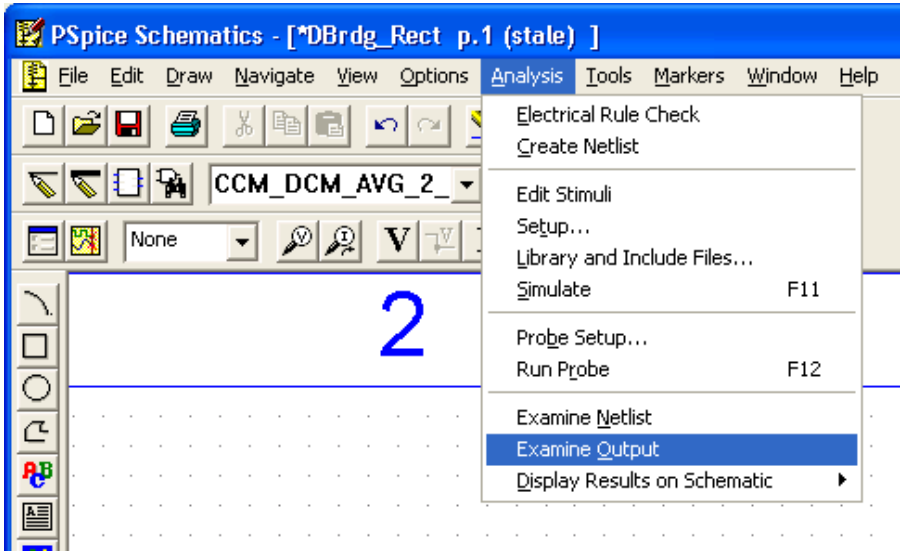


Output or load voltage

Current through source inductance (Ls)

Diode Rectifier Fourier Analysis - Total Harmonic Distortion





* Set up Fourier analysis in Transient window shown above.
* Uses the last 1/freq seconds of the simulation time window. (freq is the specified center frequency)
* View Fourier components of inductor current and total harmonic distortion by using Analysis pulldown menu in Schematics to access Output text file.

FOURIER COMPONENTS OF TRANSIENT RESPONSE I(L_Ls)

DC COMPONENT = 1.201188E-01

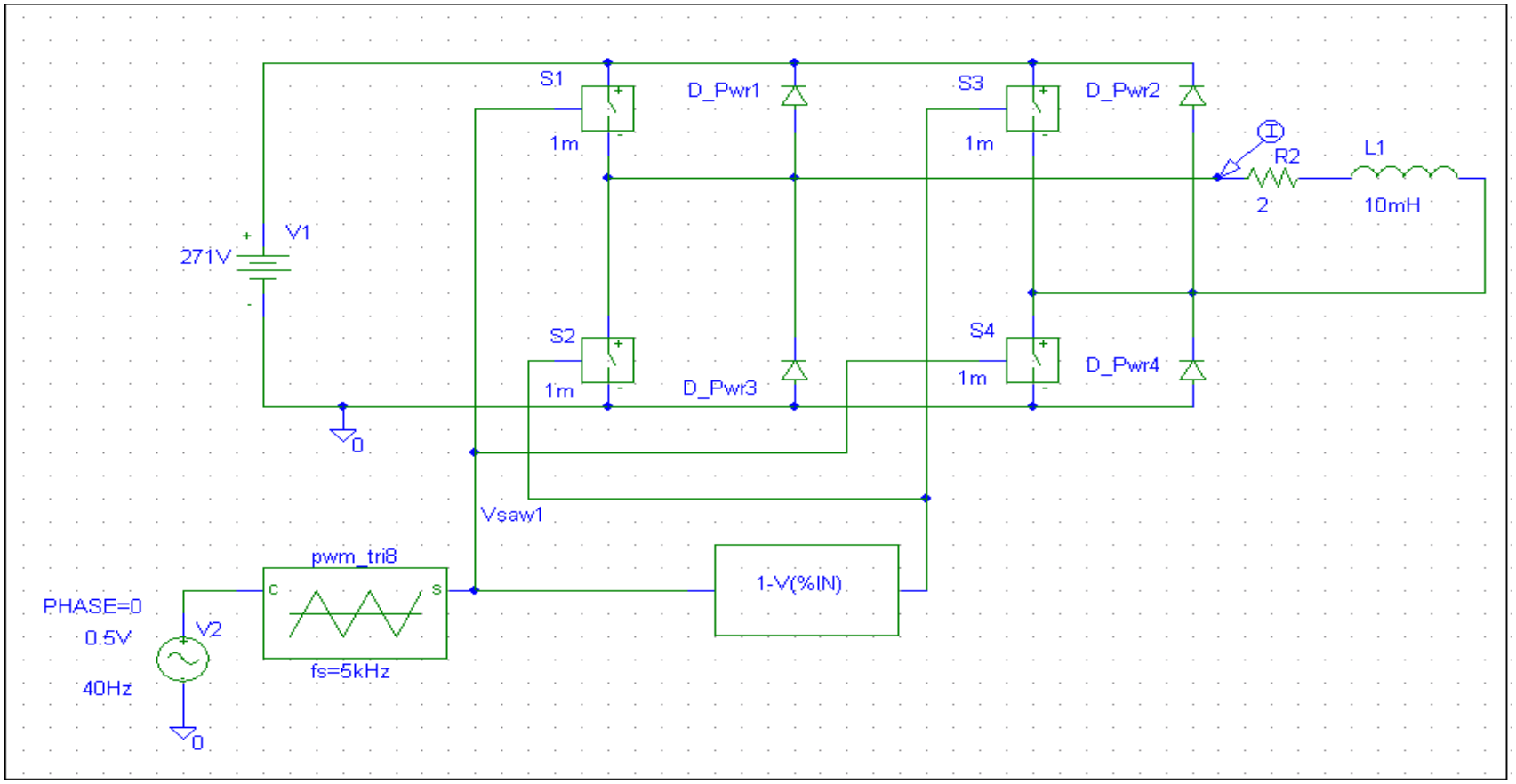
HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	6.000E+01	1.538E+01	1.000E+00	-1.005E+01	0.000E+00
2	1.200E+02	2.111E-01	1.373E-02	-9.199E+01	-7.190E+01
3	1.800E+02	1.175E+01	7.638E-01	1.489E+02	1.791E+02
-					
-					
29	1.740E+03	9.761E-02	6.348E-03	7.876E+01	3.701E+02
30	1.800E+03	2.230E-03	1.450E-04	3.908E+01	3.405E+02

TOTAL HARMONIC DISTORTION = 8.898523E+01 PERCENT

DC-to-AC Inversion

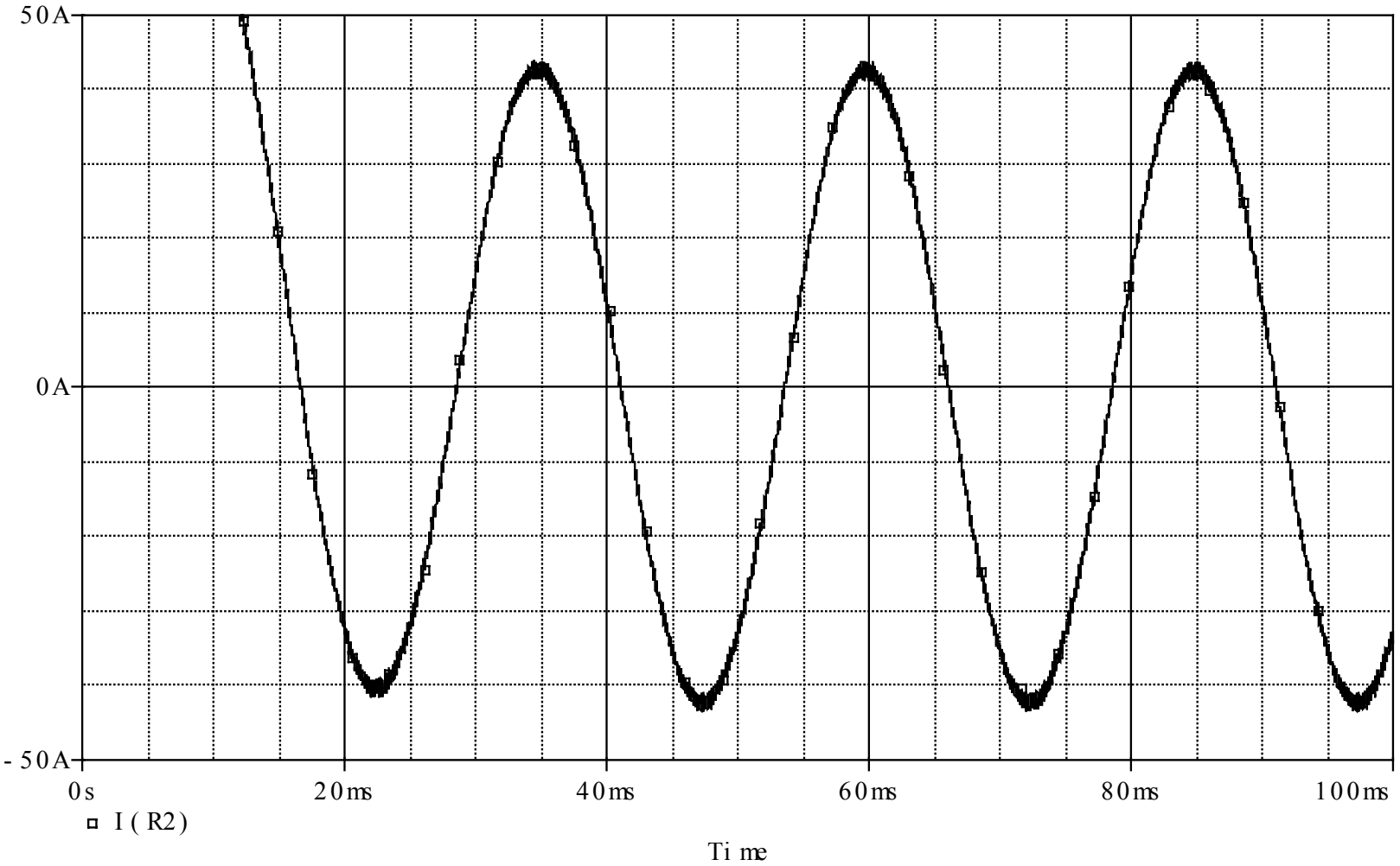
Single Phase Inverter

Single Phase DC-to-AC Inversion



* Circuit file name: Inverter_1PH_BP.sch. Located in Pspice Turtorial Circuits folder.
* Bipolar mode switching of inverter legs.

Single Phase Inverter Output Current



TOTAL HARMONIC DISTORTION = 6.489123E-01 PERCENT

Conclusions

1. Student version of PSpice is capable of simulating nearly all converter circuits of interest.

2. Both time domain and frequency domain simulation capabilities of PSpice useful for power electronic simulations.

3. Specialized component models for power electronics significantly simplify construction and simulation of various converters.

4. Wealth of detailed information available via advanced capabilities of Probe without necessarily running additional simulations.

5. PSpice learning curve not overly steep for acquiring a basic ability to use it.

6. PSpice or some other equivalent tool should be used in all power electronic courses.