Metallisation

Outline

- Introduction
- Applications of a metal
  - Gate
  - Interconnect
  - Contacts
- Metal Deposition

Properties of a Metal

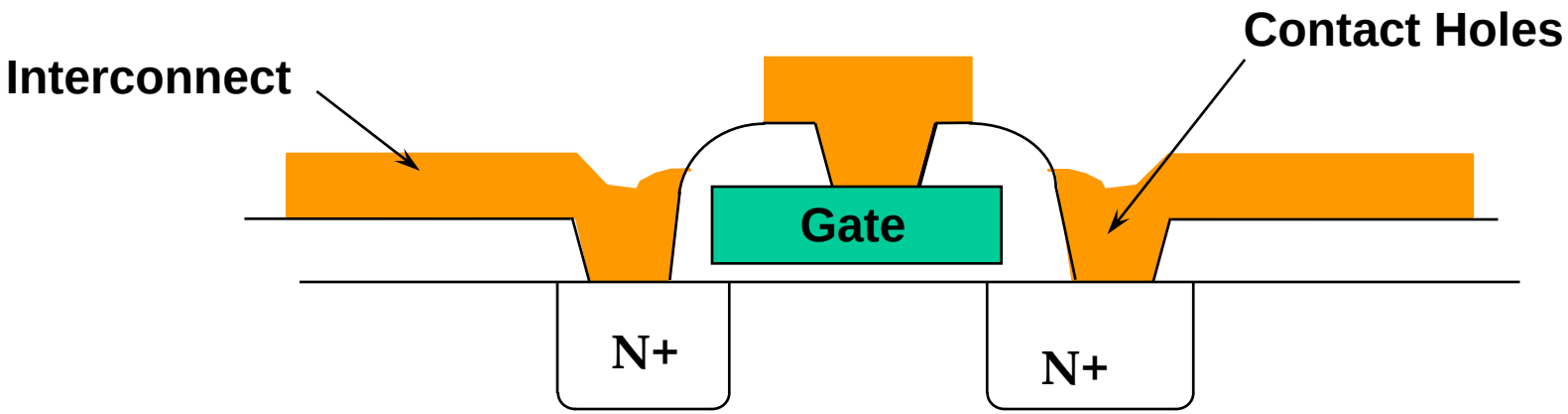
- Low Resistance
- Good adhesion
- Make good contacts
- Thermal stability
- Reliable over time

Metal Resistivity (μΩ.cm)

Cu	1.7- 2.0
Al	2.7 - 3.0
W	8 - 15
Ti	40 - 70
$TiSi_2$	13 - 16
$CoSi_2$	15 - 20
Poly	450 - 1000

Main Applications of metal

- Gate - used to control the devices
- Interconnect - used to connect up the devices
- Contact - make contact to the device

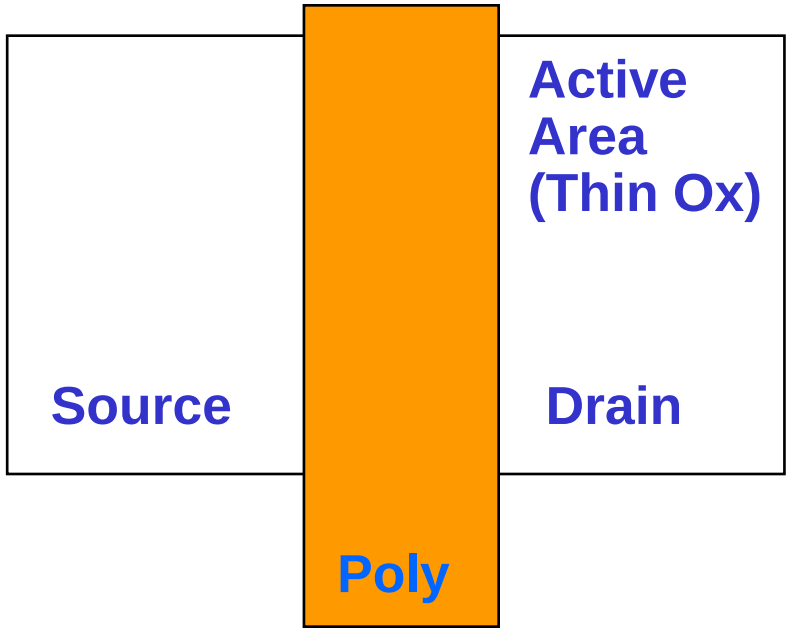


Application 1 : Gate Metal

- Originally one layer of metal performed all three functions
- However a metal gate is not suitable for complex designs due to design limitations, temperature restrictions and interactions between the metal and the underlying gate oxide
- Doped polysilicon is the most commonly used gate material (and first layer of interconnect)

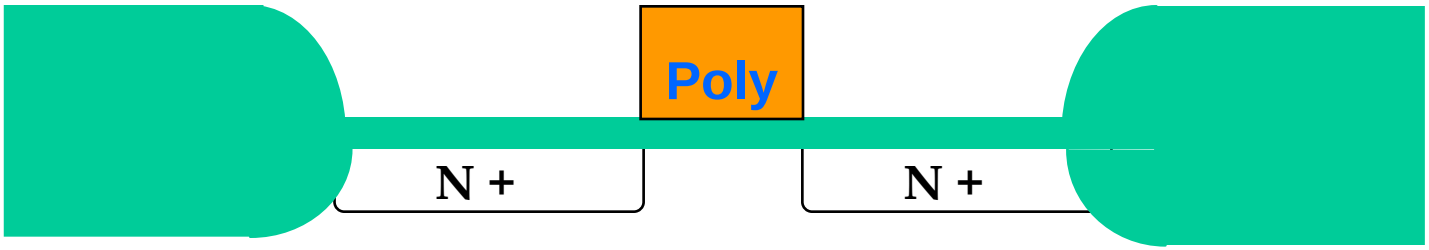
Polysilicon as a gate material

Plan View



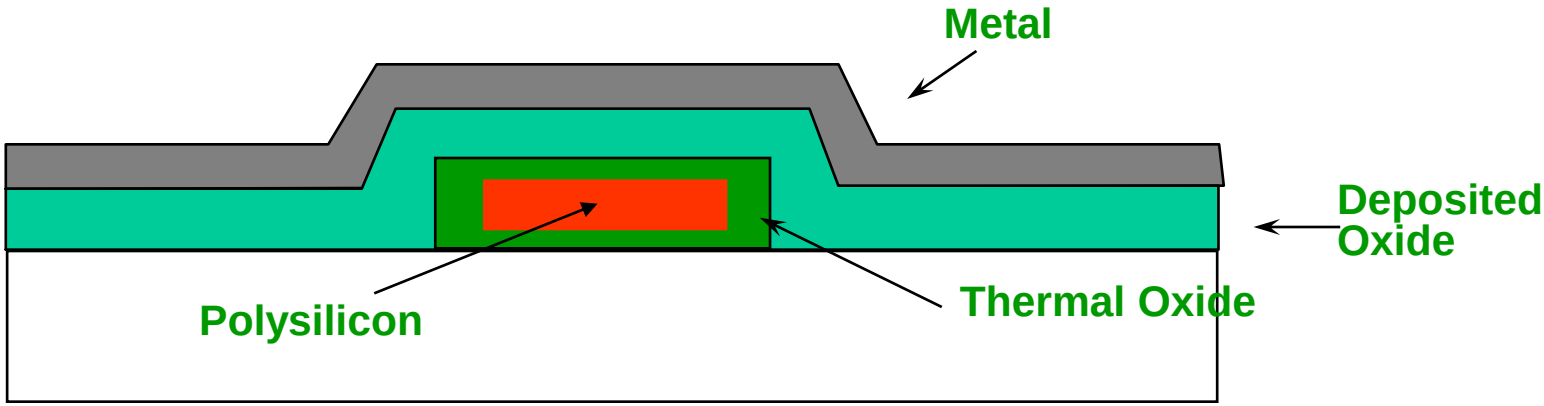
Thick
Field
Oxide

Cross section



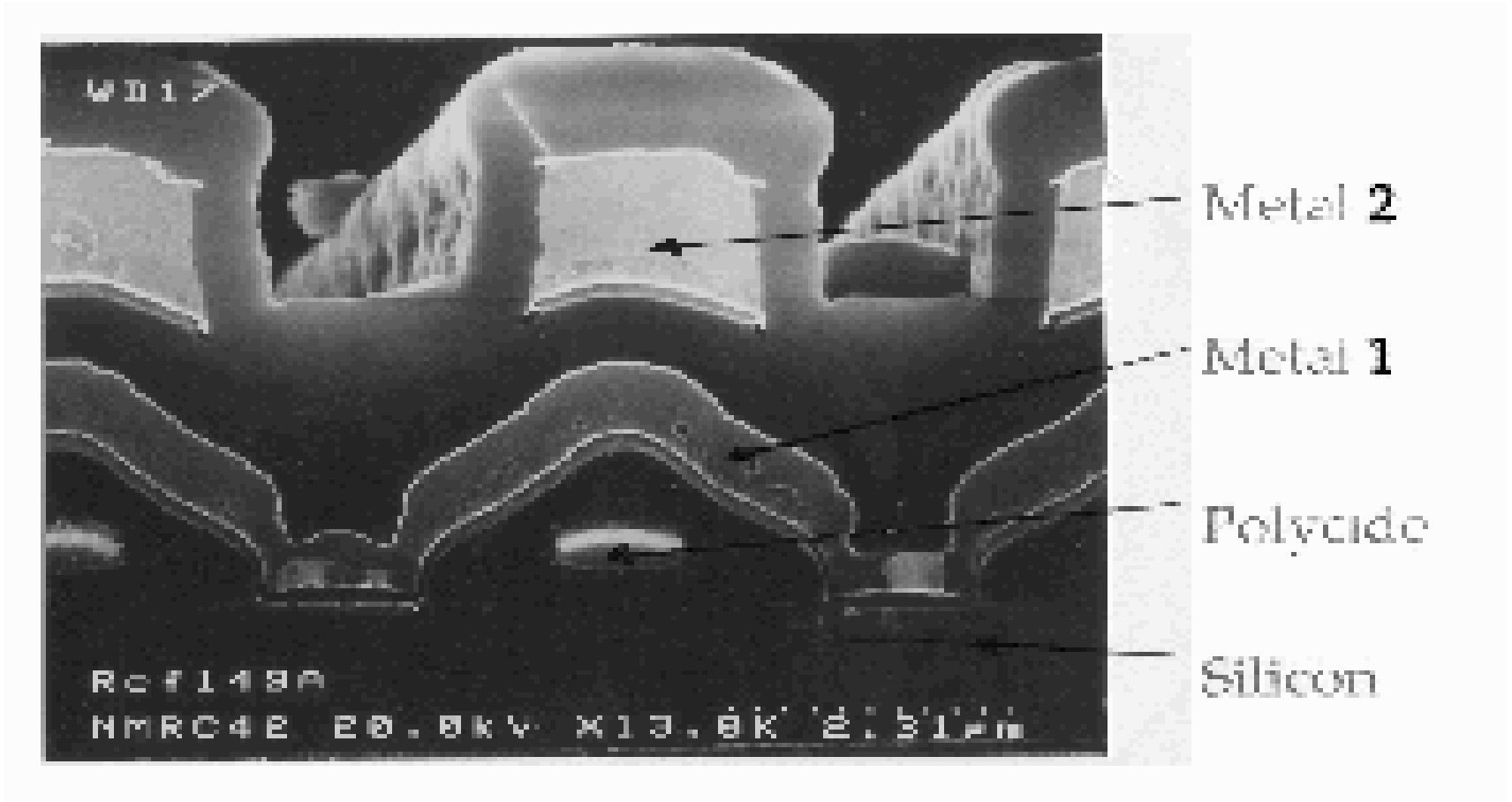
Metallisation

Application 2 : Interconnect metal



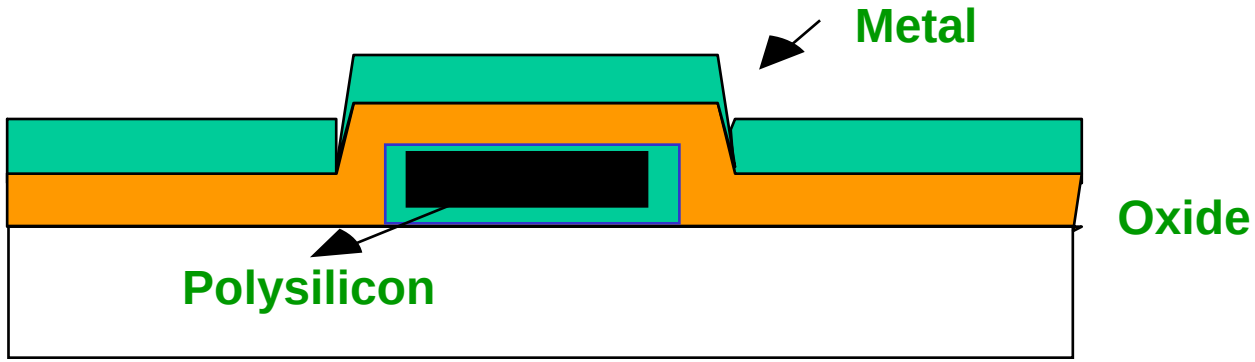
- Low resistance metal connects up the devices
- Polysilicon gate is isolated from the metal interconnect by oxide layers
- As the circuit becomes more complex single level metal is not sufficient and two to four layers of metal can be used

Double Level Metallization



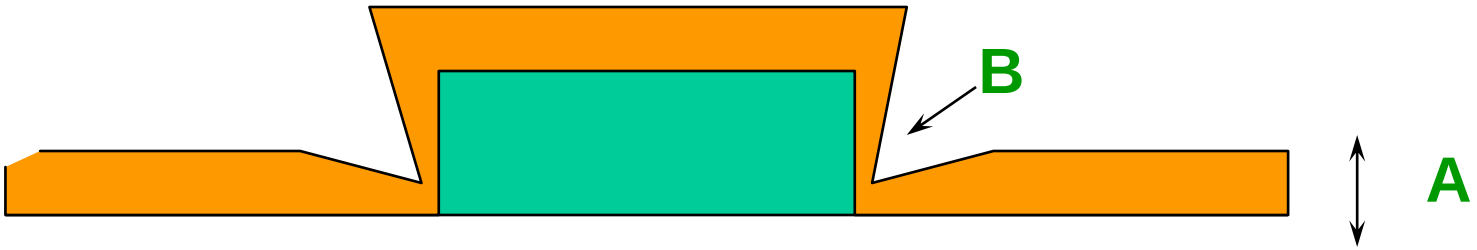
Interconnect Problem 1

Step Coverage



- If the dielectric is conformal then it may be difficult for the metal to remain continuous over sharp edges
- The dielectric should be planarised to ensure good metal step coverage

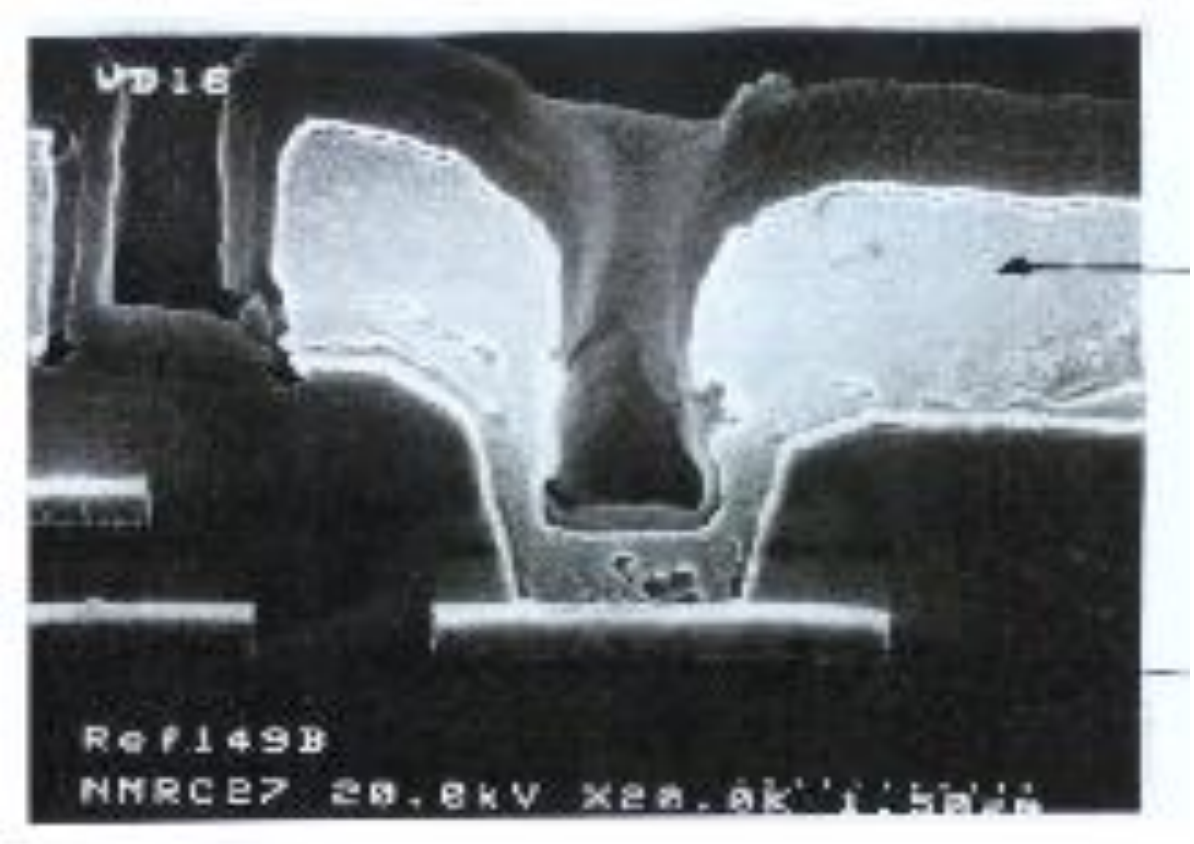
Definition of step coverage



- **Step Coverage % = B/A**
  0.5µm/1.0µm = 50%

Example :

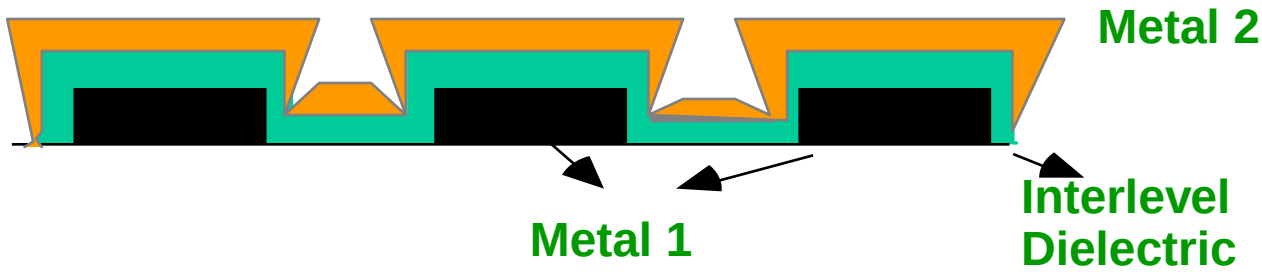
Single Level Metallization



Metal

Polycide

Planarisation



Unplanarized Double Level Metal Scheme

Planarized Metalization Scheme

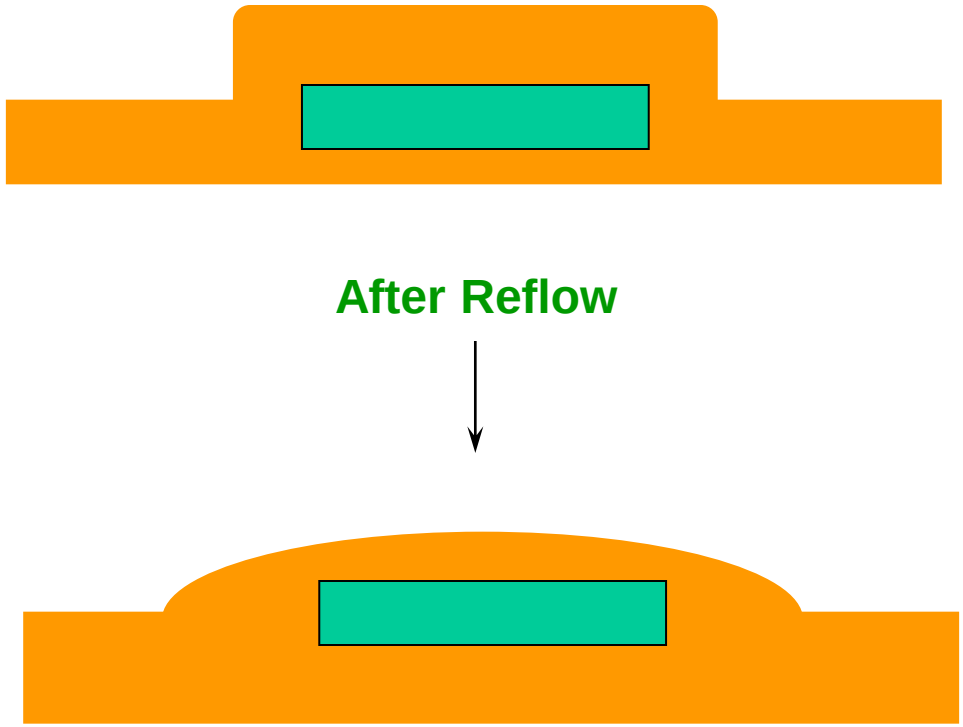
Metallisation

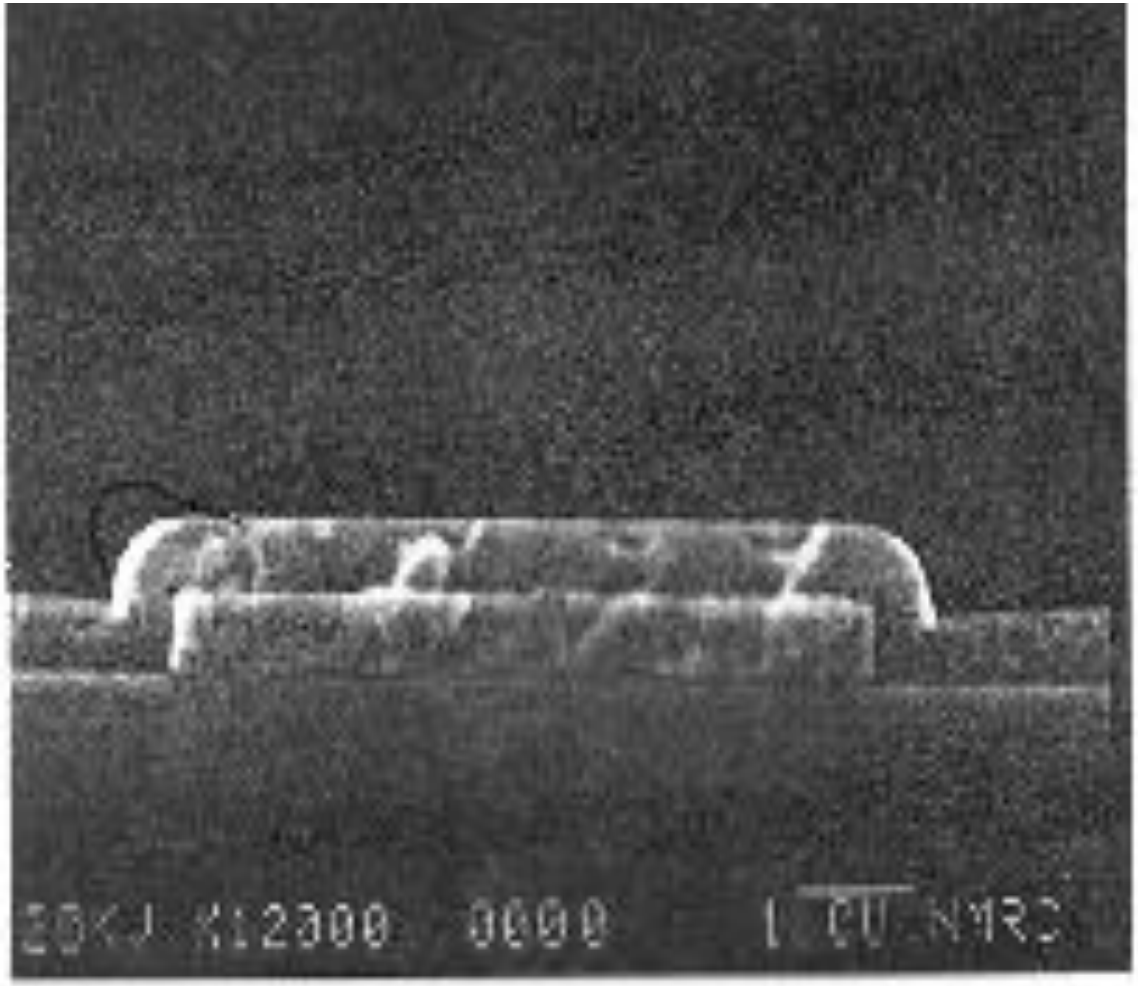
Planarisation Techniques

- **High Temperature**
  - **Reflow**
- **Low Temperature**
  - **Spin On Glass**
  - **Resist Etch Back**
  - **Chemical Mechanical Polishing**

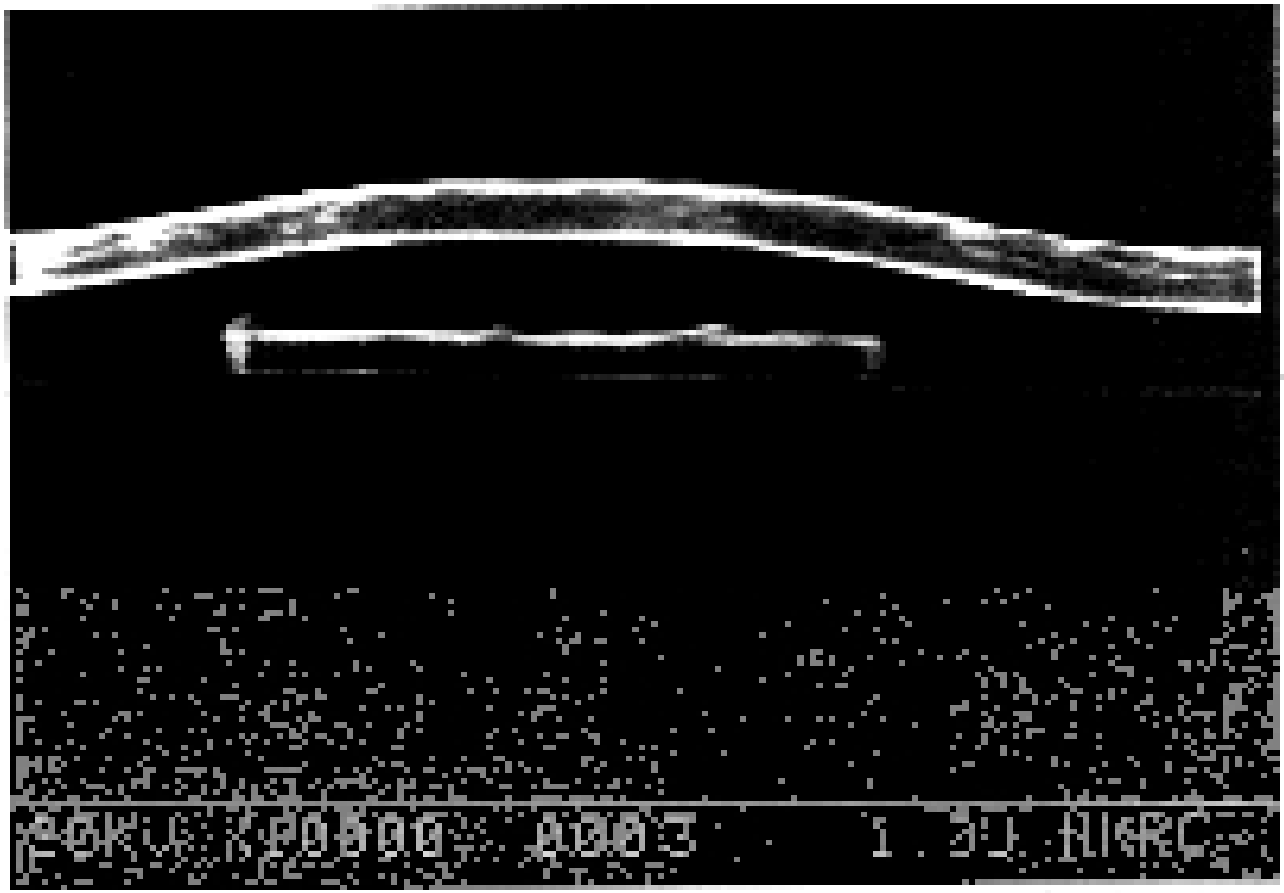
Reflow

- High Temperature anneal of doped oxide





Metallisation



Metallisation

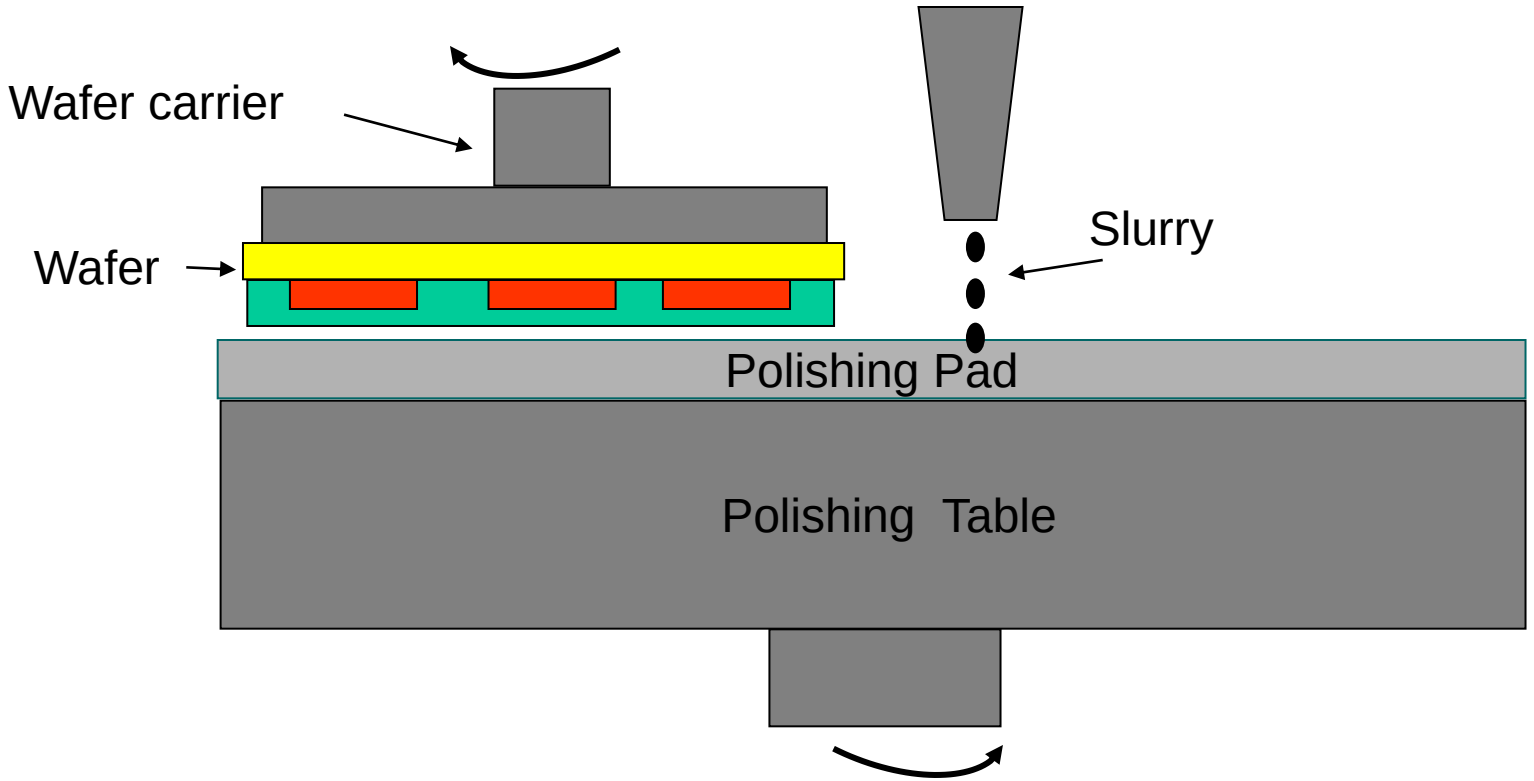
Spin On Glass (S.O.G.)

- Deposit Oxide

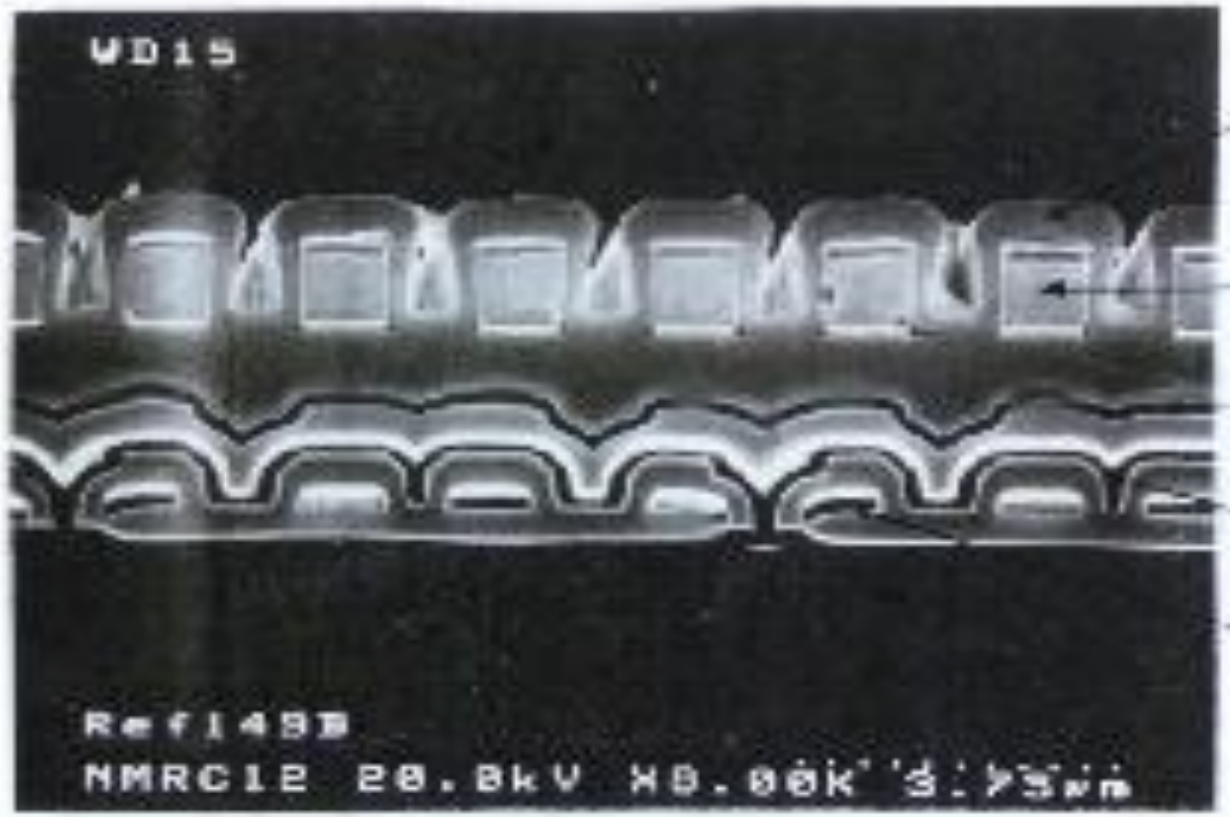
- Spin on SOG

- Etch back SOG

Chemical Mechanical Polishing



Interlevel Planarization



Passivation

Metal

Polysilicon

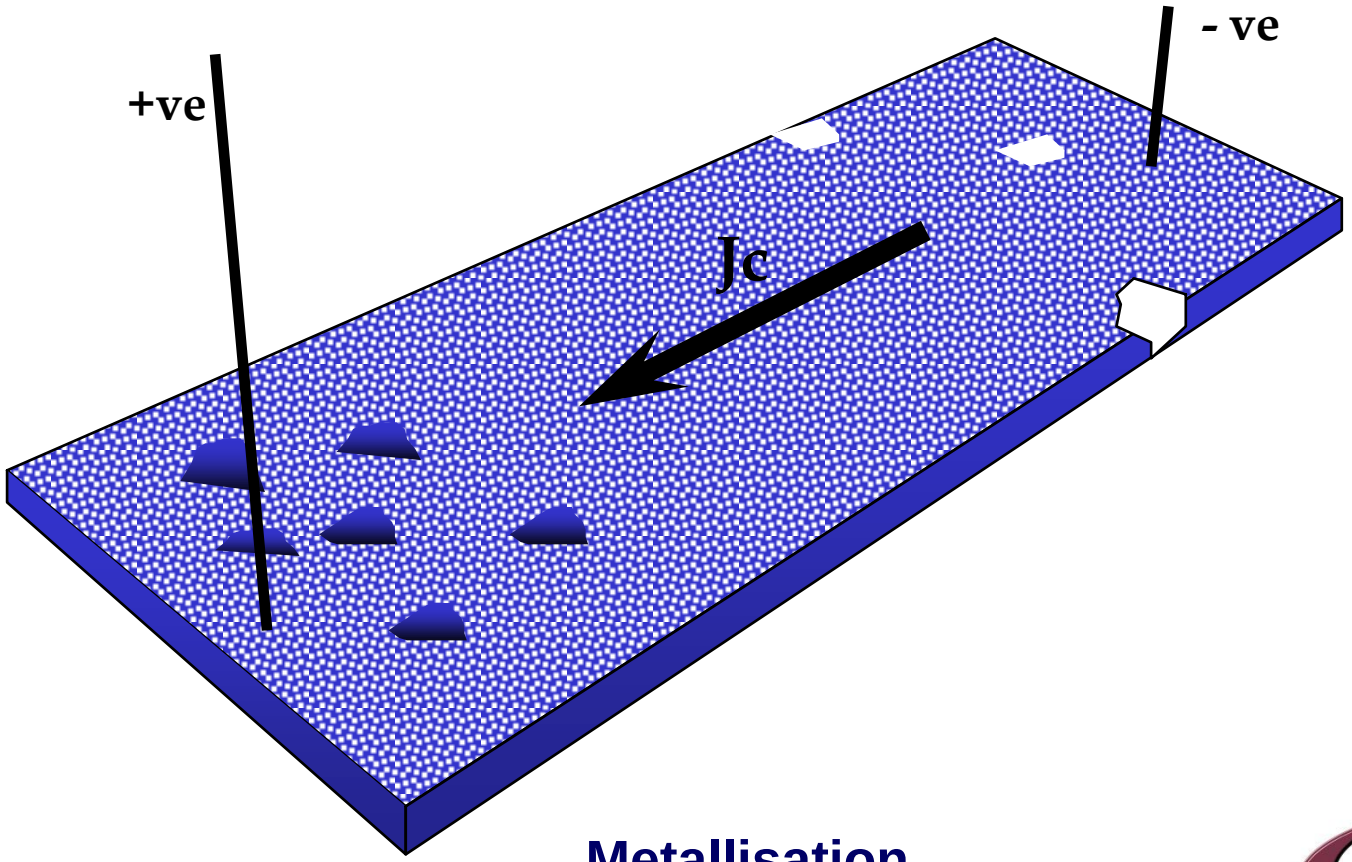
Polycide 2

Polycide 1

Metallisation

Interconnect Problem 2
Electromigration

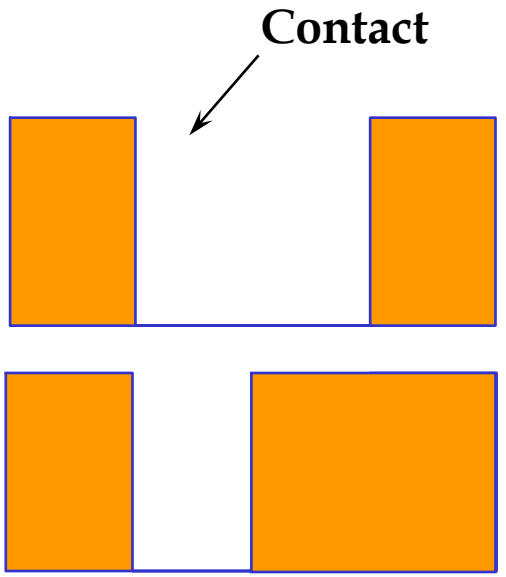
Mass transport of the metal due to high current density in the metal



Metallisation

Application 3 : Metal in Contacts

- Potential problems
  - Step coverage
  - Spiking
  - Contact Resistance
- Problem is worse as aspect ratio increases
  - AR = Depth : Width



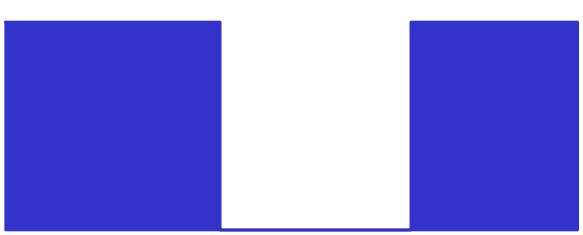
Contact Problem 1 : Step Coverage into Contacts

- It is difficult for the metal to remain continuous when it is deposited into small contact holes

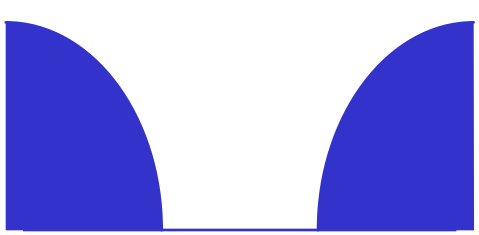
- Three main solutions
  - Alter the shape of the contact
  - Use another metal to fill the contact
  - Change the deposition conditions

Step Coverage in to Contacts

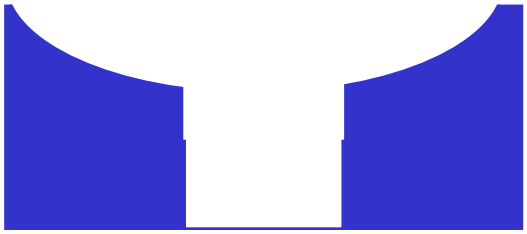
1. Alter the shape of the contact



Anisotropic Etch

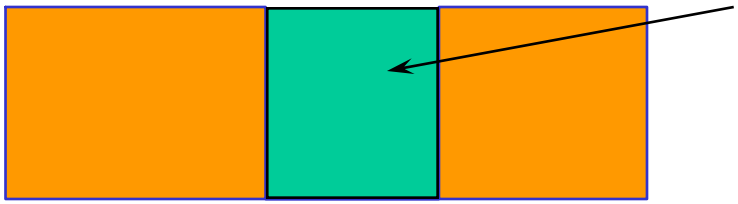


Tapered Etch



Champagne Etch

2. Use a contact fill



Example : CVD Tungsten

Metallisation

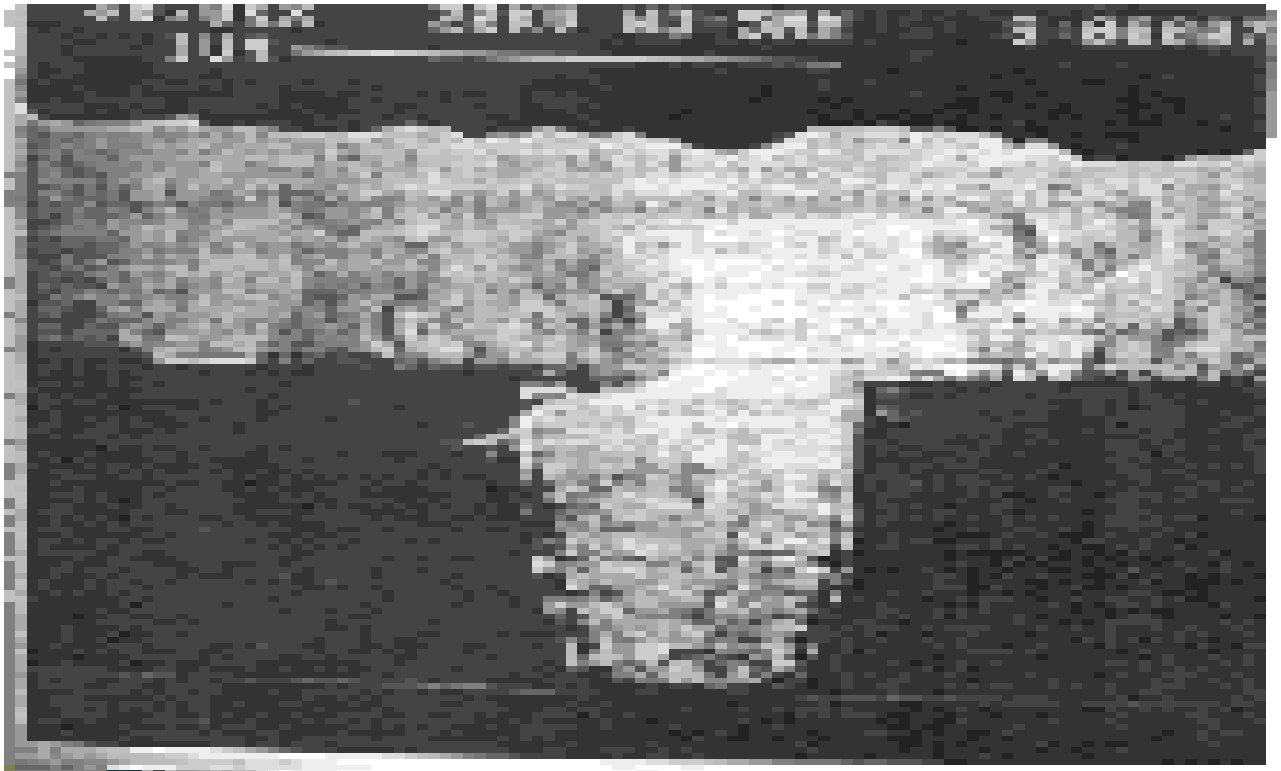
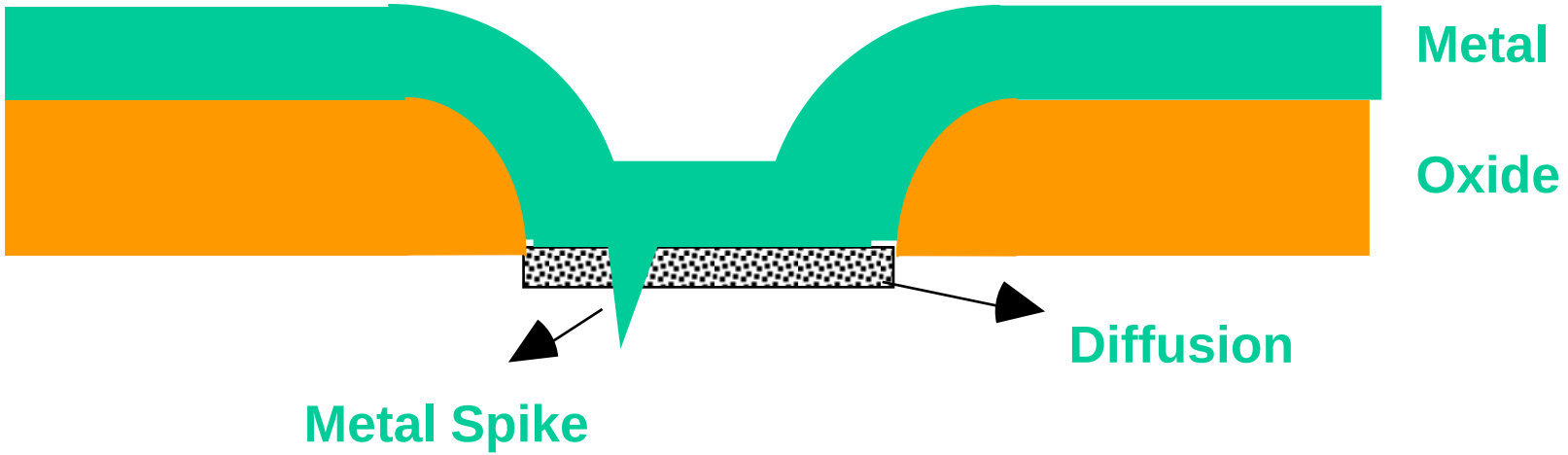


Fig. 2: LPCVD TiN adhesion layer with tungsten metal

Metallisation

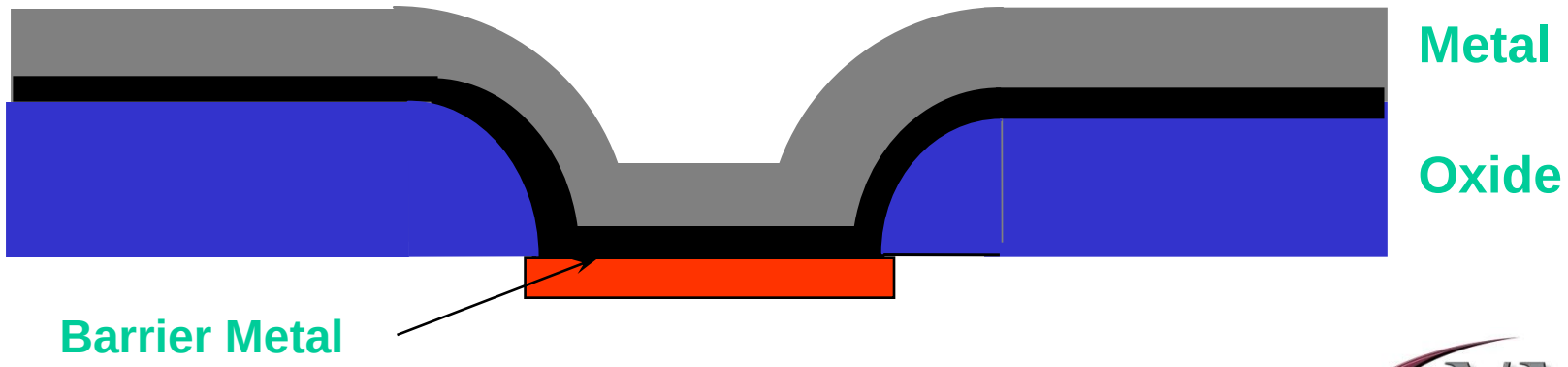
Contact Problem 2 - Spiking

- Silicon dissolves in Al and the Al moves into the Si to fill up the void



Spiking Solutions

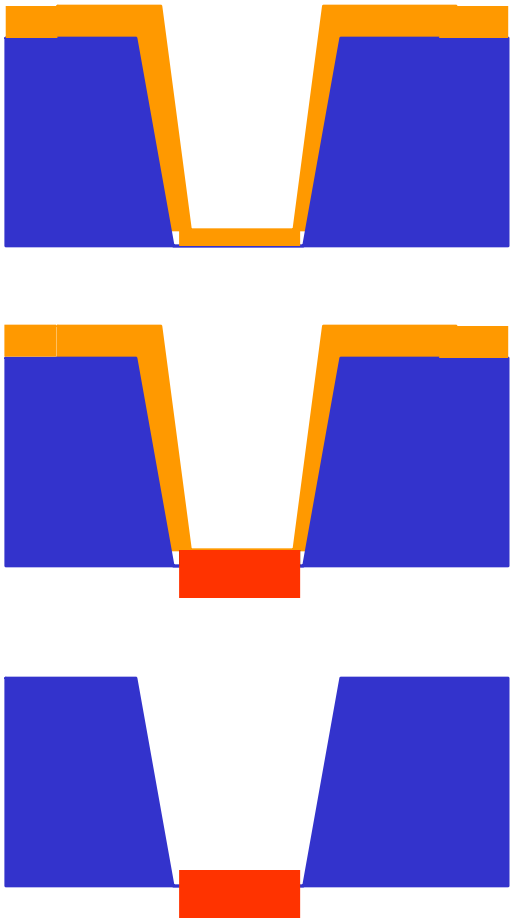
- Add small amounts of Si to the Aluminium to prevent the Si being absorbed. (equilibrium at 2%)
- Use a barrier to prevent the Aluminium / Si interaction
  - TiW and TiN are the most common barriers used



Contact Problem 3
Contact Resistance

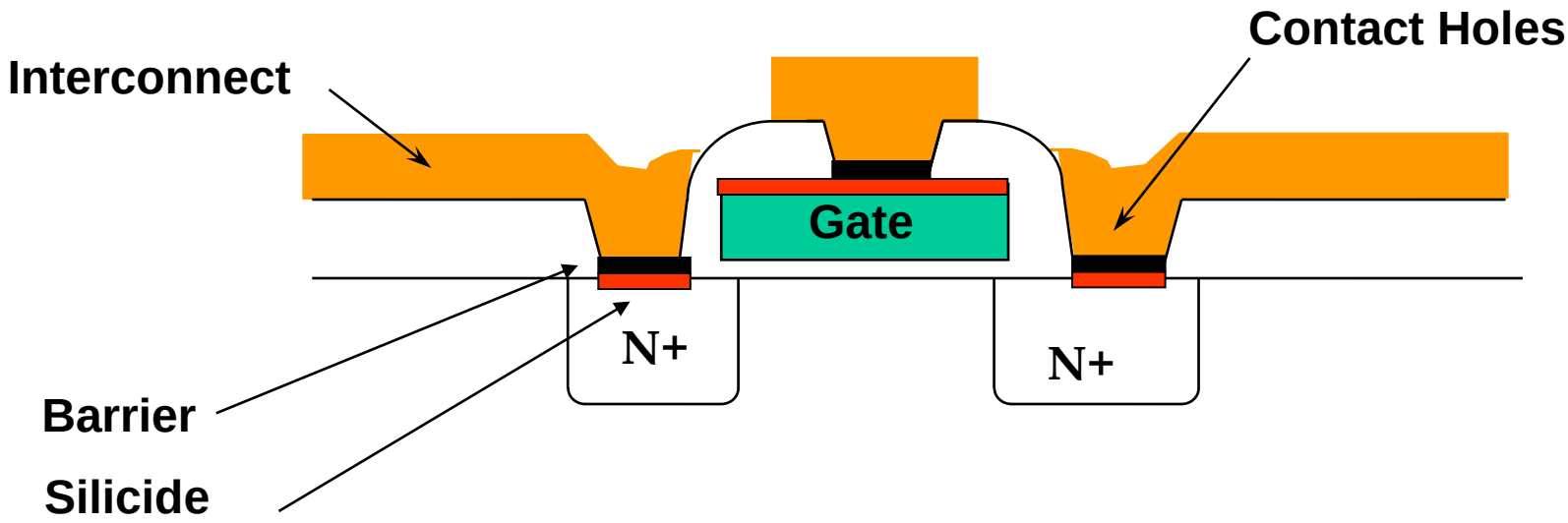
- The resistance between the metal and the Silicon must be kept as low as possible
- This can be achieved by forming a silicide in the contact
- Refractory metals are the most common metals used for silicide (eg: $TiSi_2$, $CoSi_2$)

Silicide formation in a contact



- Deposit metal eg: Titanium
- Low temperature anneal
  - Ti reacts with Si not SiO_2
- Remove unreacted Ti and anneal to form stable $TiSi_2$

Silicide in a transistor

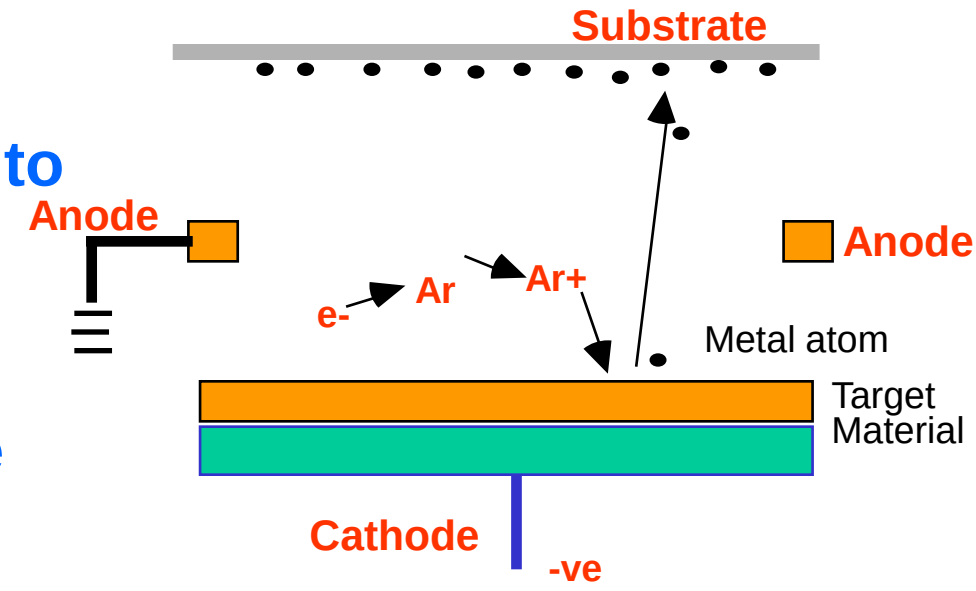


Metal Deposition

- The most common deposition technique is sputtering down to about the 180nm node
- After the 180nm node a copper damascene process is used
- Sputtering is a physical process that takes place in vacuum chamber
- A vacuum of ~ 10-7T is achieved after the wafers are loaded (base pressure)
- Argon gas is introduced to a pressure of ~ 10-3T
- This pressure is maintained by balancing the gas inlet rate and the pumping rate

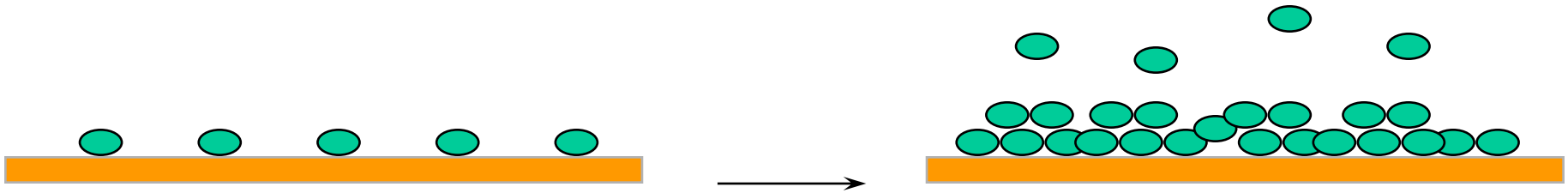
Sputtering Principle

- Electrons leave the target and collide with the gas atoms
- Positive ions are created
- The gas ions are attracted back to the negative target where they collide with it
- Metal atoms are knocked off the target and travel across to the wafer surface



FILM GROWTH

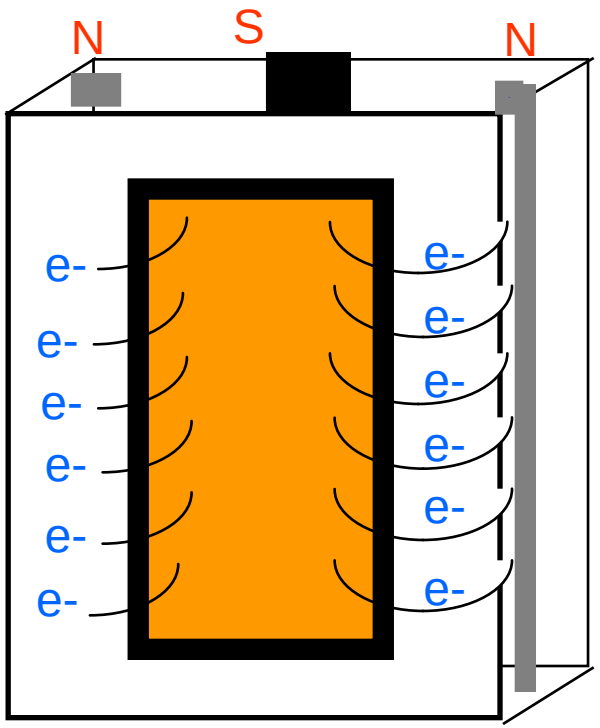
- The first atoms act as nucleation sites on the surface
- Subsequent atoms grow around them in cluster type formation until a continuous layer is formed



Magnetron Sputtering

- There are two problems in a non-magnetron system
  - (1) If electrons leaving the target reach the wafer the wafer can become very hot
  - (2) A very large voltage must be applied to the target to ensure there are a sufficient number of electrons
- Permanent magnets are placed behind the target and the magnetic field acts to keep the electrons close to the target surface

Magnetron Sputtering



DC Magnetron Sputtering Cathode

Damascene Metal Processing

- Small geometry semiconductor manufacturers are moving away from Al/Si - SiO2 processes to Copper - Low k Dielectric processes
- Copper is a difficult metal to etch - the process used to over come this difficulty is the “Damascene” process
- In the process where the vias or contacts to the underlying transistors or another layer of metal are cut at the same time as the metal, it is known as “Dual Damascene”

Trench Cut in Dielectric Layer

2-D

3-D

Metallisation

Deposit Barrier/Seed Layer

These are usually two separate materials

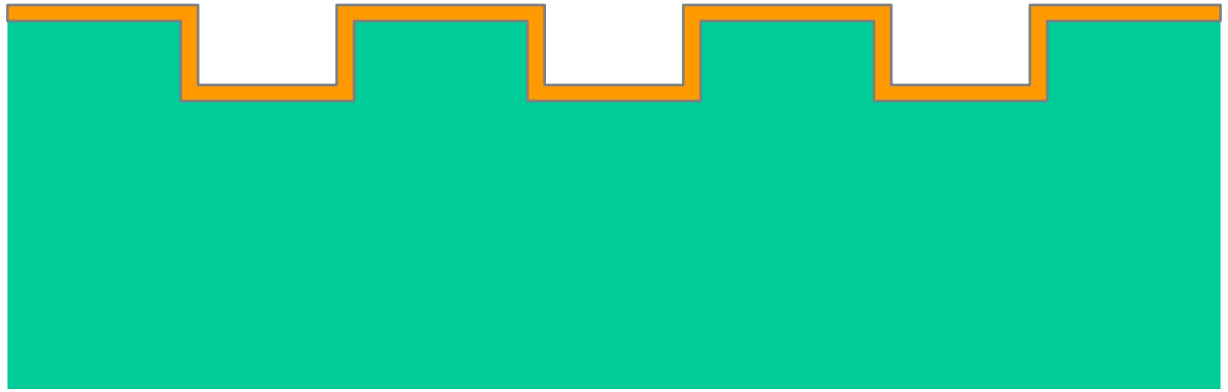
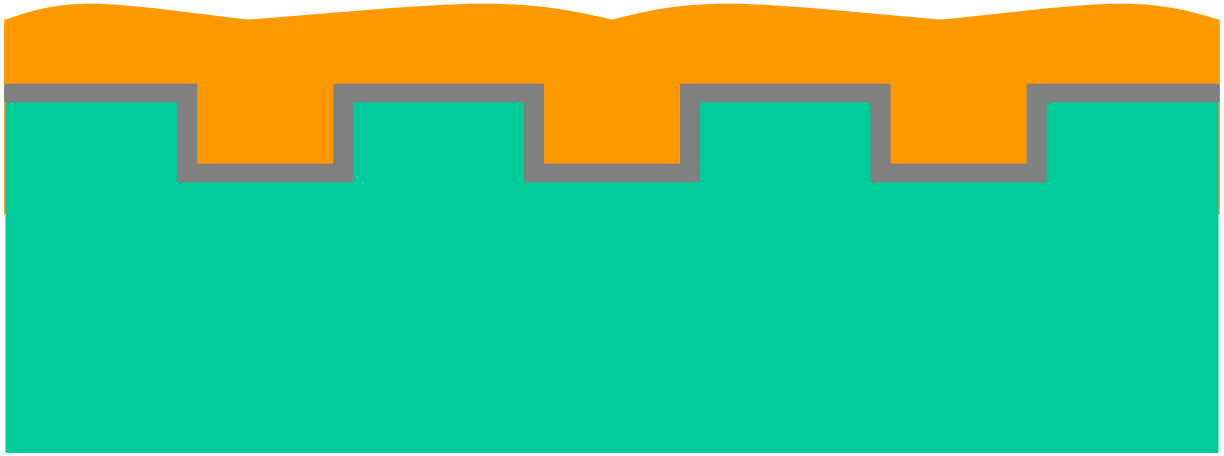
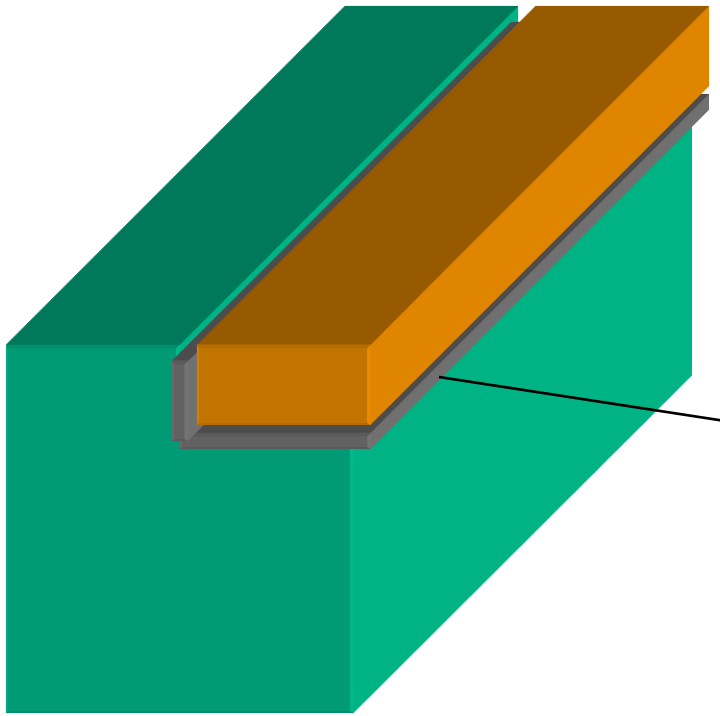


Plate with Copper



CMP the Copper and the Barrier Layer

Exploded View



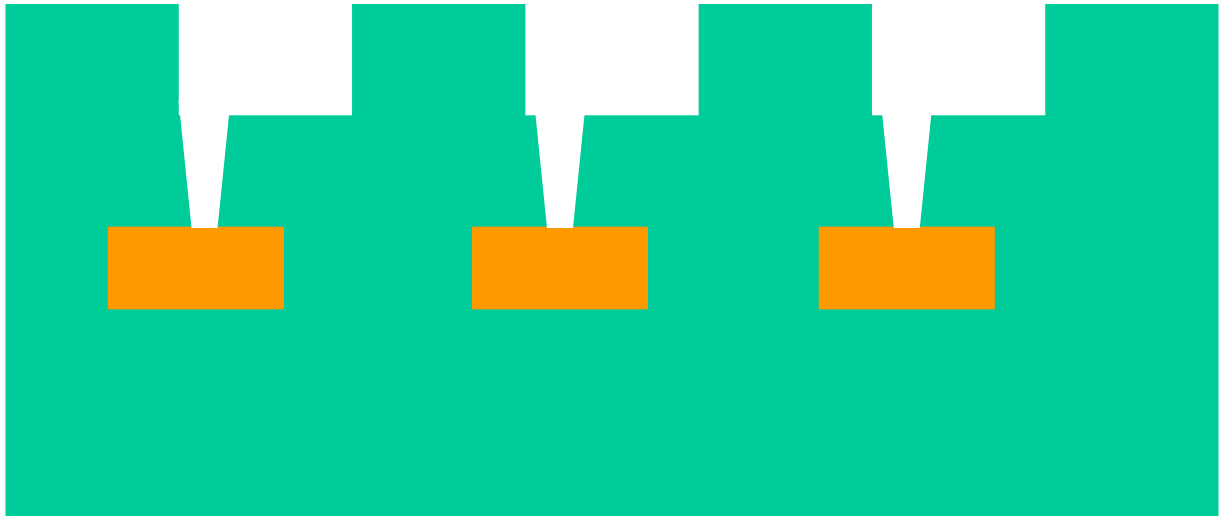
Metallisation

Dual Damascene

Tracks for second metal layer are cut (etched) in the dielectric

Dual Damescene Vias

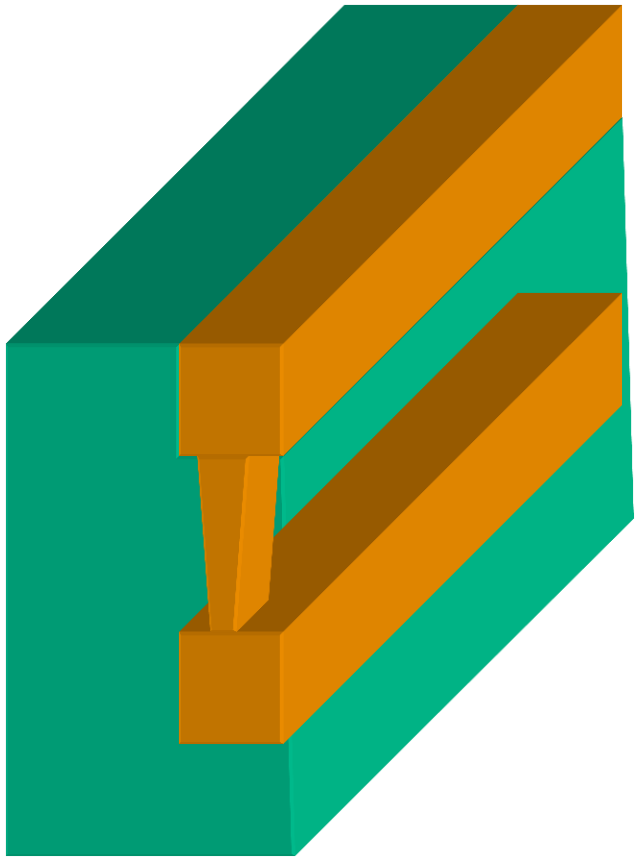
Vias are then opened down to the first layer of metal



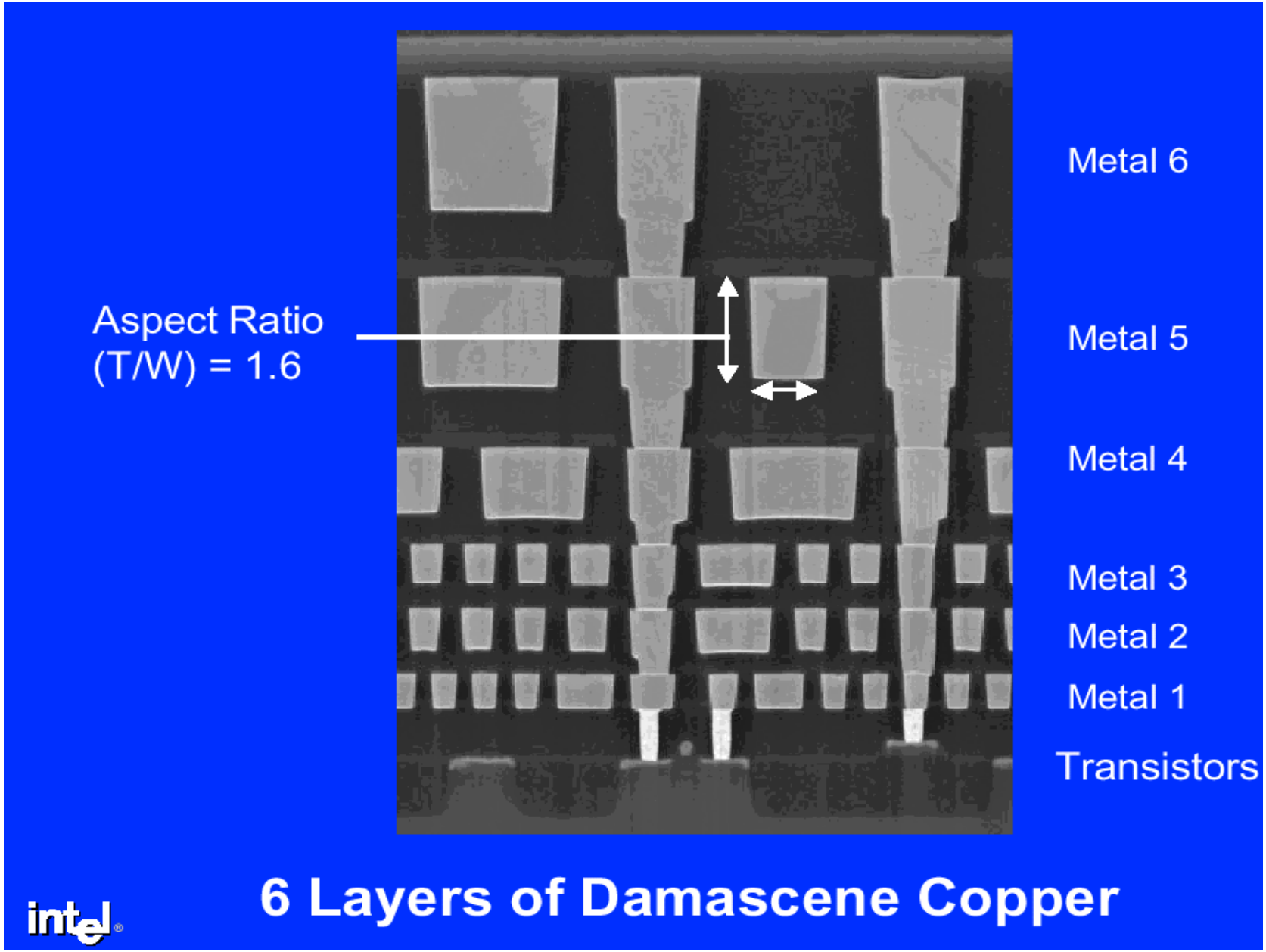
The Dual process can be done as a “Via First” or as a “Trench First Process”

Dual Damascene Exploded View

The barrier/seed layer is left out for the sake of clarity



Metallisation


Aspect Ratio
(T/W) = 1.6
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Transistors
intel
6 Layers of Damascene Copper

Damascene Copper Interconnects

intel

Interconnect Summary

- Copper was introduced to MPUs at the 220nm node
- For very high speed DRAMs Cu will also be used but in the main DRAM will not use Cu until the 100nm node
- It is necessary to get beyond the 2.2μΩ-cm effective resistivity characteristic of barrier/Cu
- Solutions <100nm
  - Reduction of operating temperature to allow the use of super conducting material
  - Optical interconnect

Sheet Resistance

$R = \rho L/A$

A is the cross-sectional area.

ρ is the material resistivity.

L is the length.

$R = \rho L/t.W$

$R = \rho/t \; L/W$

ρ/t is the sheet resistance,

is always given as ohms/square

because L/W is the number of squares.

It should actually be ohms

because L/W is dimensionless.

$R_s = \rho/t$

$\rho = R_s.t$