OLLSCOIL NA hÉIREANN
THE NATIONAL UNIVERSITY OF IRELAND

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

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2009 Engineering (Electrical & Electronic) Examination

Microelectronics (UE4008)

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Time allowed **1 ½ Hours**
Answer three out of four questions

Approved calculator permitted.

Question 1:

a) With the aid of diagrams describe how certain elements of a MOS transistor have changed in the shrink from processes with minimum dimensions of about 1.0μm to processes with dimensions in the region of 45-65nm. Give a very brief explanation for the technological reasons for these changes. (Hint: concentrate on the "Gate Stack" and substrate.)

b) In the shrink from 65nm to 45nm a company changes the gate dielectric to hafnium oxide with a dielectric constant of 25, if the resultant gate capacitance is 3.0×10^{-6} F/cm^2 what is the actual new dielectric thickness and the silicon dioxide equivalent?

Given:
The permittivity of free space is 8.86×10^{-14} F/cm
The dielectric constant of silicon dioxide is 3.9

Question 2:

a) Describe a physical model for the thermal oxidation of silicon.

b) Describe what happens to dopant in the silicon during the thermal oxidation cycle if:
   i) The segregation co-efficient is less than 1,
   ii) If the segregation coefficient is greater than 1.

c) A silicon <100> wafer, which had been patterned for ion implant with 50nm of oxide in the windows to be implanted and 1.0μm in the other areas to protect against the implant, is put through a thermal oxide process at 1000°C in pyrogenic steam for 3 hours, what is the final oxide thickness in:
   i) The areas which had 50nm on the surface prior to oxidation?
   ii) The areas which had 1.0μm on the surface prior to oxidation?

Question 3:

a) Describe the Reactive Ion Etch process, outlining parameters that effect the process and describing the equipment used

b) Describe how polymer formation in RIE can assist the anisotropic etch of aluminium alloys, outline problem(s) associated with this etch.

c) Using a linear etch model for a silicon etch with Photoresist as a masking material, where;

Etch Rate = **R**

$$R = \frac{\left(S_c K_f F_c + K_i F_i\right)}{N}$$

S_c = Sticking coefficient (.01), K_f = (.02) and K_i = (1) are the relative rate constants for the two processes

F_c = (2.5 x 10^{18} atoms cm^{-2}s^{-1}) and F_i = (1 x 10^{16} atoms cm^{-2}s^{-1}) are the chemical and ion fluxes,

N is the density = (5 x 10^{22} atoms/cm^3)

How deep is the silicon etched in the vertical direction well away from the mask edge, and in a lateral direction under the mask edge, if the etch time is 5 minutes?

Question 4:

a) Describe in terms movement of holes and electrons the operation of an NMOS transistor as the gate voltage is swept from 0V to a voltage greater than the threshold voltage. Assume the source is grounded and there is a small positive voltage on the drain. What effect will the application of a reverse bias to the substrate or bulk have on the device?

b) By how much will the threshold voltage shift in an NMOS transistor if a 1.0V reverse bias is applied to the substrate at a measurement temperature of 27°C?

Given:

Substrate doping =1 x 10^{15} atoms cm^{-3}

ε_o = 8.86 x 10^{-14} F cm^{-1}

k_s = 11.7

n_i = 1.45 x 10^{10}cm^{-3}

q = 1.602 x 10^{-19} Joule

C_{ox} = 1.4 x 10^{-8} F cm^{-2}

k = 1.38 x 10^{-23} JK^{-1} (Boltzmann’s constant)