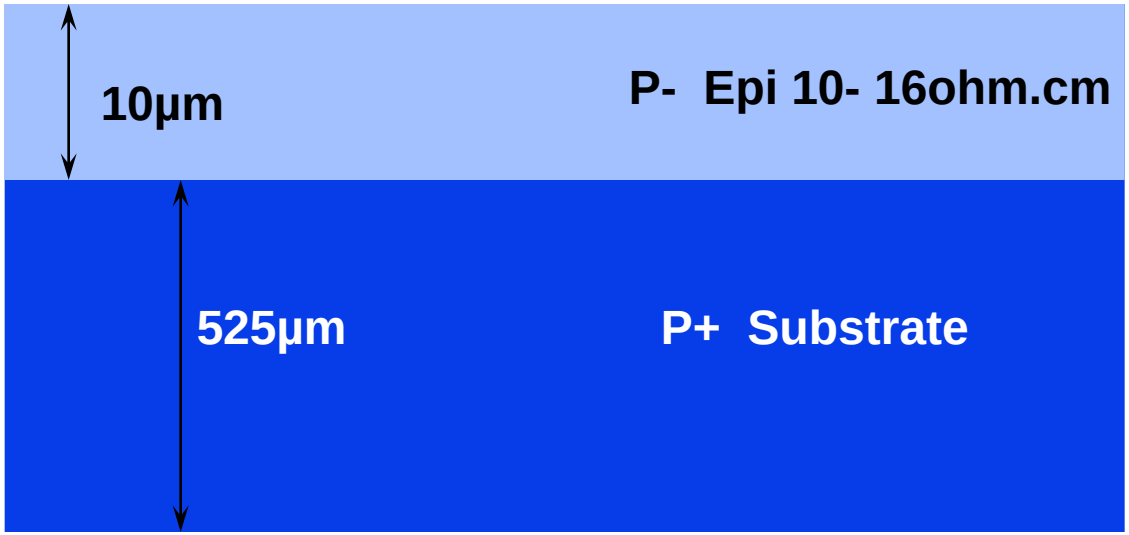
CMOS Process

Tyndall 10V 1.5micron Process

Starting Material

- P on P+ epi material
- Pseudo twin well process

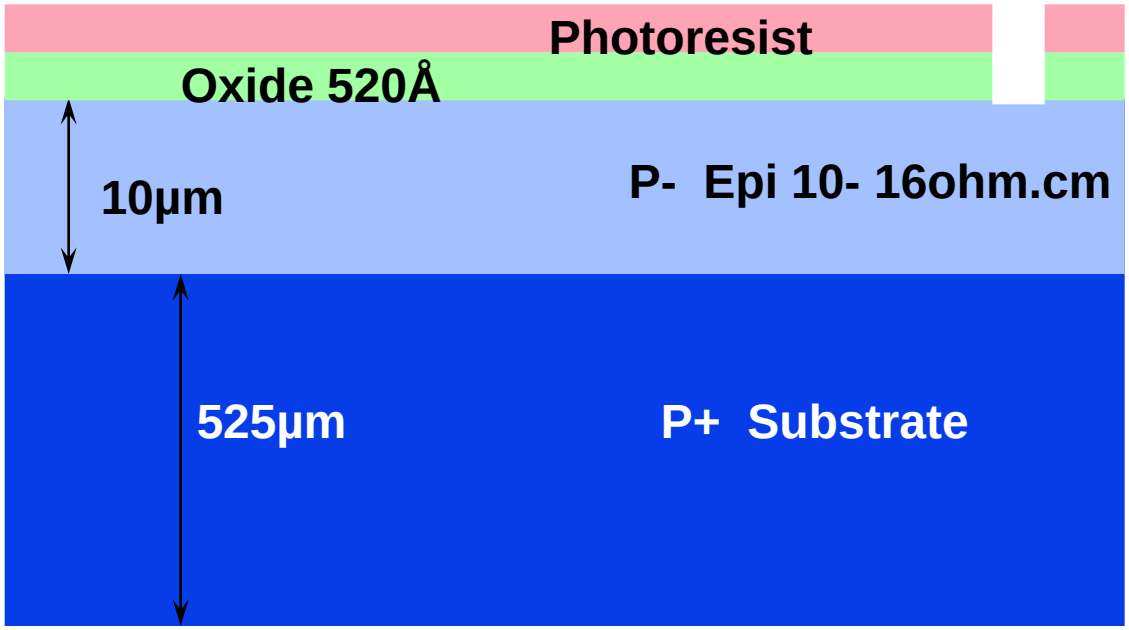
- All furnace ramps in this process are up from 800ºC and down to 800ºC



- Some dimensions in Angstroms
- 1A=10nm

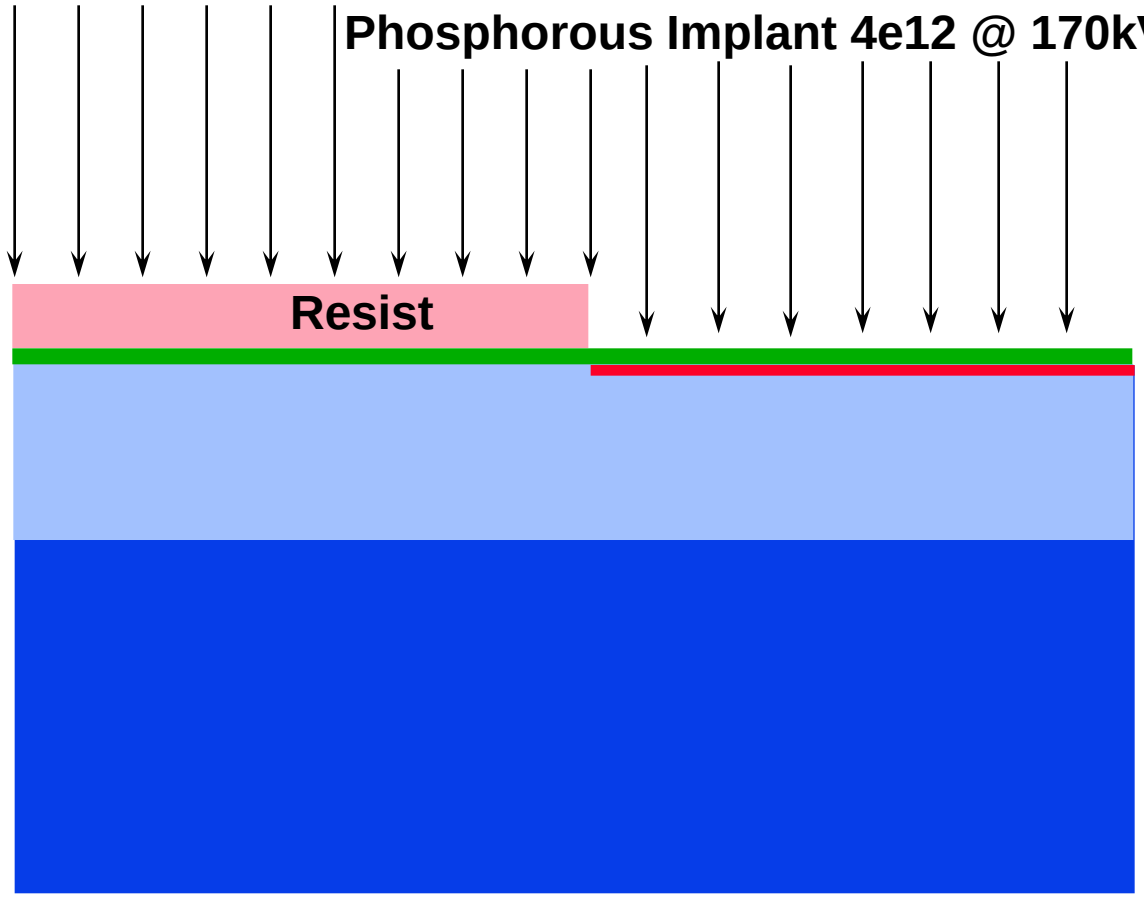
Zero Level Alignment Mark

- **A mark is etched into the silicon for use as an alignment target**



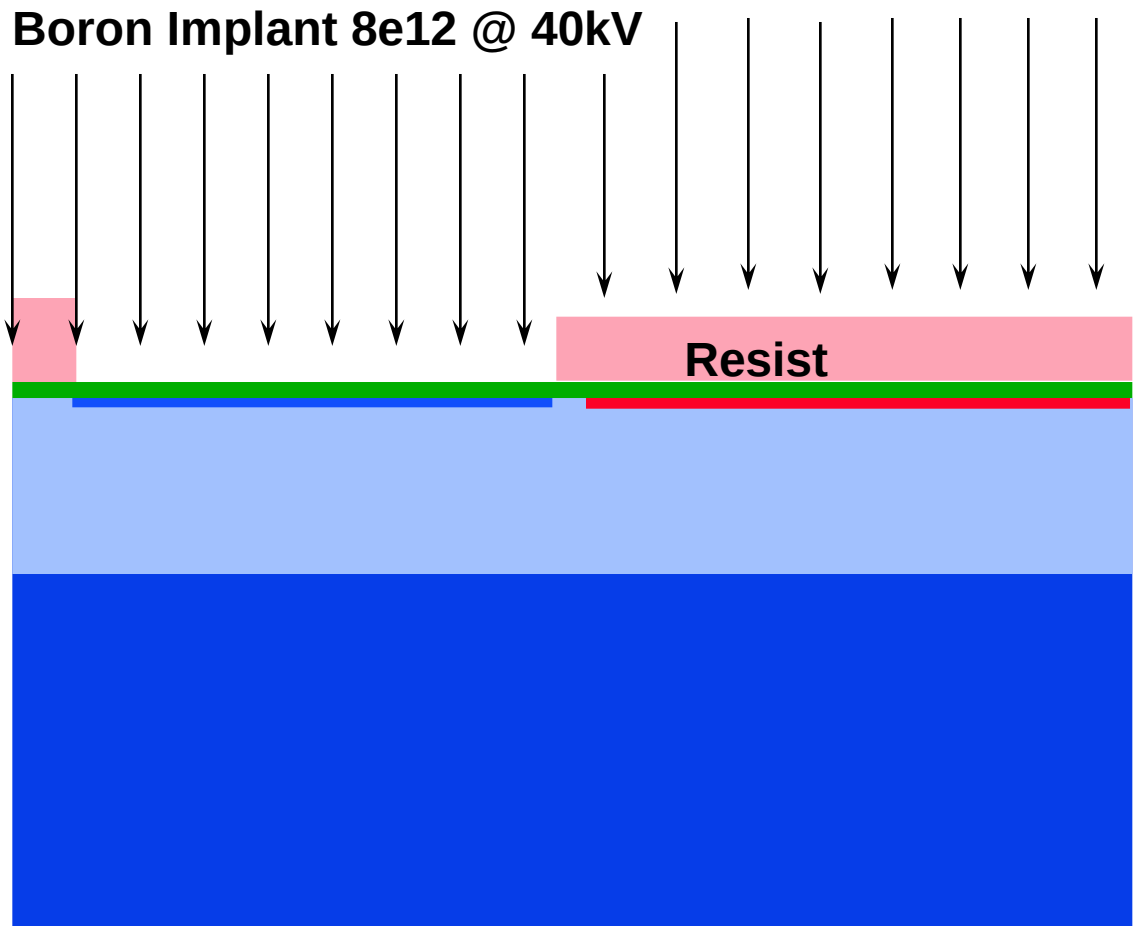
- **Initial Oxide**
- **Temp 975°C**
- **Time 90min**
- **Gas O_2**
- **Target Tox 52nm**
- **Ramp up 20min O_2**
- **Ramp down 30min N_2**

NWell Mask and Implant



- **PWell is the inverse of the NWell**
- **That is the NWell is drawn and the PWell mask is generated from it**

PWell Mask and Implant

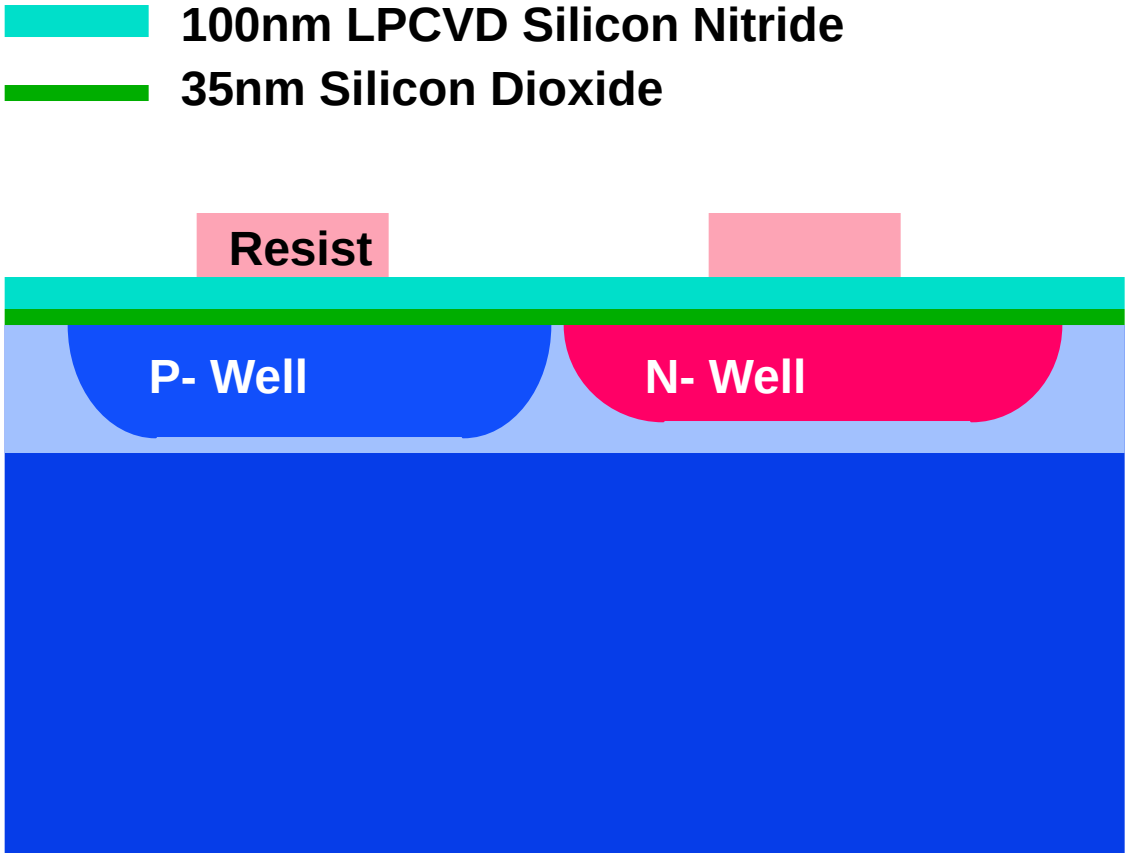


- Pattern the resist
- PWell areas exposed
- Resist protects NWell areas
- Resist stripped after implant

Twin Well Drive

- Well Drive
- Ramp up 30min/N_2
- Temp 1100^{o}C
- Time 22hrs/N_2
- Time 120min/O_2
- Ramp down 60min/N_2
- Strip grown oxide
- The original epi interface is now about 4µm deep because of up diffusion of boron

LOCOS Process 1

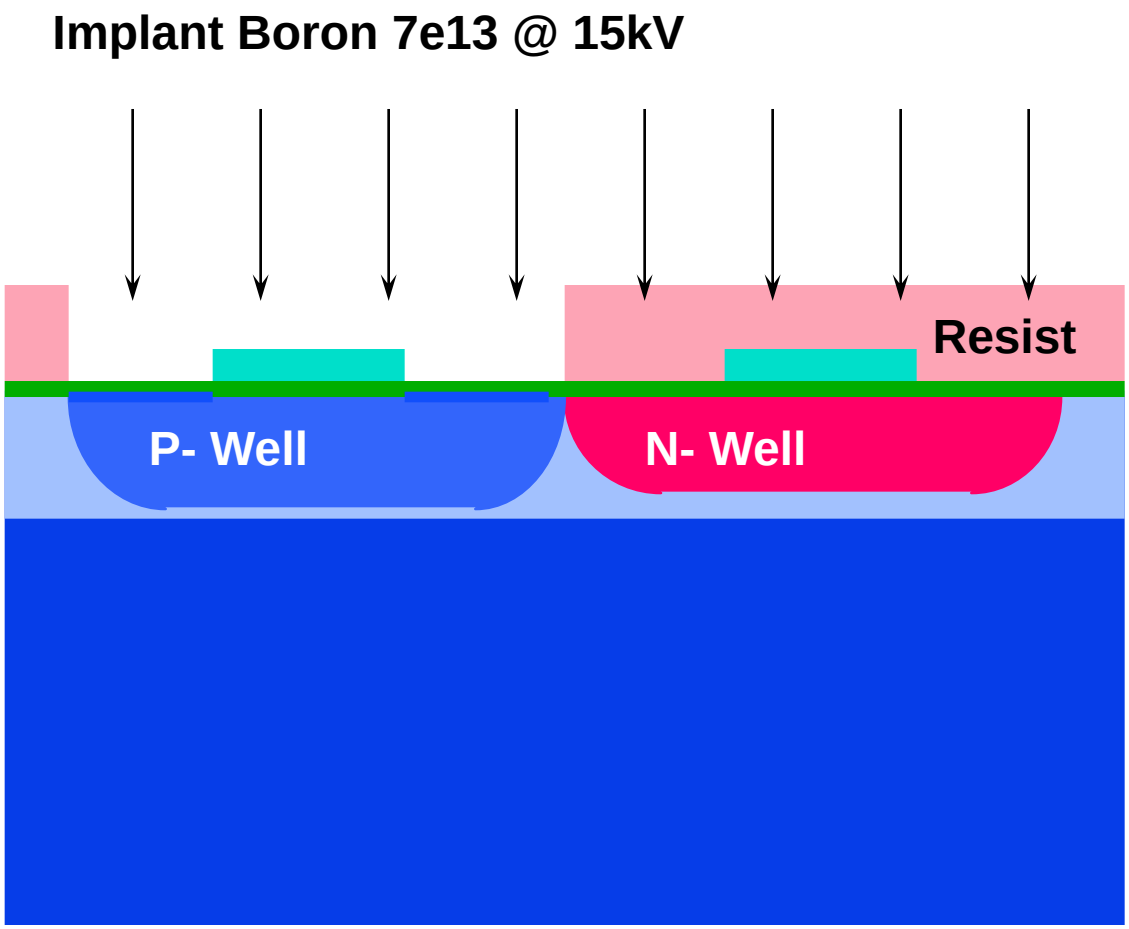


- Pad Oxidation
- Temp 900°C
- Time 152min/O_2
- Time 20min/N_2
- Ramp up 10min/O_2
- Ramp dn 20min/N_2
- 100nm Nitride Deposition
- Temp 800°C
- Time 33min approx

LOCOS Process 2

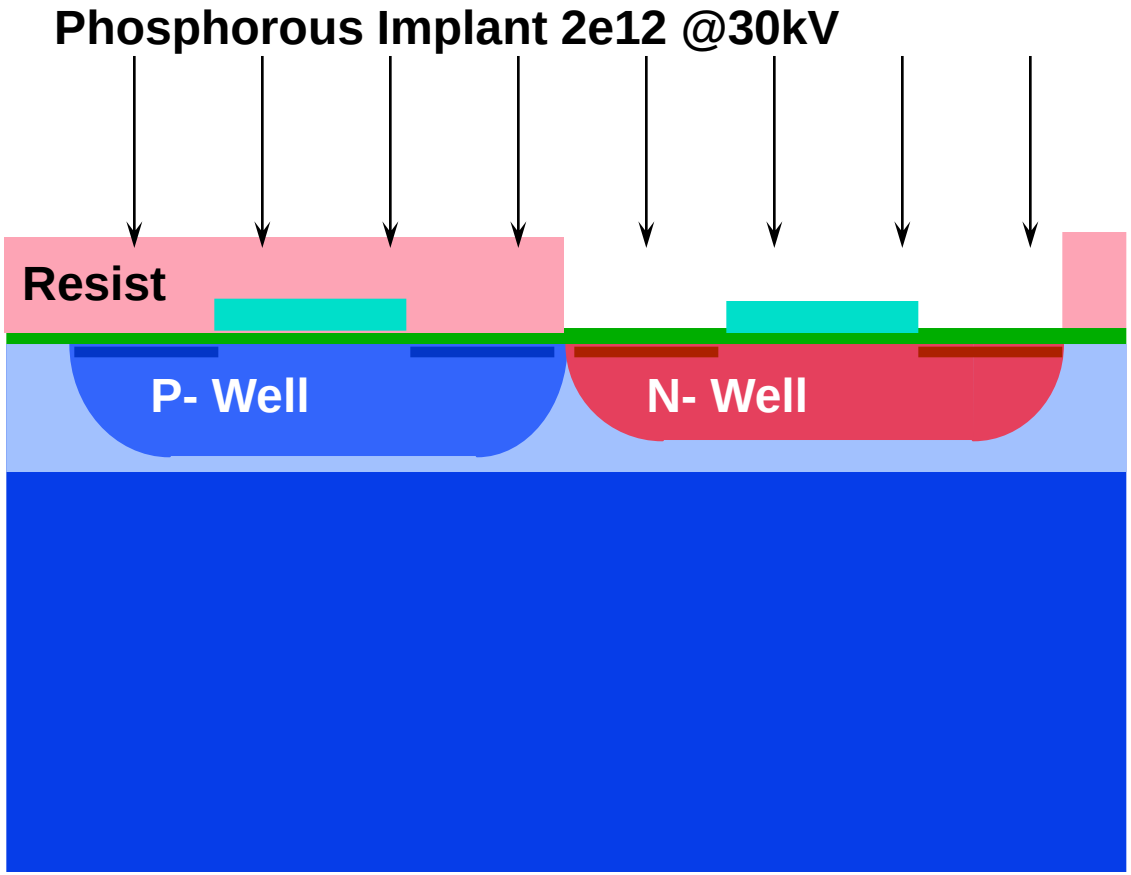
- **Etch the nitride, stop on the oxide**
- **Strip the resist**

Boron Field Mask and Implant



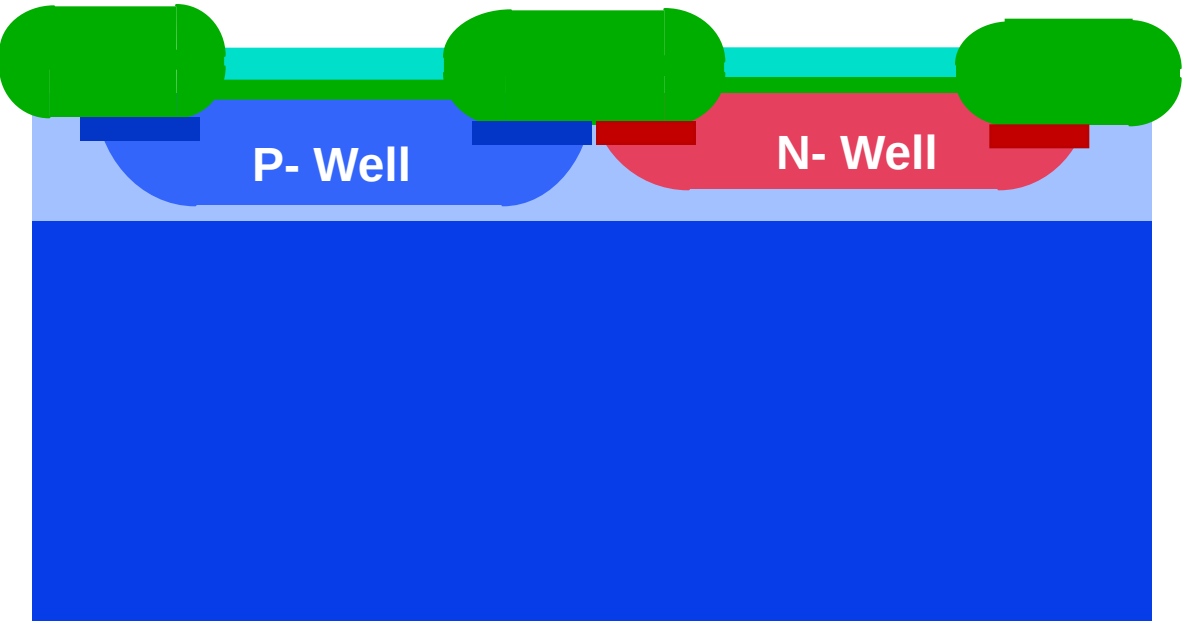
- Boron is implanted into the field areas of the PWell to increase the surface doping concentration

Phosphorous Field Mask and Implant



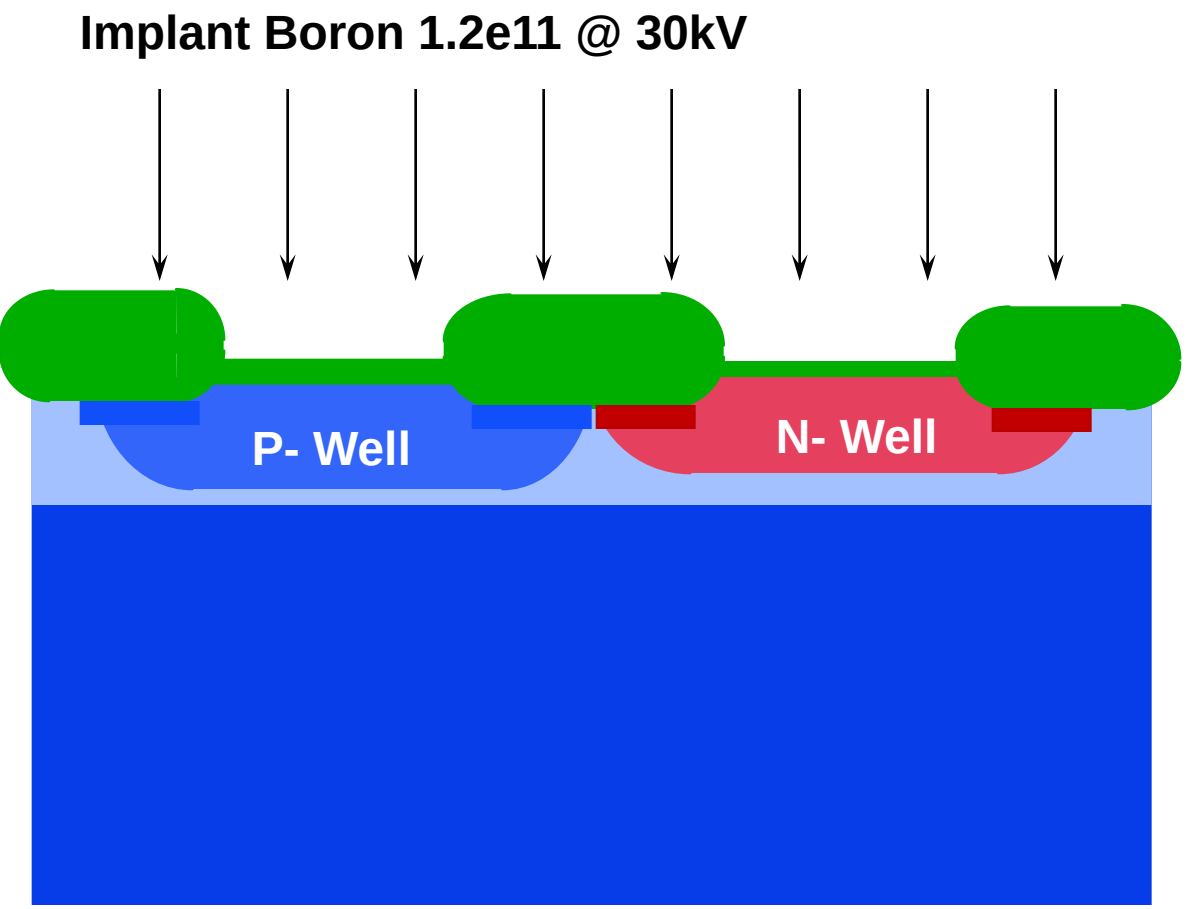
- **Phos is implanted into the non-active NWell areas**

LOCOS 3 Field Oxide Growth



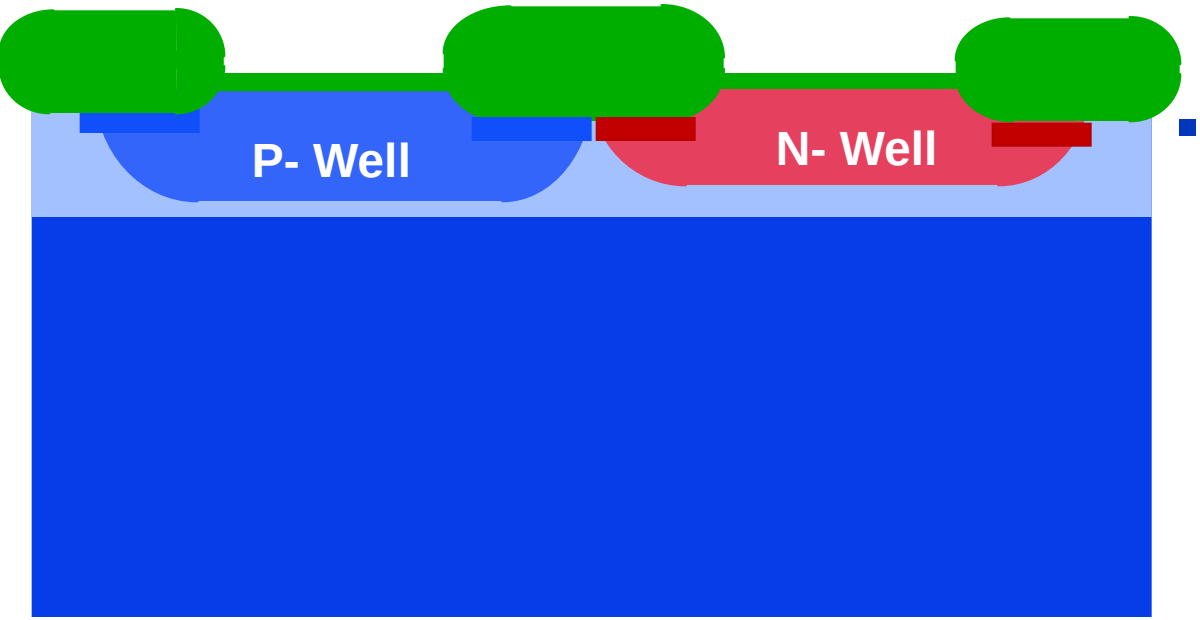
- Field oxidation
- Temp 1000°C
- Time 60min/N_2
- Time 180min/Wet H_2/O_2
- Time 5min /O_2
- Time 10min /N_2
- Ramp up 20min /N_2
- Ramp dn 40min /N_2
- Target Tox 700nm
- Remove nitride

Sacrificial Oxide Growth and Vt Adjust Implant



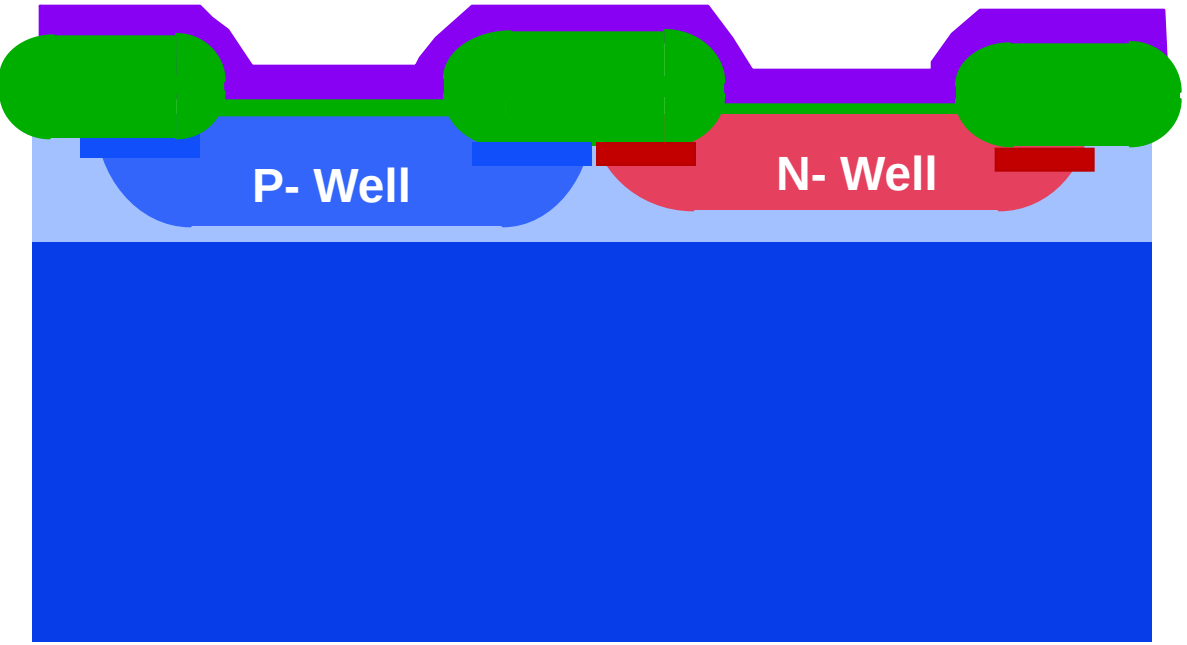
- Grow SAC oxide 28nm
- Temp 950°C
- Time 24min /O_2
- Time 16min /O_2 -TCA
  - cannot be modelled, take as O_2
- Time 20min /N_2
- Ramp up 18min /O_2
- Ramp dn 30min /N_2
- Target Tox 28nm
- Implant Vt adjust
- Strip SAC oxide

Gate Oxidation



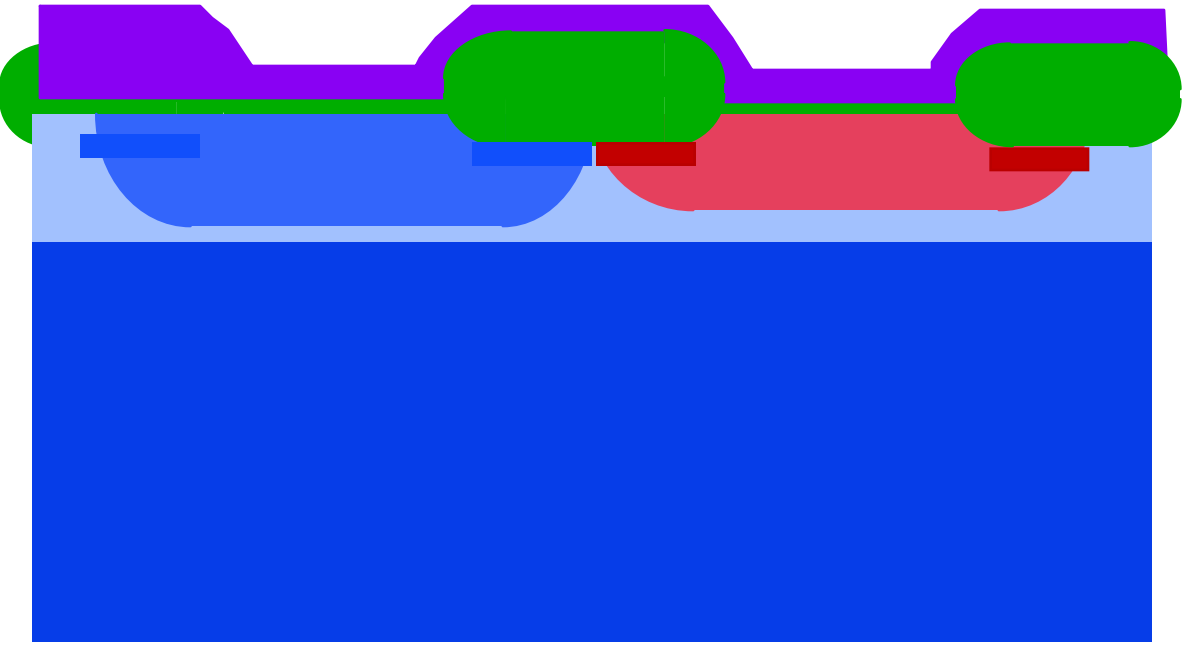
- **Grow Gate Oxide 28nm**
- **Exact same cycle as the SAC oxide previous slide**

Polysilicon Deposition



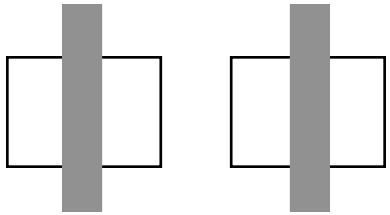
- Deposit 450nm Polysi
- Temp 620°C Time 45-50min

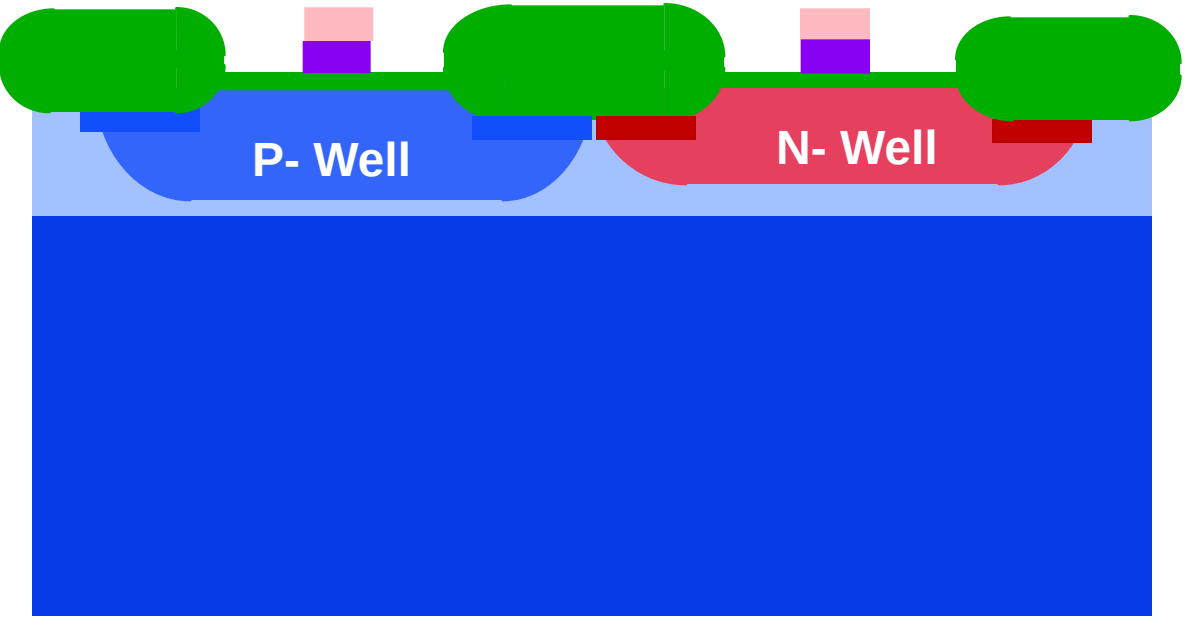
Polysilicon Doping



- Dope the poly with phos
- Temp 900^{o}C
- Time 10min N_2(4l/m)/O_2(95ml/m)
- Time 90min ($POCl_5$) N_2(95ml/m)/O_2(95ml/m
- Time 10min N_2(4l/m)/O_2(95ml/m)
- Ramp up 10min N_2
- Ramp dn 20min N_2
- Pattern the poly mask

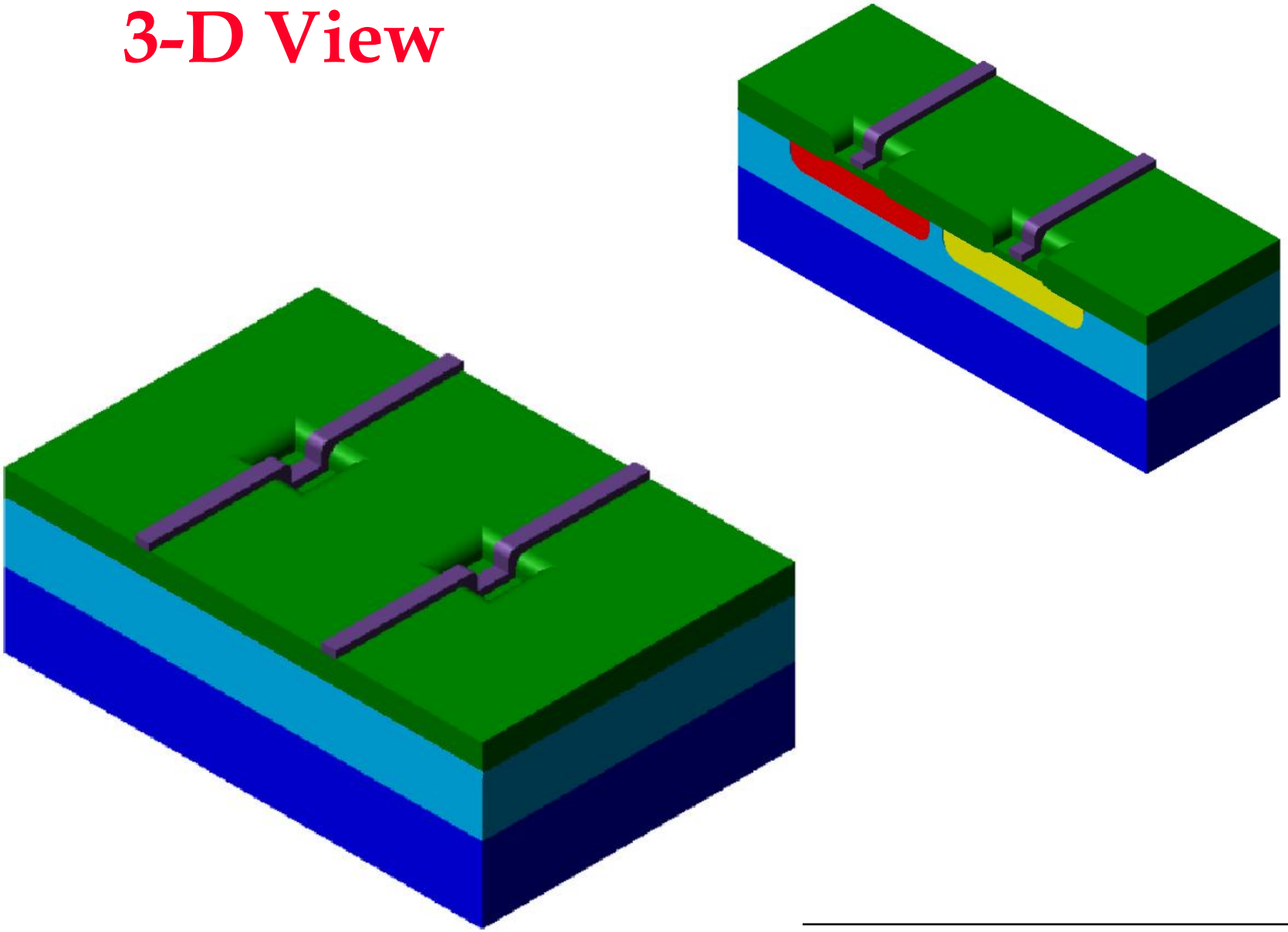
Etch Polysilicon



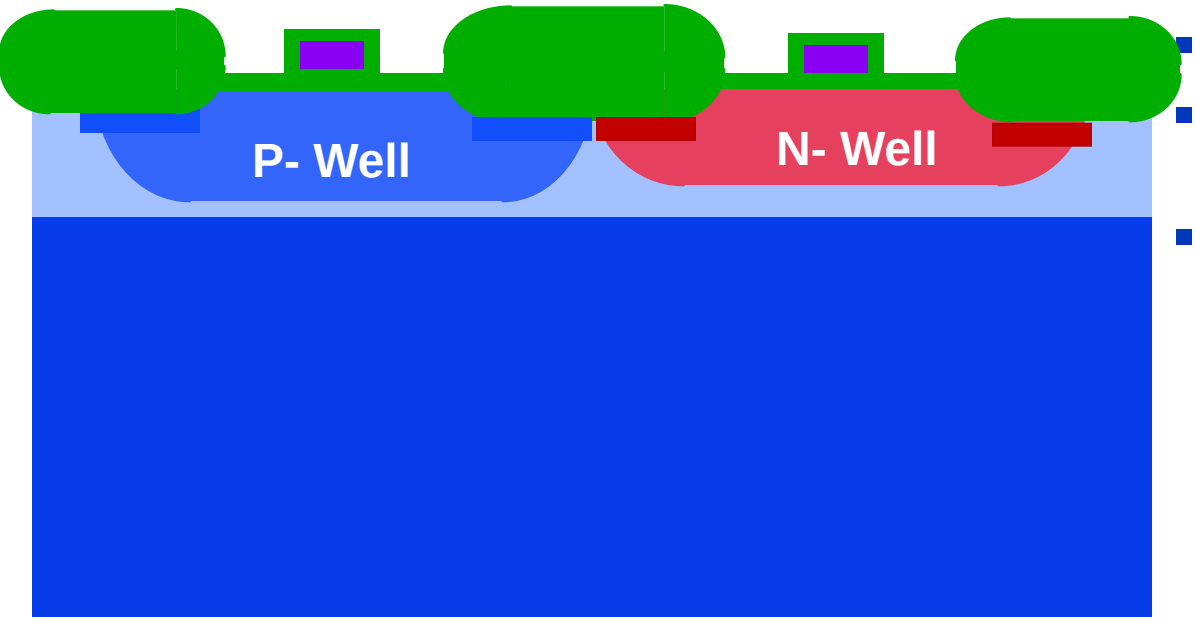


- **Etch the poly leaving the tracks behind**
- **Strip the resist**

3-D View

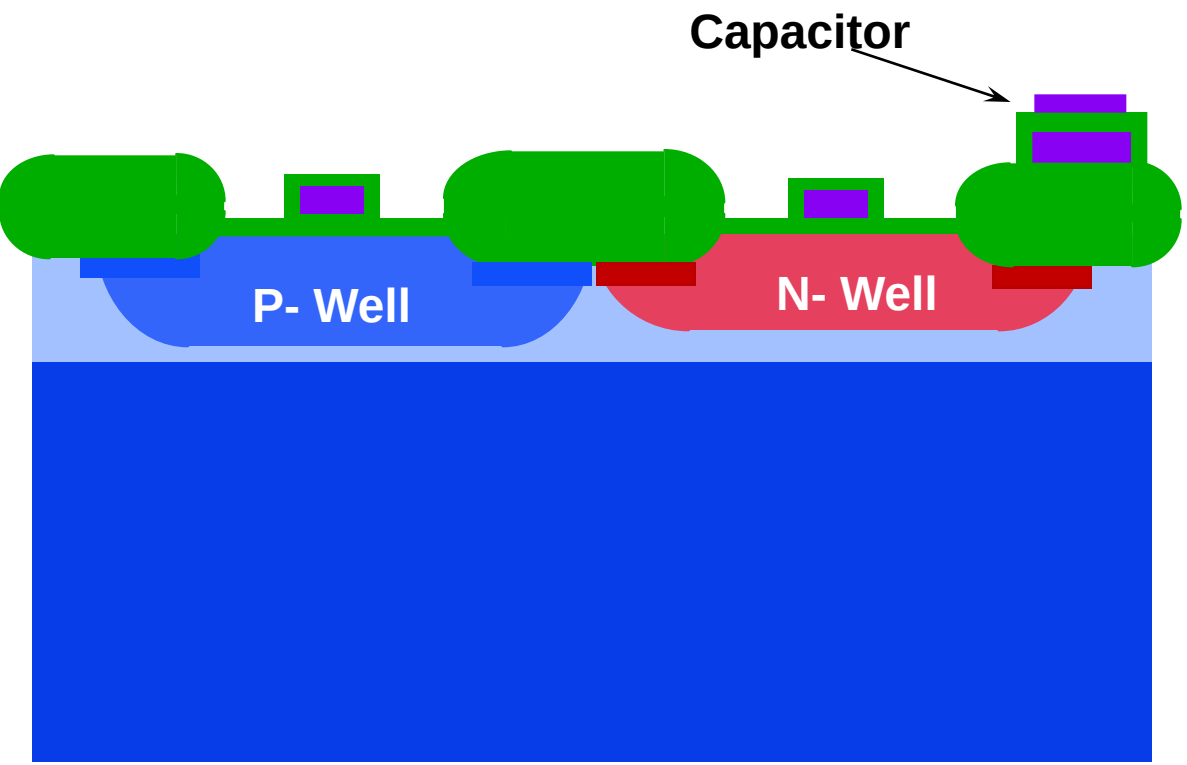


Poly Oxidation



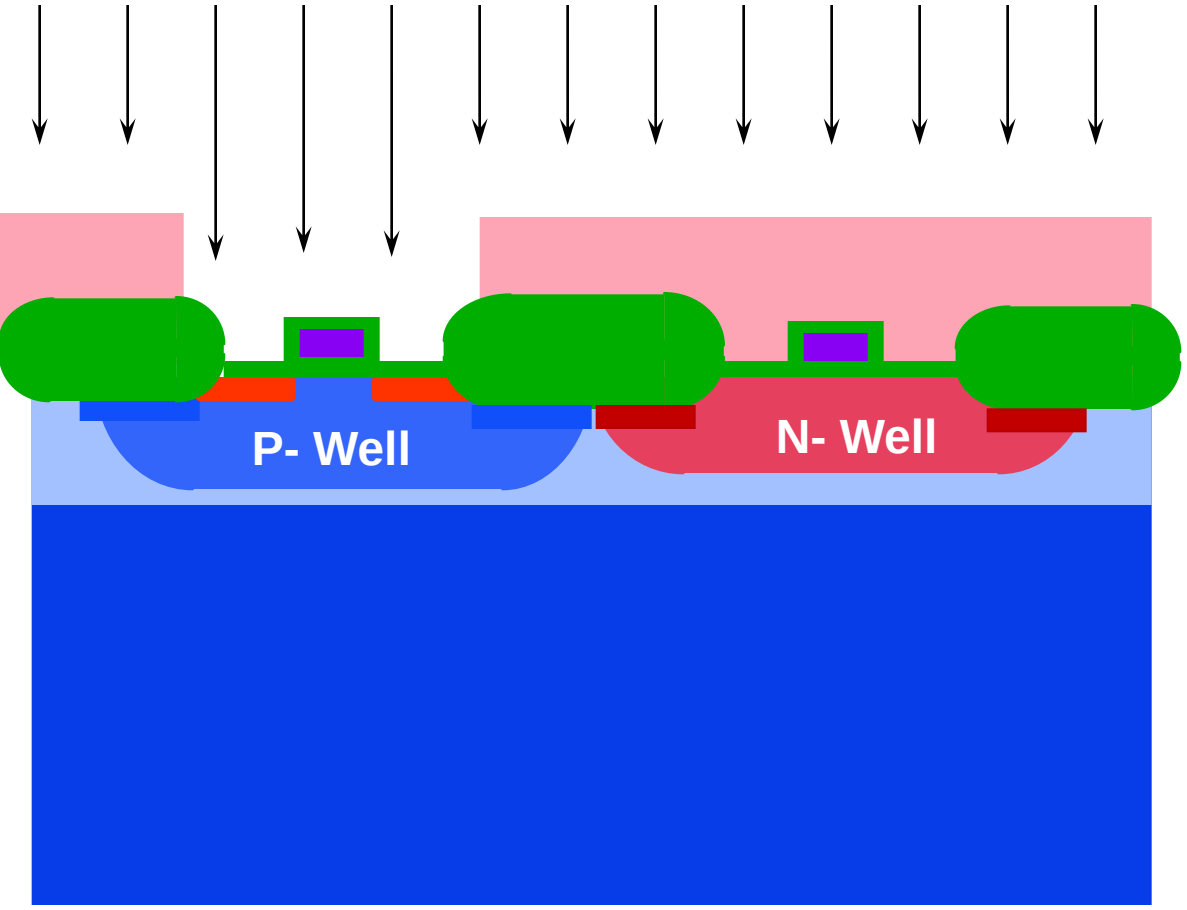
- Polysilicon is reoxidised
- Temp 900°C
- Stabilisation Time 20min N_2(4l/m)/O_2 (1.8l/m)
- Time 105min O_2
- Ramp up 10min N_2(4l/m)/O_2 (1.8l/m)
- Ramp dn 20min N_2

Polysilicon Capacitor Formation



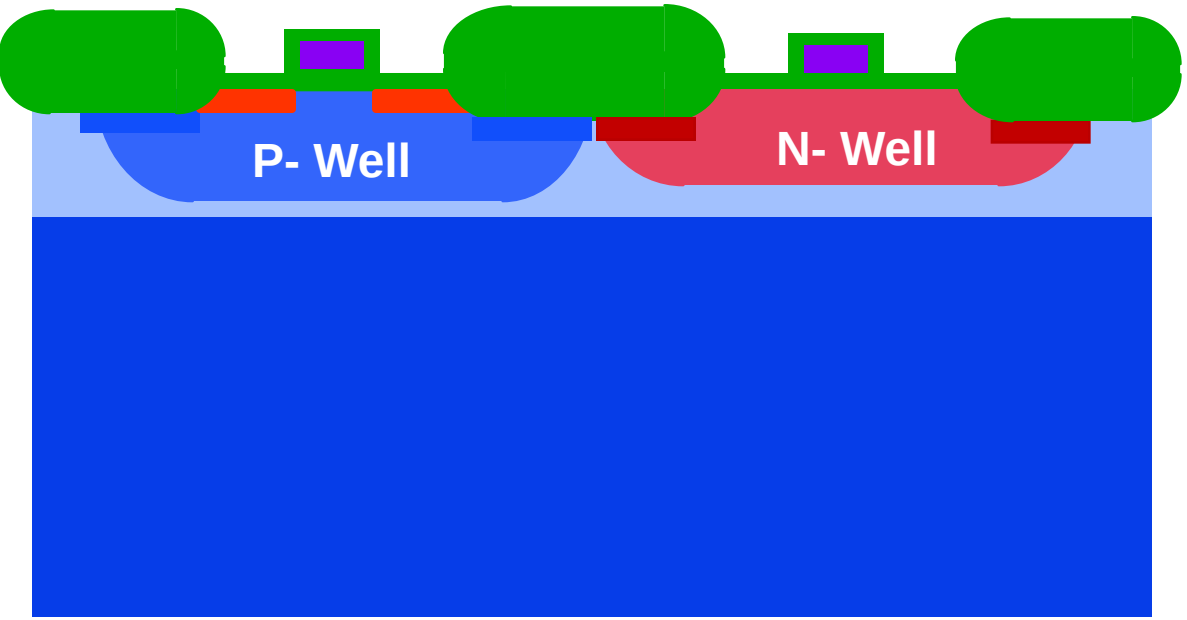
- By adding a second layer of polysilicon (200nm) and doping it
- A poly-poly capacitor can be formed between the 2 levels of polysilicon
- These capacitors are only allowed in the field areas. They are not allowed over active area

N+ Source/Drain Mask and Implant



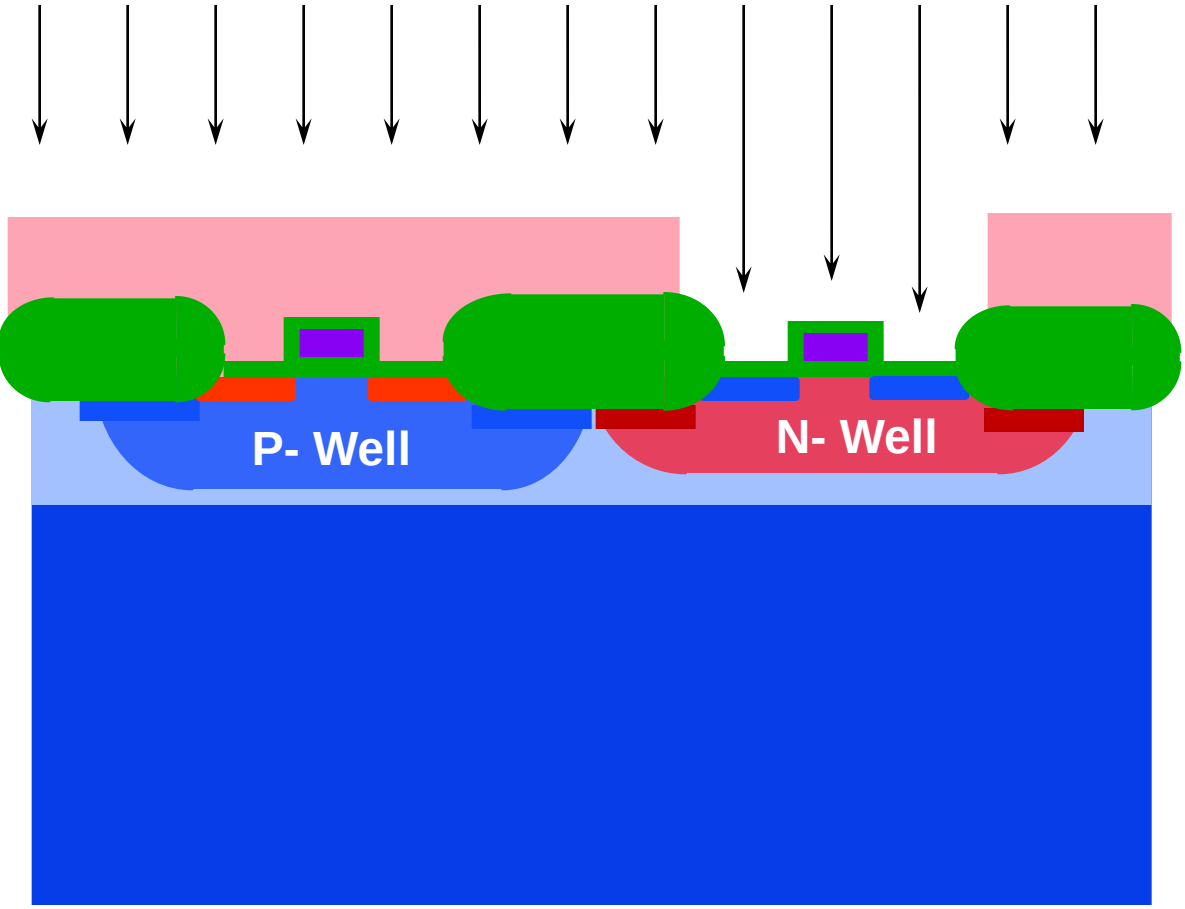
- **Implant Phos/As for the N+ source/drains**
- **Phos 5e13@110keV**
- **As 6e15@110keV**
- **The poly protects the channel areas**

N+ Anneal



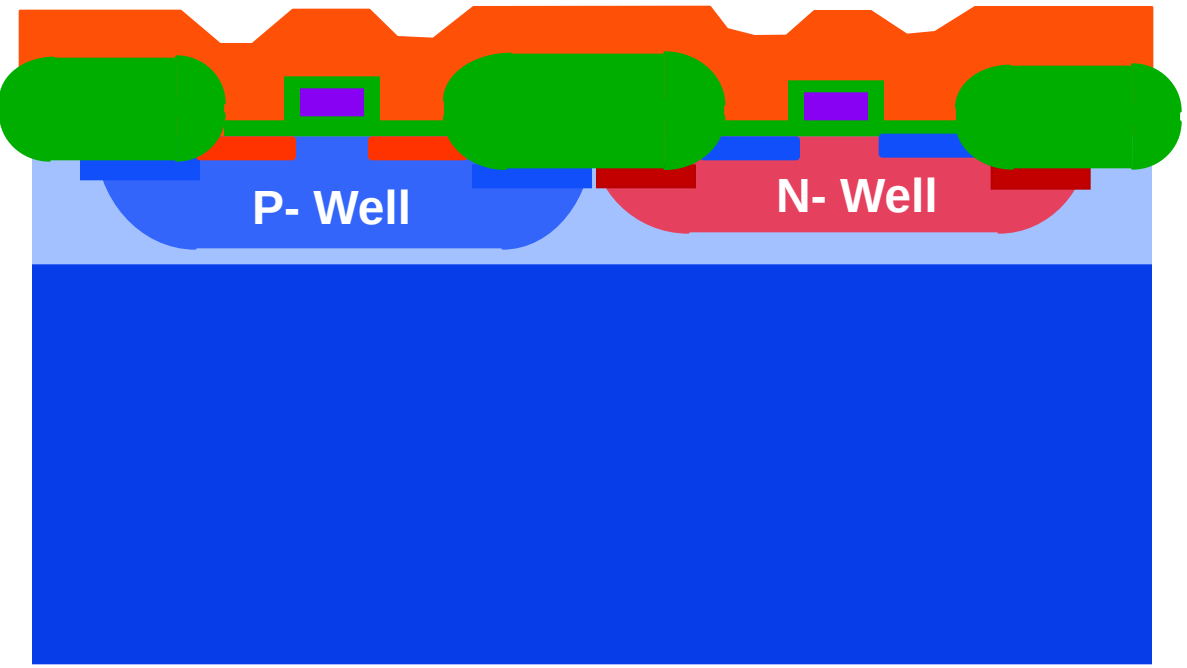
- N+ anneal of the implant
- Temp 900°C
- Time 60min N_2
- Ramp up 5min N_2
- Ramp dn 20min N_2

P+ Source/Drain Mask and Implant



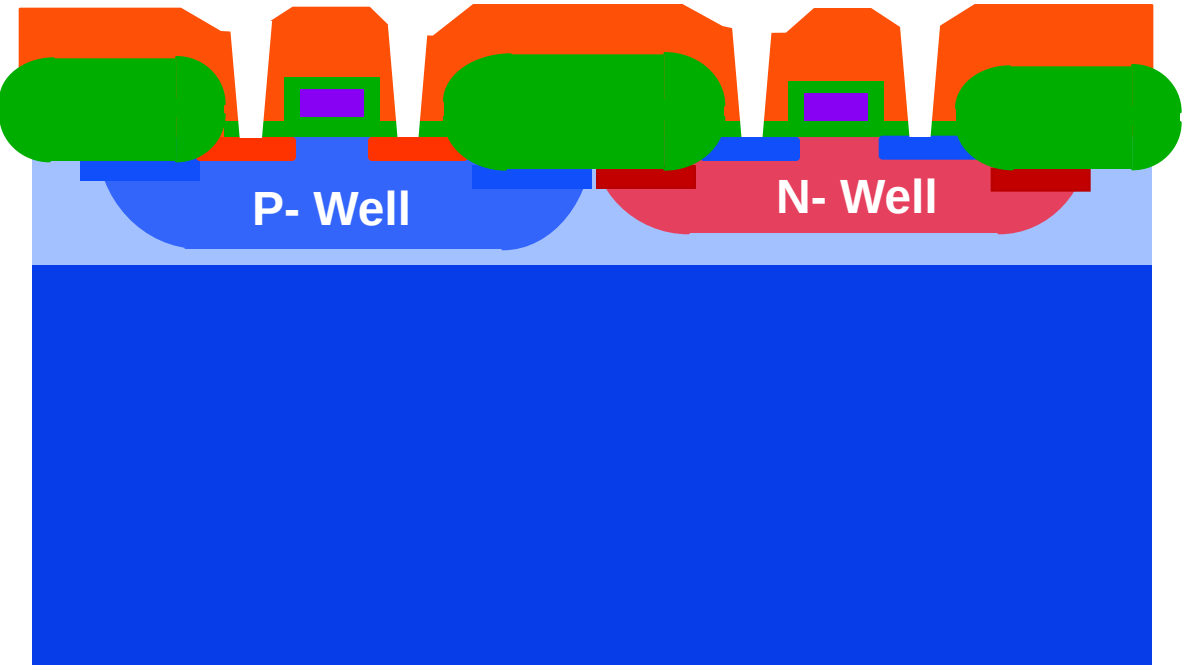
- **Boron is implanted into the P+ S/D regions**
- **Boron 4e15@15keV**

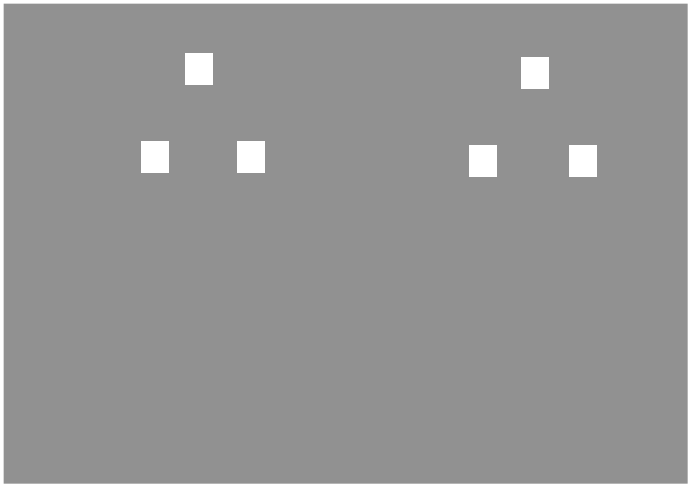
Deposit BPSG Reflow and Anneal



- BPSG deposition
  - 350
  - 4% B - 4%P
- Reflow Anneal
- Temp 900°C
- Time 3min O_2
- Time 5min H_2/ O_2
- Time 3min O_2
- Time 30min N_2
- Ramp up 10min O_2
- Ramp dn 20min N_2

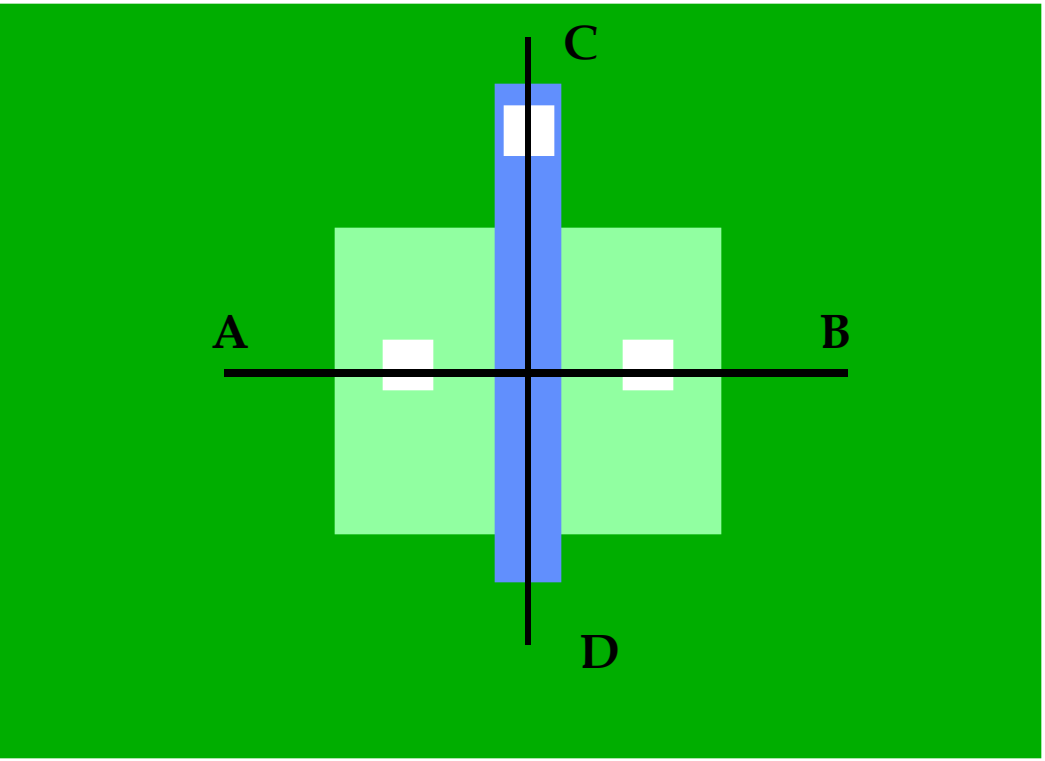
Contact Mask and Etch





- **Contact holes are etched with a taper etch through to the S/D and the polysilicon**
- **This is a dry etch process (RIE)**

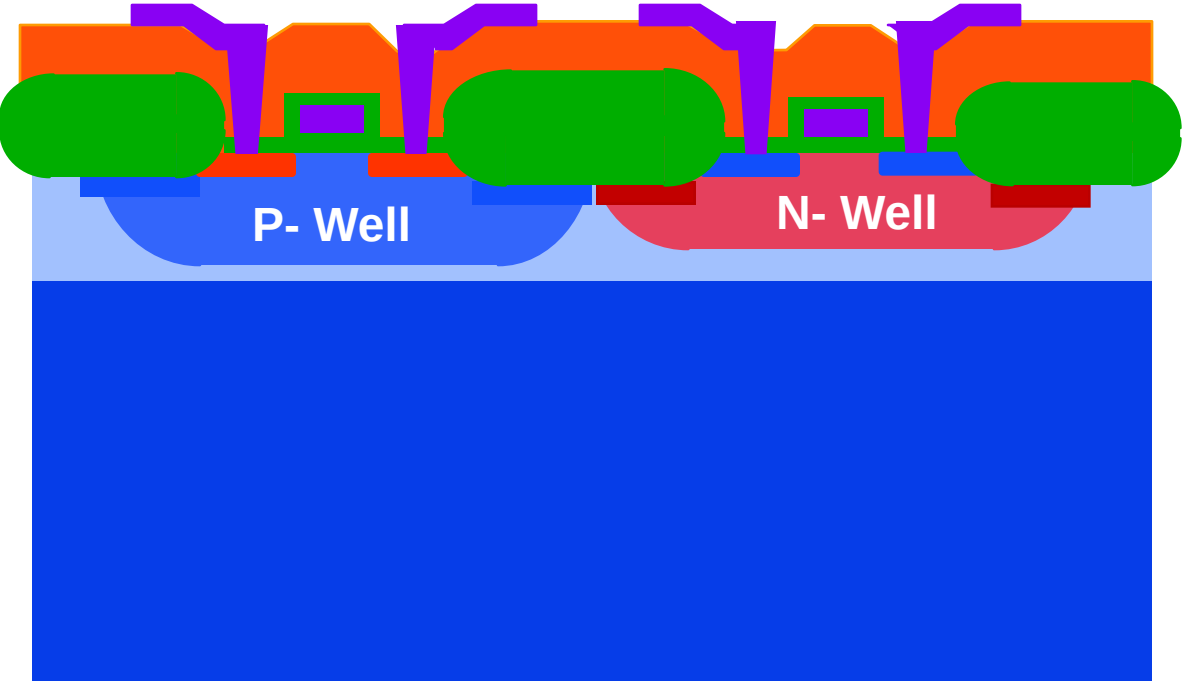
Plan View of Contact Location



- All previous cross-sections through A-B
- The Polysilicon contact is not made in the thin ox/active area, but on the field oxide area
- Poly contact cannot be seen in the A-B cross section
- See C-D section next slide

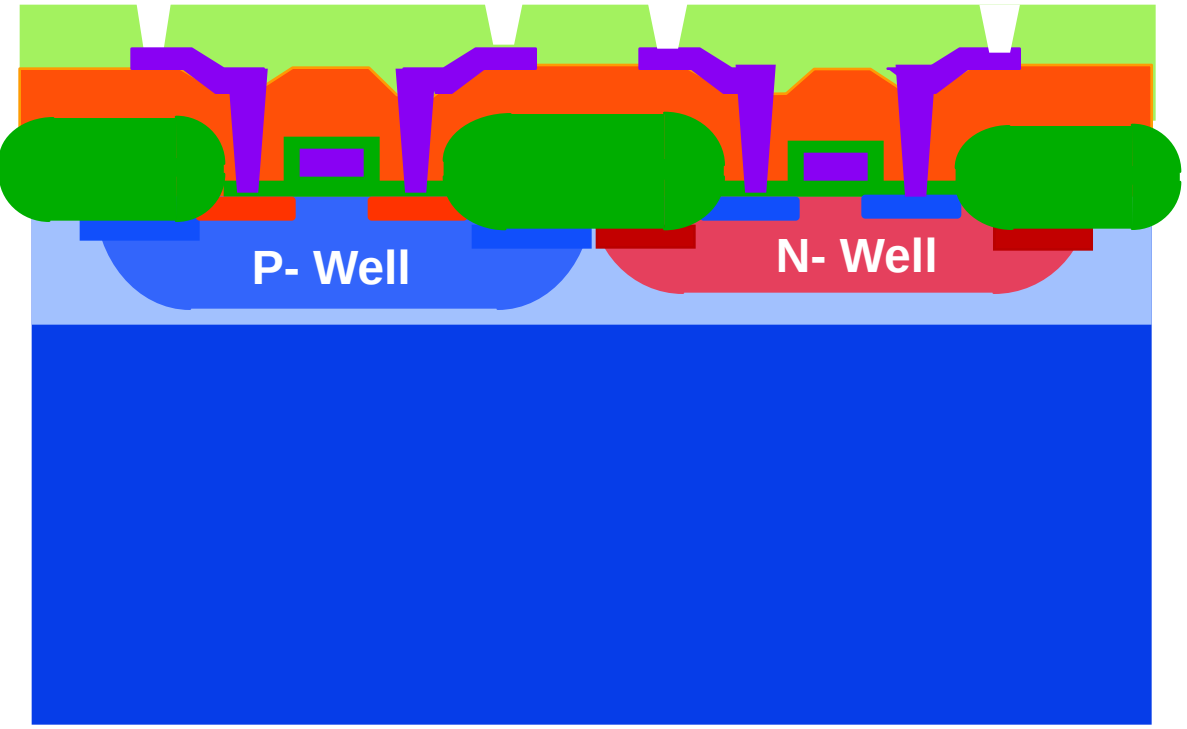
C-D Cross-Section Showing Polysilicon Contact

Sputter Mask and Etch Metal 1



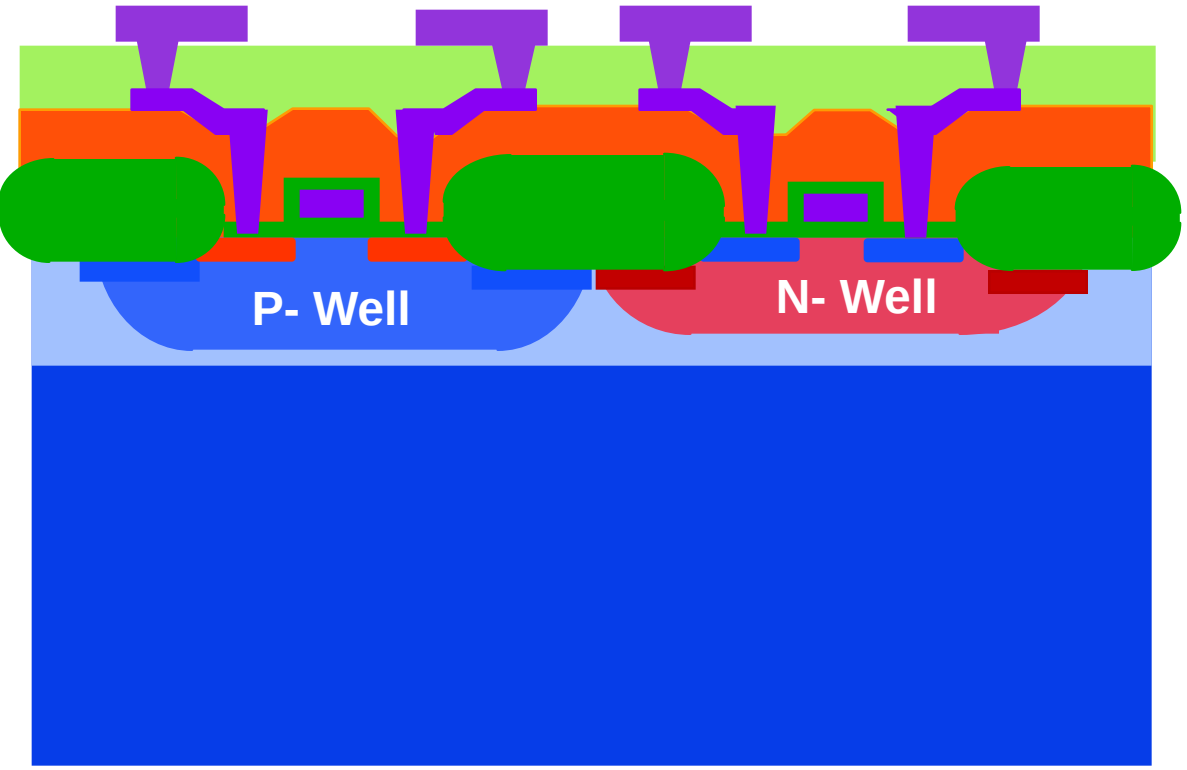
- **0.5µm Aluminium/0.5% Silicon is sputtered on the wafer surface**
- **Patterned and then etched**

Deposit Interlevel Dielectric mask and Etch vias



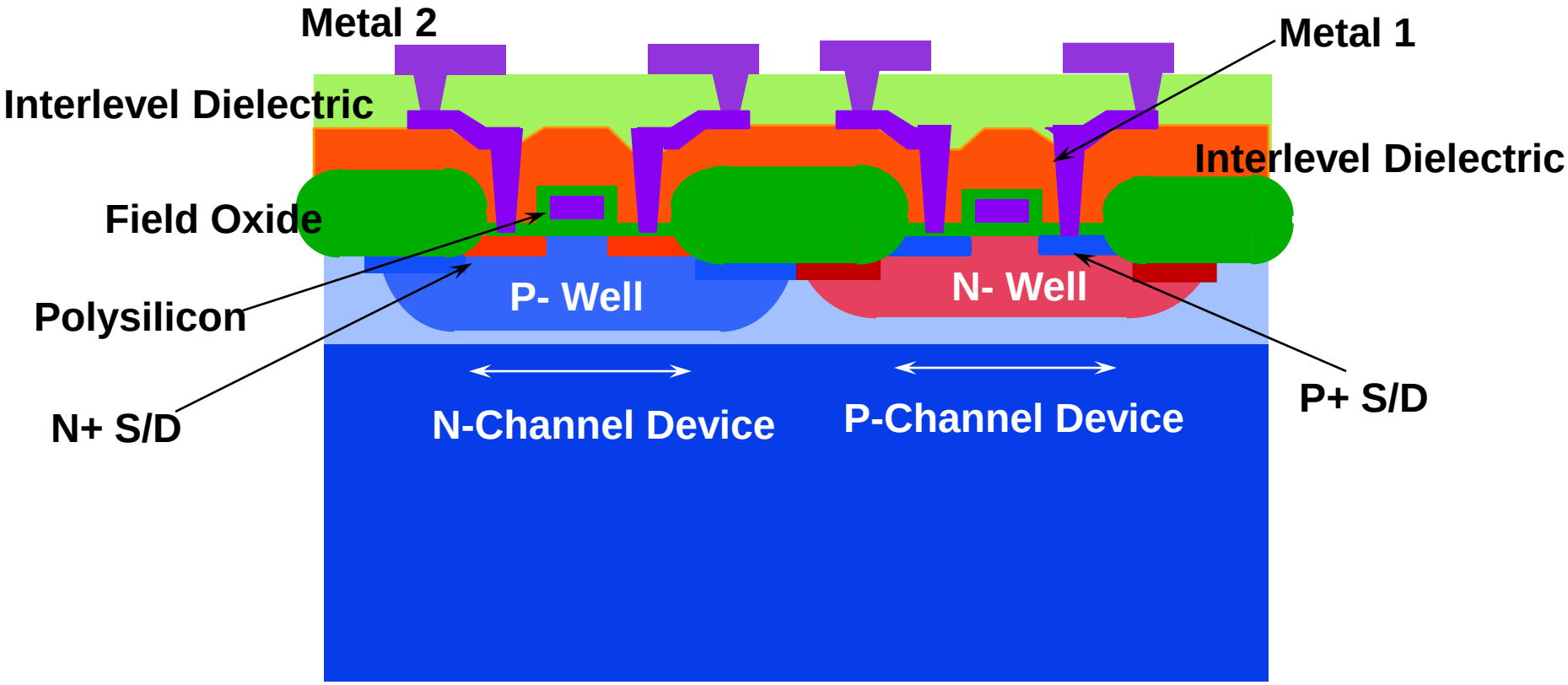
- **Most modern small geometry processes will have more than 1 level of metal ours uses a Spin on Glass**
- **SOG sinter**
- **Temp 425^{o}C**
- **Time 75min N_2**

Metal 2 Sputter Mask and Etch

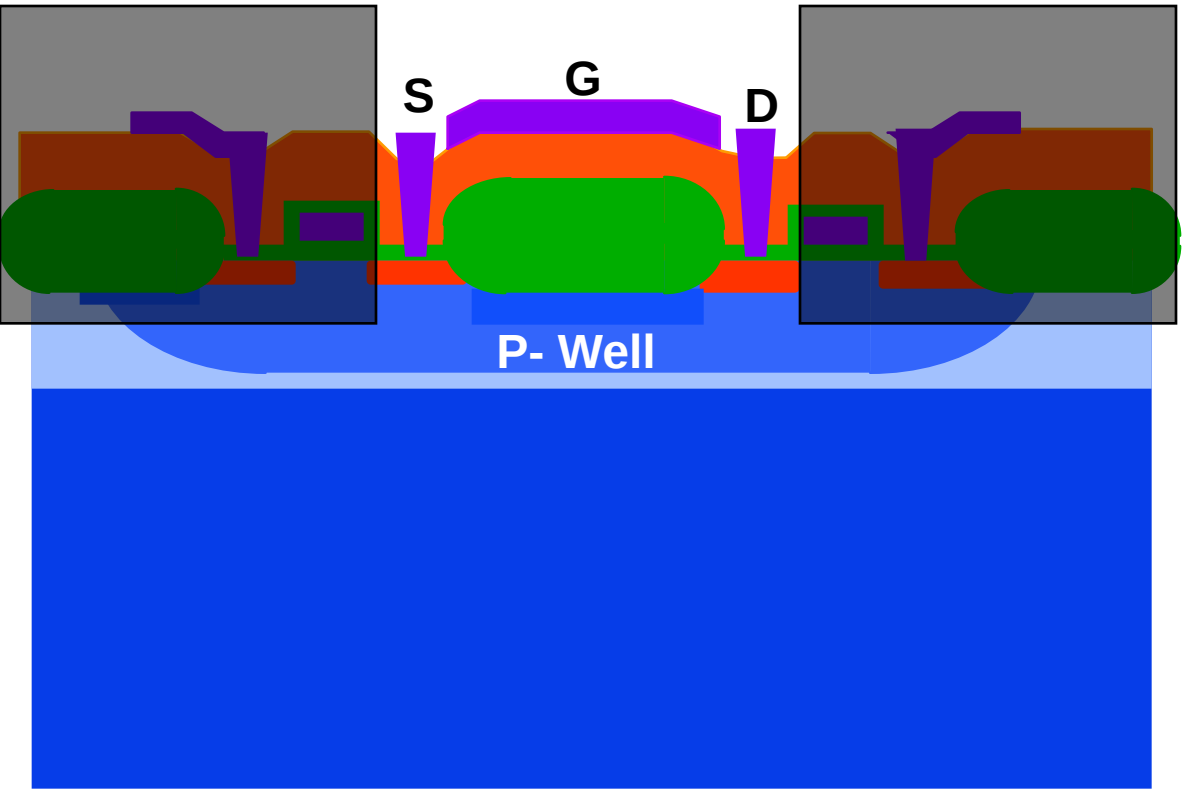


- 1.0µm of aluminium silicon is deposited for metal 2
- The Wafers are then alloyed or sintered
- Alloy
- Temp 400^{o}C
- Time 15min N_2
- Time 60min N_2/ H_2
- Time 5min N_2

Finished Product

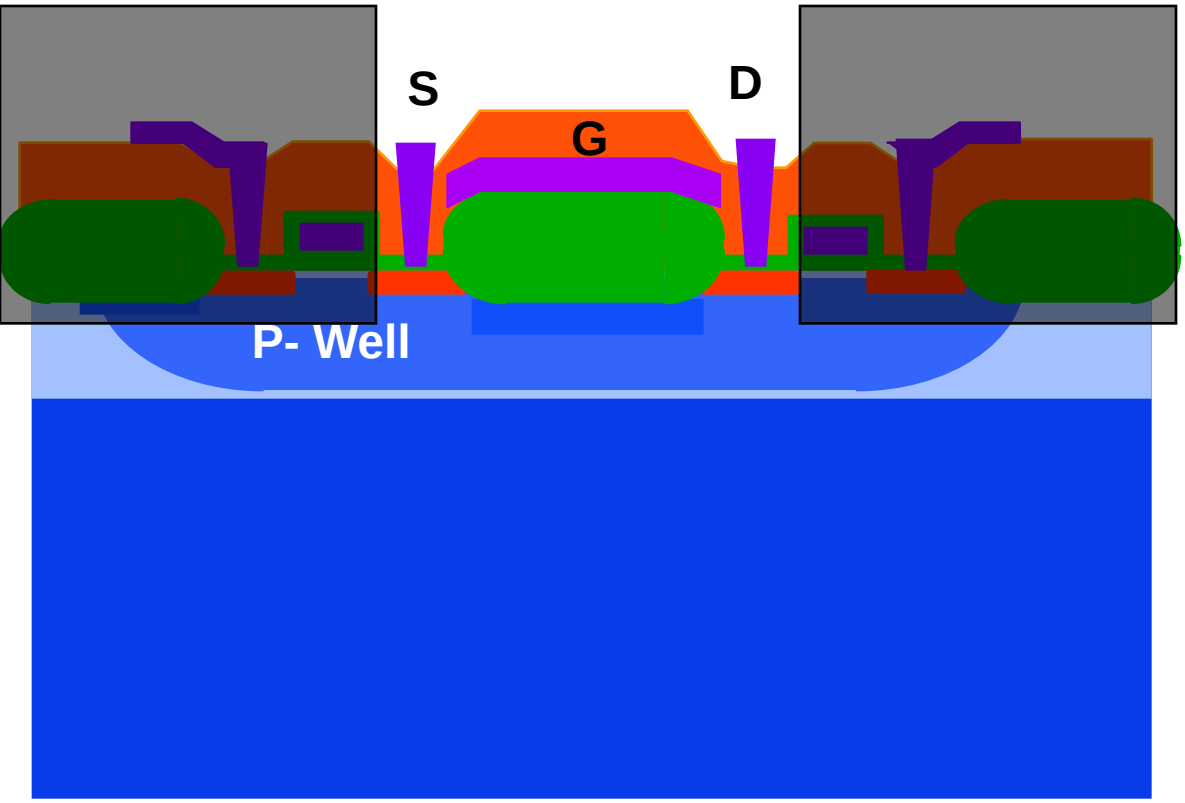


Metal Gate Field Device



- A channel can be inadvertently formed in the field areas
- It is important that this device is not turned on

Polysilicon Gate Field Device



- Poly gate device should have a lower threshold than the metal gate device
- Threshold of the field devices should be higher than the power supply voltage

High-k + Metal Gate Transistors

Improved Transistor Density	~2x
Improved Transistor Switching Speed	>20%
Reduced Transistor Switching Power	~30%

65 nm Transistor | **45 nm HK + MG**