UE4010 Summer 2006 Part A

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an NMOS in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.
In each question, capacitances other than those mentioned may be ignored.

Question 1

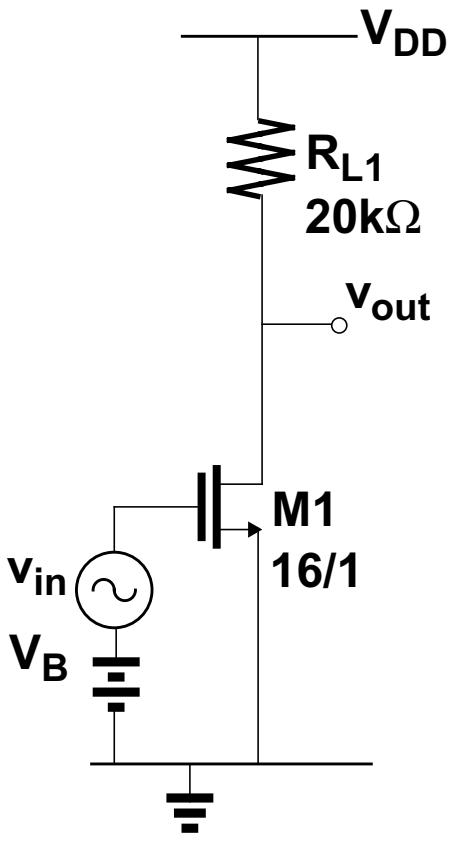

Figure 1a

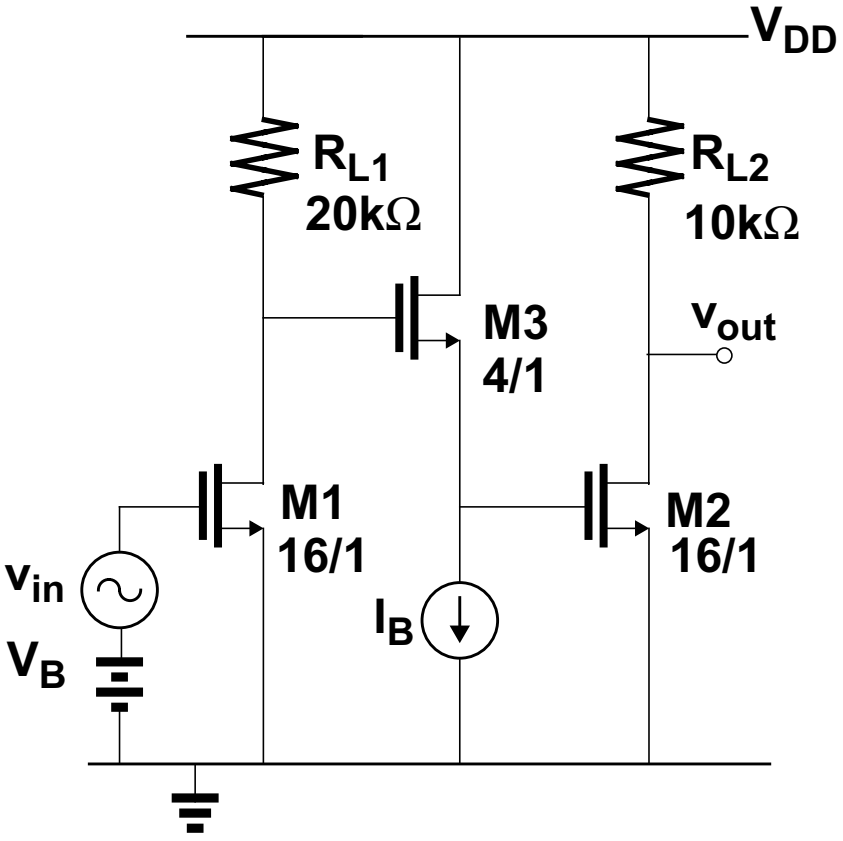

Figure 1b

Assume all transistors in the circuits shown in Figure 1a and 1b are biased in saturation.

(i) Draw the small-signal equivalent circuit for the common-source stage shown in Figure 1a.

(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}) of this circuit in terms of the small-signal transistor parameters and R_{L1}.

(iii) Calculate the small-signal voltage gain (v_{out}/v_{in}) in dB if
V_{DD}=5V, V_B = 1V, V_{tn} = 0.75V, K_n'=200μA/V^2.
Assume $R_L << 1/g_{ds1}$. Transistor dimensions in microns, and resistor values are as shown in Figure 1a.

(iv) The stage shown in Figure 1a is cascaded with a similar stage, as shown in Figure 1b.
What value of I_B is required so that M2 has the same gate bias voltage as M1?
Calculate the small-signal voltage gain (v_{out}/v_{in}) in dB of the circuit in Figure 1b.
Assume the source-follower stage has unity gain.

Question 2

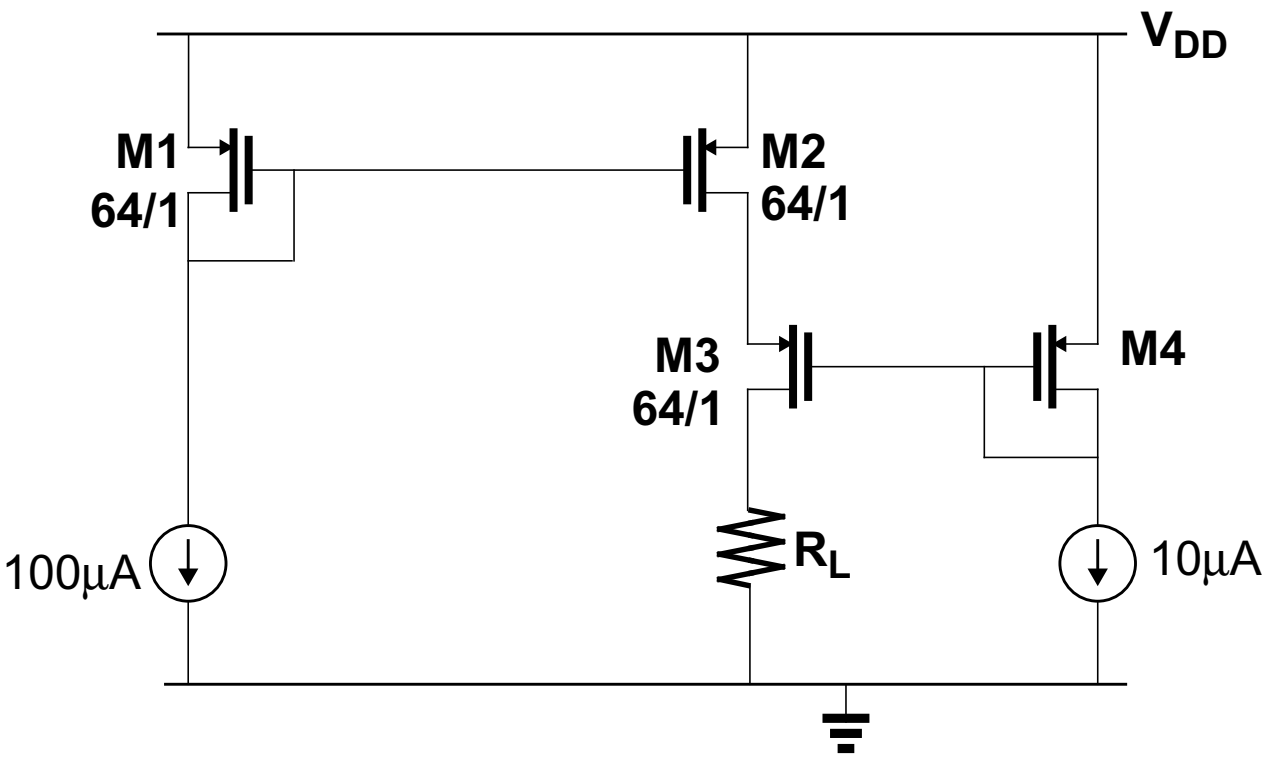

Figure 2

Figure 2 shows a PMOS current mirror (M1, M2) with cascoded output. The bias voltage for the cascode is generated by the diode-connected PMOS M4, which is biased by a current source as shown.

For this question K_p'=50µA/V^2, V_{tp}= -750mV, V_{DD}=3V.

The device sizes of M1, M2 and M3 in microns are as indicated in Figure 2.

(i) What is the maximum voltage at the drain of M2 such that M2 is just biased in saturation?
If M4 has L=10µm, what is the required value of W for M4 such that M2 is just biased in saturation, assuming M3 is in saturation?

(ii) What is then the maximum value of R_L such that M3 is also biased in saturation?

(iii) Given the bias conditions established in (i) and (ii), estimate the percentage inaccuracy of the current mirror due to the finite output conductance of M1 and M2.
For this calculation take λ_p=0.04V^{-1}.

(iv) Estimate the 3 sigma percentage inaccuracy of the current mirror due to transistor V_{tp} mismatch.
Note: Assume the mismatch is normally distributed and that the 1 sigma V_{tp} mismatch of a transistor pair (in mV) is given by

$$\sigma_{\Delta V_{tp}} = \frac{A_{V_{tp}}}{\sqrt{WL}}$$

Take A_{Vtp}= 10mVµm.

Question 3

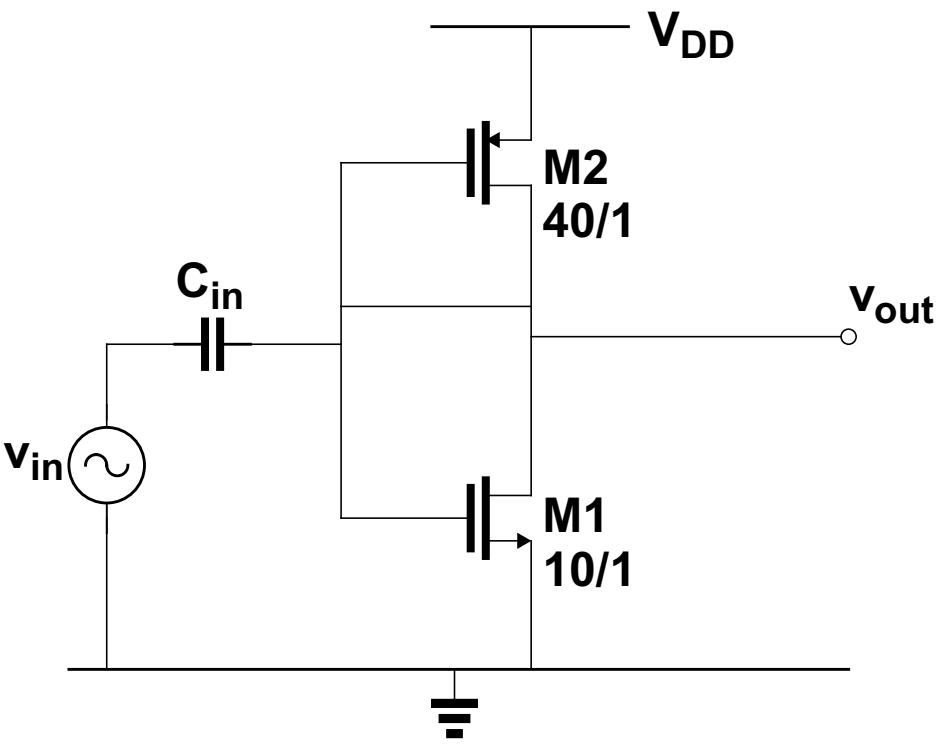

Figure 3

For the questions below you may assume $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$ and that all devices are biased in saturation.
Transistor dimensions in microns are as shown in Figure 3.

(i) Figure 3 shows a CMOS inverter stage. The input signal v_{in} is capacitively coupled into the stage through the capacitor C_{in}.
Draw the small-signal model for this circuit.

(ii) Ignoring all capacitances except C_{in}, derive an expression for the high-frequency transfer function of the small-signal voltage gain (v_{out}/v_{in}) of the circuit shown in Figure 3.

(iii) Calculate the break frequencies (i.e. pole and/or zero frequencies) if
V_{DD} = 3V, V_{tn} = $|V_{tp}|$ = 0.7V, K_n'=200µA/V^2,K_p'=50µA/V^2,C_{in}= 1nF.

(iv) Draw a Bode diagram of the gain response.
What is the value of gain at frequencies well above the break frequencies.

Question 4

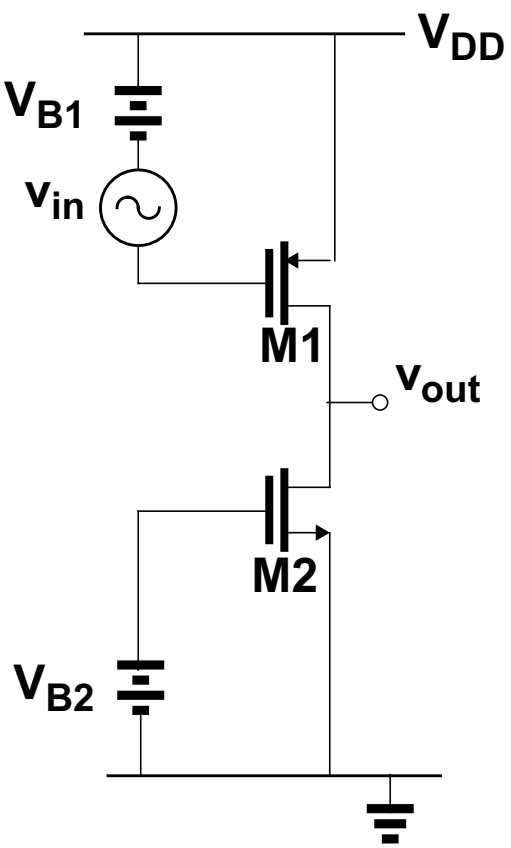

Figure 4a

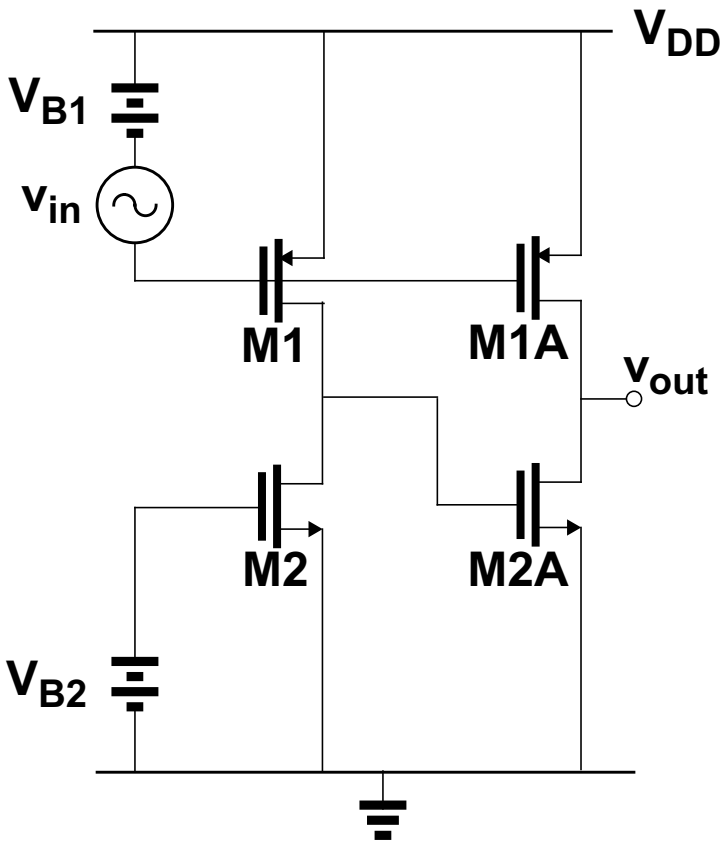

Figure 4b

For the circuits shown in Figure 4a and 4b, assume all transistors are operating in saturation.
Only thermal noise sources need be considered.

Take Boltzmann's constant $k=13.8X10^{-24}J/^oK$, temperature $T=300^oK$.

(i) Draw the small-signal model for the circuit shown in Figure 4a.
What is the low-frequency small-signal voltage gain (v_{out}/v_{in}) in terms of the small-signal parameters of M1 and M2?

(ii) What is the input-referred noise voltage density in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T?

(iii) Calculate the input-referred noise voltage density if $g_{m1}=100\mu A/V$, $g_{m2}=40\mu A/V$, $g_{ds1}=g_{ds2}=2\mu A/V$.
What is the noise voltage density at the output?
(Note: the units $\mu A/V$ are equivalent to μS).

(iv) The gain stage shown in Figure 4a is cascaded with an identcal gain stage, with identical transistor dimensions and biasing conditions, as shown in Figure 4b. Calculate the input-referred noise voltage density of this circuit.
What is the total input-referred noise in a bandwidth of 1MHz to 10MHz?