# Solutions UE4002 Autumn 2005

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an nmos in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.
In each question, capacitances other than those mentioned may be ignored.

## Question 1

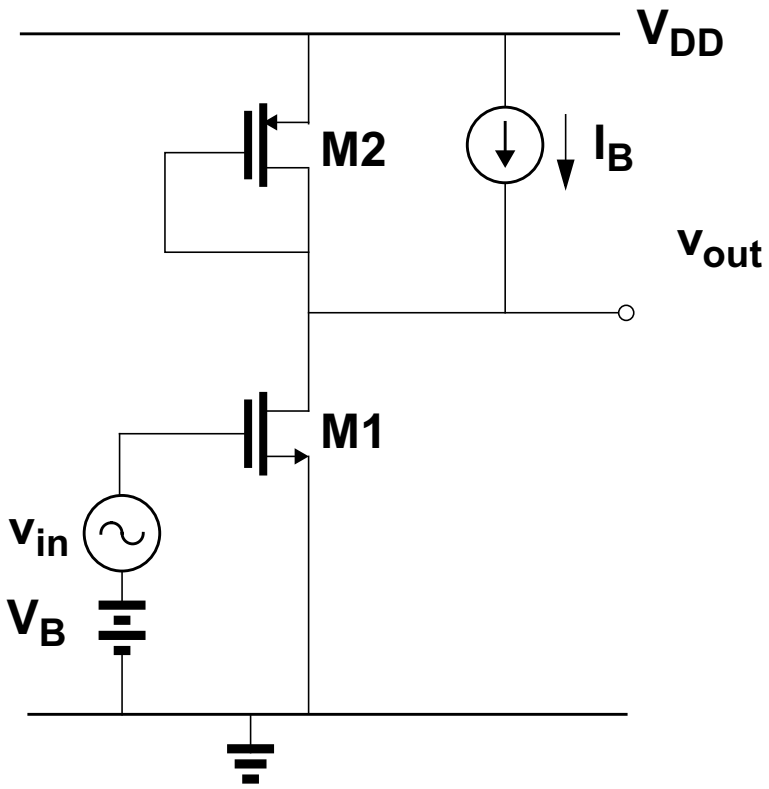
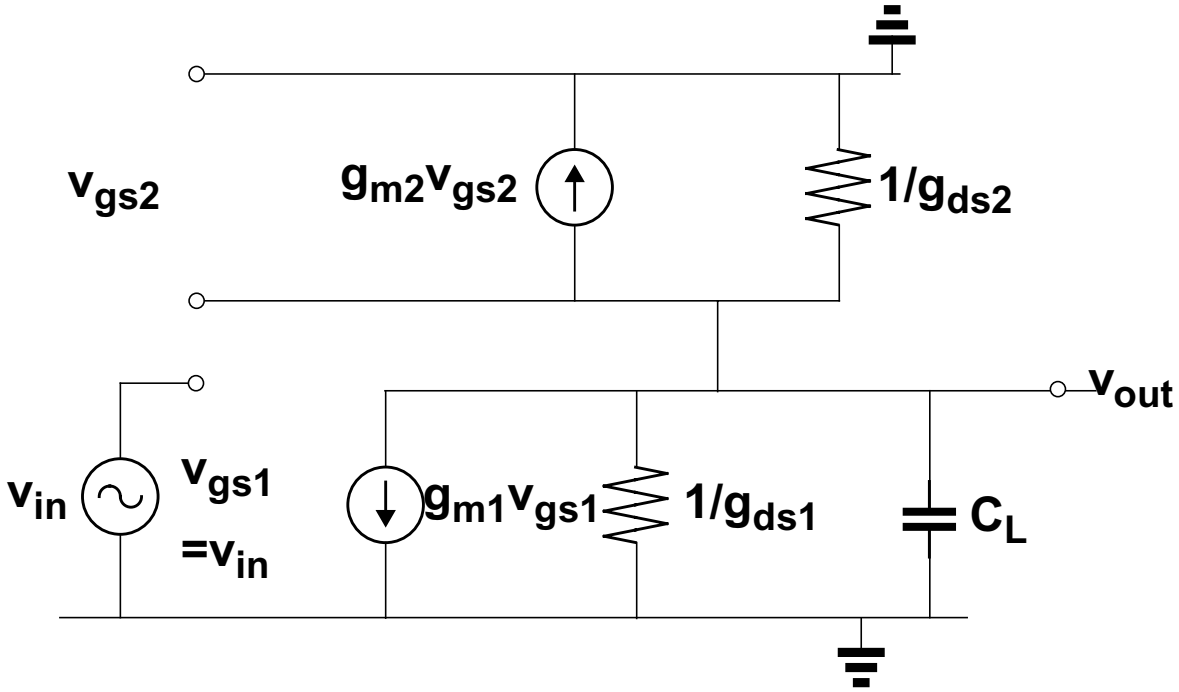



**Figure 1**

For the questions below you may assume $g_{m1},g_{m2}>>g_{ds1},g_{ds2}$ and that all devices are biased in saturation.

(i) Figure 1 shows a gain stage with a diode-connected load. An additional DC bias current is injected from $V_{DD}$ into the output node. Draw the small-signal model for this circuit.
(ii) Derive an expression for the small signal voltage gain ($v_{out}/v_{in}$).
(iii) Calculate the small-signal voltage gain ($v_{out}/v_{in}$) in dB if $V_B$=1V,$|V_{GS2}|$=1.75V, $V_{tn}=|V_{tp}|$=0.75V, $I_{D1}$=200µA, $I_B$= 150µA.
(iv) Calculate the small-signal voltage gain in dB if the additional bias current $I_B$ is reduced to zero. Assume $V_B$ is unchanged.

(i) Figure 2 shows a gain stage with a diode-connected load. Draw the small-signal model for this circuit.
Note DC bias current source is open-circuit in small-signal model.




(ii) Derive an expression for the low-frequency small signal voltage gain ($v_{out}/v_{in}$).
Current at output node

$$g_{m1}v_{gs1} + g_{m2}v_{gs2} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$g_{m1}v_{in} + g_{m2}v_{out} + v_{out}g_{ds1} + v_{out}g_{ds2} = 0$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \cong -\frac{g_{m1}}{g_{m2}}$$

Alternatively recognise that the current of the current-source $g_{m2}v_{gs2}$ is determined by voltage across its terminals i.e. is equivalent to a resistance $1/g_{m2}$.
Since $1/g_{m2} << 1/g_{ds2}$, $1/g_{m2} << 1/g_{ds1}$, can write directly

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2}}$$

(iii) Calculate the small-signal voltage gain ($v_{out}/v_{in}$) if $V_B$=1V,$|V_{GS2}|$=1.75V, $V_{tn}=|V_{tp}|$=0.75V, $I_{D1}$=200µA, $I_B$= 150µA.

150µA supplied by $I_B$, 50µA by M2

$$g_{m1} = \frac{2I_{D1}}{(V_{GS1}-V_{tn})} = \frac{2\times 200\mu A}{1-0.75} = 1600\mu A/V$$

$$g_{m2} = \frac{2|I_{D2}|}{(|V_{GS2}|-|V_{tp}|)} = \frac{2\times 50\mu A}{1.75-0.75} = 100\mu A/V$$

Low-frequency gain given by

$$\frac{v_{out}}{v_{in}} \cong -\frac{g_{m1}}{g_{m2}} = \frac{1600\mu A/V}{100\mu A/V} = -16 = \underline{\underline{24dB}}$$

(iv) Calculate the small-signal voltage gain in dB if the additional bias current $I_B$ is reduced to zero. Assume $V_B$ is unchanged.

If $I_B$ is removed, all $I_{D1}$ flows through M2 i.e $I_{D2}$ will increase from 50µA to 200µA, a factor 4.
$|V_{GS2}|$ - |Vtp| will then double from 1V to 2V

$$g_{m1} = \frac{2I_{D1}}{(V_{GS1}-V_{tn})} = \frac{2\times 200\mu A}{1-0.75} = 1600\mu A/V$$

$$g_{m2} = \frac{2|I_{D2}|}{(|V_{GS2}|-V_{tp})} = \frac{2\times 200\mu A}{2} = 200\mu A/V$$

Low-frequency gain given by

$$\frac{v_{out}}{v_{in}} \cong -\frac{g_{m1}}{g_{m2}} = \frac{2000\mu A/V}{200\mu A/V} = -8 = \underline{\underline{18dB}}$$

## Question 2

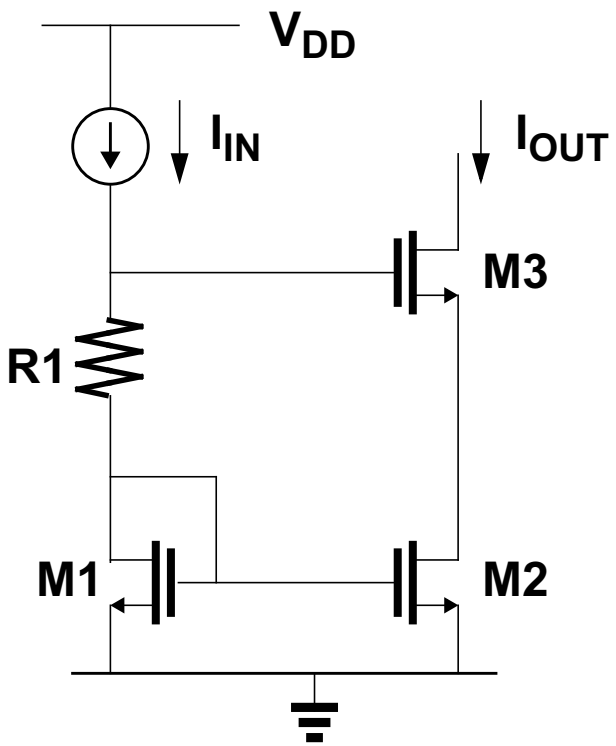



**Figure 2**

Figure 2 shows a cascoded current mirror.
Assume $K_n'=200\mu A/V^2$, $V_{tn}=800mV$.
All transistors have W/L=12.5/2.

(i) If $I_{IN}=I_{OUT}=100\mu A$, what is the minimum voltage at the output node, i.e. the drain of M3, such that all transistors are biased in saturation?
What minimum value of R1 is required to ensure M2 is in saturation?

(ii) What value of R1, and W/L of M2 would be required to increase the output current to 400μA and still ensure all transistors are in saturation?

(iii) It is required to measure the small-signal output resistance of the current mirror (i.e. the small-signal resistance looking into the drain of M3). Draw a small signal model showing how this can be done.

(iv) Derive an expression for the small-signal output resistance. Reduce this to its simplest form assuming $g_{m1}, g_{m2}, g_{m3} >> g_{ds1}, g_{ds2}, g_{ds3}$.

(i) If $I_{IN}=I_{OUT}=100\mu A$, what is the minimum voltage at the output node, i.e. the drain of M3, such that all transistors are biased in saturation?
What minimum value of R1 is required to ensure M2 is in saturation?

Bias current of M1, M2, M3 is 100µA. All have same W/L so same $V_{GT}$

$$I_{D1} = \frac{K_n'}{2}\frac{W}{L}(V_{GS1}-V_t)^2 \Rightarrow V_{GS1}-V_t = \sqrt{\frac{2I_{D1}}{K_n'\frac{W}{L}}} = \sqrt{\frac{2\cdot 100\mu A}{200\mu A/V^2\frac{12.5}{2}}}$$

$$V_{GS1}-V_t = 400mV$$

$$V_{D4min} = (V_{GS2}-V_t)+(V_{GS3}-V_t) = 0.4V+0.4V = \underline{0.8V}$$

Then

$$V_{G3} = (V_{GS2}-V_t)+(V_{GS3}-V_t)+V_t = 0.4V+0.4V+0.8V = 1.6V$$

$$R_1 = \frac{V_{G3}-V_{G1}}{I_{IN}} = \frac{1.6V-1.2V}{100\mu A} = \underline{4k\Omega}$$

(ii) What value of R1, and W/L of M2 would be required to increase the output current to 400µA and still ensure all transistors are in saturation?

$$I_{D2} = \frac{K_n'}{2}\frac{W}{L}(V_{GS2}-V_t)^2$$

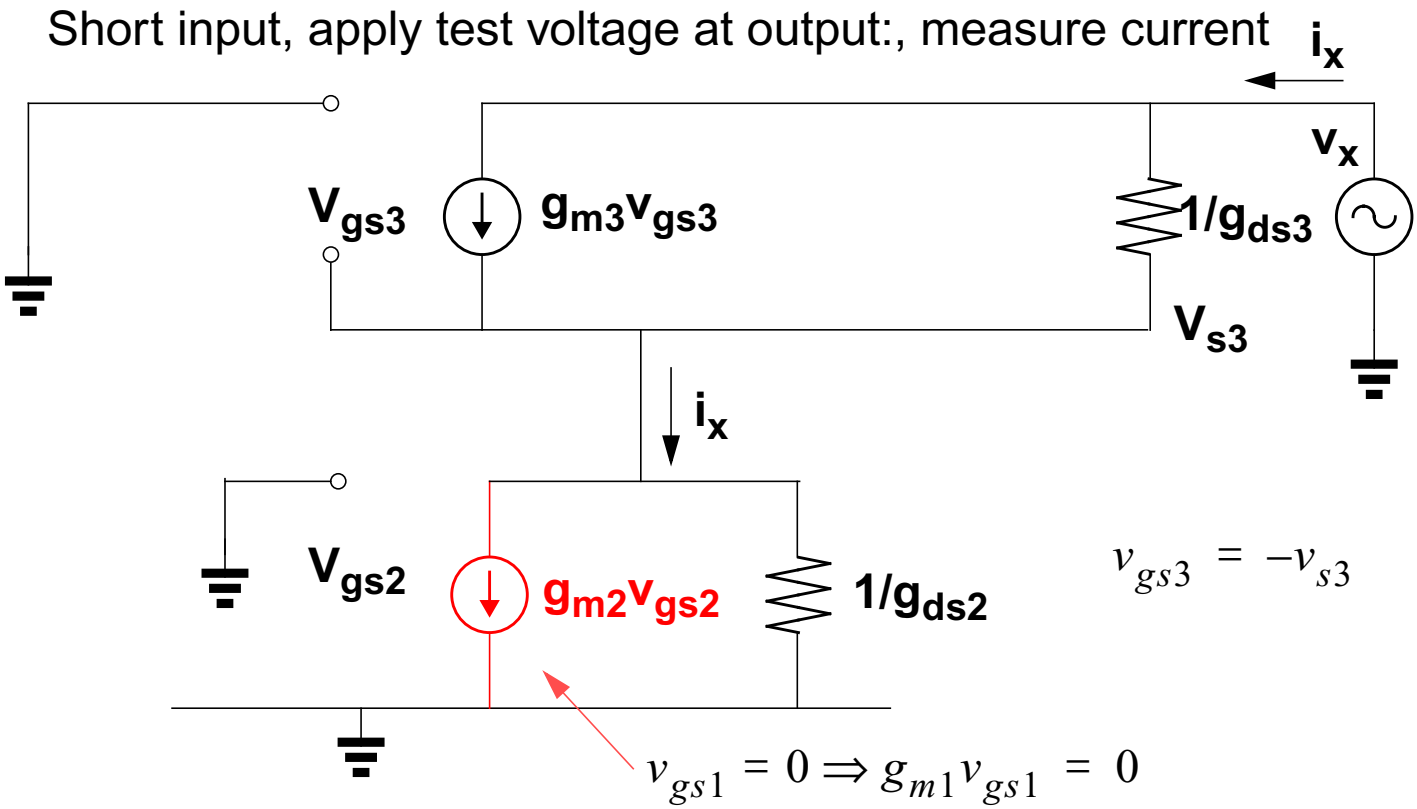
For $I_{D2}$ = 400µA, same $V_{GS}$-$V_t$, W/L needs to increase by 4 times, e.g. to 50/2

For ID4 = 400µA, $V_{GS3}$-$V_t$ needs to increase by 2 times, i.e. to 0.8V, so $V_{G3}$=2V

$$R_1 = \frac{V_{G3}-V_{G1}}{I_{IN}} = \frac{2V-1.2V}{100\mu A} = \underline{8k\Omega}$$

(iii) It is required to measure the small-signal output resistance of the current mirror (i.e. the small-signal resistance looking into the drain of M3). Draw a small signal model showing how this can be done.

Cascode: Output Resistance $R_{out}$




(iv) Derive an expression for the small-signal output resistance.

$$i_x = g_{m3}v_{gs3} + (v_x - v_s)g_{ds3}$$

$$i_x = -g_{m3}v_{s3} + v_x g_{ds3} - v_s g_{ds3}$$

Since $v_{s3} = \dfrac{i_x}{g_{ds2}}$

$$i_x = -g_{m3}\frac{i_x}{g_{ds2}} + v_x g_{ds3} - \frac{i_x}{g_{ds2}}g_{ds3}$$

$$r_{out} = \frac{v_x}{i_x} = \frac{1}{g_{ds3}}\left(1 + \frac{g_{m3}}{g_{ds2}} + \frac{g_{ds3}}{g_{ds2}}\right) \approx \frac{1}{g_{ds2}}\left(\frac{g_{m3}}{g_{ds3}}\right)$$

**Question 3**

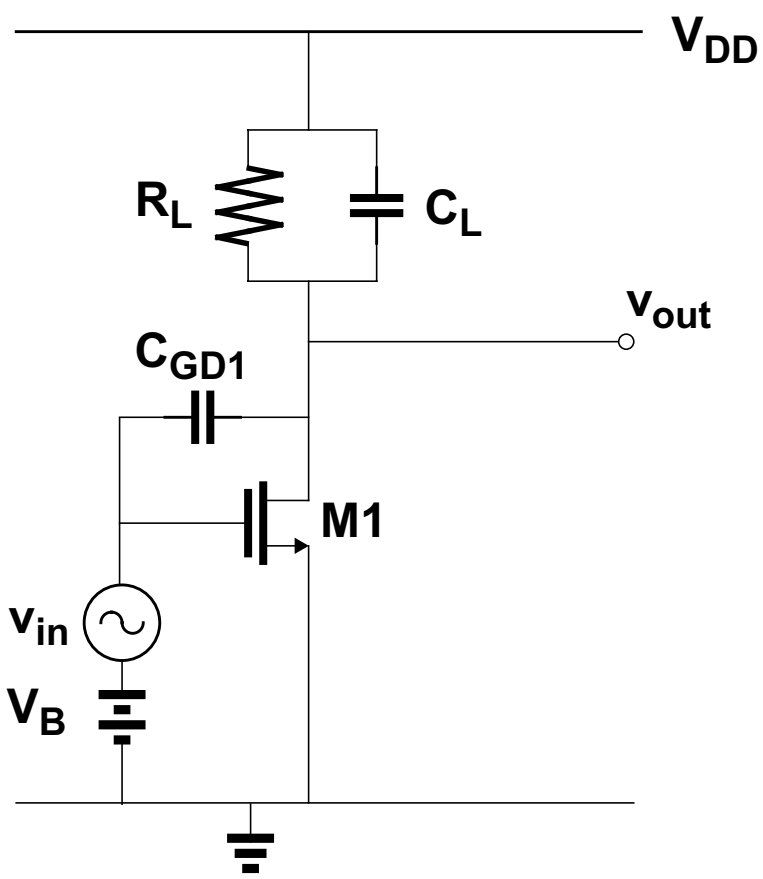
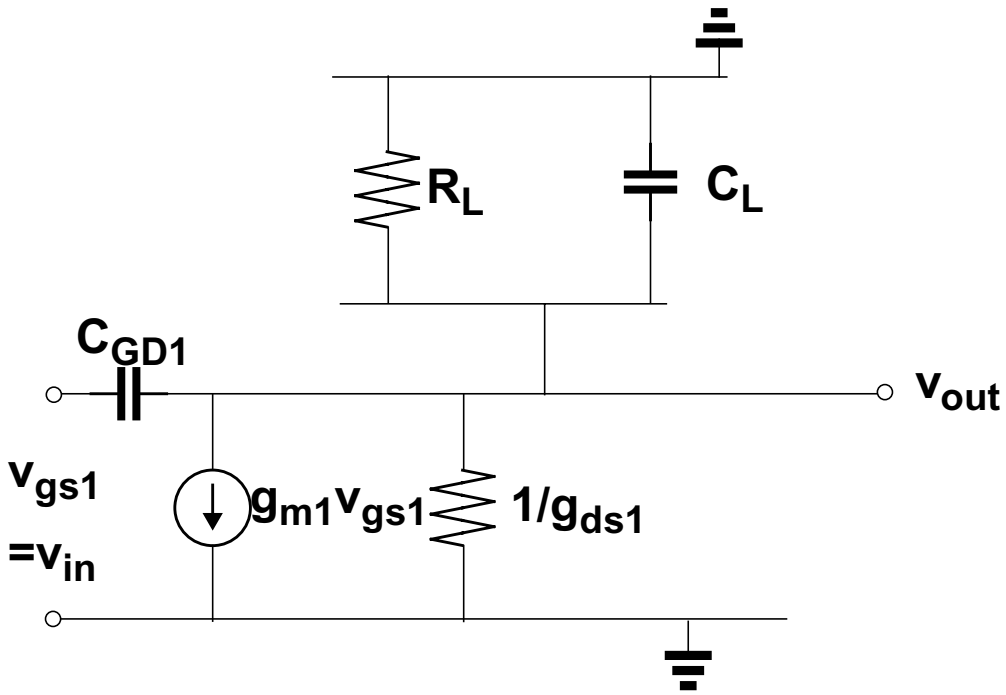



**Figure 3**

For the questions below you may assume $g_{m1} >> g_{ds1}$ , $g_{ds1} << 1/R_L$ and that M1 is biased in saturation.

(i) Figure 3 shows a gain stage with an RC load. Draw the small-signal model for this circuit.
(ii) Ignoring all capacitances except $C_{GD1}$ and $C_L$, derive an expression for the high-frequency transfer function.
(iii) Calculate the low-frequency gain ($v_{out}/v_{in}$) and the pole and zero frequencies if $V_B$=1V,$V_{GS2}$=1.75V, $V_{tn}$=0.75V, $I_{D1}$=250μA, $C_{GD1}$=0.1pF, $C_L$=4.9pF,$R_L$=10kΩ.
(iv) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the pole and zero frequencies.

(i) Figure 2 shows a gain stage with a RC load. Draw the small-signal model for this circuit.




(ii) Ignoring all capacitances except $C_{GD1}$ and $C_L$, derive an expression for the high-frequency transfer function.

KCL at output node:

$$(v_{out} - v_{in})sC_{GD1} + g_m v_{in} + v_{out}g_{ds} + v_{out}/R_L + v_{out}sC_L = 0$$

$$v_{in}(g_m - sC_{GD1}) + v_{out}(g_{ds} + 1/R_L + s(C_{GD1} + C_L)) = 0$$

$$a(s) = \frac{v_{out}}{v_{in}}(s) = -\frac{g_m - sC_{GD1}}{g_{ds} + 1/R_L + s(C_{GD1} + C_L)}$$

$$a(s) = \frac{v_{out}}{v_{in}}(s) = -\frac{g_m}{g_{ds} + 1/R_L}\left(\frac{1 - s\frac{C_{GD1}}{g_m}}{1 + \frac{s(C_{GD1} + C_L)}{g_{ds} + 1/R_L}}\right)$$

(iii) Calculate the low-frequency gain ($v_{out}/v_{in}$) and the pole and zero frequencies if $V_B$=1V,$V_{GS2}$=1.75V, $V_{tn}$=|$V_{tp}$|=0.75V, $I_{D1}$=250μA, $C_{GD1}$=0.1pF, $R_L$=4.9pF.

$$g_{m1} = \frac{2I_{D1}}{(V_{GS1}-V_{tn})} = \frac{2\times 250\mu A}{1-0.75} = 2000\mu A/V$$

Low-frequency gain given by

$$\frac{v_{out}}{v_{in}} \cong -\frac{g_{m1}}{g_{ds1}+1/R_L} \approx -g_{m1}R_L = -2000\mu A/V \times 10k = -20 \Rightarrow 26dB$$

Zero frequency given by

$$|\omega_z| = \frac{g_{m1}}{C_{GD1}} = \frac{2000\mu A/V}{0.1\,pF} = \underline{20Grad/s}$$

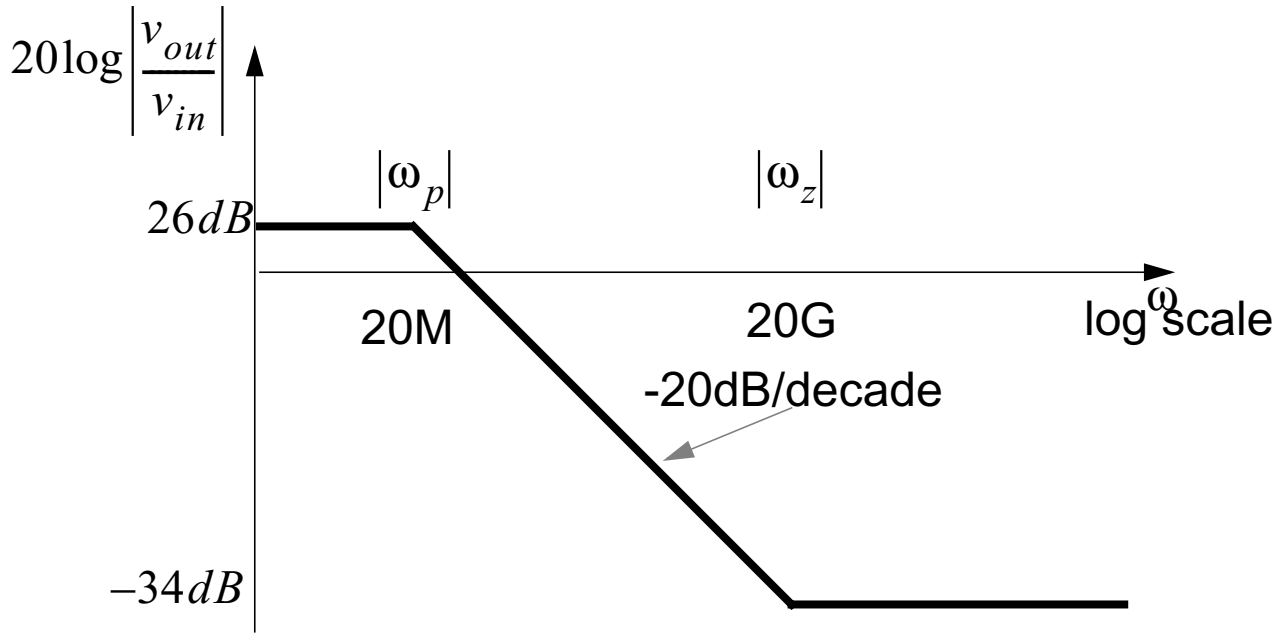
Pole frequency given by

$$|\omega_p| = \frac{g_{ds}+\frac{1}{R_L}}{C_L+C_{GD1}} \approx \frac{\frac{1}{R_L}}{C_L+C_{GD1}}$$

$$|\omega_p| = \frac{\frac{1}{10k\Omega}}{4.9\,pF+0.1\,pF} \approx \frac{1}{10k\Omega\times 2\,pF} = \underline{20Mrad/s}$$

(iv) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the pole and zero frequencies.

Zero is 3 decades down, so gain at high frequecies = -34dB



## Question 4

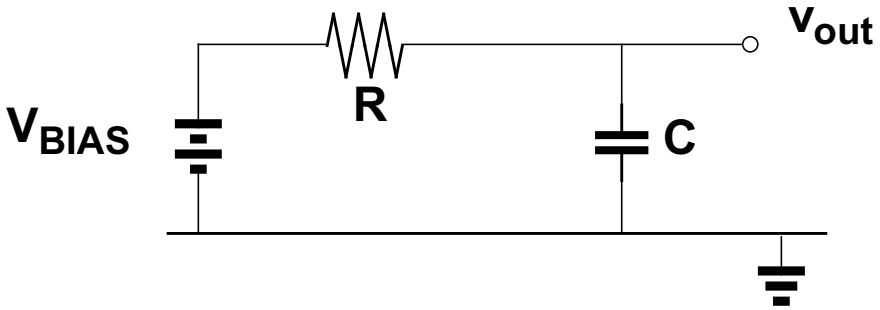


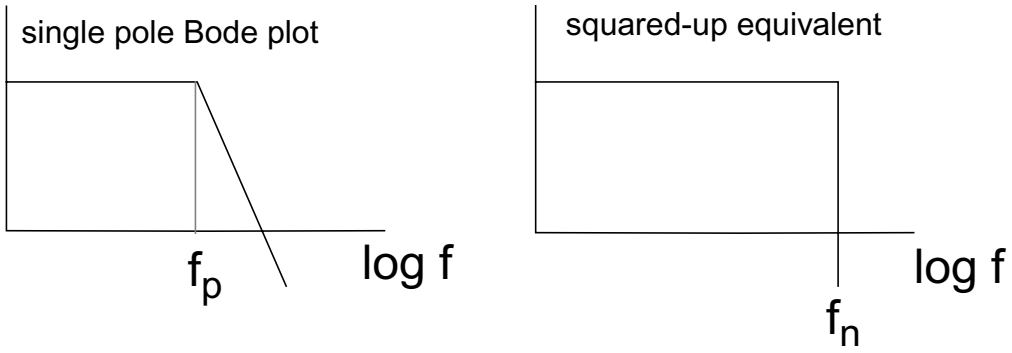

**Figure 4**

For numerical calculations take Boltzmann's constant k=1.38X10$^{-23}$J/$^{o}$K, temperature T=300$^{o}$K.

(i) Show that the total integrated thermal noise voltage at node $v_{out}$ in Figure 4 is

$$v_{nout}^2 = \frac{kT}{C}$$

where k is Boltzmann's constant, and T is the temperature.
You may assume the following:




For the area underneath the curves to be the same then $f_n=(\pi/2)*f_p$

(ii) If R= 1kΩ and C=1pF calculate the total thermal noise in $V_{rms}$ at node $v_{out}$ in Figure 4?

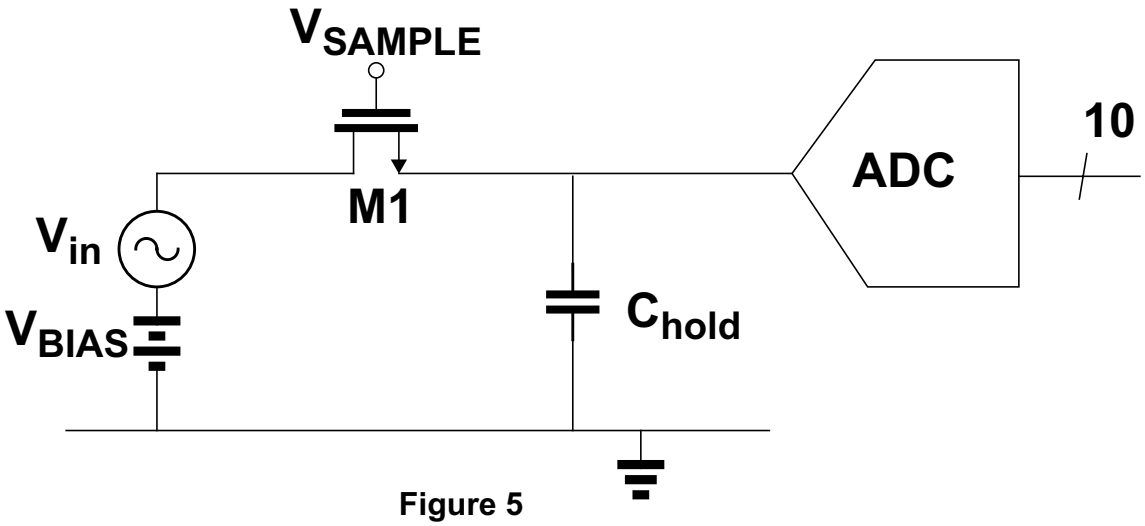



**Figure 5**

(iii) Figure 5 shows a sampling circuit preceding a 10-bit A/D converter. The sampling switch M1 is turned on.If the A/D converter has an input range of 1Vrms, and the noise budget for the sampling circuit is 0.1 LSB, what is the minimum value required for $C_{hold}$?

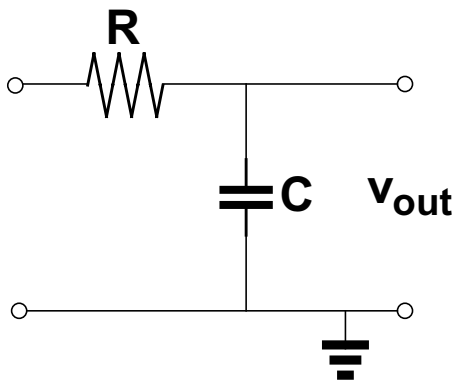
(iv) If a 12-bit A/D converter is used with the same input range, and the noise budget for the sampling circuit is kept at 0.1LSB, what is the new minimum value required for $C_{hold}$?

Solution

(i) Show that the total integrated thermal noise voltage at node $v_{out}$ in Figure 4 is

$$v_{nout}^2 = \frac{kT}{C}$$

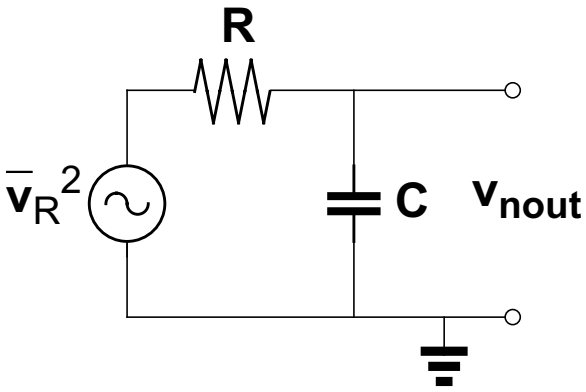
where k is Boltzmann's constant, and T is the temperature.




The resistor R generates a noise voltage $v_r^2 = 4kTR$

The noise from the resistor is filtered by the pole formed by R,C

Pole frequency: $f_o = \frac{1}{2\pi RC}$




Total output noise noise power:

$$v_{nout}^2 = v_r^2 \cdot \frac{\pi}{2} \cdot f_o = 4kTR \cdot \frac{\pi}{2} \cdot \frac{1}{2\pi RC} = \frac{kT}{C}$$

(ii) If R= 1kΩ and C=1pF what is the total thermal noise in Vrms at node $v_{out}$ in Figure 4?

$$v_{nout} = \sqrt{\frac{kT}{C}} = \sqrt{\frac{1.38\times10^{-23}\,300}{1\,pF}} = \underline{\underline{64\mu V_{rms}}}$$

(iii) Figure 5 shows a sampling circuit preceding a 10-bit ADC. The sampling switch M1 is turned on. If the A/D converter has an input range of 1Vrms, and the noise budget for the sampling circuit is 0.1 LSB, what is the minimum value required for $C_{hold}$?

10-bit ADC full-scale input range = 1Vrms

ADC LSB = $1V/2^{10}$ =1mVrms

The sample-and-hold circuit is a first-order circuit => noise is

$$v_n^2 = \frac{kT}{C}$$

For error budget want $\bar{v}_n$ < LSB/10 = 0.1mV

$$\sqrt{\frac{kT}{C}} < 0.1mV \Rightarrow C > \frac{kT}{(0.1mV)^2} \Rightarrow C > \frac{1.38\times10^{-23}\times 300}{(0.1mV)^2} = \underline{\underline{0.41\,pF}}$$

(iv) If a 12-bit ADC is used, and the noise budget for the sampling circuit is kept at 0.1LSB, what is the new minimum value required for $C_{hold}$?

12-bit ADC full-scale input range = 1Vrms

ADC LSB = $1V/2^{10}$ =0.25mV

The sample-and-hold circuit is a first-order circuit => noise is

$$v_n^2 = \frac{kT}{C}$$

For error budget want $\bar{v}_n$ < LSB/10 = 0.025mV

$$\sqrt{\frac{kT}{C}} < 0.1mV \Rightarrow C > \frac{kT}{(0.025mV)^2} \Rightarrow C > \frac{1.38\times10^{-23}\times 300}{(0.025mV)^2} = \underline{\underline{6.6\,pF}}$$