Solutions UE 4008 Summer 2011

Question 1

a) The 90nm node (ITRS Roadmap for Semiconductors) is generally considered to be the end of the "Traditional Scaling Era" describe some of the changes in CMOS devices that occurred between 1µm technology to 90nm?
b) What major changes are being introduced beyond the 65nm node?
c) What are the equivalent oxide thickness and the actual thickness in the gate region of a MOS transistor if hafnium oxide with a dielectric constant of 25 is used as the gate dielectric and the resultant capacitance is 3.46 X 10^{-7} F/cm^2?

Given:
The permittivity of free space is 8.86 X 10^{-14} F/cm
The dielectric constant of silicon dioxide is 3.9

a) From 1µm to 90nm

Polysilicon is silicided to reduce resistance
Poly silicon over the N Channel devices is doped N-Type and the Poly over P Channel is doped P type from 130nm node down to match work function differences
Gate oxide becomes nitrided
Strain is introduced with silicon germanium for PMOS and Nitride over films for NMOS
At 220nm to 180nm damascene copper replaces aluminium
Side wall spacers are introduced
At 65nm SiGe Source drains introduce strain to PMOS

b) The major change below 65nm is the introduction of a gate dielectric other than silicon dioxide or nitrided silicon dioxide. High k dielectrics have to be used because of increasing leakage currents in oxide layers. In the move from 90nm to 65nm there was no reduction in the gate dielectric thickness on Intel's process shrink because of the gate leakage problem. On Intel's 45 nm process a replacement gate technology is used where the wafers are processed with a normal polysilicon gate electrode and towards the backend of the process the polygate is etched out and replaced with a metal gate.

c) What are the equivalent oxide thickness and the actual thickness in the gate region of a MOS transistor if hafnium oxide with a dielectric constant of 25 is used as the gate dielectric and the resultant capacitance is 3.46 X 10^{-7} F/cm^2?

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$\varepsilon_{ox} = k\varepsilon_0$$

ε_0 is the permittivi ty of free space

$$k = 3.9$$

$$k_{Ha} = 25$$

k is the dielectric constant of silicon

$$\varepsilon_0 = 8.86 \times 10^{-14} F/cm$$

t_{ox} is the oxide thickness

$$3.46 \text{ x } 10^{-7} = \frac{25 \times 8.86 \times 10^{-14}}{t_{Ha}}$$

$$t_{Ha} = \frac{25 \times 8.86 \times 10^{-14}}{3.46 \text{ x } 10^{-7}}$$

$$t_{Ha} = 6.4 \times 10^{-6} cm$$

$$t_{Ha} = 6.4 \times 10^{-8} m$$

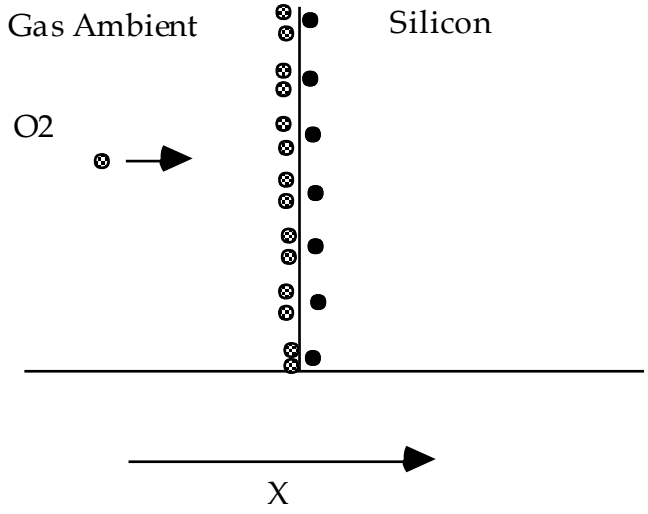
$$t_{Ha} = 64nm$$

Equivalent oxide thickness would be (64/25 x 3.9)= 9.98nm (10nm)

Question 2

a) Explain why the thermal oxidation rate of silicon slows down over time

Initially



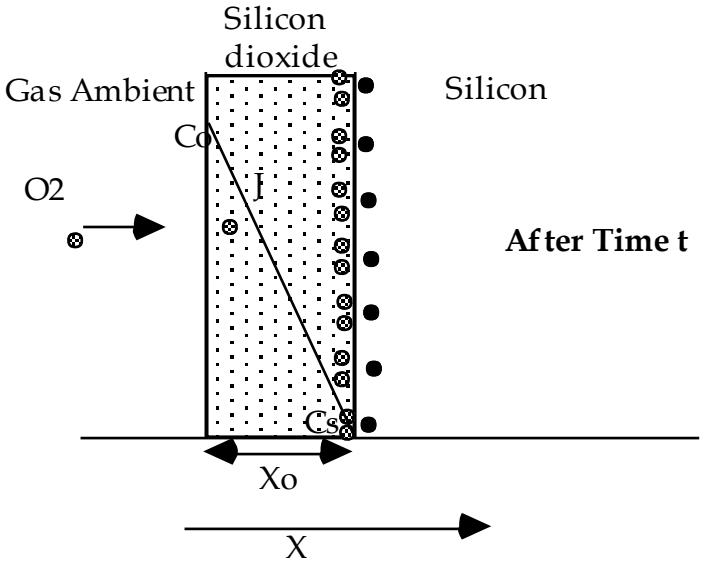
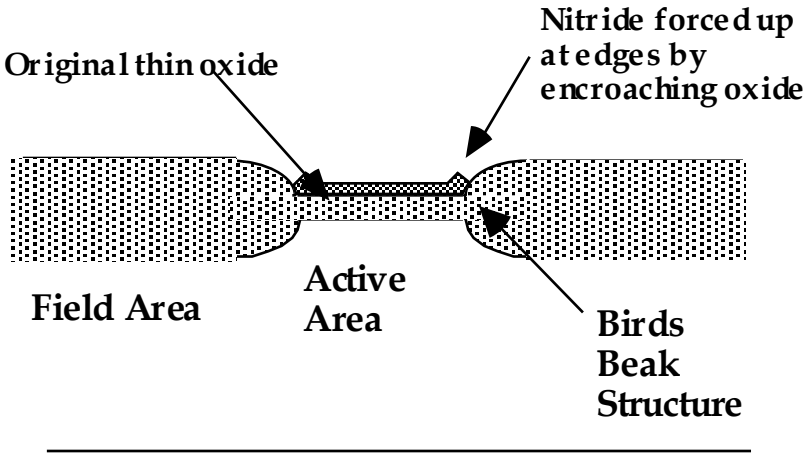


Diagram 1
Reaction controlled
How fast the chemical reaction between the oxidizing species and the silicon can take place
Growth is linear

Diagram 2
Oxide on the surface
Oxidizing species must diffuse through the oxide
As the oxide gets thicker this takes longer
Growth rate becomes dominated by the diffusion time

Growth rate parabolic

b) How is silicon nitride used to form a semi-recessed field oxide profile in CMOS processing



An area of silicon nitride is defined on the surface of the silicon in the "active" areas (areas where the CMOS devices will be located). The wafers are put into an oxidising environment in a hight temp furnace, usually water vapour. The nitride is a very good diffusion barrier to the oxidising agent and prevents the silicon being oxidised to SiO2. The areas outside the nitride are oxidised and the silicon is consumed to form the SiO2 giving the semi-recessed profile.

c) If a <100> silicon wafer on which some areas have an existing silicon dioxide thickness of 200nm and some areas are etched back to bare silicon is thermally oxidised in steam at 1000°C for 60 minutes, what is the final thickness of the oxide on the previously bare areas and on the areas with the existing oxide

Answer

i) To calculate the thickness in the areas which were etched clear before the second oxidation simply read the value from the curve supplied.

On the x axis go to the 60 minute point go up to the intersection with the 1000°C line and read off the thickness.

Ans. 0.35μm

ii) The thickness in the un-etched areas.

This is not a matter of simply adding the thickness already on the wafer to what is grown on bare silicon during the second oxidation.

The thickness of oxide on the wafer from the first oxidation must be converted to the time it would have taken to grow this thickness at the new temperature (1000°C).

The thickness already on the wafer from the first oxidation is 0.2μm.

This would have taken 28 minutes to grow at 1000°C.

This oxide then spends an additional 60 minutes in dry oxygen at 1100°C.

An equivalent of 88 minutes at 1000°C

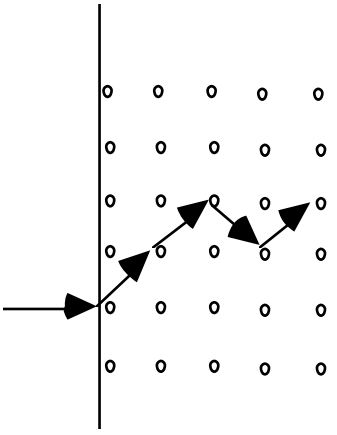
Look up the total thickness from the second curve for an oxidation time of 88 minutes. Ans. = 0.46μm

Question 3

a) In relation to a high energy beam of ions striking the surface of crystalline silicon explain the following terms
   (i) Range
   (ii) Projected range
   (iii) Straggle

Range

Ions with a particular energy collide with the atoms of the crystal lattice. These collisions and interactions mean that the incident ions do not have a straight path to their ultimate resting place in the target material.
The ions do not come to rest until they have lost all of their energy through the collisions, there are 2 types of collision Nuclear and Electronic.

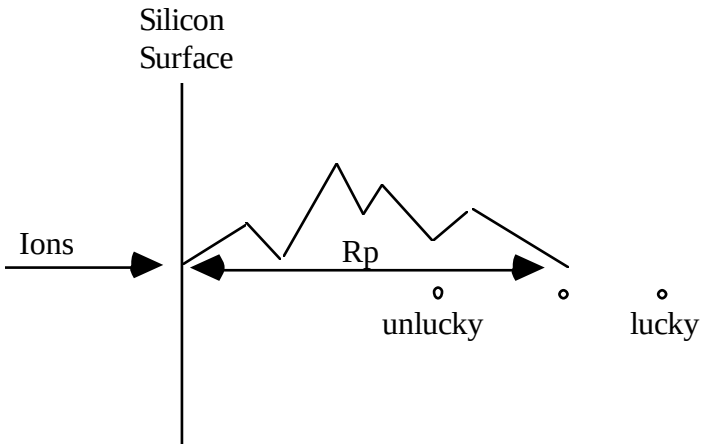


The total Distance Travelled in the Silicon is Called the Range

The total distance the ion travels in the target material is the range generally called R.

Projected range

The projection of the distance along the x-axis is the projected range, Rp, and is the effective distance into the material.



Some ions will be 'lucky' and travel further than the mean distance. Some will be unlucky and travel less far. The distribution is is statistical about a mean point, the peak concentration occurs at the statistical mean, Rp.

Straggle

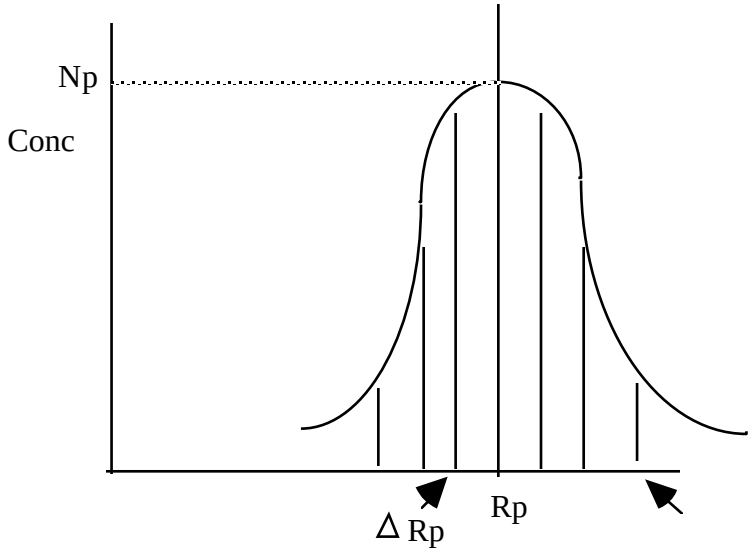
The distribution is characterised by the std. deviation. This is descriptive of the spread of the implanted ions about the mean this standard deviation for ion implant is called the straggle and is assigned the notation ΔRp. The ion distribution is Gaussian with mean Rp and std. deviation ΔRp.

The expression which describes this distribution is :

$$C_{(x,t)} = C_p \exp\left[\frac{-(x-R_p)^2}{2\Delta R_p^2}\right]$$

or

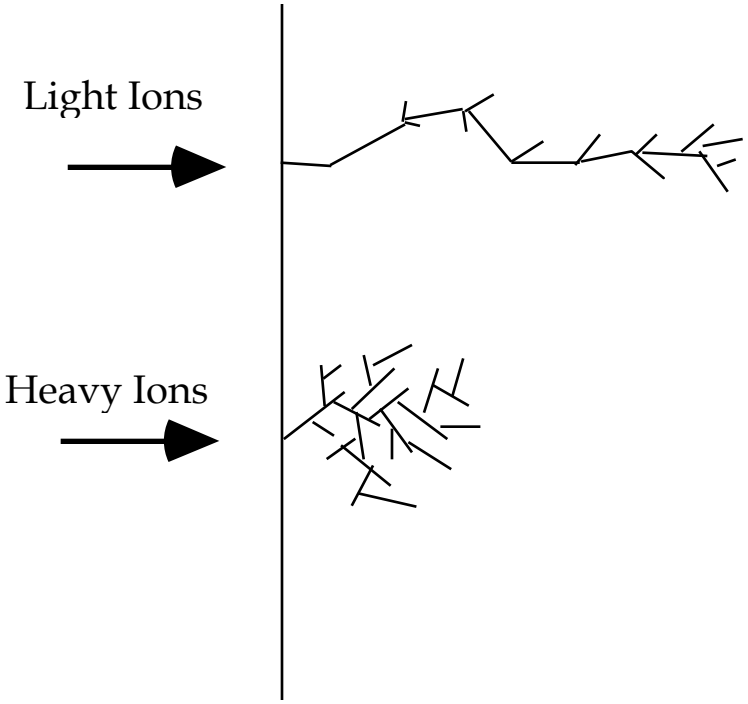
$$N(x) = Np \exp[-(x-Rp)^2/2\Delta Rp^2]$$



Graphic representation of Rp and ΔRp, Np is the peak concentration.

b) Explain the function(s) of the high temperature heat treatment given to wafers following ion implantation

The heat treatment given to wafers following implant serve two functions;
One is to activate the dopant following the implant. Immediately after implant the implanted material is simply sitting in the silicon the dopant atoms have not taken the place of the silicon in the crystal lattice. The heat treatment causes this to happen.
The second thing is that the heat repairs any damage done to the crystal during the implant. Different atoms cause different amounts of damage to the crystal structure. Light ions like boron cause relatively little damage but travel deeper for a given implant energy. Heavier ions/atoms can severely disrupt the crystal structure even to the extent of rendering it amorphous.(Diagram of tree of disorder would be useful)



Counterintuitively above a certain dose when the crystal becomes amorphous less heat (temperature is needed to anneal the damage because of the phenomenon of “Solid Phase Epitaxial Growth” (Plot/Diagram would be useful

c) What energy is needed to place the peak of a phosphorus implant at the silicon/oxide interface if the oxide thickness is 0.07μm, and what thickness of oxide is needed to protect other parts of the silicon from this implant? The implant dose is 1X 10^{16}/cm^{2}and the background concentration is 1 10^{15}/cm^3.

Given:

$C_{(x)} = C_p.\exp[-(x-R_p)^2/2\Delta R_p^2]$

Projected Range and Projected Standard Deviation Graphs attached.

Answer

To place the peak of the implant at the interface, simply a read off of from the projected range graph from 0.07μm on the X axis to the Phosphorus - Oxide line, giving an implant energy of 60KeV

For the thickness of oxide needed to block the implant use the equation

$$Xo = Rp + \Delta Rp\sqrt{2\ln 10 Np / Nb}$$

This assumes that any implant “leaking” into the protected area is less than 1/10 of the background concentration.

From the question R_p is 0.07μm this is a 60KeV implant, ΔR_p is 0.0325μm

N_p is calculated from the equation

$$Q = \sqrt{2\pi} Np \Delta Rp$$

Where Q is the implant dose
From the above figures this gives a value of 1.228 x 10^{21} /cm^3 for N_p

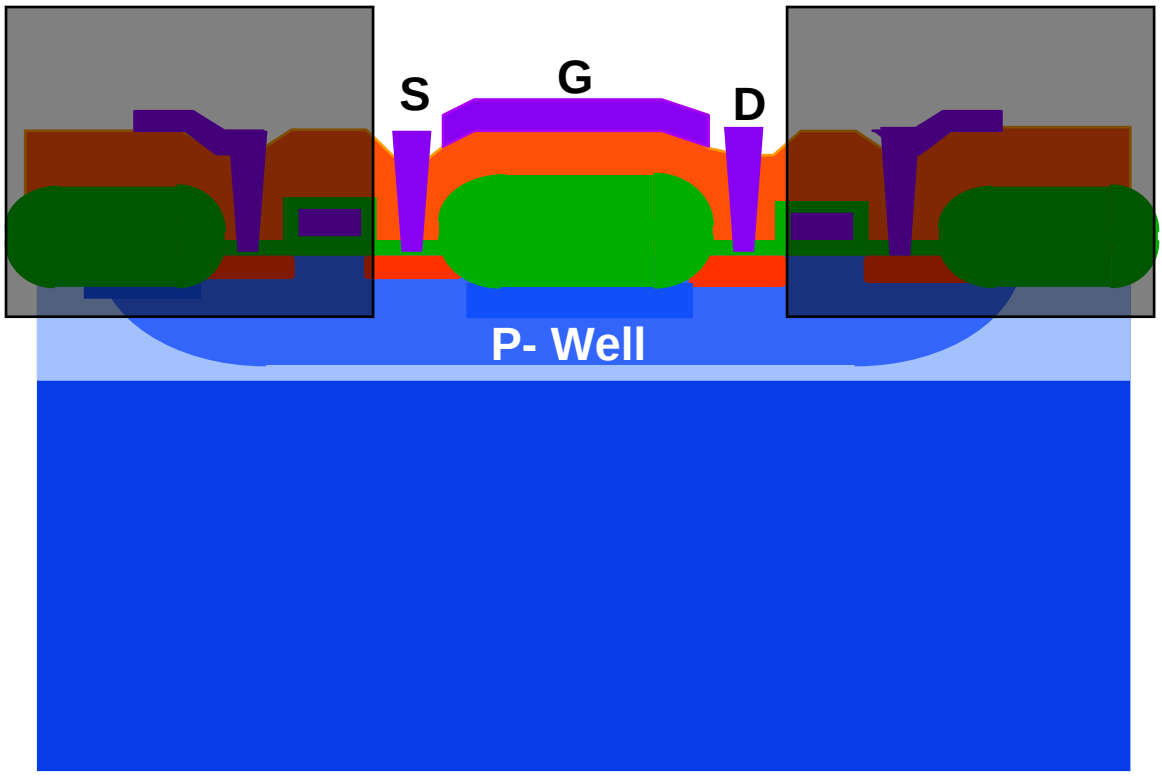
$$Xo = Rp + \Delta Rp \sqrt{2 \ln 10 Np / Nb}$$

Solving this equation for X_o

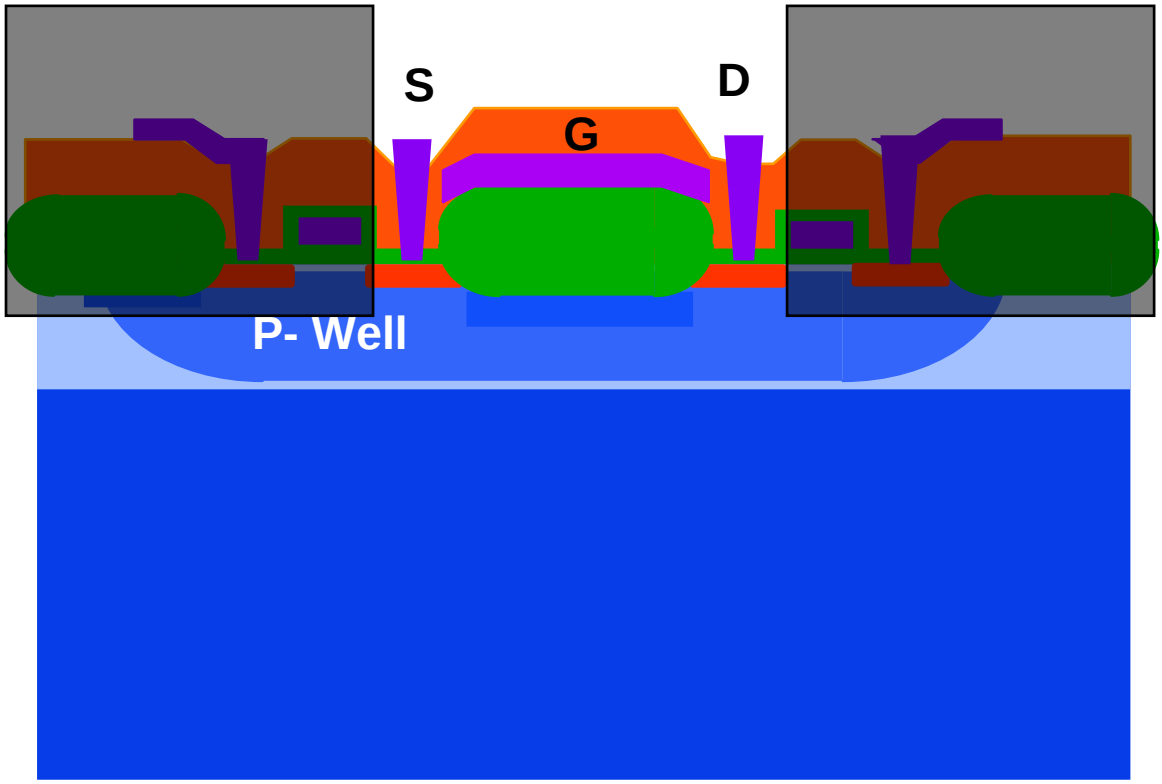
$$Xo = Rp + \Delta Rp \sqrt{32.65}$$
$$Xo = Rp + \Delta Rp (5.71)$$
$$Xo = 0.07 + 0.0325(5.71)$$
$$Xo = 0.07 + 0.186$$
$$Xo = 0.256 \mu m$$

Question 4

a) Describe how parasitic or field devices can be formed in a CMOS process; what measures can be taken to prevent the turn on of these devices, use diagrams to illustrate the answer.



The diagram above shows how a metal gate parasitic MOS transistor can be formed in a CMOS process

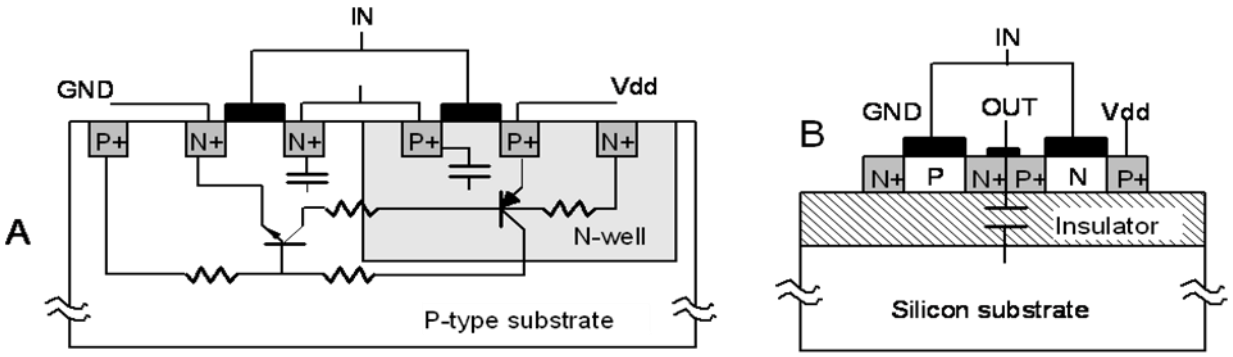


The diagram above shows how a polysilicon gate parasitic MOS transistor can be formed in a CMOS process.

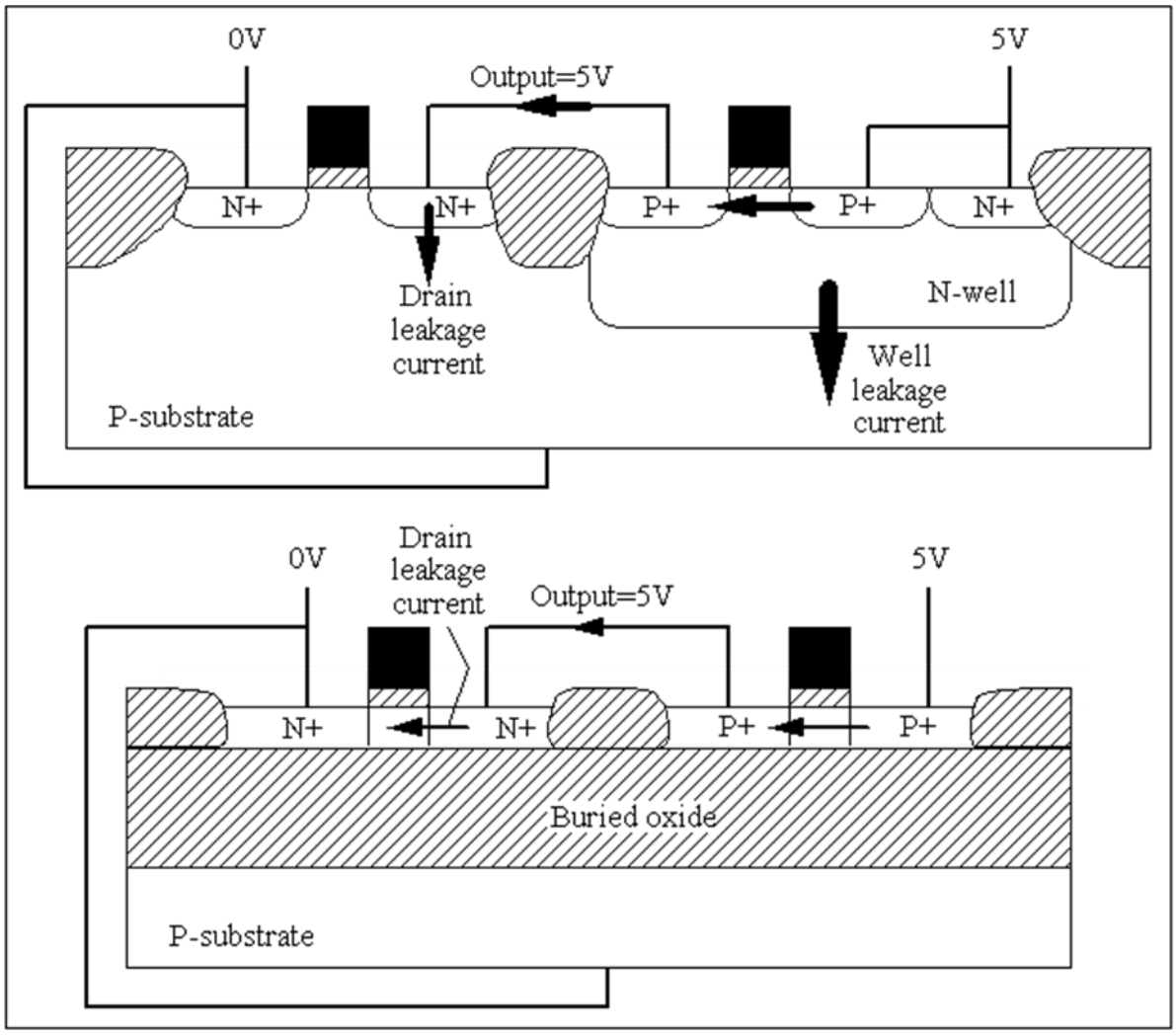
Both diagrams must be fully labelled to show the active devices and how the parasitics are formed between adjacent devices.

The measures to be taken to prevent turn-on of these transistors include field implants under the FOX areas.
Important to mention that implants into the boron regions are more important that those into N type areas because of the difference in segregation coefficients and the fact that boron “sucks out” and phos “piles up. These implants must be carried out prior to the FOX growth process.
Also the thickness of the field oxide (FOX) and the BPSG or other dielectric in the case of the metal gate device and the FOX alone in the case polygate combined with the doping in the “channel region of the field device is sufficient to push the field threshold above the power supply voltage. Typically aiming for a value of 10-20% above the PS value.
This could be illustrated by referring to the Vt equation.

b) Compare an SOI (Silicon-on-Insulator) CMOS process with a bulk silicon process use cross-sectional diagrams to illustrate the answer, state some of the advantages and disadvantages of each, mention the two principal types of SOI transistor configuration.



A: Cross section showing the latchup path in a bulk CMOS inverter.
B: Cross section of an SOI CMOS inverter.
The drain parasitic capacitances are also presented.



Leakage current paths in bulk (top) and SOI (bottom) CMOS inverters. No current flow to the substrate is allowed in SOI.

Advantages
Lower leakage
Less prone to latchup
Inherently radiation hard
Better performance

Disadvantages
Cost of substrates
Quality of substrates

Differentiate between Partially depleted and fully depleted devices (illustrate)
Mention the “kink effect in PD devices.

c) In an NMOS process with a minimum allowed drawn gate length of 2.0μm, a threshold voltage of 0.8V and a power supply voltage of 10V. What is the smallest device that can be used to deliver a current of 10mA between the source and drain?

Given:

$\mu_n = 1000 cm^2/V.s$

$C_{ox} = 5 \times 10^{-8}$ F/ cm^2

Assume that the maximum current will be delivered with the device in saturation, the current equation that determines this current is:

$$I_{DS} = \mu_n C_{ox} W/2L (V_G - V_t)^2$$

To find the minimum sized device that will deliver a 10mA current solve the above equation for W/L, which is the device dimensions.

$$I_{DS} = \mu_n C_{ox} W/2L (V_G - V_t)^2$$

$$W/L = \frac{I_{DS}}{\mu_n \times C_{ox} \times 0.5 \times (V_G - V_t)^2}$$

$$W/L = \frac{10 \times 10^{-3}}{1000 \times 5 \times 10^{-8} \times 0.5 \times (10 - 0.8)^2}$$

$$W/L = 4.72$$

Minimum allowed L is 2μm

$$W/2 = 4.72$$

$$W = 9.44$$

Smallest transistor to deliver 10mA

$2 \times 9.44\mu$m

Or more realistically 2×9.5 or $2 \times 10\mu$m