PHOTOLITHOGRAPHY

PHOTOLITHOGRAPHY
Overview

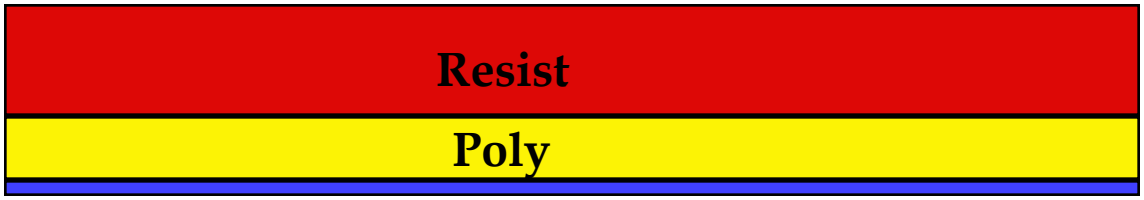
- PROCESS INTRODUCTION
- LITHOGRAPHY PROCESS
- INSPECTION

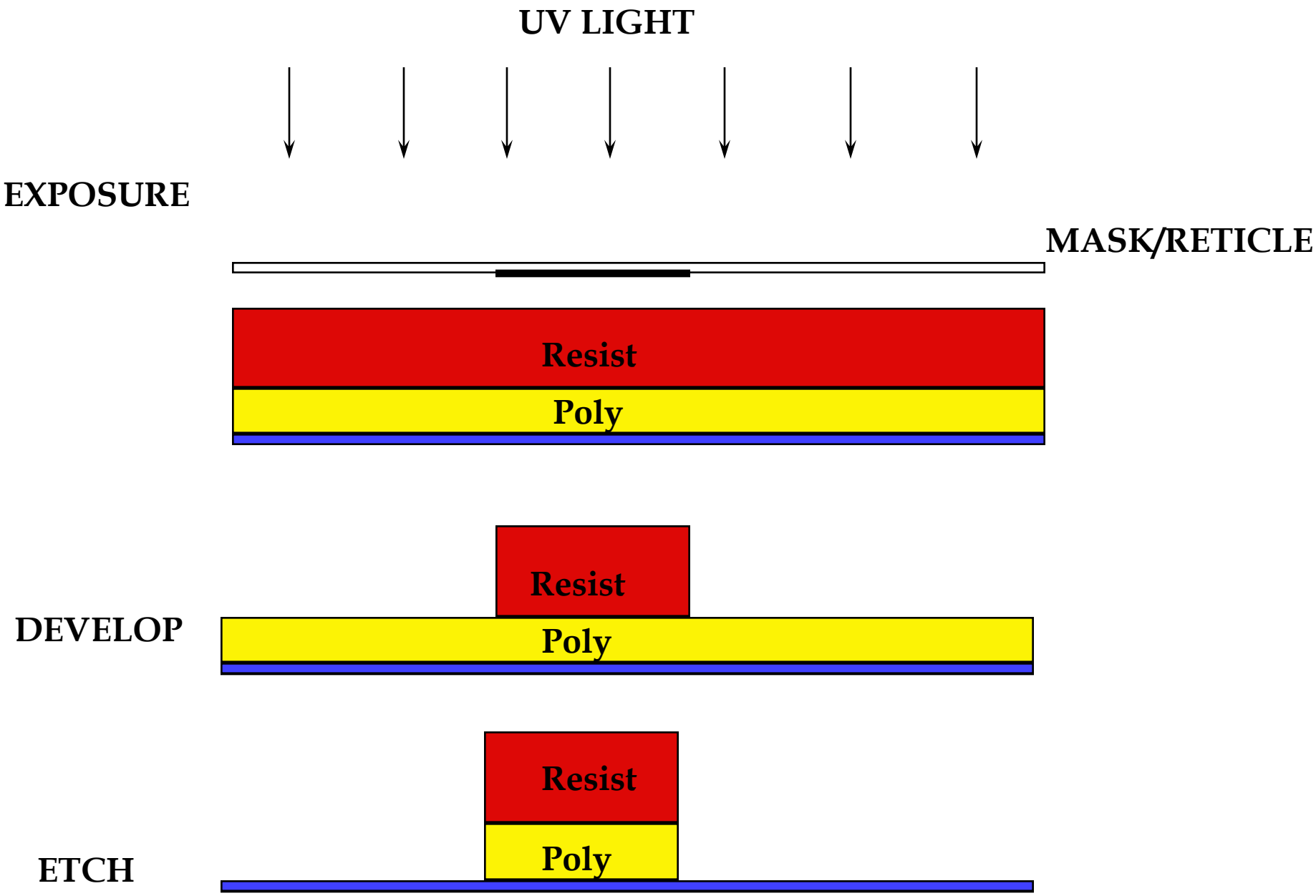
Overview

OXIDE

POLY DEPOSITION

RESIST APPLICATION





Resist Strip

Introduction

- Process is carried out in the ‘yellow room’ as white light will expose the resist
  - The UV element of white light
- Environmental conditions (temperature, humidity) are carefully controlled
  - Humidity in particular affects adhesion of the resist
- Very clean processing conditions (class 10 or better) are required as any defects on the reticle will be printed on every field
  - With a mask on every wafer

PHOTORESIST

- Light sensitive material which is spun on wafer surface
- Photoresist is exposed and developed during the photolithography process to generate the final image
- Two Types of Resist
  - POSITIVE RESIST - Exposed areas of resist are removed during the develop step
  - NEGATIVE RESIST - Unexposed areas of resist are removed during the develop step

POSITIVE PHOTORESIST

- Resin based polymer containing a photoactive compound (PAC)
- Resists used in IC manufacturing are in liquid form.
- There are Three main components
  1. DQN materials ((Diazoquinones)
  2. Novalak, an organic resin
  3. Solvents
- The first two are Photoactive Compounds (PAC)

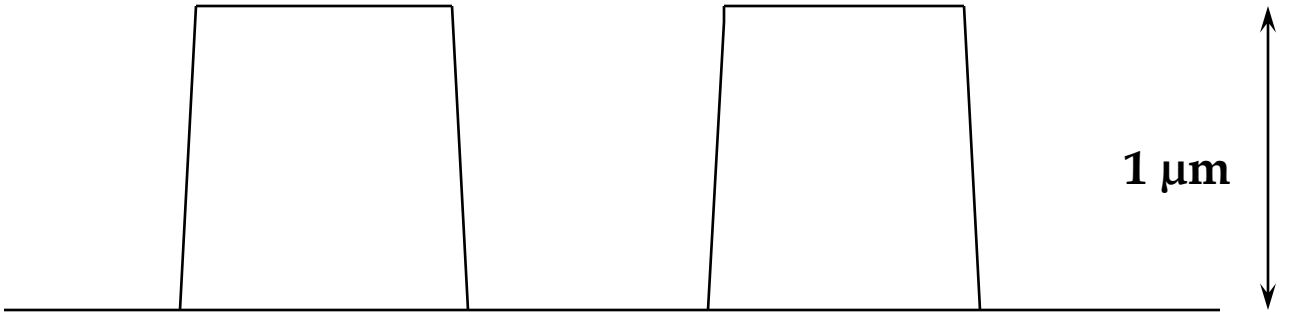
POSITIVE RESIST

- The DNQ prevents dissolution of the Novalak resin in developer
- When exposed to UV radiation the chemical structure of the DNQ changes and becomes soluble in developer solution
- Unexposed areas of resist are also soluble (barely) in developer solution. Difference in develop rates between exposed and unexposed areas is ~1000:1

POSITIVE RESIST

- Positive resist used in all small geometries (<3 Microns)

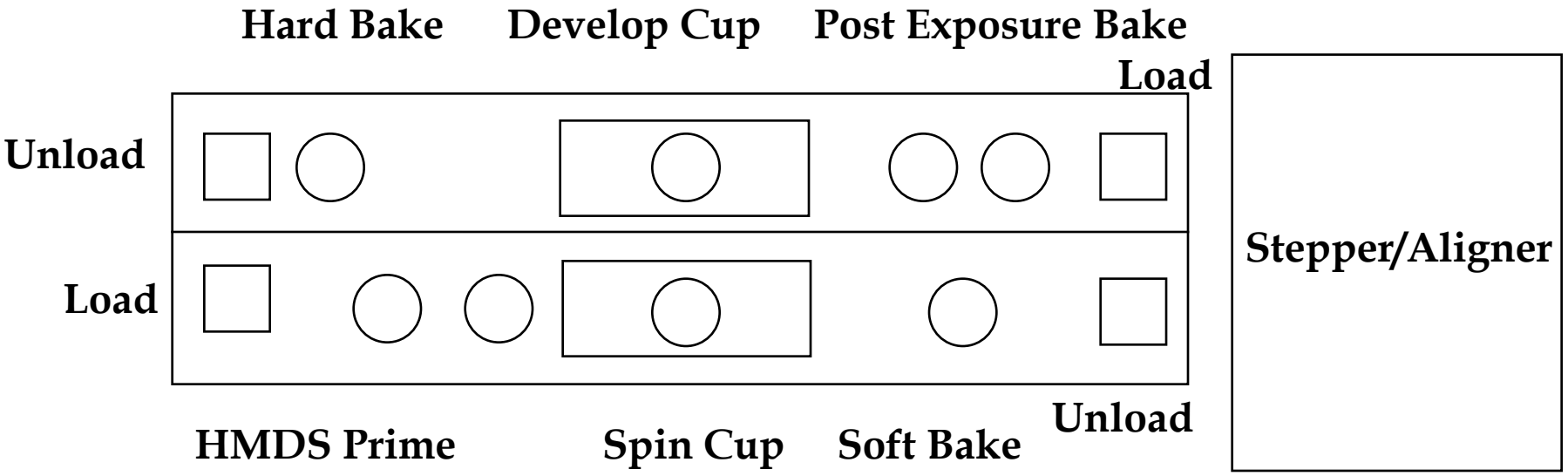
- Resist profiles of 90º are possible



Lithography Process

1. Dehydrate Bake
2. Surface Prime
3. Resist Spin
4. Soft Bake
5. Exposure
6. Post Exposure Bake
7. Develop
8. Hard Bake
9. Inspect

Equipment Layout



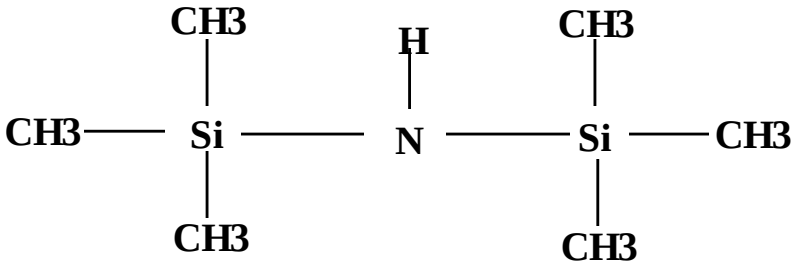
1 DEHYDRATE BAKE

- Moisture on wafer surface will affect adhesion of the resist to the wafer
- Wafers are baked at ‘high temperatures’ (250ºC) for up to 30 minutes
- Vacuum ovens can also be used as water boils at a lower temperature under vacuum

2 HMDS PRIME

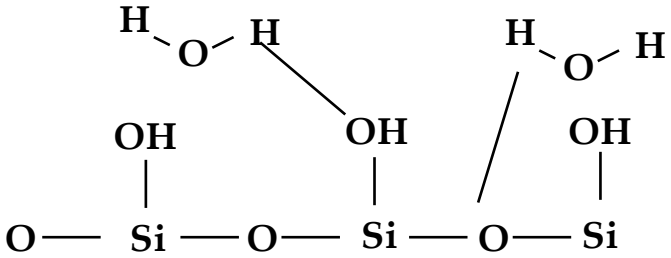
- Hexamethyldisilizane is used as an adhesion promoter between the resist and the wafer
- N_2 is bubbled through a reservoir of HMDS. HMDS vapour is carried to the wafer which sits on a hot plate
- Hot plate temperature of >200ºC are required
- Must be followed by a cool step prior to resist application

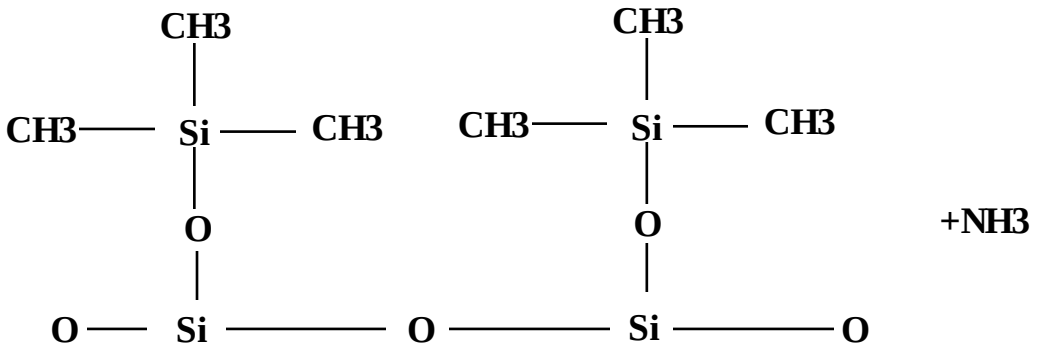
HMDS Prime



HMDS Chemical Configuration

Silicon Dioxide surface with OH groups attached (Water)





HMDS Displaces the OH and bonds to the silicon surface and in turn to the Photoresist

Photolithography

Tyndall National Institute
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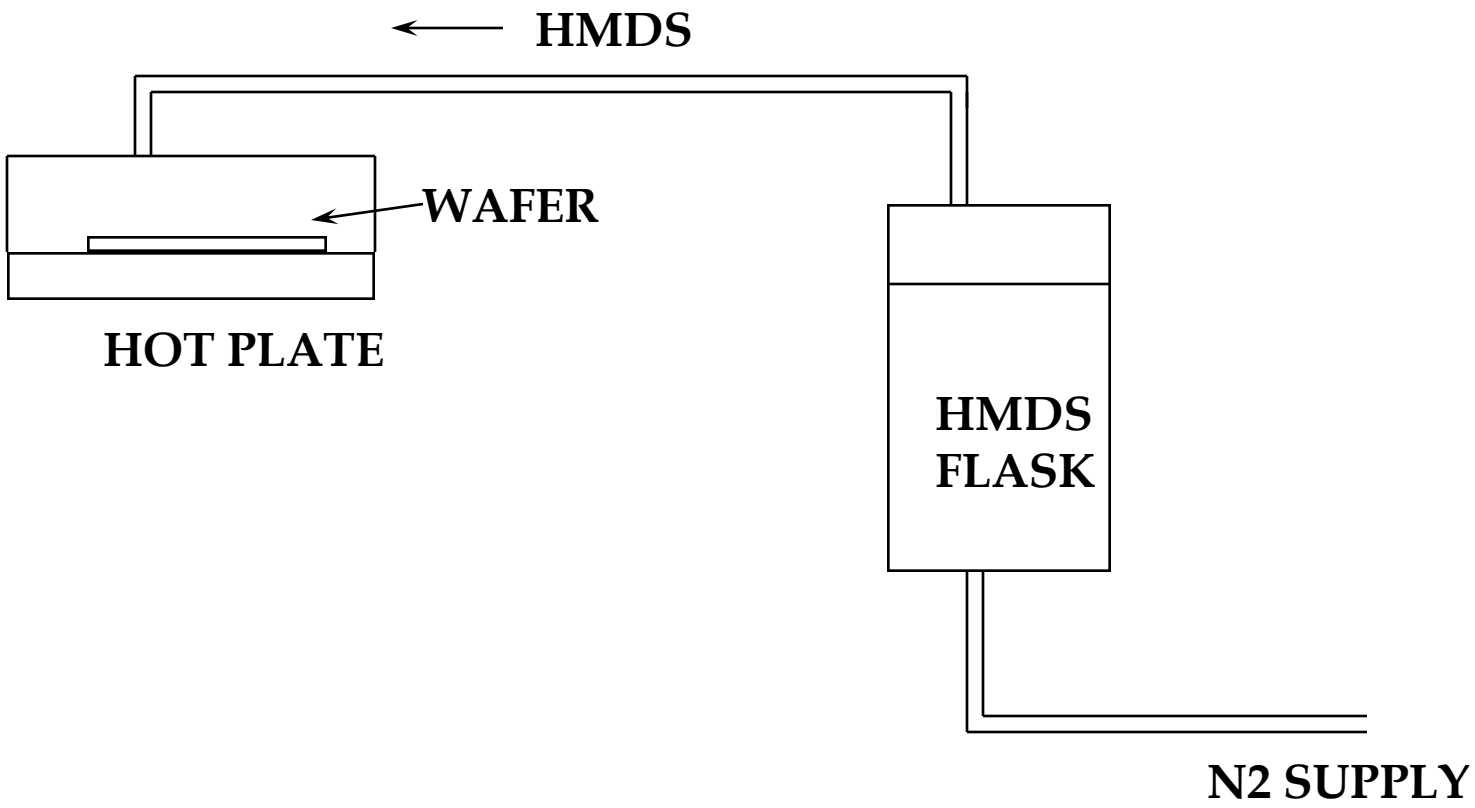
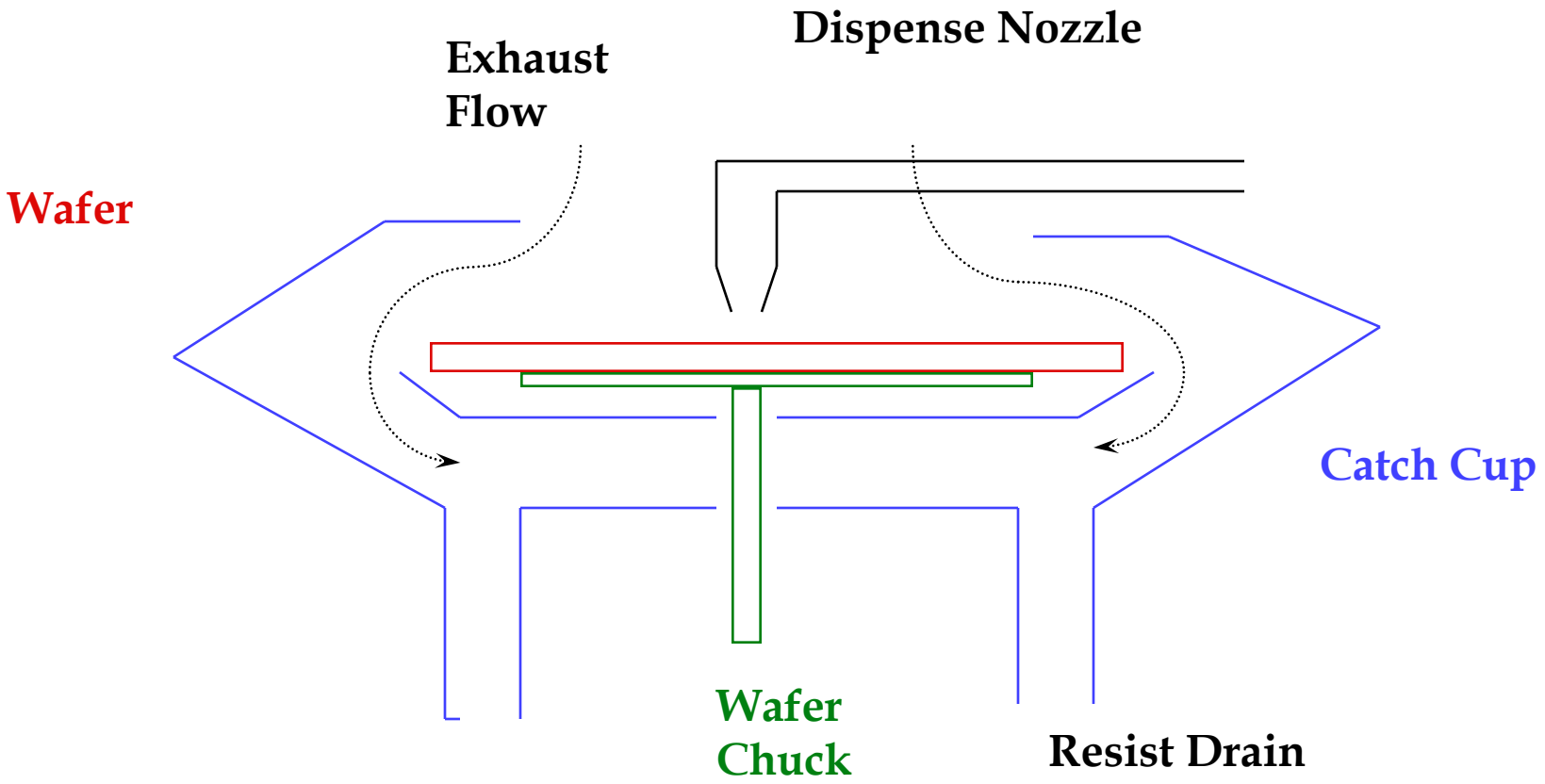
HMDS PRIME EQUIPMENT



3 RESIST APPLICATION



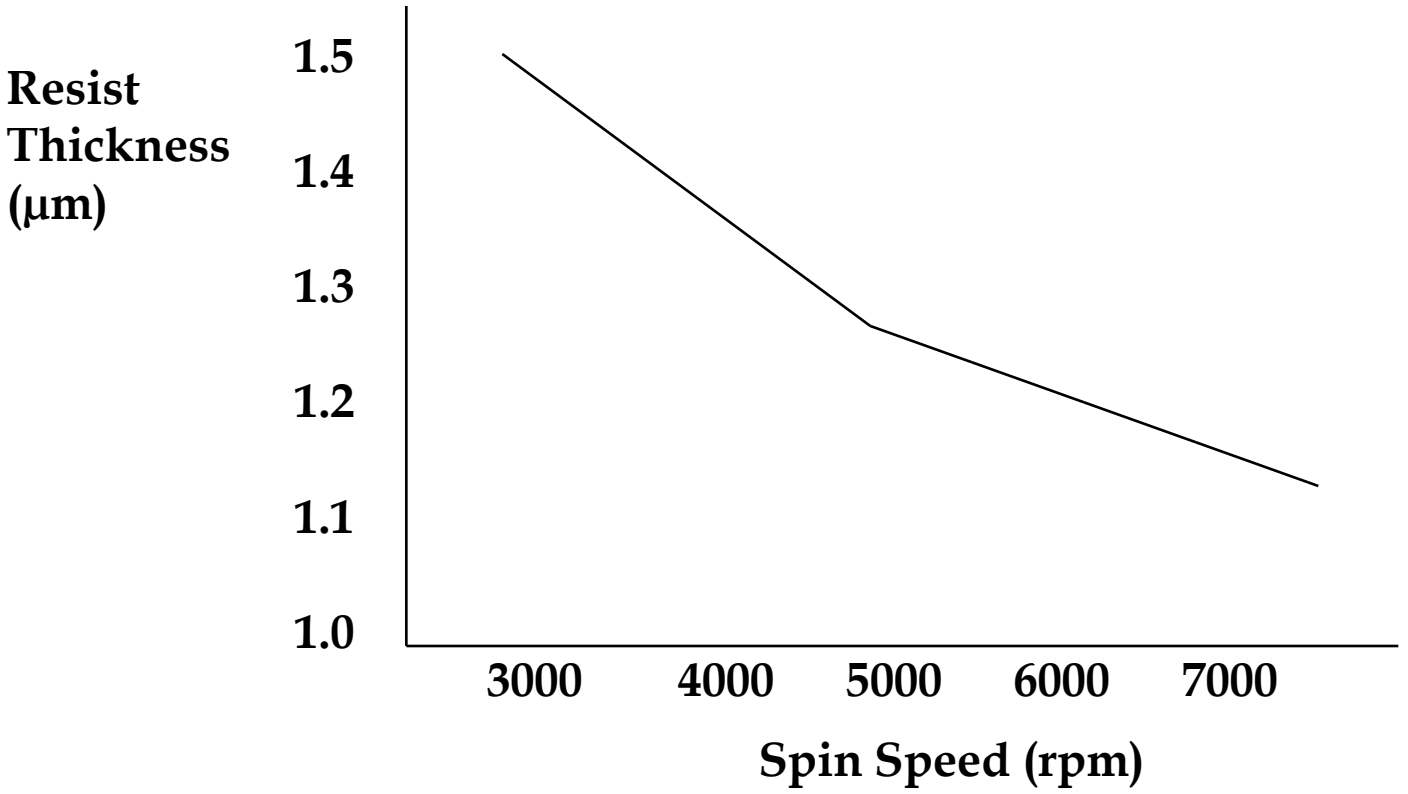
RESIST APPLICATION

- Photoresist is dispensed in liquid form
- The steps in a typical dispense program would be as follows
  1. Spin wafer at 1000rpm
  2. Dispense resist at center of wafer for two seconds
  3. Accelerate to 5000 rpm and spin at 5000rpm for thirty seconds

RESIST APPLICATION

- Typical resist thickness after spin is 1-1.2 microns
- Resist thickness is determined by final spin speed
- Uniformity of resist layer is usually better than 10nm across the wafer
- Environment around the wafer must be tightly controlled

RESIST THICKNESS

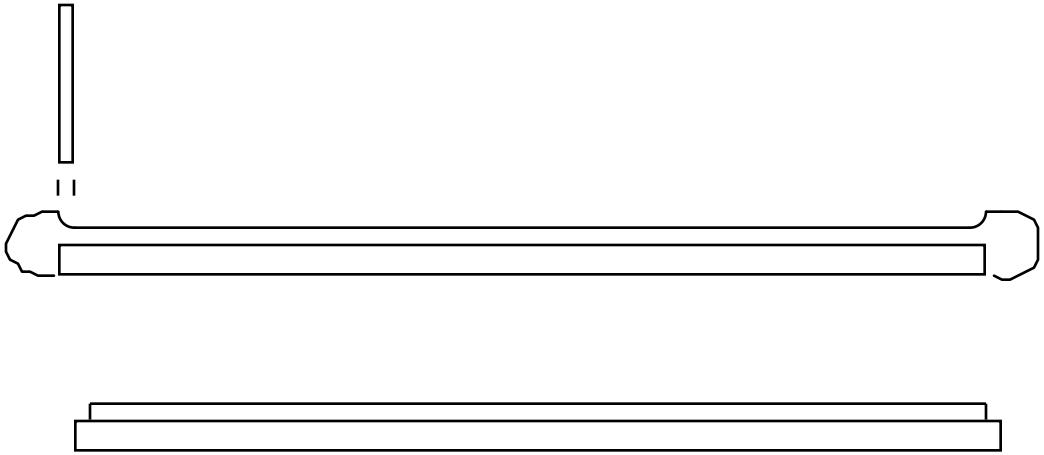


ENVIRONMENTAL CONSIDERATIONS

- **Environmental conditions must be maintained at a constant level**
  - **humidity**
  - **temperature**
  - **spin cup exhaust**
  - **room cleanliness**

EDGE BEAD REMOVAL (EBR)

- After resist spin solvent is applied to wafer edge to remove the edge bead
- Edge bead can cause particle generation in later processing steps



WAFER EDGE EXPOSURE

- Other possibility is a Fibre optic based system
- UV light used to expose areas of the wafer to be clamped in the following processing stage
- Resist in these areas is developed off during the normal develop process

4 SOFT BAKE

- Removes solvents from the resist prior to exposure
- Normally done on a hot plate at temperatures from 80ºC to 100ºC

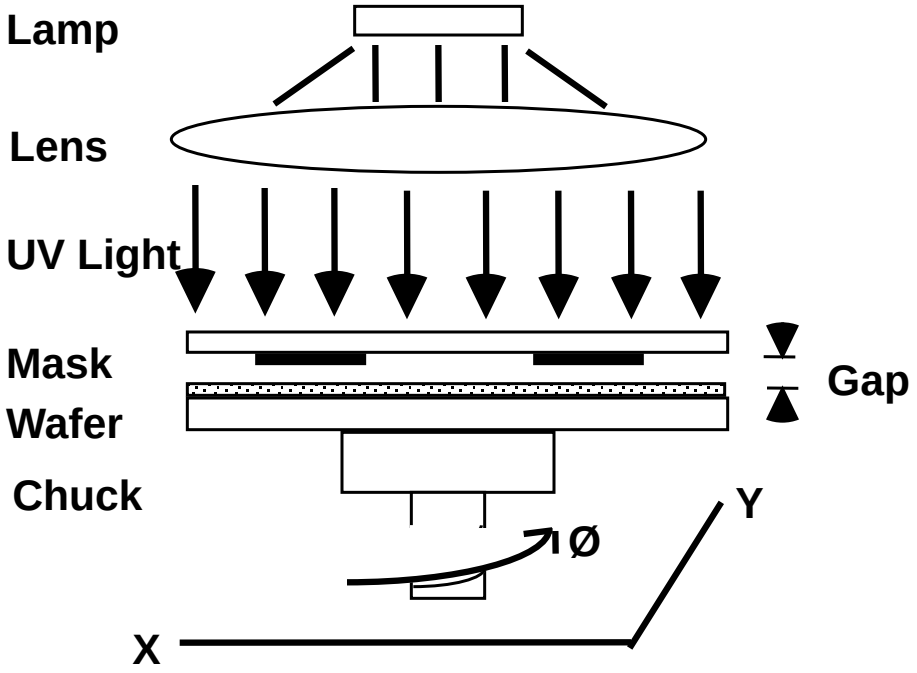
5 EXPOSURE

- Resist is exposed using a UV light source through a reticle or mask which contains the pattern to be exposed

- Exposure tools commonly used include
  - contact aligners
  - projection aligners
  - steppers

CONTACT/PROXIMITY ALIGNERS

Minimum Resolution
$\approx \sqrt{g\lambda}$



MASKS

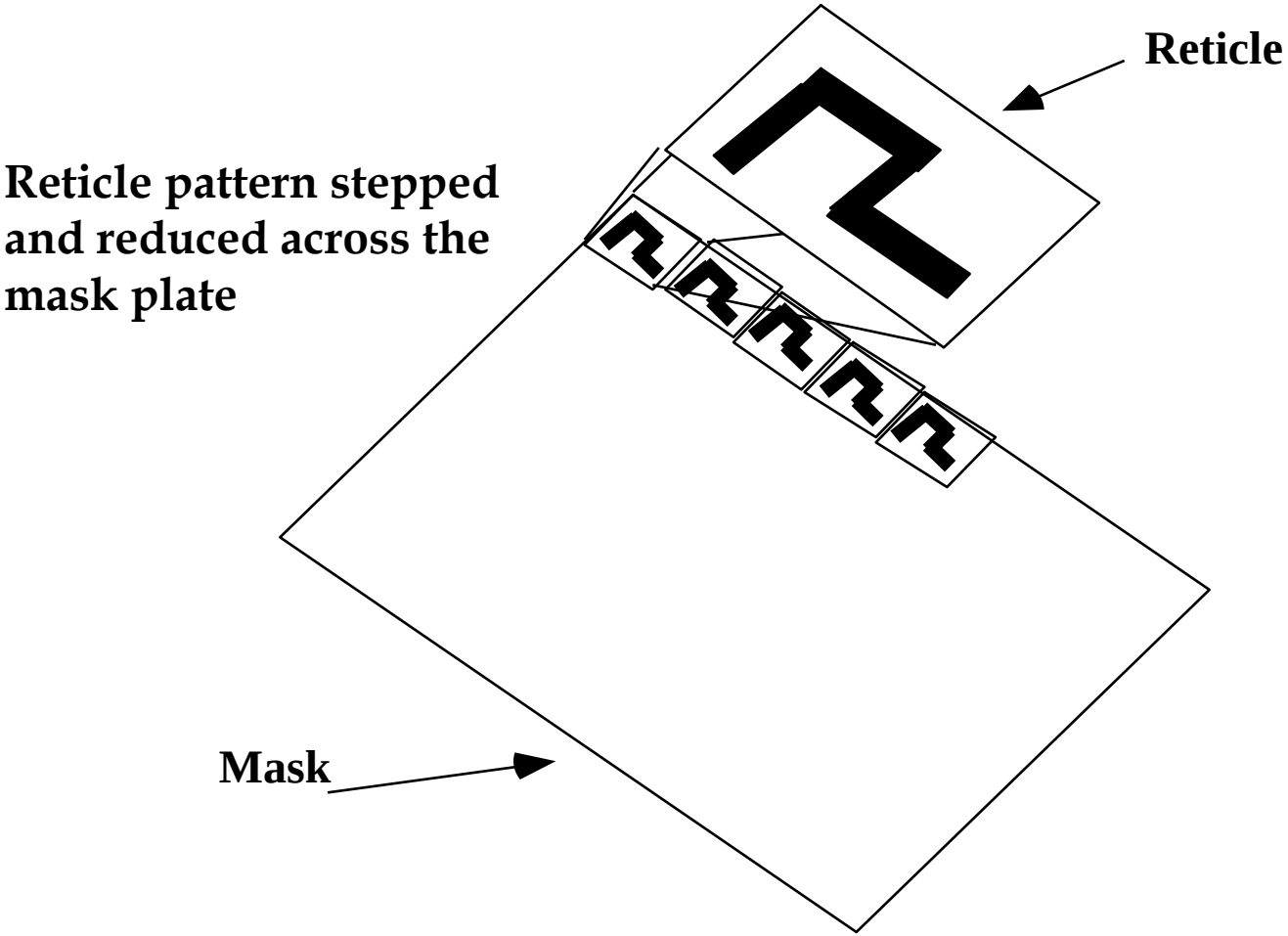
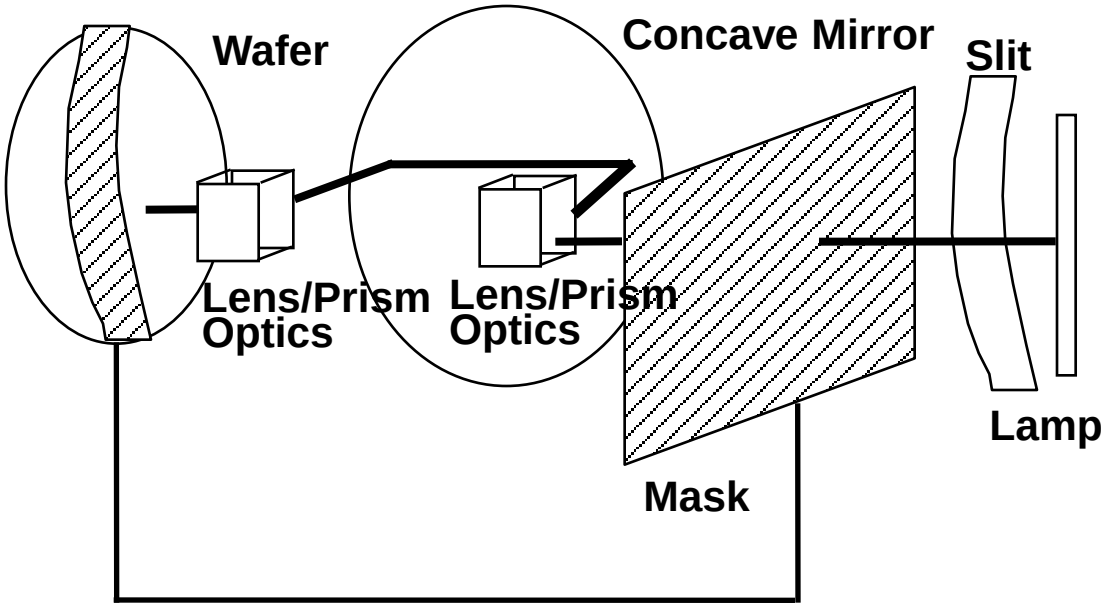


Fig 4 The mask making sequence.

MASKS

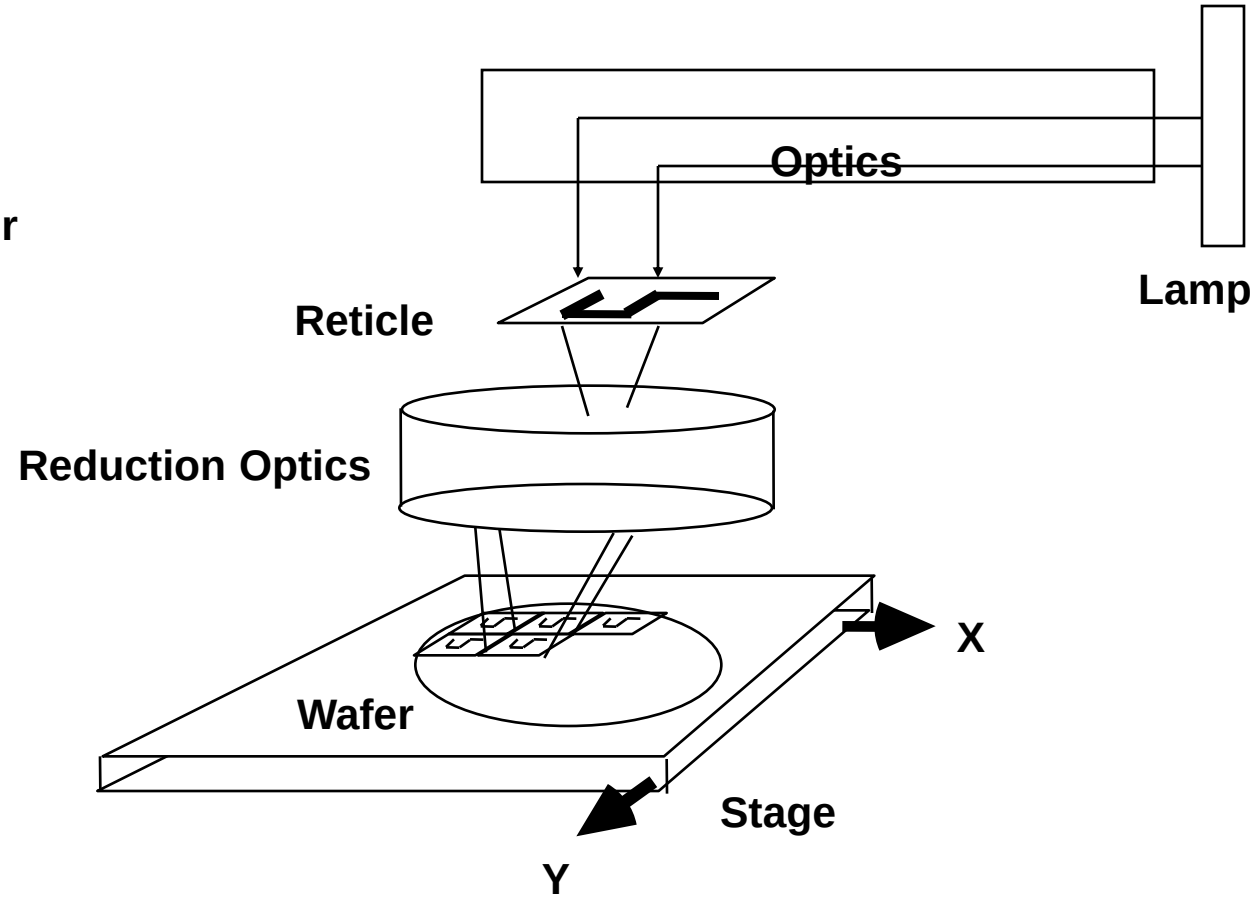
- Quartz or glass plate with pattern etched in chrome surface
- Pattern is repeated many times over mask
- Single exposure step used to expose the pattern over the entire wafer

PROJECTION ALIGNERS

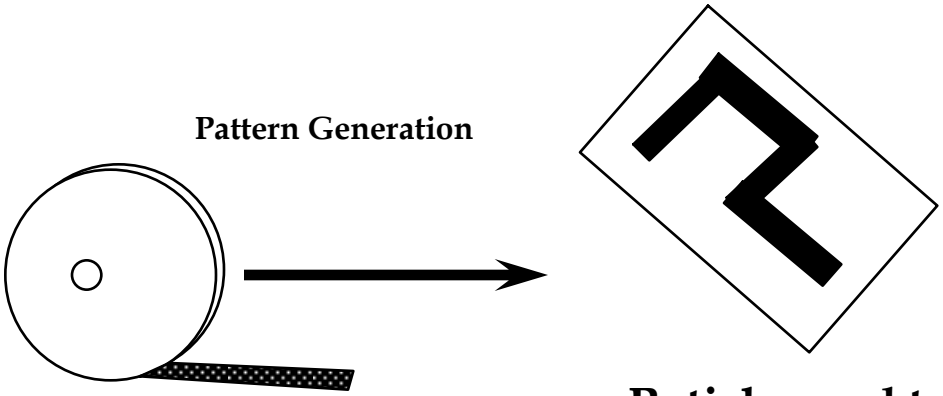


STEPPERS

5 or 10X Stepper Configuration



RETICLE



Reticle used to make masks or directly on the wafers on a DSW (stepper) system

RETICLES

- Used with stepper exposure systems
- Single pattern etched in chrome on reticle using e-beam direct write system
- Wafer moves underneath reticle and each field is exposed individually
- 5x reduction steppers - image on reticle is 5 times bigger than on wafer
- 1x steppers
  -image size on reticle is same as on wafer

RETICLES

- Reticles are pellicised
- Thin membrane positioned over chrome surface
- Particles deposited on membrane surface will be out of focus
- Particle image will not be printed on wafer

Exposure Parameters

- Exposure wavelength
- Resolution
- Depth of Focus
- Exposure Energy

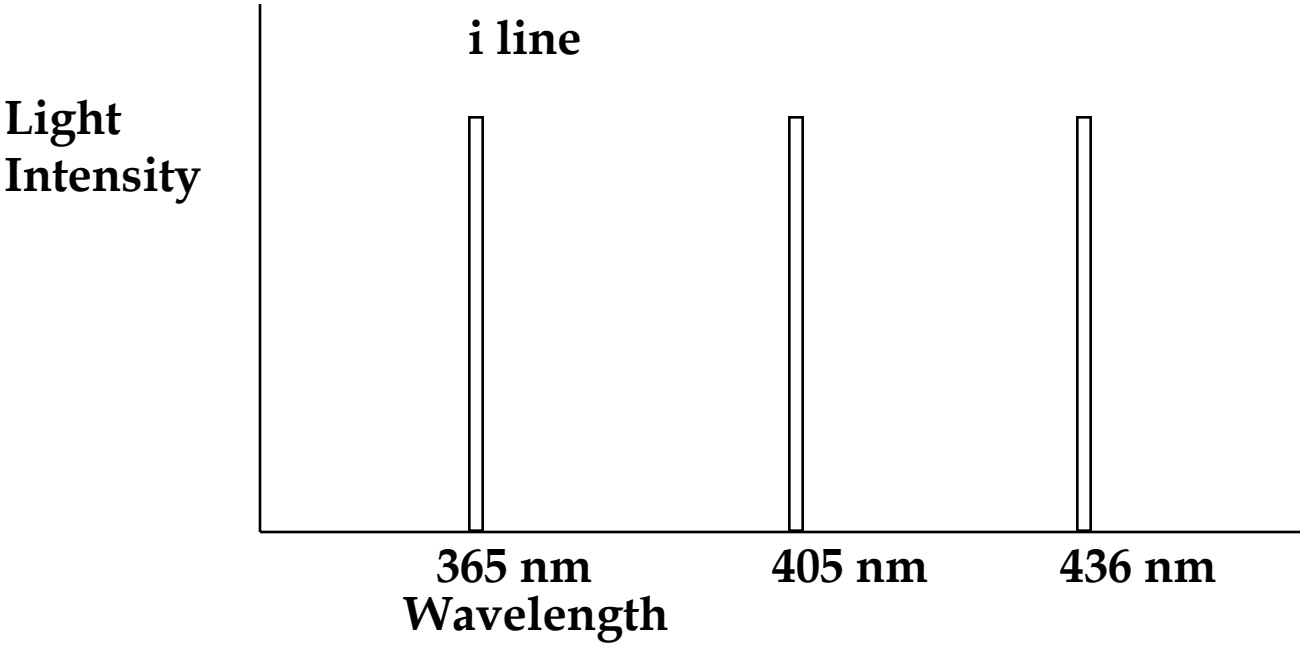
Exposure Wavelength

- Exposure tools can use either broadband or monochromatic UV light sources
- Shorter wavelengths used for smaller geometries
  - I-line exposure 365nm (0.35 µm)
  - G-line exposure 436nm (0.6 µm)
  - Broadband exposure (0.8 µm)

Deep Sub-Micron Exposure

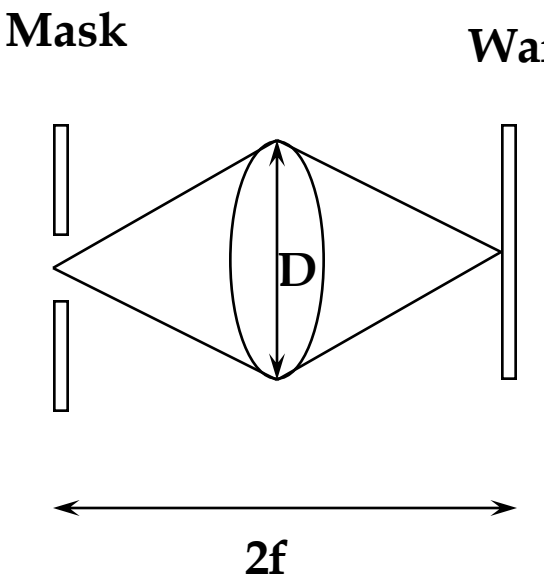
- Deep sub-micron processes use laser exposure systems - from the ITRS Roadmap
  - 180nm-130nm node uses KrF laser with λ=248nm
  - 130nm-100nm node uses/will use ArF laser with λ =193nm
  - 100nm-70nm node will use the F_2 laser (under development) with λ =157nm
  - For the 50nm node no laser available

MERCURY LAMP SPECTRUM



Resolution

- **Numerical aperture**
  -light gathering capability of a lens



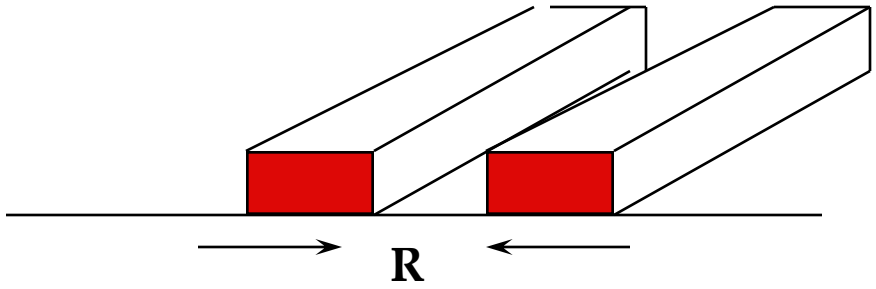
NA=D/2f

Resolution

- **Resolution (R)**
  - **Minimum resolvable linewidth that can be printed**

$$R \alpha (0.5)\, \lambda / NA$$

- **Shorter wavelengths give smaller resolution**



Electron Beam Lithography

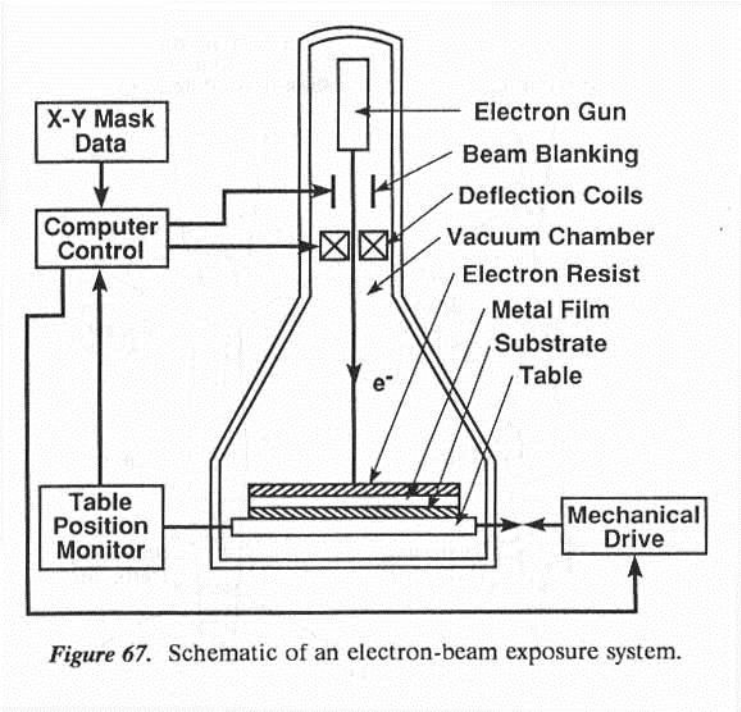
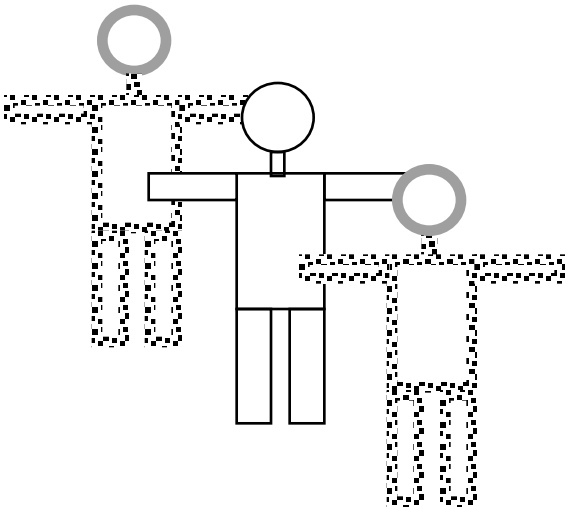


Figure 67. Schematic of an electron-beam exposure system.

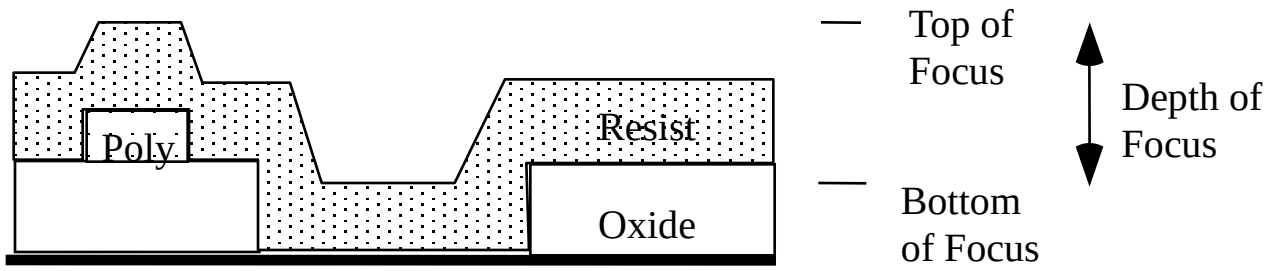
- Instead of using light a beam of electrons is used to directly write patterns into resist
- Effective wavelength $\lambda = h/mv$
  - where h= Planck's constant
  - m=mass and v=velocity
- At 10keV effective wavelength is 0.012nm
- Most modern E-Beam systems operate at energies of 50-100keV

Depth of Focus



In some photographs some objects are perfectly in focus or have a sharp image, objects either closer or further away than the focus point may be fuzzy.

Depth of Focus



Because of different step heights on wafers the optical system must have a wide depth of focus.

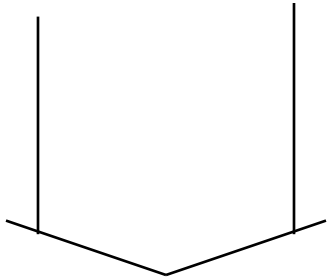
DEPTH OF FOCUS

- Depth of focus (DOF)

$$DOF \propto \lambda/2(NA)^2$$

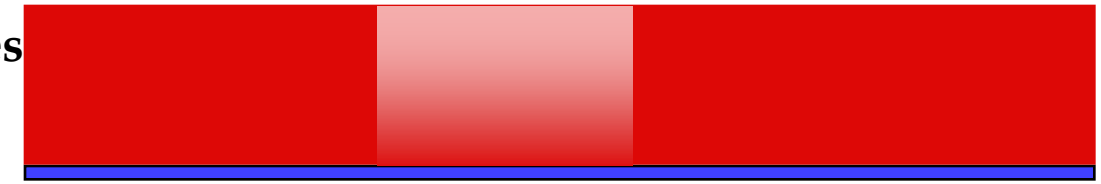
- Shorter wavelengths result in reduced DOF

Exposure Energy

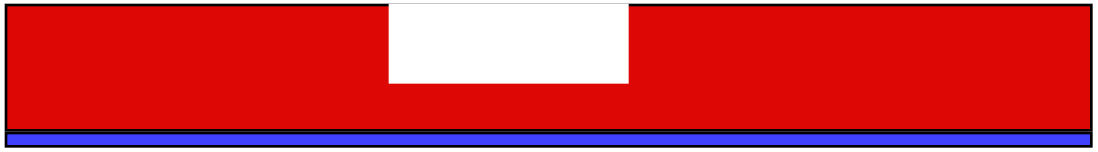


UV Light

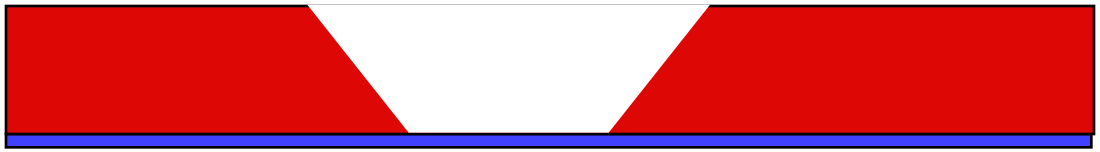
Resist bleaches as light is absorbed



Under exposed Results in Residual Resist

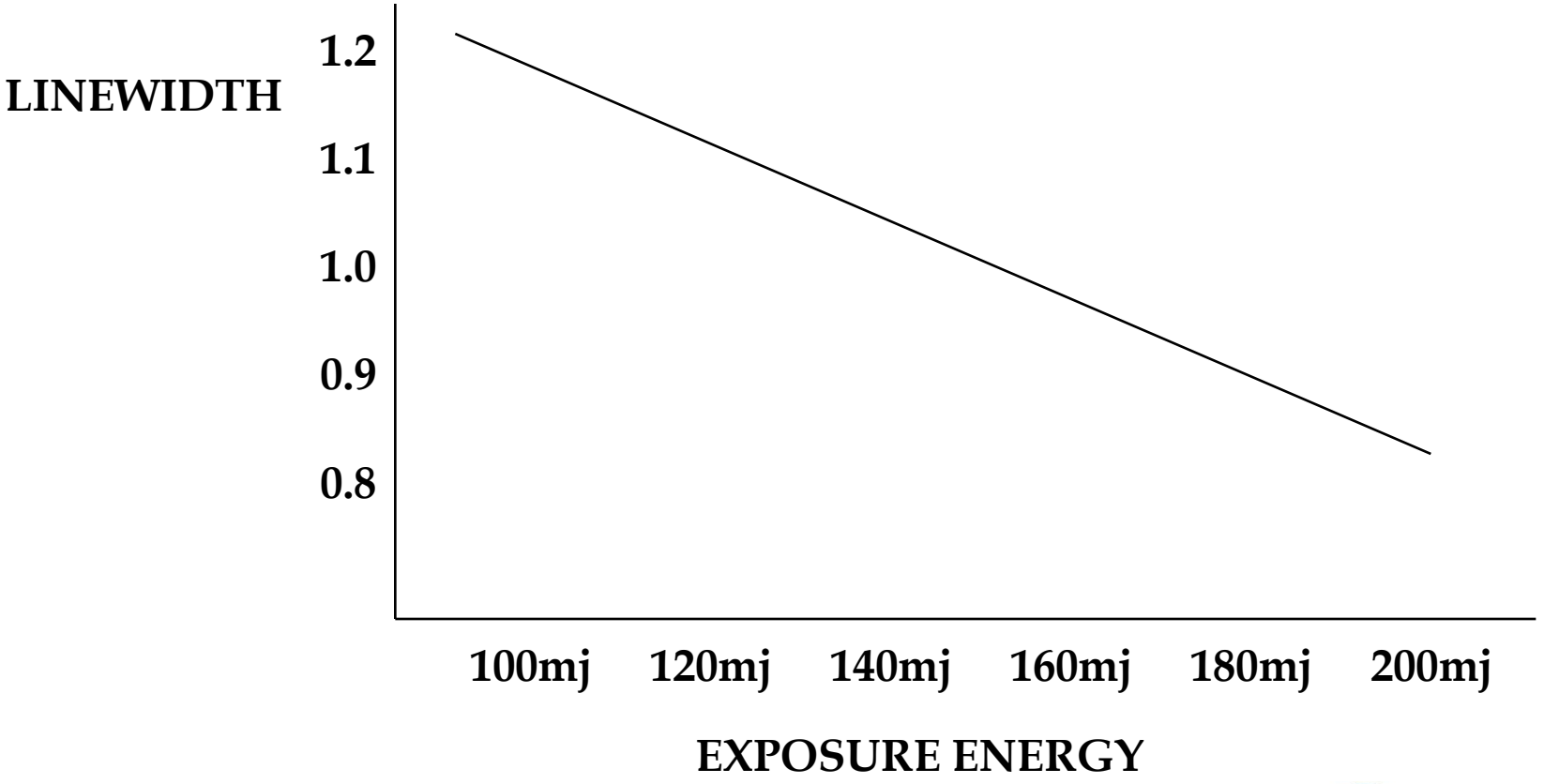


Over Exposed Poor profile CD error



Exposure Energy

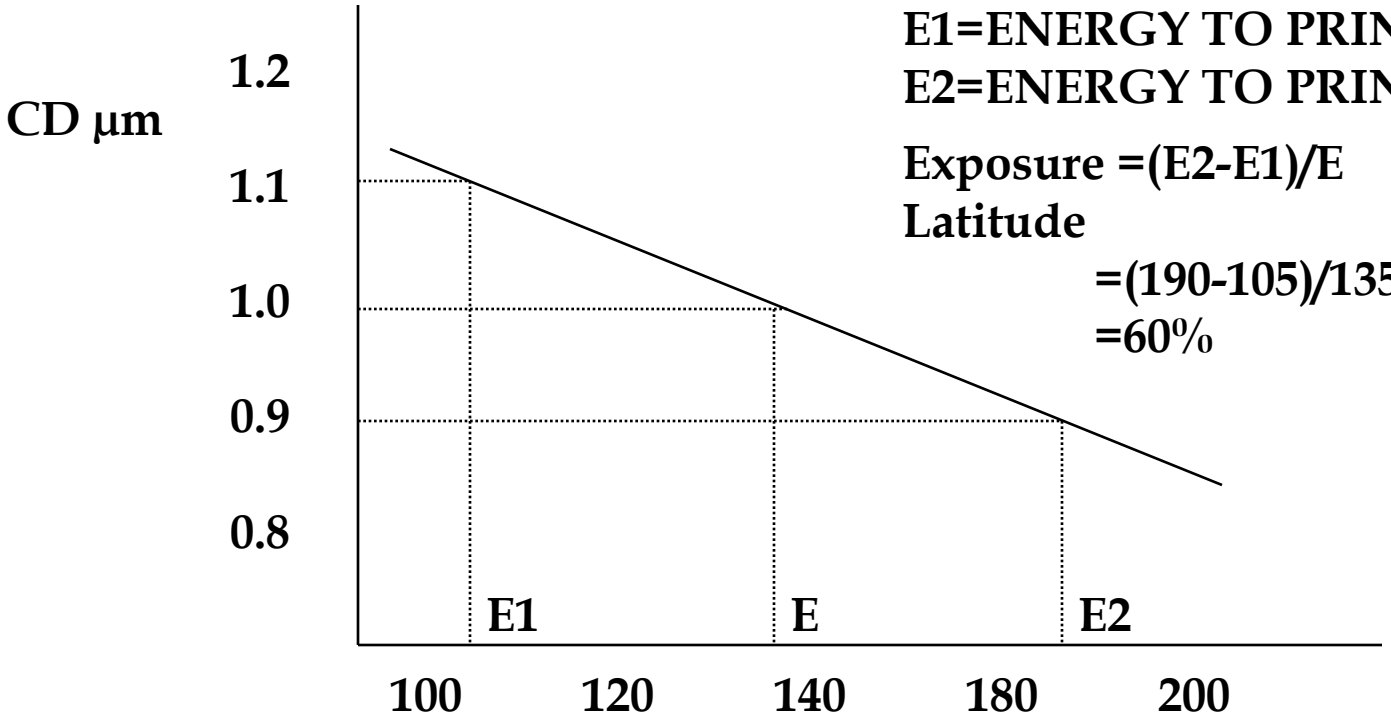
CD VARIATION DUE TO EXPOSURE ENERGY



EXPOSURE LATITUDE

All lines measured from 1.0µm line on the reticle
E=ENERGY TO PRINT 1.0µm
E1=ENERGY TO PRINT 1.1µm
E2=ENERGY TO PRINT 0.9µm

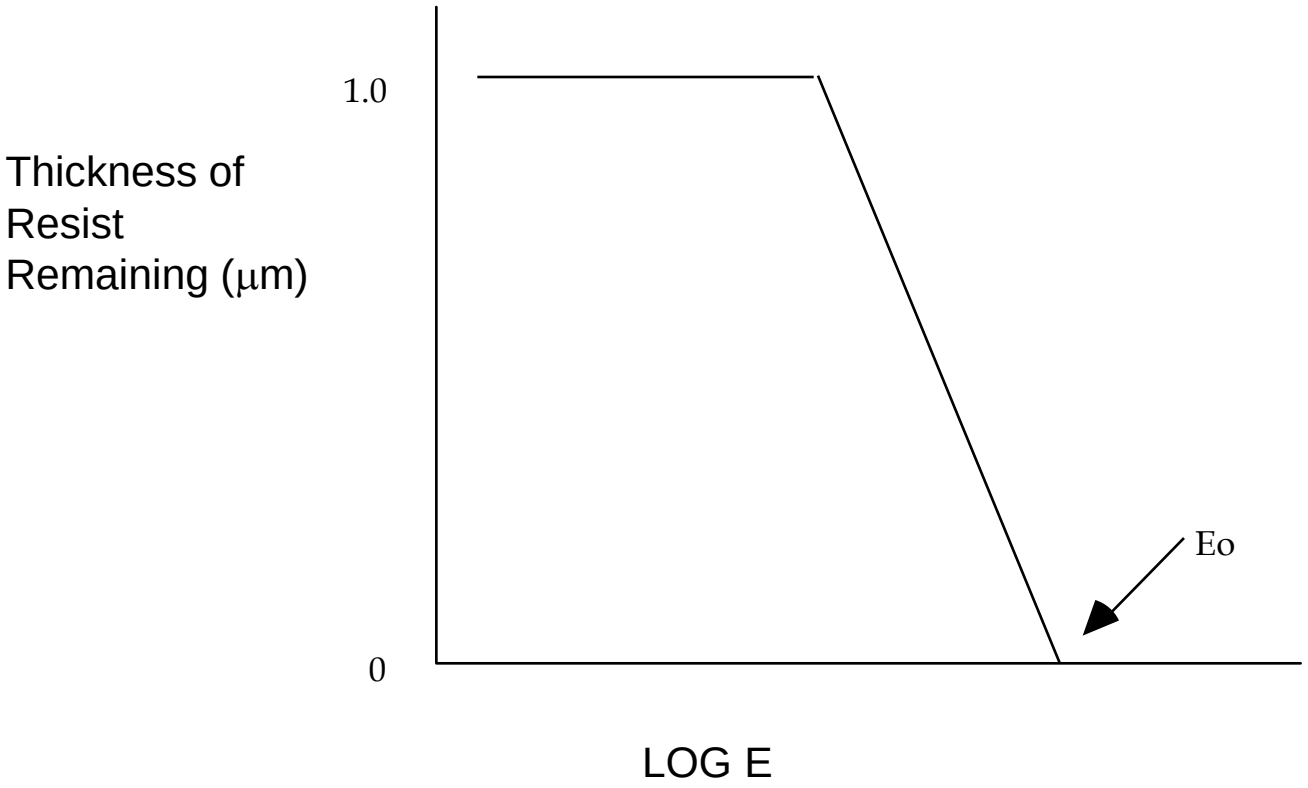
Exposure =(E2-E1)/E
Latitude
=(190-105)/135
=60%



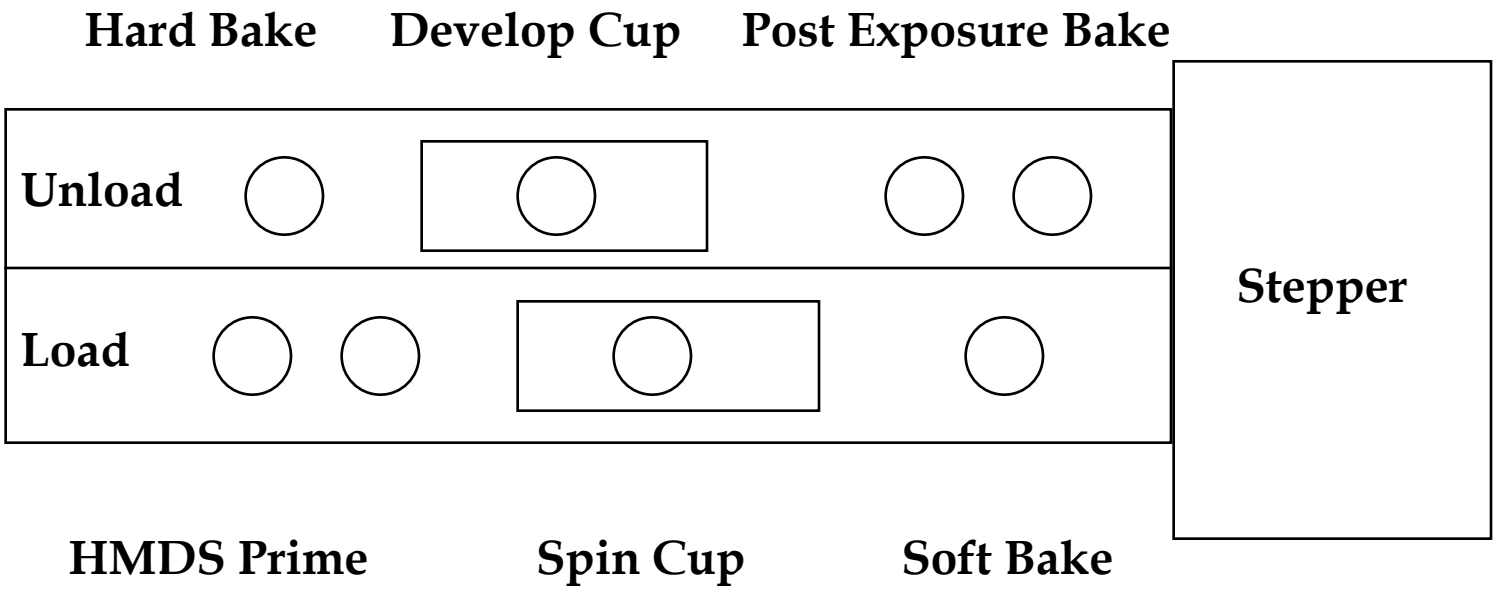
E0 PROCESS MONITOR

- E0 - energy required to clear resist
- Plot log exposure energy v normalized resist thickness
- E0 is the intersection of the line with the x axis

E0 Process Monitor



Equipment Layout



6 POST EXPOSURE BAKE

- Wafer is baked after the exposure step
- Typical process 120ºC for 60 seconds on a hot plate
- Followed by cool step prior to develop
- Used to reduce standing wave effects in exposed resist

Post Exposure Bake

EXPOSURE

No PEB

POST DEVELOP

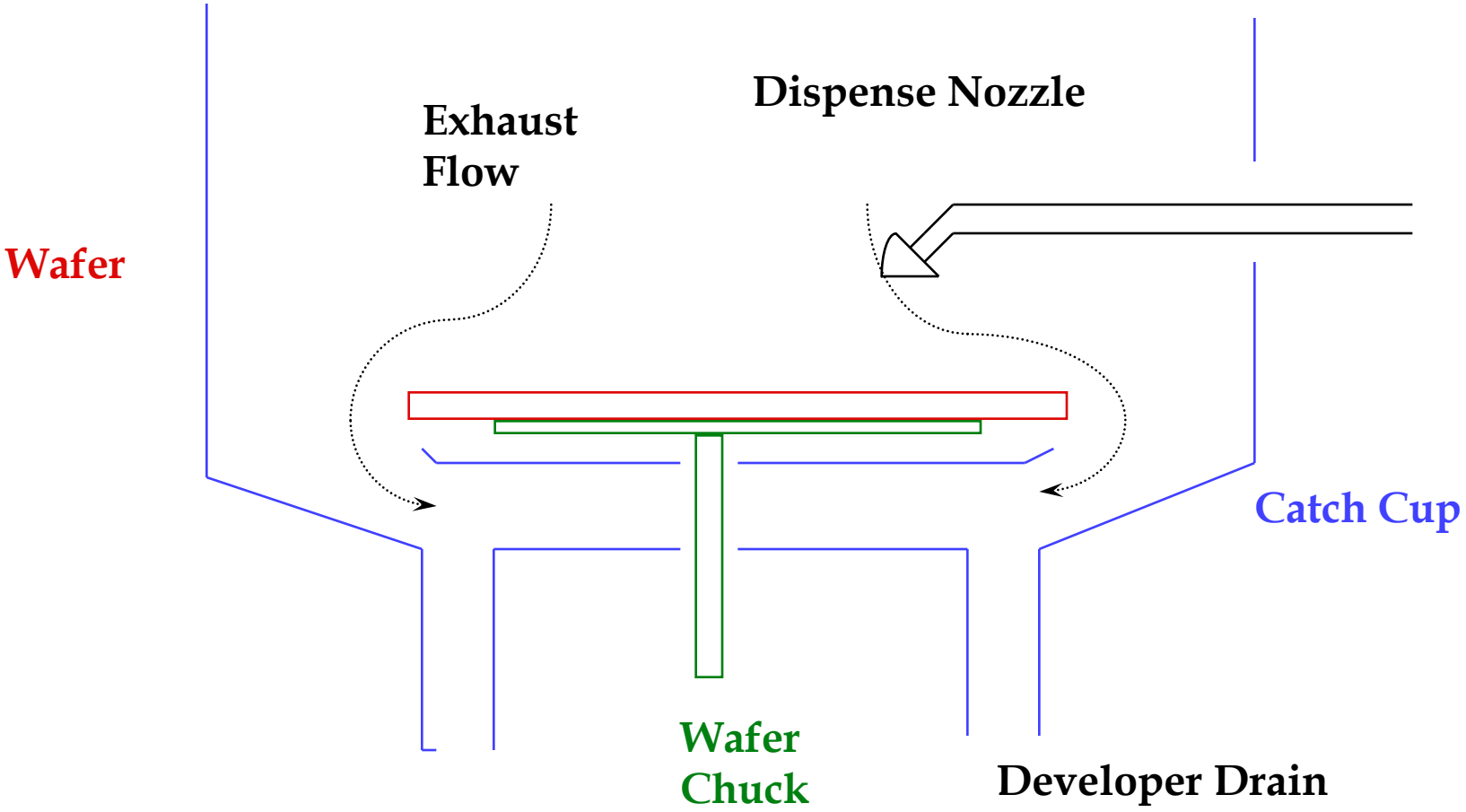
PEB

POST DEVELOP

7 DEVELOPER

- Alkaline based developer reacts with the exposed areas of resist
- Resulting solution is rinsed off with a DI water rinse
- Typical process
  - Spray developer on wafer surface for 5 seconds
  - Puddle develop for 60 seconds
  - DI water rinse for 10 seconds
  - Spin dry at 5000rpm for 15 seconds
- Temperature of developer must be controlled to ensure constant develop rate

7 Developer Application



8 HARD BAKE

- Wafer is baked on a hot plate after develop
- Typical process 120ºC for 60 seconds on a hot plate
- Improves resist adhesion
- Removes residual solvent from resist (important for high vacuum applications)
- Improves thermal stability of the resist

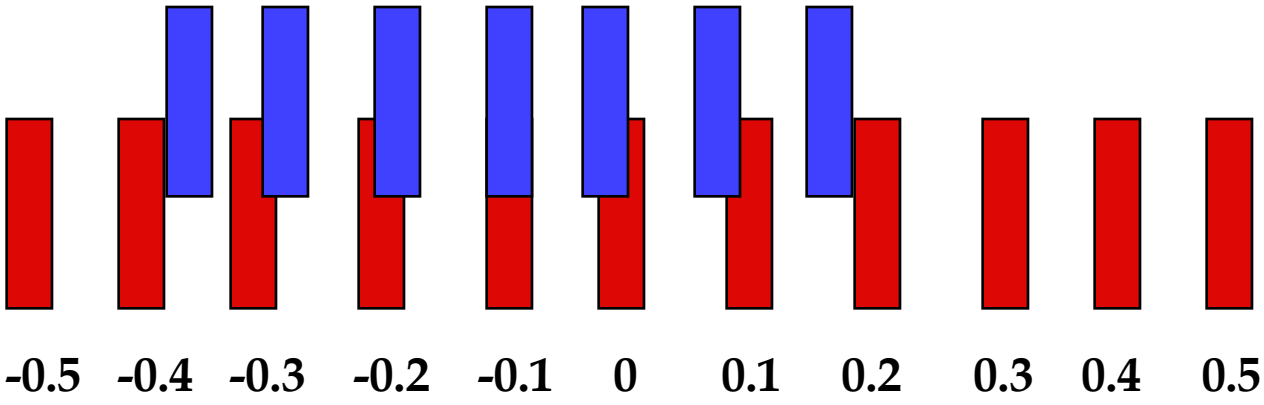
9 Inspection

- Resist Quality is inspected
  - Ragged edges etc
- Developed areas examined
  - Incomplete develop/resist residue in developed areas?
- Registration (or alignment accuracy) is measured
- Critical Dimension (or linewidth) control is measured
- Photolithography is one of the few processes in IC manufacturing that can be reworked

REGISTRATION

- Alignment between each layer must be better that 0.1µm for a small geometry process (<1µm)
- Alignment accuracy can be measured using dedicated measurement systems or using optical examination
- Use vernier scales with microscope

VERNIER SCALE



Future Developments

- Optical lithography has continued to at least the 32nm node (ITRS Roadmap)
  - In spite of initial fears that it would run out of resolution at geometries as large as 0.35µm (350nm)
- A number of resolution enhancement techniques will have to be adopted (RET)
  - Immersion Lithography
  - Wavelength reduction
  - Off-Axis Illumination (OAI)
  - Phase Shift Masks (PSM)
  - Optical Proximity Correction (OPC)

Critical Dimension

- Linewidth or CD (critical dimension) is width of line as measured on the wafer
- Resist CD is width of resist line printed on the wafer
- Polysilicon CD is width of poly rail as measured after etch and resist strip
- Important that measured CD is equal to dimension drawn on the reticle

CD MEASUREMENT

- Optical based systems used for large (>1.0μm) processes

- SEM based systems used for small geometry (<1.0μm) processes

Photolithography Summary

- Transfer of patterns from photomasks/reticles to wafer surface
- Largest single element of IC fabrication costs ----35%
- Most sensitive to particle contamination - yield loss
- Most sensitive to cleanroom conditions
- High degree of focus in ITRS roadmaps