Exam UE4002 Summer 2011

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an NMOS in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.
In each question, capacitances other than those shown may be ignored.

Question 1

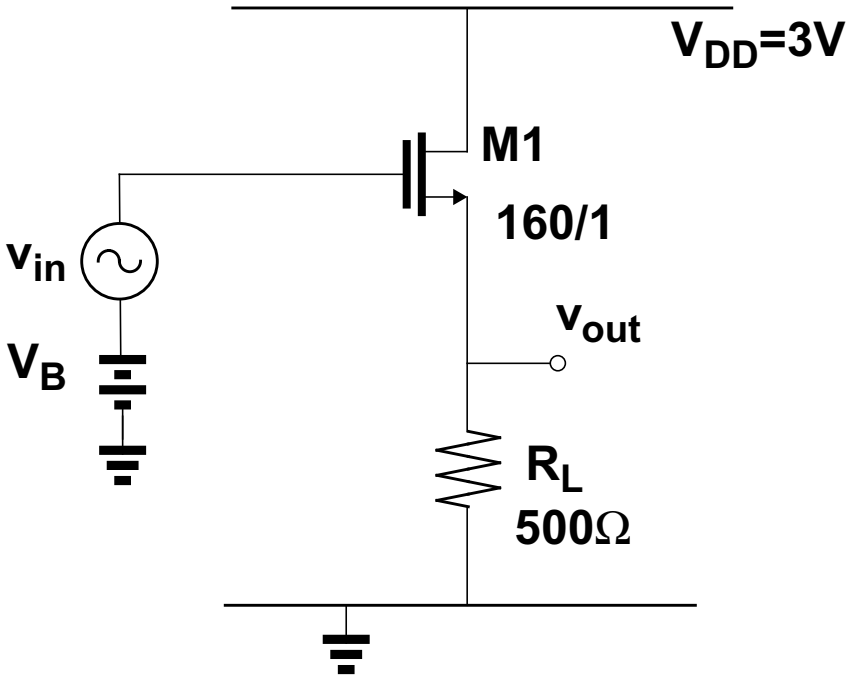

Figure 1

Figure 1 shows an NMOS source follower driving a resistive load. Assume M1 is in saturation. Resistor value and transistor dimensions in μm and are as shown in Figure 1. Take $K_n'=200\mu A/V^2$. Assume $g_{ds1}<<1/R_L$.

(i) Draw the small-signal equivalent circuit for the source follower stage shown in Figure 1.
(ii) Derive an expression for the small-signal voltage gain (v_{out}/v_{in}).
(iii) Calculate the small-signal voltage gain (v_{out}/v_{in}).
Take $I_{D1}=250\mu A$.
(iv) What is the minimum required value of I_{D1} so that the small-signal voltage loss between the input and output is less than 20%?

Question 2

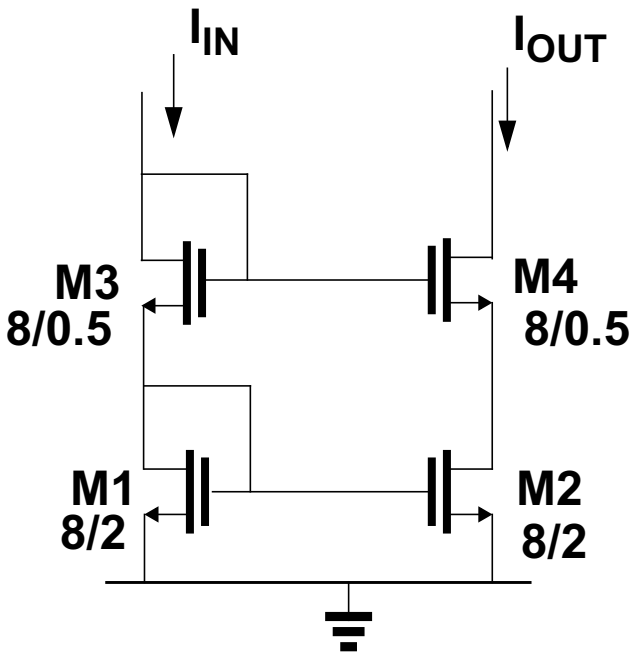

Figure 2

Figure 2 shows a cascoded current mirror.
Assume $I_{IN}=I_{OUT}=100\mu A$, $K_n'=200\mu A/V^2$, $V_{tn}=750mV$, $\lambda_n = 0.04V^{-1}/L$, L in μm.
Transistor dimensions in μm are shown in Figure 2.

(i) What is the minimum voltage at the output node, i.e. the drain of M4, such that all transistors are biased in saturation?
(ii) Derive an expression for the small-signal output resistance.
Assume g_{m1}, g_{m2}, g_{m3}, g_{m4} >> g_{ds1}, g_{ds2}, g_{ds3}, g_{ds4}.
(iii) What is the change in output current if the voltage at the output node varies by 10mV?
Assume all transistors are in saturation.
(iv) It is desired to increase the mirroring ratio by increasing the width of M2 only. What is the largest value of output current such that M2 remains in saturation?

.

Question 3

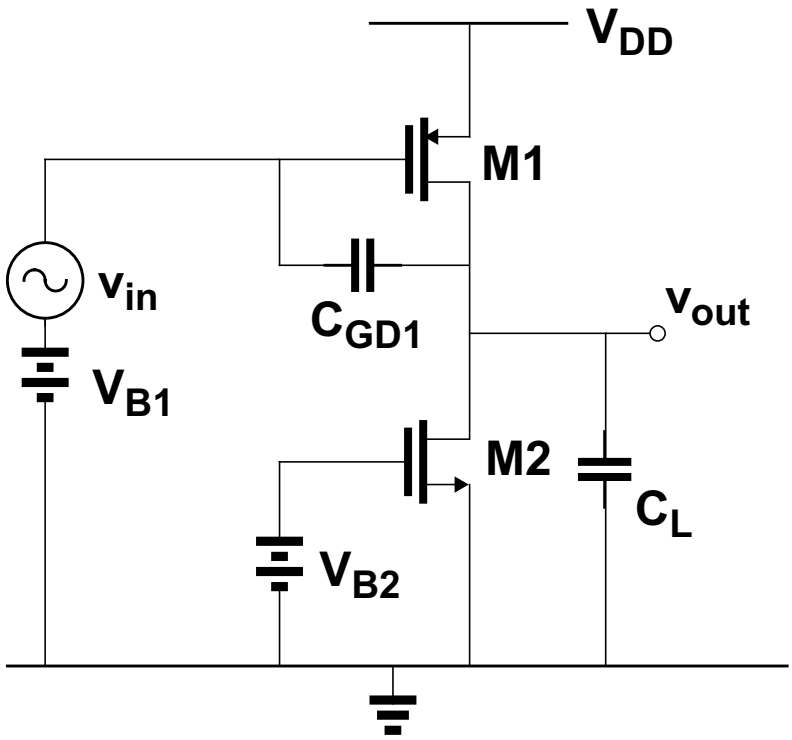

Figure 3

For the questions below you may assume $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$ and that all devices are biased in saturation.

(i) Figure 3 shows a gain stage with an active load. Draw the small-signal model for this circuit.
(ii) Derive an expression for the high-frequency transfer function of the circuit.
(iii) Calculate the low-frequency gain (v_{out}/v_{in}) and the break frequencies (i.e. pole and/or zero frequencies) if
V_{DD}= 3V, V_{B1}= 2V, $|V_{tp}|$ = 0.75V, $|I_{D1}|$ = 200μA, $\lambda_p = \lambda_n$ = 0.04V^{-1}, C_{GD1}= 0.1pF, C_L= 1.5pF.
(iv) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the pole and/or zero frequencies.

Question 4

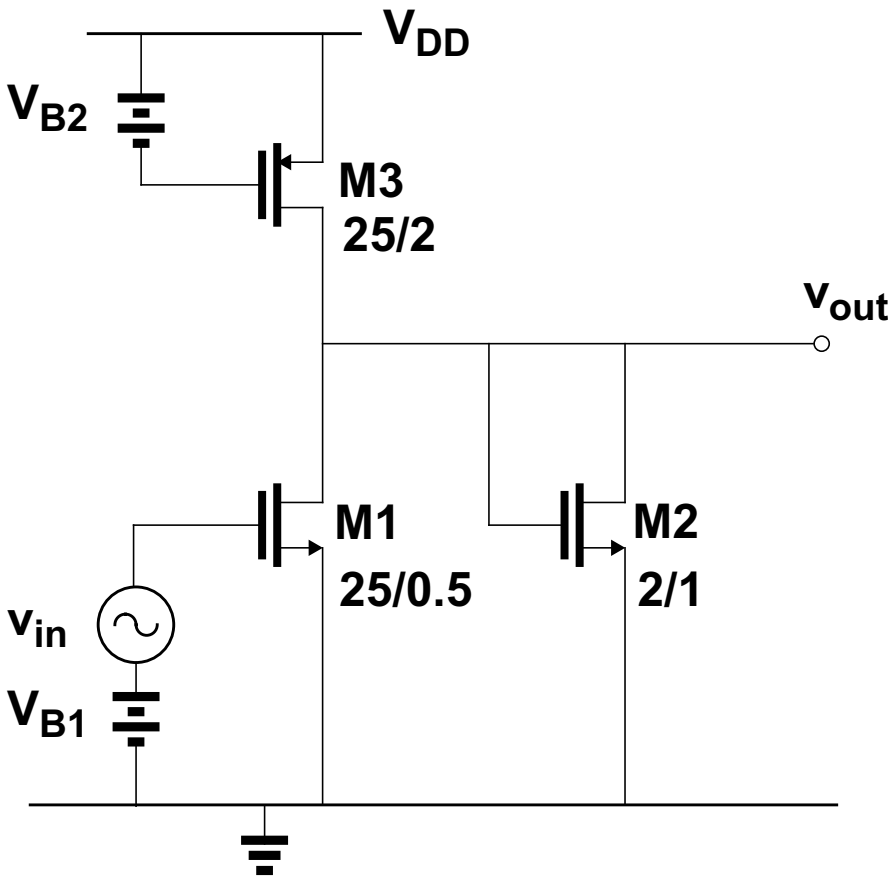

Figure 4

For the questions below you may assume g_{m1}, g_{m2}, g_{m3} >> g_{ds1}, g_{ds2}, g_{ds3}, and that all transistors are biased in saturation.
Transistor dimensions μm are as shown in Figure 4.
Only thermal noise sources need be considered.
For calculations take Boltzmann's constant $k=1.38X10^{-23}J/^oK$, temperature $T=300^oK$.

(i) Draw the small-signal model for the circuit shown in Figure 4.
What is the small-signal voltage gain (v_{out}/v_{in}) in terms of the transistor small-signal parameters?
(ii) What is the input-referred thermal noise voltage density of the circuit shown in Figure 4?
The answer should be in terms of the transistor small-signal parameters, Boltzmann's constant k and temperature T.
(iii) Calculate the input-referred thermal noise voltage density of the circuit if $K_n'=200\mu A/V^2$, $K_p'=50\mu A/V^2$, $I_{D1}=50\mu A$, $|I_{D3}|=100\mu A$.
(iv) If the output signal is 100mVrms, what is the signal-to-noise ratio at the output if the noise is measured over a bandwidth of 10MHz?