Part A

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an nmos in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For d.c. biasing calculations you may take $\lambda=0$

Question 1

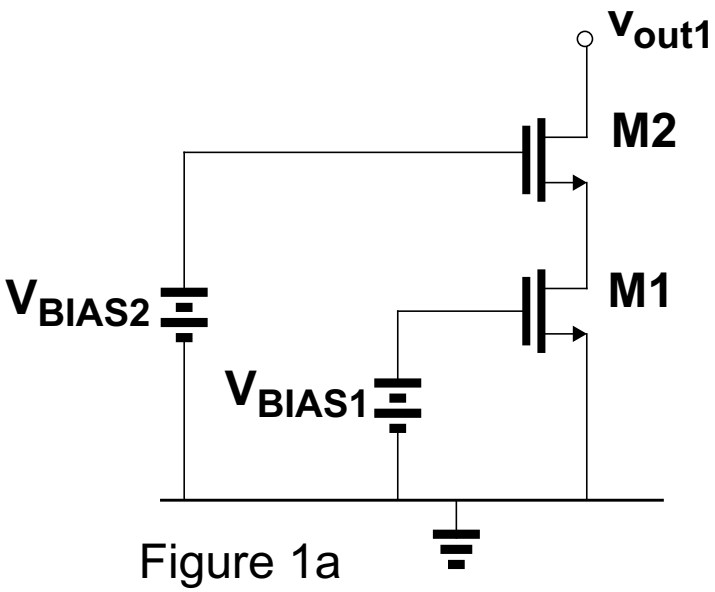

Figure 1a

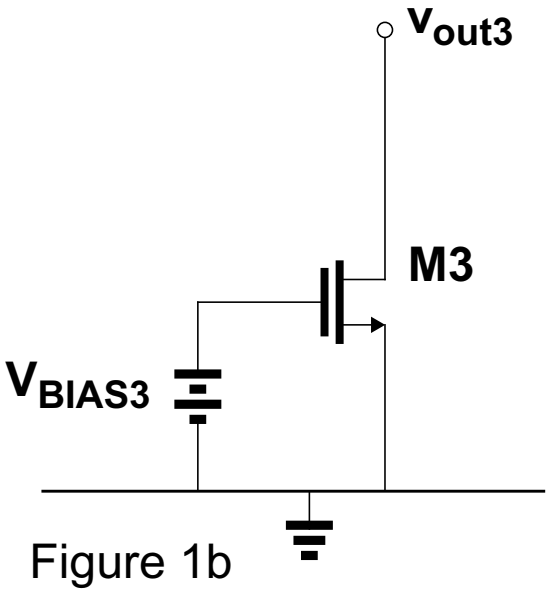

Figure 1b

(i) Draw the small-signal model of the cascode stage shown in Figure 1a.
(ii) Derive an expression for the output resistance r_{out1} of the cascode stage i.e. the resistance looking into the output node v_{out1} and show that this can be simplified to

$$r_{out1} = \frac{g_{m2}}{g_{ds2}} \cdot \frac{1}{g_{ds1}}$$

assuming $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$

(iii) $W_1=W_2=8\mu m$, $L_1=L_2=1\mu m$, $K_n'=200\mu A/V^2$, $V_{tn}=0.75V$ and V_{BIAS1} is set so that $I_{D1}=200\mu A$ in saturation.
What is the minimum value of voltage at the drain of M1 such that M1 is in saturation?
What is the value of V_{BIAS2} required to achieve this biasing condition?
What is the headroom (i.e. the minimum voltage at the output such that all devices are in saturation) required by the cascode stage?
(iv) Figure 1b shows a simple transistor stage. If this stage is implemented in the same technology with the same bias current, transistor width and voltage headroom as the cascode stage, what is the maximum value of L3 such that M3 is in saturation?
(v) Calculate the approximate output resistances of the configurations shown in Figure 1a and 1b for the bias conditions and dimensions used in (iii) and (iv).
Take $\lambda_n=0.04/L\ V^{-1}$ (L in μm) for this calculation.

Question 2

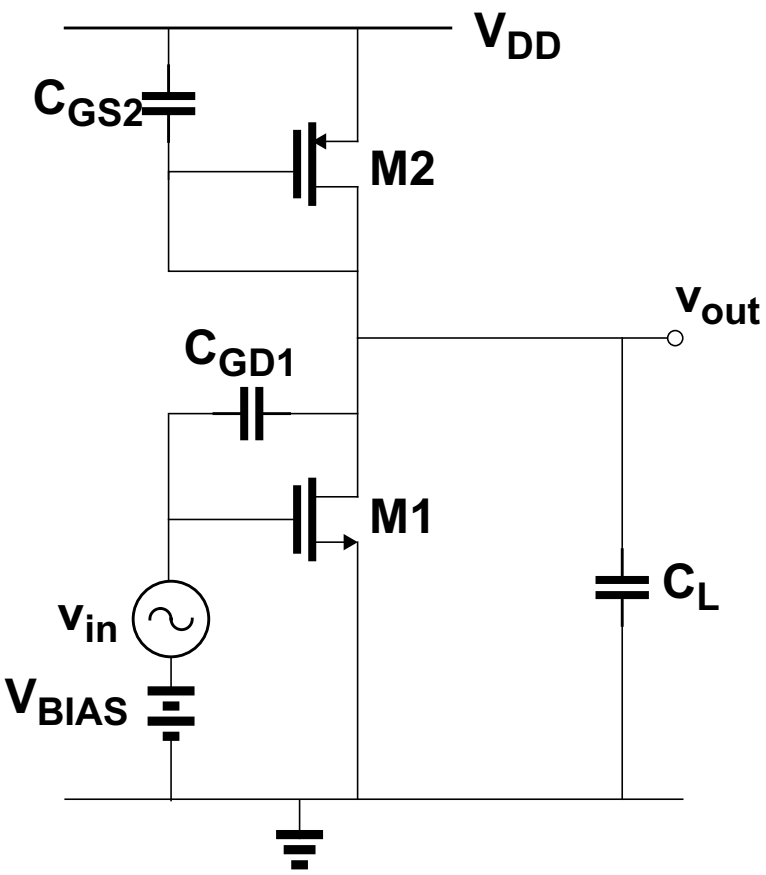

Figure 2

For the questions below you may assume g_{m1},g_{m2}>>g_{ds1},g_{ds2} and that all devices are biased in saturation.

(i) Figure 2 shows a gain stage with a diode-connected load. Draw the small-signal model for this circuit.
(ii) Derive an expression for the low-frequency small signal voltage gain (v_{out}/v_{in}).
(iii) Ignoring all capacitances except C_{GD1}, C_{GS2} and C_L derive an expression for the high-frequency transfer function.
(iv) Calculate the low-frequency gain (v_{out}/v_{in}) and the pole and zero frequencies if V_{GS1}=1V,V_{GS2}=1.75V, V_{tn}=|V_{tp}|=0.75V, I_{D1}=250μA, C_{GD1}=0.1pF, C_{GS2}=1pF, C_L=1.5pF.
(v) Draw a Bode diagram of the gain response. Indicate the values of gain at d.c. and at frequencies well above the pole and zero frequencies.

Question 3

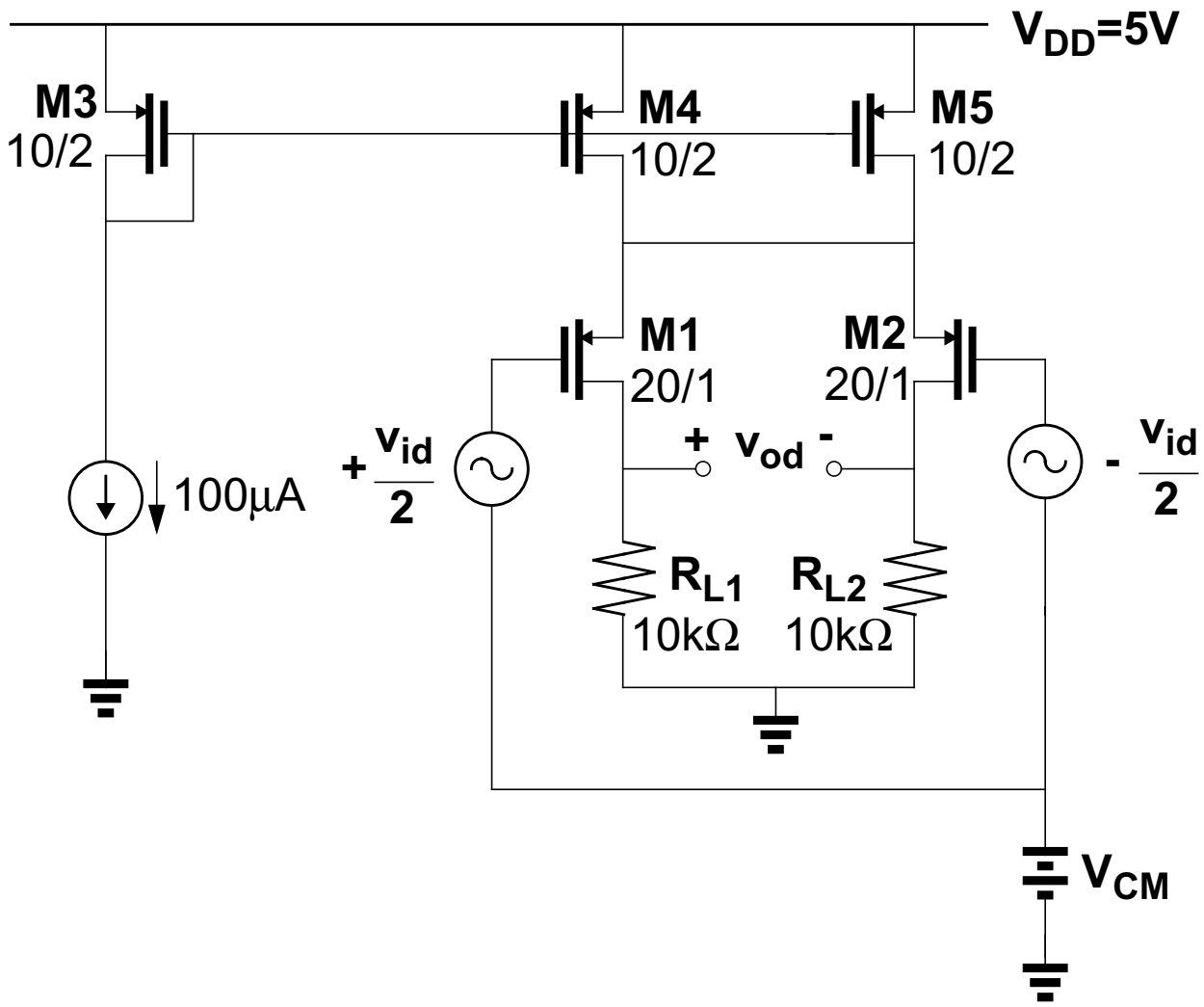

Figure 3

Figure 3 shows a pmos differential pair biased by a common-mode voltage V_{CM}.

For the calculations below use K_p'=50µA/V^2, $|V_{tp}|$=0.8V.

(i) What is the maximum value of V_{CM} such that all devices are still biased in saturation?
(ii) What is the minimum value of V_{CM} such that all devices are still biased in saturation?
(iii) A differential small-signal v_{id} is applied at the inputs. Give an expression for the low-frequency small signal voltage gain (v_{od}/v_{id}).
(iv) Calculate the low-frequency small-signal voltage gain. Assume all devices are biased in saturation and $1/g_{ds1}$,$1/g_{ds2}$>>R_{L1},R_{L2}.
(v) A small signal sine wave with a differential peak-peak voltage of 40mV is applied to the inputs. The common-mode voltage V_{CM}=V_{DD}/2. What is the maximum value of gain that can be achieved by increasing the load resistance (R_{L1} and R_{L2})?