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THE NATIONAL UNIVERSITY OF IRELAND CORK

COLAISTE NA h -OLLSCOIL, CORAIGH
UNIVERSITY COLLEGE CORK

Summer 2013

B.E. ENGINEERING (ELECTRICAL & ELECTRONIC)

Digital Integrated Circuit Design UE4001

Dr. Luke Seed
Prof. Nabeel Riza
Dr. Emanuel M. Popovici

Answer Question 1 and 2 of the remaining 3 questions

3 HOURS

Approved Calculator Allowed

Questions follow overleaf

Question 1) **(40 marks)**

a) Describe System Level Design and Architecture Design concepts by listing some types of decisions taken for each. Present a generic FPGA architecture, naming its constituent blocks. When do dedicated architectures make sense? [8 marks]

b) Define decomposition, pipelining, replication and time sharing in the context of architectural design. Present the performance implications of each (area and delay). [8 marks]

c) Present an SRAM and DRAM cell architecture and describe the functionality for each. [8 marks]

d) Briefly describe the 4 constituents of the energy dissipation in a switching CMOS inverter [8 marks]

e) In the context of clock distribution, discuss the architecture and the issues related to collective clock buffers versus distributed clock buffers. [8 marks]

Question 2) **(30 Marks)**

Consider two flip-flops with combinational logic in between them.

a) Present and discuss the schematic of a single edge-triggered D-type flip-flop. [6 marks]

b) Derive the setup condition. What is the worst time condition on the clock period which, when satisfied will guarantee the setup times are obeyed? [8 marks]

c) Derive the hold condition. What are the implications on the hold condition in the absence of the combinational logic (no contamination delay)? [8 marks]

d) Implement and discuss a clock gating strategy for the system. Assuming that the gate equivalent of the combinational logic is GE(C), what is the gate equivalent of the system? [8 marks]

Question 3) **(30 Marks)**

In the context of power optimisation, discuss:

a) dynamic dissipation reduction techniques at architecture and RTL levels. [6 marks]

b) leakage reduction techniques using dynamic back biasing and multi-threshold logic. [9 marks]

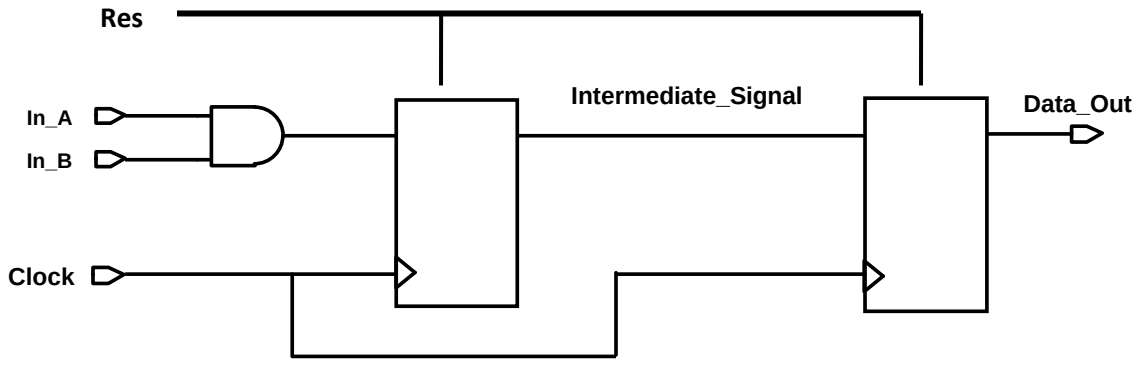
c) Describe the Dynamic Voltage and Frequency Scaling (DVFS) technique as well as the open loop and closed loop approaches. [9 marks]

d) Use an inverter to describe adiabatic switching. [6 marks]

Question 4) **(30 Marks)**

a) Describe a 3 input majority voting circuit using Gate, Dataflow and Behavioural level Verilog. [6 marks]

b) Describe in Verilog the architecture for a circuit represented in the figure below. The D-type flip-flops are initialised by an active high asynchronous reset (Res). [6 marks]



c) Describe in Verilog a 16 bit up-down counter with synchronous reset given by:

```
module counter    (
                    c_out,    // Output of the counter
                    c_data,  // parallel load for the counter
                    c_load,   // parallel load enable
                    c_enable, // counter enable signal
                    up_down,  // up_down control for counter
                    clk,    // clock input
                    reset);          // reset input
```

where **clk** is the clock input, **reset** is the active low **synchronous** reset input, **up_down** is a one bit control input, **c_enable** is the enable signal, **c_load** is the parallel load enable, **c_out** is the parallel (16 bit) output. up_down=1'b0 means count up while up_down=1'b1 means count down. [10 marks]

d) Describe a Verilog testbench for the counter module. The clock period should be 20ns. The counter has to count up to 100 and then count down to 50. [8 marks]