OLLSCOIL NA h-EIREANN, CORCAIGH
THE NATIONAL UNIVERSITY OF IRELAND CORK

COLAISTE NA h -OLLSCOIL, CORAIGH
UNIVERSITY COLLEGE CORK

Summer 2012

FOURTH ENGINEERING (ELECTRICAL & ELECTRONIC)

Digital IC Design UE4001

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Answer Question 1 and two of the remaining three questions
3 HOURS

Approved Calculator Allowed

Questions follow overleaf

Question 1 (Answer all parts. **Each part is worth 5 marks**) **[40 marks]**

a) Describe the following terms: structural design; synthesis; system level design; algorithm complexity; asynchronous design.

b) Present the average energy dissipation due to charging and discharging of capacitive loads in the context of a digital Integrated Circuit.

c) Describe the implementation of an 8-bit parity checker and optimise it for speed using associative transformations and pipelining. Discuss your options.

d) Draw the gate level schematic of a one-bit adder and discuss its transistor complexity.

e) Implement the following logic function F using two-input NAND gates (and inverters respectively) as well as a 4 input complex gate (AOI gate):

F= NOT((IN1 AND IN2) OR (IN3 AND IN4))

Draw the corresponding transistor diagrams.

f) Define the following: cycles per data item; longest path delay; data throughput; latency; size time product; energy per data item.

g) Given the circuits in figure 1, discuss the setup and hold times for balanced distribution delays and in the presence of skew.

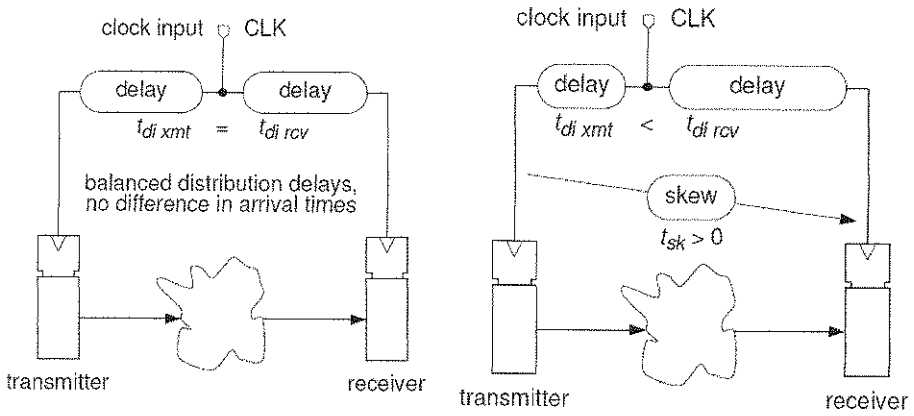

Figure 1

h) Describe two on-chip clock distribution schemes. For the on-chip interconnect, derive the propagation delay using a single buffer and multiple buffers/repeaters.

Question 2 [30 marks]

i) Explain the main architectural differences between SRAM and DRAM memories and the relevant performance (speed and power) trade-off. (5 marks)

ii) A part of a memory with four memory cells, highlighted with the dotted lines, is shown in Figure 2.

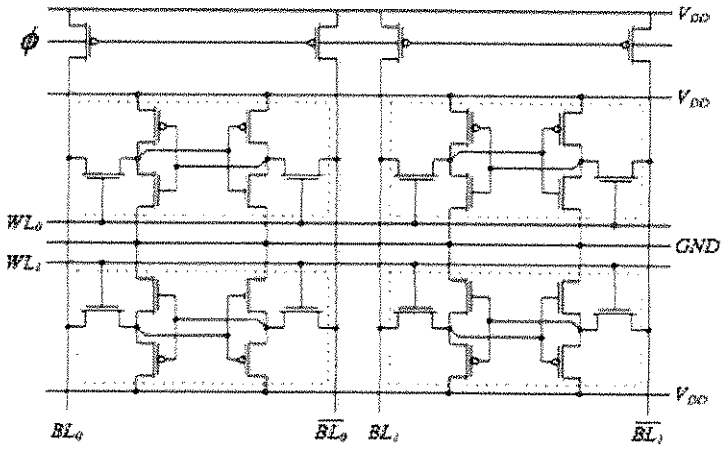

Figure 2

a. What type memory cell is it? Justify your answer. (3 marks)
b. What purpose do the four transistors at the top have? (2 marks)
c. Describe the procedure for writing a word into the memory. (5 marks)
d. Describe the procedure for reading a word from the memory. (5 marks)

iii) Describe the architecture and functionality of a latch. (10 marks)

Question 3 [30 marks]

For the circuit in Figure 3 assume a unit delay through the register and logic blocks (t_R=t_L). Assume that the registers, which are positive edge triggered, have a set-up time t_S of 1. The delay through the multiplexer t_M is 2 t_R.

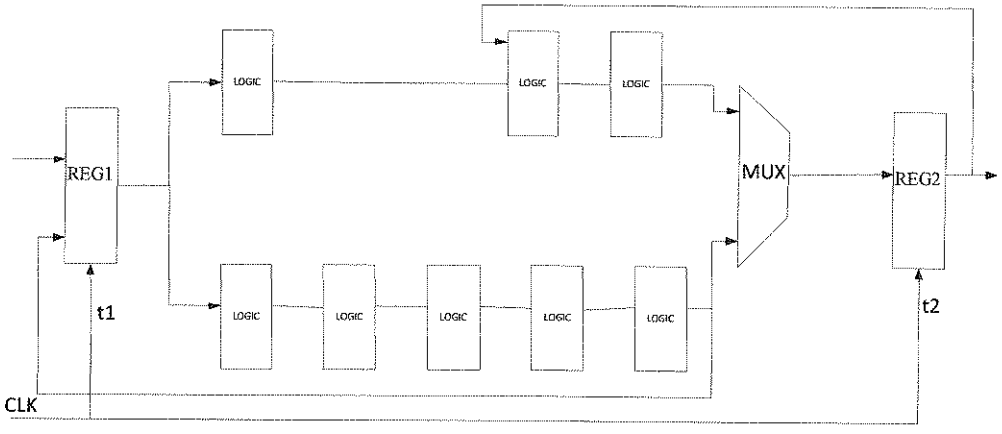

Figure 3

a) Assuming that the clock skew is zero, determine the minimum clock period of the circuit. (10 marks)

b) What is the minimum period of CLK if the clock skew is $t_{sk}=t_2-t_1=4$?(10p)

c) Given that the area of logic blocks is expressed as **AL** times 2 input XOR gates, area of the register is **AR** times 3 input NOR gates and area of multiplexer is **AMUX** times 2 input NAND gates, what is the complexity of the circuit expressed in terms of two input NAND gates (gate equivalents) and the total number of transistors.(10p)

Question 4 **[30 marks]**

a) Given the waveforms in Figure 4, describe in VHDL (or **Verilog)** the corresponding testbench which would generate them. CLK, A1 and A2 are input signals to an abstract block given by:

VHDL
entity block_A(CLOCK, A_ONE, A_TWO: in std_logic, OTP: out std_logic_vector(3 downto 0));
or
Verilog
module block_A (CLOCK, A_ONE, A_TWO, OTP);

What is the clock frequency? The time units are in nano seconds. (10marks)

b) Describe in VHDL the architecture (or Verilog module) of an entity/block for which OTP is the output of a 4 bit up-down counter with an active high reset A_TWO and up-down signal is given by A_ONE (=1 for count up, 0 for count down). Present the sequence for the counter assuming that at time 0, OTP is 3. (10 marks)

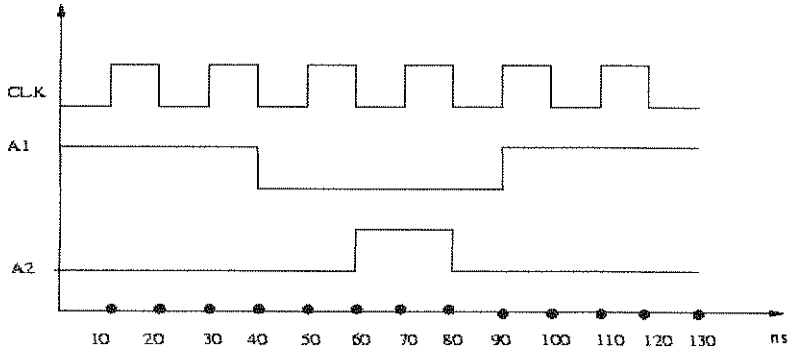

Figure 4

c) Present the schematic (block or RTL level) of the 4-bit up down counter by presenting the constituent blocks and associated gate complexity. (10 marks)