Part A

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an nmos in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda V_{DS})$$

Question 1

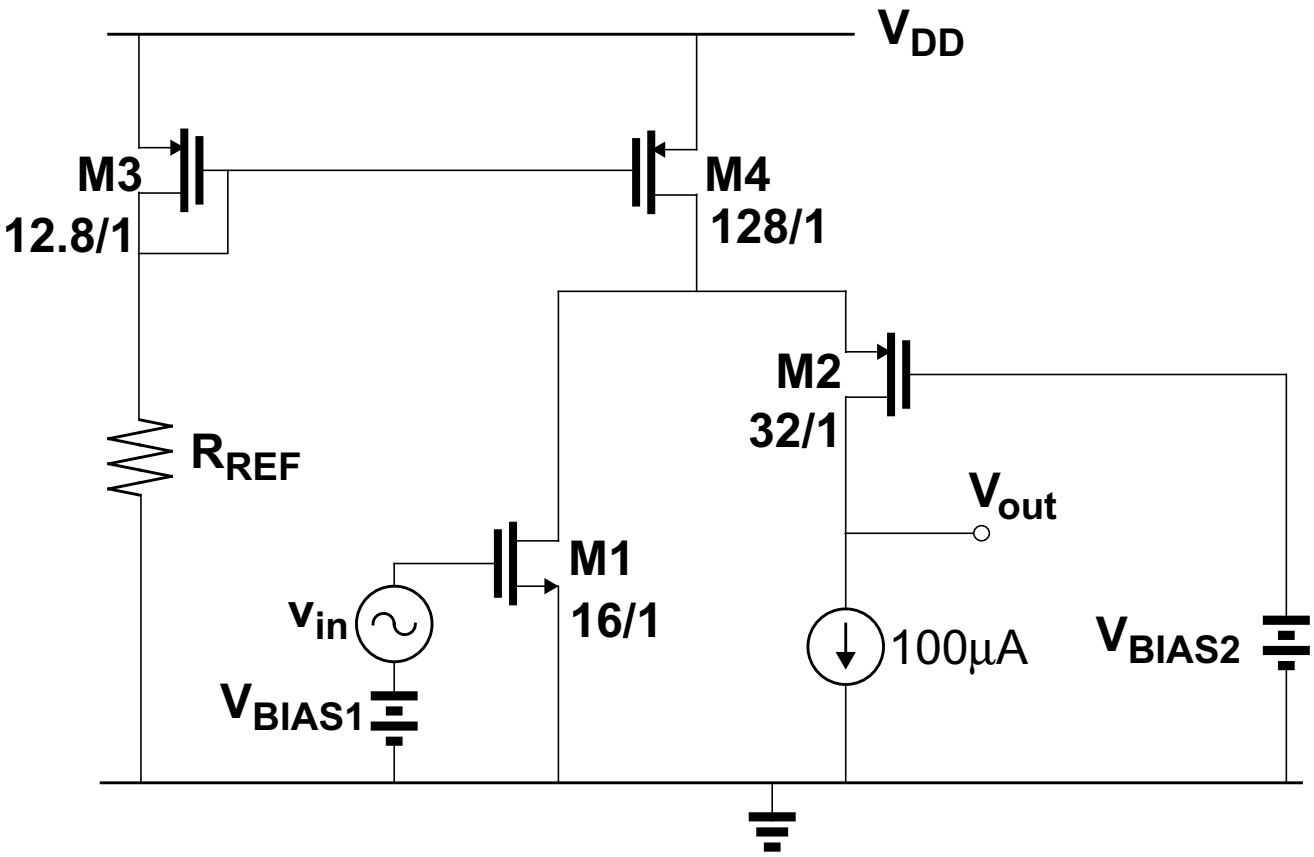

Figure 1

Figure 1 shows a folded-cascode gain stage with an ideal current source load. The bias current for the stage is provided by the current mirror and resistor R_{REF}.

$K_n'=200\mu A/V^2$, $K_p'=50\mu A/V^2$, $V_{tn}=|V_{tp}|=750mV$. $V_{DD}=3V$.
The device sizes in microns are as indicated in Figure 1.
Assume all devices are biased in saturation. For dc biasing calculations take $\lambda=0$.

(i) M1 has the same quiescent bias current as M2. What is the value of V_{BIAS1}? What are the drain currents of M3 and M4?
(ii) What value of R_{REF} is required to generate the total bias current for the folded cascode stage?
(iii) What is the maximum value of V_{BIAS2} such that M4 is in saturation?
(iv) Draw the small-signal model of the folded-cascode gain stage shown in Figure 1.
(v) Derive an expression for the output resistance i.e. the resistance looking into the output node.

Question 2

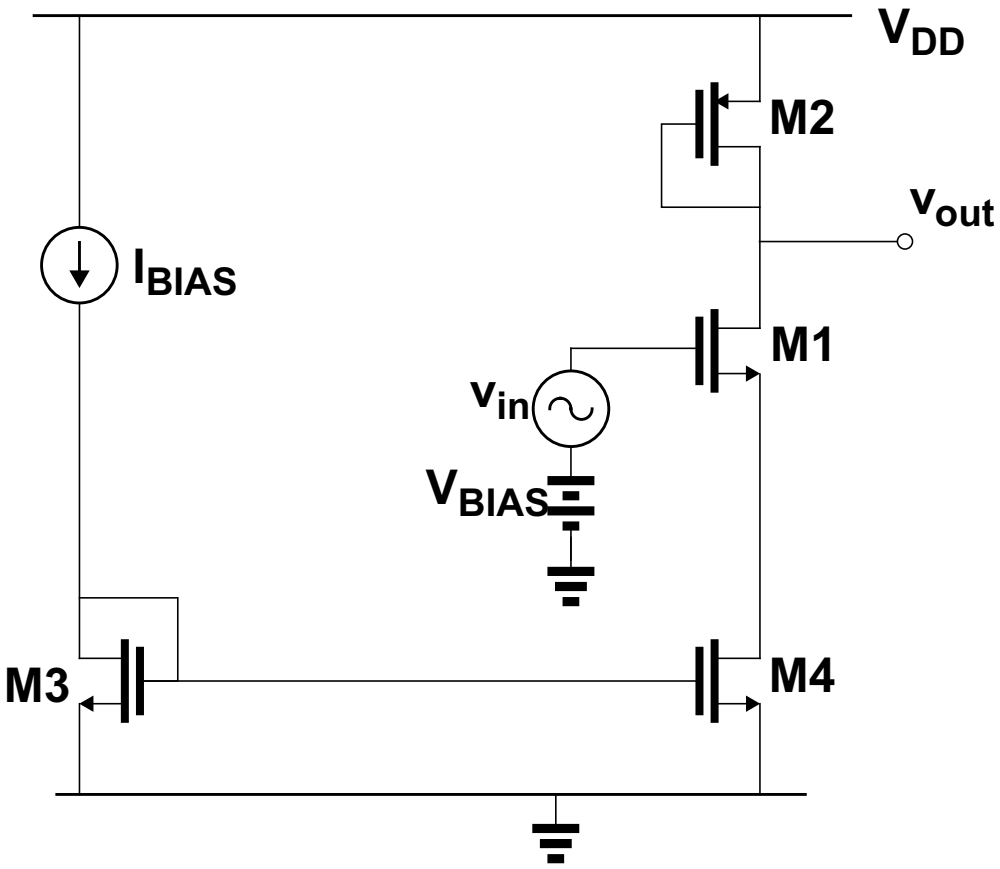

Figure 2

For each part of this question assume all nmos transistors have equal transconductances g_{mn} and output conductances g_{dsn}, and similarily that all pmos transistors have equal transconductances g_{mp} and output conductances g_{dsp}.
Assume g_{mn},g_{mp}>>g_{dsn},g_{dsp}. Ignore all capacitances.

(i) Figure 2 shows a gain stage with a diode load biased by a current mirror. Draw the small signal model for this circuit.
(ii) Show that the small signal voltage gain (v_{out}/v_{in}) is approximately given by

$$\frac{v_{out}}{v_{in}} = -\frac{g_{dsn}}{g_{mp}}$$

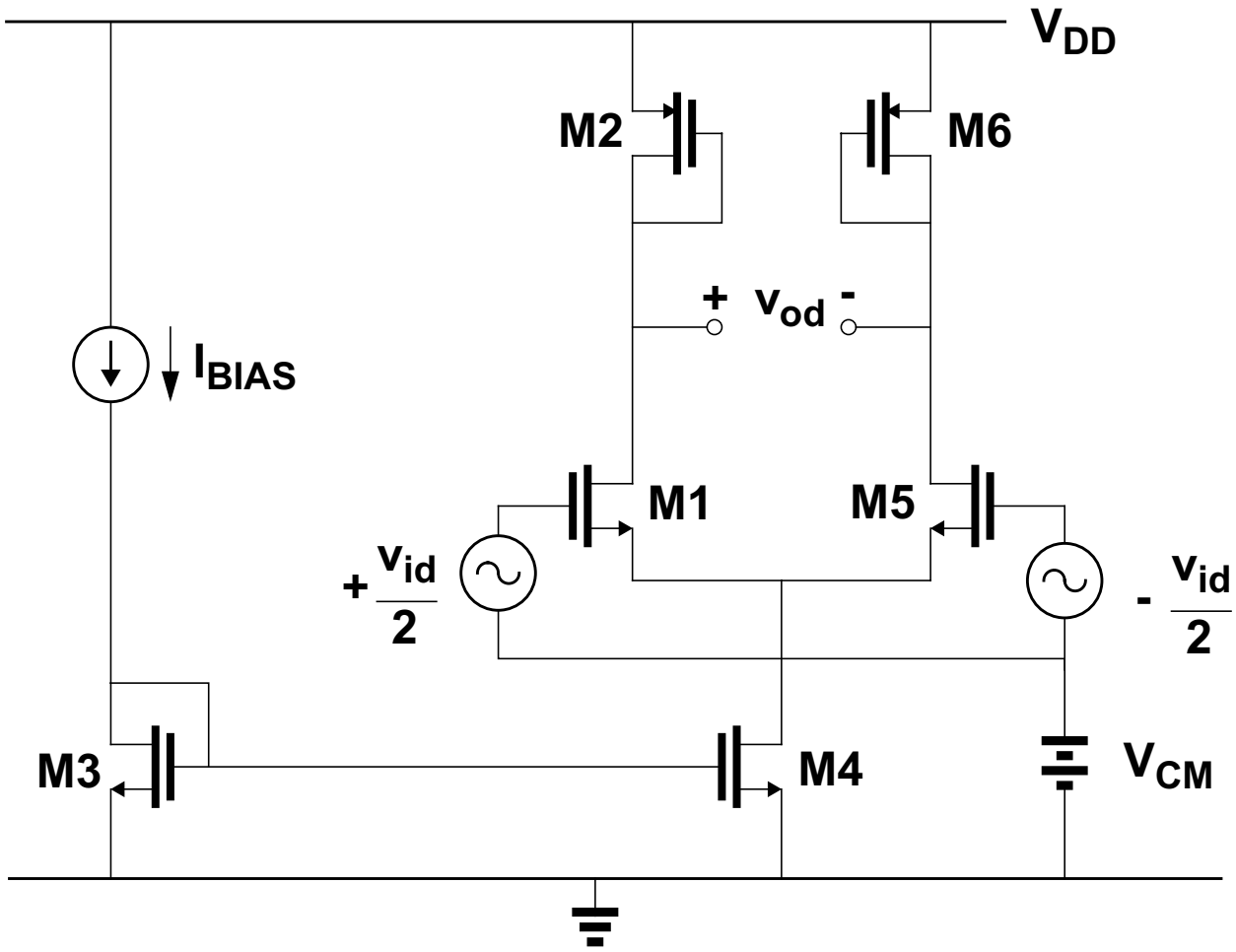

Figure 3

(iii) Figure 3 shows a differential amplifier with pmos diode loads. What is the small-signal differential gain (v_{od}/v_{id}) of this amplifier ?
You may assume the common source of M1,M5 is at ac ground.

(iv) What is the common-mode gain of the differential amplifier shown in Figure 3?

(v) What is the common-mode rejection ratio (i.e. the ratio of the differential gain to the common-mode gain) of the differential amplifier shown in Figure 3?
Calculate the common-mode rejection ratio in dB if
I_{BIAS} = 100μA,K_n'=200μA/V^2, K_p'=50μA/V^2, $\lambda_n=\lambda_p$=0.04/L V^{-1}. (L in μm)
All nmos transistors have W/L = 10μm/2μm. All pmos transistors have W/L = 40μm/2μm.

Question 3

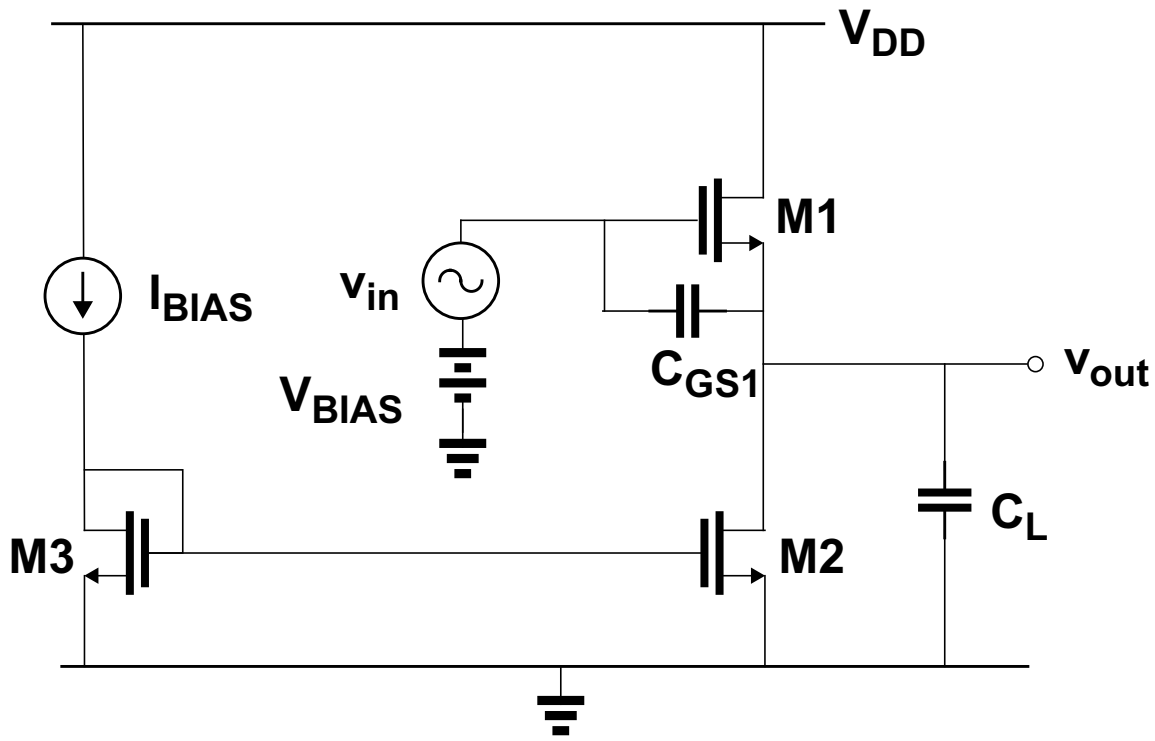

Figure 4

Figure 4 shows a source follower stage biased by a current mirror.
All transistors have equal dimensions, transconductances g_{mn} and output conductances g_{dsn}.
Assume $g_{mn} >> g_{dsn}$.

(i) Draw the small signal equivalent circuit for the source follower stage shown in Figure 4.
(ii) Derive an expression for the low-frequency small signal voltage gain (v_{out}/v_{in}).
(iii) Ignoring all capacitances except C_{GS1} and C_L derive an expression for the high frequency transfer function.
(iv) Calculate the pole and zero frequencies if V_{GS1}=1V, V_{tn}=0.75V, I_{BIAS}=100μA, C_{GS1}=1pF, C_L=9pF.
(v) Draw a Bode diagram of the gain. Indicate the dc gain and the gain at frequencies well above the pole and zero frequencies.