OLLSCOIL NA hÉIREANN, CORCAIGH
THE NATIONAL UNIVERSITY OF IRELAND, CORK

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

SUMMER EXAMINATIONS, 2007

B. E. (ELECTRICAL)
B.E. (MICROELECTRONICS)
M.ENG.SC. (MICROELECTRONICS)
H.DIP. (MICROELECTRONICS)

RF IC Design
EE4011

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Dr. K. G. McCarthy

Answer *five* questions.

All questions carry equal marks.
The use of a Casio fx570w or fx570ms calculator is permitted.
The use of mathematical/statistical tables is permitted.
Smith charts are appended to this paper. Detach and use as required. Write your examination number on any charts you use and return them with your examination script.

The following physical constants may be used as appropriate:
Boltzmann's Constant: $k = 1.38 \times 10^{-23}$ J/K
Elementary Charge: $q = 1.602 \times 10^{-19}$ C

Time allowed: *3 hours*

1. (a) Show a suitable small-signal equivalent circuit for a GaAs MESFET and derive expressions for the y-parameters of the device assuming it is considered to be a two port network with port 1 at the gate, port 2 at the drain and the source grounded. You may ignore the gate-to-drain capacitance.

[*10 marks*]

(b) Calculate the y-parameters for the device in 1(a) at a frequency of 1.5GHz using the following component values:

$R_G = 6\Omega$, $C_{GS} = 0.8$pF, $g_m = 0.15$S, $R_{DS} = 50\Omega$, $C_{DS} = 0.3$pF

[*4 marks*]

Note: Express the calculated y-parameters in polar form with the angles in degrees.

(c) If the device in 1(a) with component values in 1(b) is used as an amplifier at a frequency of 1.5GHz within a 50Ω system, without any matching networks, calculate:

(i) The input reflection coefficient (at port 1).

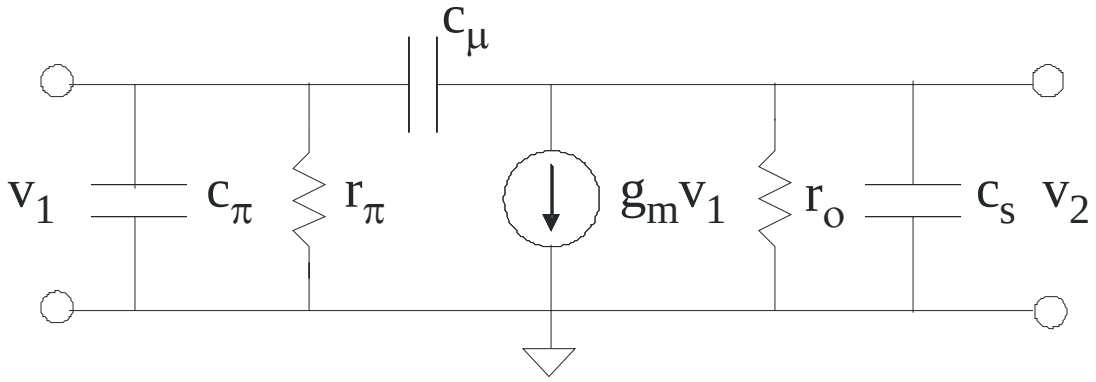
[3 *marks*]

(ii) The output reflection coefficient (at port 2).

[3 *marks*]

Note: Express the calculated reflection coefficients in polar form with the angles in degrees.

2. (a) A bipolar transistor with the following equivalent circuit has been measured at a frequency of 1GHz using a y-parameter set-up with port 1 corresponding to the input, v_1, and port 2 corresponding to the output, v_2.



The measured y-parameters are as follows:

$y_{11} = 0.0221\angle 85.7°$
$y_{12} = 0.0031\angle -90°$
$y_{21} = 0.2000\angle -0.9°$
$y_{22} = 0.0094\angle 88.8°$

From these y-parameters determine the values of the 6 elements of the equivalent circuit.

[16 *marks*]

(b) Based on the equivalent circuit and the element values determined in 2(a), determine the cut-off frequency of the transistor.

[4 *marks*]

3. (a) Show a graphical means by which the input-referred third-order intercept point (P_{IIP3}) of an amplifier can be determined by measuring the fundamental output power and the IM3 output power of an amplifier for just one input power level. Clearly identify all important parts of your diagram.

[5 *marks*]

(b) Starting with the definition of the noise factor for an amplifier, develop an expression for the sensitivity of the amplifier which specifies the minimum input power that is required to give an acceptable minimum signal-to-noise ratio, SNR_{min}, at the output. Assume the amplifier has bandwidth B, and also assume that the amplifier input forms a conjugate match to the source so that the noise power delivered from the source is given by

$$P_{RS} = kT \quad W / Hz$$

From the expression you derive, identify the noise floor of the system.

[*8 marks*]

(c) Illustrate the concept of spurious free dynamic range (SFDR) using a suitable diagram and calculate the SFDR for a receiver system that requires a minimum SNR of 12dB at the output. The system characteristics are as follows:

NF=12 dB, P_{IIP3}= -10dBm, B=1MHz, T=300K

[*7 marks*]

4. (a) Describe the principles of operation of a high-frequency balanced amplifier.

[*7 marks*]

(b) A high-frequency transistor has the following characteristics (at 4 GHz with 50Ω reference):

$$S_{11} = 0.863 \angle -79.1°$$
$$S_{12} = 0.072 \angle 36.5°$$
$$S_{21} = 3.434 \angle 106.2°$$
$$S_{22} = 0.627 \angle -58.3°$$

Sketch the input and output stability circles and the 5dB source gain circle.

[*13 marks*]

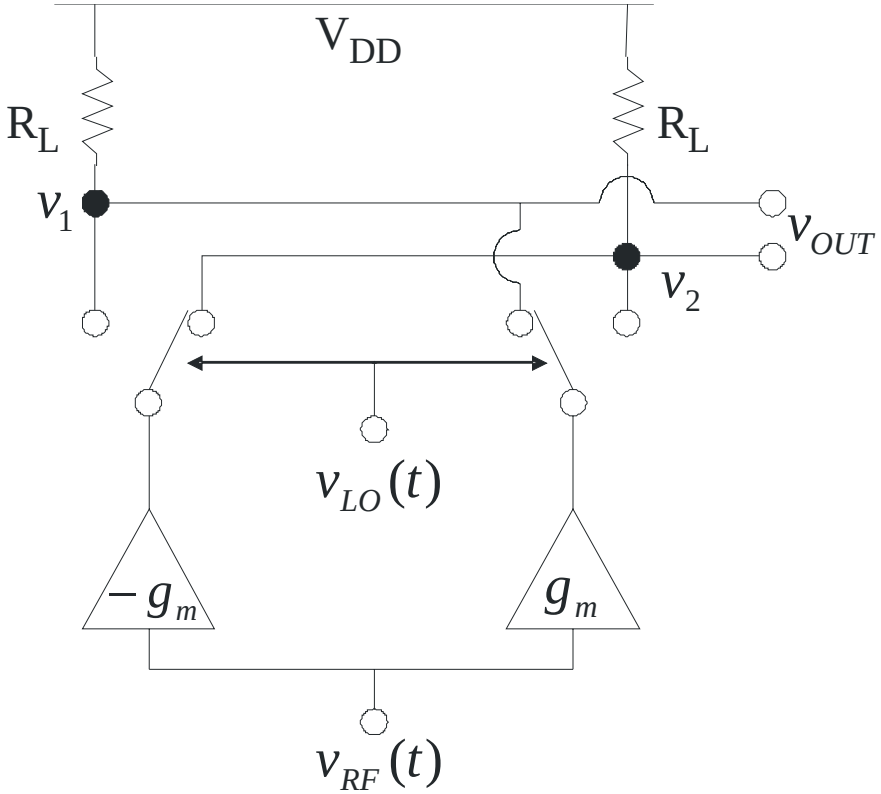
5. (a) What do you understand by the "unilateral figure of merit" of a high-frequency amplifier?

[*8 marks*]

(b) Discuss the factors which led to the development of "Direct Conversion" RFIC transceivers and identify the advantages and disadvantages of the direct conversion architecture.

[*12 marks*]

6. (a) The diagram below shows a simplified schematic of a double-balanced mixer for RF applications. The switches are ideal single-pole, double-throw switches controlled by the LO waveform and they operate 180° out of phase with each other as indicated by the connections on the diagram. Each transconductance stage draws a DC bias current, I_{DC}, through its output terminal.



Assuming the LO waveform is a square wave, and the RF waveform is cosinusoidal with a form $V_{RF}\cos(\omega_{RF}t)$, develop an expression for the output voltage, V_{OUT}, which clearly shows the frequency spectrum of the output waveform.

[12 *marks*]

Note: A square wave which toggles between 0 and 1V at a frequency of ω radians/s has a Fourier expansion as follows:

$$s(t) = \frac{1}{2} + \frac{2}{\pi}\left[\sin(\varpi t) + \frac{1}{3}\sin(3\varpi t) + \frac{1}{5}\sin(5\varpi t) + \cdots\right]$$

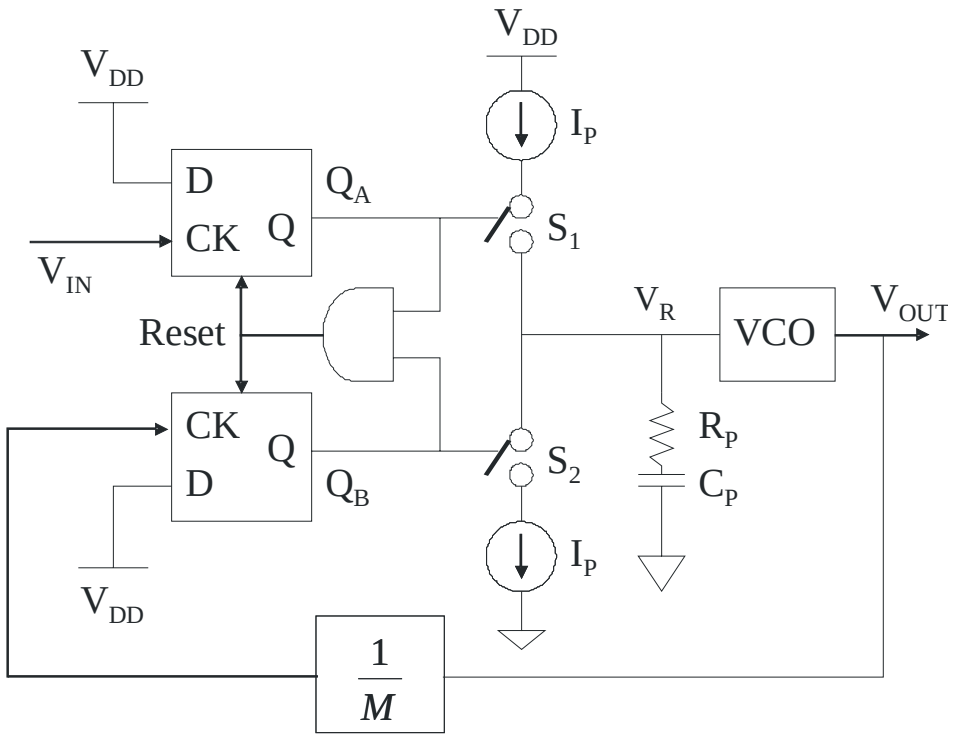
(b) If the transconductance elements in 6(a) are implemented with two bipolar transistors connected as an emitter coupled pair with a total tail current of 1mA, and the load resistors (R_L) have a value of 1kΩ, determine the voltage conversion gain of the mixer at 300K.

[*4 marks*

(c) Show a circuit diagram of a Gilbert cell that implements the mixer in part (a) with bipolar transistors. Clearly show the circuit interconnections and the inputs and outputs.

[*4 marks*]

7. (a) The diagram shows a typical Type II PLL circuit.



(i) Derive an expression for the open-loop response.

[6 *marks*]

(ii) Derive an expression for the closed-loop response.

[4 *marks*]

The "average current" method can be used to determine the transfer function of the PFD/CP combination.

(b) A Type II PLL has the following parameters:

I_P=1mA, C_P=100pF, R_P=10kΩ, K_{VCO}=100MHz/V, M=1000

(i) Determine the natural frequency.

[2 *marks*]

(ii) Determine the damping factor.

[2 *marks*]

(c) Show a suitable schematic for a Delay Locked Loop (DLL) to produce four clock phases with equal delay between the phases and describe the unique elements of the circuit compared to a standard PLL.

[6 *marks*]

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