OLLSCOIL NA hÉIREANN
THE NATIONAL UNIVERSITY OF IRELAND

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

Summer 2010
2010 Engineering (Electrical & Electronic) Examination

Microelectronics (UE4008)

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Time allowed **1 ½ Hours**
Answer three out of four questions

Approved calculator permitted.

Question 1:

a) With the aid of diagrams describe the gate and channel region of a modern CMOS transistor, explain how elements of this device differ from a CMOS device of greater than 1.0μm channel length. Modern devices can be considered to be those in processes from 90nm down to 45nm. Explain the reasons for these process changes.
b) If a 60nm CMOS process has 1.2nm of silicon dioxide as the gate dielectric, calculate the gate capacitance and also calculate the thickness of dielectric that would be used if the material was changed from silicon dioxide to Hafnia ($Hf0_2$) whilst maintaining the same capacitance per unit area.

Given:
The permittivity of free space is 8.86 X 10^{-14} F/cm
The dielectric constant of hafnia ($Hf0_2$) is 25

Question 2:

a) In thermal oxidation of silicon explain why the initial growth rate is faster that the growth rate after a significant oxidation time.
b) Explain the function of the silicon nitride layer in the formation of a LOCOS or Semi-Recessed field oxide.
c) Explain why, particularly in P-doped field regions, it is normal to bring up the boron doping concentration under the field oxide by having a field implant prior to oxide growth?
d) A silicon <100> wafer, which had been patterned and etched with bare silicon in the patterned windows and 0.4μm in the other areas, is put through a thermal oxide process at 1000°C in pyrogenic steam for 2 hours 10 minutes, what is the final oxide thickness in:
    i) The areas which had no oxide on the surface prior to oxidation?
    ii) The areas which had 0.4μm on the surface prior to oxidation?

Oxide Growth in Pyrogenic Steam Plot included.

Question 3

a) Explain why a CMOS process needs ion implant technology and cannot be fabricated using simple furnace doping techniques.
b) Compare the doping concentration versus depth into silicon for pre-deposition and drive-in for different furnace times; explain the reason(s) for the differences.
c) If Phosphorus at a dose of 1 x 10^{16} ions/cm^2 is implanted into a boron doped wafer with a substrate doping of 1 x 10^{15}atoms/cm^3 through an oxide of thickness 170nm so that the peak of the implant sits at the interface between the silicon and the oxide.

i. Calculate the energy at which the implant is carried out
ii. What will the resulting junction depth be if given a heat treatment that activates the dopant but causes no further dopant diffusion.
iii. How much oxide will be needed to block the implant in the areas that are not to be doped?

Projected Range and Projected Standard Deviation Graphs attached.

Question 4

a) Describe in simple terms the operation of an enhancement mode NMOS transistor; explain how the gate controls the current flow between source and drain. Use cross-sectional diagrams to illustrate the answer. Indicate what bias is applied at various stages of operation; mention how the biasing of the "back gate" or substrate contact affects the threshold voltage.

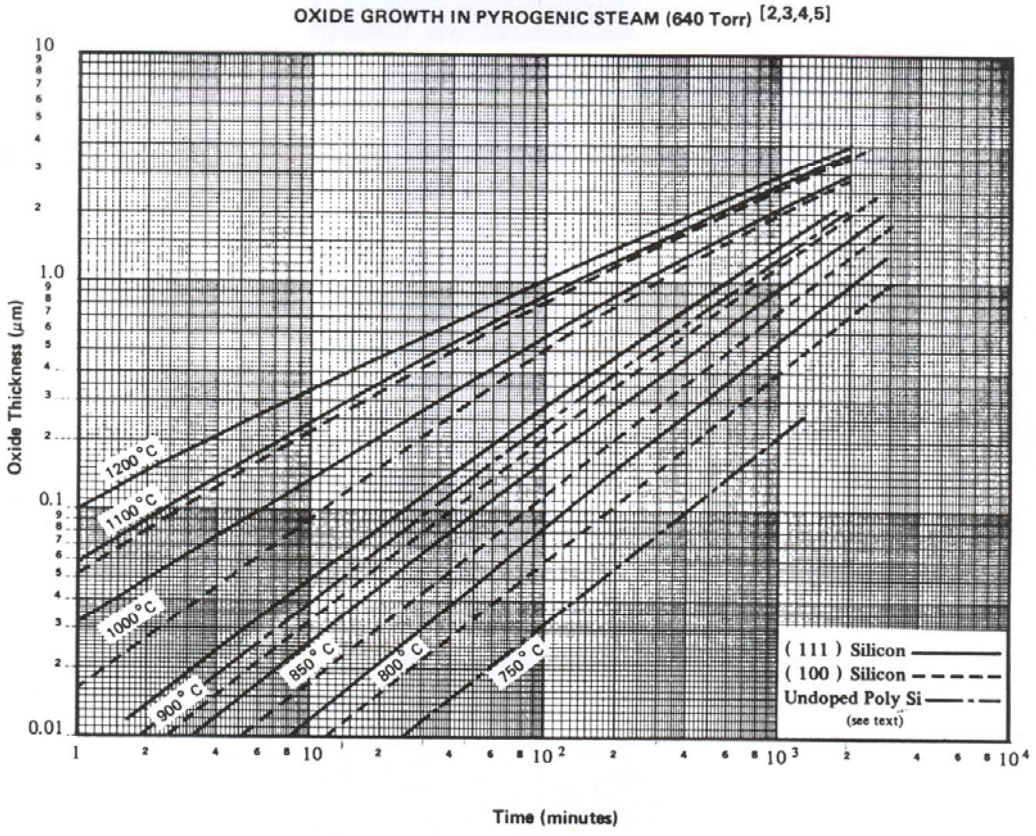
(b) If the polysilicon gate of an NMOS transistor in a Self-Aligned LOCOS process is over etched during processing by 0.1μm per side, calculate the change in maximum saturated current that would result on a transistor with a design gate length of 1.0μm and width of 10μm. What would the affect if the LOCOS processing meant the "birds beak" (LOCOS edge) encroached into the active area 0.5μm all round?

Given

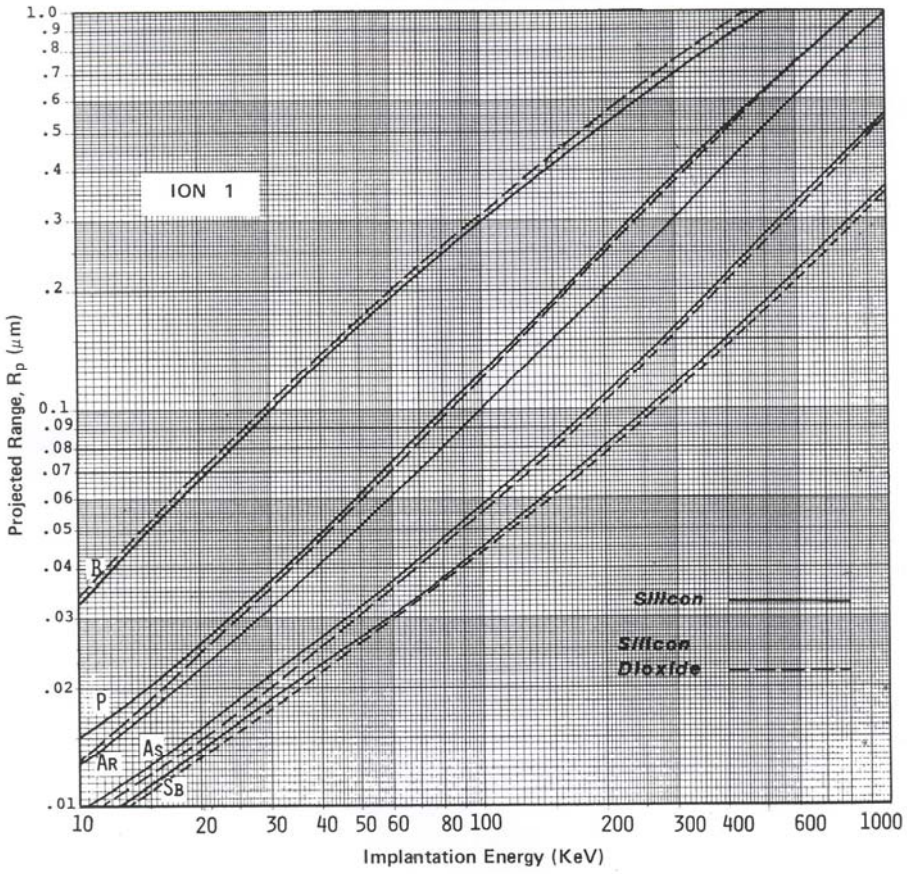
V_t = 0.8V and the maximum power supply voltage is 5.0V

μ_n = 1450cm^2/V.s

C_{ox} = 5 x 10^{-8}F/cm^2


OXIDE GROWTH IN PYROGENIC STEAM (640 Torr) [2,3,4,5]
Oxide Thickness (μm)
10
1.0
0.1
0.01
1200 °C
1100 °C
1000 °C
900 °C
850 °C
800 °C
750 °C
(111) Silicon
(100) Silicon
Undoped Poly Si
(see text)
1
10
10 2
10 3
10 4
Time (minutes)

PROJECTED RANGE IN SILICON & SILICON DIOXIDE[1]



PROJECTED STANDARD DEVIATION IN SILICON & SILICON DIOXIDE[1]