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THE NATIONAL UNIVERSITY OF IRELAND, CORK

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

SUMMER EXAMINATIONS, 2012

B. E. (ELECTRICAL AND ELECTRONIC)
M.ENG.SC. (MICROELECTRONICS)
VSEU (VISITING EUROPEAN)

RF IC Design
EE4011

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Answer *five* questions.

All questions carry equal marks.

The use of departmental approved non-programmable calculators is permitted.

Smith Charts are appended to this paper. Detach and use as required. Write your examination number on any charts you use and return them with your examination script.

The following physical constants may be used if necessary:

Boltzmann's Constant: $k = 1.381 \times 10^{-23}$ J/K
Elementary Charge: $q = 1.602 \times 10^{-19}$ C
Vacuum Permittivity: $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m
Dielectric Constant of Silicon-Dioxide (SiO_2): $\varepsilon_r = 3.9$

Time allowed: *3 hours*

Questions Begin on Next Page

1. (a) Draw a small-signal model suitable for an RF MOSFET. Include as many small-signal elements as you think are necessary to allow the device behaviour to be represented accurately. Clearly label these elements and provide a brief description of each element.

[*4 marks*]

(b) Define the ABCD parameters for a two-port network.

[*2 marks*]

(c) An n-type MOSFET has the following geometry, temperature, bias conditions and device parameters:

Geometry:	$W = 200\mu m$, $L = 0.35\mu m$
Parameters:	$T_{ox} = 5nm$, $\mu = 400cm^2/Vs$, $V_{TH} = 0.7V$, $\lambda = 0.01\ V^{-1}$, $R_G = 10\Omega$
Bias Conditions:	$V_{GS} = 2V$, $V_{DS} = 2.5V$, $V_{BS}=0V$
Temperature:	300K

Determine the ABCD parameters of the device at 10GHz when it is configured for 2-port measurements with the gate connected to port 1 and the drain connected to port 2. For this calculation assume that the only significant capacitance is C_{GS}. Present the ABCD parameters in magnitude and phase format with the phase in degrees.

[*9 marks*]

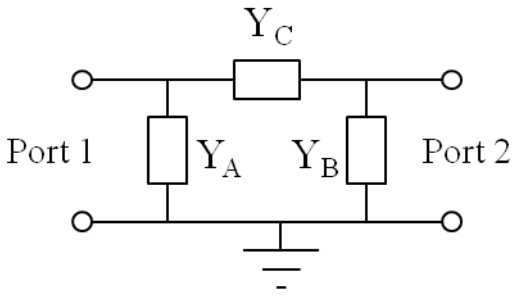
(d) Draw an approximate sketch to illustrate the velocity vs. electric field characteristic of electrons and briefly describe the important parts of this characteristic.

[*2 marks*]

(e) Assuming that the cut-off frequency of a MOSFET is strongly influenced by the channel transit time of the carriers and using the characteristic illustrated in part (d), develop an approximate relationship between the cut-off frequency of a MOSFET and its channel length for both long- and short-channel devices.

[*3 marks*]

2. (a) Determine the y-parameters of the following network, where the elements Y_A, Y_B and Y_C are admittances.

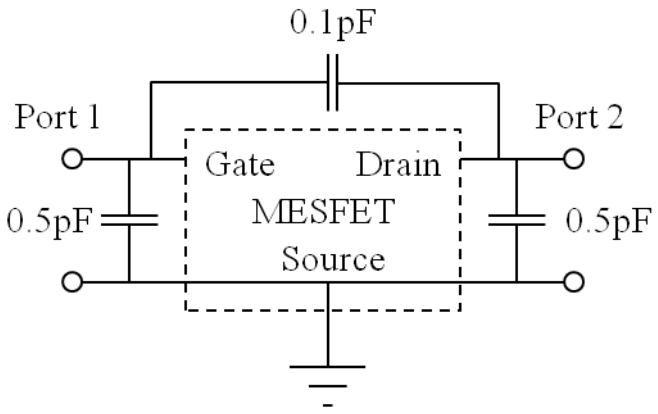


[*4 marks*]

(b) For two networks connected in parallel, state how the y-parameters of the combination of networks can be determined from the y-parameters of the individual networks.

[*2 marks*]

(c) Y-parameter measurements have been performed on a MESFET at a frequency of 3GHz. Because of the design of the test structure, the intrinsic device was surrounded by undesired parasitic capacitances as illustrated below:



The measured y-parameters for the full set-up (device and parasitic capacitances) are as follows:

$y_{11} = 0.0264 \angle 88.03°$
$y_{12} = 0.0019 \angle -90°$
$y_{21} = 0.0999 \angle -4.53°$
$y_{22} = 0.0247 \angle 57.26°$

Determine the y-parameters of the intrinsic MESFET (the MESFET on its own).

[*4 marks*]

(d) The MESFET in part (c) can be represented by a small-signal equivalent circuit. Assuming that R_G, C_{GS}, g_m, R_{DS} and C_{DS} are the only significant elements of this small-signal network, determine their values and the cut-off frequency of the device.

[*10 marks*]

3. (a) State the formula for the noise factor of an amplifier and define all the quantities in the formula.

[*2 marks*]

(b) Derive an expression for the noise factor of a two-port network driven by a source with resistance R_S. The two-port can be considered to be a voltage amplifier with gain A and small-signal input resistance R_{IN}. For the noise analysis, assume that the two-port can be represented by a noiseless two-port with equivalent input-referred noise voltage and current sources (which are correlated). The small-signal input resistance, $R_{IN,}$ does not contribute noise

[*12 marks*]

(c) The equivalent input-referred noise voltage and current sources of a bipolar transistor at moderate frequencies are given by:

$$\overline{v^2} = 4kT\left(r_b + \frac{1}{2g_m}\right)\Delta f \quad \overline{i^2} = 2q\frac{I_C}{\beta}\Delta f$$

where r_b is the parasitic base resistance and the other symbols have their usual meaning.

A BJT is biased in the forward active region with a collector current of 1.5mA at 300K. It has a forward active current gain of 100 and a parasitic base resistance of 100Ω. Determine the noise figure (in dB) of the BJT for a bandwidth of 1Hz if it is driven by a source with an impedance of 50Ω.

[*4 marks*]

(d) Determine the noise temperature of the BJT in part (b).

[*2 marks*]

4. (a) An RF transistor is used to make a single-transistor Low Noise Amplifier. It has the following characteristics at 5GHz in a 50Ω system:

$$s_{11} = 0.55\angle -150° \quad s_{12} = 0.04\angle 20° \quad s_{21} = 2.82\angle 180° \quad s_{22} = 0.45\angle -30°$$

$$F_{\min} = 3.0\,dB \quad \Gamma_{opt} = 0.45\angle 180° \quad R_N = 4\Omega$$

Using a Smith-Chart, design input and output matching networks to give a source gain of 1.2dB and a load gain of 0.7dB at 5GHz. The source and load impedances are both 50Ω and make an approximation that the transistor is unilateral.

[*12 marks*]

Note:

The following formulae specify the source gain circle where the symbols have their usual meaning:

$$|C_S| = \frac{g_s |s_{11}|}{1 - |s_{11}|^2 (1 - g_s)} \qquad R_S = \frac{\sqrt{1 - g_s}\left(1 - |s_{11}|^2\right)}{1 - |s_{11}|^2 (1 - g_s)}$$

Formulae for the load gain circle are similar with substitution of appropriate quantities.

(b) For the LNA designed in part (a):

(i) Determine if the LNA is stable.

[*2 marks*]

(ii) Determine the unilateral transducer gain (in dB).

[*2 marks*]

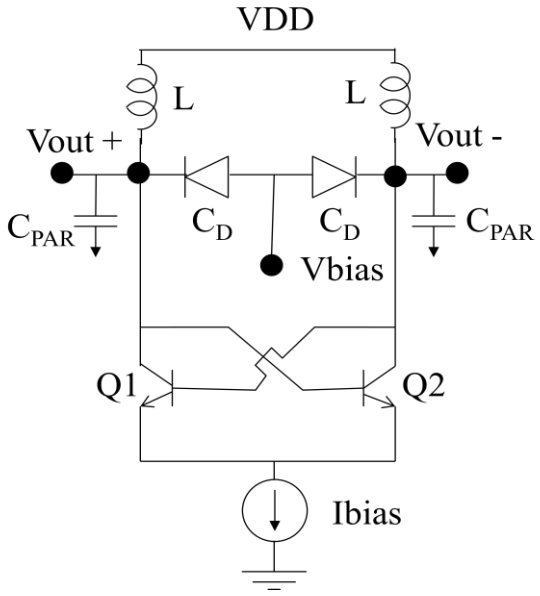
(iii) Determine the maximum error (in dB) when approximating the transducer gain by the unilateral transducer gain.

[*2 marks*]

(iiiv) Comment on the expected noise performance.

[*2 marks*]

5. (a) The circuit below shows a LC oscillator. Each of the inductors has a value of 5nH and the parasitic capacitance at each output node, C_{PAR}, is 0.6pF which includes all the capacitance at each node except the capacitance contributed by the varactor diodes, C_D. Transistors Q1 and Q2 are identical NPN devices and the circuit operates at 300K.



Using an appropriate small-signal analysis, determine the input resistance of the cross-coupled NPN transistors, Q1 and Q2, and use this to specify the condition needed to sustain oscillation in the circuit if the inductors are resistive. Ignore the base current of the transistors in your analysis.

[*10 marks*]

(b) If the inductors in part (a) have a parasitic resistance of 10Ω, calculate the minimum current, *Ibias*, needed to ensure oscillation.

[*2 marks*]

(c) If the circuit in part (a) is intended to oscillate at a frequency of 1.8GHz when the voltage across the varactor diodes is 0V, determine the zero-bias capacitance of these diodes.

[*2 marks*]

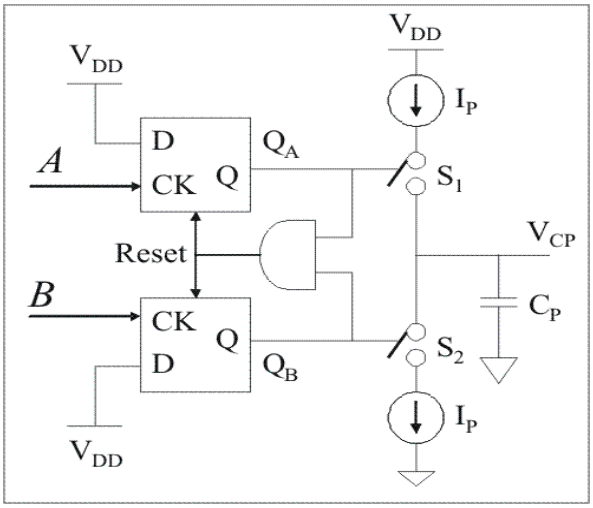
(d) If the varactor diodes in parts (a) and (c) have a built-in potential of 0.75V and a junction grading coefficient of 0.3, determine the percentage change in the oscillation frequency when the voltage on the varactor diodes changes from 0V to a reverse bias of 1V.

[*4 marks*]

(e) Specify a component that is used in modern CMOS technologies to form a voltage-controlled capacitance instead of a varactor diode and briefly sketch its C-V characteristics.

[*2 marks*]

6. (a) The following topology is frequently used to implement a combined phase-frequency detector/charge-pump (PFD/CP) in Type II PLLs.:



Illustrate the operation of this circuit using clear timing diagrams for the case where logic waveforms of the same frequency are applied to lines A and B, but where A leads B by a phase angle $\Delta\phi$, assuming that the voltage V_{CP} begins at 0V. Using your diagram as a starting point, derive an expression for the s-domain transfer function of this circuit.

[*5 marks*]

(b) Show the overall block diagram for a full Type II PLL based on the PFD/CP in part (a), with an integer divider and also include any extra component that you think is necessary to improve the stability of the system. Derive an expression for the closed-loop transfer function of the full PLL.

[5 *marks*]

Note: The denominator of 2nd-order systems is written in standard form as:

$$s^2 + 2\varsigma\omega_n s + \omega_n^2$$

(c) A Type II PLL has the following parameters:

I_P=0.5mA, C_P=150pF, R_P=20kΩ, K_{VCO}=100MHz/V, M=200

(i) Determine the natural frequency of the closed-loop system response.

[2 *marks*]

(ii) Determine the damping factor of the closed-loop system.

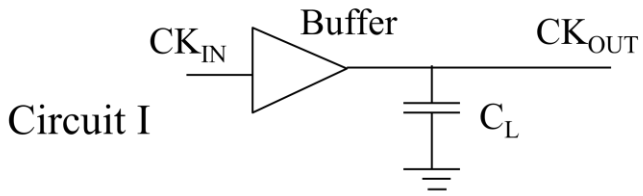
[2 *marks*]

(iii) If K_{VCO} varies across the tuning range, determine the lowest allowable value of K_{VCO} if the damping factor cannot go more than 20% lower than its nominal value.

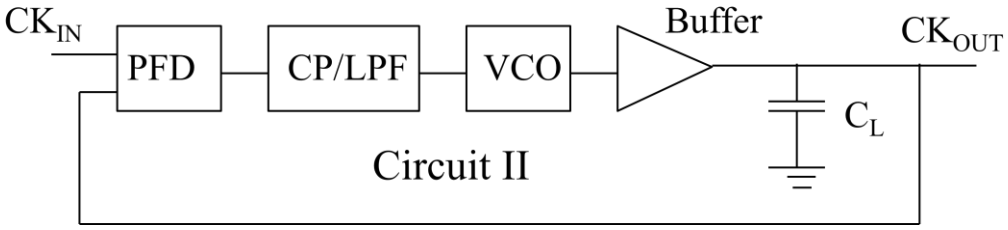
[2 *marks*]

Question 6 is continued on the next page

(d) Circuit I below is often used in digital ICs. Here, a non-inverting digital buffer is used to drive the clock signal to a large set of digital gates (represented by the load capacitance C_L) from an input clock line CK_{IN}.



Circuit I



Circuit II

Describe and illustrate using sample clock waveforms how Circuit II above can eliminate the most common problem associated with Circuit I.

[4 *marks*]

7. (a) Draw a detailed block-level architecture of a single-chip GPS/Galileo receiver and outline the functions of the main blocks in the IC providing details of frequencies, bandwidth, gain, noise levels and data rates as appropriate.

[*10 marks*]

(b) Answer EITHER section (i) OR section (ii) below:

EITHER:

(i) For the GPS receiver in part (a), select one block from the overall architecture and discuss the design of this block in detail. In your discussion, show a more detailed schematic diagram of the block you choose (if necessary) and outline the typical design trade-offs that must be made when designing this block, as well as the typical performance characteristics that can be achieved with a single-chip CMOS approach.

[*10 marks*]

OR:

(ii) Discuss the operation of the GPS system including the frequencies, power levels and the modulation and coding schemes used. Show how the characteristics of the GPS system lead to the specifications for receiver systems such as the single-chip solution discussed in part (a).

[*10 marks*]

End of Examination Paper