ADVANCED ENERGY®

Better technology. Better results.

Overview of the Use of Copper Interconnects in the Semiconductor Industry

Annabelle Pratt, Ph.D., Advanced Energy Industries, Inc.

This paper presents an overview of the use of copper for interconnects in integrated circuits (ICs). Topics include the benefits of using copper, the process development history for depositing copper on a wafer, and a discussion of the electroplating process step.

Interconnects in integrated circuits distribute clock and other signals and provide power/ground to the various integrated circuits. There are three types of interconnects: local, intermediate, and global.

- *Local interconnects consist of very thin lines, connecting gates, and transistors within a functional block. They usually span only a few gates and occupy first and, sometimes, second metal layers.*
- *Intermediate interconnects are wider and taller than local interconnects in order to provide lower resistance; intermediate wiring provides clock and signal distribution within a functional block with typical lengths up to 3 to 4 mm.*
- *Global interconnects provide clock and signal distribution between the functional blocks and deliver power/ground to all functions. Global interconnects occupy the top one or two layers, and they are longer than 4 mm—as long as half the chip perimeter. It is critical that low-resistivity global interconnects be used as the bias voltage decreases and the total current consumption of the chip increases [1].*

Contents

The interconnects in an integrated circuit are becoming the dominant factor in determining system performance and power dissipation [2]. It is illuminating to consider that the interconnection of over 400 million transistors will require several miles of interconnects at 100 nm technology, as shown in Table 1.

Table 1 Attributes of microprocessor chips at different technology nodes [3]

Year	2001	2003	2005	2007
Technology node	130 nm	100 nm	80 nm	65 nm
Transistors/chip	276 M	439 M	697 M	1106 M
Transistors/cm² (including on-chip SRAM)	38.6 M	61.2 M	97.2 M	154.3 M
Chip size	3.1 cm²	3.1 cm²	3.1 cm²	3.1 cm²
Local wiring pitch	350 nm	245 nm	185 nm	150 nm
Number of metal layers	8	8	10	10
Total interconnect length (excluding global wiring)	7.8 mi	11.1 mi	17.5 mi	21.5 mi
Interconnect RC delay 1 mm line	86 psec	176 psec	256 psec	342 psec

The on-chip local clock frequency of circuits built with 65 nm technology is projected to be approximately 6.7 GHz, which results in the interconnect resistance-capacitance (RC) time delay per 1 mm line exceeding a clock cycle [3].

Benefits of Copper

The most important benefit of using copper in integrated circuits is that copper offers lower resistivity than aluminum, which historically has been the dominant interconnect material. Using a lower resistivity interconnect material like copper decreases the interconnect RC delay, which, in turn, increases the IC speed. The intrinsic speed limit of an integrated circuit is determined by the frequency at which its transistors can be turned on and off. Since smaller transistors have inherently higher clock frequencies, advances in IC speed historically have been achieved by downward scaling of feature sizes. Currently, however, the speed limit of advanced ICs is set by the delay in signal propagation in the metal interconnect lines [4], which is determined by the time constant of the line. The time constant is the product of the resistance of the line and the capacitance between the line and all adjacent lines.

The resistance R of the basic structure of conductive material shown in Figure 1 is expressed in Equation 1. It is determined by the geometry and the resistivity ρ of the interconnect material. Similarly, the capacitance C between two parallel plates, shown in Figure 2, is expressed in Equation 2. Capacitance C between the plates is determined by the geometry and the relative permittivity ε_r of the dielectric between the plates.

Equation 1

$$R = \frac{\rho L}{WT}$$

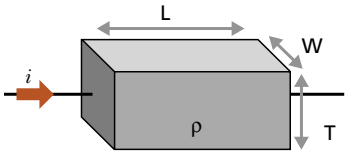

Figure 1 Basic structure for resistance

Where:

R = Resistance
ρ = Resistivity of the conductive material
L = Length of the conductive material
W = Width of the conductive material
T = Thickness of the conductive material

Equation 2

$$C = \frac{\varepsilon_0 \varepsilon_r \, lw}{d}$$

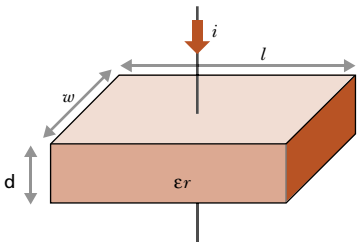

Figure 2 Basic structure for capacitance [4]

Where:

C = Capacitance

l = Length of plate

w = Width of plate

ε_0 = The permittivity of free space

ε_r = The relative permittivity of the dielectric

d = Distance between plates

The RC time constant of the generic multi-layer stack illustrated in Figure 3 can be calculated as [4]:

$$R_w C_w = 2R_w (C_V + C_L) = \frac{2\rho L}{WT}\left(\frac{\varepsilon_0 \varepsilon_r WL}{H} + \frac{\varepsilon_0 \varepsilon_r TL}{X}\right) = 2\rho\varepsilon_0\varepsilon_r \frac{L}{WT}\left(\frac{WL}{H} + \frac{TL}{X}\right) = 2\rho\varepsilon_0\varepsilon_r \left(\frac{L^2}{TH} + \frac{L^2}{WX}\right)$$

Where:

R_w = Resistance of the interconnect

C_w = Capacitance associated with the interconnect

C_V = Inter-layer capacitance

C_L = Intra-layer capacitance

L = Length of the interconnect

W = Width of the interconnect

T = Thickness of the metal layer

H = Height of the dielectric layer

X = Spacing between adjacent interconnects

P = Pitch of the line

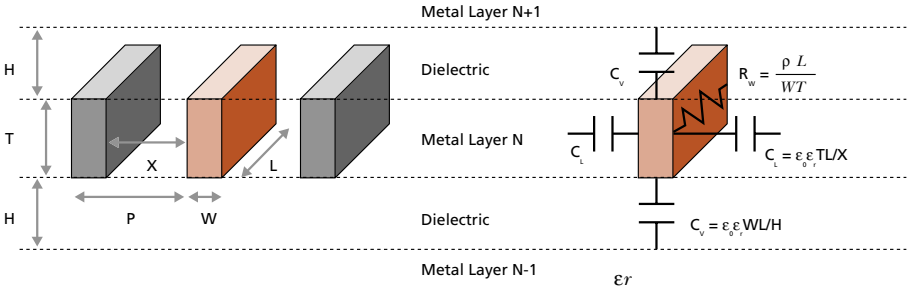

Figure 3 Generic multi-layer stack

Assuming that H = T and P = 2W (that is, X = W), the equation can be simplified to:

$$R_w C_w = 2\rho\varepsilon_0\varepsilon_r L^2\left(\frac{1}{T^2}+\frac{4}{P^2}\right)$$

This equation shows that the RC time constant of the interconnect can be reduced by reducing the resistivity of the interconnect material, using a dielectric with a low permittivity and/or making the line lengths as short as possible. Copper, which has a resistivity ρ of only 1.7 μΩ.cm, provides a reduction of almost 40% in resistivity over aluminum, which has a ρ of 2.7 μΩ.cm; typical aluminum alloys can have ρ as high as 3 μΩ.cm [4]. Since the RC time constant is directly proportional to the resistivity, a 40% reduction in the RC time constant can be achieved by using copper rather than aluminum. By combining the copper interconnect with a dielectric material with a low permittivity, the interconnect RC delay can decrease to 50% of that for Al/SiO_2 [5]. The interconnect RC delay can also be reduced by increasing the thickness T of the metal layer, that is, increasing the aspect ratio AR, or increasing the pitch P of the line. However, when the aspect ratio is increased by increasing T, the capacitance C_L is increased, and high aspect ratios are hard to fill uniformly; therefore, industry roadmaps predict local wiring AR <1.7 and global wiring AR < 2.2 through 65 nm technology [3, 6].

The delay in signal propagation between two transistors is caused by the interconnect RC time constant and the capacitive loads, given approximately by:

$$t_{\text{int}} \cong R_o C_w + 0.4\left(\left(R_w C_w\right)^{1.6} + \left(t_{of}\right)^{1.6}\right)^{1/1.6} + 0.7 R_w C_{in}$$

Where:

t_{int} = Delay in signal propagation between two transistors
R_o = Output resistance of the driver device
C_w = Capacitance associated with the interconnect
R_w = Resistance of the interconnect
t_{of} = Time of flight of the electromagnetic wave along the interconnect, which is approximately equal to:
$t_{of} = \sqrt{\mu_0 \varepsilon_0 \varepsilon_r} \approx 3.3\sqrt{\varepsilon_r}$ psec/mm [6]
C_{in} = Input capacitance of the next device

A change to copper will lower R_w only, and the dielectric material has to be changed to lower t_{of}. In the above model, the inductance of the line is ignored, but it is useful to keep in mind that the use of copper can amplify overshoot of a signal, since the Q factor is increased by reducing the resistance [7].

Other advantages of copper include that copper has twice the thermal conductivity of aluminum and copper has ten to 100 times more resistance to electromigration failures than aluminum [4]. Electromigration causes transport of the conductor material as a result of high current densities, which can ultimately lead to a void in the conductor [8]. The use of copper results in a power consumption reduction of 30% at a specific frequency. By using copper rather than aluminum as interconnect material, the interconnect routing can be simplified, reducing the number of interconnect levels and resulting in fewer process steps. This translates to cost savings and higher device yield [5].

Damascene Process

The word *damascene* is derived from the city of Damascus in Syria, and the damascene process was originally developed for jewelry manufacturing. This section explains the damascene process as it relates to interconnects.

History of Copper Interconnects

Since the inception of integrated circuit manufacturing, aluminum as a conductor and SiO_2 as an insulator have been the materials of choice. The transition to copper as a conductor is one of the most significant changes in semiconductor manufacturing history. Manufacturers have long recognized the benefits of using copper interconnects, but switching to copper only became a priority in the late 1980s as feature sizes decreased. The first working microprocessor using copper was made by IBM® in 1997. By 1998, the process was used in high-volume manufacturing in IBM's Burlington, Vermont, facility [8].

Replacement of aluminum by copper was an enormous obstacle for semiconductor process engineers, since aluminum is deposited over the entire wafer surface and then patterned by reactive ion etching (RIE), and all efforts to apply RIE to copper failed. Copper cannot be patterned, and a new process had to be developed that could successfully fill a patterned dielectric. Various forms of PVD, including sputtering, deposition etch, electron cyclotron resonance, as well as CVD and electroless plating were examined initially [8]. It was found to be very difficult to cover trench walls with PVD, and CVD will tend to result in conformal growth, which leaves a seam in the middle of the trench [9]. The damascene process has emerged as the industry standard. Superfilling, which refers to the effect where higher deposition rates are achieved in the bottom of trenches than on the sides, resulting in void-free and seamless filling of trenches and vias for high aspect ratio features, played a pivotal role in the success of this technology [8, 10]. Superfilling characteristic of electroplating is discussed on page 16.

Damascene Process Steps

The damascene process has three steps, as shown in Figure 4.

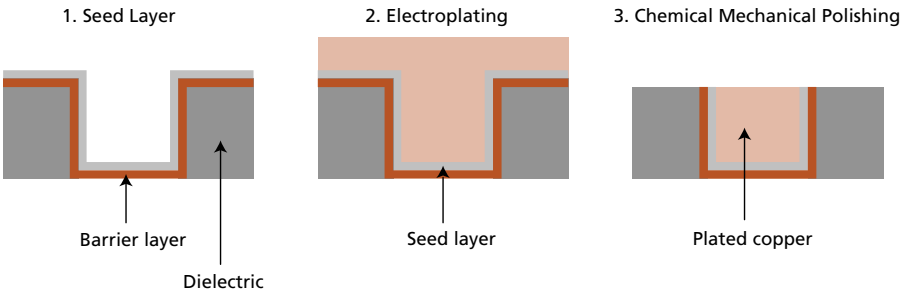

Figure 4 Damascene process steps

1. *First, a barrier layer such as Ta or TiN is deposited over the patterned dielectric to prevent interaction between the metal and the dielectric [10], since diffusion of the Cu into the Si would cause a deep level impurity that degrades device performance. The barrier layer is applied by ionized PVD (iPVD) or an ion metal plasma (IMP) process. A copper seed layer is applied over the barrier layer by PVD or iPVD, or sometimes CVD [1]. The use of iPVD for the seed layer results in increased step coverage of 10 to 15%, compared to 5 to 7% for PVD [11]. To put this in perspective, with 5% step coverage, you can have as little as 50 Å on the side walls of a trench in a 1000 Å process. Uniformity of seed layer is very important, since a poor seed layer can result in voids [11]. It is also important to ensure that the seed layer surface is free of oxides for efficient charge transfer during plating. This can be achieved by using thin (10 to 20 Å), acid-soluble oxide layers applied by PVD [12].*

2. *The pattern is then filled by electroplating, also called electrochemical deposition (ECD), which is discussed in more detail on page 7. Reliable ECD is highly dependent on the lithography, etch, barrier, and seed processes that precede ECD [11]. Rapid, uniform wetting of the wafer surface is required for good filling performance. Novellus® Systems features a zero current induction time, which is a time period after the wafer has entered the bath during which no significant deposition current is applied, allowing the wafer to be wetted. However, a small cathodic current is applied to prevent copper corrosion and cuprous oxide dissolution [12].*

3. *Chemical mechanical polishing (CMP) removes excess copper to planarize the wafer surface. CMP is a synergistic process that removes material through the physical grinding of a slurry containing abrasive particles such as silica, as well as through chemical action as a result of oxidizing agents such as hydrogen peroxide contained in the slurry [9]. The introduction of low permittivity (low-k) dielectrics has spurred many advances in CMP, since the low-k/Cu interface is not very robust [13, 14].*

Figure 5 shows the dual damascene process, which allows for copper deposition in interconnect and via to reduce the number of process steps required.

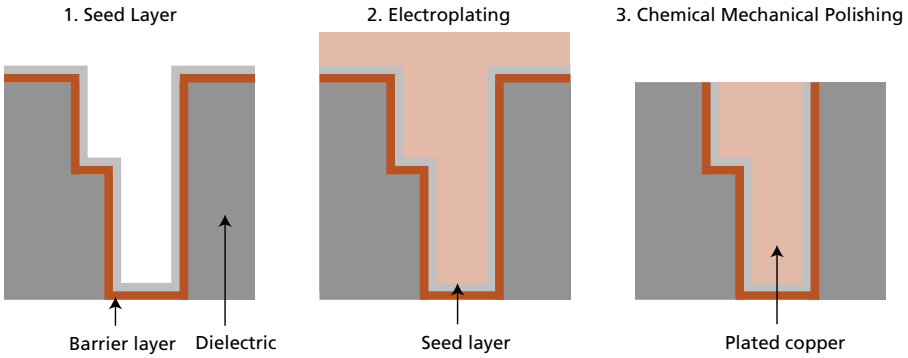

Figure 5 Dual damascene process steps

State of the Art in ECD

The use of copper interconnects was introduced at the 220 nm technology node in microprocessors [1], and the current state of the art can be derived from the manufacturers of ECD tools; for example, the Novellus SABRE® tool provides fill capability of aspect ratios of up to 10:1 at 130 nm technology with a throughput of 75 wafers per hour [5]. Applied Materials® recently replaced its ELECTRA CU® tool with SlimCell®, which features individual chemical baths for each cell. This tool is expected to be extendable beyond the 65 nm node [15]. The Semitool® Paragon® 300 tool can fill features as small as 80 nm at aspect ratios of 30:1 [16]. Several advanced chipmakers have announced breakthrough technologies down to 45 nm and aspect ratios of 30:1 on various tools.

Figure 6 shows a graphical representation of a single electroplating cell in a tool.

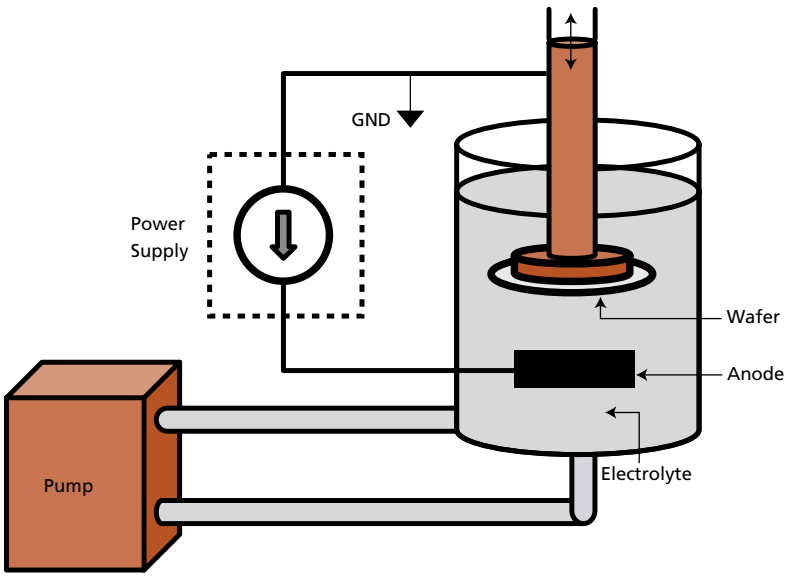

Figure 6 Diagram of an electroplating tool [5]

Electrochemical Deposition (ECD)

Basic Electrochemistry

The field of electrochemistry is defined as the study of phenomena caused by charge separation. In an electrochemical cell, the focus is on the charge transfer processes at the electrolyte/electrode interface [17], where the ions move from the electrolyte to the electrode.

Ions are divided into monatomic and polyatomic ions. Positively charged polyatomic ions are called cations, and negatively charged polyatomic ions are called anions. Cations and anions could be singly, doubly, or triply charged. Copper ions are monatomic, and a singly charged copper ion is called a cuprous ion, while a doubly charged copper ion is called a cupric ion [18].

The process of electrochemistry is the conversion between electrical and chemical energy, and these conversions take place in electrochemical cells. In a voltaic or galvanic cell, there is a spontaneous reaction converting chemical energy into electrical energy. In an electrolytic cell, electrical energy is converted to chemical energy, but this reaction is not spontaneous. There are two types of reactions in an electrochemical cell: oxidation and reduction (redox). In oxidation, electrons are lost; in a reduction, electrons are gained. Each combination of materials in an electrochemical cell has a unique cell potential (for example, 1.1 V for

Zn-Cu and 0.62 V for Zn-Sn). A single material is assigned a cell potential based on the voltage developed when combined with hydrogen (for example, 2.87 V for F and 1.36 V for Cl) [18].

An electrolyte is an electrically conductive solution of ionic compounds; for example, $CuSO_4$ in its solid form is made up of Cu^{2+} and SO_4^{2-} and held in place by electrostatic force. When dissolved, they dissociate ($CuSO_4(aq) \rightarrow Cu^{2+} + SO_4^{2-}$), leaving the ions free to move [19]. The bulk electrolyte is neutral since the charges cancel each other.

Basic ECD

When a conducting surface is immersed in a solution containing metal ions and this surface is electrically connected to a power supply that passes current through the surface to the solution, metal will be deposited on the surface. This is the ECD process. The barrier layer, although still conductive, has significantly higher resistivity than copper; therefore, a thin seed layer of copper is deposited over the entire wafer prior to the ECD process step [20]. A high resistivity metal layer will cause a significant voltage drop across the wafer, resulting in copper being deposited in island formations rather than uniformly [21]. The requirements for uniform copper deposition are discussed on page 11. A simple electrochemical cell is shown in Figure 7, and the associated electrode reactions are presented below [22].

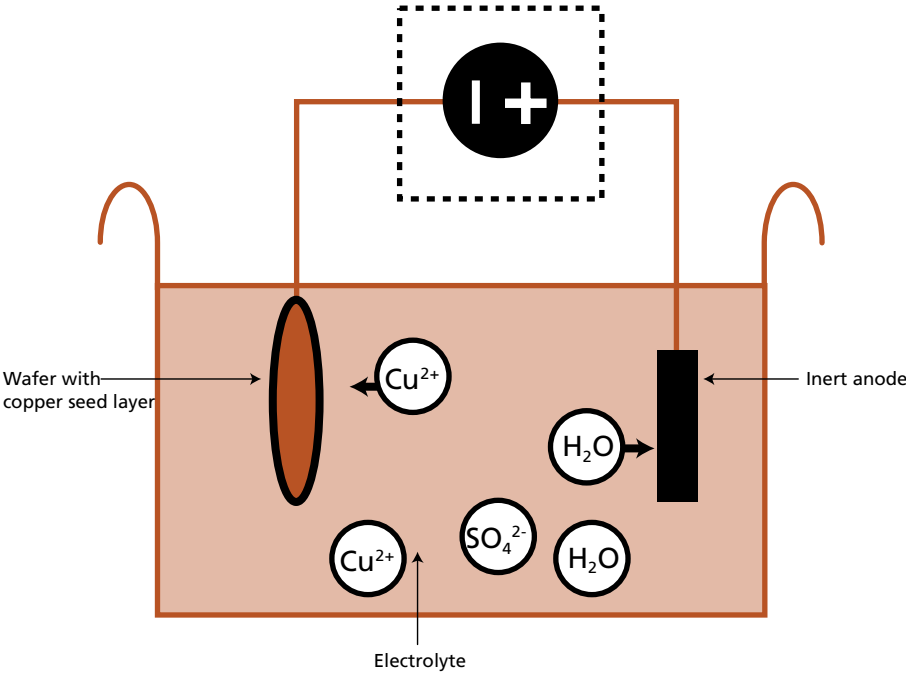

Figure 7 Copper electrochemical cell

The electrolyte is a copper sulfate solution:

$CuSO_4(aq) \rightarrow Cu^{2+} + SO_4^{2-}$

Where:
aq= Solution

At the cathode (wafer), either H_2O or Cu^{2+} could undergo reduction, depending on the reduction potential ε^0:

$Cu^{2+}(aq) + 2e^- \rightarrow Cu(s)$ $\varepsilon^0 = +0.32V$
$2H_2O + 2e^- \rightarrow H_2 + 2OH^-$ $\varepsilon^0 = -0.83V$

Where:
ε^0 = Reduction potential
s = Solid

Since the reduction potential for copper is more positive, it will more readily undergo reduction. Similarly, at the anode, either H_2O or SO_4^{2-} could undergo oxidation. The final redox reactions are:

At cathode (wafer surface)	$2Cu^{2+}(aq) + 4e^- \rightarrow 2Cu(s)$	reduction
At anode	$2H_2O(l) \rightarrow O_2(g) + 4H^+(aq) + 4e^-$	oxidation

Where:
l = Liquid
g = Gas

The cathode and anode reactions balance each other in order to maintain electrical neutrality in the solution. It is also possible to use a solid copper anode, as shown in Figure 8, in which case the cell and reactions are as follows [23]:

At cathode (wafer surface)	$Cu^{2+}(aq) + 2e^- \rightarrow Cu(s)$	reduction
At copper anode	$Cu(s) \rightarrow Cu^{2+}(aq) + 2e^-$	oxidation

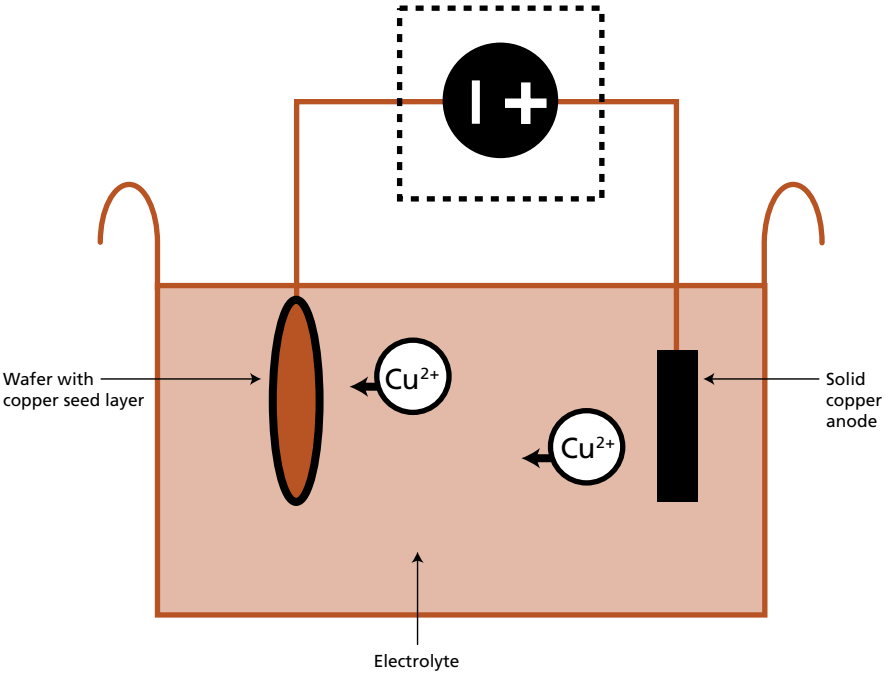

Figure 8 Electrochemical cell with solid copper anode

The mass of copper deposited on the wafer can be calculated by using Faraday's law for electroplating: the number of moles of products formed during electrolysis is proportional to the number of moles of electrons that pass through the cell [23]. For example, if 30 A of current is applied to the above copper electrochemical cell for one minute, the total number of moles of electrons is:

$$N_e = \frac{30A \times 60\ \text{sec}}{e \times N_A} = \frac{30A \times 60\ \text{sec}}{1.6 \times 10^{-19}\ C \times 6.023 \times 10^{23}} = 18.68 \times 10^{-3}\ moles$$

Where:
N_e = Number of moles of electrons
N_A = Avagadro's constant
e = Single electron charge

Since one copper atom is deposited for every two electrons that flow through the electrolyte, the number of moles of copper deposited is 9.34×10^{-3}, which is equal to a mass of:

$$M = \frac{N_e}{2} \times N_A \times m_{Cu} = 9.34 \times 10^{-3} \times 6.023 \times 10^{23} \times 63.55 \times 1.67 \times 10^{-27} kg \approx 0.6 \times 10^{-3} kg = 0.6g$$

Where:
M = Total mass of deposited copper
m_{Cu} = Molecular weight of copper

V-I Curves

A typical current-potential curve for the cathode/electrolyte interface in a copper electrochemical cell is shown in Figure 9, where the cathode is a wafer covered with a copper seed layer. The potential of the electrolyte with respect to the wafer, which is typically grounded, is plotted; since the electrolyte is electrically neutral, this is approximately equal to the potential of the anode with respect to the wafer (cathode).

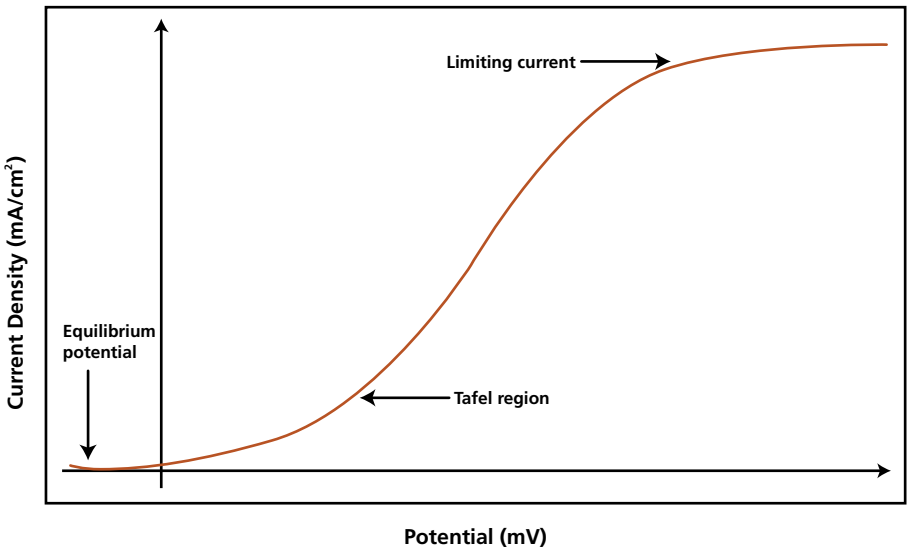

Figure 9 Typical V-I curve for electroplating

When there is zero current across the cathode/electrolyte interface, an equilibrium potential is exhibited. This equilibrium potential is established by the tendency of metals to dissolve in water, which produces positive ions that leave their valence electrons on the cathode, which, in turn, results in the cathode acquiring a negative potential with respect to the electrolyte. However, this tendency to dissolve is diminished, and may be reversed, by the presence of ions of the metal in the electrolyte. For copper, this happens at a cupric ion concentration of 5.5×10^{-9} mol.cm^{-3}; therefore, a copper electrode in a $CuSO_4$

solution will tend to accept cupric ions from the electrolyte, resulting in a slightly positive potential on the wafer (cathode) with respect to the electrolyte [24], that is, a negative electrolyte to cathode potential, as shown in Figure 9.

When the power supply applies a potential across the electrochemical cell, the current density is described by the Tafel law, which was formulated in 1905 based on empirical data [25]:

Tafel Law

$$\ln(J_c) = \ln(J_0) - \frac{n\alpha_c F\eta}{RT} = \ln(2k_0 F[Cu^{2+}]) - \frac{2\alpha_c F\eta}{RT}$$

Where:
J_c = Observed current density at cathode
J_0 = Exchange current density
n = Number of electrons required for reduction ($n = 2$ for Cu^{2+})
α_c = Cathodic transfer coefficient (tends to be approximately 0.5 for metals)
F = Faraday's constant
η = Applied potential
R = Gas constant
T = Temperature
k_0 = Standard rate constant
$[Cu^{2+}]_\infty$ = Concentration of cupric ions in the bulk electrolyte

It has since been corrected for transport effects, and the equation containing the corrections is shown below [17]:

$$\ln\left[\frac{1}{J_{L,c}} - \frac{1}{J}\right] = \ln(k_0) + \ln(2F[Cu^{2+}]) - \frac{2\alpha_c F(\eta - \varepsilon^0)}{RT}$$

Where:
$J_{L,c}$ = Diffusion limited cathodic current density (this value is measured at the equilibrium potential, shown in Figure 8), which is equal to:
$J_{L,c} = -2k_{d,O}F[Cu^{2+}]$

Where :
$k_{d,O}$=Mass transfer coefficient at the electrode surface
J = Observed current density
ε^0 = Standard electrode potential

The current density is limited by mass transfer effects, as shown in Figure 9, and processes generally operate at current densities no greater than 50% of the limiting current density [20].

Uniformity

Since the current density is dependent on the voltage applied, it is necessary to achieve uniform potential across the wafer in order to obtain uniform current density and copper thickness. Non-uniformities in potential can be modeled with a dimensionless distance x and a dimensionless overpotential ϕ [21]:

$$x = \frac{r}{r_1}$$

Where:
x = Dimensionless distance
r = Arbitrary radius
r_1 = The wafer radius.

$$\phi = \frac{\eta(r)}{\eta(r_1)}$$

Where:
ϕ = Dimensionless overpotential
$\eta(r)$ = The electrical potential at radius r
$\eta(r_1)$ = The electrical potential at radius r_1

The dimensionless over-potential is described by:

$$\frac{\partial^2\phi}{\partial x^2}+\frac{1}{x}\frac{\partial\phi}{\partial x}=\xi J^*$$

With the following boundary conditions:
$\partial\phi/\partial x = 0$ at $x = 0$ and $\phi = \phi_1$ at $x = 1$

Where:
J^* = The dimensionless plating current density

$$J^*=\frac{J}{J_0}$$

ξ = A dimensionless polarization parameter

$$\xi=\frac{J_0\rho r_1^2\alpha_c F}{hRT}$$

Where:
h = Thickness of the metal film
ρ = Resistivity of the metal film

The non-uniformity of the rate at which copper is electrodeposited onto the metal film is proportional to the dimensionless parameter $\xi J^*/4\phi_1$. If $\xi J^*/4\phi_1 >> 1$; the deposition rate close to the contacts at the edge of the wafer will be much higher than at the center of the wafer. It can be seen that a thin film (small h) of a metal with a high resistivity will increase ξ and therefore result in an increase in non-uniformity of deposition rate. The dimensionless plating rate $J(x)/J(x = 1)$ is shown as a function of ξ in Figure 10.

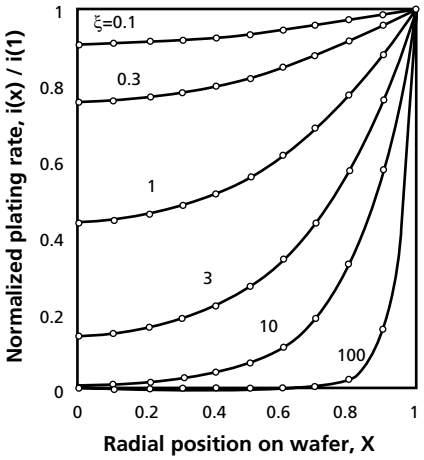

Figure 10 Plating rate as a function of ξ [21]

In a conventional bath for a 200 mm wafer with a 500 Å Ta barrier film and 1000 Å copper seed layer, $\xi \cong 1$, which results in a plating rate at the center of the wafer of approximately 45% of that at the edge of the wafer initially. However, as the copper layer becomes thicker, ξ diminishes, and the plating rate becomes more uniform. It has been suggested that copper can be deposited onto seedless barrier films [21]. However, if no copper seed layer is present, $\xi \cong 50$, and the plating rate at the center of the wafer of five orders of magnitude lower than at the edge of the wafer, and, in this case, there is not sufficient build-up of copper in the center of the wafer to reduce ξ.

In order to accomplish copper plating directly onto a barrier layer, ξ needs to be lowered, and the only practical way to achieve that is to lower the exchange current density J_0, which is proportional to the cupric ion density and a rate constant k and depends strongly on additives. It would be necessary to lower the cupric ion density from its conventional levels of 1 M to the order of 10 mM initially; then the plating rate can be increased proportionally to the thickness of the copper layer [21]. However, it has been observed that for a given additive system, too low a copper concentration diminishes superfilling attributes [12], and therefore more investigation is required into this proposed deposition system.

Boundary Layer

The cathode/electrolyte interface is also referred to as a boundary layer [10], diffusion layer [17], or interfacial region. Most of the potential difference established by the power supply between the anode and cathode is dropped across this layer since the bulk electrolyte is electrically neutral, as shown in Figure 11. This is similar to a sheath in a gas plasma.

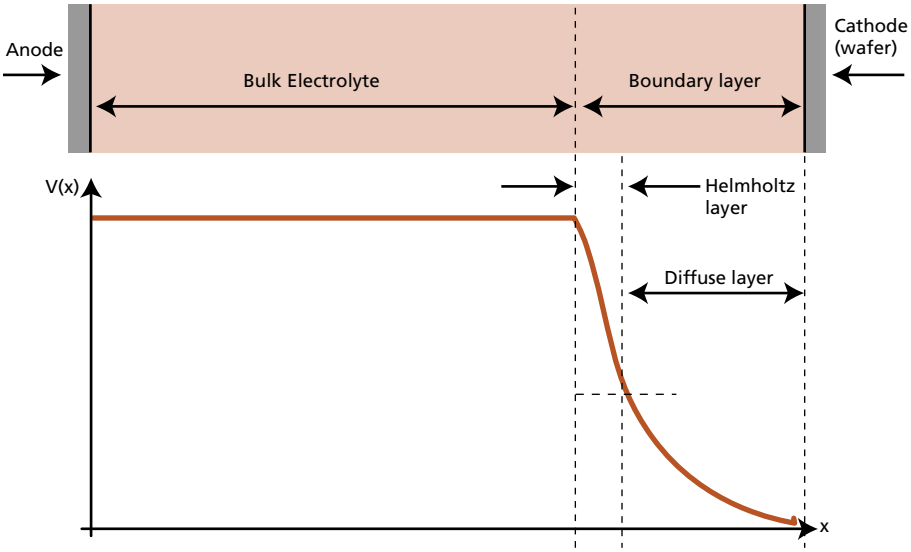

Figure 11 Voltage as a function of distance from anode with wafer grounded [26]

The charge separation across the boundary layer looks like a capacitor with typical capacitance values of 10 µF/cm² to 100 µF/cm², resulting in 700 nF to 7 µF of capacitance for a 300 mm wafer [17]. The boundary layer is further subdivided into the outer Helmholtz layer and the inner diffuse, or Gouy, layer where each region has a separate equivalent capacitor associated with it. The potential is linear in the Helmholtz layer, and the equivalent capacitance for this layer is independent of the concentration. In the diffuse layer, the equivalent capacitance is a function of the concentration with a higher concentration resulting in a higher capacitance, and the potential varies exponentially in this region [26], as shown in Figure 11.

Conductivity

The current-potential relationship is not linear, and therefore the conductivity of the cell can only be calculated within a potential range where a linear current-potential relationship can be assumed. Conductivity κ is a material property and is the inverse of resistivity:

$$K = \frac{1}{\rho}$$

Where:
κ = Conductivity

With this definition, Equation 1 (see page 2), which provides the resistance of a solid conductor, can be re-written as:

$$R = \frac{\rho L}{WT} = \frac{L}{WT} \times \frac{1}{K}$$

Where:
L = Length of the conductor
W = Width of the conductor
T = The thickness of the conductor

If we define the cell constant χ as:

$$\chi = \frac{L}{WT}$$

Then [24],

$$R = \chi \times \frac{1}{K}$$

$$\therefore K = \frac{\chi}{R}$$

The conductivity can therefore be calculated if the resistance and the cell constant are known. The resistance R is determined by applying a voltage across the conductor and measuring the current.

Therefore:

$$R = \frac{V_{applied}}{I_{measured}}$$

It is difficult to calculate the cell constant χ of an electrochemical cell since the conductance path is not normal to the electrodes. It can be determined by calibration against a solution of known conductivity.

The molar conductivity Λ_c [$m^2\Omega^{-1}mol^{-1}$] of the electrolyte is defined as:

$$\Lambda_c = \frac{K}{c}$$

Where c is the concentration.

The molar conductivity in strong electrolytes decreases with an increase in concentration since the interactions between cations and anions increase [24]:

$$\Lambda_c = \Lambda_0 - \sqrt{c}$$

$$\forall\Lambda_0 = \lim_{c\to 0} \frac{K}{c}$$

Bath Chemistry and Plating Waveforms

The combination and relative concentrations of additives to the bath, as well as the plating currents used, have a profound impact on the fill characteristics [28]. Conventional electroplating baths are formulated using a highly stable base electrolyte containing copper sulfate, in concentrations of 75 to 210 g/L [27], and sulfuric acid. Typical cupric ion concentrations range from 17 to 60 g/L. Sulfuric acid is added in concentrations of 45 to 325 g/L to increase electrolyte conductivity and improve wetting. More conductive electrolytes result in a system where plating thickness distribution is less dependent on the plating cell geometry, while low acid electrolytes result in a system with less dependence on seed layer resistivity [12]. Several additives, which are neutral, are also added to the electrolyte in order to improve the copper deposition rate and/or material properties of the deposited copper.

Additives can dramatically change the fill evolution of the trench. A combination of three types of organic additives is added to the electrolyte: accelerators, suppressors, and levelers [12].

- *Accelerators are molecules that contain pendant sulfur atoms (for example mercaptan [9]) that locally accelerate current at a given voltage where they adsorb. Accelerators are added in a concentration range of 1 to 25 ppm.*
- *Suppressors (also called inhibiting agents [9]) are polymers, such as polyethylene glycol, which form a current-suppressing film on the entire wafer, especially in the presence of chloride ions. Suppressors are added in high concentrations of 200 to 2000 ppm; therefore, their distribution across the wafer is not strongly dependent on their rate of mass transfer or diffusion to the surface.*
- *Levelers are also current-suppressing molecules added at a low concentration, and therefore their concentration at the wafer is mass-transfer dependent. This means that isolated locations, such as the inside of a via where mass transfer is limited, are less suppressed while corners are more suppressed where mass transfer is more efficient.*

It is also instructive to note that the additives by themselves have a relatively minor influence on the deposition, but, together, they have a synergistic effect [11]. There are three transport mechanisms to consider that could impact deposition of additives: diffusion, migration, and convection.

Diffusion is due to a concentration gradient. Migration is due to an electric field gradient, and, since additives are electrically neutral, they are not influenced by migration. Convection is due to fluid movement. This does not usually occur within the boundary layer and does not affect deposition. Thus, diffusion is the primary transport mechanism of neutral additives to the cathode (wafer). The concentration gradient is produced by the consumption of additives at the surface [17].

However, a hydrodynamic electrode is oftentimes employed, which can be implemented by either a moving electrode or a moving electrolyte. This imposes controlled convection which defines the mass transport of electrolyte towards the electrode to result in a thinner boundary layer, which, in turn, enhances the response at the electrode and also influences the limiting current. The flow is usually laminar rather than turbulent for a moving cathode, as shown in Figure 12.

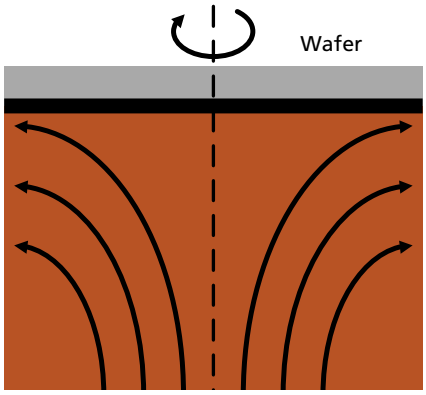

Figure 12 Laminar flow established across wafer with moving cathode

The cathodic pulse frequency and current density also impact the fill characteristics, and good superfilling performance has been reported with current densities of 13 to 22 mA/cm^2, which translates to 4 to 7 A for a 200 mm wafer [11]; but higher current densities are necessary to improve throughput, and additive packages have been developed to support higher current densities.

Superfilling

Superfilling refers to the effect where higher deposition rates are achieved in the bottom of trenches than on the sides, as illustrated in Figure 13. It provides void-free and seamless deposits inside trenches with high aspect ratios, and extensibility of this technology down to 65 nm trenches has been demonstrated.

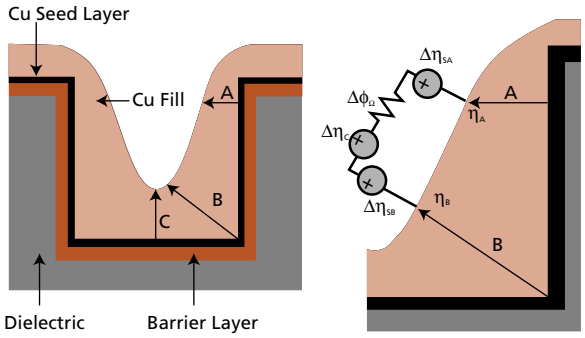

Figure 13 Diagrams showing superfilling phenomenon

The difference in deposition rates between points A (close to surface of wafer) and B (deep in trench) can be understood by considering the potential between these points. The total potential difference is zero since the solid copper electrically shorts the two points:

$$\Delta\eta = \eta_A - \eta_B = 0 = -\Delta\eta_{SA} + \Delta\phi_\Omega + \Delta\eta_C + \Delta\eta_{SB}$$

Where:

η_A and η_B = The electrical potentials at points A and B

$\Delta\eta_{SA}$ and $\Delta\eta_{SB}$ = The surface potentials at points A and B

$\Delta\eta_C$ = Concentration potential

$\Delta\phi_\Omega$ = The ohmic potential drop in the electrolyte

Since the distance between the two points is less than a micron, the ohmic potential drop is negligible—on the order of 1 μV (that is, $\Delta\phi_\Omega \cong 0$). On the same basis, it can also be assumed that the concentration potential is negligible (that is, $\Delta\eta_C \cong 0$) since the short distance will also result in a negligible difference in cupric ion (Cu^{2+}) concentration. As the aspect ratio increases, this assumption will no longer be valid. These simplifications result in:

$$-\Delta\eta_{SA}+\Delta\eta_{SB}=0$$

$$\therefore \Delta\eta_{SA}=\Delta\eta_{SB}$$

By writing the surface potentials in the form of a Tafel expression:

$$\ln(J^A)-\ln(J_0^A)=\ln\left(\frac{J^A}{J_0^A}\right)=-\frac{2\alpha_c F\Delta\eta_{SA}}{RT}$$

$$\therefore \Delta\eta_{SA}=\frac{RT}{2\alpha_c F}\ln\left(\frac{J^A}{J_0^A}\right)$$

Now we can write:

$$\frac{RT}{2\alpha_c F}\ln\left(\frac{J^A}{J_0^A}\right)=\frac{RT}{2\alpha_c F}\ln\left(\frac{J^B}{J_0^B}\right)$$

$$\therefore \frac{J^A}{J_0^A}=\frac{J^B}{J_0^B}$$

Point A has a higher flux of additives, including levelers, which are mass transfer dependent, since point A is closer to the surface of the wafer, resulting in a lower exchange current density J_0^A. Since $J_0^A<J_0^B$, it follows that $J^A<J^B$, and therefore copper will be deposited at point B at a higher rate than at point A [8]. (See Andricacos et al., for a rigorous numerical model [10].)

Morphology

The desired grain morphology of the deposited copper is a *bamboo* type grain morphology, where the size of the grains are larger than the width of the device features in order to improve resistance to electromigration. The grain size of the deposited copper is inversely proportional to the current density; that is, higher current density results in smaller grain size, but high current density is desirable for high throughput. The texture of the seed layer also exhibits a large influence on the grain size. The texture is measured as the percentage of x-ray diffraction reflection, and larger grain size results in a higher percentage reflection [27].

The right combinations of additives to the electrolyte also allow the copper deposits to undergo room temperature annealing, a process during which the copper grains grow, decreasing the resistance [9]. Over a period of 3 to 200 days, up to 20% reduction in resistivity has been observed. Annealing does not occur for additive-free depositions. The annealing also results in an increase of crystallinity and alignment of grains in a copper film, but these effects are not observed within the features; therefore, the copper is still polycrystalline in the actual device features [27]. Some ECD tools include annealing chambers [15].

A Look to the Future

The technology roadmap for 2002 predicted that ECD of copper could be extended to 65 nm but that simultaneous development of alternative filling techniques such as CVD, CVD/PVD fill, or high-pressure flow are necessary for small, high aspect ratio features. Alternative conductors may also be explored, including superconducting materials, if the chip temperature can be reduced [1]. Atomic layer deposition (ALD) may be used to deposit the barrier layer and copper seed layer [29].

Historically, the use of additives has been a form of art, not science, and it is imperative for future developers to understand the fundamental physics of plating [11].

Other areas of improvement are the environmental, safety, and health challenges, including developing methods for treating and recycling ECD baths and appropriate abatement, reducing generation and handling of hazardous waste, and reducing employee exposure to chemicals (acidic electrolytes) [1].

The reliability of copper interconnects with low-k dielectrics needs to be improved and much work is being done in this area [30, 31].

Other applications of electroplating in the semiconductor manufacturing process on the horizon include controlled collapse chip connection (C4), which involves chip connection to a substrate that contains power and signal connections, and multi-chip module packages, which require increased thickness of 5 to 10 µm for internal package wiring needs [10].

References

[1] Semiconductor Industry Association, *International Technology Roadmap for Semiconductors: 1999 Edition*, Austin, TX: International SEMATECH, 1999, pp. 163-186.

[2] H. Sanchez, "Design implications of low-k," in *Proceedings of the IEEE 2003 International Interconnect Technology Conference*, 2003, pp. 3-5.

[3] Semiconductor Industry Association, *International Technology Roadmap for Semiconductors: 2002 Update*, Austin, TX: International SEMATECH, 2002.

[4] R. A. Powell, A. S. Harrus, R. Hill, "Raising the IC speed limit by the use of copper interconnects," Novellus Systems, Inc., 2000, http://www.novellus.com/damascus/tec/tec_15.asp.

[5] Novellus Systems, "Step 10 Cu electrofill," Novellus Systems, Inc., 2000, http://www.novellus.com/damascus/tsd/tsd_10.asp.

[6] R. Liu, C. Pai, H. Cong, W. Lai, E. Martinez, "Impact of interconnect architecture on chip size and die yield," in *Proceedings of the IEEE 1999 International Interconnect Technology Conference*, 1999, pp. 21-23.

[7] C. Cregut, G. Le Carval, J. Chilo, "High-frequency simulation and characterization of advanced copper interconnects," in *Proceedings of the IEEE 1999 International Interconnect Technology Conference*, 1999, pp. 221-223.

[8] P.C. Andricacos, "Copper on-chip interconnections, a breakthrough in electrodeposition to make better chips," *The Electrochemical Society Interface* (spring 1999), pp. 32-37.

[9] S.Campbell, "The science and engineering of microelectronic fabricaiton," 2nd Ed. Oxford University Press, 2001.

[10] P. C. Andricacos, C. Uzoh, J.O. Dukovic, J. Horkans, H. Deligianni, "Damascene copper electroplating for chip interconnections," *IBM Journal of Research and Development* 42, no. 5, pp. 567-574.

[11] R.D. Mikkola, Q-T. Jiang, R. Carpio, B. Carpenter, "Bath additive and current density effects on copper electroplating fill of copper damascene structures," *Material Research Proceedings: Polycrystalline Metal and Magnetic Thin Films* 562, pp.243-248.

[12] J. Reid, S. Mayer, E. Broadbent, E. Klawuhn, K. Ashtiani, "Factors influencing damascene feature fill using copper PVD and electroplating," *Solid State Technology* (July 2000), pp. 86-98.

[13] J. Pallinti, S. Lakshminarayanan, W. Barth, P. Wright, M. Lu, S. Reder, L. Kwak, W. Catabay, D. Wang, F. Ho, "An overview of stress free polishing of Cu with ultra low-k (k<2.0) films," in *Proceedings of the IEEE 2003 International Interconnect Technology Conference*, 2003, pp. 83-85.

[14] S. Kondo, S. Tokitoh, B.U. Yoon, A. Namiki, A. Sone, N. Ohashi, K. Misawa, S. Sone, H.J. Shin, T. Yoshie, K. Yoneda, M. Shimada, S. Ogawa, I. Matsumoto, N. Kobayashi, "Low-pressure CMP for reliable porous low-k/Cu integration," in *Proceedings of the IEEE 2003 International Interconnect Technology Conference*, 2003, pp. 86-8.

[15] Applied Materials, "Copper electrochemical plating," Applied Materials, Inc., http://www.appliedmaterials.com/products/copper_interconnect.html.

[16] Semitool, "Electrochemical deposition," Semitool, Inc., http://www.semitool.com/lt308.html.

[17] C.M.A. Brett and A.M.O. Brett, *Electroanalysis*, Oxford: Oxford Science Publications, 1998.

[18] T.R. Dickson, *Introduction to Chemistry*, 8th ed., New York: John Wiley and Sons, 1999.

[19] J.E. Brady and G.E Humiston, *General Chemistry*, 4th ed., New York: John Wiley and Sons, 1986.

[20] J. D. Reid, "Fundamentals of copper," Novellus Systems, Inc., 2000, http://www.novellus.com/damascus/foc/foc_e.asp.

[21] K. M. Takahashi, "Overcoming sheet resistance effects to enable electro-plating of copper onto seedless barrier films," in *Proceedings of the IEEE 1999 International Interconnect Technology Conference*, 1999, pp. 281-3.

[22] D. Wolfe, *College Chemistry*, New York: HarperCollins Publishers, 1993.

[23] M. Ladd, *Introduction to Physical Chemistry*, 3rd ed., Cambridge: Cambridge University Press, 1998, p. 379.

[24] M. Ladd, *Introduction to Physical Chemistry*, 3rd ed., Cambridge: Cambridge University Press, 1998.

[25] E. Katz, "Biosensors and Bioelectronics," Hebrew University, http://chem.ch.huji.ac.il/~eugeniik/tafel_equation.htm.

[26] J. Wang, *Analytical Electrochemistry*, New York: VCH Publishers, 1994.

[27] S. Grunow, D. Diatezua, S-C. Seo, T. Stoner, A.E. Kaloyeros, "Study of electrochemical deposition of copper and microstructure evolution in fine lines," *Material Research Proceedings: Polycrystalline Metal and Magnetic Thin Films* 562, pp.243-246.

[28] J. Reid, V. Bhaskaran, R. Contolini, E. Patton, R. Jackson, E. Broadbent, T. Walsh, S. Mayer, R. Schetty, J. Martin, M. Toben, S. Menard, "Optimization of damascene feature fill for copper electroplating process," Novellus Systems, 2000, http://www.novellus.com/damascus/tec/tec_14.asp.

[29] K.I. Choi, B. H. Kim, S. W. Lee, J. M. Lee, "Characteristics of ALD-TaN thin films using a novel precursors for copper metallization," in *Proceedings of the IEEE 2003 International Interconnect Technology Conference*, 2003, pp. 129-131.

[30] A.H. Fischer, A. von Glasow, S. Penka, F. Ungar, "Process optimization—the key to obtain highly reliable Cu interconnects," in *Proceedings of the IEEE 2003 International Interconnect Technology Conference*, 2003, pp. 253-255.

[31] S. Matsumoto, A. Ishii, K. Tomita, K. Hashimoto, Y. Nishioka, M. Sekiguchi, A. Iwasaki, S. Isono, T. Satake, G. Okazaki, M. Fujisawa, M. Matsumoto, S. Yamamoto, M. Matsuura, "Reliability improvement of 90 nm-node Cu/low-k interconnects," in *Proceedings of the IEEE 2003 International Interconnect Technology Conference*, 2003, pp. 262-264.

ADVANCED ENERGY®

Advanced Energy Industries, Inc. • 1625 Sharp Point Drive • Fort Collins, Colorado 80525
T: 800.446.9167 or 970.221.4670 • F: 970.221.5583 • support@aei.com • www.advanced-energy.com

United Kingdom
T: 44.1869.320022
F: 44.1869.325004

Germany
T: 49.711.779270
F: 49.711.7778700

Korea
T: 82.31.622.0555
F: 82.31.622.0556

Japan
T: 81.3.32351511
F: 81.3.32353580

Taiwan
T: 886.2.82215599
F: 886.2.82215050

China
T: 86.21.5857.9011
F: 86.21.5857.9003