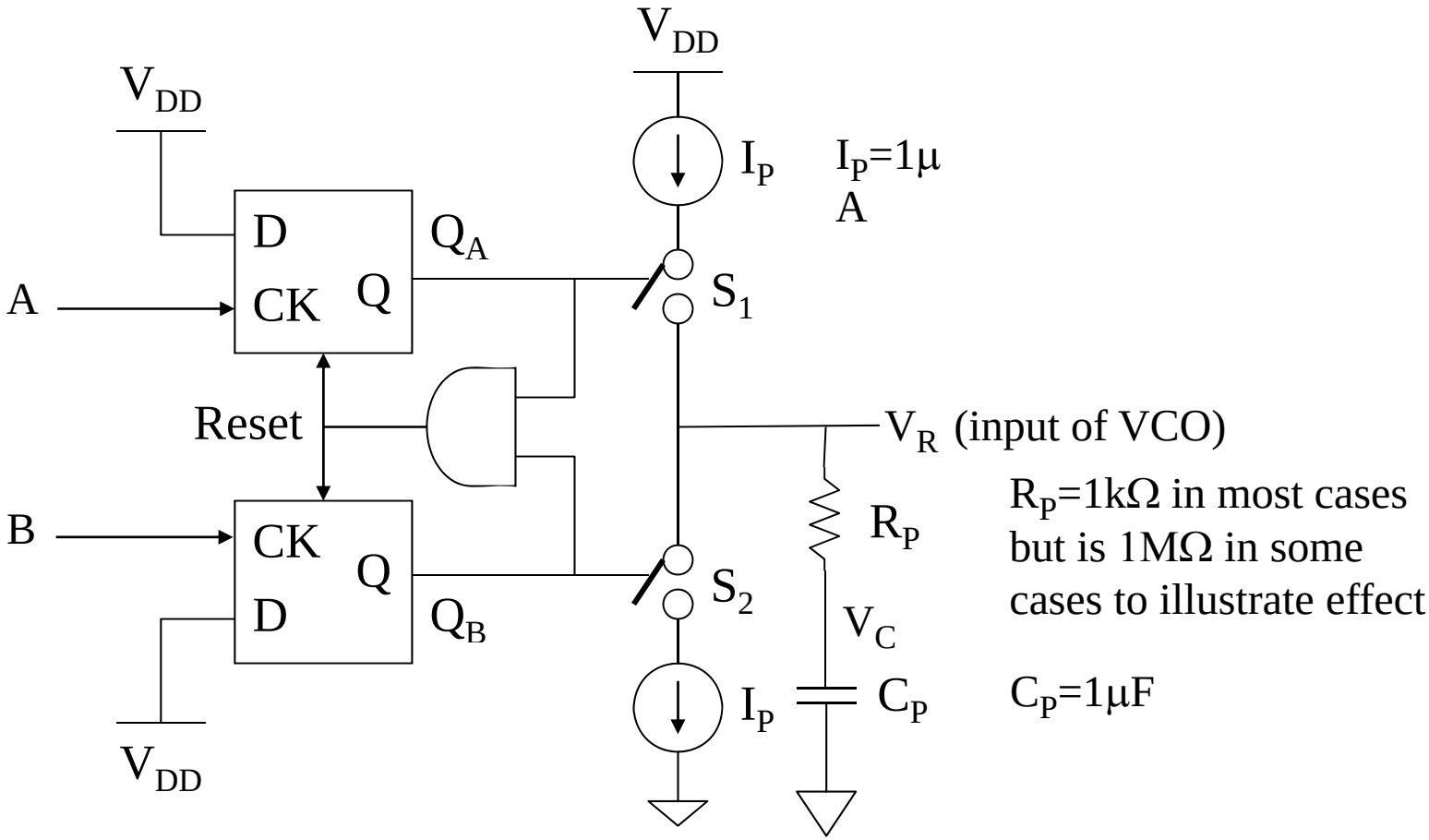
EE4011: RF IC Design
Sample Response of Type II PLL

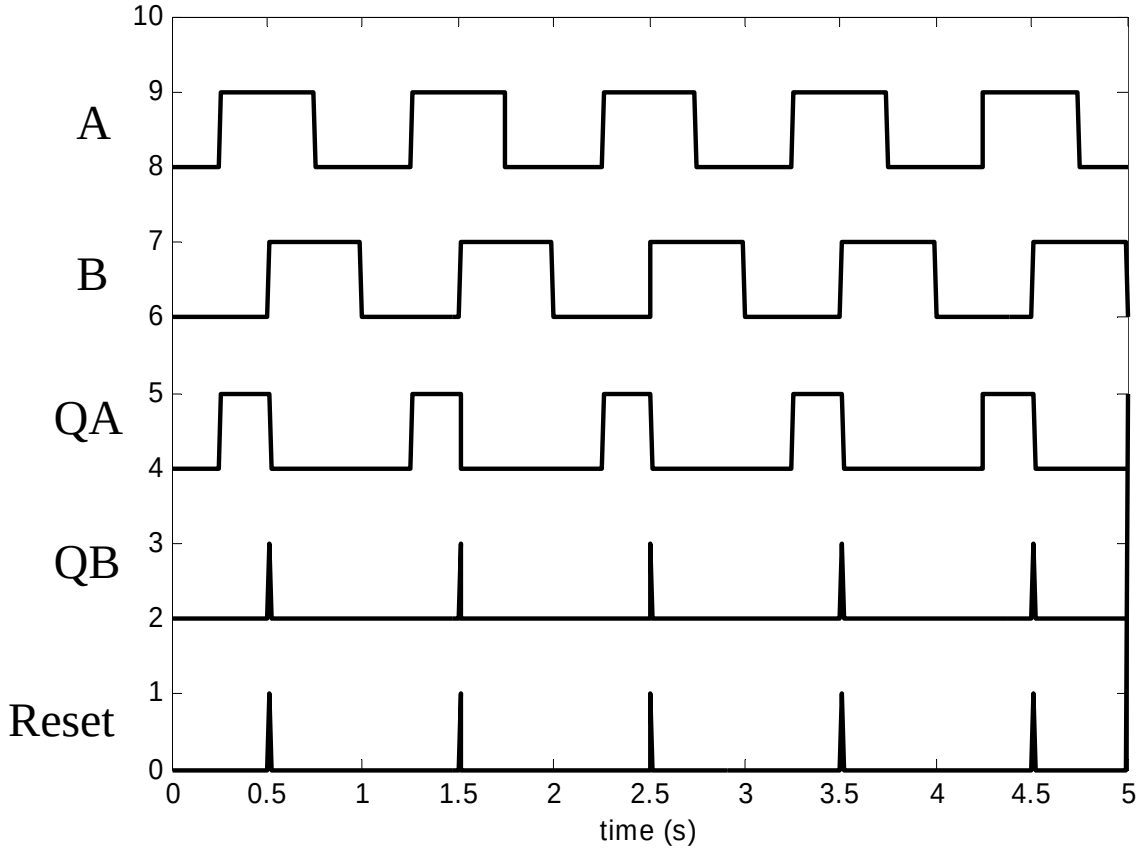
Sample Open-Loop Waveforms



A and B are square waves (digital 0 or 1) with different phase offsets and/or frequencies.
A and B are independent waveforms for these open-loop examples and there is no feedback.

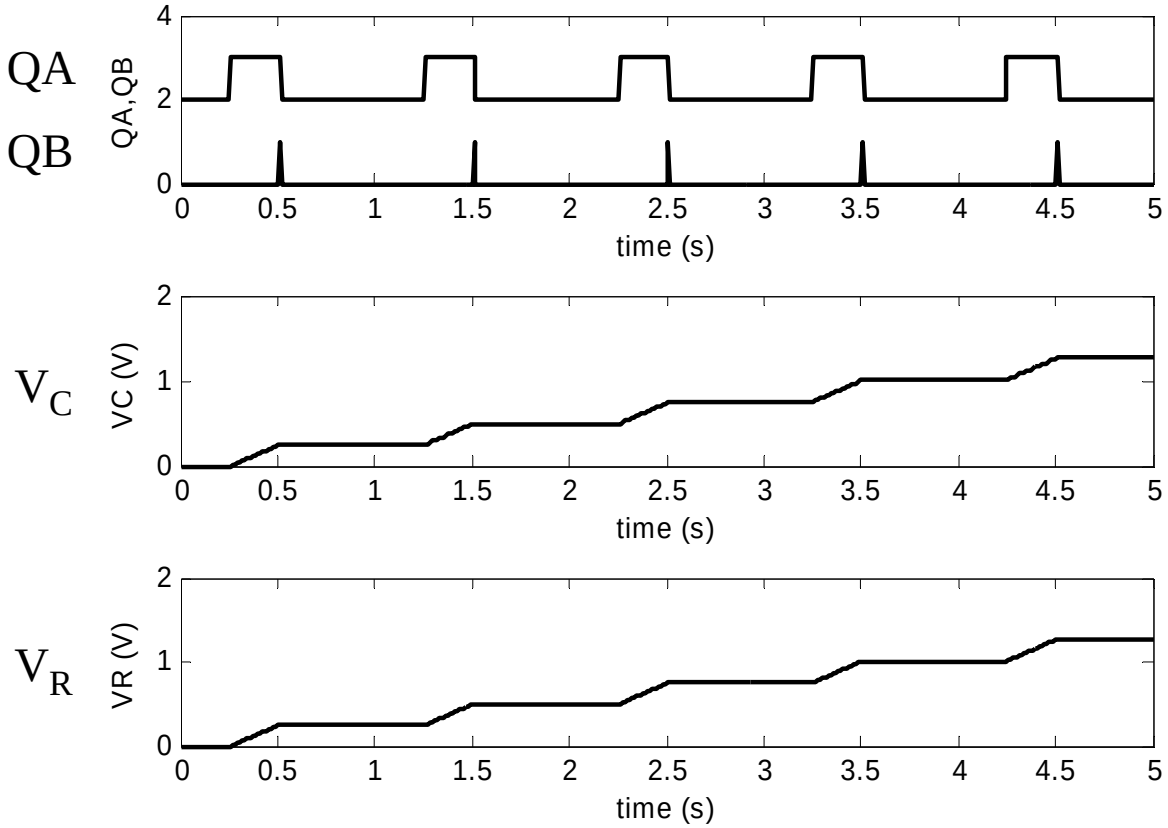
A, B have the same frequency but A is π/2 ahead of B

General behaviour: QA goes high following a rising edge of A, if it isn't high already
QB goes high following a rising edge of B, if it isn't high already
Reset goes high when both QA and QB are high and resets QA and QB



Here A and B are the same frequency but A leads B by a phase difference of π/2. As a result the logic level QA is high for a much greater time than logic level QB.

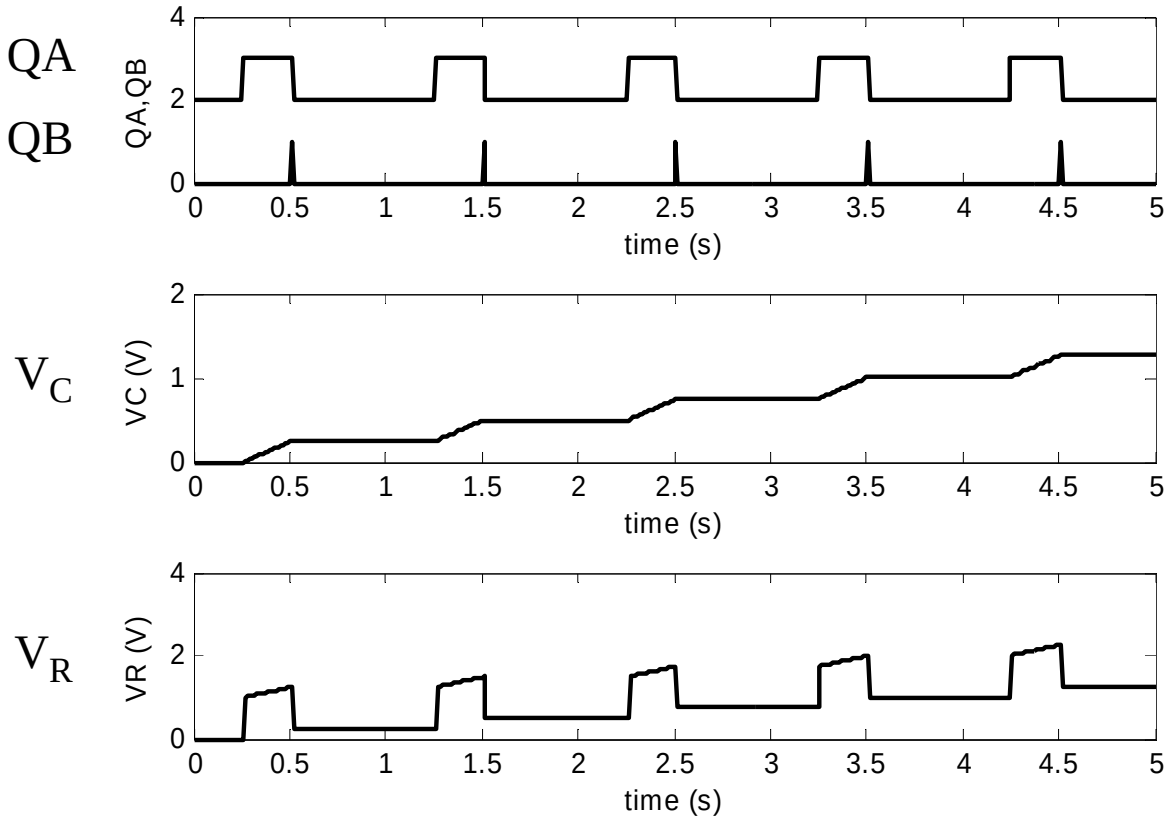
A, B have the same frequency but A is $\pi/2$ ahead of B



General behaviour: When QA is high the capacitor is charged
When QB is high the capacitor is discharged
When QA and QB are low the capacitor holds its voltage
In this example R=1kΩ and I_P=1μA so the IR drop across the resistor is not noticeable
The capacitor is gradually charging up because A leads B

A, B have the same frequency but A is $\pi/2$ ahead of B

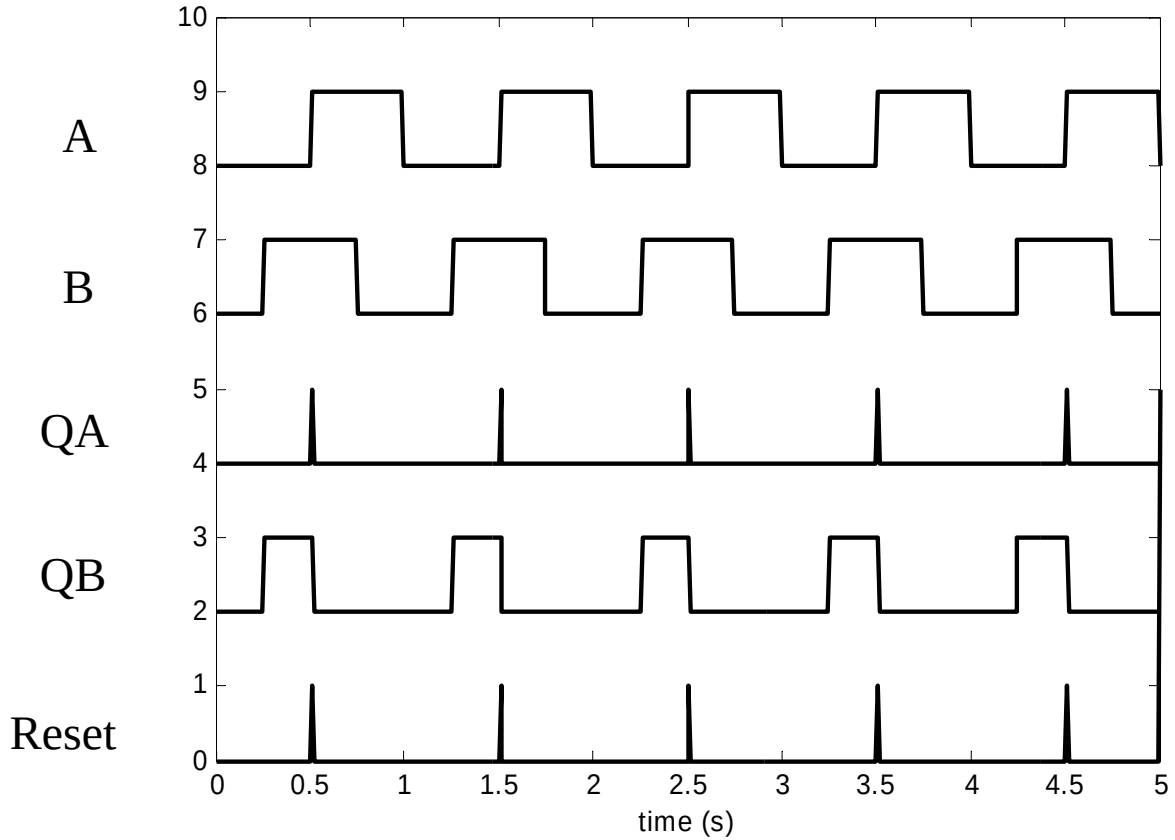
Case for R=1MΩ



General behaviour: When QA is high the capacitor is charged
When QB is high the capacitor is discharged
When QA and QB are low the capacitor holds its voltage
In this example R=1MΩ and I_P=1μA so the IR drop across the resistor is VERY noticeable

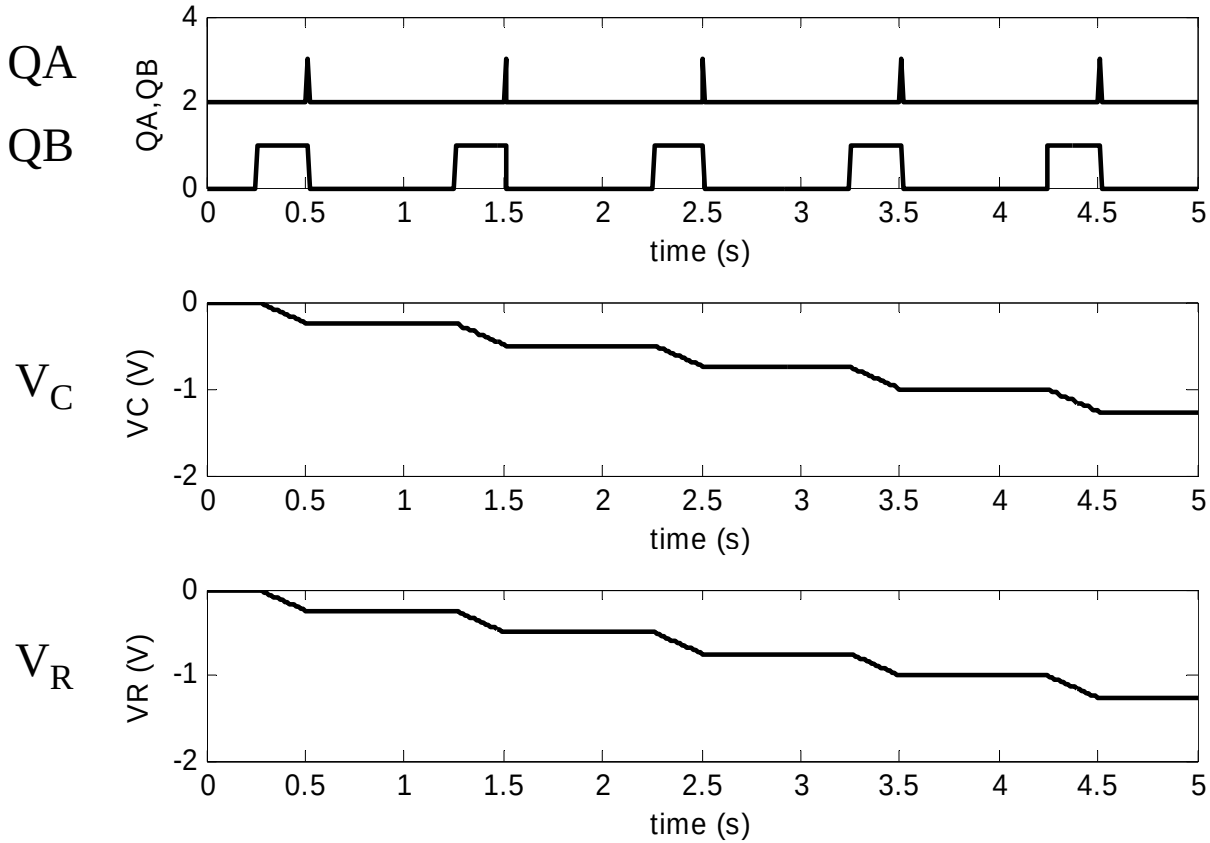
A, B have the same frequency but B is π/2 ahead of A

General behaviour: QA goes high following a rising edge of A, if it isn't high already
QB goes high following a rising edge of B, if it isn't high already
Reset goes high when both QA and QB are high and resets QA and QB



Here A and B are the same frequency but B leads A by a phase difference of π/2. As a result the logic level QB is high for a much greater time than logic level QA.

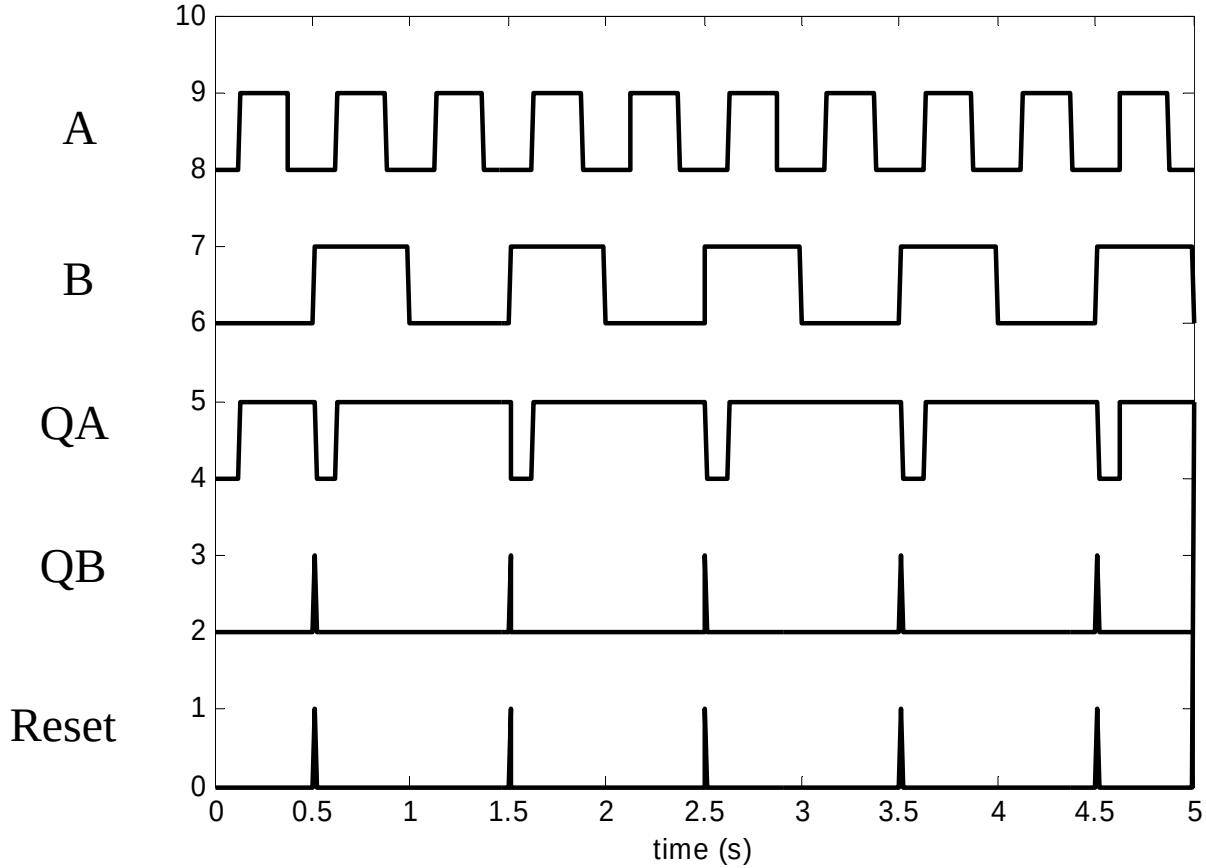
A, B have the same frequency but B is $\pi/2$ ahead of A



General behaviour: When QA is high the capacitor is charged
When QB is high the capacitor is discharged
When QA and QB are low the capacitor holds its voltage
In this example R=1kΩ and I_P=1μA so the IR drop across the resistor is not noticeable
The capacitor which started at 0V is being discharged because B leads A. The capacitor voltage is thus going negative in this case.

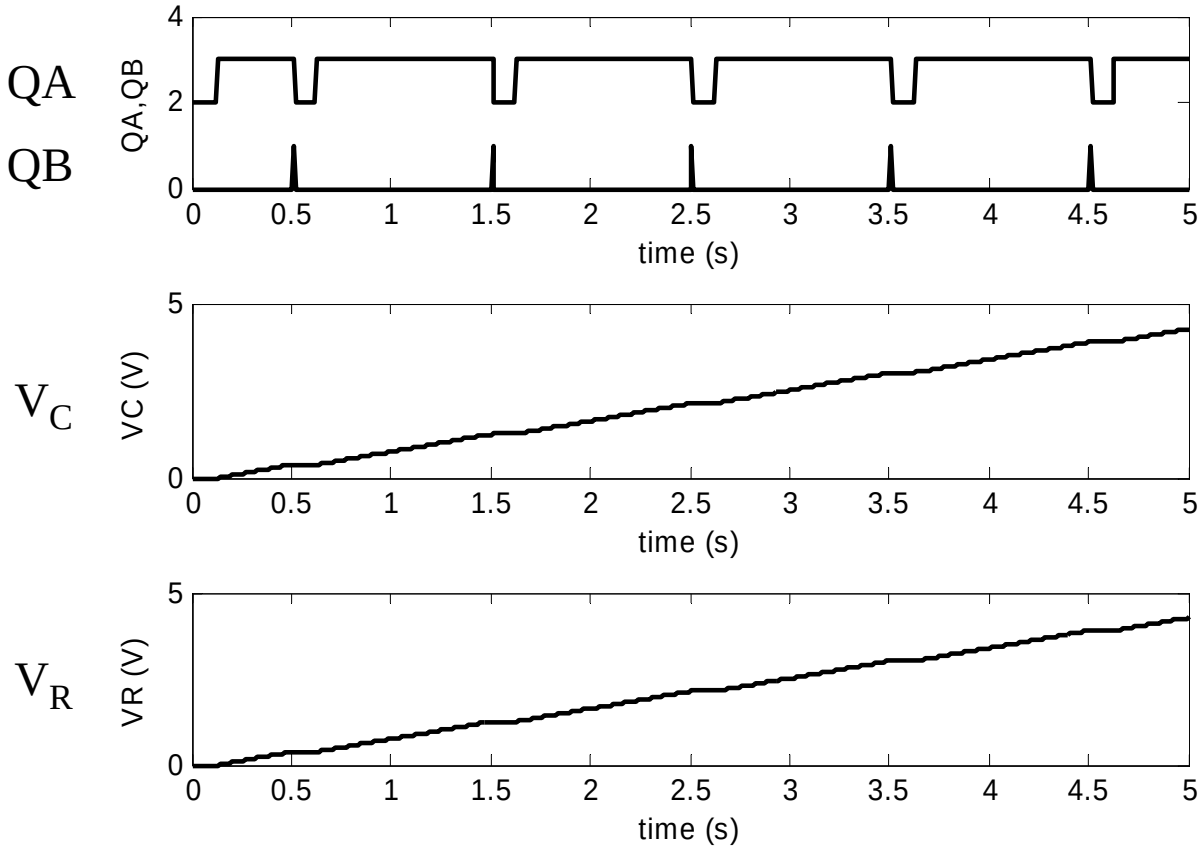
A is twice the frequency of B

General behaviour: QA goes high following a rising edge of A, if it isn't high already
QB goes high following a rising edge of B, if it isn't high already
Reset goes high when both QA and QB are high and resets QA and QB



A is twice the frequency of B and as a result QA is high nearly all the time.
(There is also a phase difference between A and B here just to separate the rising and falling edges of QA and QB for clarity.)

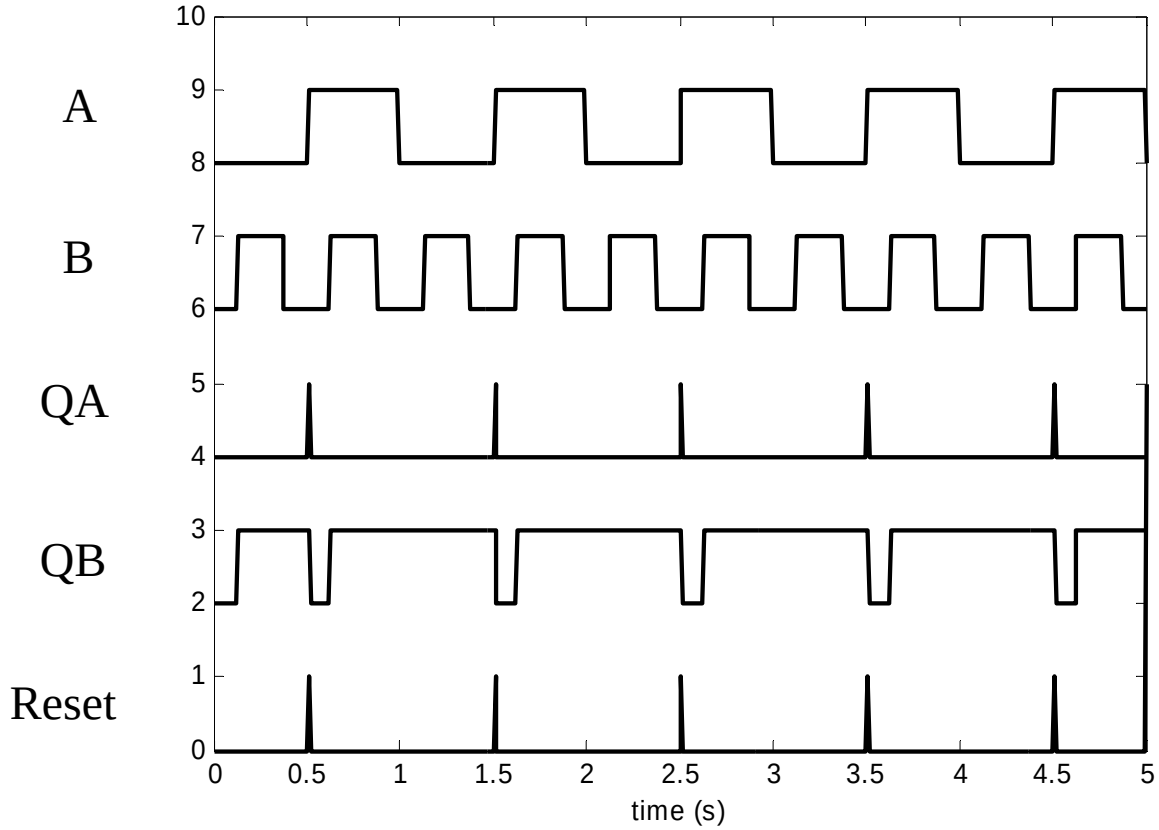
A is twice the frequency of B



General behaviour: Because QA is high most of the time, the capacitor is charging most of the time so its waveform looks like a linearly rising voltage (but there are flat regions when QA is 0).

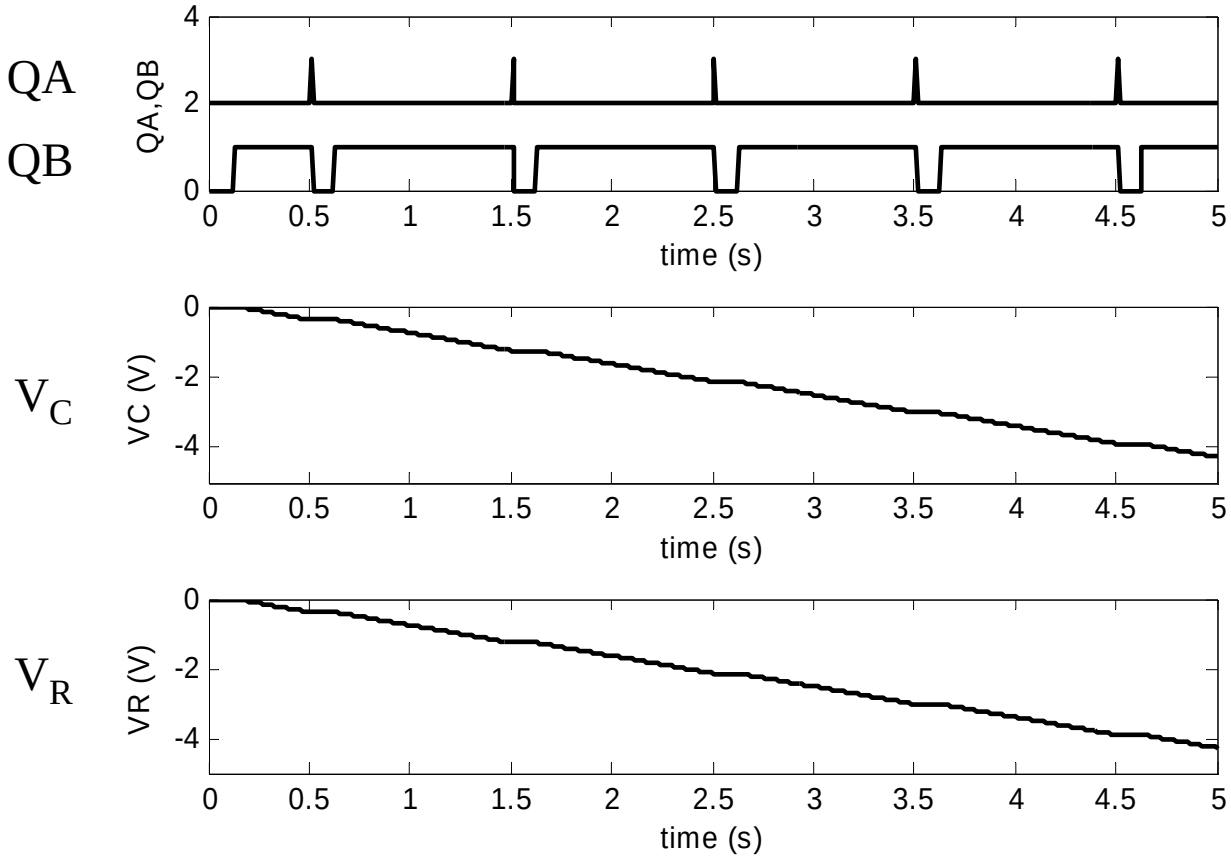
B is twice the frequency of A

General behaviour: QA goes high following a rising edge of A, if it isn't high already
QB goes high following a rising edge of B, if it isn't high already
Reset goes high when both QA and QB are high and resets QA and QB



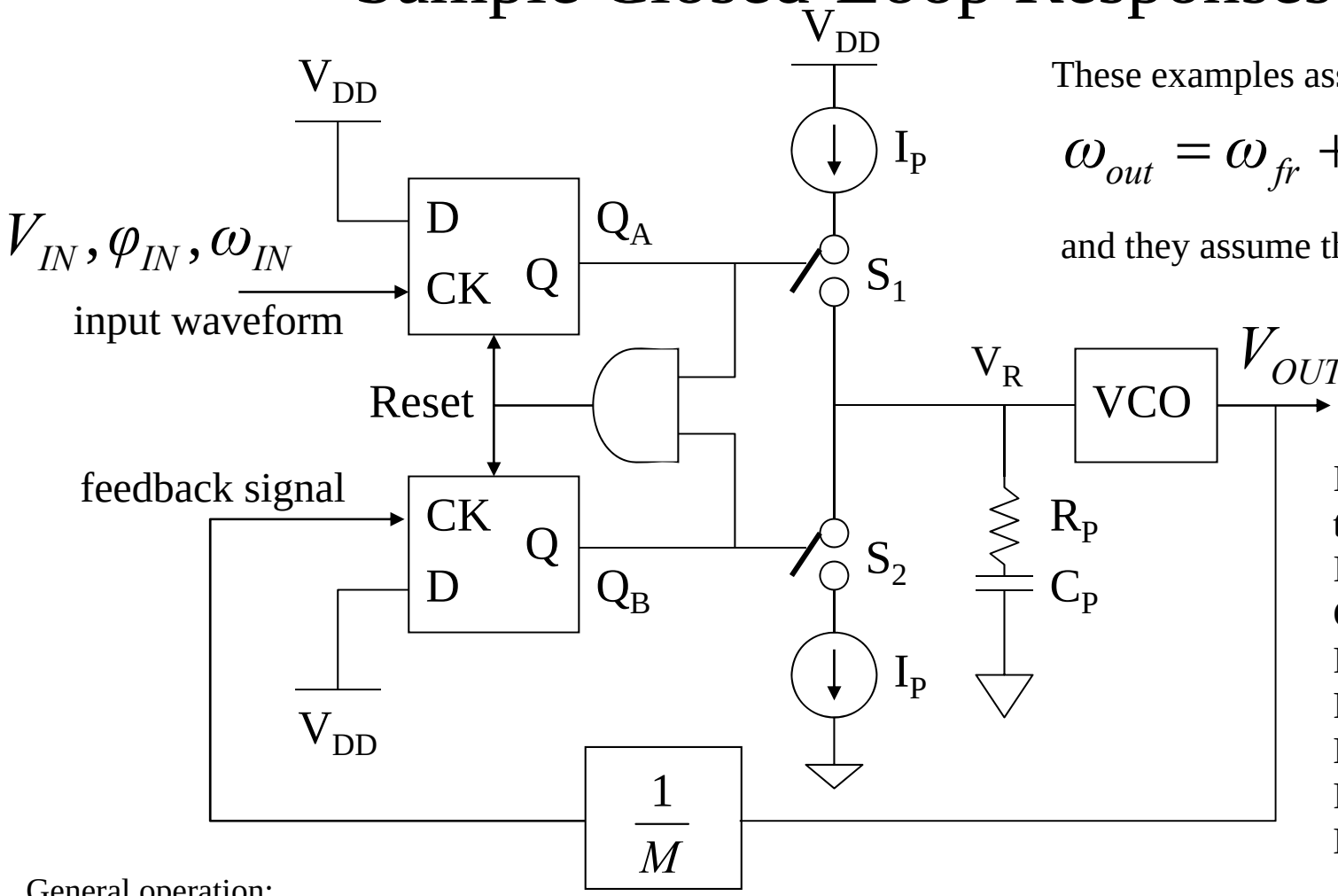
B is twice the frequency of A and as a result QB is high nearly all the time.
(There is also a phase difference between A and B here just to separate the rising and falling edges of QA and QB for clarity.)

B is twice the frequency of A



General behaviour: Because QB is high most of the time, the capacitor is discharging most of the time so its waveform looks like a linearly decreasing voltage (but there are flat regions when QB is 0).

Sample Closed-Loop Responses



These examples assume an ideal VCO

$$\omega_{out} = \omega_{fr} + K_{VCO} V_{CP}$$

and they assume that V_{CP} starts at 0V

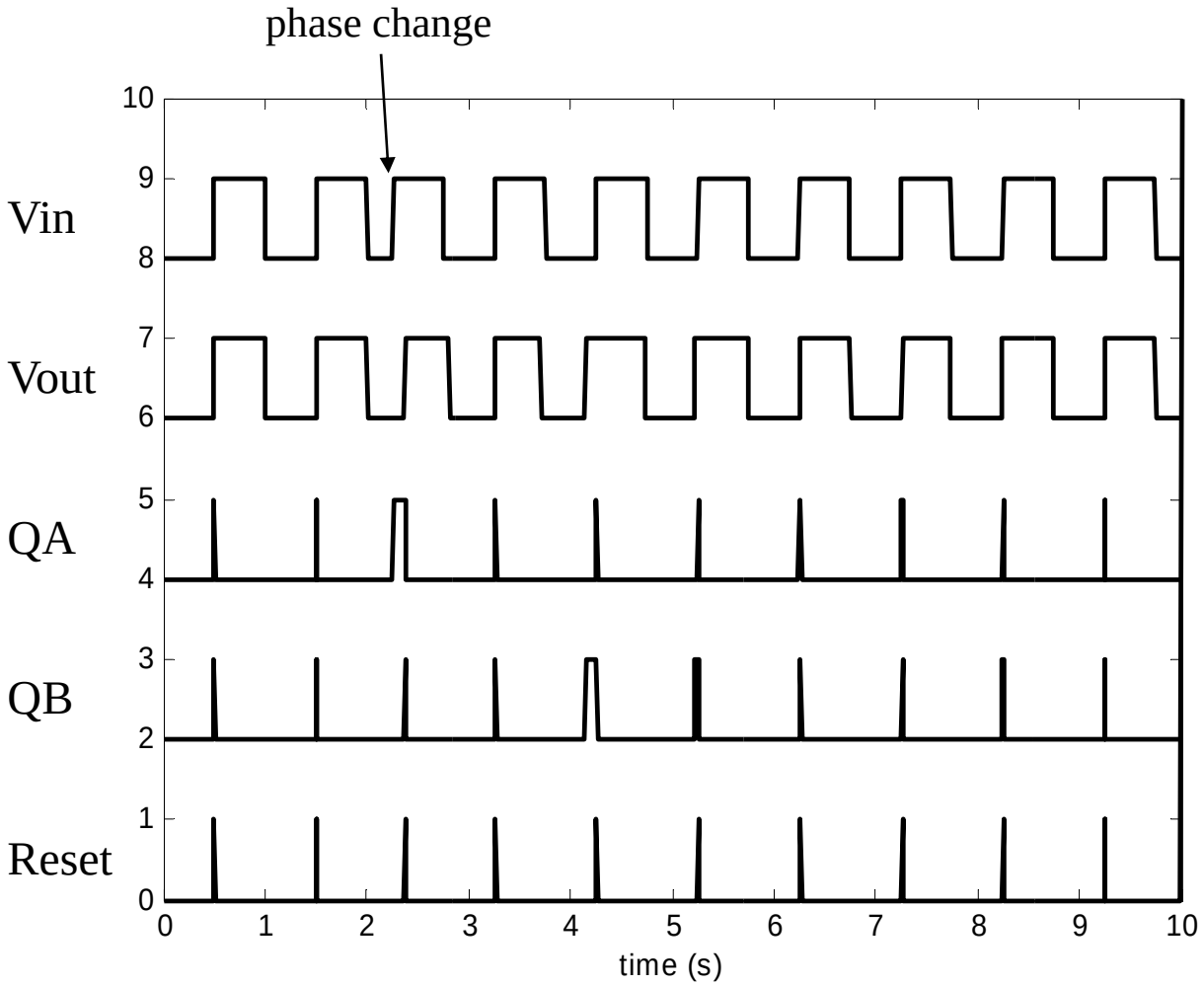
In most cases these examples use

I_p=1μA
C_p=1μF
R_p=1MΩ
F_{FR}=1Hz
K_{VCO}=1Hz/V
F_{IN}=1Hz
M=1

General operation:

With V_R at 0V the VCO runs at its free running frequency. If the input waveform has a higher frequency than the VCO or has the same frequency but is ahead of the VCO in phase, then QA will be high for longer durations than QB. This will cause a net charging current to be applied to the capacitor which will increase V_R and speed up the VCO. The system "should" eventually reach a stable condition where the feedback signal has the same phase and frequency as the input. At this point there will be no further *net* charging (or discharging) of the capacitor.

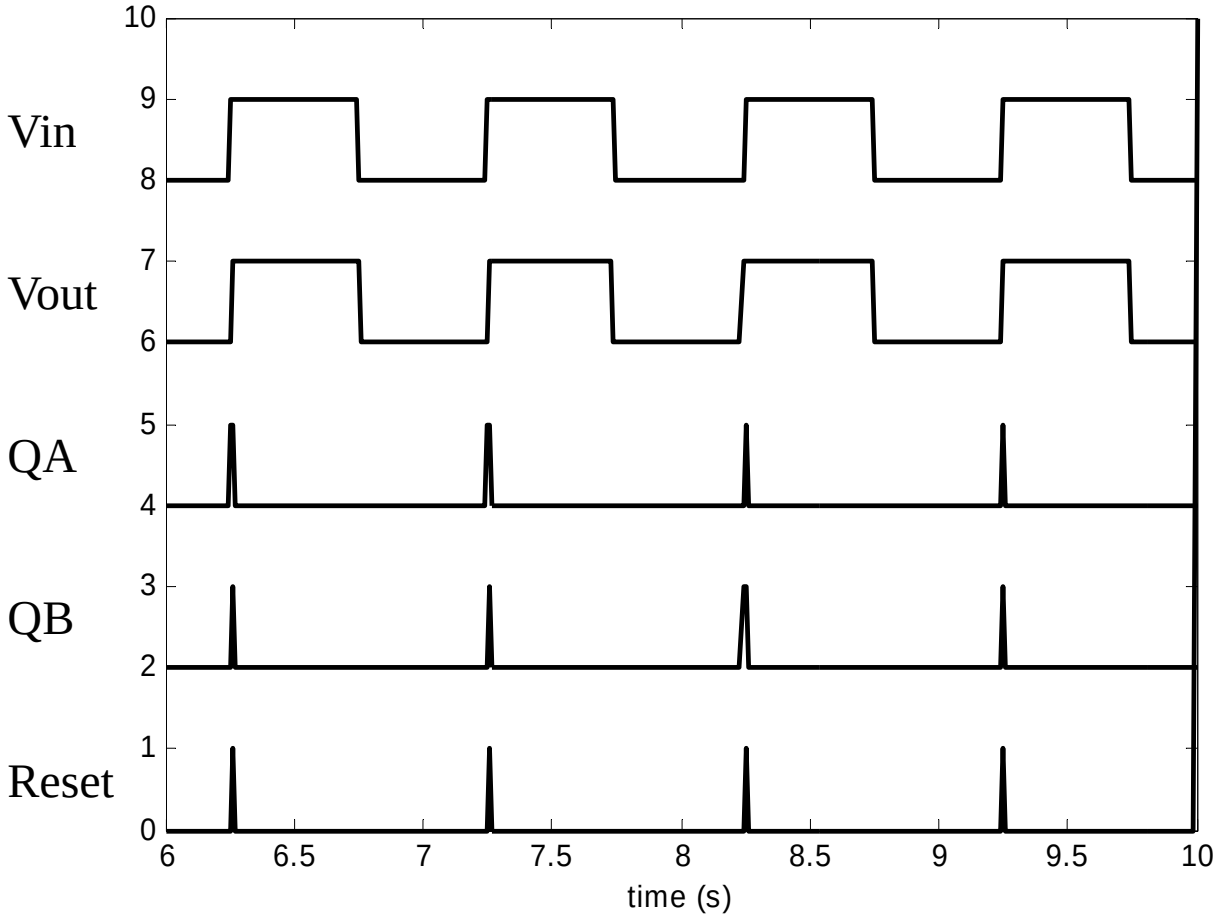
Phase step example (i)



ignore the y-axis scale – the waveforms are supposed to be logic levels

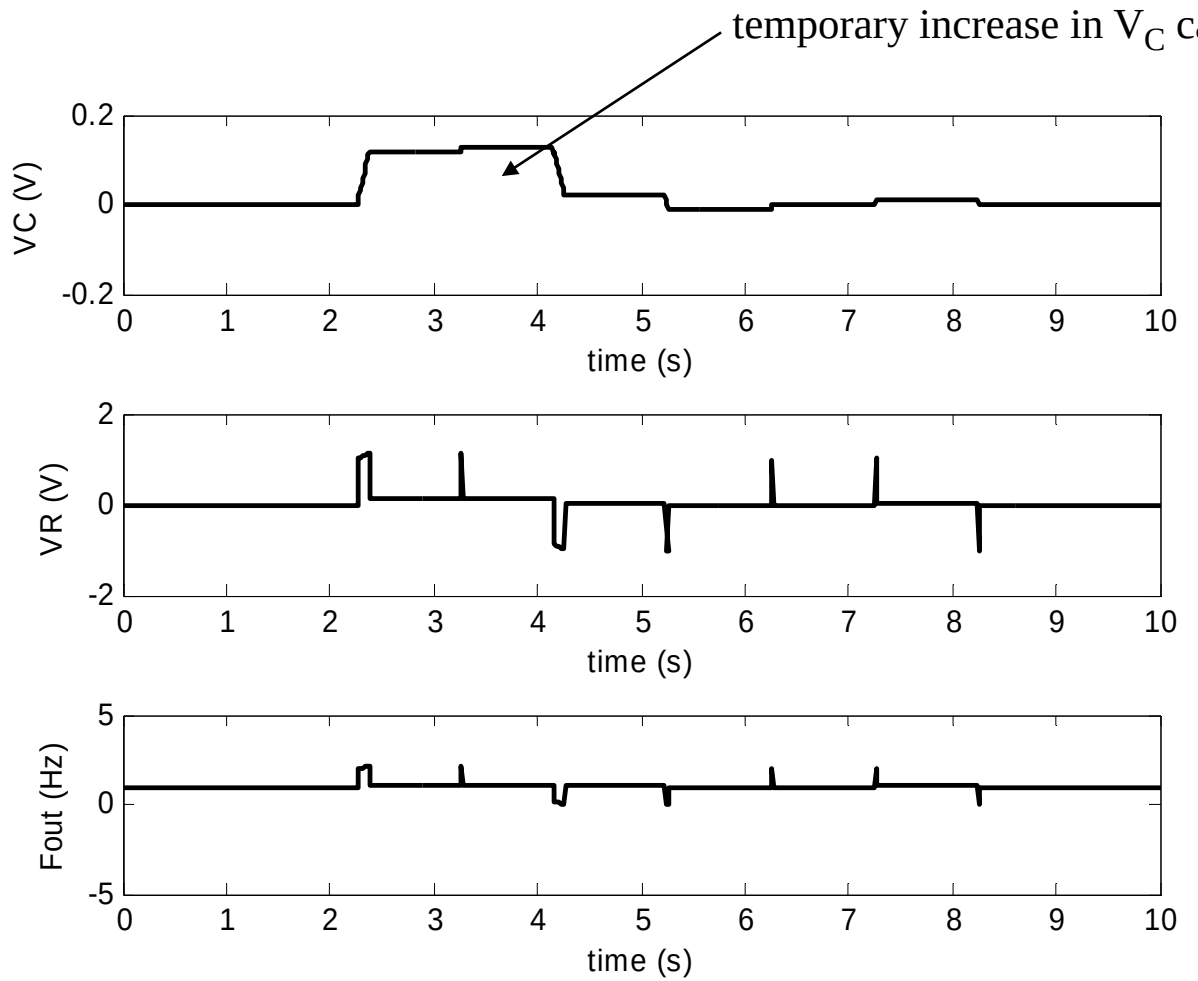
Phase step example (ii)

zoom-in to show waveforms when the loop has stabilized



ignore the y-axis scale – the waveforms are supposed to be logic levels

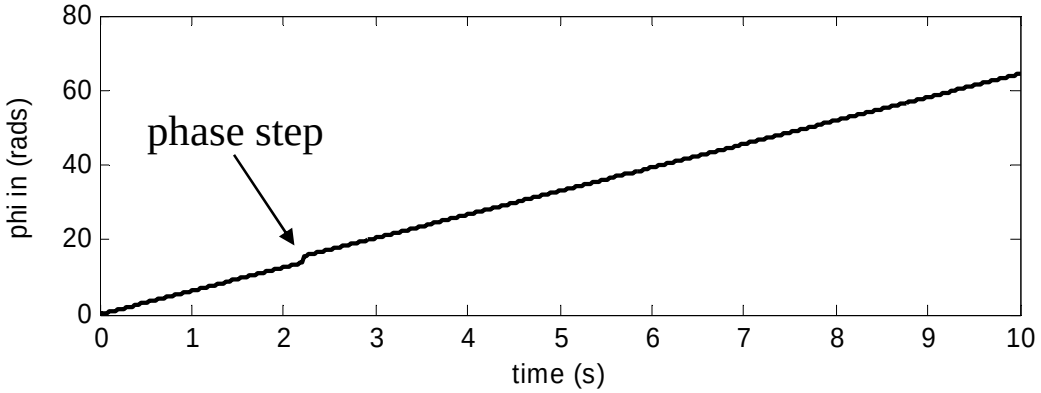
Phase step example (iii)



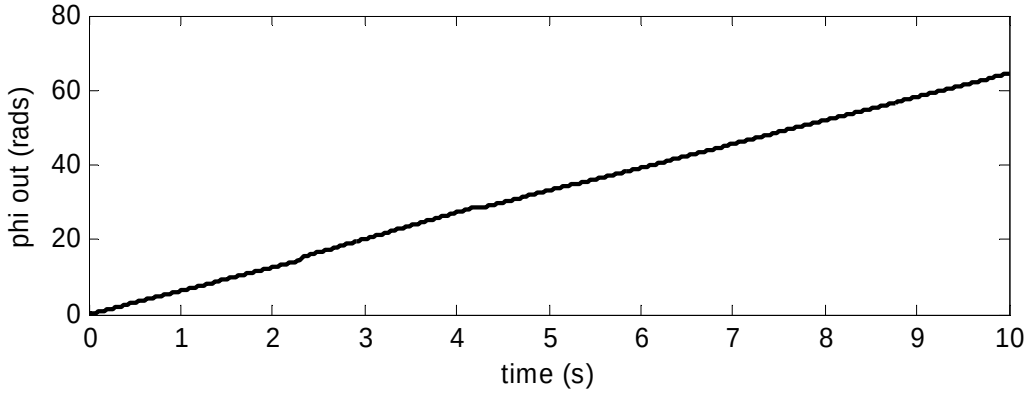
The input frequency is the same as the free running frequency of the VCO so the CP output settles back to 0V once the transient has settled down.

Phase step example (iv)

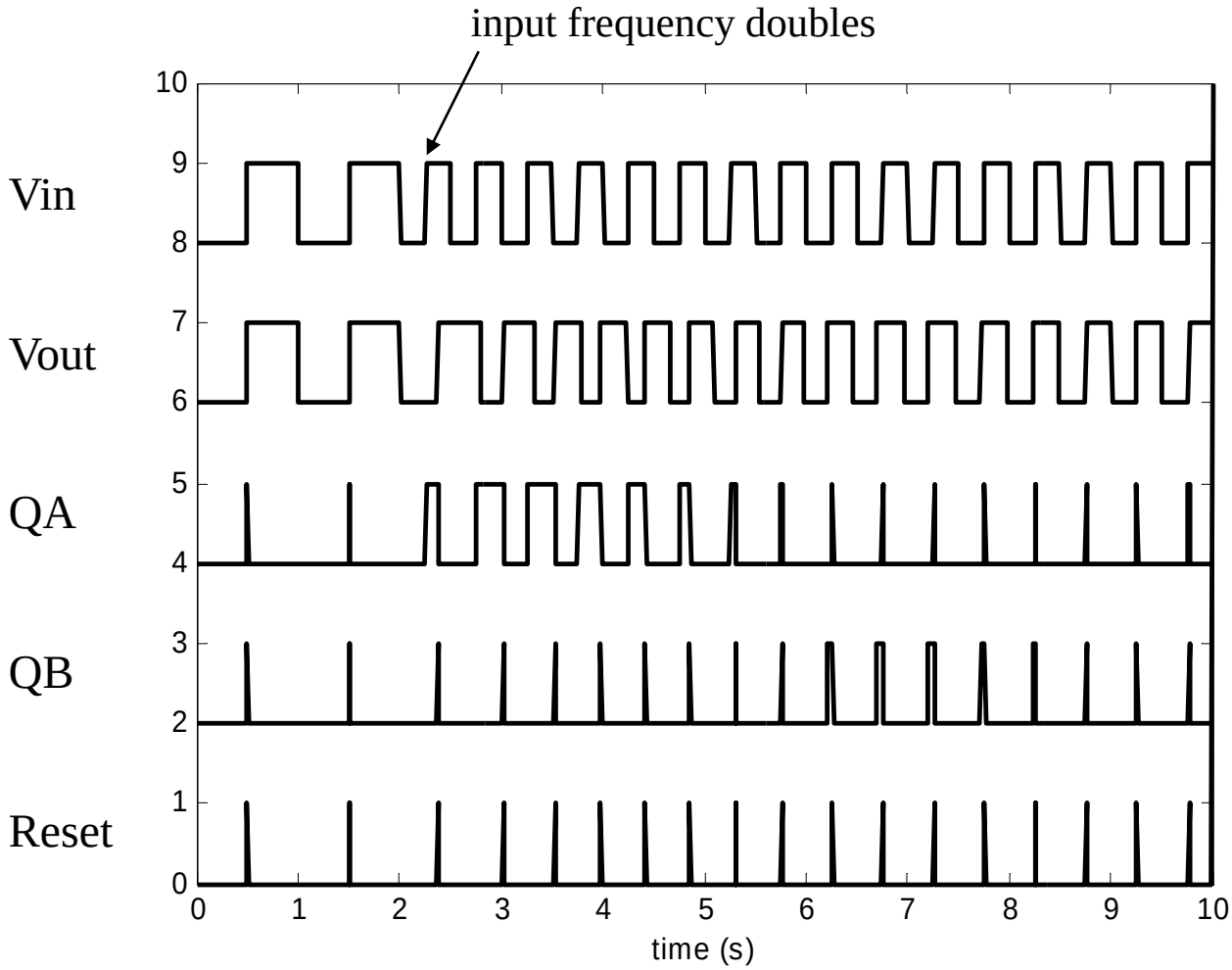
input phase



output phase



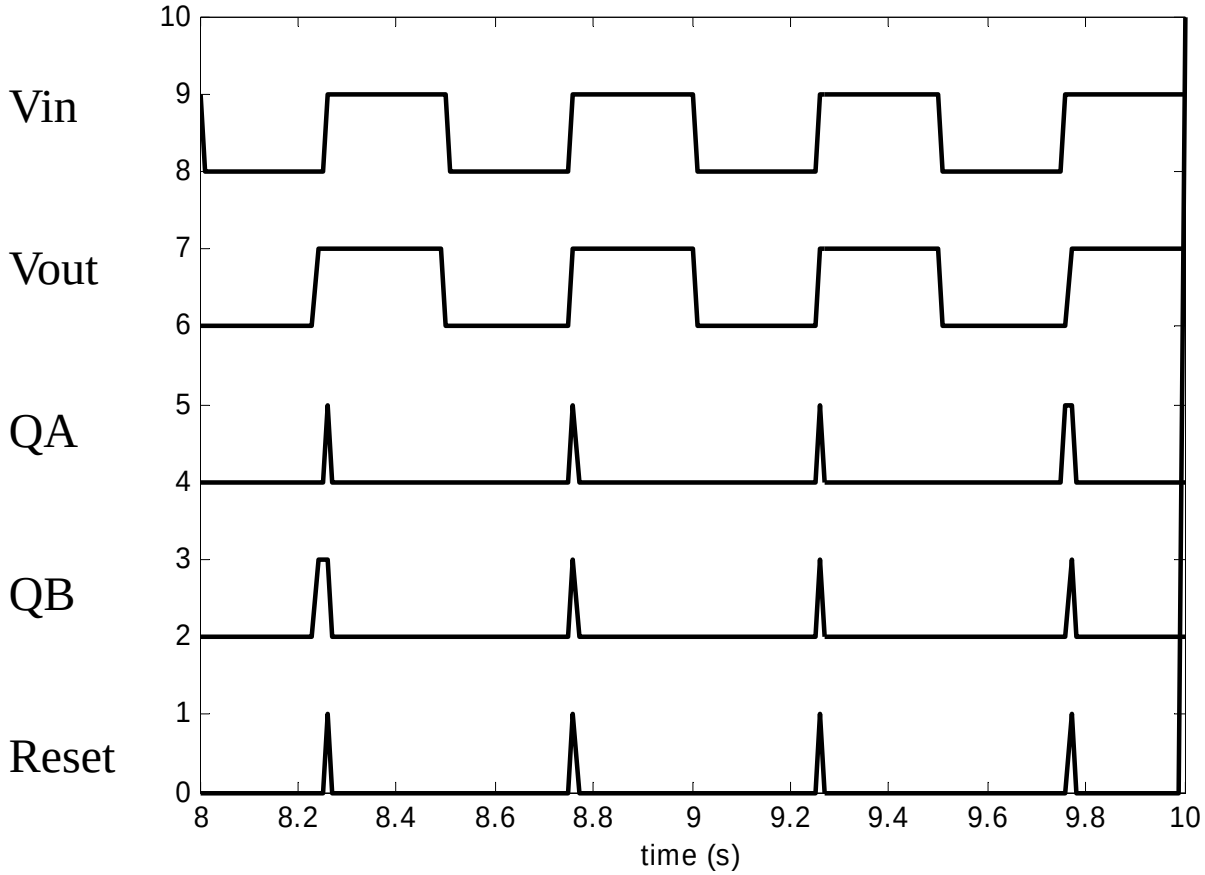
Frequency step example (i)



ignore the y-axis scale – the waveforms are supposed to be logic levels

Frequency step example (ii)

zoom-in to show waveforms when the loop has stabilized



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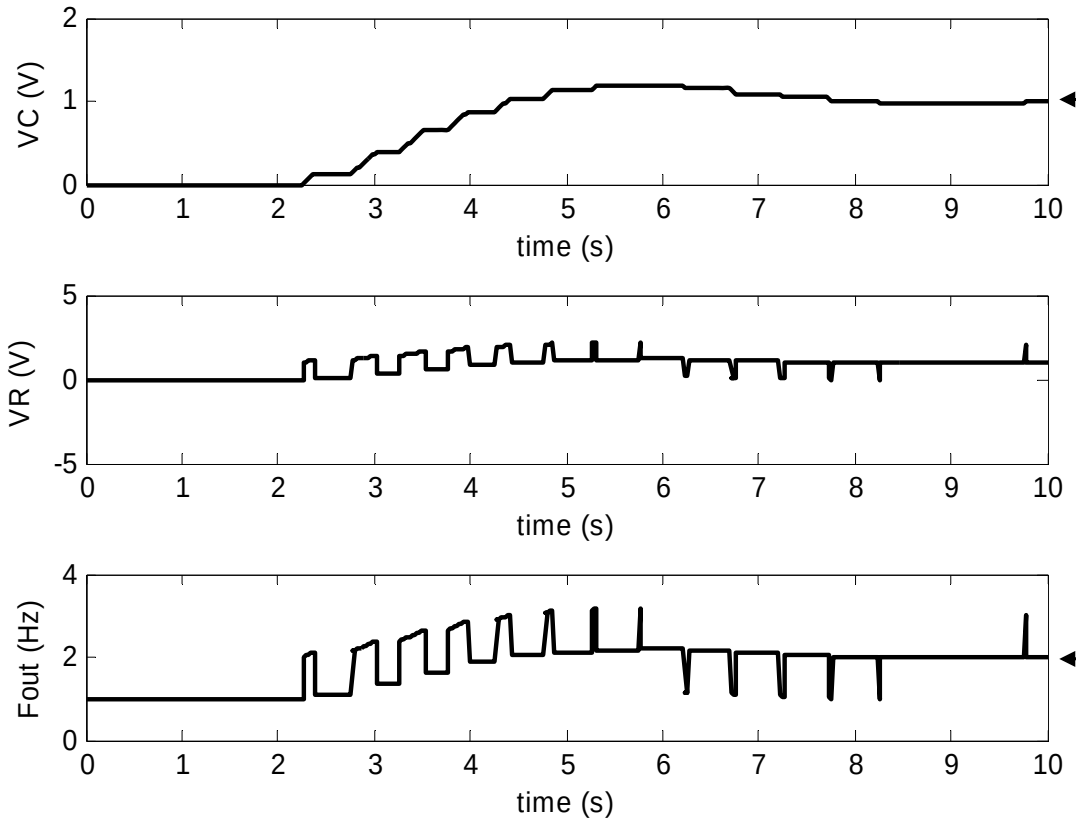
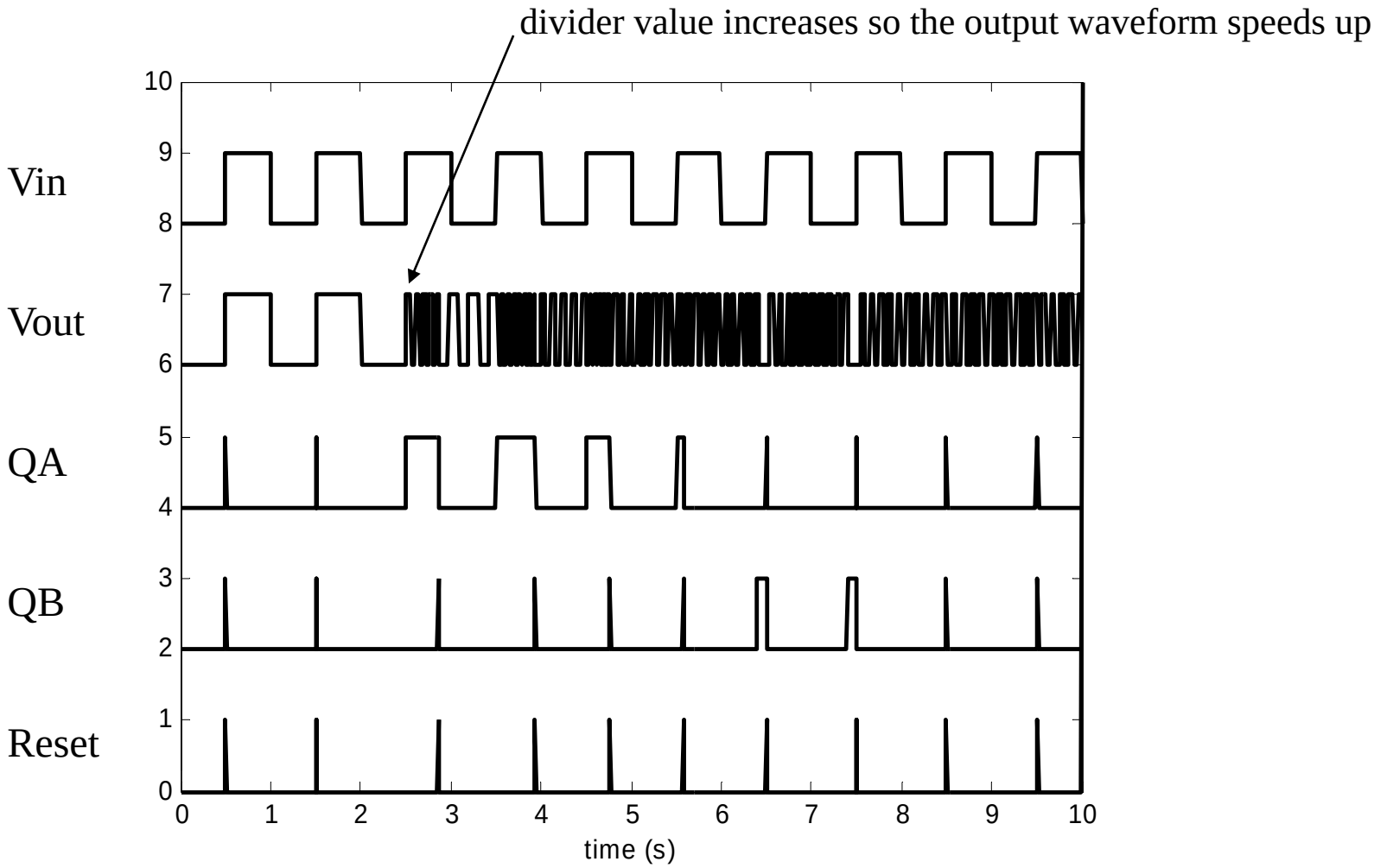
Frequency step example (iii)



The final o/p voltage of the CP is 1V which is needed to give a VCO frequency of 2Hz.

The o/p frequency settles down to the new i/p frequency of 2Hz.

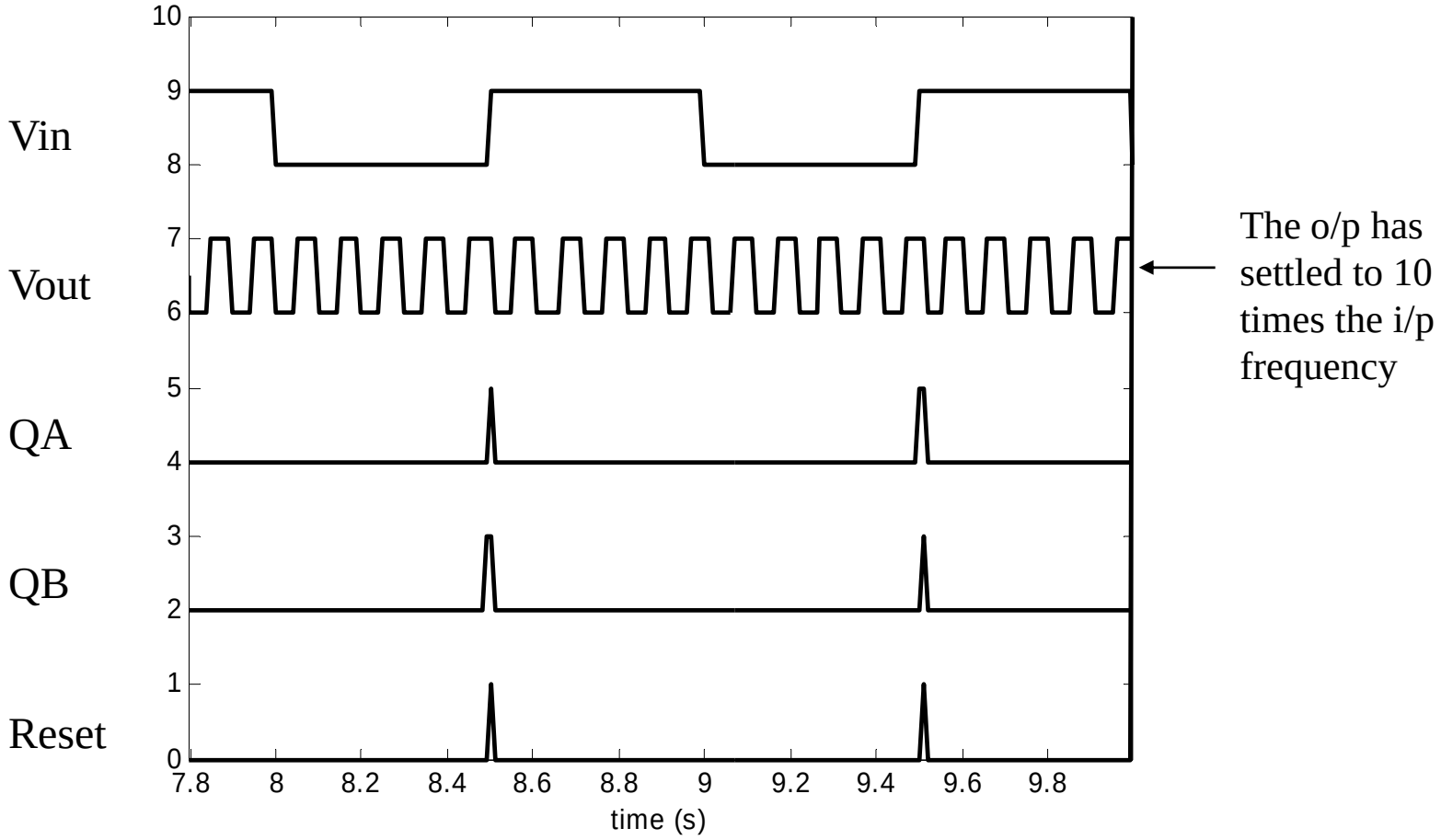
Change of feedback divider (M) from 1 to 10 (i)



ignore the y-axis scale – the waveforms are supposed to be logic levels

Change of feedback divider (M) from 1 to 10 (ii)

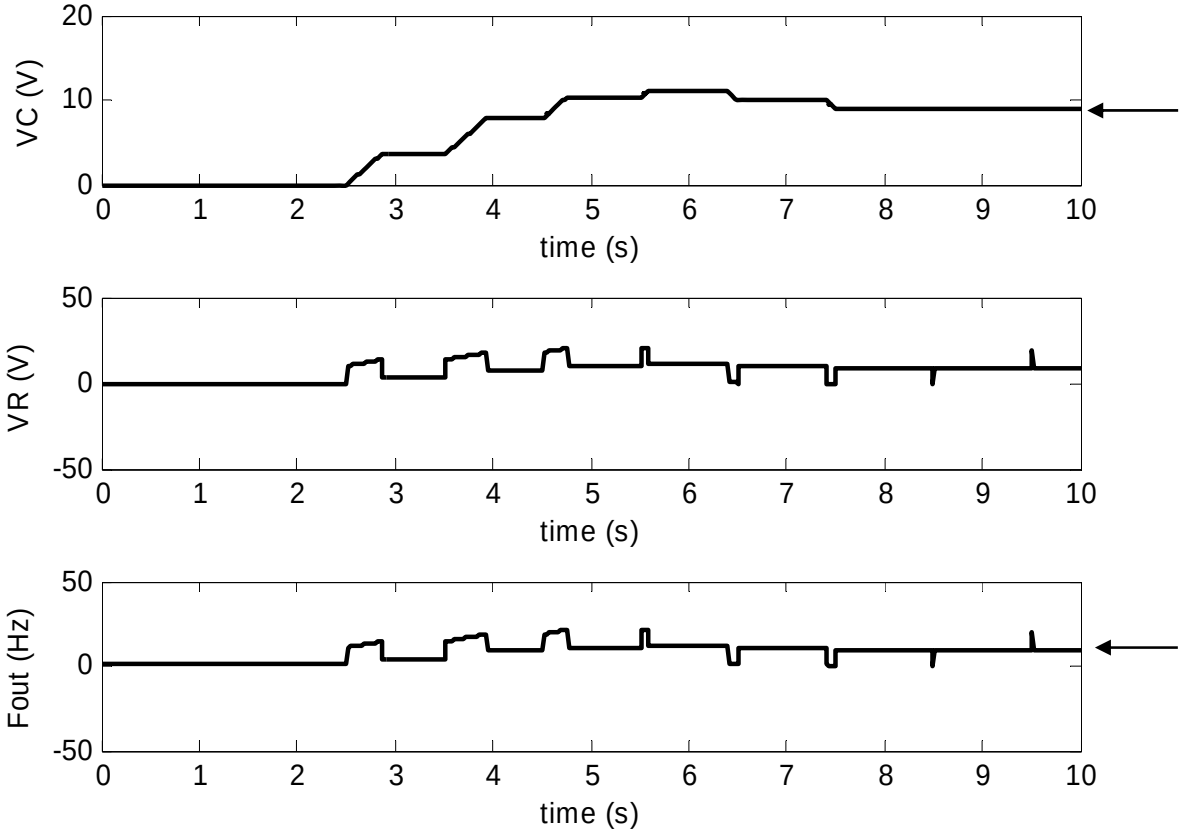
zoom-in to show waveforms when the loop has stabilized



ignore the y-axis scale – the waveforms are supposed to be logic levels

slight cheat here – I_P has been changed to 10μA to make the PLL work with a divider of 10 !

Change of feedback divider (M) from 1 to 10 (iii)

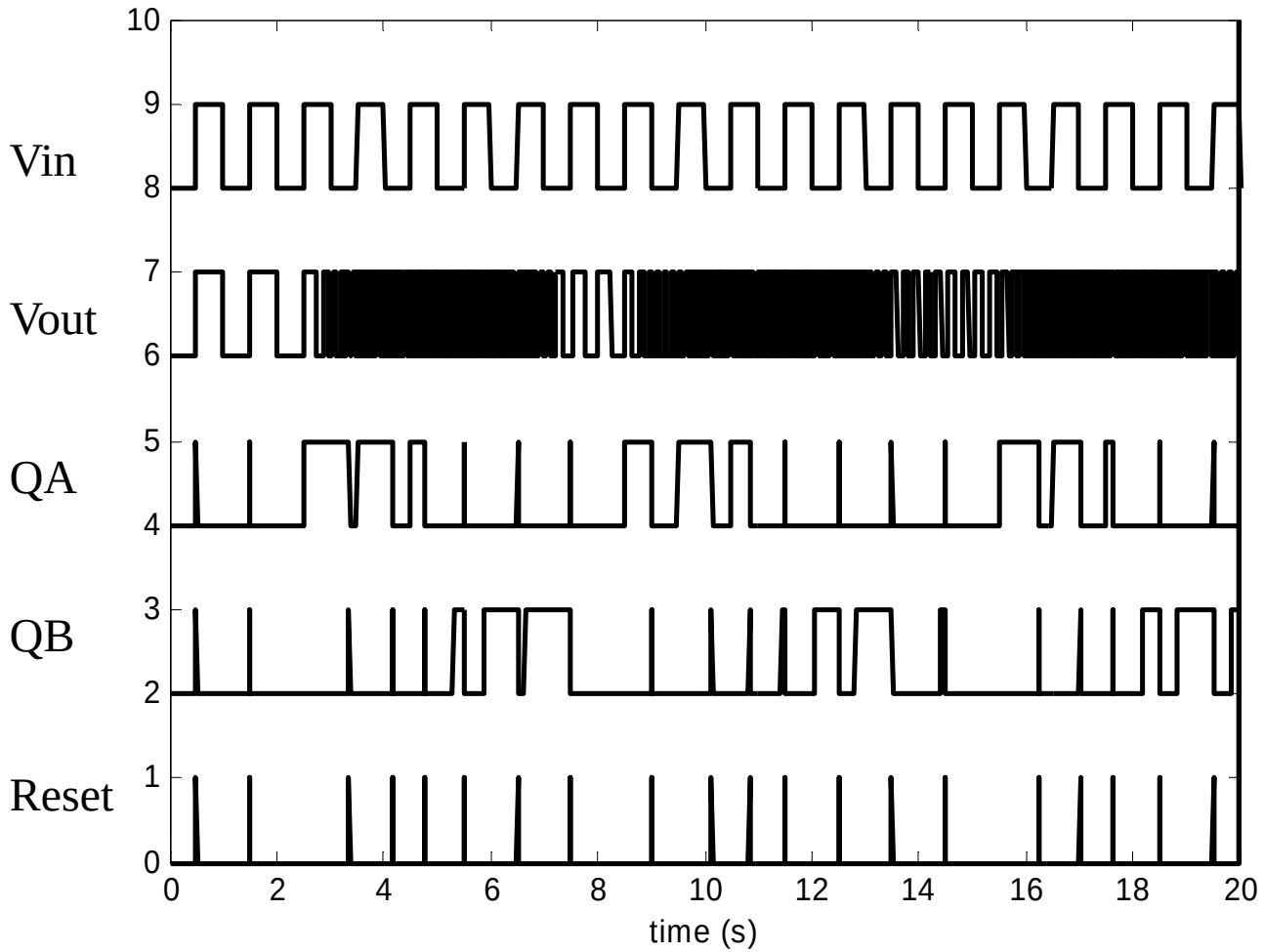


The CP o/p settles to 9V to give a VCO frequency of 10Hz.

The o/p settles to a frequency of 10HZ

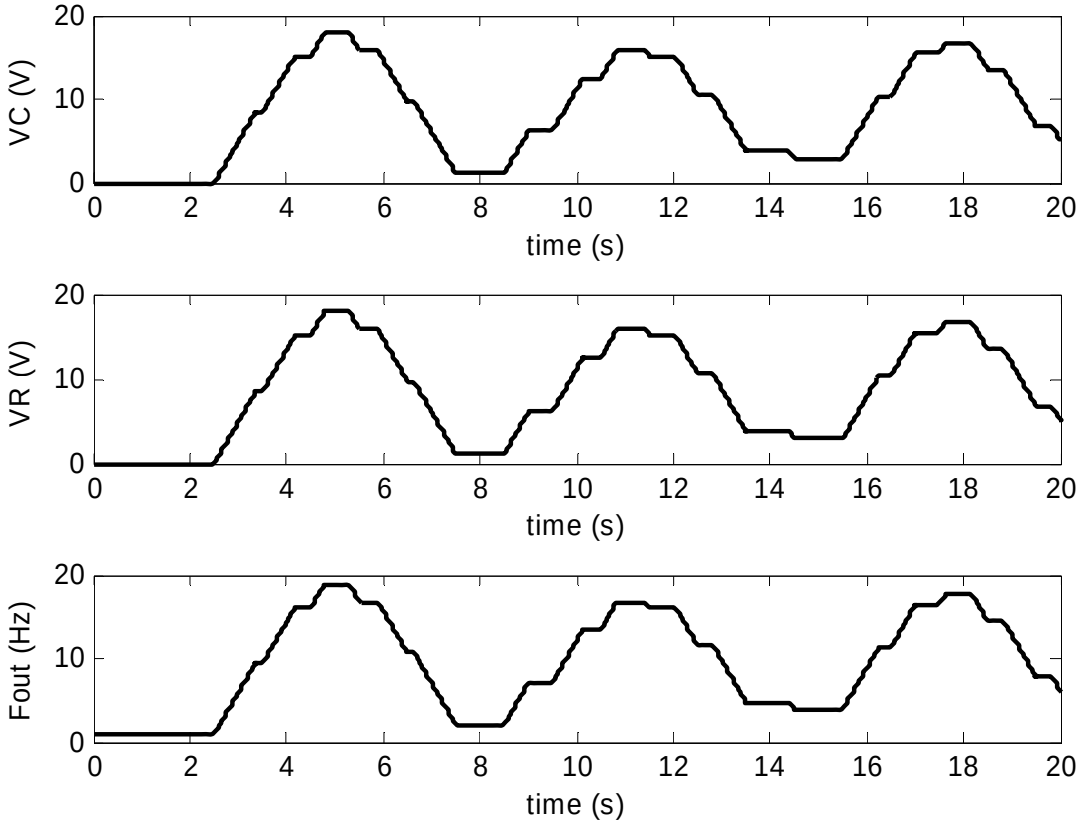
Note: there are some ridiculous voltages coming out of the charge pump here (25V) but it's only an example!

Change of feedback divider (M) from 1 to 10 and where R_P=0 (i)



With R_P=0 the loop becomes unstable when the divider value is changed from 1 to 10.

Change of feedback divider (M) from 1 to 10 and where R_P=0 (ii)



Here the loop quantities never settle down after the step change in the divider ratio. The loop is unstable with R_P=0