

UE4010 Exam



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Assume $I_{IN}=I_{OUT}=100\mu A$, $K_n'=200\mu A/V^2$, $V_{tn}=750mV$, $\lambda_n=0.04V^{-1}$.

- (i) What is the minimum voltage at the output node, i.e. the drain of M4, such that all transistors are biased in saturation?
- (ii) Derive an expression for the small-signal output resistance.
Assume $g_{m1}, g_{m2}, g_{m3}, g_{m4} \gg g_{ds1}, g_{ds2}, g_{ds3}, g_{ds4}$.
- (iii) What is the change in current if the voltage at the output node varies by 10mV?
Assume all transistors are in saturation.
- (iv) It is desired to increase the mirroring ratio by increasing the width of M2 only. What is the largest value of output current such that M2 remains in saturation?

Question 3

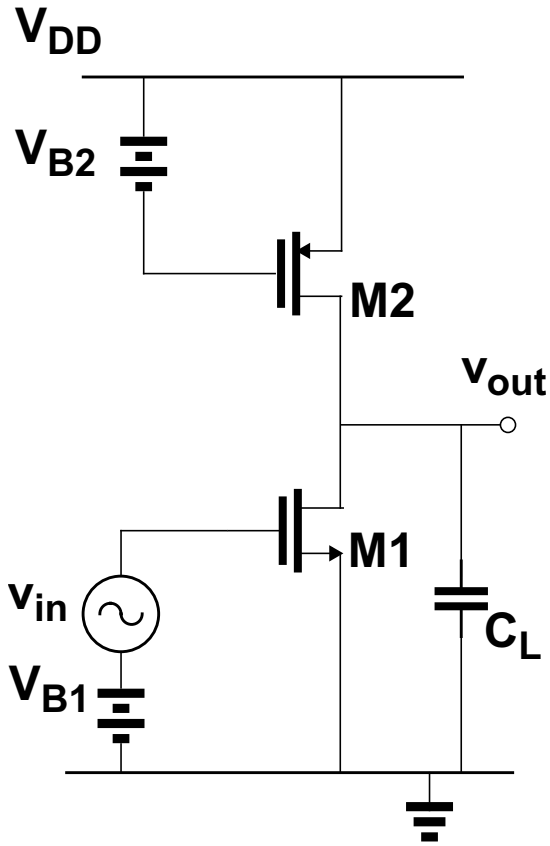


Figure 3a

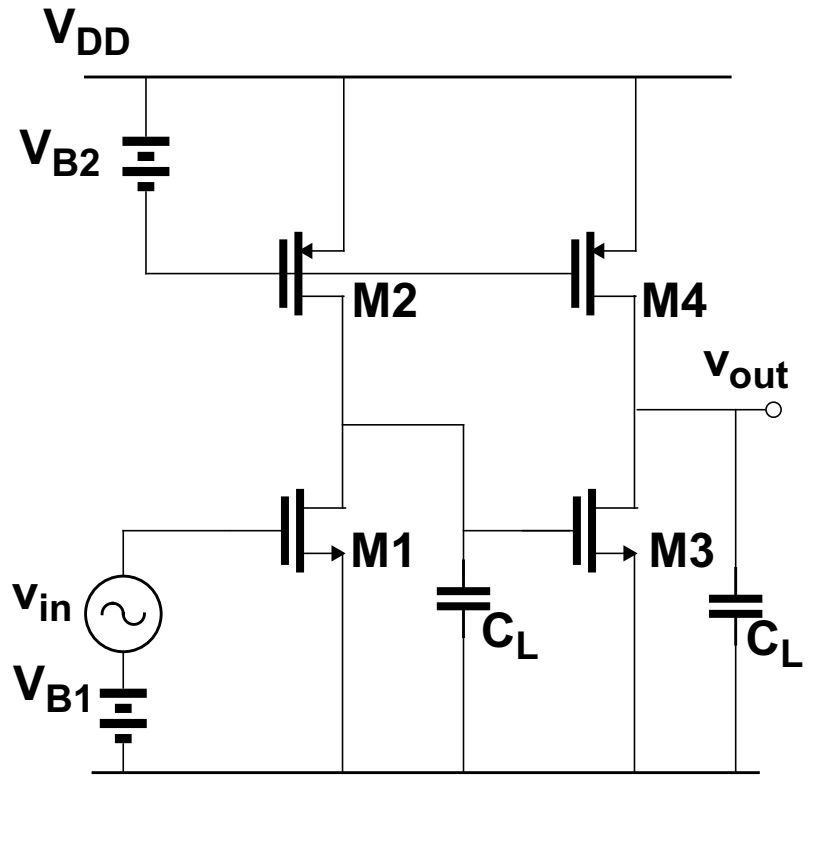


Figure 3b

- (i) Draw the small-signal equivalent circuit for the gain stage shown in Figure 3a.
- (ii) Ignoring all capacitances except C_L , derive an expression for the high frequency transfer function (v_{out}/v_{in}).
- (iii) Draw a Bode diagram of the gain. Indicate the values of the dc gain in dB, the pole frequency and the high-frequency roll-off if
 $V_{B1}=1.1V$, $V_{tn}=0.7V$, $V_{tp}=-0.7V$, $\lambda_n=\lambda_p=0.02V^{-1}$, $C_L=1pF$.
 Assume both transistors are in saturation with a drain current of $200\mu A$.
- (iv) The circuit shown in Figure 3a is cascaded with an identical stage with an identical load capacitance as shown in Figure 3b. Draw the Bode diagram of the gain of the cascaded circuit, indicating the values of the dc gain in dB, the pole frequency and the high-frequency roll-off.

