Thermal Oxidation Of Silicon

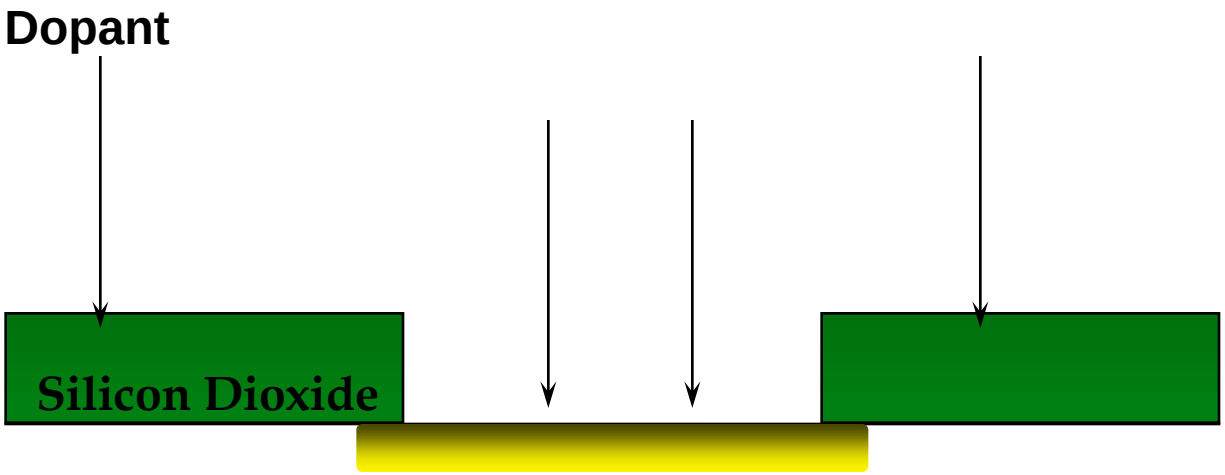
Introduction

- Oxidation is one of the key processes in the manufacture of silicon integrated circuits
- SiO_2 is relatively easy to grow
- It is an excellent insulator
- It is an excellent diffusion barrier
- It is stable at high temperatures
- It is easily etchable

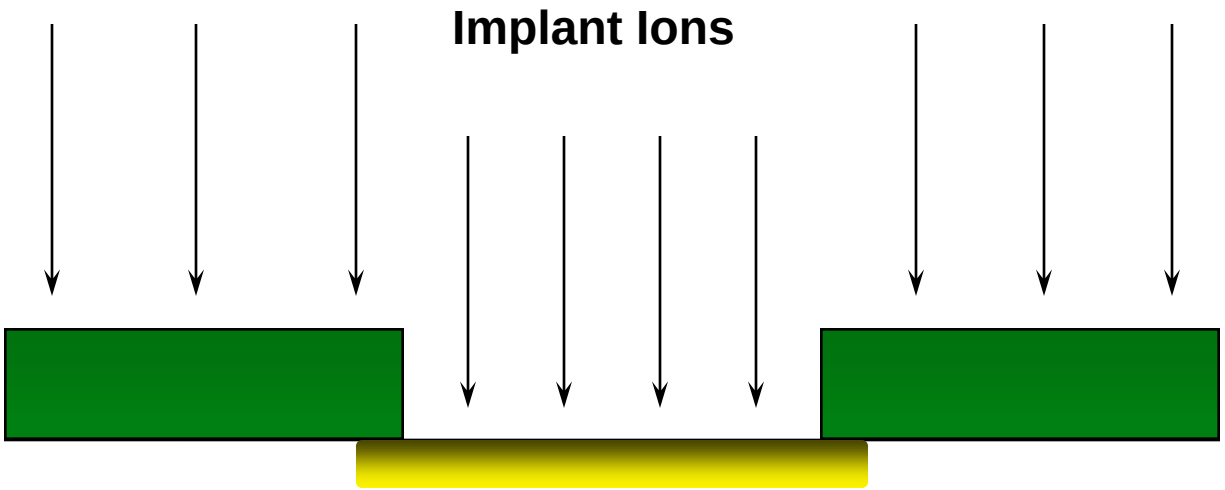
Silicon Dioxide

- Good insulator -- Breakdown field 10MV/cm
  - **1000Å oxide will block 100V**
  - **1000Å=100nm=1/100,000 of a cm**
- Very stable at high temperatures
  - **up to 1300C**
- A very good diffusion barrier
- It is etchable
  - **Wet in HF**
  - **Dry in Fluorine compounds**

Oxide as a Diffusion Barrier



Oxide as an Implant Barrier



Oxidation Mechanism

- Dry Oxidation: the oxidising ambient is oxygen
  - **$Si(solid) + O_2(gas) \text{ --------Heat-----> } SiO_2(solid)$**
- Wet oxidation: the oxidising ambient is water vapour
  - **$Si(solid) + H_2O(gas) \text{ ----Heat---> } SiO_2(solid) + 2H_2(gas)$**

Interface States

- When the charge density between the oxide and the silicon is required to be low, thermal oxidation is the preferred technique (Silicon dioxide can also be formed by CVD deposition)
- Typical oxidation temperatures
  - **800^{o}C -- 1200^{o}C**
- Typical gas flows for furnaces setup for 4” wafers 5/6 slpm

Wet or Dry Oxidation I

- Oxides grown by dry oxidation
  - **in general have a lower trap density than those grown by wet oxidation**
  - **the critical oxides in a MOS process are generally grown dry**
  - **for example the Gate Oxide**
  - **oxidation rates tend to be low**

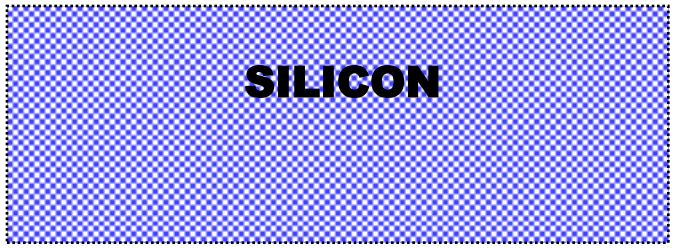
Wet or Dry Oxidation II

- Oxides grown by wet oxidation
  - **the thicker oxides in the non-device areas of the circuits are grown wet**
    - **for example field oxides**
  - **these oxides tend to be thicker and can be grown more quickly using wet oxidation techniques**

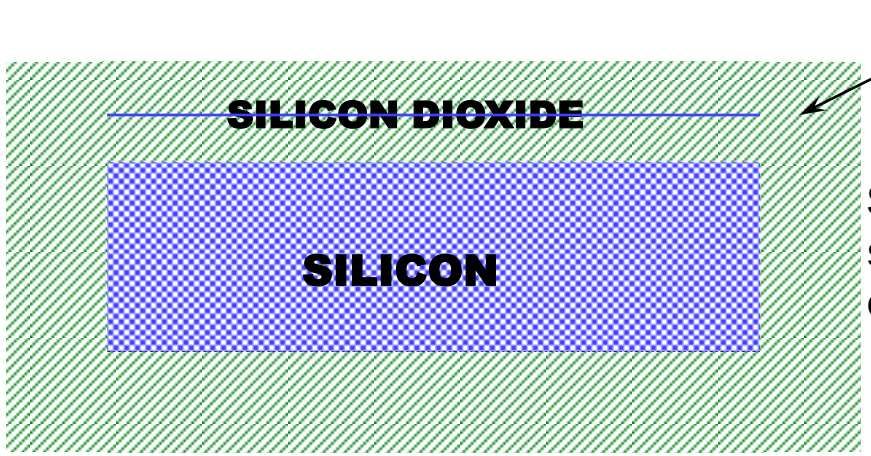
Wet Oxides Vs Dry (Oxidation Rate)

- Part of the reason why wet oxidation is faster than dry oxidation is the concentration of the oxidising species (i.e. oxygen and water vapour) at typical oxidation temperatures
  - **at 1000°C**
    - » **O_2 = 5.2 X10^{16} /cm^3**
    - » **H_2O = 3.0X10^{19}/cm^3**
- The concentration of water vapour is approximately 1000 times that of oxygen at 1000°C

OXIDATION



Section of silicon before oxidation



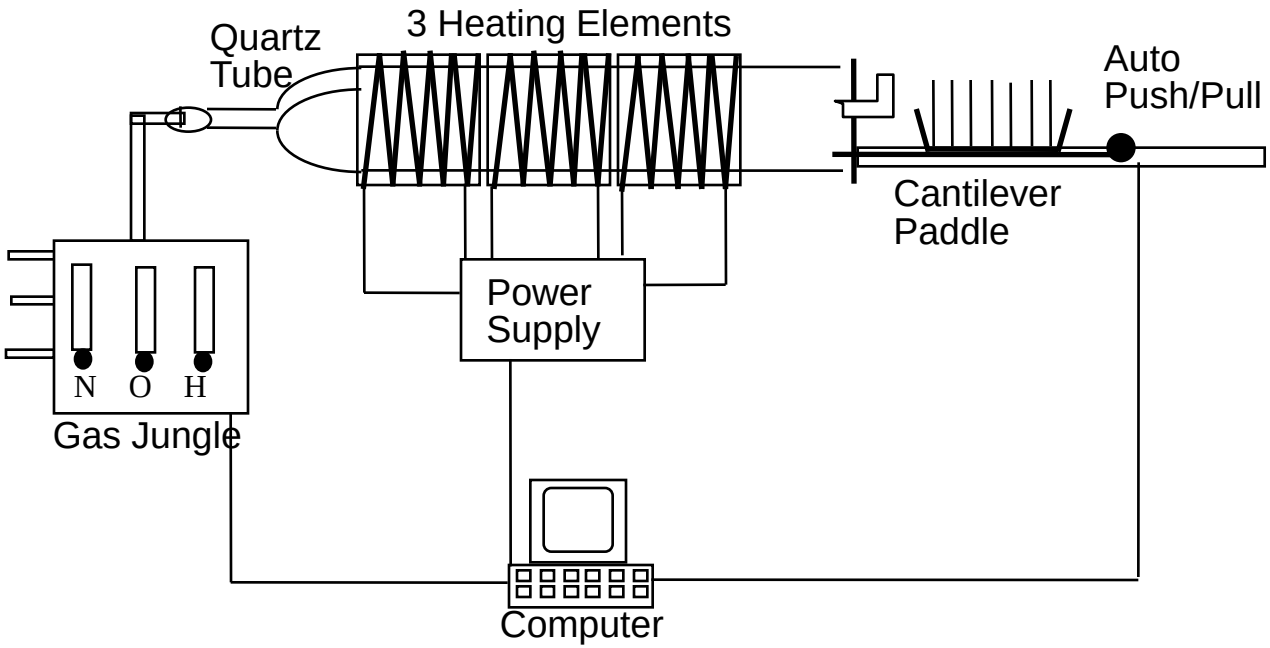
Previous silicon surface

Section of silicon after oxidation

Silicon Consumed During Oxidation

- The silicon in the silicon dioxide is provided by the wafer itself
- This means some of the silicon is consumed during the oxidation process
- The amount of silicon consumed is 0.44 times the thickness of oxide grown
  - **i.e. 1000nm of oxide grown**
  - **440nm of silicon consumed**

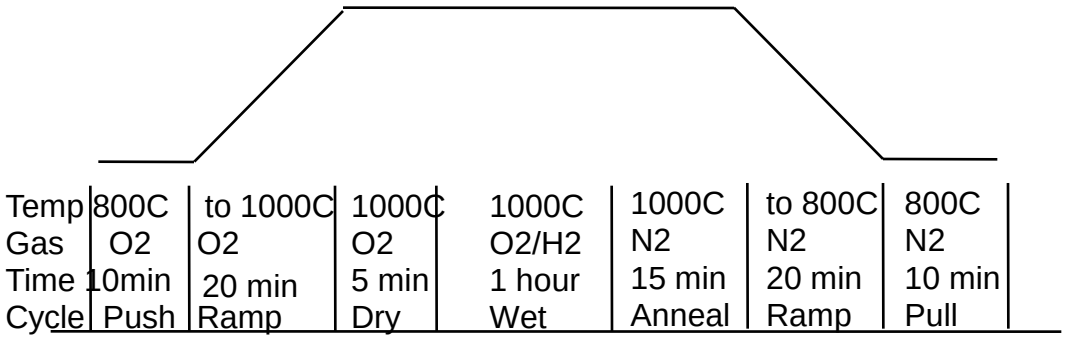
Horizontal Furnace Set-up



Typical Furnace Sequence

- Step 1 Push in O_2 @ 800°C
- Step 2 Ramp to 1000°C in O_2
- Step 3 Dry oxidation 5 min in O_2 @ 1000°C
- Step 4 Wet oxidation 1 hour (O_2/H_2) @ 1000°C
- Step 5 Anneal in N_2 for 30 min @ 1000°C
- Step 6 Ramp down to 800°C in N_2
- Step 7 Pull in N_2

FURNACE CYCLE



Temperature Control

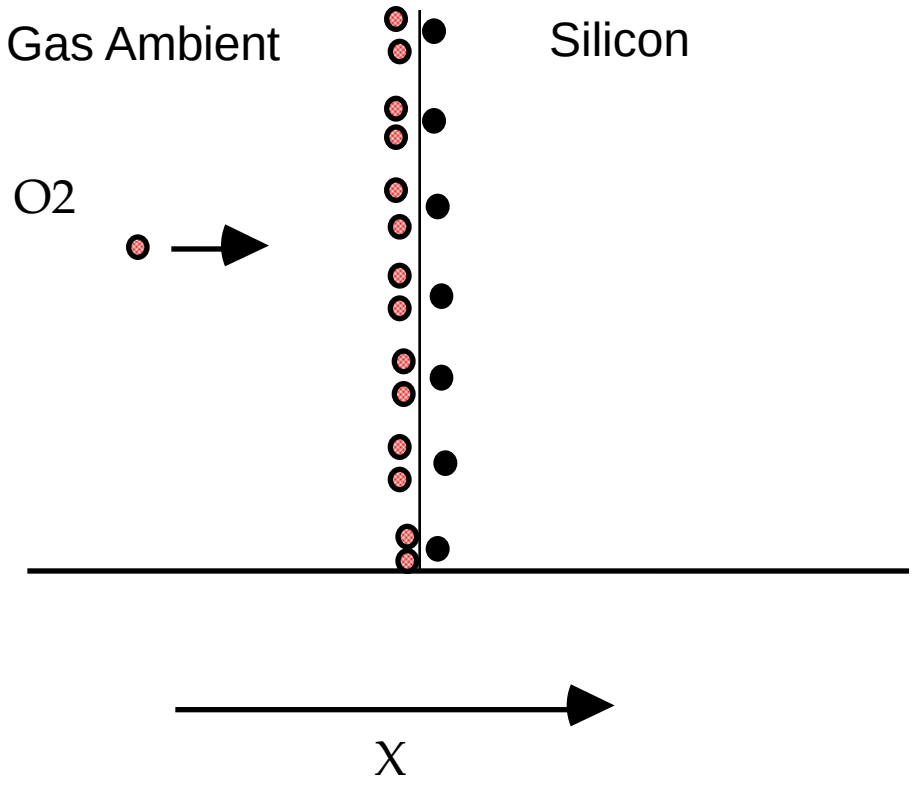
- The temperature of the furnace is one of the principle parameters in determining the oxidation thickness
- Tight temperature control is critical for
  - **thickness control**
    - **across the batch**
    - **across the wafer**
    - **batch to batch**
- Two sets of thermocouples are used, controlled by a computer algorithm

Temperature Control 2

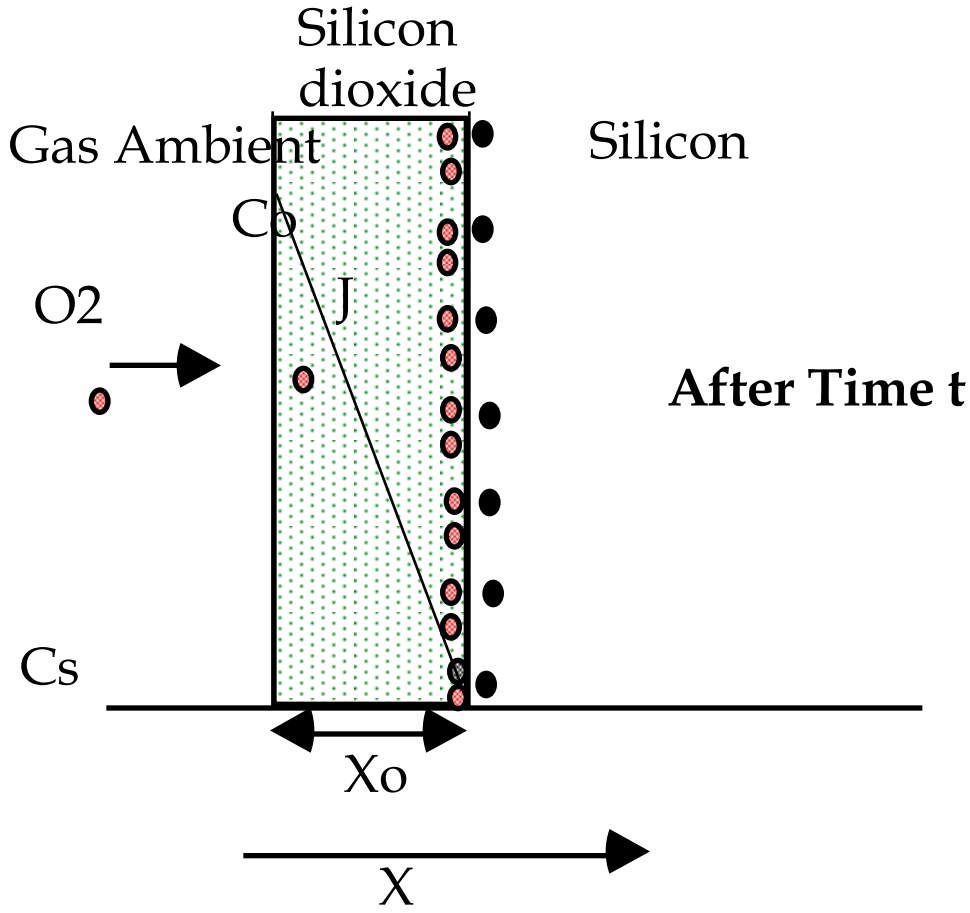
- Spike thermocouples
  - **Set outside the quartz tube between the windings of the furnace element**
  - **Give a fast response to temperature changes**
- Profile thermocouples
  - **Inside the quartz tube in close proximity to the wafers**
  - **Give an accurate representation of the actual temperature being seen by the wafers in the tube**

Oxidation Model

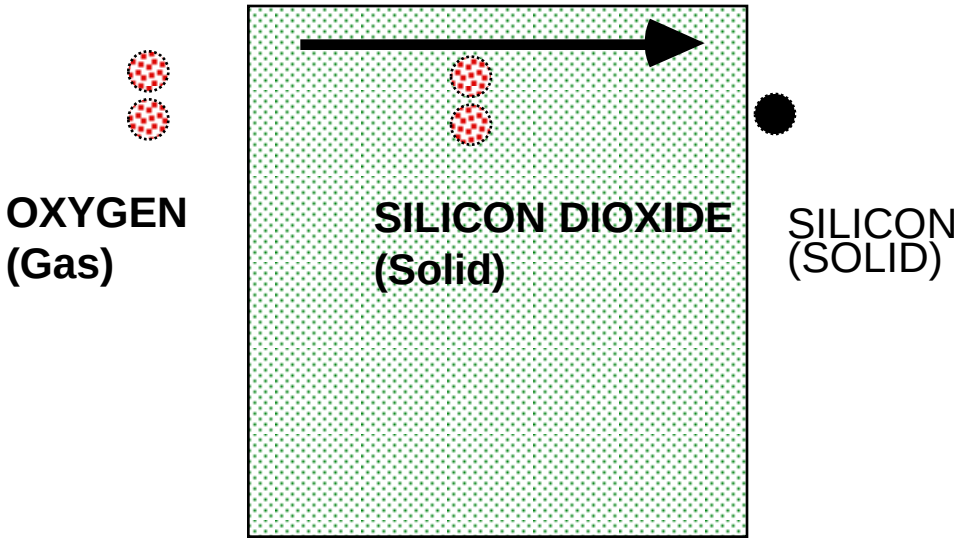
Initially



Oxidation Model 2

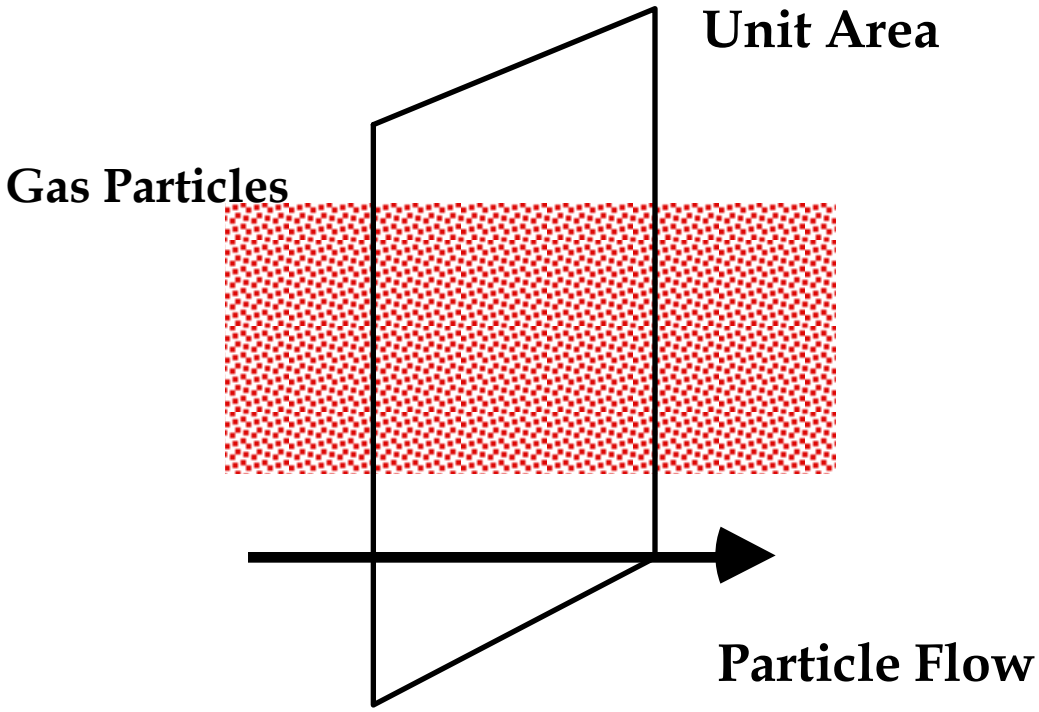


Oxidising Molecules Diffusing through Oxide



Diffusion of oxygen through silicon dioxide

Flux



Ficks Law States : The particle flow per unit area J (flux) is directly proportional to the concentration gradient.

Mathematical Model

- Derived from Ficks law
  - **J = D (dC/dx)**
  - **J = flux**
    - » **the number of particles diffusing through unit area**
  - **D = the diffusion coefficient (different for different diffusing molecules**
  - **dC/dx = the concentration gradient**
    - » **Particles move from areas of high concentration to areas of low concentration**

Mathematical Model

- Based on this law and the reaction rate an equation can be derived relating the grown oxide thickness to time and temperature

Ficks Law

Ficks Law States : The particle flow per unit area J (flux) is directly proportional to the concentration gradient.

1. $$J = D\frac{\partial C}{\partial x}$$

D = diffusion coefficient
N or C = particle concentration

Ficks Law becomes :

2. $$J = D\frac{(Co - Cs)}{Xo}$$

Xo is the thickness of the oxide at any given time.

Oxidation Rate

The oxidation rate is proportional to the concentration at the silicon surface.

3. $J_1 = k_s C_s$ **ks - Rxn rate const.**

Combine Equations 2.3 Eliminating Cs

4. $$J = \frac{D\ C_o}{X_o + D/k_s}$$

Rate of Change of Thickness

The rate of change of oxide thickness is equal to the flux divided by the number of molecules.

5. $$\frac{dx}{dt} = \frac{J}{C_1} = \frac{D\frac{C_o}{C_1}}{X_o\frac{D}{k_s}}$$

The solution to this differential equation

6. $$X_o^2 + AX_o = B(t + \tau)$$ **where**

$$A = \frac{2D}{k_s}$$

$$B = 2D\frac{C_o}{C_1}$$

Oxidation Thickness Equation

At the boundary condition t = 0 Xo = do

$$\tau = d_o^2 + \frac{A d_o}{B}$$

$$= d_o^2 + \frac{2D/k_s d_o}{C_1/2D\ C_o}$$

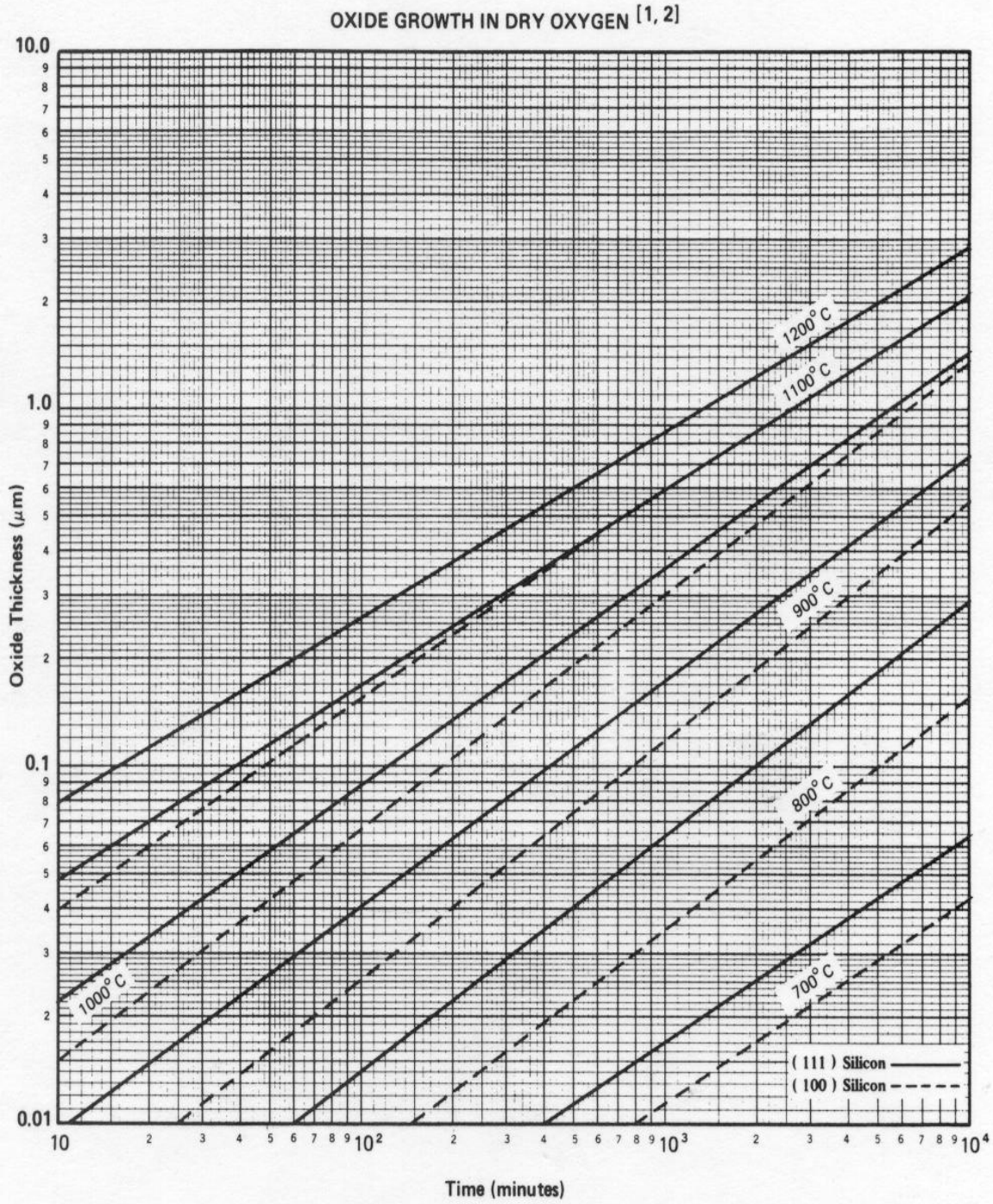
τ represents a time coordinate shift to take account of any initial oxide thickness before the oxidation takes place (a native oxide or an oxide from a previous oxidation).

7 $$X_o = A/2\left[\sqrt{1 + \frac{t+\tau}{A^2/4B}} - 1\right]$$

Approximations to Full Equation

For very short times i.e. $(t + \tau) << A^2/ 4B$
This equation simplifies or is approximated by :-
$Xo = B/ A (t + \tau)$
This describes the linear growth region
B/ A = Linear Rate Constant

For very long times $(t + \tau) >> A^2/ 4B$ or $t >> \tau$
The equation is approximated by : -
$Xo = \sqrt{Bt}$ This describes the parabolic region.
B = Parabolic rate constant



Dry Oxidation Plot

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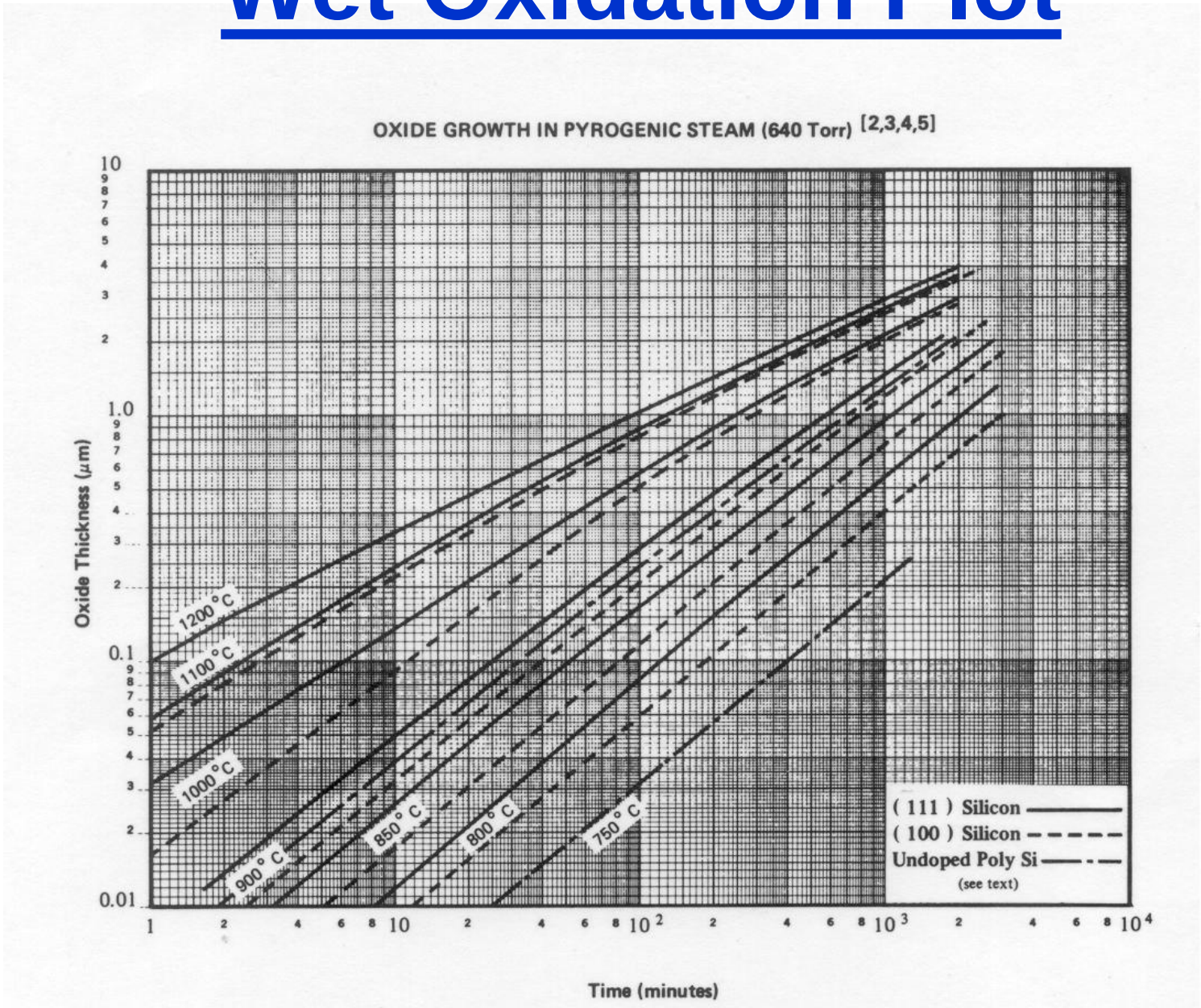
Wet Oxidation Plot



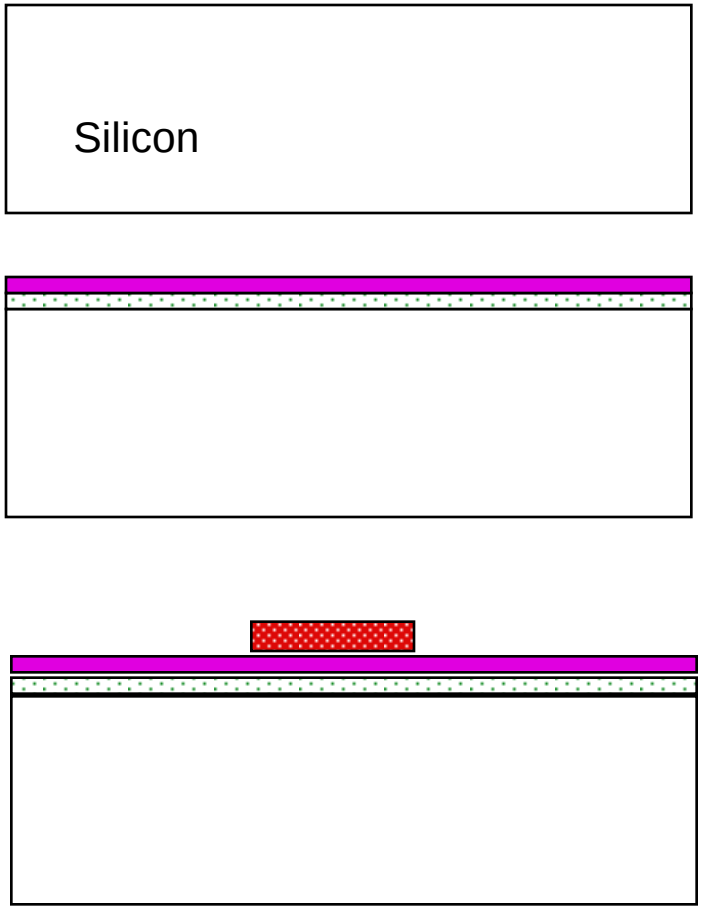
Oxides in the MOS Process

- Initial Oxide
  - **implant barrier against subsequent implants**
  - **or a diffusion barrier against furnace doping**
- Gate Oxide
  - **the most critical oxide in a MOS process**
    - **plays a large part in setting the electrical characteristics**
- Field Oxides
  - **thick oxides in the non-device areas**
  - **part of the isolation between devices**
  - **in modern processes are formed as LOCOS oxides**

Field Oxides
The LOCOS Process

- Field oxides are formed using a LOCOS process
- LOCOS
  - **Local Oxidation of Silicon**
- Silicon Nitride is used as a mask to prevent oxidation of the silicon in some areas
- This gives a semi-recessed structure
  - **1µm of oxide with a step height of approximately half that**

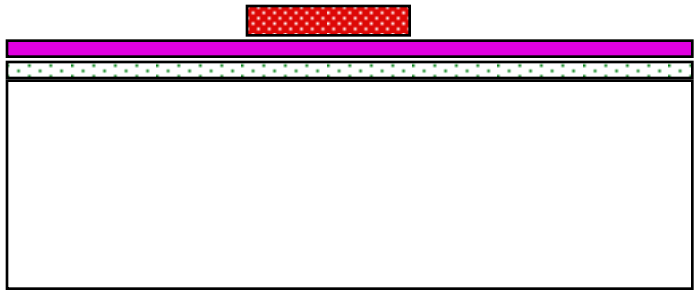
LOCOS or Semi Recessed Oxide



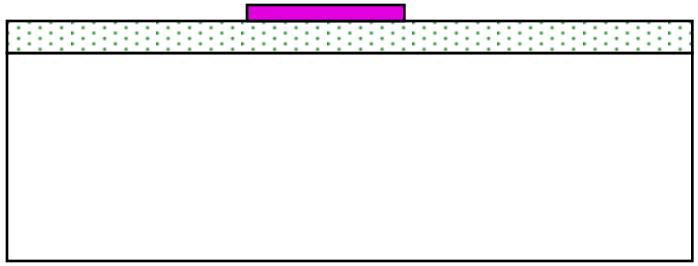
Deposit Silicon Nitride
Grow Thin Oxide

Pattern with
Photoresist

Thermal Oxidation

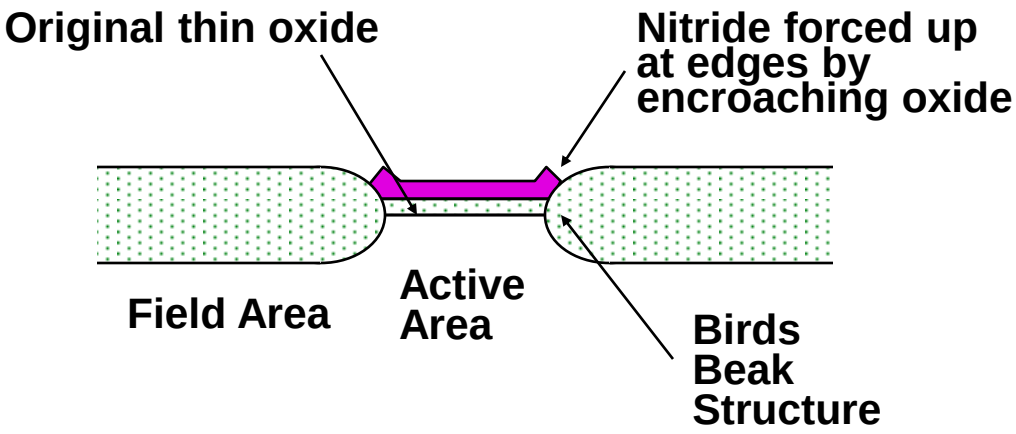


Etch unprotected nitride

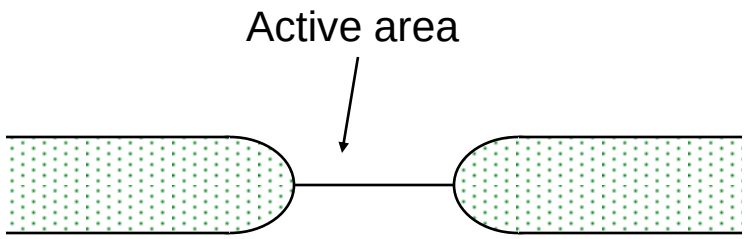


Remove the Resist
Leaving nitride pad on thin oxide

Grow the field oxide



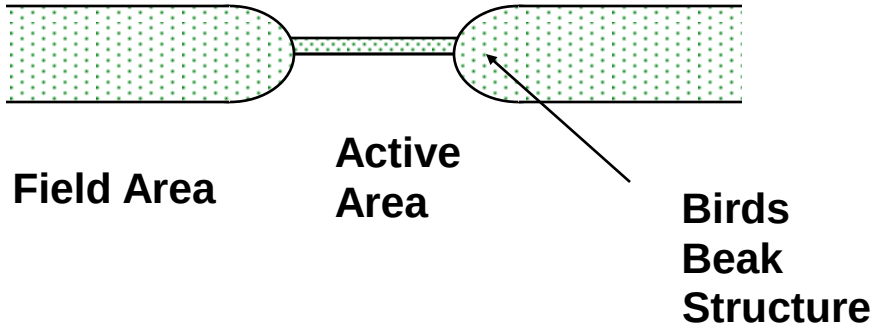
Strip the nitride and the thin oxide



Semi-recessed
Field Oxide

Final LOCOS structure showing the birds beak, so called because of the shape.

The final structure after the SAC and gate oxidations



Traps

- Traps are defects in the structure of the silicon dioxide at the atomic level
- These defects can trap charge and raise the total charge level in the oxide
- Processing conditions can reduce the level of traps in the oxide

Addition of Chlorine

- Chlorine is often added in small quantities to the oxidising ambient to improve the overall quality of the oxides
  - **It improves the Dielectric strength of the oxide**
  - **Helps to passivate against ionic sodium contamination**
  - **Enhances minority carrier lifetime in the silicon**

Methods of Introducing Chlorine

- HCl
  - **low flow gas bleed into the furnace during oxidation**
- Trans-LC
  - **liquid source**
  - **carrier gas bubbled through the liquid**

Sodium Contamination in MOS Processes

- MOS processes are particularly susceptible to ionic contamination from elements in the alkali metal group
- Sodium is the main danger (Any alkali metal)
- This contamination manifests itself as shifts in the threshold voltage under temperature stress

Prevention and Detection

- Special handling precautions are needed to prevent contamination from humans to the furnace equipment
- All chemicals in the process chain must have low alkali metal content
- Water used in the cleaning process must have low ion content
- Mobile ions incorporated in the oxides can be detected using stressed CV techniques

Stressed CV Measurement

- By forming a capacitor using the thermal oxide as the dielectric and the silicon wafer as the lower plate of the capacitor the quality of the oxide can be assessed in terms of the quantity of charge incorporated in the oxide

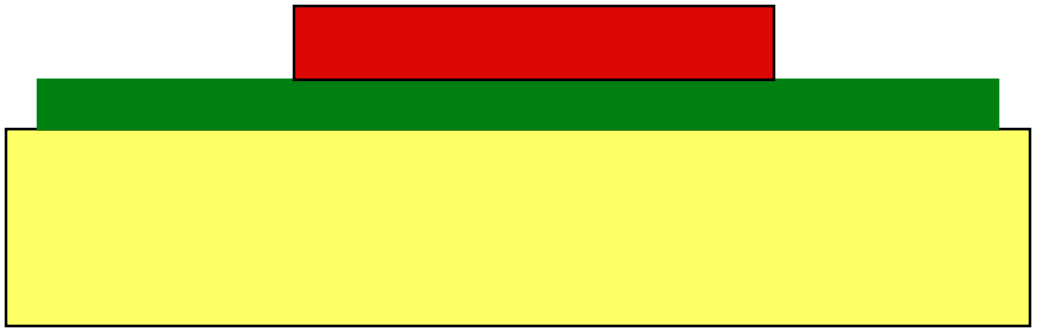
- The mobile ion content can be measured from one stress measurement

MOS Capacitor

Metal or Poly

Thermal Oxide

Silicon



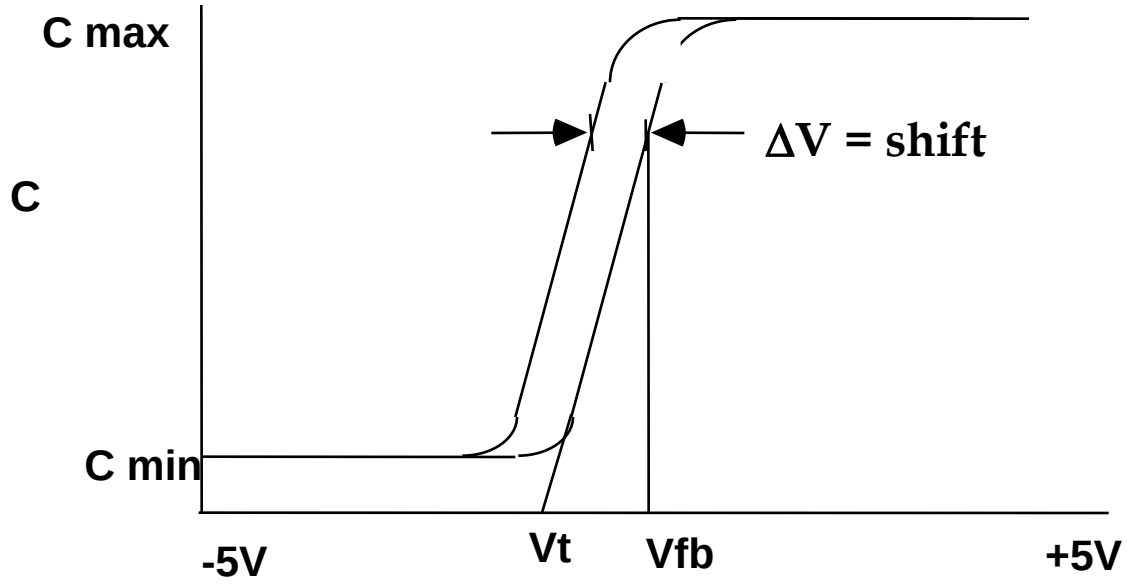
Stress CV Cycle

- Measure the CV at room temp, plot or save data
- Apply +ve bias to the top plate of the capacitor, proportional to the oxide thickness 1V/10nm
- Heat the sample up to 250°C and hold for 3 min

Stress CV Cycle II

- Cool the sample back to room temp
- Re-measure the CV
- Compare the two plots
- The level of shift in the plots is a measure of the degree of contamination

Capacitance Vs Voltage Plot



Capacitance versus Voltage Plot

Stressed CV Measurement II

- The fixed charge can be monitored by recording the flat band voltage over time
- Process conditions set the level of fixed charge
- Contamination or absence of contamination sets the level of mobile charge

Fixed Charge

- Fixed charge Qss
  - **contained within 20nm of the silicon /silicon dioxide interface**
  - **the level of fixed charge is set by the processing conditions, temp, gas ambient**
- It is only the last high temp stage that the oxide “sees” which effects the Qss

Qss Triangle