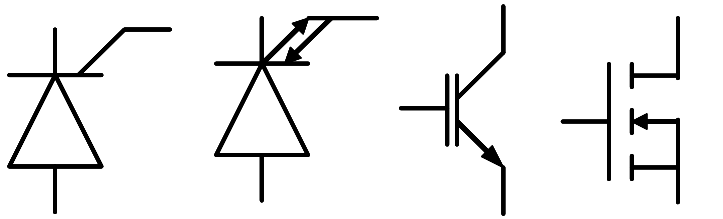
# Chapter 2

# DESIGN OF SWITCHING POWER-POLES

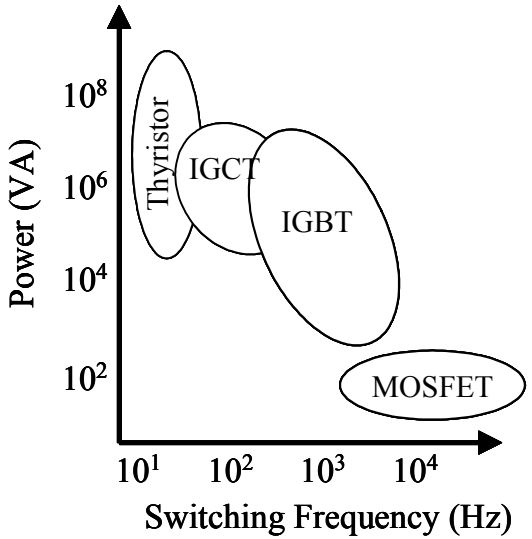
# POWER TRANSISTORS AND POWER DIODES

- Voltage Rating
- Current Rating
- Switching Speeds
- On-State Voltage

# SELECTION OF POWER TRANSISTORS




(a)




(b)

- MOSFETs
- IGBTs
- IGCTs
- GTOs
- Niche devices: BJTs, SITs, MCTs

# MOSFETs

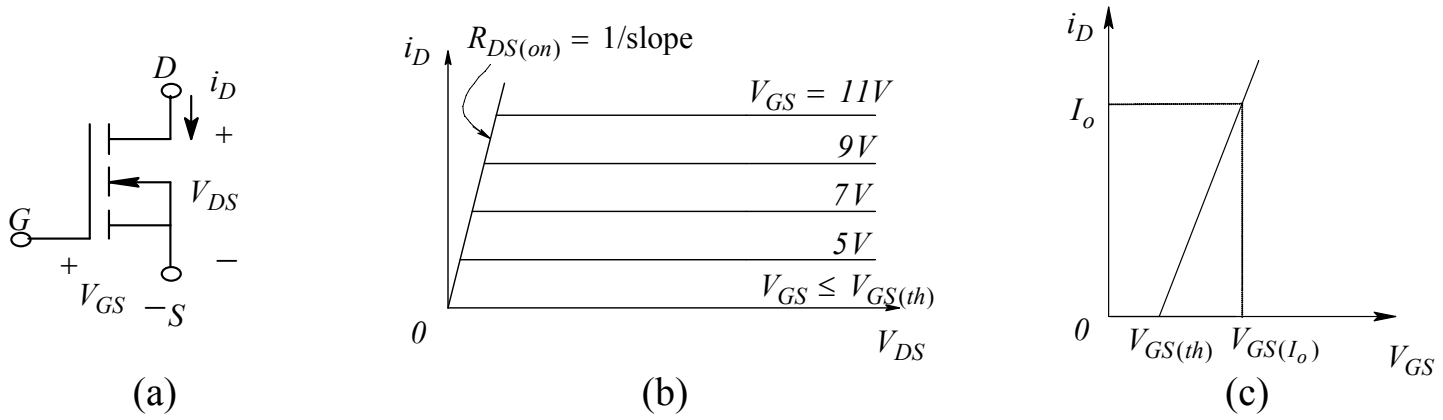



Figure 2-1 MOSFET: (a) symbol, (b) *i-v* characteristics, (c) transfer characteristic.

$$R_{DS(on)} \alpha V_{DSS}^{2.5 to 2.7}$$

# IGBTs

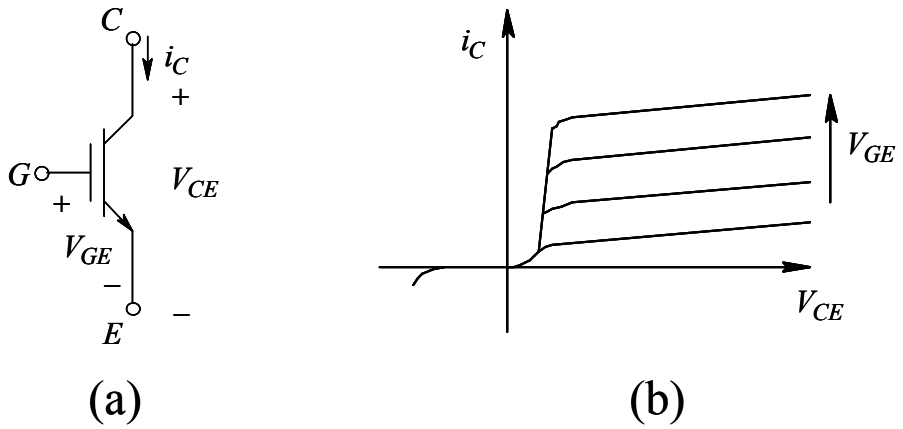
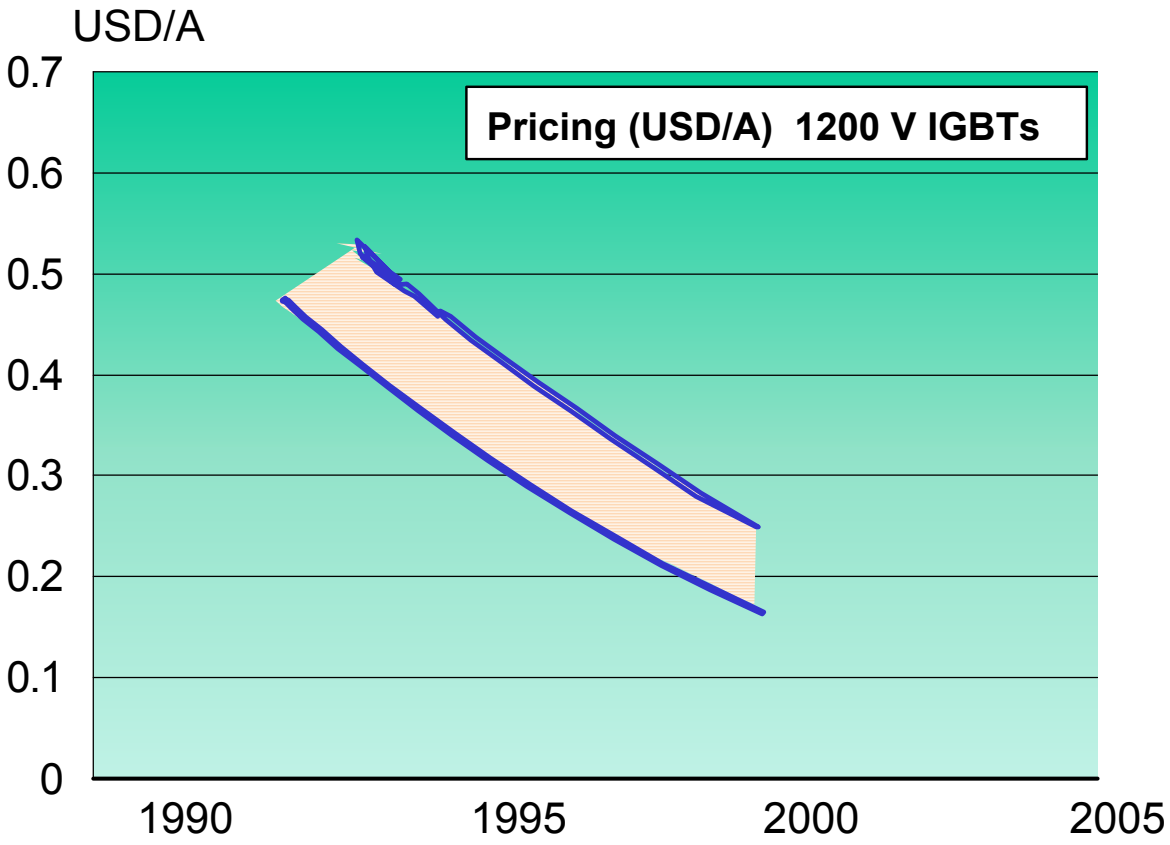



Figure 2-2 IGBT: (a) symbol, (b) *i-v* characteristics.

# Power-Integrated Modules and Intelligent-Power Modules

# Power Semiconductor Price Trends



# SELECTION OF POWER DIODES

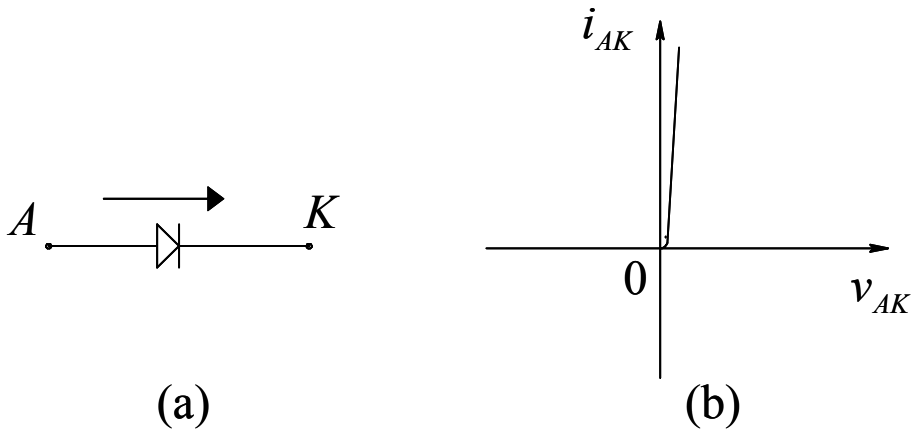



Figure 2-3 Diode: (a) symbol, (b) *i*-*v* characteristic.

- **Line-frequency diodes**
- **Fast-recovery diodes**
- **Schottky diodes**
- **SiC Schottky diodes**

# SWITCHING CHARACTERISTICS AND POWER LOSSES IN POWER-POLES

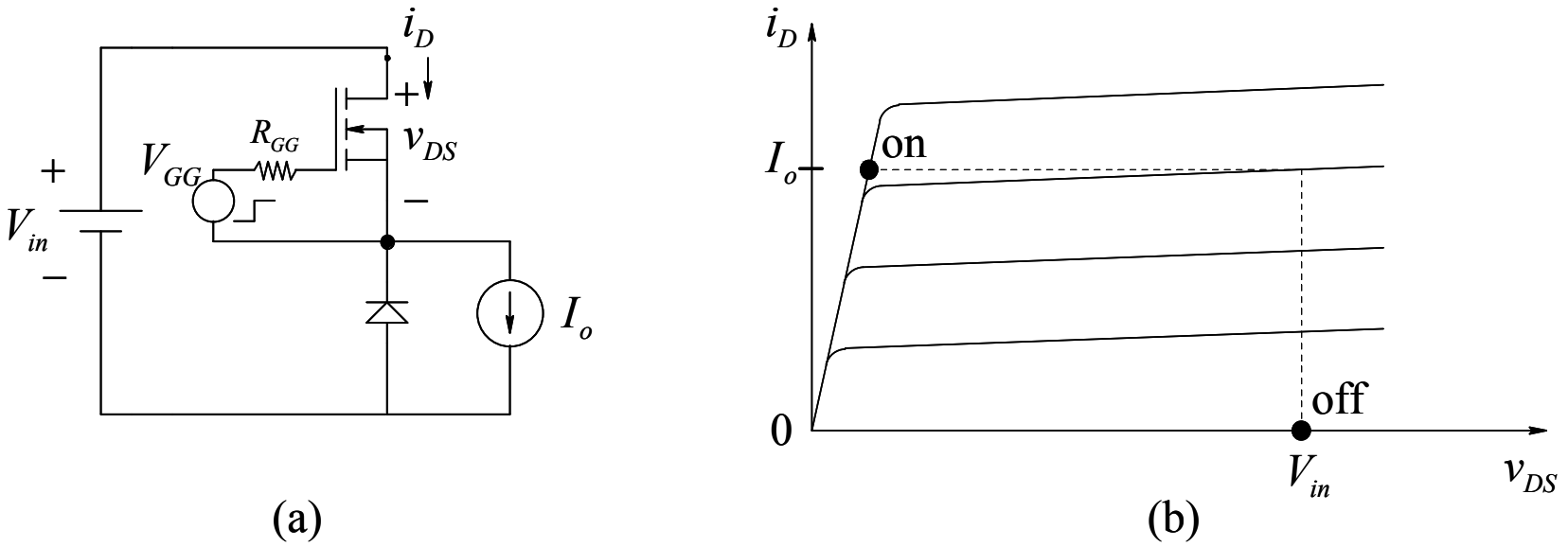



Figure 2-4 MOSFET in a switching power-pole.

# Turn-on Characteristic

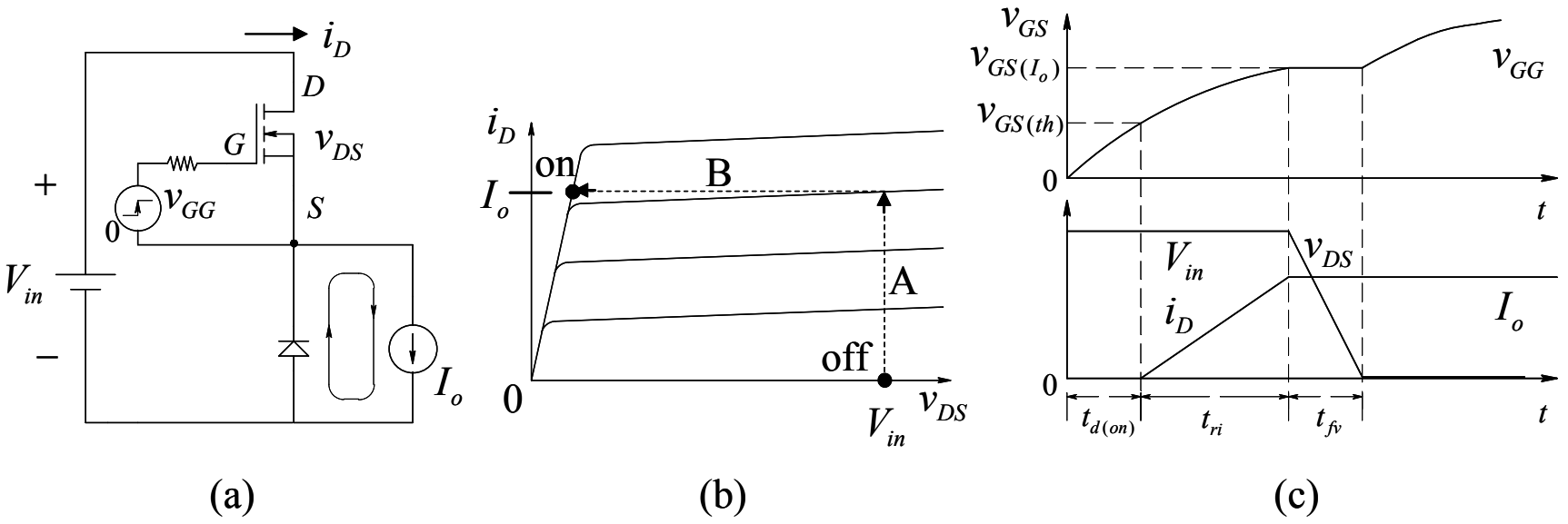



Figure 2-5 MOSFET turn-on.

# Turn-off Characteristic

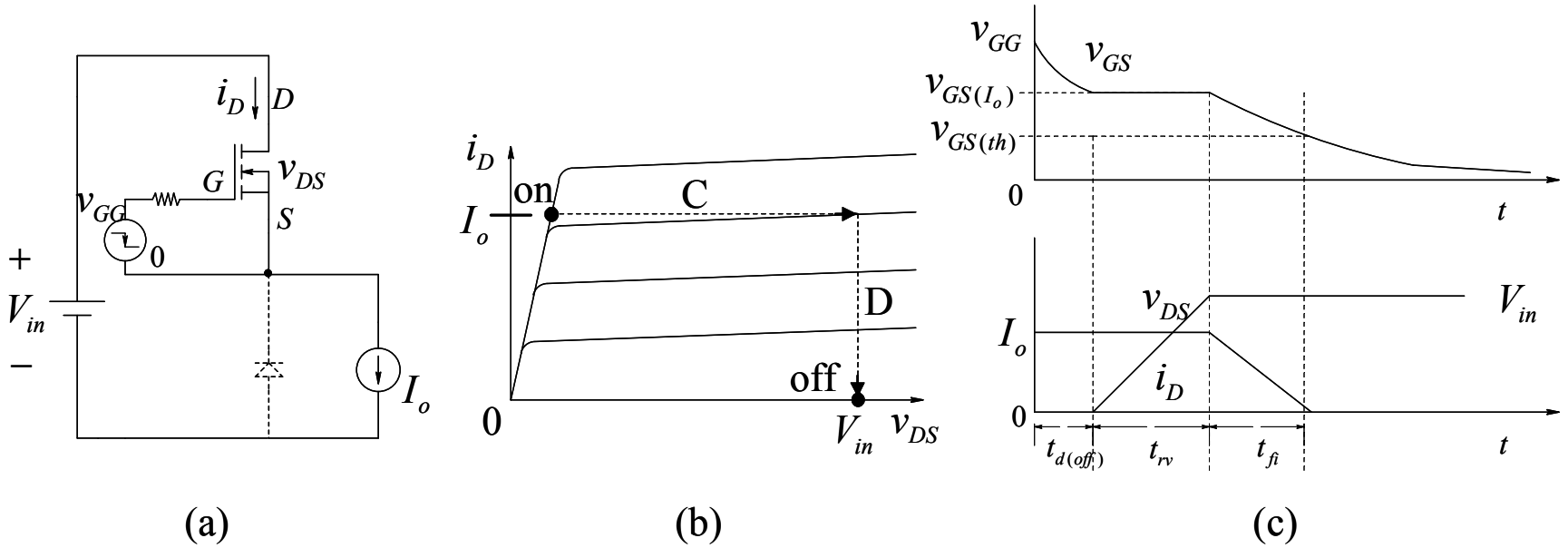
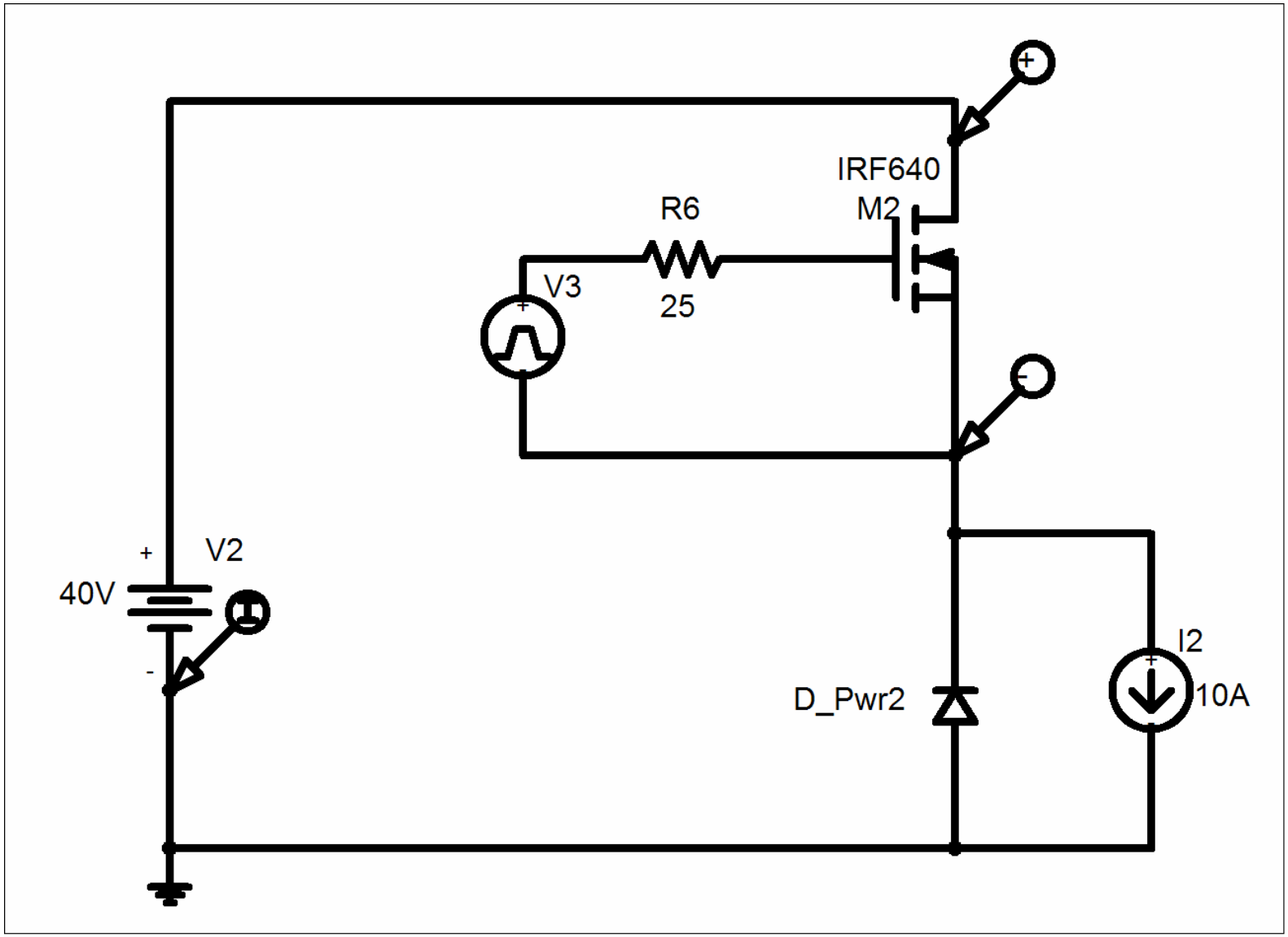
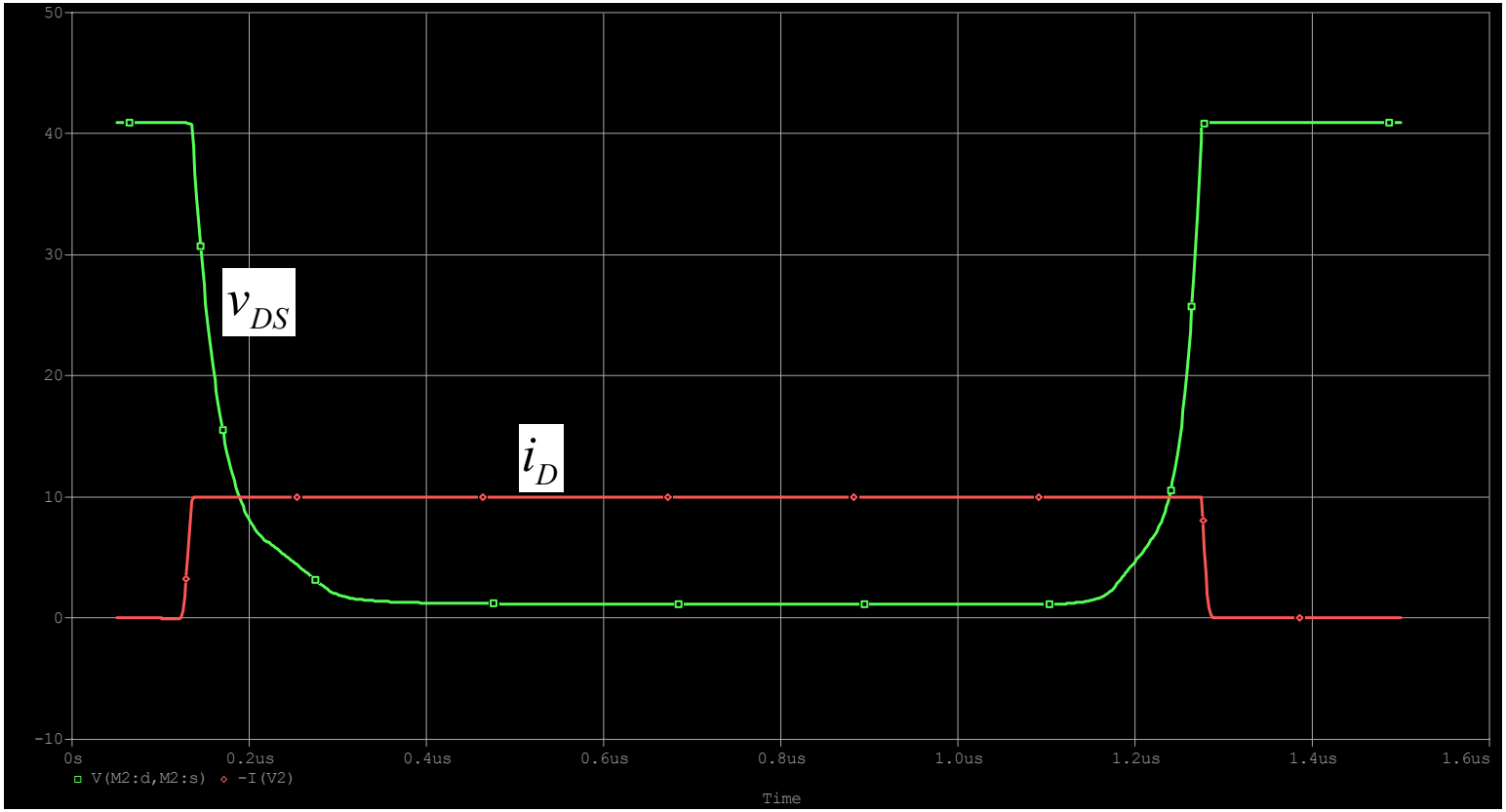



Figure 2-6 MOSFET turn-off.

# PSpice Modeling: C:\FirstCourse_PE_Book03\Power_pole_PSpice_Diode.sch



# Simulation Results: MOSFET Voltage and Current



# Calculating Power Losses Within the MOSFET (assuming an ideal diode)

**Conduction Loss:** $P_{cond} = d\, R_{DS(on)} I_o^2$

**Switching Losses:** $P_{sw} = \frac{1}{2} V_{in} I_o (t_{c,on} + t_{c,off}) f_s$

$t_{c,on} = t_{ri} + t_{fv}$

$t_{c,off} = t_{rv} + t_{fi}$

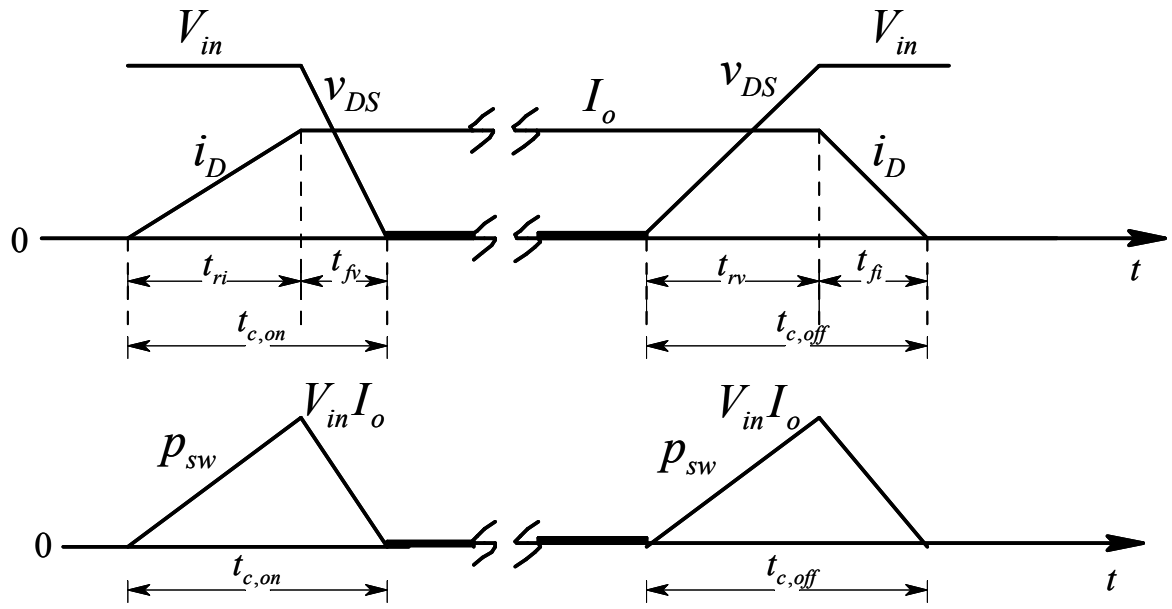



Figure 2-7 MOSFET switching losses.

# Gate Driver Integrated Circuits (ICs) with Built-in Fault Protection

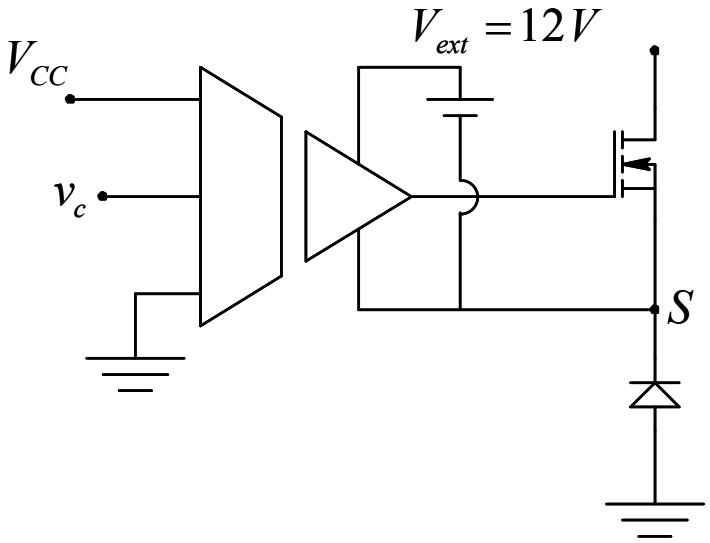



Figure 2-8 Gate-driver IC functional diagram.

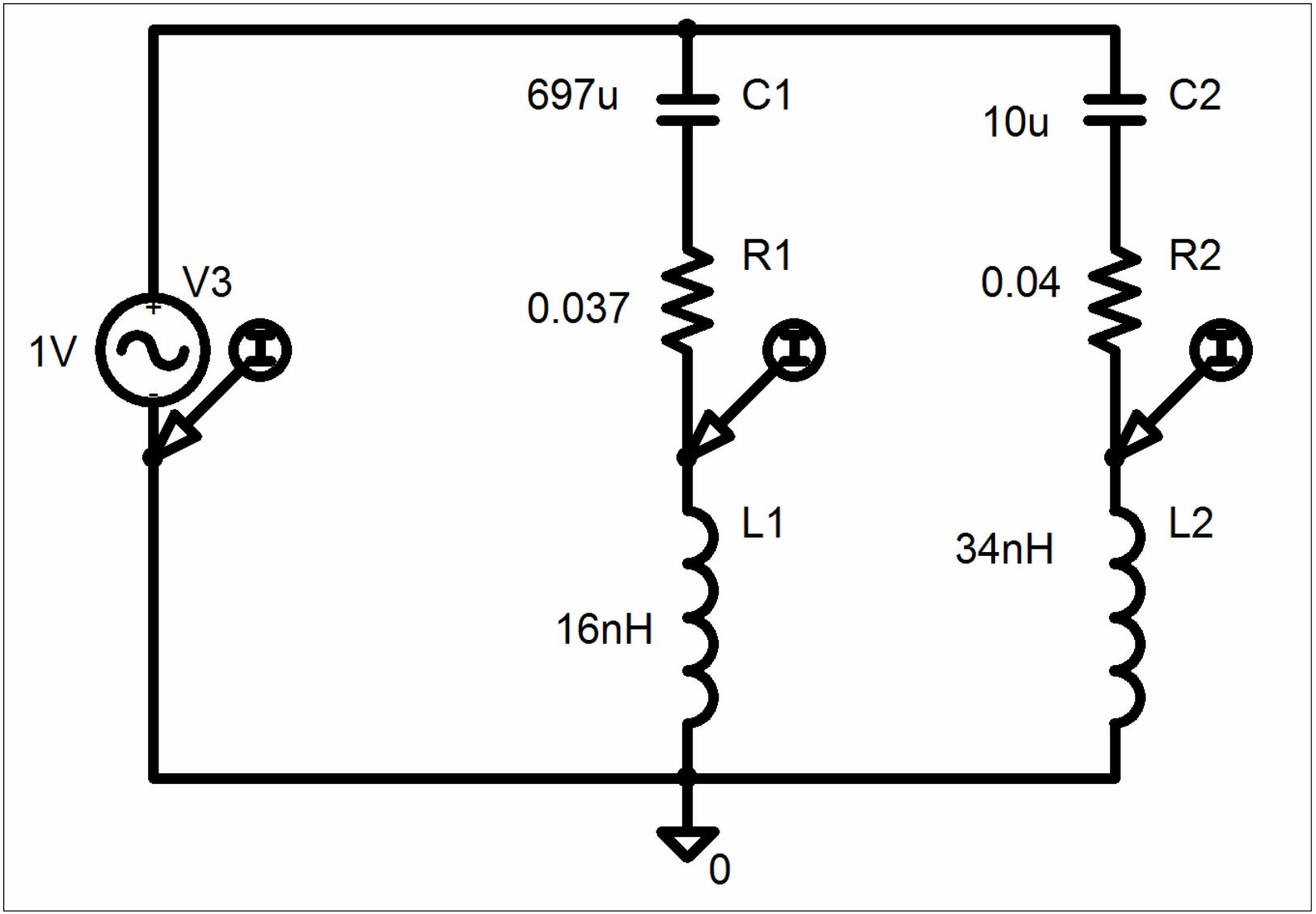
# JUSTIFYING SWITCHES AND DIODES AS IDEAL

# DESIGN CONSIDERATIONS

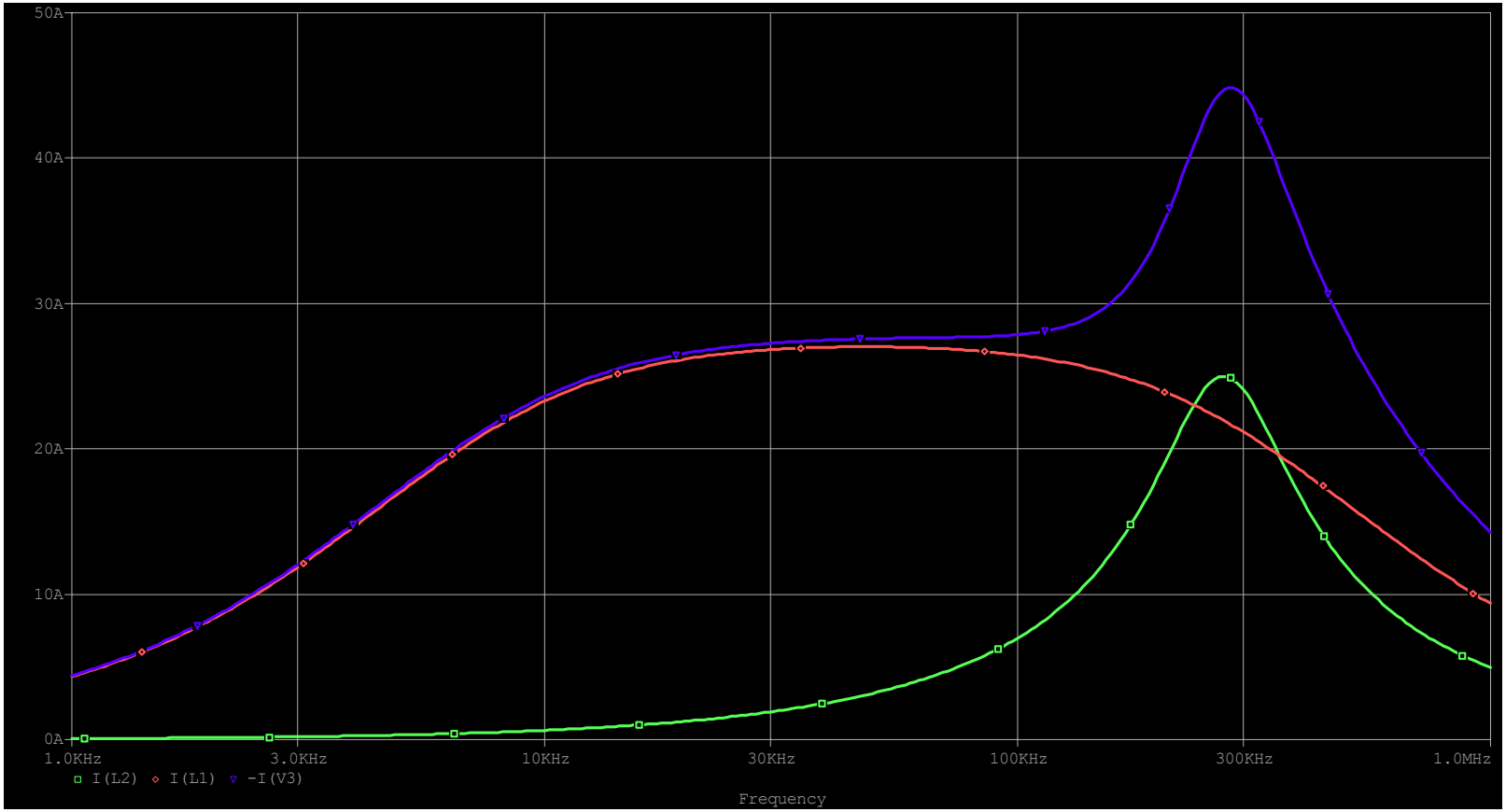
- **Switching Frequency**
- **Selection of Transistors and Diodes**
- **Magnetic components** $A_p = \dfrac{L\hat{I}I_{rms}}{k_w J_{\max} B_{\max}}$ $A_p = \dfrac{k_{conv}\sum V_y I_{y,rms}}{k_w B_{\max} J_{\max} f_s}$
- **Capacitor Selection**


Figure 2-9 Capacitor ESR and ESL.

# PSpice Modeling: C:\FirstCourse_PE_Book03\Capacitor_Characteristics.sch



# Simulation Results: Individual and Total Admittances



# Thermal Design

$$T_j = T_a + (R_{\theta jc} + R_{\theta cs} + R_{\theta sa})P_{diss}$$

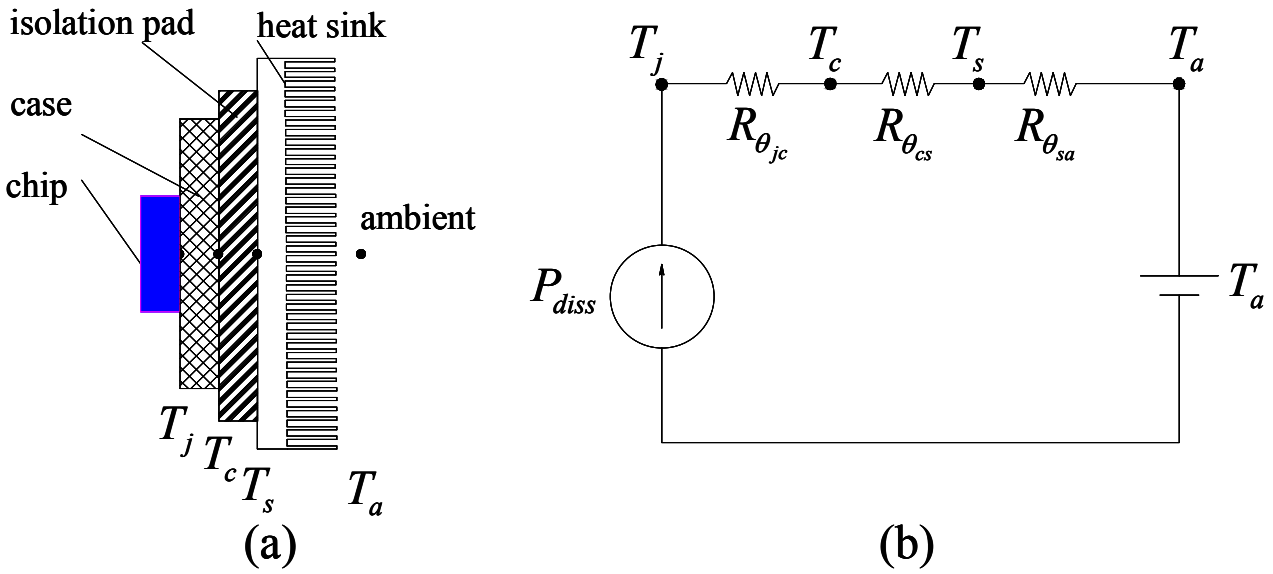



Figure 2-10 Thermal design: (a) semiconductor on a heat sink, (b) electrical analog.

# Design Tradeoffs

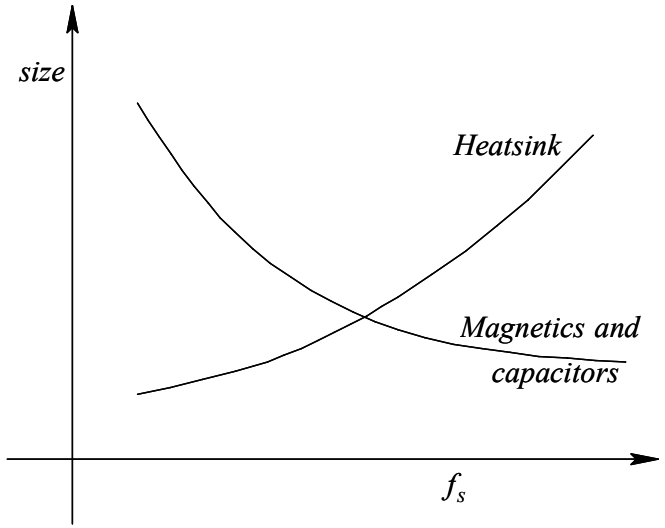



Fig. 2-12. The output switching signal represents the transistor switching function $q(t)$,

# PWM CONTROLLER IC

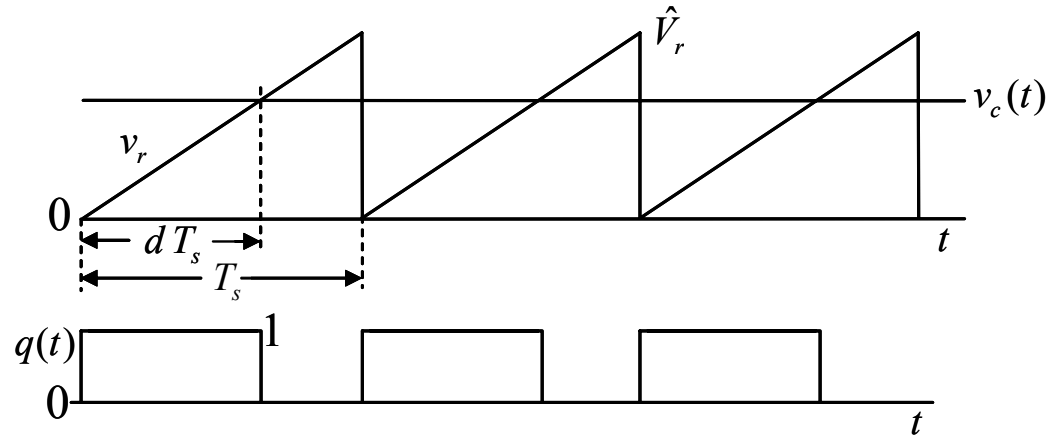



Figure 2-12 PWM IC waveforms.

$$d(t) = \frac{v_c(t)}{\hat{V}_r}$$

# APPENDIX 2A: Diode Reverse Recovery and Power Losses

**Diode Forward Loss:** $P_{diode,F} = (1-d)\cdot V_{FM} I_o$

**Diode Reverse Recovery Characteristic:**

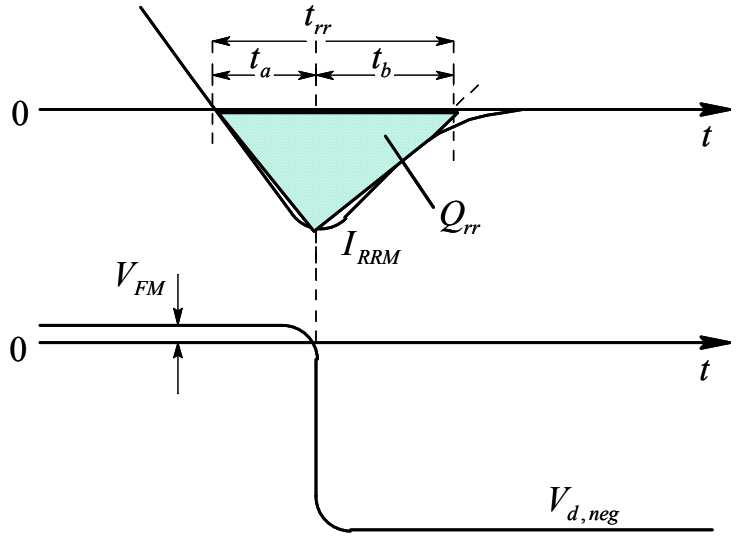
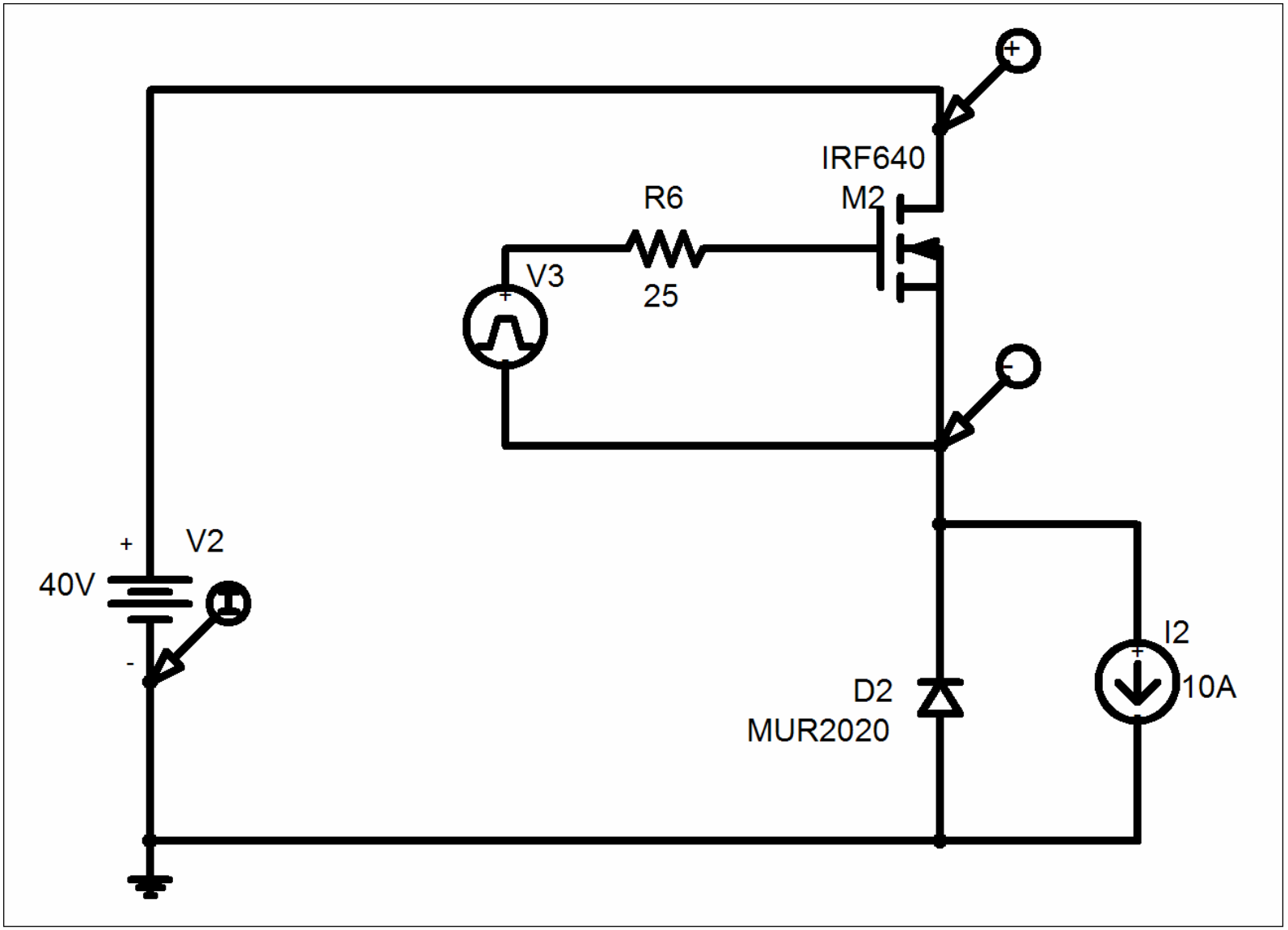



Figure 2A-1 Diode reverse recovery characteristic.

**Diode Switching Losses:** $P_{diode,sw} = (\frac{1}{2} I_{RRM} t_b)\cdot V_{d,neg}\cdot f_s$

# PSpice Modeling: C:\FirstCourse_PE_Book03\ Power_pole_PSpice_MUR2020.sch



# Simulation Results: MOSFET Voltage and Current