# UE4002 2005

Each part of each question carries equal marks.
The body effect may be ignored in each question.
The following equation is given for the drain current of an nmos in saturation:

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{tn})^2(1+\lambda_n V_{DS})$$

For dc biasing calculations take $\lambda_n=\lambda_p=0$.
In each question, capacitances other than those mentioned may be ignored.

### Question 1

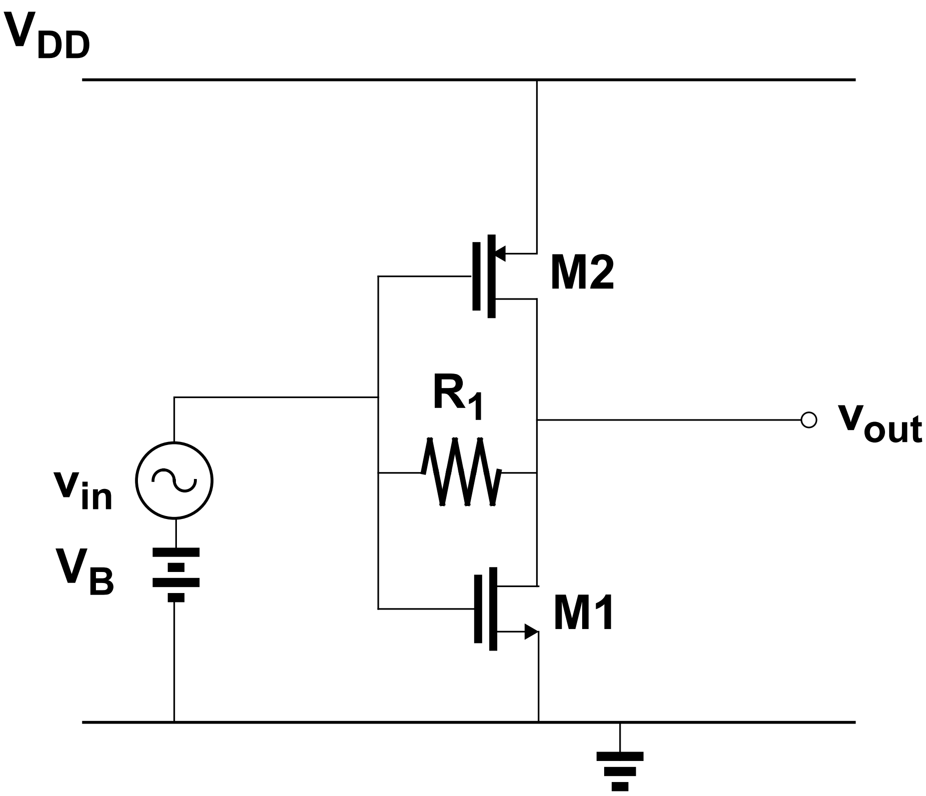



**Figure 1**

(i) Draw the small-signal equivalent circuit for the CMOS inverter stage shown in Figure 1.
(ii) Derive an expression for the small-signal voltage gain ($v_{out}/v_{in}$) in terms of the small-signal transistor parameters and $R_1$.
(iii) Calculate the small-signal gain if
$V_B$ = 1.5V, $V_{tn}$ = 0.7V, $V_{tp}$ = -0.7V, $\lambda_n = \lambda_p = 0.04V^{-1}$, $R_1$ = 5kΩ, $V_{DD}$ = 3V.
Assume both transistors are in saturation with a drain current of 200μA.
(iv) What is the value of the gain if $R_1$ is increased to 10kΩ?
What is the value of the gain if $R_1$ is increased to infinity?

**Question 2**

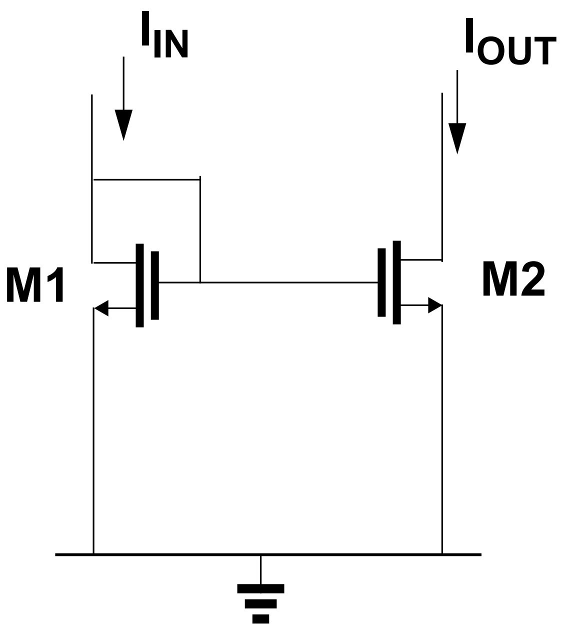



**Figure 2a**

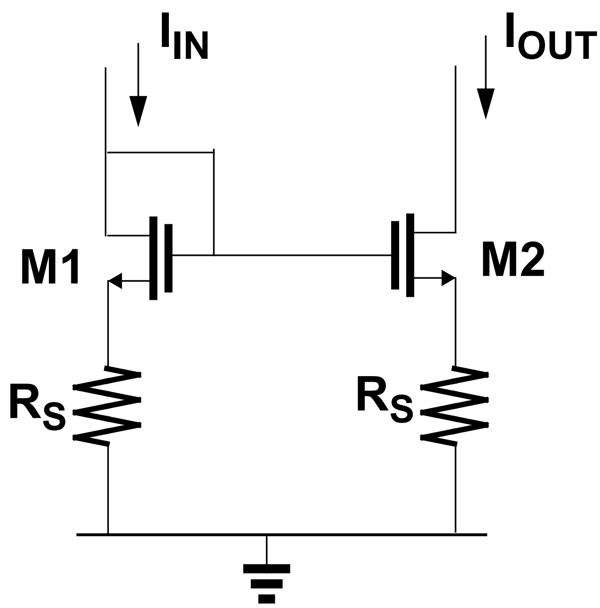



**Figure 2b**

For the current mirrors in Figure 1a and Figure 1b

$I_{IN} = I_{OUT} = 100\mu A$, $\lambda_n = 0.04V^{-1}$, $V_{GS1} = V_{GS2} = 1.2V$, $V_{tn} = 0.7V$, $R_S=10k\Omega$.

Assume all devices are in saturation and that $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$.

(i) What is the small-signal output resistance of the current mirror shown in Figure 2a in terms of the small-signal parameters of M2?

(ii) What is the variation in output current of the current mirror shown in Figure 2a if the voltage at the output node varies by 10mV?

(iii) Derive an expression for the output resistance of the current mirror shown in Figure 2b in terms of the small-signal parameters of M2 and the resistance $R_S$?

(iv) What is the variation in output current of the current mirror shown in Figure 2b if the voltage at the output node varies by 10mV?

**Question 3**

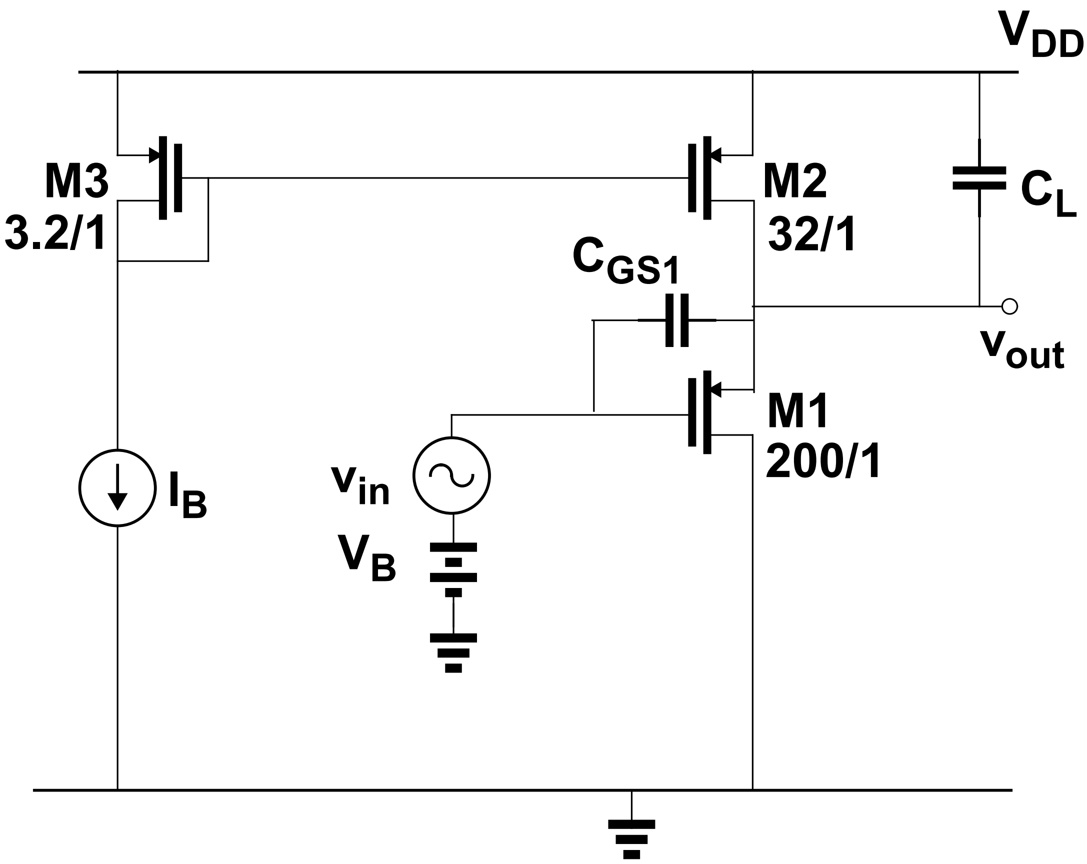



**Figure 3**

Figure 3 shows a pmos source follower. Assume all transistors are in saturation and $g_{m1}, g_{m2} >> g_{ds1}, g_{ds2}$.

(i) Draw the small-signal equivalent circuit for the source follower stage shown in Figure 3.

(ii) Ignoring all capacitances except $C_{GS1}$ and $C_L$ derive an expression for the high frequency transfer function.

(iii) Calculate the dc gain in dB, and the pole and zero frequencies, if $K_p{}' = 50\mu A/V^2$, $I_B = 20\mu A$, $C_{GS1} = 1pF$, $C_L = 9pF$. W/L in $\mu m$ for each transistor is as indicated in Figure 3.

(iv) Draw a Bode diagram of the gain. On the diagram indicate the pole and zero frequencies, the value of the dc gain in dB, and the value of the gain at frequencies well above the pole and zero frequencies.

**Question 4**

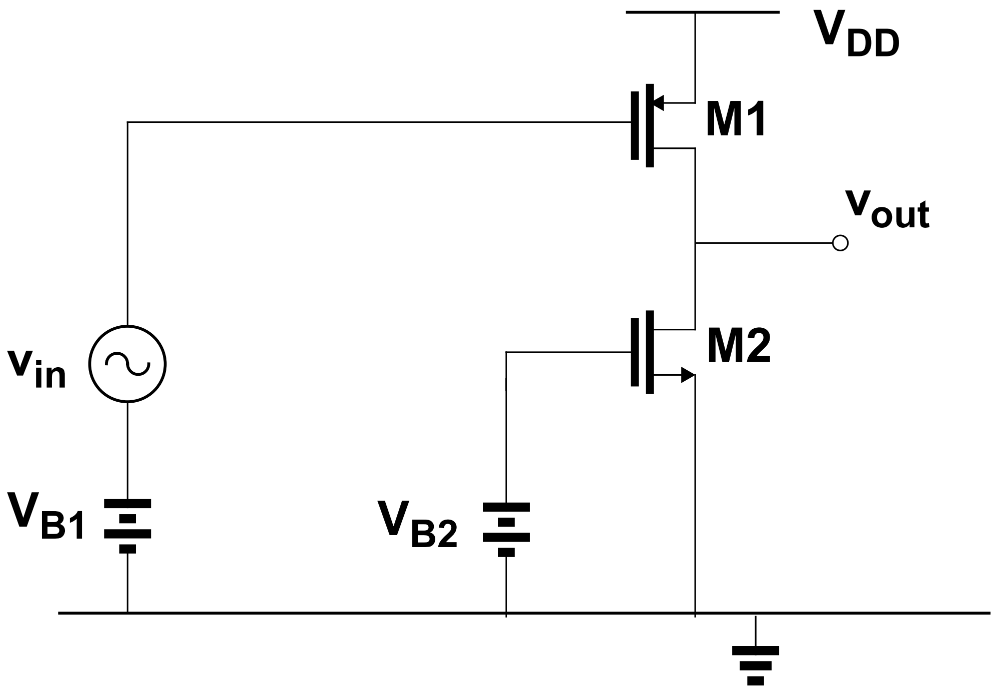



**Figure 4**

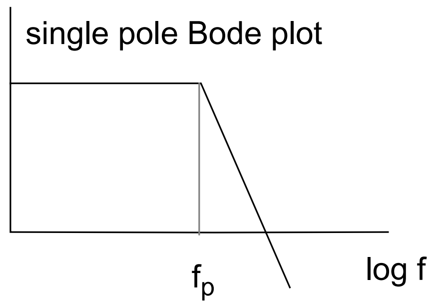
Assume M1 and M2 are operating in saturation. Only thermal noise sources need be considered.

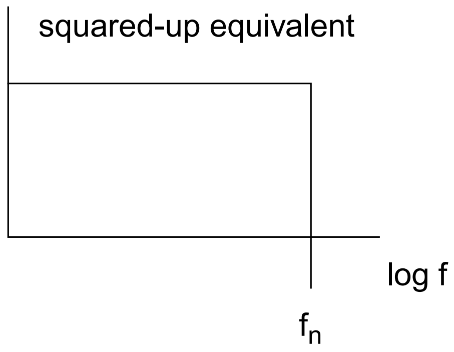
(i) What is the low-frequency small-signal voltage gain ($v_{out}/v_{in}$) of the circuit shown in Figure 4?

(ii) What is the input-referred thermal noise voltage in terms of the small-signal parameters of M1 and M2, Boltzmann's constant k and temperature T?

(iii) If a capacitor $C_L$ is connected between the output node and ground what is the total integrated thermal noise at the output node?

You may assume the following:




For the area underneath the curves to be the same then $f_n=(\pi/2)*f_p$

(iv) It is desired to limit the bandwidth such that a signal-to noise ratio of 40dB is achieved at the output, when the input is a 1mVrms sine wave with a frequency much lower than the frequency of the pole at the output node. Using the result of (iii) calculate the minimum value of $C_L$ required.
For this calculation take $V_{B1}$ = 2.0V, $V_{B2}$ = 1.0V, $V_{DD}$ = 3V, $V_{tn}$ = 0.75V, $V_{tp}$ = -0.75V,
$\lambda_n = \lambda_p = 0.04V^{-1}$.
The drain current of M1 is 100µA.
Assume Boltzmann's constant k=$1.38X10^{-23}$J/$^o$K, temperature T=300$^o$K.