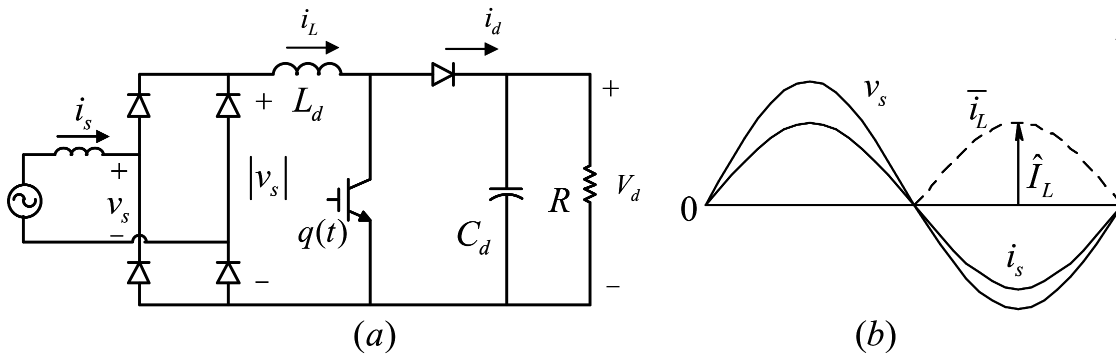
Chapter 6

POWER-FACTOR-CORRECTION (PFC) CIRCUITS AND DESIGNING THE FEEDBACK CONTROLLER

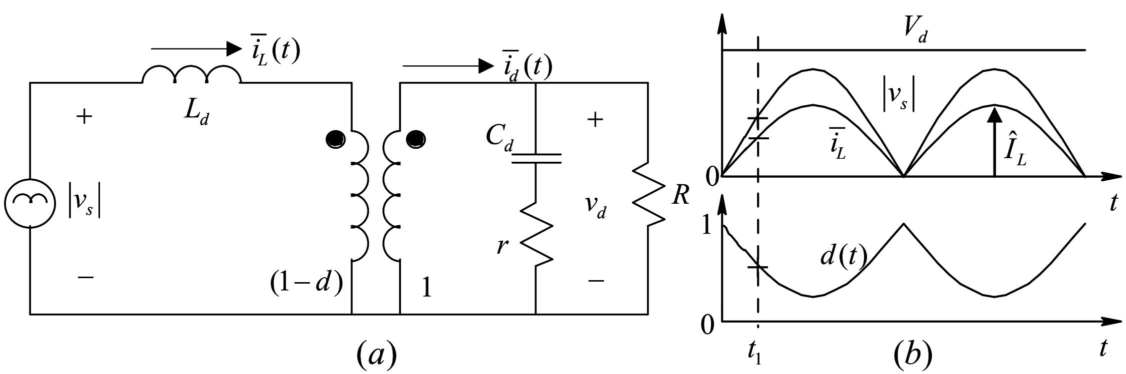
Implementation of PFC

- ❑ Use a boost dc-dc converter to shape the rectified current



$$V_d > \hat{V}_s$$

Figure 6-1 PFC circuit and waveforms.



$$\frac{V_o}{|v_s|} = \frac{1}{1-d(t)}$$

$$\therefore \; d(t) = 1 - \frac{\hat{V}_s |sin(\omega t)|}{V_o}$$

Figure 6-2 Average model and waveforms.

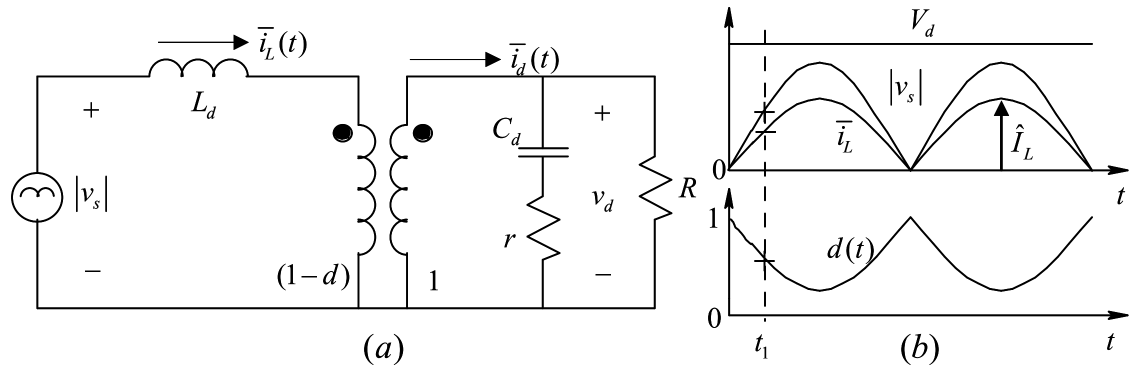


Figure 6-2 Average model and waveforms.

$$d(t) = 1 - \frac{\hat{V}_s |\sin(\omega t)|}{V_o}$$

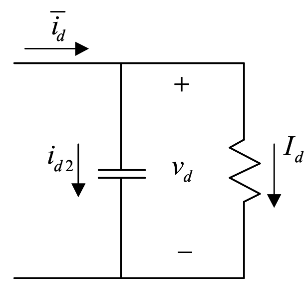


Figure 6-3 Current division in the output stage.

$$\overline{i}_d = \underbrace{\frac{1}{2}\frac{\hat{V}_s}{V_d}\hat{I}_L}_{I_d} - \underbrace{\frac{1}{2}\frac{\hat{V}_s}{V_d}\hat{I}_L \cos 2\omega t}_{i_{d2}(t)}$$

$$v_{d2} = -\frac{1}{\omega C}\frac{\hat{I}_L}{2}\frac{\hat{V}_s}{V_d}\int \cos 2\omega t \cdot d(\omega t) = -\underbrace{\left(\frac{\hat{I}_L \hat{V}_s}{4\omega C V_d}\right)}_{\hat{V}_{d2}} \sin 2\omega t$$

$$\hat{V}_{d2} = \frac{\hat{I}_L}{4\omega C}\frac{\hat{V}_s}{V_d}$$

CONTROL OF PFCs

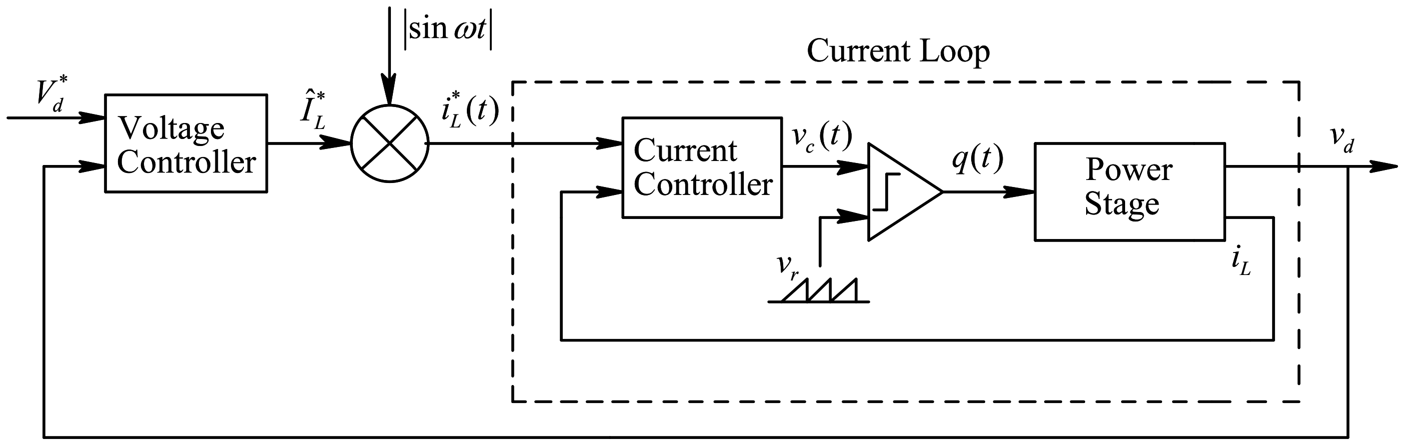


Figure 6-4 PFC control loops.

DESIGNING INNER AVERAGE-CURRENT-CONTROL LOOP

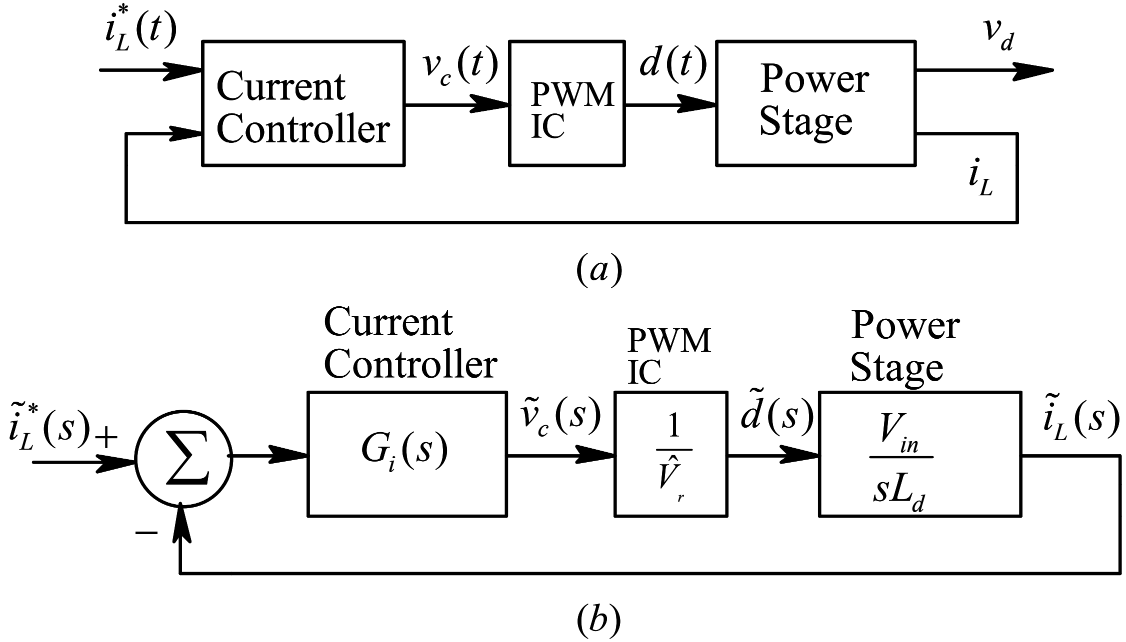


Figure 6-5 PFC current loop.

PWM-IC: $$\frac{\tilde{d}(s)}{\tilde{v}_c(s)} = \frac{1}{\hat{V}_r}$$

Power-Stage: $$\frac{\tilde{i}_L(s)}{\tilde{d}(s)} = \frac{V_d}{sL_d}$$

Controller: $$G_i(s) = \frac{k_c}{s}\underbrace{\frac{1+s/\omega_z}{1+s/\omega_p}}_{\text{phase boost}}$$

$$K_{boost} = \tan(45^o + \frac{\phi_{boost}}{2})$$

$$f_z = \frac{f_{ci}}{K_{boost}} \qquad f_p = K_{boost} f_{ci} \qquad k_c = \omega_z \left|G_C(s)\right|_{f_c}$$

DESIGNING THE OUTER VOLTAGE LOOP

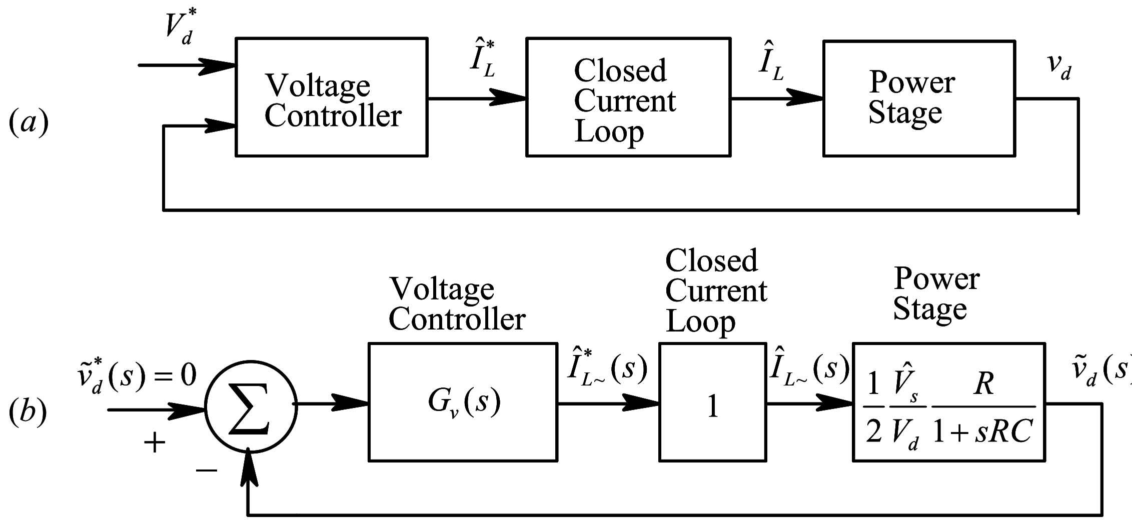


Figure 6-6 Voltage control loop.

$$G_v(s) = \frac{k_v}{1 + s/\omega_{cv}}$$

$$\left| \frac{k_v}{1+s/\omega_{cv}} \frac{1}{2} \frac{\hat{V}_s}{V_d} \frac{R}{1+sRC} \right|_{s=j\omega_{cv}} = 1$$

$$\left| \frac{k_v}{1+s/\omega_{cv}} \right|_{s=j(2\pi\times 120)} = \frac{\hat{I}_{L2}}{\hat{V}_{d2}}$$

EXAMPLE OF SINGLE-PHASE PFC SYSTEMS

Table 6-1

Parameters and Operating Values

Nominal input ac source voltage, $V_{s,rms}$	$120V$
Line frequency, f	60 Hz
Output Voltage, V_d	$250V$ (dc)
Maximum Power Output	$250W$
Switching Frequency, f_s	$100kHz$
Output Filter capacitor, C	$220\,\mu F$
ESR of the Capacitor, r	$100m\Omega$
Inductor, L_d	$1mH$
Full-Load Equivalent Resistance, R	250Ω

Design of the Current Loop

$$\hat{V}_r = 1 \qquad \phi_{PM} = 60^0 \qquad \omega_{ci} = 2\pi \times 10^4$$

$$G_i(s) = \frac{k_c}{s} \underbrace{\frac{1 + s/\omega_z}{1 + s/\omega_p}}_{\text{phase boost}}$$

$$k_c = 4212$$

$$\omega_z = 1.68 \times 10^4 \, rad/s$$

$$\omega_p = 2.34 \times 10^5 \, rad/s$$

DESIGNING THE OUTER VOLTAGE LOOP

$$G_v(s) = \frac{k_v}{1 + s/\omega_{cv}}$$

In this example at full-load, the plant transfer function given by Eq. 6-15 has a pole at the frequency of 18.18 rad/s (2.89 Hz). At full-load, $\hat{I}_L = 2.946\,A$, and in Eq. 6-8, $\hat{V}_{d2} = 6.029\,V$. Based on the previous discussion, the second-harmonic component is limited to 1.5 percent of $\hat{I}_L$, such that $\hat{I}_{L2} = 0.0442\,A$. Using these values, from Eq. 6-17 and 6-18, the parameters in the voltage controller transfer function of Eq. 6-16 are as follows: $k_v = 0.0722$, and $\omega_{cv} = 76.634\, rad/s$ (12.2 Hz).

$$G_v(s) = \frac{k_v}{1 + s/\omega_{cv}}$$

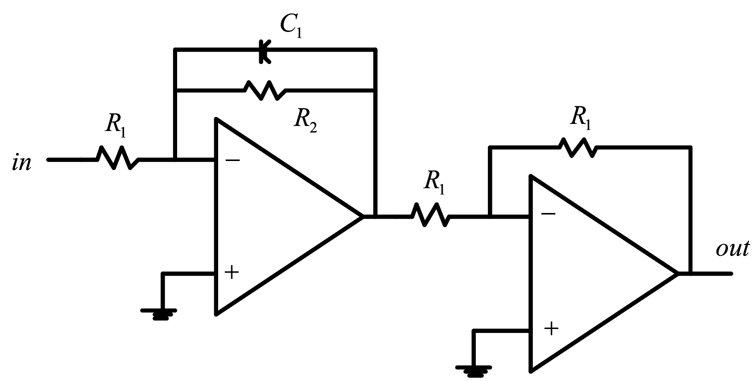
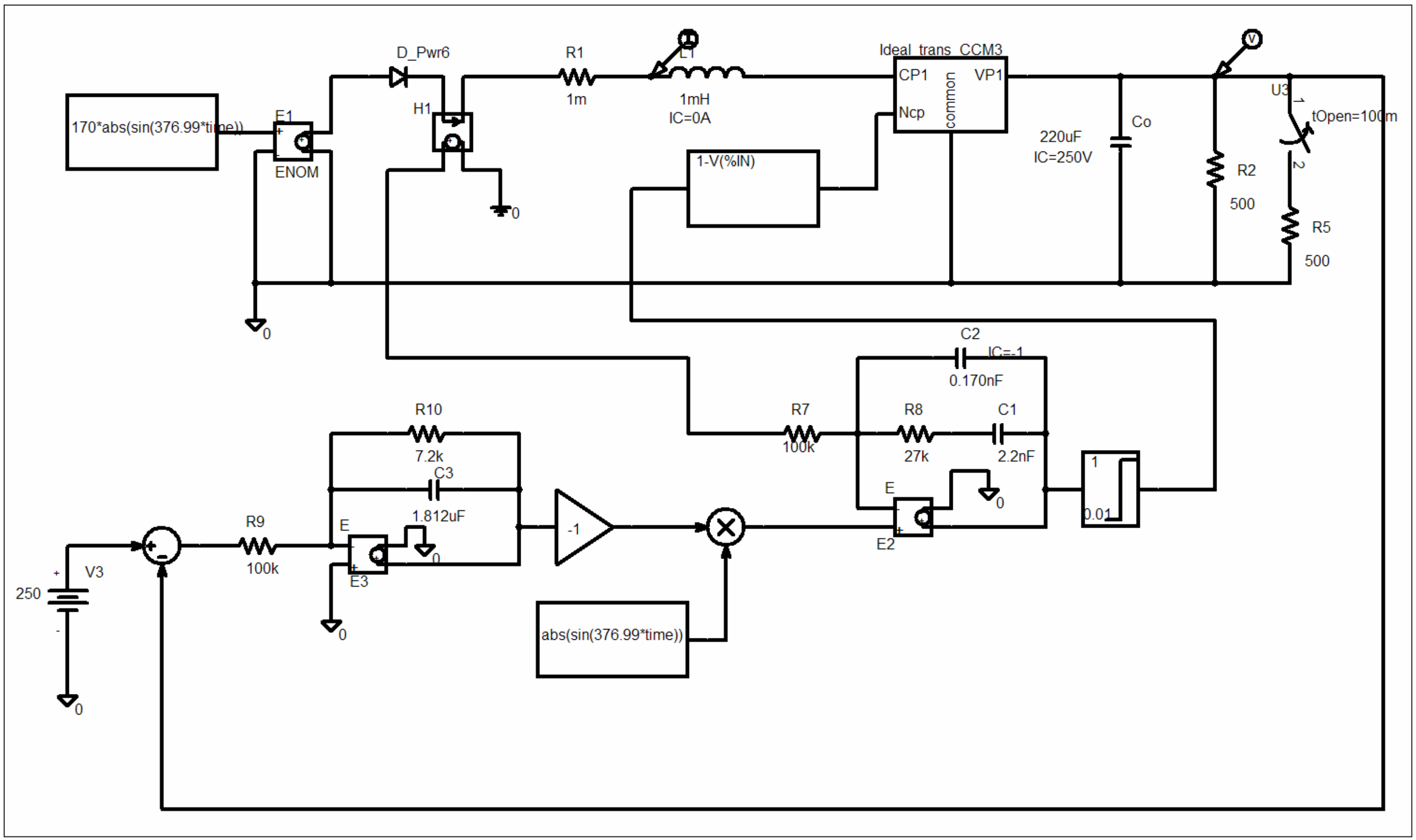


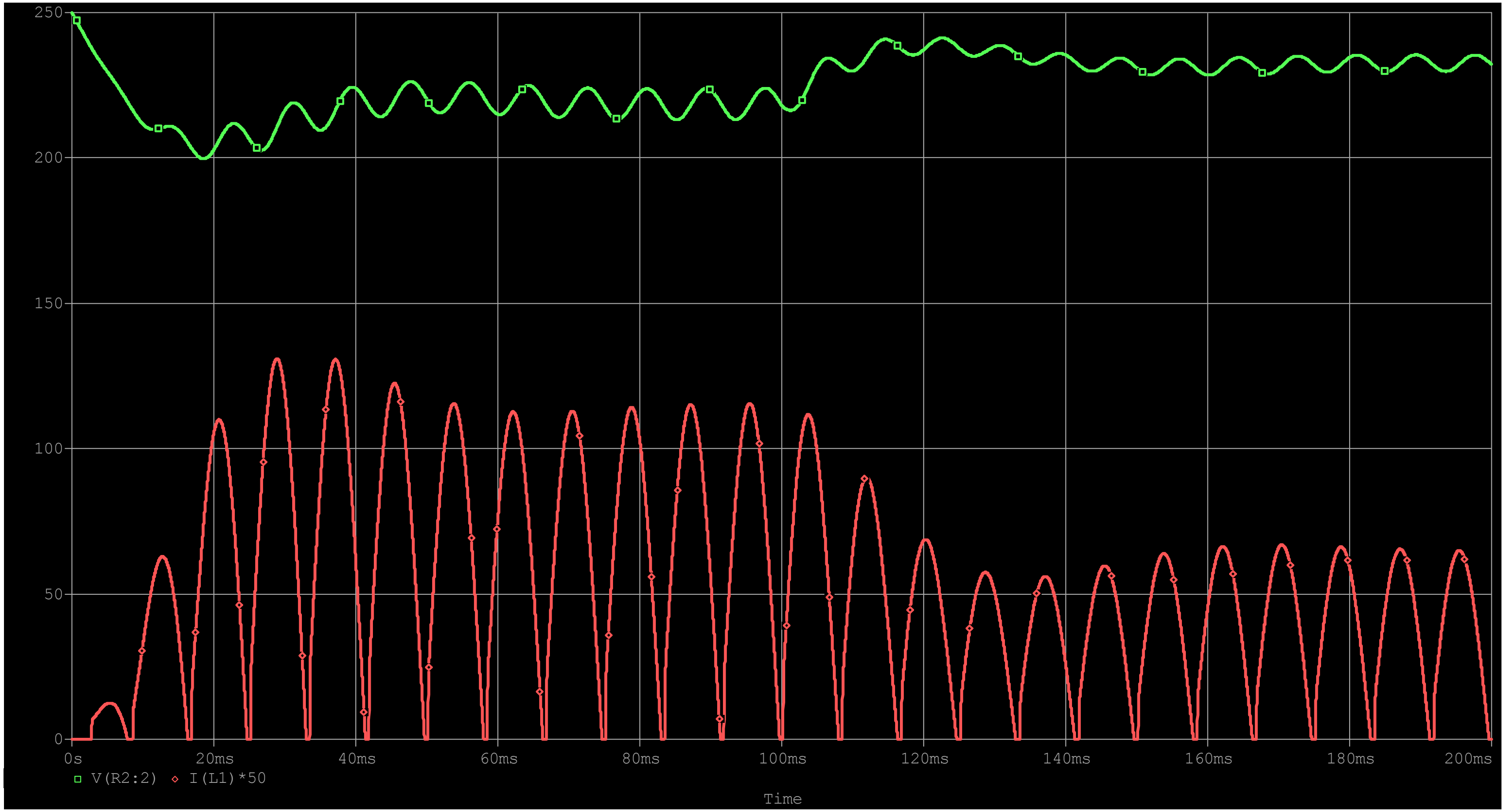
Figure 6-7 Op-amp circuit to implement transfer function $G_v(s)$.

$$R_1 = 100\,k\Omega$$
$$R_2 = 7.2\,k\Omega$$
$$C_1 = 1.8\,\mu\text{F}$$

PSpice Modeling: C:\FirstCourse_PE_Book03\pfc__Avg_opm.sch



Simulation Results



FEEDFORWARD OF THE INPUT VOLTAGE

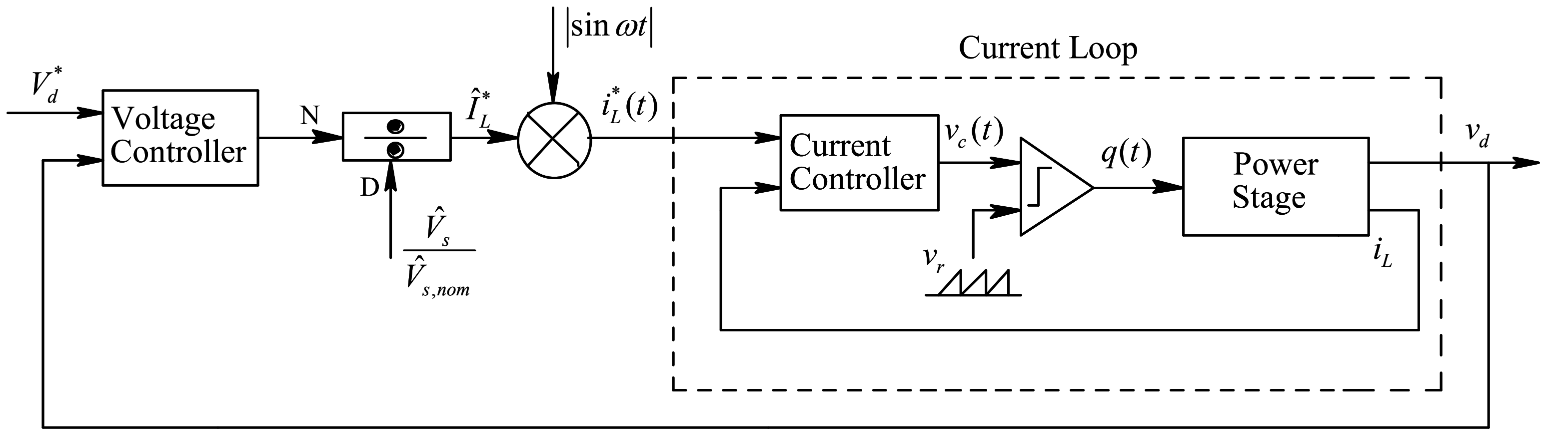


Figure 6-10 Feedforward of the input voltage.