Contact

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Top Skills

Perl
DFT
Static Timing Analysis

Steve Tung

Senior Staff Test Engineer at NXP
Selangor

Experience

2008
Senior Staff Product Engineer
February 2008 - Present (13 years 11 months)

DFT and Test consultant in New Product Introduction (NPI) team.
Qualified and delivered production test programs for automotive products (microcontrollers), network processors and sensor products, including a C90 pioneering product into Japanese market in collaboration with ST Microelectronics.
Review DFT features of NPIs and feedback to core development site; in focusing to introduction of new DFT techniques, test time reduction opportunities, and ensuring test programs meeting manufacturing requirements. This includes enhancements in Power/Ground pins continuity testing, express JTAG interface, and new ADC BI techniques.
Setup the TPC-VT (Test Program Conversion - Virtual Testing) infrastructure that was transferred from India Design Center to KLM (Freescale Malaysia).
Lectures DFT Trainings to product and test engineers in KLM.

Intel Corporation
6 years 5 months

Senior Component Design Engineer
June 2003 - January 2008 (4 years 8 months)

DFT owner and PCIe DFx lead for the MCH, codename Eaglelake and Bearlake of Intel chipsets.
Responsible to deliver the state of the art DFT features to be used by High-Volume Manufacturing (HVM), and silicon debug. Highly involved in architectural definitions include High-Speed IO testing, Scan, at-speed Scan, Self Heating Burn-in, Boundary Scan, observability, structural and BIST testing for all interfaces in the MCH with extensive interaction with Product Engineers.
Strong knowledge on ASIC design and validation flow, from architectural definition to Tape-out, and to Production. Related soft skill sets include driving weekly meetings, risk management, project and time management, efficient cross-site working model, and junior training.
DFT lead for Enterprise South Bridge 2 (ESB2), an integrated chip of MCH and ICH for embedded server market. Expert in DFx features for high speed

interfaces e.g. PCI-express, SATA II, and USB2, and other structural testing. Successfully implemented the unified clocking scheme for BI that saved Intel USD1.3M. Familiar with post-Si debug using S9K tester together with Product Development Engineers.

Hardware Design Engineer
September 2001 - June 2003 (1 year 10 months)
Santa Clara, CA

Collateral owner of the PCI-Express (3GIO) IO cluster integration into the 4P-based Twin Castle chipset. Extensive design interaction with back-end and front-end designers in ACE group of EPG to meet design considerations such as quality of RTL coding, intra-block and inter-block timing, full chip and system validation, placement and route, various DFT features, ISCAN, burn-in, risks, deadline and milestones.

HEWLETT-PACKARD COMPANY
Hardware Design Engineer
January 2001 - September 2001 (9 months)
Cuptertino, CA

Direct involvement in post-silicon electrical validation of HPs top of the line enterprise superscalable server Superdome for its recent introduced PA-8700 processors. Familiarized with usage of digital analyzers, tester boards, and other post-silicon validation equipment. Exposed to broad range of server architectures of local and competitors.

Techincal Background

Test Program Development for automotive and network processor products.
DFT unit for Intel MCH which consists of controlling units for Scan, at-speed scan, Scan dump, SHBI, DACBIST, RAMBIST, IOBIST, Fuse, Process Monitoring, Channel Sharing, Straps, and other structural testing like All0/1/Z, Buffer Toggle, and XOR chain.
Owner of behavioral model of the PCI-Express IO cluster in a 4P-based chipset.
An offset auto-canceling Ping-Pong Operational Amplifier on Partially-Depleted SOI CMOS
Technology (Thesis work)
3.3 V Comparator on Partially-Depleted SOI CMOS Technology with sub-2ns propagation
delay

3.3 V Beta-Multiplier Reference on Fully-Depleted and Partially Depleted SOI CMOS
Technology

Rail-to-rail Input and Output Operational Amplifier with Class-AB Output Stage

Fully Pipelined 4-bit Adder and Multiplier using Domino Logic

Standard CMOS Static Random-access Memory Cell with Read and Write Capability

Education

MISSISSIPPI STATE UNIVERSITY MISS. STATE

Masters of Science, Electrical Engineering · (1999 - 2001)

MISSISSIPPI STATE UNIVERSITY MISS. STATE

Bachelor of Science; MS, Electrical Engineering · (1996 - 1998)

MISSISSIPPI STATE UNIVERSITY MISS. STATE

Bachelor of Science; MS, Computer Engineering · (1996 - 1998)

INTI COLLEGE

· (1994 - 1996)