Alex Kisil

he/him/his • alxkisil@gmail.com • (586) 321-6151 • alexkisil.com • Chicago, IL

WORK EXPERIENCE

Agita Labs **Ann Arbor, MI**

Lead Computer Engineer (Remote) *April 2022 - Present*

- Manage and mentor a team of four engineers in the agile development of TrustForge, Agita Labs' secure hardware enclave
- Design and iterate on TrustForge SDK and emulator to allow clients to trial our tech without needing HW access
- Maintain and document a 50,000+ line codebase (C++, SystemVerilog, Assembly, Node.js, Python) in AWS and Azure
- Present proposals, technical specs, and challenges to investors and potential partners to help secure over $4mil in funding
- Implement performance-critical C++ interfaces between HW and native SW libraries to facilitate practical user adoption

Computer Engineer (Onsite, Remote) *Jan 2019 - April 2022*

- Designed and built an FPGA-powered secure hardware enclave, custom ISA and SW programming framework to enable side-channel-proof encrypted computation
- Built hardware performance monitor and ciphertext cache to identify and reduce >70% of our latency at FPGA interfaces
- Created HW-accelerated encryption and data integrity modules, achieving secure computation without performance compromise
- Architect and build novel data hashing, IEEE754 floating point, and exception handling approaches under bit-granularity memory constraints leveraging open source library HardFloat

Qualcomm **San Diego, CA**

Software Engineering Intern *May 2018 - Aug 2018*

- Implemented OpenVX/OpenCV corollary library to enable efficient data flow between the Computer Vision and VR teams
- Optimized legacy computer vision functions for a 2.5x average speedup to meet Qualcomm's new VR chips' specs

University of Michigan **Ann Arbor, MI**

Undergraduate Research Assistant (Computer Security Lab) *December 2017 - May 2018*

- Assessed security profile of novel encryption accelerators via side-channel analysis to identify vulnerabilities before tape-out
- Programmed data tagging for the RocketChip open-source processor to allow for finer-grained encryption

University of Michigan **Ann Arbor, MI**

Student Instructor (EECS 280: Programming and Data Structures) *December 2016 - December 2017*

- Instructed labs on OOP, performed code review in office hours, and designed and tested exam problems for 1000+ students
- Implemented cheat-checking SW to analyze students' C++ code to provide a fair and opportunistic learning environment

SKILLS

Languages: C/C++, C#, Python, SystemVerilog, JavaScript, Bash, Assembly (RISC-V, ARM, x86)
Hardware Development: Xilinx FPGA, Custom ISA Design, Hardware Security
Cloud & DevOps: CI/CD, AWS, Azure, Git, Jenkins
Development Tools: VS Code, GDB, Make

PUBLICATIONS & PATENTS

- *Morpheus II: A RISC-V Security Extension for Protecting Vulnerable Software and Hardware, 2021 IEEE HotChips 33*
- Patent US11748521: *Privacy-Enhanced Computation via Sequestered Encryption*
- Patent US12105855: *Safe Disclosures in Sequestered Encryption Systems*

EDUCATION

University of Michigan **Ann Arbor, MI**

B.S.E Computer Engineering, cum laude *September 2015 - December 2018*