

5.2.17 Register (0x17) DATA_13

DESCRIPTION: ACC_Z(MSB)

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x17) DATA_13			
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	acc_z_15_8			
Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	acc_z_15_8			

5.2.18 Register (0x18) SENSORTIME_0

DESCRIPTION: Sensor time <7:0>

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x18) SENSORTIME_0			
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	sensor_time_7_0			
Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	sensor_time_7_0			

sensor_time_7_0: Sensor time <7:0> in units of 39.0625 us.

5.2.19 Register (0x19) SENSORTIME_1

DESCRIPTION: Sensor time <15:8>

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x19) SENSORTIME_1			
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	sensor_time_15_8			
Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	sensor_time_15_8			

sensor_time_15_8: Sensor time <15:8> in units of 10 ms.

5.2.20 Register (0x1A) SENSORTIME_2

DESCRIPTION: Sensor time <23:16>

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x1A) SENSORTIME_2			
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	sensor_time_23_16			
Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	sensor_time_23_16			

sensor_time_23_16: Sensor time <23:16> in units of 2.56 s.

5.2.21 Register (0x1B) EVENT

DESCRIPTION: Sensor status flags

RESET: 0x01

DEFINITION (Go to [register map](#)):

Name	Register (0x1B) EVENT			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			
Bit	3	2	1	0
Read/Write	n/a	n/a	n/a	R
Reset Value	0	0	0	1
Content	reserved			por_detected

por_detected: '1' after device power up or softreset. Clear-on-read

5.2.22 Register (0x1C) INT_STATUS_0

DESCRIPTION: Interrupt/Feature status. This register will be cleared on read.

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x1C) INT_STATUS_0			
Bit	7	6	5	4
Read/Write	R	R	R	n/a
Reset Value	0	0	0	0
Content	error_int_out	no_motion_out	any_motion_out	reserved
Bit	3	2	1	0
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			

any_motion_out: Any-motion detection output

no_motion_out: No-motion detection output
 error_int_out: Error interrupt output

5.2.23 Register (0x1D) INT_STATUS_1

DESCRIPTION: Interrupt Status. This register will be cleared on read.

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x1D) INT_STATUS_1			
Bit	7	6	5	4
Read/Write	R	n/a	R	n/a
Reset Value	0	0	0	0
Content	acc_drdy_int	reserved	aux_drdy_int	reserved
Bit	3	2	1	0
Read/Write	n/a	n/a	R	R
Reset Value	0	0	0	0
Content	reserved		fwm_int	ffull_int

ffull_int: FIFO Full Interrupt
 fwm_int: FIFO Watermark Interrupt
 aux_drdy_int: Auxiliary sensor data ready interrupt
 acc_drdy_int: Accelerometer data ready interrupt

5.2.24 Register (0x22) TEMPERATURE

DESCRIPTION: Contains the temperature value of the sensor

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x22) TEMPERATURE			
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	temperature			
Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	temperature			

temperature: Temperature value in two's complement representation in units of 1 Kelvin: 0x00 corresponds to 23 degree Celsius.

5.2.25 Register (0x24) FIFO_LENGTH_0

DESCRIPTION: FIFO byte count register (LSB)

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x24) FIFO_LENGTH_0			
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	fifo_byte_counter_7_0			
Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	fifo_byte_counter_7_0			

fifo_byte_counter_7_0: Current fill level of FIFO buffer.

5.2.26 Register (0x25) FIFO_LENGTH_1

DESCRIPTION: FIFO byte count register (MSB)

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x25) FIFO_LENGTH_1			
Bit	7	6	5	4
Read/Write	n/a	n/a	R	R
Reset Value	0	0	0	0
Content	reserved		fifo_byte_counter_13_8	
Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	fifo_byte_counter_13_8			

fifo_byte_counter_13_8: FIFO byte counter bits 13..8

5.2.27 Register (0x26) FIFO_DATA

DESCRIPTION: FIFO data output register

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x26) FIFO_DATA			
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	fifo_data			
Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	fifo_data			

fifo_data: FIFO read data.

5.2.28 Register (0x2A) INTERNAL_STATUS

DESCRIPTION: Error bits and message indicating internal status

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x2A) INTERNAL_STATUS			
Bit	7	6	5	4
Read/Write	n/a	R	R	R
Reset Value	0	0	0	0
Content	reserved	odr_50Hz_error	axes_remap_error	message
Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	message			

message: Internal status message

message		
0x00	not_init	ASIC is not initialized
0x01	init_ok	ASIC initialized
0x02	init_err	Initialization error
0x03	drv_err	Invalid driver
0x04	sns_stop	Sensor stopped

axes_remap_error: Incorrect axes remapping. X,Y,Z axes must be mapped to exclusively separate axes i.e. they cannot be mapped to same axes.

odr_50Hz_error: The minimum bandwidth conditions are not respected for the features which require 50 Hz data

5.2.29 Register (0x40) ACC_CONF

DESCRIPTION: Sets the output data rate, the bandwidth, and the read mode of the acceleration sensor

RESET: 0xA8

DEFINITION (Go to [register map](#)):

Name	Register (0x40) ACC_CONF			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	1	0	1	0
Content	acc_perf_mode	acc_bwp		
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	1	0	0	0
Content	acc_odr			

acc_odr: ODR in Hz. The output data rate is independent of the power mode setting for the sensor, but not all settings are supported in all power modes.

acc_odr		
0x00	reserved	Reserved
0x01	odr_0p78	25/32
0x02	odr_1p5	25/16
0x03	odr_3p1	25/8
0x04	odr_6p25	25/4
0x05	odr_12p5	25/2
0x06	odr_25	25
0x07	odr_50	50
0x08	odr_100	100
0x09	odr_200	200
0x0a	odr_400	400
0x0b	odr_800	800
0x0c	odr_1k6	1600
0x0d	odr_3k2	Reserved
0x0e	odr_6k4	Reserved
0x0f	odr_12k8	Reserved

acc_bwp: Bandwidth parameter, determines filter configuration (acc_perf_mode=1) and averaging for undersampling mode (acc_perf_mode=0)

acc_bwp		
0x00	osr4_avg1	acc_perf_mode = 1 -> OSR4 mode; acc_perf_mode = 0 -> no averaging
0x01	osr2_avg2	acc_perf_mode = 1 -> OSR2 mode; acc_perf_mode = 0 -> average 2 samples
0x02	norm_avg4	acc_perf_mode = 1 -> normal mode; acc_perf_mode = 0 -> average 4 samples
0x03	cic_avg8	acc_perf_mode = 1 -> Reserved; acc_perf_mode = 0 -> average 8 samples
0x04	res_avg16	acc_perf_mode = 1 -> Reserved; acc_perf_mode = 0 -> average 16 samples
0x05	res_avg32	acc_perf_mode = 1 -> Reserved; acc_perf_mode = 0 -> average 32 samples
0x06	res_avg64	acc_perf_mode = 1 -> Reserved; acc_perf_mode = 0 -> average 64 samples
0x07	res_avg128	acc_perf_mode = 1 -> Reserved; acc_perf_mode = 0 -> average 128 samples

acc_perf_mode: Select accelerometer filter performance mode:

acc_perf_mode		
0x00	cic_avg	averaging mode.
0x01	cont	continuous filter function.

5.2.30 Register (0x41) ACC_RANGE

DESCRIPTION: Selection of the Accelerometer g-range

RESET: 0x01

DEFINITION (Go to [register map](#)):

Name	Register (0x41) ACC_RANGE			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			
Bit	3	2	1	0
Read/Write	n/a	n/a	RW	RW
Reset Value	0	0	0	1
Content	reserved		acc_range	

acc_range: Accelerometer g-range

acc_range		
0x00	range_2g	+/-2g
0x01	range_4g	+/-4g
0x02	range_8g	+/-8g
0x03	range_16g	+/-16g

5.2.31 Register (0x44) AUX_CONF

DESCRIPTION: Sets the output data rate of the Auxiliary interface

RESET: 0x46

DEFINITION (Go to [register map](#)):

Name	Register (0x44) AUX_CONF			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	0	1	0	0
Content	aux_offset			
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	1	1	0
Content	aux_odr			

aux_odr: Select the poll rate for the sensor attached to the Auxiliary interface.

aux_odr		
0x00	reserved	Reserved
0x01	odr_0p78	25/32
0x02	odr_1p5	25/16
0x03	odr_3p1	25/8
0x04	odr_6p25	25/4
0x05	odr_12p5	25/2
0x06	odr_25	25
0x07	odr_50	50
0x08	odr_100	100
0x09	odr_200	200
0x0a	odr_400	400
0x0b	odr_800	800
0x0c	odr_1k6	Reserved
0x0d	odr_3k2	Reserved
0x0e	odr_6k4	Reserved
0x0f	odr_12k8	Reserved

aux_offset: trigger-readout offset in units of 2.5 ms. If set to zero, the offset is maximum, i.e. after readout a trigger is issued immediately.

5.2.32 Register (0x45) FIFO_DOWNS

DESCRIPTION: Configure Accelerometer downsampling rates for FIFO

RESET: 0x80

DEFINITION (Go to [register map](#)):

Name	Register (0x45) FIFO_DOWNS			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	1	0	0	0
Content	acc_fifo_filt_data	acc_fifo_downs		
Bit	3	2	1	0
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			

acc_fifo_downs: Downsampling for accelerometer data ($2^{**}acc_fifo_downs$)

acc_fifo_filt_data: selects filtered or unfiltered Accelerometer data for fifo

acc_fifo_filt_data		
0x00	unfiltered	Unfiltered data
0x01	filtered	Filtered data

5.2.33 Register (0x46) FIFO_WTM_0

DESCRIPTION: FIFO Watermark level LSB

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x46) FIFO_WTM_0			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	fifo_water_mark_7_0			
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	fifo_water_mark_7_0			

5.2.34 Register (0x47) FIFO_WTM_1

DESCRIPTION: FIFO Watermark level MSB

RESET: 0x02

DEFINITION (Go to [register map](#)):

Name	Register (0x47) FIFO_WTM_1			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	RW
Reset Value	0	0	0	0
Content	reserved			fifo_water_mark_12_8
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	1	0
Content	fifo_water_mark_12_8			

5.2.35 Register (0x48) FIFO_CONFIG_0

DESCRIPTION: FIFO frame content configuration

RESET: 0x02

DEFINITION (Go to [register map](#)):

Name	Register (0x48) FIFO_CONFIG_0			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			
Bit	3	2	1	0
Read/Write	n/a	n/a	RW	RW
Reset Value	0	0	1	0
Content	reserved		fifo_time_en	fifo_stop_on_full

fifo_stop_on_full: Stop writing samples into FIFO when FIFO is full.

fifo_stop_on_full		
0x00	disable	do not stop writing to FIFO when full
0x01	enable	Stop writing into FIFO when full.

fifo_time_en: Return sensortime frame after the last valid data frame.

fifo_time_en		
0x00	disable	do not return sensortime frame
0x01	enable	return sensortime frame

5.2.36 Register (0x49) FIFO_CONFIG_1

DESCRIPTION: FIFO frame content configuration

RESET: 0x10

DEFINITION (Go to [register map](#)):

Name	Register (0x49) FIFO_CONFIG_1			
Bit	7	6	5	4
Read/Write	n/a	RW	RW	RW
Reset Value	0	0	0	1
Content	reserved	fifo_acc_en	fifo_aux_en	fifo_header_en
Bit	3	2	1	0
Read/Write	RW	RW	n/a	n/a
Reset Value	0	0	0	0
Content	fifo_tag_int1_en	fifo_tag_int2_en	reserved	

fifo_tag_int2_en: FIFO interrupt 2 tag enable

fifo_tag_int2_en		
0x00	disable	disable tag
0x01	enable	enable tag

fifo_tag_int1_en: FIFO interrupt 1 tag enable

fifo_tag_int1_en		
0x00	disable	disable tag
0x01	enable	enable tag

fifo_header_en: FIFO frame header enable

fifo_header_en		
0x00	disable	no header is stored (output data rate of all enabled sensors need to be identical)
0x01	enable	header is stored

fifo_aux_en: Store Auxiliary data in FIFO (all 3 axes)

fifo_aux_en		
0x00	disable	no Auxiliary data is stored
0x01	enable	Auxiliary data is stored

fifo_acc_en: Store Accelerometer data in FIFO (all 3 axes)

fifo_acc_en		
0x00	disable	no Accelerometer data is stored
0x01	enable	Accelerometer data is stored

5.2.37 Register (0x4B) AUX_DEV_ID

DESCRIPTION: Auxiliary interface slave device id

RESET: 0x20

DEFINITION (Go to [register map](#)):

Name	Register (0x4B) AUX_DEV_ID			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	0	0	1	0
Content	i2c_device_addr			
Bit	3	2	1	0
Read/Write	RW	RW	RW	n/a
Reset Value	0	0	0	0
Content	i2c_device_addr			reserved

i2c_device_addr: I2C device address of Auxiliary slave

5.2.38 Register (0x4C) AUX_IF_CONF

DESCRIPTION: Auxiliary interface configuration

RESET: 0x83

DEFINITION (Go to [register map](#)):

Name	Register (0x4C) AUX_IF_CONF			
Bit	7	6	5	4
Read/Write	RW	n/a	n/a	n/a
Reset Value	1	0	0	0
Content	aux_manual_en	reserved		
Bit	3	2	1	0
Read/Write	n/a	n/a	RW	RW
Reset Value	0	0	1	1
Content	reserved		aux_rd_burst	

aux_rd_burst: Burst data length (1,2,6,8 byte)

aux_rd_burst		
0x00	BL1	Burst length 1
0x01	BL2	Burst length 2
0x02	BL6	Burst length 6
0x03	BL8	Burst length 8

aux_manual_en: Enable auxiliary interface manual mode.

aux_manual_en		
0x00	disable	Data mode
0x01	enable	Setup mode

5.2.39 Register (0x4D) AUX_RD_ADDR

DESCRIPTION: Auxiliary interface read register address

RESET: 0x42

DEFINITION (Go to [register map](#)):

Name	Register (0x4D) AUX_RD_ADDR			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	0	1	0	0
Content	read_addr			
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	1	0
Content	read_addr			

read_addr: Address to read

5.2.40 Register (0x4E) AUX_WR_ADDR

DESCRIPTION: Auxiliary interface write register address

RESET: 0x4C

DEFINITION (Go to [register map](#)):

Name	Register (0x4E) AUX_WR_ADDR			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	0	1	0	0
Content	write_addr			
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	1	1	0	0
Content	write_addr			

write_addr: Address to write

5.2.41 Register (0x4F) AUX_WR_DATA

DESCRIPTION: Auxiliary interface write data

RESET: 0x02

DEFINITION (Go to [register map](#)):

Name	Register (0x4F) AUX_WR_DATA			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	write_data			
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	1	0
Content	write_data			

write_data: Data to write

5.2.42 Register (0x53) INT1_IO_CTRL

DESCRIPTION: Configure the electrical behaviour of the interrupt pins

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x53) INT1_IO_CTRL			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	RW
Reset Value	0	0	0	0
Content	reserved			input_en
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	output_en	od	lvl	edge_ctrl

edge_ctrl: Configure trigger condition of INT1 pin (input)

edge_ctrl		
0x00	level_tr	Level
0x01	edge_tr	Edge

lvl: Configure level of INT1 pin

lvl		
0x00	active_low	active low
0x01	active_high	active high

od: Configure behaviour of INT1 pin to open drain.

od		
0x00	push_pull	push-pull
0x01	open_drain	open drain

output_en: Output enable for INT1 pin

output_en		
0x00	off	Output disabled
0x01	on	Output enabled

input_en: Input enable for INT1 pin

input_en		
0x00	off	Input disabled
0x01	on	Input enabled

5.2.43 Register (0x54) INT2_IO_CTRL

DESCRIPTION: Configure the electrical behaviour of the interrupt pins

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x54) INT2_IO_CTRL			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	RW
Reset Value	0	0	0	0
Content	reserved			input_en
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	output_en	od	lvl	edge_ctrl

edge_ctrl: Configure trigger condition of INT2 pin (input)

edge_ctrl		
0x00	level_tr	Level
0x01	edge_tr	Edge

lvl: Configure level of INT2 pin

lvl		
0x00	active_low	active low
0x01	active_high	active high

od: Configure behaviour of INT2 pin to open drain.

od		
0x00	push_pull	push-pull
0x01	open_drain	open drain

output_en: Output enable for INT2 pin

output_en		
0x00	off	Output disabled
0x01	on	Output enabled

input_en: Input enable for INT2 pin

input_en		
0x00	off	Input disabled
0x01	on	Input enabled

5.2.44 Register (0x55) INT_LATCH

DESCRIPTION: Configure interrupt modes

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x55) INT_LATCH			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			
Bit	3	2	1	0
Read/Write	n/a	n/a	n/a	RW
Reset Value	0	0	0	0
Content	reserved			int_latch

int_latch: Latched/non-latched/temporary interrupt modes

int_latch		
0x00	none	non latched
0x01	permanent	latched

5.2.45 Register (0x56) INT1_MAP

DESCRIPTION: Interrupt/Feature mapping on INT1

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x56) INT1_MAP			
Bit	7	6	5	4
Read/Write	RW	RW	RW	n/a
Reset Value	0	0	0	0
Content	error_int_out	no_motion_out	any_motion_out	reserved
Bit	3	2	1	0
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			

any_motion_out: Any-motion detection output

no_motion_out: No-motion detection output

error_int_out: Error interrupt output

5.2.46 Register (0x57) INT2_MAP

DESCRIPTION: Interrupt/Feature mapping on INT2

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x57) INT2_MAP			
Bit	7	6	5	4
Read/Write	RW	RW	RW	n/a
Reset Value	0	0	0	0
Content	error_int_out	no_motion_out	any_motion_out	reserved
Bit	3	2	1	0
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			

any_motion_out: Any-motion detection output

no_motion_out: No-motion detection output

error_int_out: Error interrupt output

5.2.47 Register (0x58) INT_MAP_DATA

DESCRIPTION: Interrupt mapping hardware interrupts

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x58) INT_MAP_DATA			
Bit	7	6	5	4
Read/Write	n/a	RW	RW	RW
Reset Value	0	0	0	0
Content	reserved	int2_drdy	int2_fwm	int2_full
Bit	3	2	1	0
Read/Write	n/a	RW	RW	RW
Reset Value	0	0	0	0
Content	reserved	int1_drdy	int1_fwm	int1_full

int1_full: FIFO Full interrupt mapped to INT1

int1_fwm: FIFO Watermark interrupt mapped to INT1

int1_drdy: Data Ready interrupt mapped to INT1

int2_full: FIFO Full interrupt mapped to INT2

int2_fwm: FIFO Watermark interrupt mapped to INT2

int2_drdy: Data Ready interrupt mapped to INT2

5.2.48 Register (0x59) INIT_CTRL

DESCRIPTION: Start initialization

RESET: 0x90

DEFINITION (Go to [register map](#)):

Name	Register (0x59) INIT_CTRL			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	1	0	0	1
Content	init_ctrl			
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	init_ctrl			

init_ctrl: Start initialization

5.2.49 Register (0x5E) FEATURES_IN

DESCRIPTION: Feature configuration read/write port

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x5E) FEATURES_IN			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	features_in			
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	features_in			

features_in: Feature configuration read/write data

Address	Bit	Name	Description	Reset	Access
any_motion					
0x5E: 0x00		settings_1	Any-motion detection general configuration flags - part 1	0x00AA	
	10...0	threshold	Slope threshold value for any-motion detection. Range is 0 to 1g. Default value is 0xAA = 83mg.	0xAA	RW
0x5E: 0x02		settings_2	Any-motion detection general configuration flags - part 2	0x0005	
	12...0	duration	Defines the number of consecutive data points for which the threshold condition must be respected for interrupt assertion. It is expressed in 50 Hz samples (20 ms). Range is 0 to 163sec. Default value is 5=100ms.	0x5	RW
	13	x_en	Enables the feature on a per-axis basis	0x0	RW

	14	y_en	Enables the feature on a per-axis basis	0x0	RW
	15	z_en	Enables the feature on a per-axis basis	0x0	RW
no_motion					
0x5E: 0x04		settings_1	No-motion detection general configuration flags - part 1	0x00AA	
	10...0	threshold	Slope threshold value for no-motion detection. Range is 0 to 1g. Default value is 0xAA = 83mg.	0xAA	RW
0x5E: 0x06		settings_2	No-motion detection general configuration flags - part 2	0x0005	
	12...0	duration	Defines the number of consecutive data points for which the threshold condition must be respected for interrupt assertion. It is expressed in 50 Hz samples (20 ms). Range is 0 to 163sec. Default value is 5=100ms.	0x5	RW
	13	x_en	Enables the feature on a per-axis basis	0x0	RW
	14	y_en	Enables the feature on a per-axis basis	0x0	RW
	15	z_en	Enables the feature on a per-axis basis	0x0	RW
general_settings					
0x5E: 0x08		Reserved	Reserved	0x0000	
	15...0	Reserved	Reserved	0x0	
0x5E: 0x0A		axes_remap ping	Describes axes remapping	0x0088	
	1...0	map_x_axis	Map the x axis to desired axis Value Name Description 0x00 x_axis Map to x-axis 0x01 y_axis Map to y-axis 0x02 z_axis Map to z-axis 0x03 reserved Map to x-axis	0x0	RW
	2	map_x_axis _sign	Map the x axis sign to the desired one Value Name Description 0x00 not_invert Clear this bit to not invert the x axis 0x01 inverted Set this bit to invert the x axis	0x0	RW
	4...3	map_y_axis	Map the y axis to desired axis Value Name Description 0x00 x_axis Map to x-axis 0x01 y_axis Map to y-axis 0x02 z_axis Map to z-axis 0x03 reserved Map to y-axis	0x1	RW
	5	map_y_axis _sign	Map the y axis sign to the desired one Value Name Description 0x00 not_invert Clear this bit to not invert the y axis 0x01 inverted Set this bit to invert the y axis	0x0	RW

	7...6	map_z_axis	Map the z axis to desired axis			0x2	RW
			Value	Name	Description		
			0x00	x_axis	Map to x-axis		
			0x01	y_axis	Map to y-axis		
			0x02	z_axis	Map to z-axis		
			0x03	reserved	Map to z-axis		
	8	map_z_axis_sign	Map the z axis sign to the desired one			0x0	RW
			Value	Name	Description		
			0x00	not_invert	Clear this bit to not invert the z axis		
			0x01	inverted	Set this bit to invert the z axis		

5.2.50 Register (0x5F) INTERNAL_ERROR

DESCRIPTION: Internal error flags. Value of all reserved bits should be ignored.

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x5F) INTERNAL_ERROR			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			
Bit	3	2	1	0
Read/Write	n/a	R	R	n/a
Reset Value	0	0	0	0
Content	reserved	int_err_2	int_err_1	reserved

int_err_1: Internal error flag - long processing time, processing halted

int_err_2: Internal error flag - fatal error, processing halted

5.2.51 Register (0x6A) NVM_CONF

DESCRIPTION: NVM controller mode (Prog/Erase or Read only)

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x6A) NVM_CONF			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			
Bit	3	2	1	0
Read/Write	n/a	n/a	RW	n/a
Reset Value	0	0	0	0
Content	reserved		nvm_prog_en	reserved

nvm_prog_en: Enable NVM programming

nvm_prog_en		
0x00	disable	disable
0x01	enable	enable

5.2.52 Register (0x6B) IF_CONF

DESCRIPTION: Serial interface settings

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x6B) IF_CONF			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	RW
Reset Value	0	0	0	0
Content	reserved			if_mode
Bit	3	2	1	0
Read/Write	n/a	n/a	n/a	RW
Reset Value	0	0	0	0
Content	reserved			spi3

spi3: Configure SPI Interface Mode for primary interface

spi3		
0x00	spi4	SPI 4-wire mode
0x01	spi3	SPI 3-wire mode

if_mode: Auxiliary interface configuration

if_mode		
0x00	p_auto_s_off	Auxiliary interface:off
0x01	p_auto_s_mag	Auxiliary interface:Magnetometer

5.2.53 Register (0x6D) ACC_SELF_TEST

DESCRIPTION: Settings for the sensor self-test configuration and trigger

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x6D) ACC_SELF_TEST			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			
Bit	3	2	1	0
Read/Write	RW	RW	n/a	RW
Reset Value	0	0	0	0
Content	acc_self_test_am p	acc_self_test_sign	reserved	acc_self_test_en

acc_self_test_en: Enable accelerometer self-test

acc_self_test_en		
0x00	disabled	disabled
0x01	enabled	enabled

acc_self_test_sign: select sign of self-test excitation as

acc_self_test_sign		
0x00	negative	negative
0x01	positive	positive

acc_self_test_amp: select amplitude of the selftest deflection:

acc_self_test_amp		
0x00	low	low
0x01	high	high

5.2.54 Register (0x70) NV_CONF

DESCRIPTION: NVM backed configuration bits.

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x70) NV_CONF			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	acc_off_en	i2c_wdt_en	i2c_wdt_sel	spi_en

spi_en: disable the I2C and enable SPI for the primary interface, when it is in autoconfig mode

spi_en		
0x00	disabled	I2C enabled
0x01	enabled	I2C disabled

i2c_wdt_sel: Select timer period for I2C Watchdog

i2c_wdt_sel		
0x00	wdt_short	I2C watchdog timeout after 1.25 ms
0x01	wdt_long	I2C watchdog timeout after 40 ms

i2c_wdt_en: I2C Watchdog at the SDI pin in I2C interface mode

i2c_wdt_en		
0x00	Disable	Disable I2C watchdog
0x01	Enable	Enable I2C watchdog

acc_off_en: Add the offset defined in the off_acc_[xyz] OFFSET register to filtered and unfiltered Accelerometer data

acc_off_en		
0x00	disabled	Disabled
0x01	enabled	Enabled

5.2.55 Register (0x71) OFFSET_0

DESCRIPTION: Offset compensation for Accelerometer X-axis (NVM backed)

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x71) OFFSET_0			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	off_acc_x			
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	off_acc_x			

off_acc_x: Accelerometer offset compensation (X-axis).

5.2.56 Register (0x72) OFFSET_1

DESCRIPTION: Offset compensation for Accelerometer Y-axis (NVM backed)

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x72) OFFSET_1			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	off_acc_y			
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	off_acc_y			

off_acc_y: Accelerometer offset compensation (Y-axis).

5.2.57 Register (0x73) OFFSET_2

DESCRIPTION: Offset compensation for Accelerometer Z-axis (NVM backed)

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x73) OFFSET_2			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	off_acc_z			
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	off_acc_z			

off_acc_z: Accelerometer offset compensation (Z-axis).

5.2.58 Register (0x7C) PWR_CONF

DESCRIPTION: Power mode configuration register

RESET: 0x03

DEFINITION (Go to [register map](#)):

Name	Register (0x7C) PWR_CONF			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			
Bit	3	2	1	0
Read/Write	n/a	n/a	RW	RW
Reset Value	0	0	1	1
Content	reserved		fifo_self_wakeup	adv_power_save

adv_power_save		
0x00	aps_off	advanced power save disabled (fast clk always enabled).
0x01	aps_on	advanced power mode enabled (slow clk is active when no measurement is ongoing.)

fifo_self_wakeup		
0x00	fsw_off	FIFO read disabled in advanced power saving mode.
0x01	fsw_on	FIFO read enabled after interrupt in advanced power saving mode.

5.2.59 Register (0x7D) PWR_CTRL

DESCRIPTION: Sensor enable register

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x7D) PWR_CTRL			
Bit	7	6	5	4
Read/Write	n/a	n/a	n/a	n/a
Reset Value	0	0	0	0
Content	reserved			
Bit	3	2	1	0
Read/Write	n/a	RW	n/a	RW
Reset Value	0	0	0	0
Content	reserved	acc_en	reserved	aux_en

aux_en		
0x00	mag_off	Disables the auxiliary sensor.
0x01	mag_on	Enables the auxiliary sensor.

acc_en		
0x00	acc_off	Disables the Accelerometer.
0x01	acc_on	Enables the Accelerometer.

5.2.60 Register (0x7E) CMD

DESCRIPTION: Command Register

RESET: 0x00

DEFINITION (Go to [register map](#)):

Name	Register (0x7E) CMD			
Bit	7	6	5	4
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	cmd			
Bit	3	2	1	0
Read/Write	RW	RW	RW	RW
Reset Value	0	0	0	0
Content	cmd			

cmd: Available commands (Note: Register will always read as 0x00):

cmd		
0xa0	nvm_prog	Writes the NVM backed registers into NVM
0xb0	fifo_flush	Clears all data in the FIFO, does not change FIFO_CONFIG and FIFO_DOWNS registers
0xb6	softreset	Triggers a reset, all user configuration settings are overwritten with their default state

6. Digital Interfaces

6.1 Interfaces

Beside the standard primary interface (I2C and SPI configurable), where sensor acts as a slave to the application processor, BMA490L supports an auxiliary interface. See picture below.

If the auxiliary interface is enabled, the BMA490L can be connected to an external sensor (e.g. a magnetometer) in order to build a 6-DoF solution. Then the BMA490L will act as a master to the external sensor, reading the sensor data automatically and providing it to the application processor via the primary interface.

