6.2 Primary Interface

By default, the BMA490L operates in I2C mode. The BMA490L interface can also be configured to operate in a SPI 4-wire configuration. It can also be re-configured by software to work in 3-wire mode instead of 4-wire mode.
All 3 possible digital interfaces share partly the same pins. The mapping for the primary interface of the BMA490L is given in the following table:

Pin#	Name	I/O Type	Description	Connect to (Primary IF)		
				in SPI4W	in SPI3W	in I2C
1	SDO	Digital I/O	Serial data output in SPI Address select in I²C mode see chapter 7.2	SDO	DNC (float)	GND for default I2C addr.
2	SDX	Digital I/O	SDA serial data I/O in I²C SDI serial data input in SPI 4W SDA serial data I/O in SPI 3W	SDI	SDA	SDA
5	INT1	Digital I/O	Interrupt output 1 (default) (Input for external FIFO sync) *	INT1 (FIFO sync)	INT1 (FIFO sync)	INT1 (FIFO sync)
6	INT2	Digital I/O	Interrupt output 2 (default) (Input for external FIFO sync) *	INT2 (FIFO sync)	INT2 (FIFO sync)	INT2 (FIFO sync)
10	CSB	Digital in	Chip select for SPI mode	CSB	CSB	V_{DDIO} -
12	SCX	Digital in	SCK for SPI serial clock SCL for I²C serial clock	SCK	SCK	SCL

* INT1 and/or INT2 can also be configured as an input in case the external data synchronization in FIFO is used. See chapter4.6. If INT1 and/or INT2 are not used, please do not connect them (DNC).

The following table shows the electrical specifications of the interface pins:

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pull-up Resistance, CSB pin	R_{up}	Internal Pull-up Resistance to VDDIO	75	100	125	kΩ
Input Capacitance	C_{in}			5		pF
I²C Bus Load Capacitance (max. drive capability) C_{I2C_Load}		V_{DDIO}>=1.62V			400	pF
		V_{DDIO}<1.62V			120	pF

6.3 Primary Interface I2C/SPI Protocol Selection

The protocol is automatically selected based on the chip select CSB pin behavior after power-up.

At reset / power-up, BMA490L is in I2C mode. If CSB is connected to VDDIO during power-up and not changed, the sensor interface works in I2C mode. For using I2C, it is recommended to hard-wire the CSB line to VDDIO. Since power-on-reset is only executed when, both VDD and VDDIO are established, there is no risk of incorrect protocol detection due to power-up sequence.

If CSB sees a rising edge after power-up, the BMA490L interface switches to SPI until a reset or the next power-up occurs. Therefore, a CSB rising edge is needed before starting the SPI communication. Hence, it is recommended to perform a SPI single read of register CHIP_ID (the obtained value will be invalid) before the actual communication start, in order to use the SPI interface.
If toggling of the CSB bit is not possible without data communication, there is in addition the spi_en bit in Register NV_CONF, which can be used to permanently set the primary interface to SPI without the need to toggle the CSB pin at every power-up or reset.

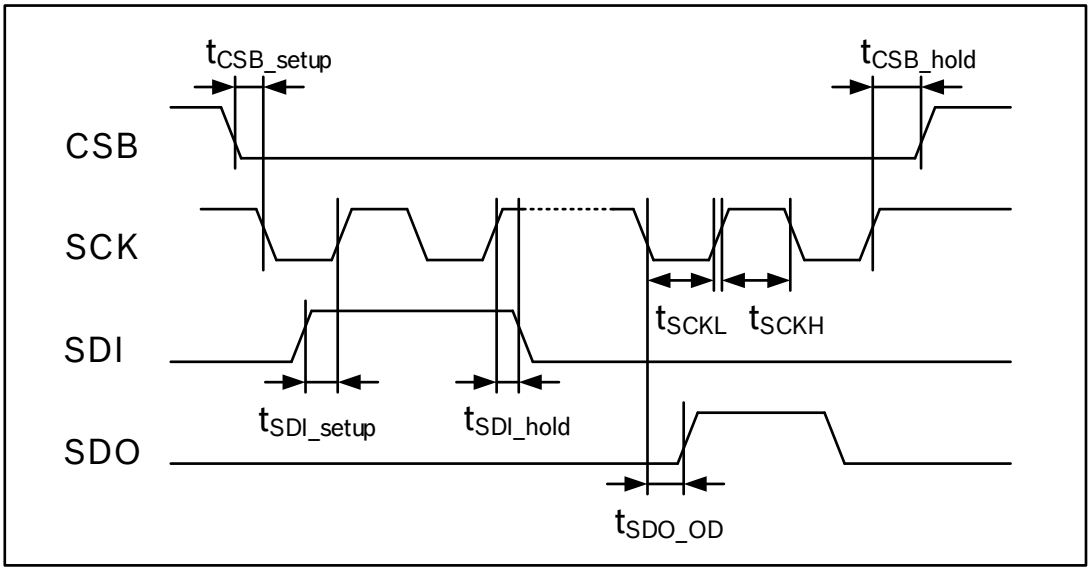
6.4 SPI interface and protocol

The timing specification for SPI of the BMA490L is given in the following table:

SPI timing, valid at $V_{DDIO} \geq 1.71V$

Parameter	Symbol	Condition	Min	Max	Units
Clock Frequency	f_{SPI}	Max. Load on SDI or SDO = 30pF, $V_{DDIO} \geq$ 1.62 V		10	MHz
		V_{DDIO} < 1.62V		7	MHz
SCK Low Pulse	t_{SCKL}	V_{DDIO}>=1.62V	45		ns
SCK High Pulse	t_{SCKH}	V_{DDIO}>=1.62V	45		ns
SCK Low Pulse	t_{SCKL}	V_{DDIO}<1.62V	66		ns
SCK High Pulse	t_{SCKH}	V_{DDIO}<1.62V	66		ns
SDI Setup Time	t_{SDI_setup}		20		ns
SDI Hold Time	t_{SDI_hold}		20		ns
SDO Output Delay	t_{SDO_OD}	Load = 30pF, $V_{DDIO} \geq$ 1.62V		30	ns
CSB Setup Time	t_{CSB_setup}		40		ns
CSB Hold Time	t_{CSB_hold}		40		ns
Idle time between write accesses, suspend mode, low-power mode 1	$t_{IDLE\_wacc\_sum}$		450		µs
Idle time after write and read access, active state	$t_{IDLE\_wr\_act}$		2		µs

The following figure shows the definition of the SPI timings:



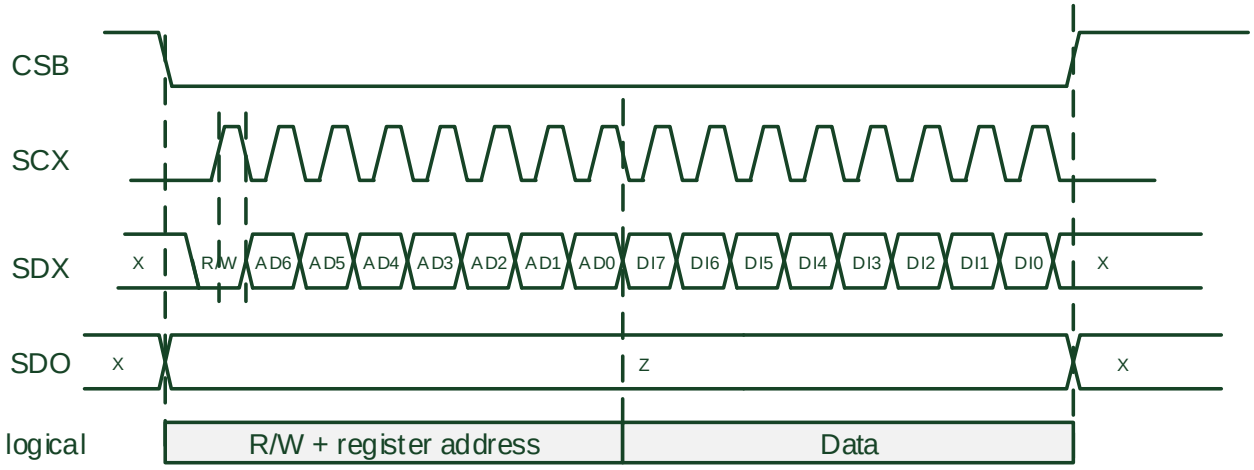
SPI timing diagram

The SPI interface of the BMA490L is compatible with two modes, ′00′ [CPOL = ′0′ and CPHA = ′0′] and ′11′ [CPOL = ′1′ and CPHA = ′1′]. The automatic selection between ′00′ and ′11′ is controlled based on the value of SCK after a falling edge of CSB.

Two configurations of the SPI interface are supported by the BMA490L: 4-wire and 3-wire. The same protocol is used by both configurations. The device operates in 4-wire configuration by default. It can be switched to 3-wire configuration by writing IF_CONF.spi3 = 0b1. Pin SDI is used as the common data pin in 3-wire configuration.
For single byte read as well as write operations, 16-bit protocols are used. The BMA490L also supports multiple-byte read and write operations.

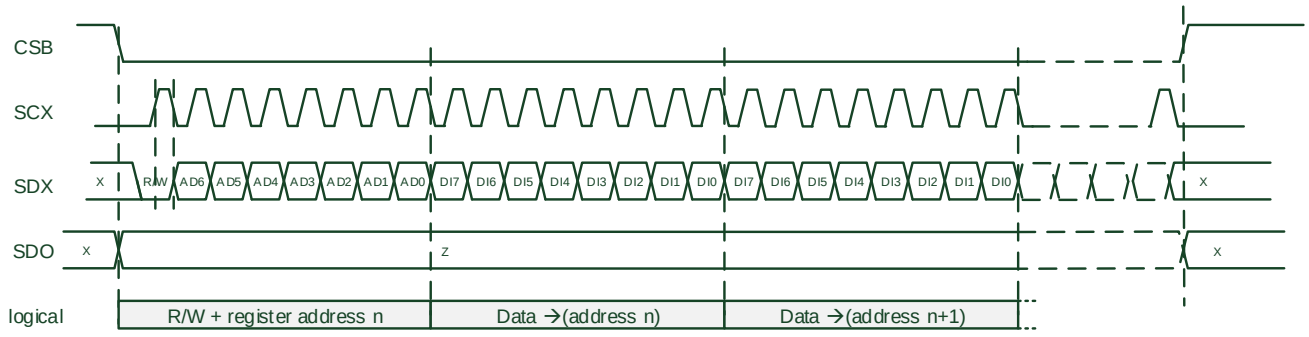
In SPI 4-wire configuration CSB (chip select low active), SCK (serial clock), SDI (serial data input), and SDO (serial data output) pins are used. The communication starts when the CSB is pulled low by the SPI master and stops when CSB is pulled high. SCK is also controlled by SPI master. SDI and SDO are driven at the falling edge of SCK and should be captured at the rising edge of SCK.

The basic write operation waveform for 4-wire configuration is depicted in the following figure. During the entire write cycle SDO remains in high-impedance state.



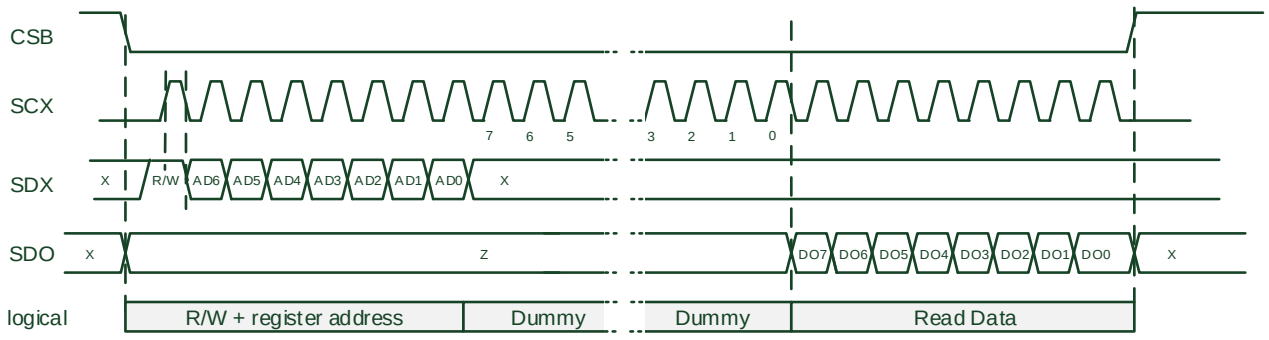
4-wire basic SPI write sequence (mode ´00´)

Multiple write operations are possible by keeping CSB low and continuing the data transfer. Only the first register address has to be written. Addresses are automatically incremented after each write access as long as CSB stays active low. The principle of multiple write is shown in figure below:



SPI multiple write

The basic read operation waveform for 4-wire configuration is depicted in the figure below. Please note that the first byte received from the BMA490L via the SDO line correspond to a dummy byte and the 2nd byte correspond to the value read out of the specified register address. That means, for a basic read operation two bytes have to be read and the first has to be dropped and the second byte must be interpreted.



4-wire basic SPI read sequence (mode ´00´)

The data bits are used as follows:

R/W: Read/Write bit. When 0, the data SDI is written into the chip. When 1, the data SDO from the chip is read.

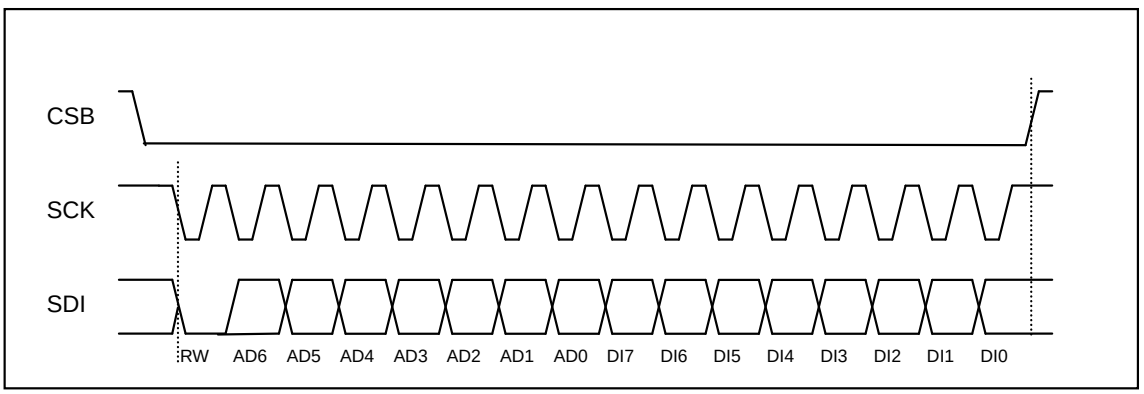
AD6-AD0: Address

DI7-DI0: When in write mode, these are the data SDI, which will be written into the address.
DO7-DO0: When in read mode, these are the data SDO, which are read from the address.

Multiple read operations are possible by keeping CSB low and continuing the data transfer. Only the first register address has to be written. Addresses are automatically incremented after each read access as long as CSB stays active low. Please note that the first byte received from the BMA490L via the SDO line correspond to a dummy byte and the 2nd byte correspond to the value read out of the specified register address. The successive bytes read out correspond to values of incremented register addresses. That means, for a multiple read operation of n bytes, n+1 bytes have to be read, the first has to be dropped and the successive bytes must be interpreted.

In SPI 3-wire configuration CSB (chip select low active), SCK (serial clock), and SDI (serial data input and output) pins are used. While SCK is high, the communication starts when the CSB is pulled low by the SPI master and stops when CSB is pulled high. SCK is also controlled by SPI master. SDI is driven (when used as input of the device) at the falling edge of SCK and should be captured (when used as the output of the device) at the rising edge of SCK.

The protocol as such is the same in 3-wire configuration as it is in 4-wire configuration. The basic operation wave-form (read or write access) for 3-wire configuration is depicted in the figure below:



3-wire basic SPI read or write sequence (mode ´11´)

6.5 Primary I2C Interface

The I²C bus uses SCL (= SCx pin, serial clock) and SDA (= SDx pin, serial data input and output) signal lines. Both lines should connected to V_{DDIO} externally via pull-up resistors so that they are pulled high when the bus is free.

The default I²C address of the device is 0b0011000 (0x18). It is used if the SDO pin is pulled to ´GND´. The alternative address 0b0011001 (0x19) is selected by pulling the SDO pin to ´VDDIO´.

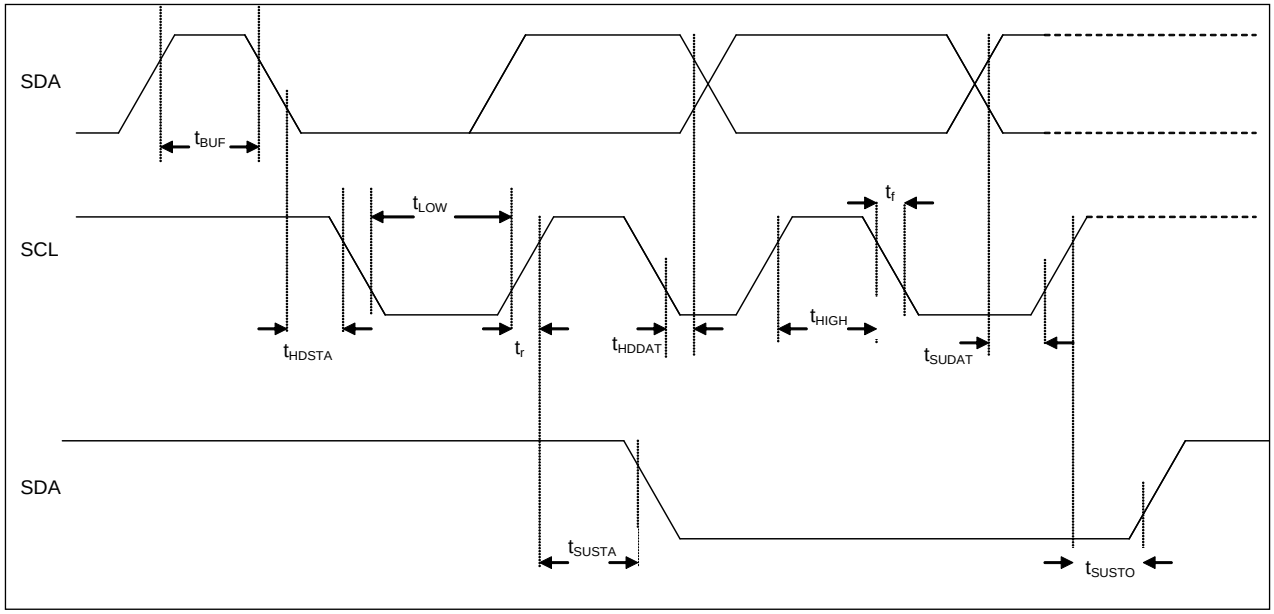
The I²C interface of the BMA490L is compatible with the I²C Specification UM10204 Rev. 03 (19 June 2007), available at http://www.nxp.com. The BMA490L supports **I²C standard mode and fast mode**, only 7-bit address mode is supported. For V_{DDIO} = 1.2V to 1.62 V the guaranteed voltage output levels are slightly relaxed as described in Table 1 of the electrical specification section.

BMA490L also supports an **extended I²C mode** that allows using clock frequencies up to 1 MHz.
In this mode all timings of the fast mode apply and it additionally supports clock frequencies up to 1MHz.

The timing specification for I²C of the BMA490L is given in the following table:

Parameter	Symbol	Condition	Min	Max	Units
Clock Frequency	f_{SCL}			1000	kHz
SCL Low Period	t_{LOW}		1.3		µs
SCL High Period	t_{HIGH}		0.6		
SDA Setup Time	t_{SUDAT}		0.1		
SDA Hold Time	t_{HDDAT}		0.0		
Setup Time for a repeated Start Condition	t_{SUSTA}		0.6		
Hold Time for a Start Condition	t_{HDSTA}		0.6		
Setup Time for a Stop Condition	t_{SUSTO}		0.6		
Time before a new Transmission can start	t_{BUF}	low power mode	400		
		performance mode	2		
Idle time between write accesses, performance mode, low-power mode	$t_{IDLE\_wacc\_nm}$	low power mode	450		
		performance mode	2		
Idle time between write accesses, suspend mode, low-power mode	$t_{IDLE\_wacc\_sum}$		450		

The figure below shows the definition of the I²C timings given in Table 28:



I²C timing diagram

The I²C protocol works as follows:

START: Data transmission on the bus begins with a high to low transition on the SDA line while SCL is held high (start condition (S) indicated by I²C bus master). Once the START signal is transferred by the master, the bus is considered busy.

STOP: Each data transfer should be terminated by a Stop signal (P) generated by master. The STOP condition is a low to high transition on SDA line while SCL is held high.

ACKS: Each byte of data transferred must be acknowledged. It is indicated by an acknowledge bit sent by the receiver. The transmitter must release the SDA line (no pull down) during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.

In the following diagrams these abbreviations are used:

S	Start
P	Stop
ACKS	Acknowledge by slave
ACKM	Acknowledge by master
NACKM	Not acknowledge by master
RW	Read / Write

A START immediately followed by a STOP (without SCL toggling from ´VDDIO´ to ´GND´) is not supported. If such a combination occurs, the STOP is not recognized by the device.

I²C write access:
I²C write access can be used to write a data byte in one sequence.

The sequence begins with start condition generated by the master, followed by 7 bits slave address and a write bit (RW = 0). The slave sends an acknowledge bit (ACKS = 0) and releases the bus. Then the master sends the one byte register address. The slave again acknowledges the transmission and waits for the 8 bits of data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol.

Example of an I²C write access:

Start	Slave Adress							R/W	ACK	Register address (0x41)								ACK	Register data (0x01)								ACK	Stop
S	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	P

Master -> Slave
Slave -> Master

I²C write

Multi-byte writes are supported without restriction on normal registers with auto-increment, on special registers with address trap.

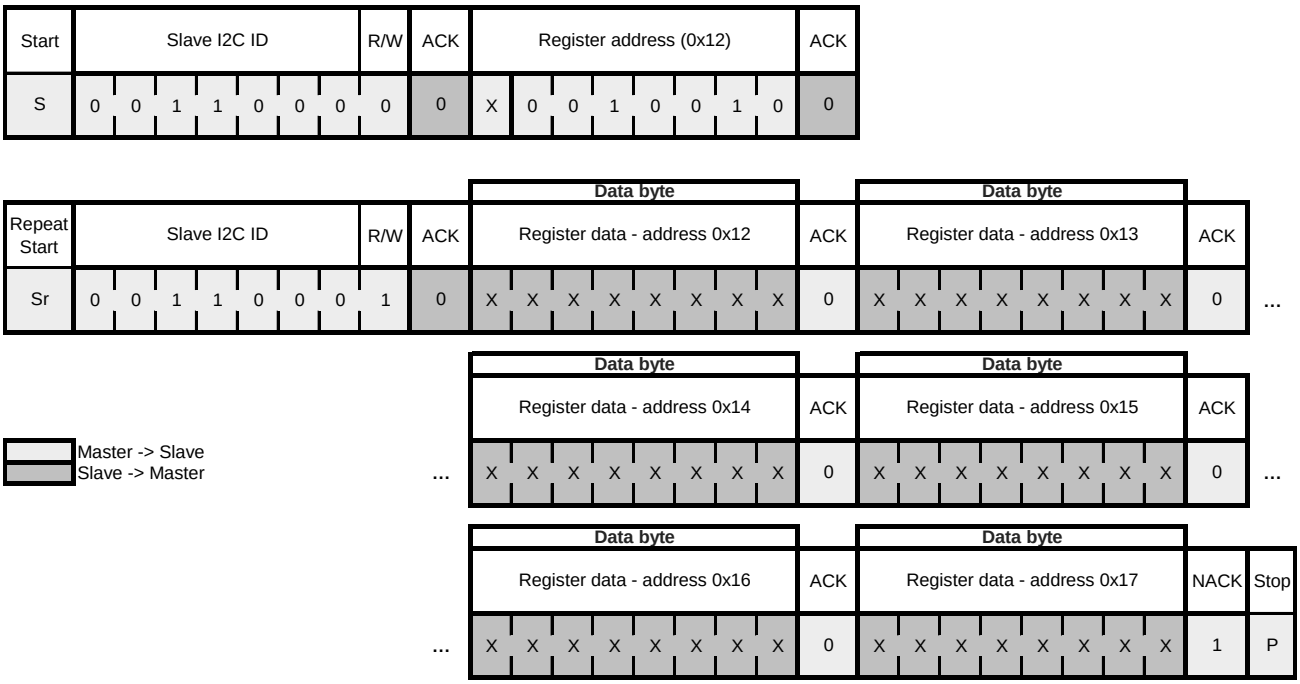
Start	Slave Adress							R/W	ACK	Register address (0x45)								ACK	Register data byte 0 (0x80)								ACK
S	0	0	1	1	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0

Register data byte 1 (0x64)								ACK	… …								ACK	Register data byte n (0xXX)								ACK	Stop
0	1	1	0	0	1	0	0	0	.	.	.	.	.	.	.	.	0	x	x	x	x	x	x	x	x	0	P

Master -> Slave
Slave -> Master

I²C read access:
I²C read access also can be used to read one or multiple data bytes in one sequence.

A read sequence consists of a one-byte I²C write phase followed by the I²C read phase. The two parts of the transmission must be separated by a repeated start condition (S). The I²C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, the master generates again a start condition and sends the slave address together with a read bit (RW = 1). Then the master releases the bus and waits for the data bytes to be read out from slave. After each data byte the master has to generate an acknowledge bit (ACKS = 0) to enable further data transfer. A NACKM (after ACKS = 1) from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a STOP condition and terminate the transmission.
The register address is automatically incremented and, therefore, more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified since the latest I²C write command. By default the start address is set at 0x00. In this way repetitive multi-bytes reads from the same starting address are possible.

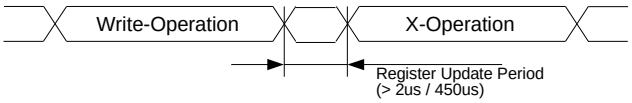


In order to prevent the I²C slave of the device to lock-up the I²C bus, a watchdog timer (WDT) is implemented. The WDT observes internal I²C signals and resets the I²C interface if the bus is locked-up by the BMA490L. The activity and the timer period of the WDT can be configured through the bits NV_CONF.i2c_wdt_en and NV_CONF.i2c_wdt_sel.

6.6 SPI and I²C Access Restrictions

In order to allow for the correct internal synchronization of data written to the BMA490L, certain access restrictions apply for consecutive write accesses or a write/read sequence through the SPI as well as I2C interface. The required waiting period depends on whether the device is operating in performance mode or other modes.

As illustrated in the figure below, an interface idle time of at least 2 µs is required following a write operation when the device operates in performance mode. In suspend mode and low power mode an interface idle time of at least 450 µs is required.



Post-Write Access Timing Constraints

6.7 Auxiliary Interface

The BMA490L allows attaching an external sensor (MAG-sensor) to a BMA490L via the auxiliary interface. The connection diagrams for the auxiliary interface are depicted in the chapter 7.3. The timings of the secondary I2C interface are the same as for the primary I2C interface, see chapter 6.5.

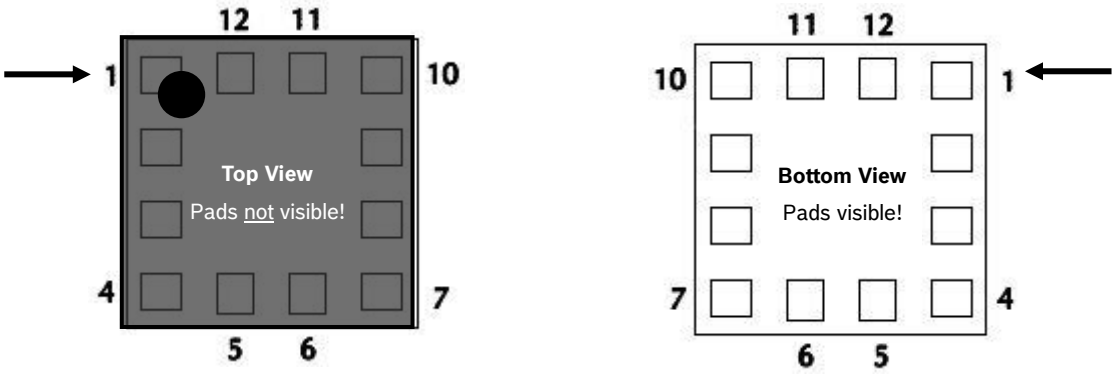
BMA490L acts as a master of the secondary interface, controls the data acquisition of the MAG-sensor (slave of the secondary interface) and presents the data to the application processor (AP) in the user registers of the BMA490L through the primary interface. The internal pull-up resistors of ASCL and ASDA are by default disabled, so it is recommended to added pull-up resistors externally onto the secondary interface for proper I2C communication. Please contact your regional sales representative in case the internal pull-up resistors are necessary to be enabled. No additional I2C master or slave devices must be attached to the magnetometer interfaces.

The BMA490L autonomously reads out the sensor data from BMM150 without intervention of the AP and stores the data in its data registers (per default) and FIFO (see Register FIFO_CONFIG_1.fifo_aux_en). The initial setup of the BMM150 after power-on is done through indirect addressing in the BMA490L. From a system perspective the initialization for BMM150 when attached to BMA490L should be possible within 100ms.

More information about the usage of Auxiliary Interface can be found in chapter 4.9.

7. Pin-out and Connection Diagrams

7.1 Pin-out



Pin description

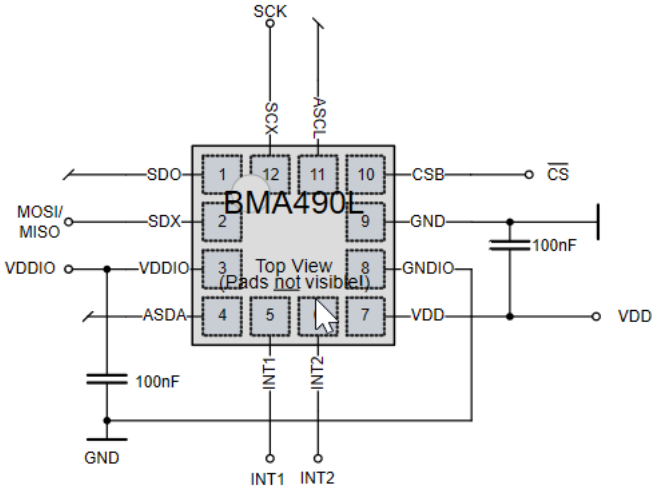
Pin#	Name	I/O Type	Description	Connect to		
				in SPI 4W	In SPI 3W	in I²C
1	SDO	Digital I/O	Serial data output in SPI Address select in I²C mode see chapter 6.5	SDO	DNC (float)	GND for default I2C addr.
2	SDX	Digital I/O	SDA serial data I/O in I²C SDI serial data input in SPI 4W SDA serial data I/O in SPI 3W	SDI	SDA	SDA
3	VDDIO	Supply	Digital I/O supply voltage (1.2V … 3.6V)	V_{DDIO}	V_{DDIO}	V_{DDIO}
4	ASDA	Digital I/O	Serial data I/O – Secondary Interface (I²C Master for Magnetometer)	VDDIO/ GNDIO/NC or (ASDA - Secondary interface)	VDDIO/ GNDIO/NC or (ASDA - Secondary interface)	VDDIO/ GNDIO/NC or (ASDA - Secondary interface)
5	INT1	Digital I/O	Interrupt output 1 (default) (Input for external FIFO sync) *	INT1 (FIFO sync)	INT1 (FIFO sync)	INT1 (FIFO sync)
6	INT2	Digital I/O	Interrupt output 2 (default) (Input for external FIFO sync) *	INT2 (FIFO sync)	INT2 (FIFO sync)	INT2 (FIFO sync)
7	VDD	Supply	Power supply for analog & digital domain (1.62V … 3.6V)	V_{DD}	V_{DD}	V_{DD}
8	GNDIO	Ground	Ground for I/O	GND	GND	GND
9	GND	Ground	Ground for digital & analog	GND	GND	GND
10	CSB	Digital in	Chip select for SPI mode	CSB	CSB	V_{DDIO}
11	ASCL	Digital out	Digital clock (out) – Secondary Interface (I²C Master for Magnetometer)	VDDIO/ GNDIO/NC or (ASCL - Secondary interface)	VDDIO/ GNDIO/ NC or (ASCL - Secondary interface)	VDDIO/ GNDIO/ NC or (ASCL - Secondary interface)
12	SCX	Digital in	SCK for SPI serial clock SCL for I²C serial clock	SCK	SCK	SCL

* INT1 and/or INT2 can also be configured as an input in case the external data synchronization in FIFO is used. See chapter 4.6. If INT1 and/or INT2 are not used, please do not connect them (DNC).

7.2 Connection Diagrams without Auxiliary Interface

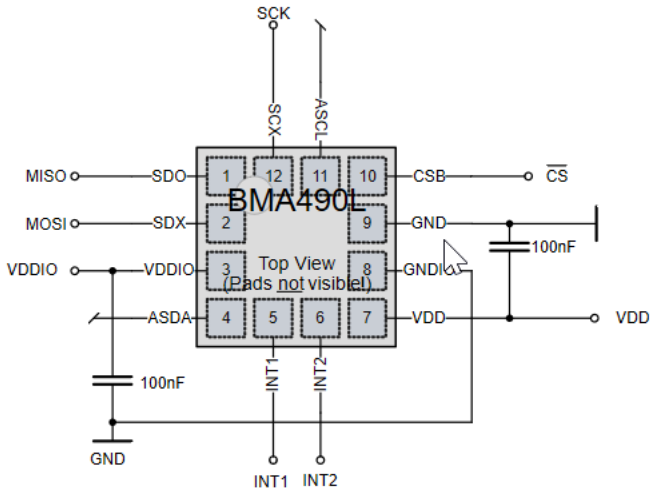
SPI

3-wire



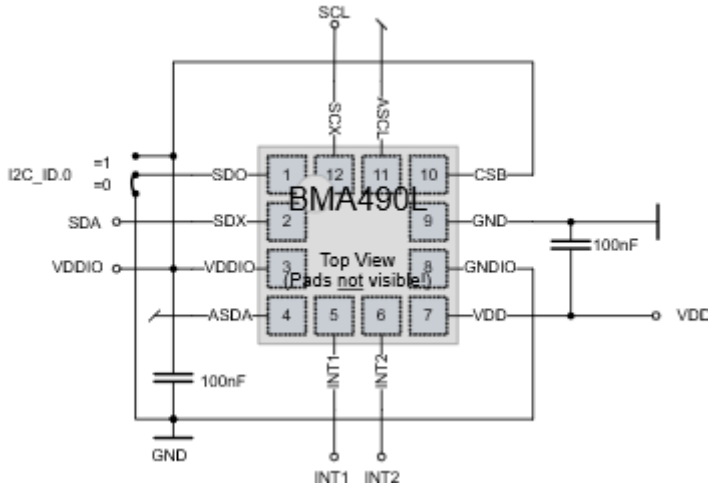
It is recommended to use 100nF decoupling capacitors at pin 3 (VDDIO) and pin 7 (VDD).

4-wire



It is recommended to use 100nF decoupling capacitors at pin 3 (VDDIO) and pin 7 (VDD).

I2C



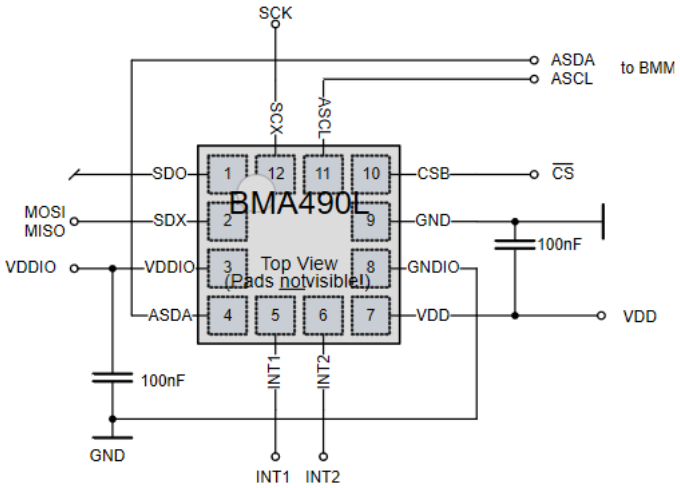
It is recommended to use 100nF decoupling capacitors at pin 3 (VDDIO) and pin 7 (VDD). SDA and SCL should be connected to V_{DDIO} externally via pull-up resistors so that they are pulled high when the bus is free.

7.3 Connection Diagrams with Auxiliary Interface

The internal pull-up resistors of ASCL and ASDA are by default disabled, so it is recommended to added pull-up resistors externally onto the secondary interface for proper I2C communication.

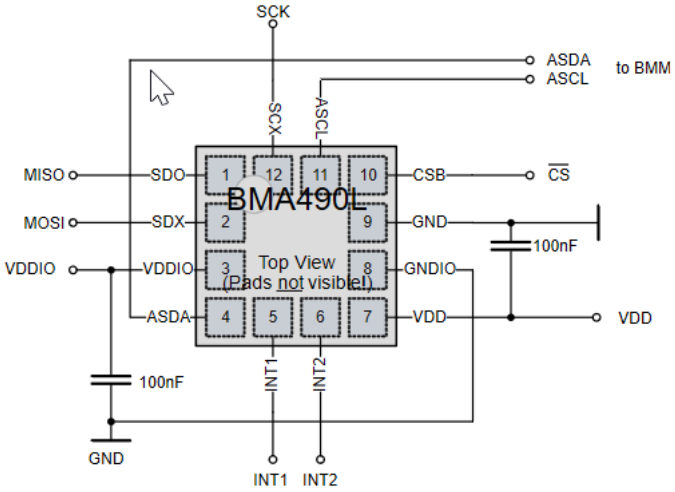
SPI

3-wire



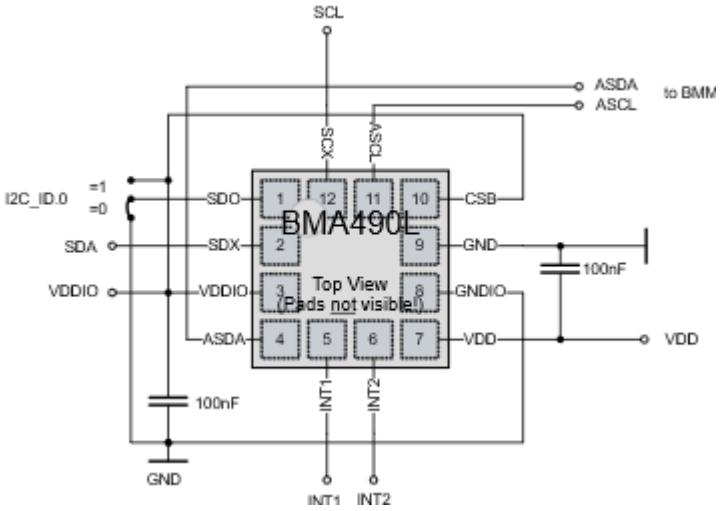
It is recommended to use 100nF decoupling capacitors at pin 3 (VDDIO) and pin 7 (VDD).

4-wire



It is recommended to use 100nF decoupling capacitors at pin 3 (VDDIO) and pin 7 (VDD).

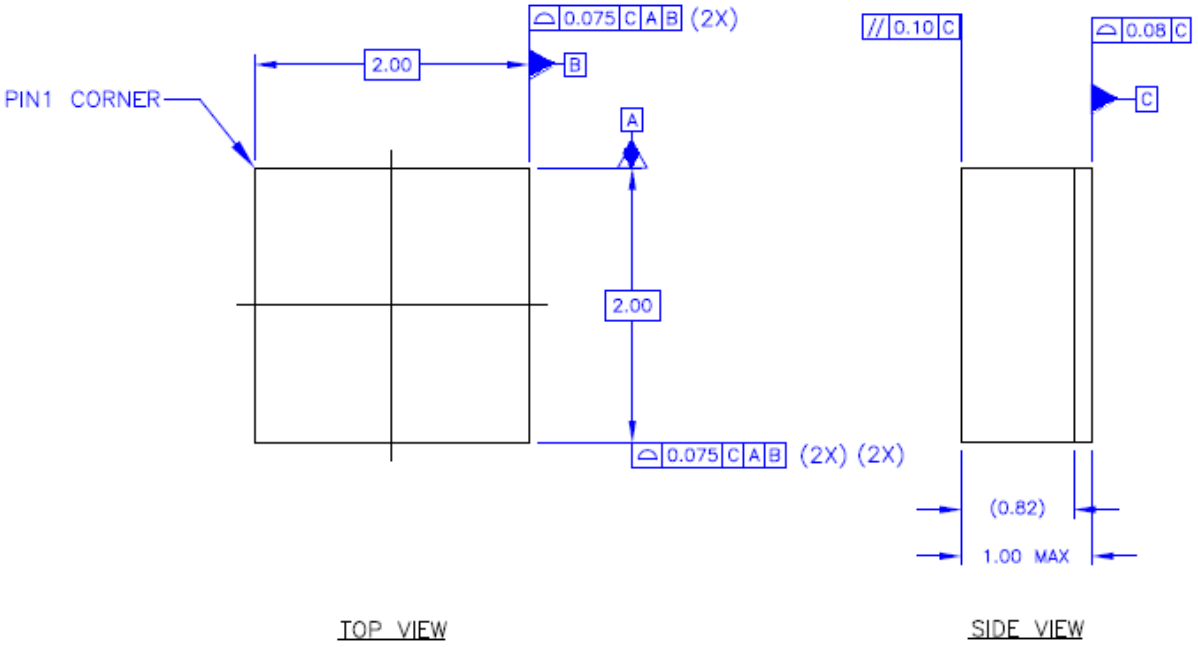
I2C

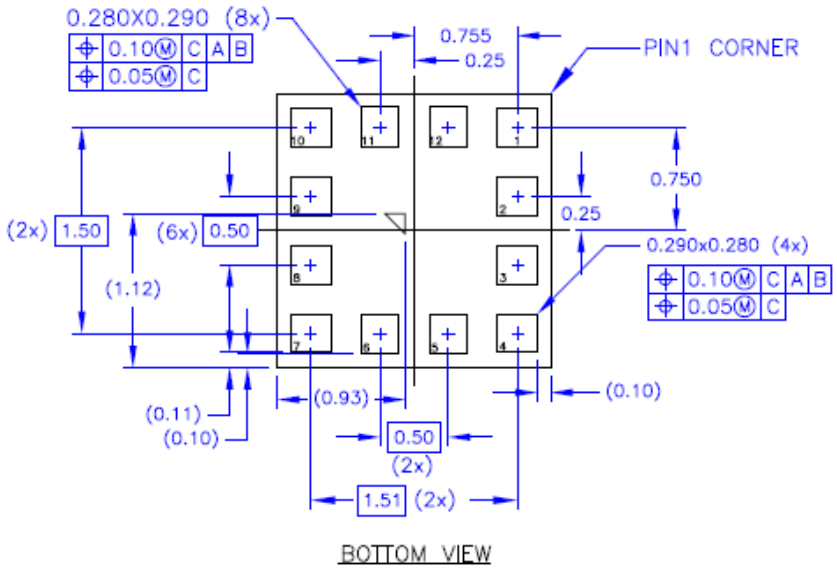


It is recommended to use 100nF decoupling capacitors at pin 3 (VDDIO) and pin 7 (VDD). SDA and SCL should be connected to V_{DDIO} externally via pull-up resistors so that they are pulled high when the bus is free.

8. Package

8.1 Package outline dimensions





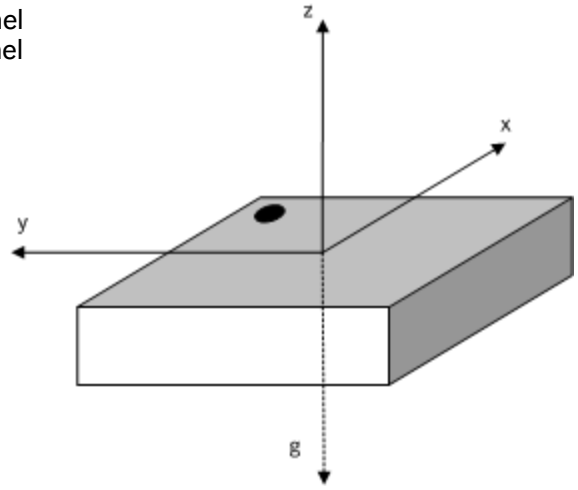
Note that the pin 5, 6, 11, 12 are in same direction (0.280*0.290, 4x), while pin 1, 2, 3, 4, 7, 8, 9, 10 are in same direction (0.290*0.280, 8x).

8.2 Sensing axis orientation

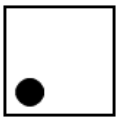
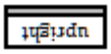
If the sensor is accelerated in the indicated directions, the corresponding channel will deliver a positive acceleration signal (dynamic acceleration). If the sensor is at rest and the force of gravity is acting along the indicated directions, the output of the corresponding channel will be negative (static acceleration).

Example: If the sensor is at rest or at uniform motion in a gravity field according to the figure given below, the output signals are:

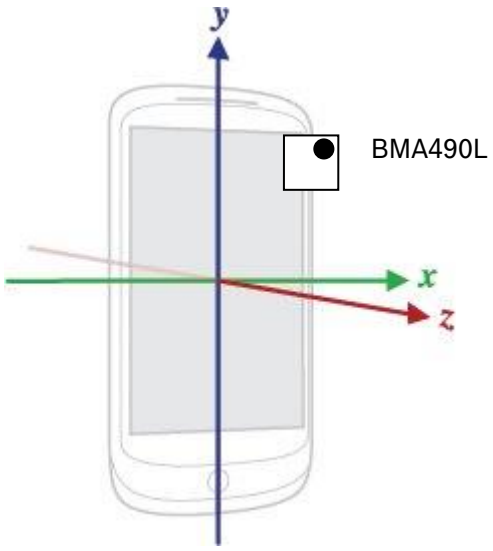
- ± 0g for the X channel
- ± 0g for the Y channel
- + 1g for the Z channel



The following table lists all corresponding output signals on X, Y, and Z while the sensor is at rest or at uniform motion in a gravity field under assumption of a ±4g range setting, a 16 bit resolution, and a top down gravity vector as shown above.

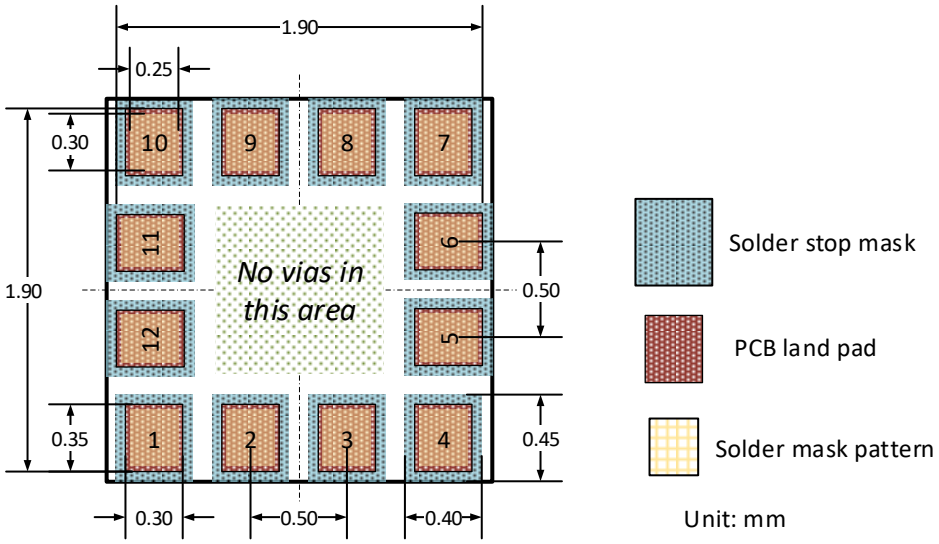
Sensor Orientation (gravity vector ↓)						
Output Signal X	0g / 0 LSB	1g / 511 LSB	0g / 0 LSB	-1g / -512 LSB	0g / 0 LSB	0g / 0 LSB
Output Signal Y	-1g / -512 LSB	0g / 0 LSB	1g / 511 LSB	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB
Output Signal Z	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB	1g / 511 LSB	-1g / -512 LSB

For reference the figure below shows the typical device orientation with an integrated BMA490L.



8.3 Landing pattern recommendation

The recommended landing pattern for the BMA490L on customer's PCB is given in the following figure. It is recommended to avoid any wiring underneath the BMA490L (shaded area).



8.4 Marking

Mass production

Labeling	Name	Symbol	Remark
	Internal Code	ZZ	internal
	Counter ID	CCC	3 alphanumeric digits, variable to generate trace-code.
	Pin 1 identifier top side	●	--

Engineering samples

Labeling	Name	Symbol	Remark
	Internal Code	X	internal
	Eng. sample ID	E, N	2 alphanumeric digits, fixed to identify engineering sample, N = “C”
	Sample ID	CC	2 alphanumeric digits, variable to generate trace-code.
	Pin 1 identifier top side	●	--

8.5 Soldering guidelines

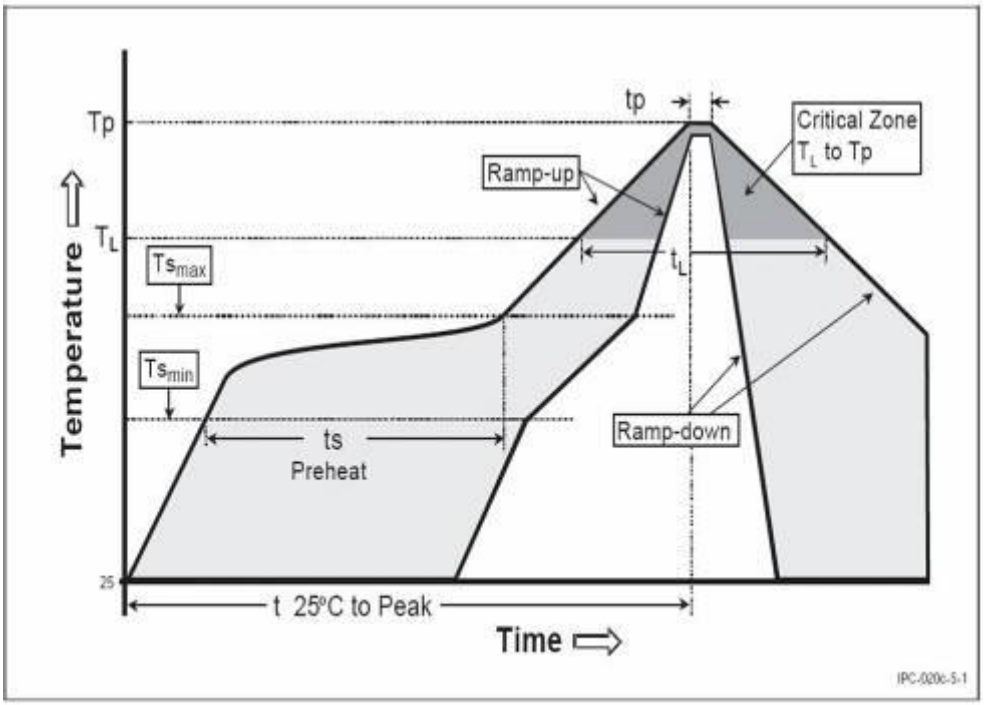
The moisture sensitivity level of the BMA490L sensors corresponds to JEDEC Level 1, see also

- IPC/JEDEC J-STD-020C "Joint Industry Standard: Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices"
- IPC/JEDEC J-STD-033A "Joint Industry Standard: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices"

The sensor fulfils the lead-free soldering requirements of the above-mentioned IPC/JEDEC standard, i.e. reflow soldering with a peak temperature up to 260°C.

Profile Feature		Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)		3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})		150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)		217 °C 60-150 seconds
Peak/Classification Temperature (Tp)		260 °C
Time within 5 °C of actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate		6 °C/second max.
Time 25 °C to Peak Temperature		8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.



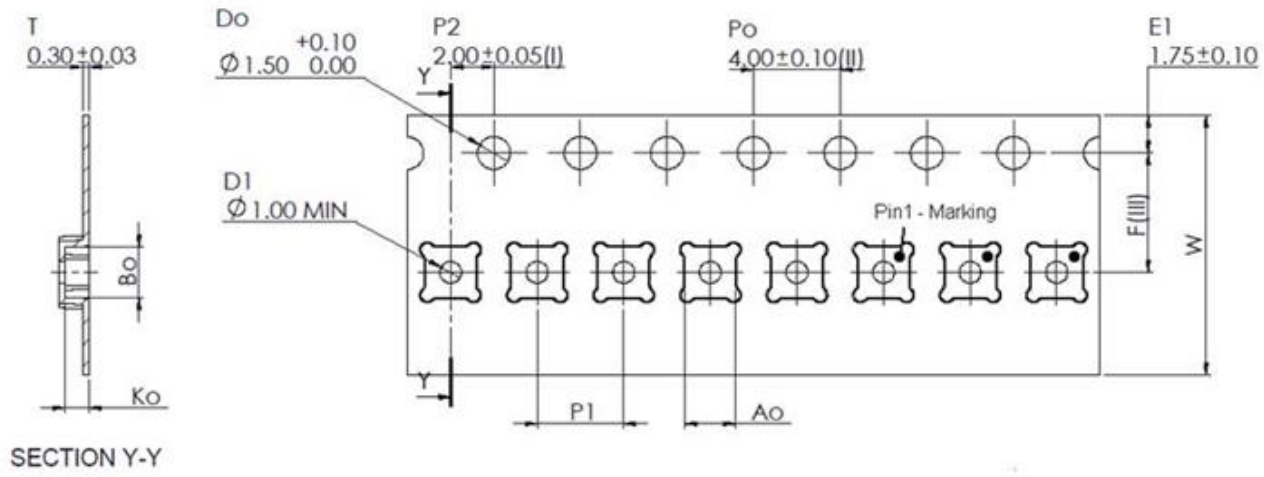
8.6 Handling instructions

Micromechanical sensors are designed to sense acceleration with high accuracy even at low amplitudes and contain highly sensitive structures inside the sensor element. The MEMS sensor can tolerate mechanical shocks up to several thousand g's. However, these limits might be exceeded in conditions with extreme shock loads such as e.g. hammer blow on or next to the sensor, dropping of the sensor onto hard surfaces etc.

We recommend to avoid g-forces beyond the specified limits during transport, handling and mounting of the sensors in a defined and qualified installation process.

This device has built-in protections against high electrostatic discharges or electric fields (e.g. 2kV HBM); however, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

8.7 Tape and Reel specification



Ao	2.35 +/- 0.05
Bo	2.30 +/- 0.05
Ko	1.10 +/- 0.05
F	5.50 +/- 0.05
P1	4.00 +/- 0.10
W	12.00 +0.30 / -0.10

8.8 Environmental safety

The BMA490L sensor meets the requirements of the EC restriction of hazardous substances (RoHS) directive, see also:

Directive 2015/863 (amending Annex II to Directive 2011/65/EU) of the European Parliament and of the Council on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Halogen content

The BMA490L is halogen-free. For more details on the corresponding analysis results please contact your Bosch Sensortec representative.

Internal package structure

Within the scope of Bosch Sensortec's ambition to improve its products and secure the mass product supply, Bosch Sensortec qualifies additional sources (e.g. 2nd source) for the LGA package of the BMA490L.

While Bosch Sensortec took care that all of the technical packages parameters are described above are 100% identical for all sources, there can be differences in the chemical content and the internal structural between the different package sources.

However, as secured by the extensive product qualification process of Bosch Sensortec, this has no impact to the usage or to the quality of the BMA490L product.

9. Legal disclaimer

9.1 Engineering samples

Engineering Samples are marked with an asterisk (*), (E) or (e). Samples may vary from the valid technical specifications of the product series contained in this data sheet. They are therefore not intended or fit for resale to third parties or for use in end products. Their sole purpose is internal client testing. The testing of an engineering sample may in no way replace the testing of a product series. Bosch Sensortec assumes no liability for the use of engineering samples. The Purchaser shall indemnify Bosch Sensortec from all claims arising from the use of engineering samples.

9.2 Product use

Bosch Sensortec products are developed for the consumer goods industry. They may only be used within the parameters of this product data sheet. They are not fit for use in life-sustaining or safety-critical systems. Safety-critical systems are those for which a malfunction is expected to lead to bodily harm, death or severe property damage. In addition, they shall not be used directly or indirectly for military purposes (including but not limited to nuclear, chemical or biological proliferation of weapons or development of missile technology), nuclear power, deep sea or space applications (including but not limited to satellite technology).
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9.3 Application examples and hints

With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Bosch Sensortec hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights or copyrights of any third party. The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. They are provided for illustrative purposes only and no evaluation regarding infringement of intellectual property rights or copyrights or regarding functionality, performance or error has been made.

10. Document history and modification

Rev. No	Chapter	Description of modification/changes	Date
1.0	All	Public release	06.2020
2.0	9	Disclaimer update	11.2020
2.1	1.1 4.7	Offset value update Integrated feature set update	03.2021

***Longevity Disclaimer**

Bosch Sensortec strives to maintain the supply of longevity product variants for a period of 10 years (from SOD/product introduction date), including the notification period. During such period, in case of significant volume decrease or manufacturing changes Bosch Sensortec may decide to

(i) replace the product by another (comparable) product
and/or
(ii) change the technology, manufacturing facilities and/or process

Any change will be notified to customers using the standard Bosch Sensortec product/process change policy (PCN)

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Document number: BST-BMA490L-DS000-03
Revision_2.1_032021