

Paper Title *TODO edit*

1st Given Name Surname
Faculty of Computer Science and Mathematics
OTH Regensburg
Regensburg, Germany
name.surname@st.oth-regensburg.de

Abstract—text

Index Terms—keyword1, keyword2

I. INTRODUCTION

- A. Overview
- B. Motivation
- C. Goal

II. BACKGROUND

- A. Instruction Set Architectures
- B. RISC
- C. ARM
text
- D. RISC-V
text

III. CONCEPT AND METHODS

A. Business Models

Who develops the CPU cores, how can you get access to them? Who supports chip manufacturers in designing a chip with that CPU core?

B. Complexity

How many instructions are there? How complex does that make the implementation of a core?

C. Performance

What are the differences in code size? Can we accurately compare the execution speed of both ISAs?

D. Extensibility

What instruction set extensions are there for both ISAs? Who can develop new extensions?

E. Ecosystem

Which compilers support ARM and RISC-V? Which operating systems and libraries?

IV. DISCUSSION

A. ARM

What are the advantages of ARM compared to RISC-V?

B. RISC-V

What are the advantages of RISC-V compared to ARM?

C. Future directions and challenges

How can we more accurately measure performance differences between ARM and RISC-V and how do ISA extensions affect performance?

V. CONCLUSION AND OUTLOOK

- A. Summary of results
- B. Accuracy of results
- C. Future directions

VI. OVERVIEW OF LITERATURE

Alexander Schmid [1] [2] [3] [4] [5] [6] [7] [8] [9]

Florian Henneke [8] [10] [3] [11] [12] [13] [14] [12]

REFERENCES

- [1] A. Akram, "A Study on the Impact of Instruction Set Architectures on Processor's Performance," Ph.D. dissertation, Western Michigan University, 08 2017.
- [2] *Arm® Architecture Reference Manual. Armv8, for Armv8-A architecture profile*, Issue F.c ed., ARM, Jul. 2020.
- [3] K. Asanović and D. A. Patterson, "Instruction Sets Should Be Free: The Case For RISC-V," University of California, Berkeley, Tech. Rep. UCB/EECS-2014-146, 2014.
- [4] Heui Lee, P. Beckett, and B. Appelbe, "High-performance extendable instruction set computing," in *Proceedings 6th Australasian Computer Systems Architecture Conference. ACSAC 2001*, 2001, pp. 89–94.
- [5] D. Patterson, J. Bennett, P. Dabbelt, C. Garlati, and O. Shinaar, "Initial Evaluation of Multiple RISC ISAs using the Embench™ Benchmark Suite," Dec. 2019, accessed on 2020-10-24. [Online]. Available: <https://riscv.org/wp-content/uploads/2019/12/12.10-12.50a-Code-Size-of-RISC-V-versus-ARM-using-the-Embench%E2%84%A2-0.5-Benchmark-Suite-What-is-the-Cost-of-ISA-Simplicity.pdf>
- [6] M. Perotti, P. D. Schiavone, G. Tagliavini, D. Rossi, T. Kurd, M. Hill, L. Yingying, and L. Benini, "HW/SW Approaches for RISC-V Code Size Reduction," in *Workshop on Computer Architecture Research with RISC-V. CARRV 2020*, 2020.
- [7] C. Shore, *ARMv8-A Architecture Overview*, ARM Limited, Sep. 2015.
- [8] A. S. Waterman, "Design of the RISC-V Instruction Set Architecture," Ph.D. dissertation, University of California, Berkeley, 2016.
- [9] X. H. Xu, S. R. Jones, and C. T. Clarke, "ARM/THUMB code compression for embedded systems," in *Proceedings of the 12th IEEE International Conference on Fuzzy Systems (Cat. No.03CH37442)*, 2003, pp. 32–35.
- [10] L. Ryzhyk, "The ARM Architecture," Tech. Rep., 2006.
- [11] S. Furber, *ARM System-on-Chip Architecture*, 2000, no. a.
- [12] Microsoft, "Windows 10 on ARM," 2020. [Online]. Available: <https://docs.microsoft.com/en-us/windows/uwp/porting/apps-on-arm>
- [13] Greenwaves Technologies, "Arm® Mbed™ OS Porting Manual for GAP8," accessed on 2020-10-28. [Online]. Available: <https://greenwaves-technologies.com/manuals/BUILD/MBED-OS/html/index.html>
- [14] Amazon Web Services, "Using FreeRTOS on RISC-V Microcontrollers," accessed on 2020-10-28. [Online]. Available: <https://www.freertos.org/Using-FreeRTOS-on-RISC-V.html>