Advantages and disadvantages of the RISC-V ISA (Instruction Set Architecture) in comparison to the ARMv8 ISA

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***Index Terms*—keyword1, keyowrd2**

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II. Background

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In order to determine whether RISC-V will gain a significant market share in the following years, it is useful to compare the two Instruction Set Architectures (ISAs) across a set of criteria that are relevant to semiconductor companies when evaluating which ISA to use with a new CPU design.

The first of these criteria is the ISA's business model. ISAs are often protected by patents that prohibit anyone not licensed by the patent owner from distributing Central Processing Units (CPUs) that implement that ISA. [1] Whether these patents exist and the licensing terms are an important factor when deciding which ISA to use.

The ISA's complexity refers to the amount of effort required to implement the ISA. The more complex an ISA is, the more developer time is spent on implementing and verifying a CPU's compatibility to the ISA, instead of optimizing the CPU for performance and efficiency, increasing a CPU's development cost.

A CPU's performance can be evaluated under multiple aspects, including the rate of instructions, the rate of floating point operations or the speed at which the CPU executes a given program. Efficiency considerations, such as the code size of a given program when compiled to the CPU's instruction set or the amount of power the CPU consumes when executing a given program are closely related to performance and shall, for the purposes of this paper, be grouped under performance.

A program's code size is greatly influenced by the ISA, since the instruction set and the compiler used are the only two factors that influence code size. As such, the code size is an important factor to consider when choosing which ISA to implement for a new processor design, especially for microcontrollers that are usually very constrained in the size of their program memory. For the other performance aspects, it is debatable to which extent they are influenced by the CPU's instruction set as opposed to the concrete implementation of the CPU. [2] [3]

ISAs often allow for a number of instruction set extensions that may or may not be implemented by a given CPU. These usually allow faster and more efficient processing of programs for a given use case, such as Single Instruction, Multiple Data (SIMD) extensions that optimize signal processing and media applications, Advanced Encryption Standard (AES) extensions that optimize cryptography or ISA-extensions with shorter instructions for applications that are constrained in program memory. Having a small base instruction set with many fine grained extensions improves the flexibility of the ISA, allowing CPUs to be optimized for specific use cases, increasing performance and efficiency for those use cases. ISA extensions do however pose a disadvantage when distributing

precompiled software to end users, as a piece of software that uses a certain ISA extension can't be executed on CPUs that don't implement that extension, potentially increasing the number of different versions of that software that need to be distributed.

An ISA's ecosystem refers to the software that supports that ISA, especially compilers that compile to that ISA, operating systems and libraries. When developing a new CPU it is preferrable to use an ISA with a large ecosystem, in order to maximize the amount of software that can run of that CPU. This is especially important in consumer desktop and mobile devices where a large variety of software is to be executed, but less important in embedded applications, where the software running on a microcontroller is specifically developed for that application and microcontroller only.

A. Business Models

When taking a look at the business model of the two rivaling ISAs one will detect two substantially different approaches. While ARM takes the traditional approach of licensing its intellectual property to semiconductor companies, RISC-V stands out with the completley different way of publishing its ISA in an open source manner. This includes giving away their ISA definition for free, which raises the standard questions concerning open source material: How is it financed?, How will it be sustained in the future?, What are the advantages? and so on.

But lets start at the classic business model: ARM sells its ISAs in various licensing models. [4] These are staggerd in multiple levels of access. The 'Desing Start' level includes free access to the ISA Defintion of the simplest ARM Chips Cortex-M0 and Cortex-M3 aswell as a fitting toolchain and processor models. For a fee between $0 and $75K you can get the ISA of the Cortex-A5 aswell as the permission for 'single use' chip production. This means you are allowed to produce and sell one type of chip for a single purpose e.g. a network controller. For every chip produced a royality must be given to ARM. The 'Design Start' access level also includes a license for accessing a 'artisan physical IP library', a license for universities which includes teaching and prototyping and allows production of own chips without royalities in low margins. At last there is a FPGA license which is free and includes a Field-programmable Gate Array (FPGA) optimized version of the Cortex-M3 and M1. Production is not allowed in this license.

The next level of access is called 'Flexible Access' and contains two license models one for $0 to $75K which allows one tape-out per year. On top of the entry price one pays per used processor design and a royality per produced chip. The other model starts at $200K per year and uses the same payment additions as the first one. But it allows unlimited tape-outs and includes employee trainings, design tools and design support.

Above those access levels, there only officially exits the 'Standard' licensing model. This means one makes a individual contract with ARM. Several articles from 2013 [5] [6] talk about an older licensing model which contains special categories for higher access licenses. The highest of these, often refered as the 'Architectural' license is the only one that allows to edit the ISA and develop completely freely. The most prominent companies with such a license are Qualcom which develops and sells mobile phone chips and Apple which does the same and just announced a 'Apple Silicon' developed laptop chip on ARM basis. [7] The article also mentions that preparing a licenese of this form often takes about 6-24 months and talks about per chip royalities of about 1-2.5%. It also notices so called 'foundry contracts' where customers can buy silicon ready ARM designs in cooperation with a silicon foundry. Most prominet example here are the Mali GPUs. This offers customers a fast and easy possibility to expand their chip with for example graphic accelerators.

Contrary to the ARM license model RISC-V is published using the 'Creative Commons Attribution 4.0' license. [8] [9] This license allows to 'share' and 'adapt'. This means you are free to copy and redistribute aswell as modify, change, build upon and sell it commercially. It is not necessary to share changes in an open source way and you are only restricted by giving credit to the original licensor. [10] An important addition is also, that the license cannot be revoked by the licensor. This means everything about RISC-V that is already published will always be free to use! Originally founded by Berkley University the RISC-V ISA standard is now managed by the 2015 founded nonprofit organization 'RISC-V International'. [11] Beeing a nonprofit already implies that there should be no massive income for the organization. Running expenses and the further development of the standard do however require certain liquidity. This is ensured by a membership program surrounding the specification. [12] Resembling the ARM licensing model, it contains three levels: 'Premier', 'Strategic' and 'Community'. Costing between $2K and $250K annually these levels do not restrict access to the ISA, but grant several levels of taking influence on the future development of the standard through seats in the 'Technical Steering Commitee', speaker slots on conferences and representation on the official RISC-V International website and blog. There are also three 'Strategic Directors', which are votet out of the 'Premier' and 'Strategic' Members and one Academic aswell as one Communtiy Director, which are votet by the 'Communtiy' level of members. [13]

Besides taking incfluence in the development process the membership also includes help in designing CPU Cores, teching for employes and more. It also allows the usage of the trademark 'RISC-V'.

B. Structure and Complexity

How many instructions are there? How complex does that make the implementation of a core?

C. Performance

What are the differences in code size? Can we accurately compare the execution speed of both ISAs?

D. Extensibility

What instruction set extensions are there for both ISAs? Who can develop new extensions?

E. Ecosystem

Which compilers support ARM and RISC-V? Which operating systems and libraries?

IV. Discussion

A. ARM

What are the advantages of ARM compared to RISC-V?

B. RISC-V

What are the advantages of RISC-V compared to ARM?

C. Future directions and challenges

How can we more accurately measure performance differences between ARM and RISC-V and how do ISA extensions affect performance?

V. Conclusion and Outlook

A. Summary of results

B. Interpretation of results

C. Future directions

VI. Overview of Literature

Alexander Schmid [3] [14] [15] [16] [17] [18] [19] [20] [21]

Florian Henneke [20] [22] [15] [23] [24] [25] [26] [24]

Michael Schneider [27] [28] [29] [30] [31] [32] [33]

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