Advantages and disadvantages of the RISC-V ISA (Instruction Set Architecture) in comparison to the ARMv8 ISA

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***Abstract*—text**
***Index Terms*—keyword1, keyowrd2**

I. Introduction

A. Topic

B. Motivation

C. Goal

D. Overview of paper

II. Background

A. Instruction Set Architectures

B. RISC

C. ARM

text

D. RISC-V

text

III. Concept and Methods (Initial section written by Alexander Schmid)

Given that the goal of this paper is to compare the two Instruction Set Architectures (ISAs) across a set of criteria that are relevant to semiconductor companies when evaluating which ISA to use with a new CPU design, these criteria shall be defined in the following section.

The first of these criteria is the ISA's business model. ISAs are often protected by patents that prohibit anyone not licensed by the patent owner from distributing Central Processing Units (CPUs) that implement that ISA. [1]

Whether these patents exist and the licensing terms are an important factor when deciding which ISA to use.

The ISA's complexity refers to the amount of effort required to implement the ISA. The more complex an ISA is, the more developer time is spent on implementing and verifying the implementation of the ISA, instead of optimizing the CPU for performance and efficiency, increasing a CPU's development cost. [2]

A CPU's performance usually refers to the speed at which the CPU executes a given program. Efficiency considerations, such as the code size of a given program or the amount of power the CPU consumes when executing a given program are closely related to performance and shall, for the purposes of this paper, be grouped under performance.

ISAs often allow for a number of instruction set extensions that may or may not be implemented by a given CPU. The choice of extensions greatly influence the flexibility of an ISA. Thus they are an important factor to consider which ISA to implement for a new CPU, because these have a large impact on performance and development cost of a CPU.

An ISA's ecosystem refers to the software that supports that ISA, especially compilers that compile to that ISA, operating systems and libraries. When developing a new CPU it is preferrable to use an ISA with a large ecosystem, in order to maximize the amount of software that can run of that CPU. This is especially important in consumer desktop and mobile devices where a large variety of software is to be executed.

A. Business Models (written by Florian Henneke)

When taking a look at the business model of the two rivaling ISAs one will detect two substantially different approaches. While ARM takes the traditional path of licensing its intellectual property to semiconductor companies, RISC-V stands out with the completely different way of publishing its ISA in an open source manner. This includes giving away their ISA definition for free, which raises the standard questions criticizing open source material.

Beginning with the classic model of ARM, the following sections will cover the two license models: ARM sells its ISAs in various licensing models. [3] These are staggered in multiple levels of access. The 'Design Start' level includes free access to the IP-Core of the simplest ARM Chips Cortex-M0 and Cortex-M3 aswell as the corresponding toolchain and processor models. For a fee between $0 and $75K the IP-Core of the Cortex-A5 aswell as the permission for 'single use' chip production can be aquired. This allows the customer to produce and sell one type of chip for a single purpose e.g. a network controller. For every chip produced, a royality must be given to ARM. The 'Design Start' access level also includes a license for accessing a 'artisan physical IP library', a license for universities which includes teaching and prototyping and allows non commercial production of own chips without royalities in small volumes. At last there is an 'FPGA' license which is free and includes a Field-programmable Gate Array (FPGA) optimized version of the Cortex-M3 and M1. Production is not allowed with this license.

The next level of access is called 'Flexible Access' and contains two license models, one for $0 to $75K which allows one tape-out per year. On top of the entry price one pays per used processor design and a royality per produced chip. The other model starts at $200K per year and uses the same payment additions as the first one. But it allows unlimited tape-outs and includes employee trainings, design tools and design support.

Above those access levels, there only officially exists the 'Standard' licensing model. This means one makes a individual contract with ARM. Several articles from 2013 [4] [5] talk about an older licensing model which contains special categories for higher access licenses. The highest of these, often referred as the 'Architectural' license is the only one that allows editing of the ISA and developing completely freely. The most prominent companies with such a license are Qualcomm which develops and sells mobile phone chips and Apple who just announced a 'Apple Silicon' developed laptop chip based on ARM. [6] The article also mentions that preparing a license of this form often takes about 6-24 months and states per-chip royalities of about 1-2.5%. It also notices so called 'foundry contracts' where customers can buy silicon ready ARM designs in cooperation with a silicon foundry. The most prominent example here are the Mali GPUs. This offers customers a fast and easy way to expand their chip with, for example, graphic accelerators.

In contrast to the ARM license model, RISC-V is published using the 'Creative Commons Attribution 4.0' license. [7] [8] This license allows the user to 'share' and 'adapt'. This means you are free to copy and redistribute as well as modify, change, build upon and sell it commercially. It is not necessary to share changes in an open source manner and you are only restricted by the obligation to give credit to the original licensor. [9] An important addition is also, that the license cannot be revoked by the licensor. This means everything about RISC-V that is already published will always be free to use. Originally founded by Berkley University, the RISC-V ISA standard is now managed by the nonprofit organization 'RISC-V International', founded in 2015. [10] As the statutes of the organization include, the association has 'no pecunuary, self-help or commercial purpose' [11]. Running expenses and further development of the standard do however require a certain liquidity. This is ensured by a membership program surrounding the specification. [12] Resembling the ARM licensing model, it contains three levels: 'Premier', 'Strategic' and 'Community'. Costing between $2K and $250K annually, these levels do not restrict access to the ISA, but grant several levels of taking influence on the future development of the standard through seats in the 'Technical Steering Commitee', speaker slots on conferences and representation on the official RISC-V International website and blog. There are also three 'Strategic Directors', which are elected out of the 'Premier' and 'Strategic' Members and one Academic as well as one Communtiy Director, which is elected by the 'Communtiy' level of members. [13]

Besides taking influence in the development process, the membership also includes help in designing CPU Cores, teaching for employees and more. It also allows the usage of the trademark 'RISC-V'.

B. Structure and Complexity

How many instructions are there? How complex does that make the implementation of a core?

C. Performance (written by Alexander Schmid)

Code size is the performance parameter most influenced by the ISA and not by the CPU's implementation, given that the ISA and the compiler are the only two factors that influence code size. For the other performance aspects, the influence of the ISA is debatable [14] [15], so code size shall be the main focus of the performance comparison. Given that code size is most critical in embedded applications, the Embench benchmark suite is a good benchmark with which to compare code sizes. It consists of a number of programs frequently used in embedded applications, such as CRC, signal filtering, AES and QR code reading. [16] When compiling the Embench suite for both RV32IMC as well as 32-bit ARM with the Thumb-2 extension using GCC 7, the code for RISC-V is approximately 11% larger than the code for ARM. [17] Part of this gap in code size can be explained by the relative immaturity of the RISC-V implementation of GCC. RISC-V was introduced in 2017 and the code size of the Embench suite compiled for RISC-V is lower with newer versions of GCC, however it is still larger than the code generated for ARM as of 2019. [16]

In [17] an extension for RISC-V is introduced, called HCC, that is aimed at reducing the code size of RISC-V. This extension brings the code size gap down to 2.2% for the Embench suite and makes the RISC-V code smaller than ARM by 1.75% in a proprietary IoT benchmark developed by Huawei. [17]

TODO: In subsequent submissions, mention RV64 being significantly smaller than AArch64 as described in [18, page

62], and possibilities of comparing execution speed and energy efficiency as described in [14] and [15].

D. Extensibility

What instruction set extensions are there for both ISAs? Who can develop new extensions?

E. Ecosystem

Which compilers support ARM and RISC-V? Which operating systems and libraries?

IV. Discussion

A. Advantages of ARM

What are the advantages of ARM compared to RISC-V?

B. Advantages of RISC-V

What are the advantages of RISC-V compared to ARM?

C. Future directions and challenges

How can we more accurately measure performance differences between ARM and RISC-V and how do ISA extensions affect performance?

V. Conclusion and Outlook

A. Summary of results

B. Interpretation of results

C. Future directions

VI. Overview of Literature

Alexander Schmid [15] [19] [20] [21] [16] [17] [22] [18] [23]

Florian Henneke [18] [24] [20] [25] [26] [27] [28] [26]

Michael Schneider [29] [30] [31] [32] [33] [34] [35]

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