A comparison of the ARMv8 and RISC-V Instruction Set Architectures

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Abstract—text
Index Terms—keyword1, keyowrd2

I. Introduction

- A. Overview
- B. Motivation
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II. BACKGROUND

- A. Instruction Set Architectures
- B. RISC
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D. RISC-V

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III. CONCEPT AND METHODS

In order to determine whether RISC-V will gain a significant market share in the following years, it is useful to compare the two Instruction Set Architectures (ISAs) across a set of criteria that are relevant to semiconductor companies when evaluating which ISA to use with a new CPU design.

The first of these criteria is the ISA's business model. ISAs are often protected by patents that prohibit anyone not licensed by the patent owner from distributing Central Processing Units (CPUs) that implement that ISA. [1] Whether these patents exist and the licensing terms are an important factor when deciding which ISA to use.

The ISA's complexity refers to the amount of effort required to implement the ISA. The more complex an ISA is, the more developer time is spent on implementing and verifying a CPU's compatibility to the ISA, instead of optimizing the CPU for performance and efficiency, increasing a CPU's development cost.

TODO Performance: Dope source [2]

A. Business Models

Who develops the CPU cores, how can you get access to them? Who supports chip manufacturers in designing a chip with that CPU core?

B. Complexity

How many instructions are there? How complex does that make the implementation of a core?

C. Performance

What are the differences in code size? Can we accurately compare the execution speed of both ISAs?

D. Extensibility

What instruction set extensions are there for both ISAs? Who can develop new extensions?

E. Ecosystem

Which compilers support ARM and RISC-V? Which operating systems and libraries?

IV. DISCUSSION

A. ARM

What are the advantages of ARM compared to RISC-V?

B. RISC-V

What are the advantages of RISC-V compared to ARM?

C. Future directions and challenges

How can we more accurately measure performance differences between ARM and RISC-V and how do ISA extensions affect performance?

V. CONCLUSION AND OUTLOOK

- A. Summary of results
- B. Accuracy of results
- C. Future directions

VI. OVERVIEW OF LITERATURE

Alexander Schmid [3] [4] [5] [6] [7] [8] [9] [10] [11] Florian Henneke [10] [12] [5] [13] [14] [15] [16] [14] Michael Schneider [17] [18] [19] [20] [21] [22] [23]

REFERENCES

- [1] G. Tang and I. W. Brown, "Intel and the x86 Architecture: A Legal Perspective," Harvard Journal of Law & Technology Digest, 2011, accessed on 2020-11-02. [Online]. Available: https://jolt.law.harvard.edu/digest/intel-and-the-x86-architecture-a-legal-perspective
- [2] E. Blem, J. Menon, and K. Sankaralingam, "Power struggles: Revisiting the risc vs. cisc debate on contemporary arm and x86 architectures," in 2013 IEEE 19th International Symposium on High Performance Computer Architecture (HPCA), 2013, pp. 1–12.
- [3] A. Akram, "A Study on the Impact of Instruction Set Architectures on Processor's Performance," Ph.D. dissertation, Western Michigan University, 08 2017.
- [4] Arm® Architecture Reference Manual. Armv8, for Armv8-A architecture profile, Issue F.c ed., ARM, Jul. 2020.
- [5] K. Asanović and D. A. Patterson, "Instruction Sets Should Be Free: The Case For RISC-V," University of California, Berkeley, Tech. Rep. UCB/EECS-2014-146, 2014.
- [6] Heui Lee, P. Beckett, and B. Appelbe, "High-performance extendable instruction set computing," in *Proceedings 6th Australasian Computer* Systems Architecture Conference. ACSAC 2001, 2001, pp. 89–94.
- [7] D. Patterson, J. Bennett, P. Dabbelt, C. Garlati, and O. Shinaar, "Initial Evaluation of Multiple RISC ISAs using the Embench™ Benchmark Suite," Dec. 2019, accessed on 2020-10-24. [Online]. Available: https://riscv.org//wp-content/uploads/2019/12/12.10-12. 50a-Code-Size-of-RISC-V-versus-ARM-using-the-Embench%E2% 84%A2-0.5-Benchmark-Suite-What-is-the-Cost-of-ISA-Simplicity.pdf
- [8] M. Perotti, P. D. Schiavone, G. Tagliavini, D. Rossi, T. Kurd, M. Hill, L. Yingying, and L. Benini, "HW/SW Approaches for RISC-V Code Size Reduction," in Workshop on Computer Architecture Research with RISC-V. CARRV 2020, 2020.
- [9] C. Shore, ARMv8-A Architecture Overview, ARM Limited, Sep. 2015.
- [10] A. S. Waterman, "Design of the RISC-V Instruction Set Architecture," Ph.D. dissertation, University of California, Berkeley, 2016.
- [11] X. H. Xu, S. R. Jones, and C. T. Clarke, "ARM/THUMB code compression for embedded systems," in *Proceedings of the 12th IEEE International Conference on Fuzzy Systems (Cat. No.03CH37442)*, 2003, pp. 32–35.
- [12] L. Ryzhyk, "The ARM Architecture," Tech. Rep., 2006.
- [13] S. Furber, ARM System-on-Chip Architecture, 2000, no. a.
- [14] Microsoft, "Windows 10 on ARM," 2020. [Online]. Available: https://docs.microsoft.com/en-us/windows/uwp/porting/apps-on-arm
- [15] Greenwaves Technologies, "Arm® Mbed™ OS Porting Manual for GAP8 ," accessed on 2020-10-28. [Online]. Available: https://greenwaves-technologies.com/manuals/BUILD/MBED-OS/html/index.html
- [16] Amazon Web Services, "Using FreeRTOS on RISC-V Microcontrollers," accessed on 2020-10-28. [Online]. Available: https://www.freertos.org/ Using-FreeRTOS-on-RISC-V.html
- [17] G. David Patterson and U. Berkeley, "50 years of computer architecture," 2018.
- [18] J. Hennessy, Computer architecture: a quantitative approach. Waltham, MA: Morgan Kaufmann, 2012.
- [19] R. D. Vladimir Herdt, Daniel Große, Enhanced virtual prototyping featuring risc-v case studies. S.I: SPRINGER NATURE, 2020.
- [20] M. D. H. of Wisconsin-Madison; Dave Christie; David Patterson; Joshua J. Yi; Derek Chiou; Resit Sendag, "Proprietary versus open instruction sets," *IEEE Micro*, 2016.
- [21] S. Higginbotham, "The Rise of RISC," IEEE Spectrum, 2018.

- [22] R. Dirvin, "The arm ecosystem: More than just an ecosystem, it's oxygen for soc design teams," April 2019. [Online]. Available: https://www.arm.com/company/news/2019/04/ the-arm-ecosystem-more-than-just-an-ecosystem
- [23] Z. Bandic, IEEE Computing Society, March 2019. [Online]. Available: http://www.hsafoundation.com/ the-inherent-freedom-of-heterogeneous-systems/