CV32E40P	OpenHW Group	GitHub	RV32	1.11	RV32IM[F]C
Ibex (formerly Zero-riscy)	lowRISC	GitHub	RV32	1.11	RV32I[M]C/RV32E[M]C
CVA6	OpenHW Group	GitHub	RV32,RV64	1.11	RV[32/64]GC
Riscy Processors	MIT CSAIL CSG	Website,GitHub	RV32,RV64		
RiscyOO	MIT CSAIL CSG	GitHub	RV64	1.10	RV64IMAFD
Lizard	Cornell CSL BRG	GitHub	RV64		RV64IM
Minerva	LambdaConcept	GitHub	RV32	1.10	RV32I
OPenV/mriscv	OnChipUIS	GitHub	RV32		RV32I(?)
VexRiscv	SpinalHDL	GitHub	RV32		RV32I[M][C]
Roa Logic RV12	Roa Logic	GitHub	RV32	1.9.1	2.1
SCR1	Syntacore	GitHub	RV32	1.10	2.2, RV32I/E[MC]
SCR3	Syntacore	Website	RV32,RV64	1.10	RV[32/64]IMC[A], 2.2, milticore
SCR4	Syntacore	Website	RV32,RV64	1.10	RV[32/64]IMCF[DA], 2.2, milticore
SCR5	Syntacore	Website	RV32,RV64	1.10	RV[32/64]IMC[FDA], 2.2, milticore
SCR7	Syntacore	Website	RV64	1.10	RV64GC, 2.2, milticore

ReonV	Lucas Castro	GitHub	RV32		
PicoRV32	Clifford Wolf	GitHub	RV32		RV32I/E[MC]
MR1	Tom Verbeure	GitHub	RV32		RV32I
SERV	Olof Kindgren	GitHub	RV32		RV32I
SweRV EH1	Western Digital Corporation	GitHub	RV32	1.11	2.1, RV32IMC
SweRV EL2	Western Digital Corporation	GitHub	RV32	1.11	2.1, RV32IMC
SweRV EH2	Western Digital Corporation	GitHub	RV32	1.11	2.1, RV32IMAC
biRISC-V	UltraEmbedded	GitHub	RV32	1.11	RV32I[M]
Reve-R	Gavin Stark	GitHub	RV32	1.10	RV32IMAC
Bk3	Codasip	Website	RV32	1.10	RV32EMC / RV32IM[F]C
Bk5	Codasip	Website	RV32	1.10	RV32IM[F]C / RV64IM[F]C
Bk7	Codasip	Website	RV64	1.10	RV64IMA[F][D][C]
DarkRISCV	Darklife	GitHub	RV32		most of RV32I
RPU	Domipheus Labs	GitHub	RV32		RV32I
RV01	Stefano Tonello	OpenCores	RV32	1.7	2.1, RV32IM
N22	Andes	Website	RV32	1.11	RV32IMAC/EMAC + Andes V5/V5e ext.
N25F	Andes	Website	RV32	1.11	RV32GC + Andes V5 ext.

					Andes V5 ext.
A25MP	Andes	Website	RV32	1.11	RV32GCP + SV32 + Andes V5 ext. + Multi-core
NX25F	Andes	Website	RV64	1.11	RV64GC + Andes V5 ext.
AX25	Andes	Website	RV64	1.11	RV64GCP + SV39/48 + Andes V5 ext.
AX25MP	Andes	Website	RV64	1.11	RV64GCP + SV39/48 + Andes V5 ext. + Multi-core
Instant SoC	FPGA Cores	Website	RV32		RV32IM
Taiga	Reconfigurable Computing Lab, Simon Fraser University	GitLab	RV32		RV32IMA
Maestro	João Chrisóstomo	GitHub	RV32		RV32I
XuanTie C910	T-Head (Alibaba group)	Website	RV64	1.10	RV64GCV + SV39 + ISA Extension + Memory model Extension + multi-core & multi-cluster(16 cores maximum)
XuanTie E902	T-Head (Alibaba group)	Website	RV32	1.10	RV32EMC/IMC/EC
BM-310	CloudBEAR	Website	RV32	1.10	RV32IMC

BI-671	CloudBEAR	Website	RV64	1.10	RV64GC + multi-core
SSRV	risclite	Website,GitHub	RV32	1.10	RV32IMC
Tinyriscv	Blue Liang	GitHub	RV32		2.1, RV32I
RSD	rsd-devel	GitHub	RV32		RV32IM
Pluto	PQShield	Website	RV32	1.11	RV32I[M][C] / RV32E[M][C] + Crypto Functions
E2	SiFive	Website	RV32	1.11	RV32I(E)MAFC 2.2
S2	SiFive	Website	RV64	1.11	RV64GC 2.2
E3	SiFive	Website	RV32	1.11	RV32I(E)MAFDC 2.2
S5	SiFive	Website	RV64	1.11	RV64GC 2.2
U5	SiFive	Website	RV64	1.11	RV64GC 2.2
E7	SiFive	Website	RV32	1.11	RV32I(E)MAFDC 2.2
S7	SiFive	Website	RV64	1.11	RV64GC 2.2

N100	Nuclei	Website	RV32	1.11	RV32EC
N200	Nuclei	Website	RV32	1.11	RV32IC(E)(M)(A)
N300	Nuclei	Website	RV32	1.11	RV32IMAC(F)(D)(P)
N600	Nuclei	Website	RV32	1.11	RV32IMAC(F)(D)(P)
NX600	Nuclei	Website	RV32	1.11	RV64IMAC(F)(D)(P)
UX600	Nuclei	Website	RV64	1.11	RV64IMAC(F)(D)(P) + MMU-SV39
WH32	UC Techip	Website	RV32	1.10	RV32GCX
WARP-V	Steve Hoover, Redwood EDA	GitHub	RV32		RV32I[M][F]
NEORV32	Stephan Nolting	GitHub	RV32	1.12-draft	2.2, RV32[I/E][M][C]
Steel	Rafael Calcada	GitHub	RV32	1.11	RV32IZicsr
Klessydra-T13	Digital Systems Lab at Sapienza University of Rome	GitHub	RV32	1.11	RV32[I/E][M][A] + Kless-Vect