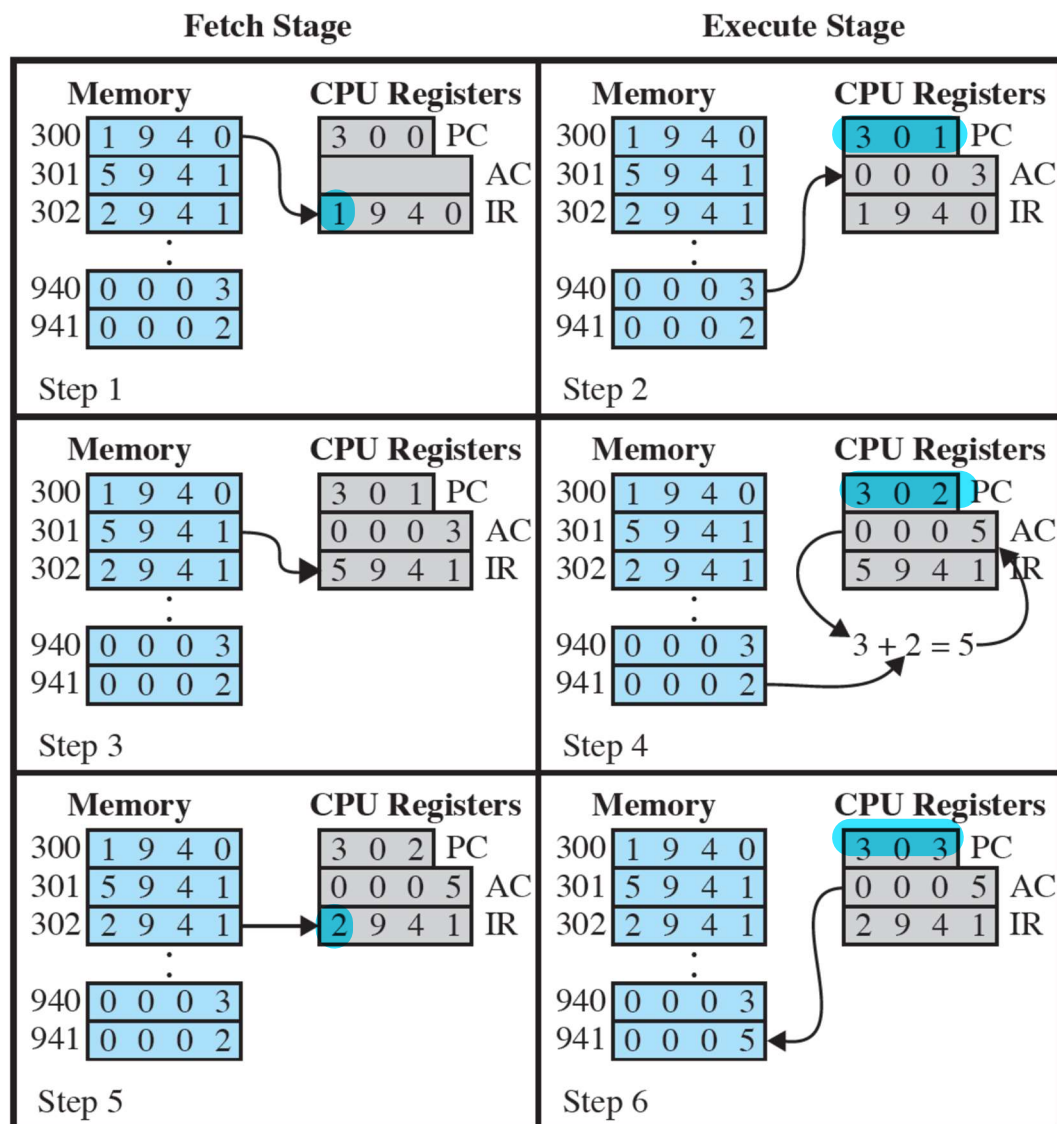1.   **Answer:**

Step 1:   Fetch the first instruction into the IR. (Since the PC contains 300, the address
            of the first instruction.)
Step 2a: Increment the PC to 301.
Step 2b: Load AC from the memory location 940.
Step 3:   Fetch the second instruction into the IR.
Step 4a: Increment the PC to 302.
Step 4b: Add to AC from the memory location 941.
Step 5:   Fetch the third instruction into the IR.
Step 6a: Increment the PC to 303.
Step 6b: Store AC to memory location 941.

Fetch Stage   **Execute Stage**

Step 1

Memory		CPU Registers	
300	1 9 4 0	3 0 0	PC
301	5 9 4 1		AC
302	2 9 4 1	1 9 4 0	IR
940	0 0 0 3		
941	0 0 0 2		

Step 2

Memory		CPU Registers	
300	1 9 4 0	3 0 1	PC
301	5 9 4 1	0 0 0 3	AC
302	2 9 4 1	1 9 4 0	IR
940	0 0 0 3		
941	0 0 0 2		

Step 3

Memory		CPU Registers	
300	1 9 4 0	3 0 1	PC
301	5 9 4 1	0 0 0 3	AC
302	2 9 4 1	5 9 4 1	IR
940	0 0 0 3		
941	0 0 0 2		

Step 4

Memory		CPU Registers	
300	1 9 4 0	3 0 2	PC
301	5 9 4 1	0 0 0 5	AC
302	2 9 4 1	5 9 4 1	IR
940	0 0 0 3		$3 + 2 = 5$
941	0 0 0 2		

Step 5

Memory		CPU Registers	
300	1 9 4 0	3 0 2	PC
301	5 9 4 1	0 0 0 5	AC
302	2 9 4 1	2 9 4 1	IR
940	0 0 0 3		
941	0 0 0 2		

Step 6

Memory		CPU Registers	
300	1 9 4 0	3 0 3	PC
301	5 9 4 1	0 0 0 5	AC
302	2 9 4 1	2 9 4 1	IR
940	0 0 0 3		
941	0 0 0 5		

2.   **Answer:**

The hit ratio has to be 0.95. Then the average time to access a word is

$(0.95)(0.1\mu s) + (0.05)(0.1\mu s + 1\mu s) = 0.095 + 0.055 = 0.15 \; \mu s$

$$x(0.1)+(1-x)(0.1+1)=0.1 \times 1.5$$

3.   **Answer:**

a)

- Spatial locality can be exploited by using larger cache blocks.
- Temporal locality can be exploited by keeping recently used instruction and data values in cache memory.

b)   transfer the whole block of data to the cache

(i)   A reference to the first instruction is immediately followed by a reference to the second.

(ii)   The ten accesses to `a[i]` within the inner for loop occur within a short interval of time.   Least Recent Used (LRU) -> low chance for using -> remove from cache

Self-test

1.   D
2.   C
3.   B
4.   D
5.   D
6.   A