

Tema de curs 1 – Alexandru Licuriceanu 332CD

Am implementat CLA-ul pe 16 biți folosind 4 CLA-uri pe 4 biți, ca la cursul de Structura și Organizarea Calculatoarelor. În interiorul arhivei se regăsesc atât fișierele cu codul sursă pentru sumatoare, cât și cel pentru testbench.

1. Rezultatele simulării:

```
1111110111101000 (65000) + 0000000000000000 (0) =  
1111110111101000 (65000) carry: 0 (CORRECT)  
  
1111110111101000 (65000) + 000000001111011 (123) =  
1111111001100011 (65123) carry: 0 (CORRECT)  
  
1111110111101000 (65000) + 0000000011110110 (246) =  
1111111011011110 (65246) carry: 0 (CORRECT)  
  
1111110111101000 (65000) + 0000000101110001 (369) =  
1111111101011001 (65369) carry: 0 (CORRECT)  
  
1111110111101000 (65000) + 0000000111101100 (492) =  
1111111111010100 (65492) carry: 0 (CORRECT)  
  
1111110111101000 (65000) + 0000001001100111 (615) =  
0000000001001111 (79) carry: 1 (CORRECT)  
  
1111110111101000 (65000) + 0000001011100010 (738) =  
0000000011001010 (202) carry: 1 (CORRECT)  
  
1111110111101000 (65000) + 0000001101011101 (861) =  
0000000101000101 (325) carry: 1 (CORRECT)  
  
1111110111101000 (65000) + 0000001111011000 (984) =  
0000000111000000 (448) carry: 1 (CORRECT)  
  
1111110111101000 (65000) + 0000010001010011 (1107) =  
0000001000111011 (571) carry: 1 (CORRECT)
```

2. Raportul generat de sinteza codului:

Synthesis Summary Report of 'cla_16bit'

General Information

Date: Sun Jan 14 21:03:38 2024
Version: 2023.1 (Build 3526262 on Mon Apr 18 15:48:16 MDT 2022)
Project: adder

Solution: solution1 (Vivado IP Flow Target)
Product Family: artix7
Target device: xc7a100t-csg324-1

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	6.590 ns	2.70 ns

Performance & Resource Estimates

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trips Count	Pipelined	BRAM	DSF	FF	LU	URAM	
cla_16bit				-	18	180.000		-	19	-	no	0	0	20	181	0
Vitis_LOOP_15_1_Vitis_LOOP_27_2				-	16	160.000		2	1	16	yes	-	-	-	-	-

HW Interfaces

AP_MEMORY

Interface	Bitwidth
a_address0	4
a_q0	1
b_address0	4
b_q0	1
sum_address0	4
sum_d0	1

REGISTER

Interface	Mode	Bitwidth
ap_return		1
carry_in	ap_none	1

TOP LEVEL CONTROL

Interface	Type	Ports
ap_clk	clock	ap_clk
ap_rst	reset	ap_rst
ap_ctrl	ap_ctrl_hs	ap_done ap_idle ap_ready ap_start

SW I/O Information

Top Function Arguments

Argument	Direction	Datatype
a	in	bool*
b	in	bool*
sum	out	bool*
carry_in	in	bool
return	out	bool

SW-to-HW Mapping

Argument	HW Interface	HW Type	HW Usage
a	a_address0	port	offset
a	a_ce0	port	
a	a_q0	port	
b	b_address0	port	offset
b	b_ce0	port	
b	b_q0	port	
sum	sum_address0	port	offset
sum	sum_ce0	port	
sum	sum_w00	port	
sum	sum_d0	port	
carry_in	carry_in	port	
return	ap_return	port	

Pragma Report

Valid Pragma Syntax

Bind Op Report

No filter settings

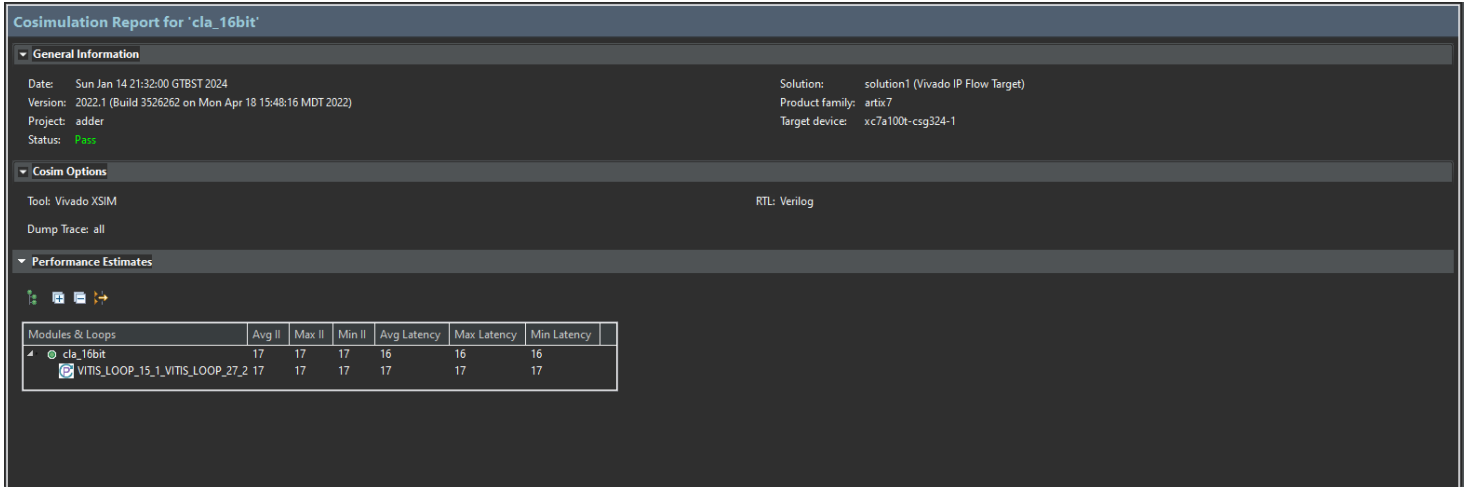
Name	DSF	Pragma	Variable	Op	Impl	Latency
cla_16bit						
Vitis_LOOP_15_1_Vitis_LOOP_27_2						

User config_op

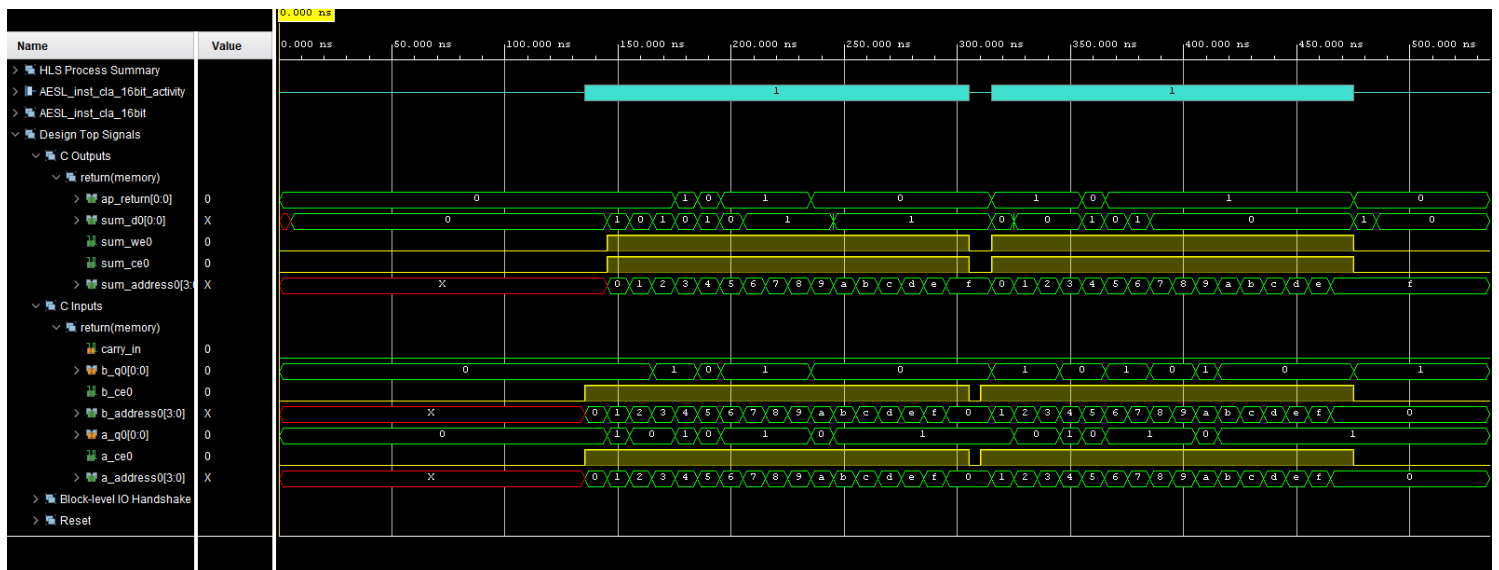
Op	Impl	Latency
mul	all mul	-1 mul
add	all add	-1 add
sub	all sub	-1 sub
fadd	all fadd	-1 fadd
fsub	all fsub	-1 fsub
fdv	all fdv	-1 fdv
fexp	all fexp	-1 fexp
flog	all flog	-1 flog
fmod	all fmod	-1 fmod
frqgt	all frqgt	-1 frqgt
frexp	all frexp	-1 frexp
fsqgt	all fsqgt	-1 fsqgt
dadd	all dadd	-1 dadd
dsub	all dsub	-1 dsub
ddiv	all ddiv	-1 ddiv
deexp	all deexp	-1 deexp
dlog	all dlog	-1 dlog
dmul	all dmul	-1 dmul
drqgt	all drqgt	-1 drqgt
drecip	all drecip	-1 drecip
dqgt	all dqgt	-1 dqgt

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3. Raportul co-simulării:



4. Formele de undă obținute prin co-simulare:



Pentru vizibilitate, aici apar doar alte două teste, anume:

```
1111110111101001 (65001) + 0000000111101100 (492) = 1111111111010101
(65493) carry: 0 (CORRECT)
1111110111101001 (65001) + 0000001001100111 (615) = 0000000001010000
(80) carry: 1 (CORRECT)
```