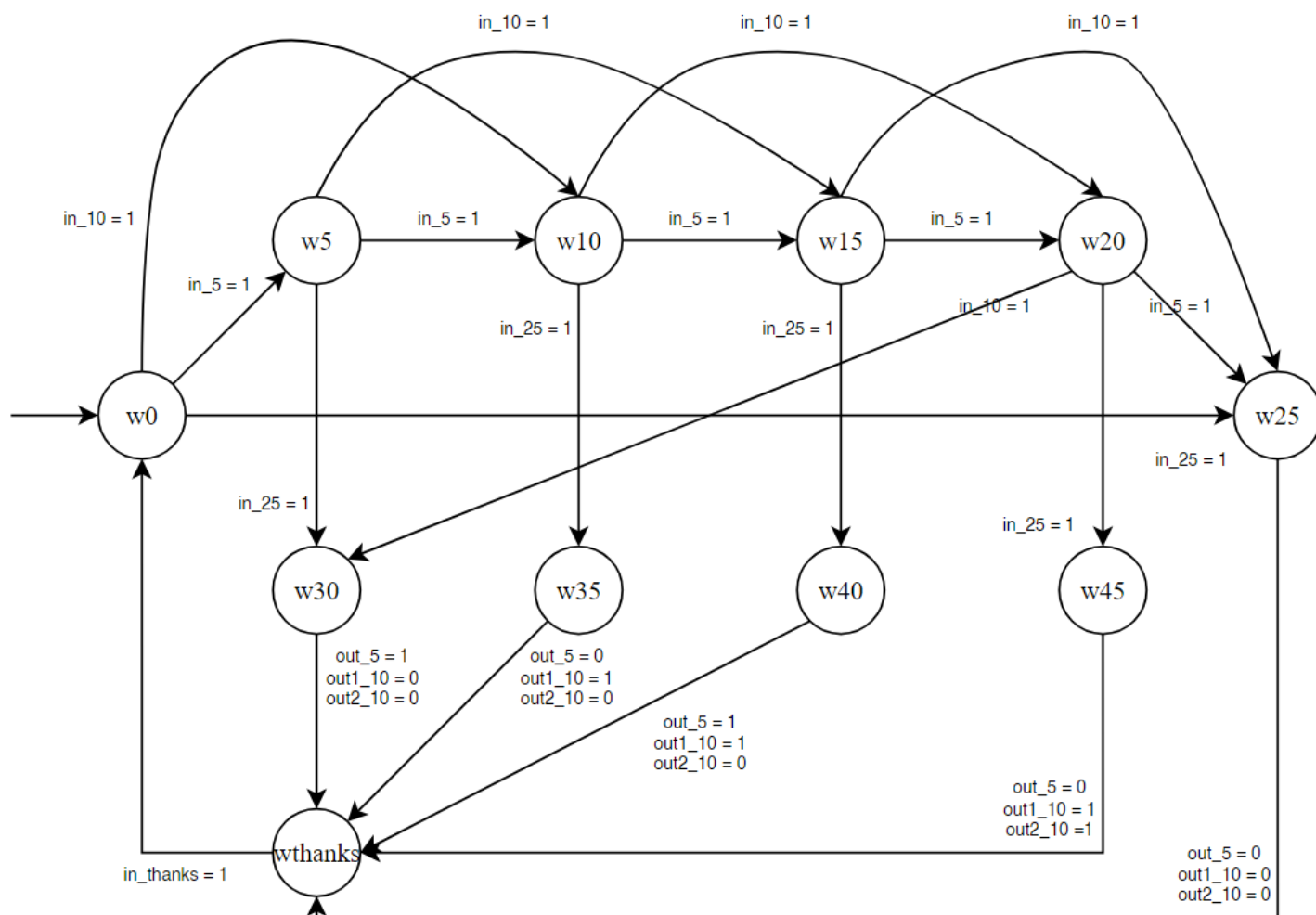


Tema de curs 2 – Alexandru Licuriceanu 332CD

1. Diagrama de stări:

Pentru vizibilitate, am omis pe unele tranziții, valorile de intrare și de ieșire care sunt setate pe 0.



2. Rezultatele simulării:

Test 1:

```
in_5 = 0 in_10 = 1 in_25 = 0 in_thanks = 0  
out_drink = 0 out_5 = 0 out1_10 = 0 out2_10 = 0
```

```
in_5 = 0 in_10 = 1 in_25 = 0 in_thanks = 0  
out_drink = 0 out_5 = 0 out1_10 = 0 out2_10 = 0
```

```
in_5 = 0 in_10 = 0 in_25 = 1 in_thanks = 0  
out_drink = 0 out_5 = 0 out1_10 = 0 out2_10 = 0
```

```
in_5 = 0 in_10 = 0 in_25 = 0 in_thanks = 0  
out_drink = 1 out_5 = 0 out1_10 = 1 out2_10 = 1
```

```
in_5 = 0 in_10 = 0 in_25 = 0 in_thanks = 1  
out_drink = 0 out_5 = 0 out1_10 = 0 out2_10 = 0
```

Test 2:

```
in_5 = 0 in_10 = 1 in_25 = 0 in_thanks = 0  
out_drink = 0 out_5 = 0 out1_10 = 0 out2_10 = 0
```

```
in_5 = 1 in_10 = 0 in_25 = 0 in_thanks = 0  
out_drink = 0 out_5 = 0 out1_10 = 0 out2_10 = 0
```

```
in_5 = 0 in_10 = 1 in_25 = 0 in_thanks = 0  
out_drink = 0 out_5 = 0 out1_10 = 0 out2_10 = 0
```

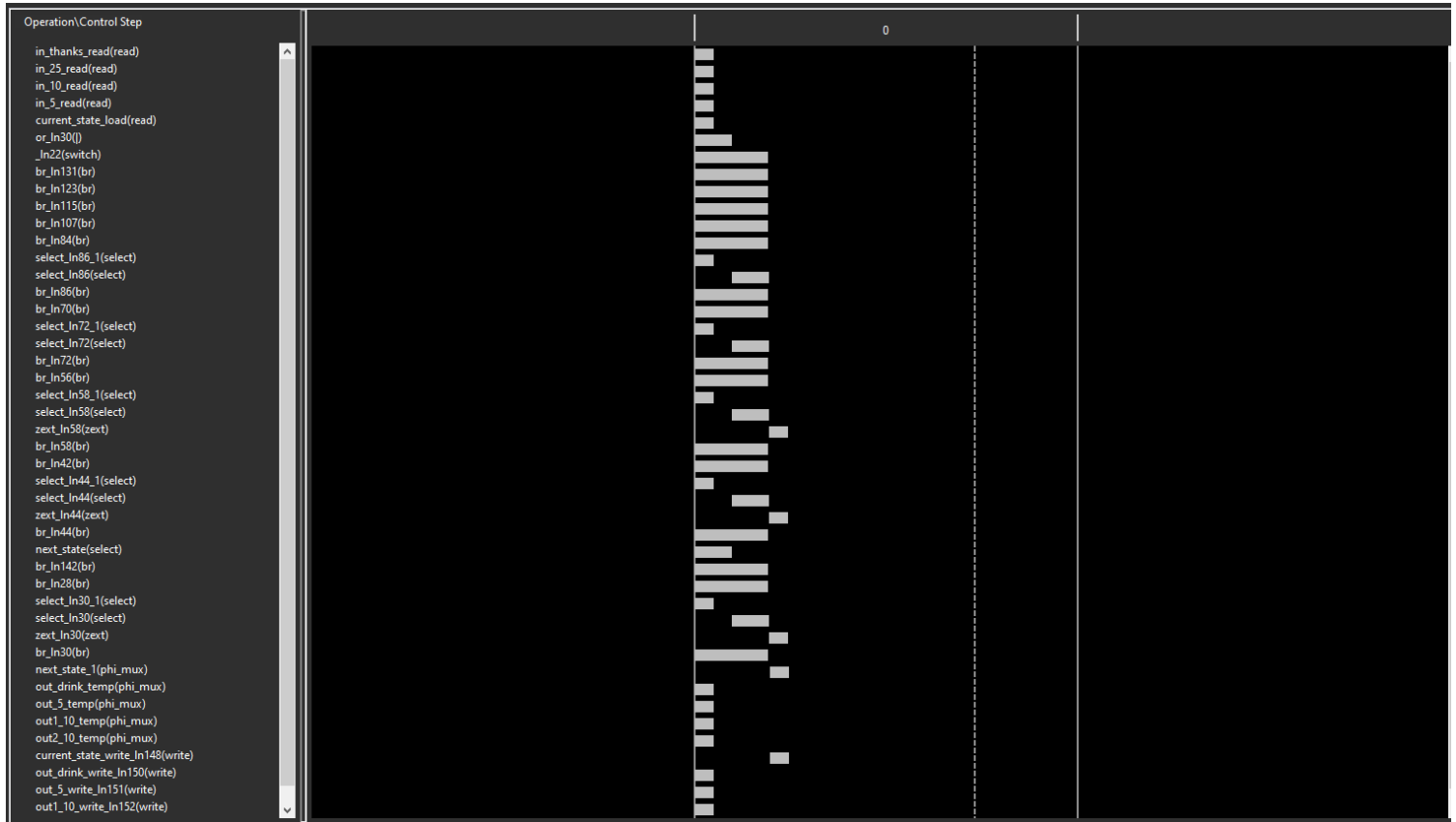
```
in_5 = 0 in_10 = 0 in_25 = 0 in_thanks = 0  
out_drink = 1 out_5 = 0 out1_10 = 0 out2_10 = 0
```

```
in_5 = 0 in_10 = 0 in_25 = 0 in_thanks = 1  
out_drink = 0 out_5 = 0 out1_10 = 0 out2_10 = 0
```

În primul test, am inserat 10, 10, 25, iar aparatul a dat rest 20.

În al doilea test, am inserat 10, 5, 10, iar aparatul a dat rest 0.

3. Raportul care demonstrează că circuitul este secvențial:



4. Raportul care arată resursele hardware în cazul utilizării unui FPGA Artix 7:

Synthesis Summary Report of 'vending_machine'

General Information

Date: Tue Jan 16 17:02:44 2024

Version: 2022.1 (Build 3526262 on Mon Apr 18 15:48:16 MDT 2022)

Project: vending

Solution: solution1 (Vivado IP Flow Target)

Product family: artix7

Target device: xc7a100t-csg324-1

Timing Estimate

Target	Estimated	Uncertainty	
10.00 ns	3.902 ns	2.70 ns	

Performance & Resource Estimates ⓘ

☒ Modules

☒ Loops

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM	
<div><div></div>vending_machine</div>				-	0	0.0		-	1	-	no	0	0	5	147	0