

Modular I/O Reasoning in DimSum

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- Formally verified compiler
 - Proof covers all optimizations
 - Correct w.r.t. the modeled semantics
- Discrepancies between hardware and model
 - Cannot implement correct calling conventions
 - Cannot support TriCore architecture
- Suboptimal code generation
 - Inserted moves
 - Higher register pressure

$$\llbracket \text{echo}_{\text{rec}} \oplus \text{getc}_{\text{spec}} \rrbracket \sqsubseteq \llbracket \text{echo}_{\text{spec}} \rrbracket$$

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  TAssume (f = "echo");;
  TAssume (vs = []);;
  v ← TGet;
  TPut (v + 1);;
  TCallRet "putc" [v] h;
  TVis (Out, Return 0 h);;
  TUb.
```

1

(Return v h)



```
int echo () :=
  let c := getc();
  putc(c);
  return 0;
```



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getc_spec :=
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TGT Call “echo” es @ $\Pi \{\{\Phi\}\}$

```
TGT Call "echo" es @  $\Pi$ 
  PRE  $|-*: es \text{ POST}_e, \lceil es = [] \rceil *$ 
    TGT Call "getc" es @  $\Pi$ 
      PRE  $|-*: es \text{ POST}, \lceil es = [] \rceil *$ 
      POST  $|*: ret,$ 
        TGT Call "putc" es @  $\Pi$ 
          PRE  $|-*: es \text{ POST}, \lceil es = [v] \rceil *$ 
          POST  $|*: \_,$ 
        POST_e  $|*: ret, \lceil ret = 0 \rceil.$ 
```

TGT Call "getc" es @ Π

PRE $|-*: es$ POST, $\exists v, P\ v * \lceil es = [] \rceil *$

POST $|*: ret, \lceil ret = v \rceil * P\ (v + 1).$

TGT Call "echo" es @ Π

PRE $|-*: es$ POST_e, $\lceil es = [] \rceil *$

TGT Call "getc" es @ Π

PRE $|-*: es$ POST, $\lceil es = [] \rceil *$

POST $|*: ret,$

TGT Call "putc" es @ Π

PRE $|-*: es$ POST, $\lceil es = [v] \rceil *$

POST $|*: _,$

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PRE $|-*: es \text{ POST}, \exists v, P \ v * \lceil es = [] \rceil *$
POST $|*: ret, \lceil ret = v \rceil * P \ (v + 1).$

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TGT Call "putc" es @ Π

PRE $|-*: es \text{ POST}, P \ (v + 1) * \lceil es = [v] \rceil *$

POST $|*: _, P \ (v + 1) \ (*)$

POST_e $|*: ret, \lceil ret = 0 \rceil * P \ (v + 1).$

$$\llbracket \text{echo}_{\text{rec}} \oplus \text{getc}_{\text{spec}} \rrbracket \preceq \llbracket \text{echo}_{\text{spec}} \rrbracket$$

```

Lemma sim_getc_spec `(!specGS)  $\Pi$   $\Phi$  :
  switch  $\Pi$ 
  PRE |-*:  $\kappa$   $\sigma_1$  POST,
     $\exists$  f es h,  $\ulcorner \kappa = \text{Some} (\text{Incoming}, \text{ERCall } f \text{ es } h) \urcorner *
  POST Tgt \_ \_ |* : \sigma' \Pi'$ ,
     $\exists$  v,  $\ulcorner f = \text{"getc"} \urcorner * \ulcorner \text{es} = [] \urcorner * \text{spec\_state } v * \ulcorner \sigma' = \sigma_1 \urcorner (*)$ 
  switch  $\Pi'$ 
  PRE |-*:  $\kappa$   $\sigma$  POST,
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  POST Tgt _ _ |*:  $\sigma' \Pi'$ ,
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$$\llbracket \text{echo}_{\text{rec}} \oplus \text{getc}_{\text{spec}} \rrbracket \preceq \llbracket \text{echo}_{\text{spec}} \rrbracket$$

```

Lemma sim_getc fns  $\Pi_l \Pi_r$  PL  $\sigma_i$  :
  "getc"  $\hookrightarrow$  None -*
  PL  $\sigma_i$  -*
   $\lceil \sigma_i.1 \equiv \text{getc\_spec} \rceil$  -*
   $\lceil \sigma_i.2 = 0 \rceil$  -*
   $\square$  switch_linked_fixed Tgt  $\Pi_l \Pi_r$ 
    PRE  $|-*:$   $\sigma_l$  POST,  $\exists h v \sigma_g, \text{PL } \sigma_g *$ 
    POST (ERCall "getc"  $\square$  h)  $\sigma_g |-*:$   $\sigma_r \Pi_r'$ ,
  switch_link Tgt  $\Pi_r'$ 
    Pre  $|-*:$   $\sigma_r'$  POST,  $\exists h'$ 
    POST (ERReturn (ValNum v) h')  $_ \sigma_l |-*:$   $_ \Pi_l'$ ,
     $\lceil \Pi_l' = \Pi_l \rceil * \text{PL } \sigma_r' ==*$ 
   $\exists P, P \ 0 *$   $\square$  rec_fn_spec_hoare Tgt  $\Pi_l$  "getc" (getc_fn_spec P).
  
```

```

Lemma sim_getc fns  $\Pi_l \Pi_r$  PL  $\sigma_i$  :
  "getc"  $\hookrightarrow$  None -*
  PL  $\sigma_i$  -*
   $\lceil \sigma_i.1 \equiv \text{getc\_spec} \rceil$  -*
   $\lceil \sigma_i.2 = 0 \rceil$  -*
   $\square$  switch  $\Pi_l$ 
    PRE  $| -: \kappa \ \sigma_0 \text{ POST}, \exists h \ v \ \sigma_g, \text{PL } \sigma_g *$ 
    POST Tgt _ _  $| -: \sigma_{i0} \ \Pi_i, \lceil \sigma_{i0} = \sigma_g \rceil * \lceil \Pi_i = \Pi_r \rceil *$ 
    switch  $\Pi_i$ 
      PRE  $| -: \kappa' \ \sigma \text{ POST}_0, \exists e' : \text{rec\_ev}, \lceil \kappa' = \text{Some (Incoming, } e') \rceil *$ 
      POST0 Tgt _ _  $| -: \sigma_r \ \Pi_r, \lceil \sigma_r = \sigma \rceil * \lceil e' = \text{ERCall "getc" [] } h \rceil *$ 
      switch  $\Pi_r$ 
        PRE  $| -: \kappa_0 \ \sigma_1 \text{ POST}_1, \exists h', \lceil \kappa_0 = \text{Some (Outgoing, ERReturn } v \ h') \rceil *$ 
        POST1 Tgt _ _  $| -: \sigma_{i1} \ \Pi_{i0}, \lceil \sigma_{i1} = \sigma_0 \rceil *$ 
        switch  $\Pi_{i0}$ 
          PRE  $| -: \kappa'_0 \ \sigma_2 \text{ POST}_2, \exists e'_0, \lceil \kappa'_0 = \text{Some (Incoming, } e'_0) \rceil *$ 
          POST2 Tgt _ _  $| -: \sigma_{r0} \ \Pi_{r0},$ 
             $\lceil \sigma_{r0} = \sigma_2 \rceil * \lceil e'_0 = \text{ERReturn } v \ h' \rceil * \lceil \Pi_{r0} = \Pi_l \rceil * \text{PL } \sigma_1 == *$ 
         $\exists P, P \ 0 * \square \text{ rec\_fn\_spec\_hoare Tgt } \Pi_l \text{ "getc" (getc\_fn\_spec } P).$ 

```

- Lemma for TCallRet
- Keep Π s the same - new lemmas for linking
- Balance between Abstraction and Information
- Balance between Hacking and Thinking