Modular I/O Reasoning in DimSum

Alex Loitzl¹

¹Institute of Science and Technology Austria (ISTA)

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Modular I/O Reasoning



Multi-language Reasoning in DimSum



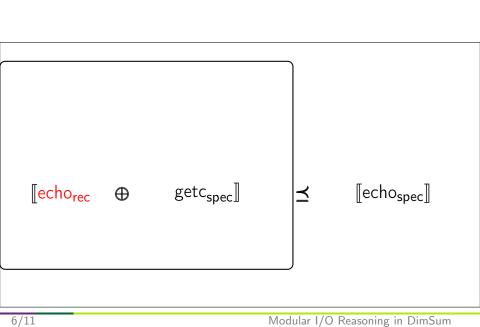
Rotation Project



Summary



- Formally verified compiler
 - Proof covers all optimizations
 - Correct w.r.t. the modeled semantics
- Discrepancies between hardware and model
 - Cannot implement correct calling conventions
 - Cannot support TriCore architecture
- Suboptimal code generation
 - Inserted moves
 - Higher register pressure



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                                                       echo_getc_spec :=
                      getc_spec :=
                                                         TExists '(f, vs, h);
                        Spec.forever(
                                                         Tvis (In, Call f vs h);;
                        TExists '(f, vs, h);
int echo () :=
                                                         TAssume (f = "echo");;
                        TVis (In, Call f vs h);;
 let c := getc();
                                                         TAssume (vs = []);;
                        TAssume (f = "getc");;
  putc(c);
                                                         v ← TGet:
                        TAssume (vs = \Pi)::
 return 0;
                                                         TPut (v + 1);;
                        v ← TGet:
                                                         TCallRet "putc" [v] h;
                        TPut (v + 1)::
                                                         TVis (Out, Return 0 h);;
                        TVis (Out, Return v h)).
                                                         TUb.
```

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                                                          TUb.
```

RTL to LTL



RTL Transition

$$c(pc) = \lfloor \operatorname{op}_{RTL}(op, \vec{x}, y, pc') \rfloor \quad \text{eval_op}(_, _, op, M(\vec{x})) = \lfloor v \rfloor$$
$$- \vdash S(_, _, _, pc, M, _) \xrightarrow{\varepsilon} S(_, _, _, pc', M[y \leftarrow v], _)$$

LTL Transition

$$\begin{array}{c} \operatorname{eval_op}(_,_,\operatorname{op},L(\vec{p})) = \lfloor v \rfloor \\ \\ _\vdash B(_,_,_,\operatorname{op}_{LTL}(op,\vec{p},q) :: bb, L,_) \xrightarrow{\varepsilon} B(_,_,_,bb,L[q \leftarrow v],_) \end{array}$$

Results - Compile Time (Arm hard float)



Results - Code Size



	vpr	mesa	fuzz1	fuzz2	fuzz3
arm_hard	-0.83%	-1.77%	-4.78%	-4.7%	-4.7%
arm_soft	-0.2%	-0.71%	-0.2%	+0.19%	+0.27%

Contributions



- Improved model of the Arm assembly semantics
- Proved all architectures correct w.o. changing their semantics
- New and more general register allocator
- Enable future support for TriCore architecture
- Small positive impact on code generation

Questions?



- Background
- 2 Project
- 3 RTL to LTL
- 4 Evaluation

Results - Allocator Statistics



	Remaining		Inserted		Reloads		Spills	
	C	C^p	C	Cp	C	Cp	С	Cp
vpr	4557	4557	165	0	275	275	298	297
mesa	13414	13420	939	0	1401	1276	2265	2133
fuzz1	119	118	40	0	17	17	17	15
fuzz2	404	404	148	0	115	115	74	65
fuzz3	1515	1515	533	0	456	461	267	226