Power Reduction Techniques for Low-Voltage Delta-Sigma Modulators

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***Abstract*—Using a Matlab-based behavioral modeling, Two $\Delta\Sigma$ modulators that employ the classic feedback architecture are implemented, one 2nd order modulator and one 3rd order modulator, using a CMOS TSMC 180nm technology node. This paper presents the summary of the entire design flow for a $\Delta\Sigma$ modulator applying power reduction techniques, implementing inverter-based switched-capacitor integrators and reducing the supply voltage as low as $0.9V$ ($< |V_{THP}| + V_{THN}$). These modulators report a $SNDR$ peak of $76dB@922mV$ Diff and $90dB@718mV$ Diff for the 2nd and 3rd order respectively, with a input dynamic Range of $53dB$ and $71dB$.**

***Index Terms*—$\Delta\Sigma$ Modulation, inverter as an amplifier, power reduction, scaled CMOS technology, switched-capacitor circuit.**

I. Introduction

In recent years, the increasing demand for interconnected systems within the ecosystem of smart cities has led to a proliferation of Internet of Things (IoT) devices. These devices gather data from the environment through sensors and process this information to provide valuable insights for decision-making. However, a critical challenge in the design of these devices is the limited availability of energy, as many of these systems are battery or solar-powered. In this context, energy-efficient solutions are essential to ensure the longevity and sustainability of these systems.

One of the fundamental components of IoT devices is the analog-to-digital converter (ADC). In essence, ADCs are the gateway between the physical and digital worlds for signal processing. From the environment, analog signals are measured through sensors, collecting information for future decision-making. However, this information needs conversion to a digital format to be processed by the core. This data conversion process is crucial for many applications, including telecommunications, instrumentation, and more. As a result, high-performance ADCs are an area of intense research and innovation.

There are many ways to implement data conversion, i.e., different types of ADCs that differ in the operations or processes executed to convert analog information (e.g., a voltage measurement of 0.87 V) to digital data (e.g., the value 010011 for 6 bits resolution). These operations can be complex and different, but the types of ADCs are classified into two groups; Nyquist converters and oversampling converters. As is well known, the Nyquist theorem states that for a signal with a specific bandwidth, it is necessary to sample it at least twice its highest frequency component (f_B) to capture all the information. Nyquist ADCs follow this principle, sampling the input signal at a rate equal to or higher than twice its bandwidth ($f_S >= 2f_B$). Oversampling ADCs, on the other hand, sample the input signal at a much higher rate than its bandwidth, which allows for a more straightforward implementation and a higher resolution.

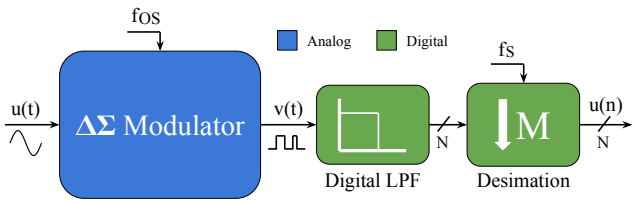


Fig. 1. Delta-Sigma ADC general structure

Among oversampling ADCs, one of the most widely used architectures is the Delta-Sigma ADC. Delta-Sigma is a popular choice for its ability to achieve high resolution and robustness against circuit imperfections with minimal power consumption [1], desired characteristics in applications such as biomedical, IoT, and HQ audio. However, they also present challenges such as stability issues, clock jitter sensitivity, and large silicon area. These converters are described in Fig 1, containing the Delta-Sigma Modulator and the Digital Filtering. The first modulates the mean value of a square signal v(t) with the value sampled at the input u(t), while the digital Low Pass Filter (LPF) processes this squared signal as a stream of bits to obtain a fully digital N-bit signal. However, the stream also contains a large amount of noise that is *shaped* by the modulator. Therefore, a decimation filter is required to reduce the sampling rate and remove the noise from the output.

This paper presents a detailed design of a Low-Voltage Low-Power Delta-Sigma Modulator, highlighting its key features, performance metrics, and practical considerations for implementation. This modulator is designed for audio applications, reducing as much possible power consumption. Table I shows the specifications this design must achieve. However, in figure 2, some of the most classic examples of low-voltage analog design are shown, where a) shows that if the supply is reduced below $|V_{THP}| + V_{THN}$ the implementation of switches as

CMOS passing-gates does not work, since the voltage of node V_{FS} may not be sufficient to turn on either of the two transistors. In addition, b) shows that a differential pair input stage requires at least $V_{TH} + V_{OV}$ at the input to operate, a limit that reduces the range of input excursion.

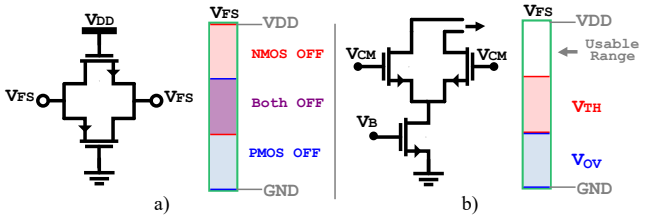


Fig. 2. Classic low voltage design challenges. a) CMOS Complementary switch. b) differential pair input stage

TABLE I
MODULATOR'S SPECIFICATIONS TO ACHIEVE.

Specification	Value
Technology Node	CMOS 180nm
Supply Voltage (V)	<=1
Bandwidth (Hz)	20k
SNDR (dB)	>65
Differential Vin Swing (V)	$500m$
Power Consumption	In order of hundreds of uW

The modulator is designed by implementing a system abstraction methodology, starting with the analysis in section II, which presents the system's general architecture, its fundamental operation, and a system model to predict its behavior in the face of its non-linearity. One of the techniques used to reduce power consumption is the reduction of the supply voltage (V_{DD}). However, in analog design, this involves many challenges when it comes to guaranteeing the performance of a system in the transistor implementation [2]. Therefore, sections III and IV describe the design and considerations of the integrators and the differential comparator. In addition, section V presents the non-idealities of transistors in the switching application, which affect the speed and accuracy of the modulator. At this point, some additional circuits to guarantee the correct performance of the modulator are mentioned. In section VI, these circuits are presented. Then, section VII shows the simulation results of the modulator design. This work leaves opened the door for possible improvements to obtain better performance of a Low-Voltage Low-Power Delta-Sigma modulator. In section VIII, these improvements are discussed. Finally, section IX summarizes all the work developed in this paper.

II. Delta-Sigma Modulation

In the previous section, the modulator is mentioned as a black box, a system that converts the amplitude of the input signal u(t) into the average value of a square signal v(t). This section presents how this modulation is implemented and what trade-offs are associated with it. First, it is necessary to show one of the most straightforward systems of this modulation in Figure 3 a). This system comprises four blocks: an adder, an integrator, a quantizer (for this simple case, a 1-bit quantizer), and a delay of 1 sample. Note that this diagram denotes the output signal of the modulator as v(n), while in Figure 1 v(t). This notation is taken based on the time discretization of the system as a function of the sampling frequency f_{OS}.

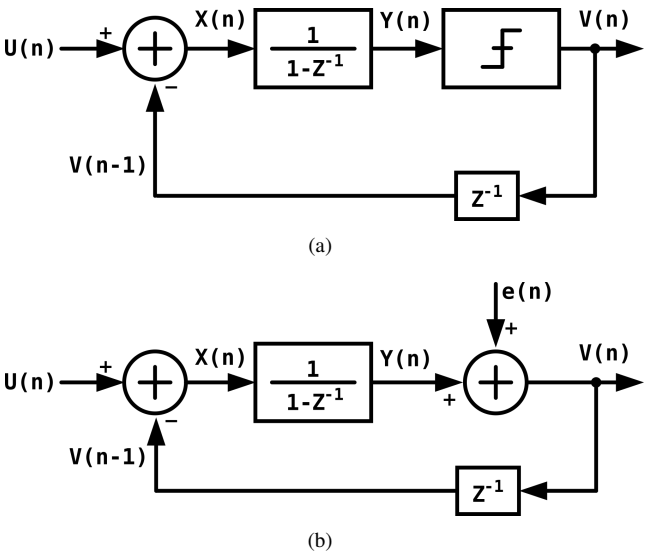


Fig. 3. First Order $\Delta\Sigma$ Modulator block diagram. (a) Using the 1-bit quantizer symbol. (b) Using a linear model for the quantizer.

To understand how the system operates, it is necessary to calculate the transfer function from the input $u(n)$ to the output $v(n)$. However, a linear model of the quantizer is required for this [1]. This explains why this is not an easy task, and, as a standard, this block is modeled as a sum of the quantizer input and a noise signal $e(n)$. This signal is known as quantization noise, as shown in Figure 3b). Note now that the output signal $v(n)$ is now a function of the input signal $u(n)$ and the quantization noise signal $e(n)$. When calculating $v(n)$ in the complex frequency domain z, it is obtained that,

$$V(z) = U(z) + (1 - z^{-1}) \cdot E(z) \tag{1}$$

This equation can be written as,

$$V(z) = STF(z) \cdot U(z) + NTF(z) \cdot E(z) \tag{2}$$

Where, the *Signal Transfer Function* (STF) and the *Noise Transfer Function* (NTF) correspond to,

$$STF(z) = 1$$
$$NTF(z) = (1 - z^{-1})$$

From Eq. 1, the input signal will be seen directly at the output, while the quantization noise signal passes through a filter given by $NTF(z)$. This filter becomes very interesting when replacing $z = e^{jw}$. Figure 4 shows the graph of the squared magnitude of $NTF(z)$ as a function of ω, normalized to an arbitrary sampling frequency f_S. Note that low-frequency spectral components (around 0) are attenuated while

high-frequency components (close to 0.5) are amplified; the behavior of a *High-Pass Filter*.

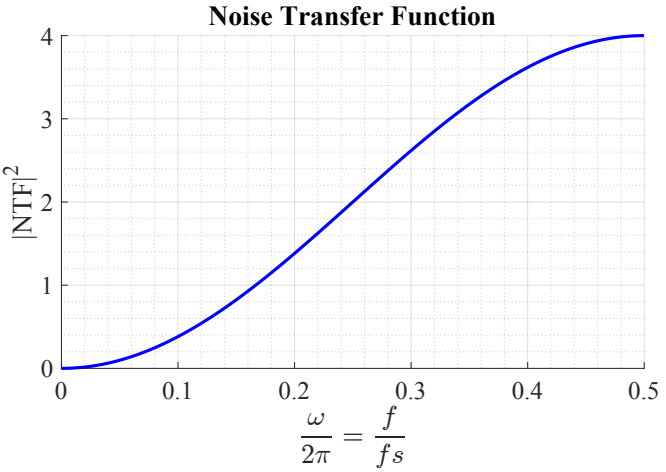


Fig. 4. $NTF(z)$ from Eq. 2

Another way to reason for this behavior is in terms of power. The filter translates the power distribution of the noise from low-frequency components to high-frequency components. Interestingly, this happens only with the quantization noise but not with the signal. This effect of filtering the noise is called *noise shaping*. Shaping the noise becomes extremely useful when the input bandwidth is close to 0 (i.e., in low-bandwidth applications). Using a sampling frequency far higher from the signal bandwidth reduces the power of the noise contained in this band. The amplified higher frequency noise is filtered by the digital systems of Figure 1. Therefore, it becomes necessary to define the *Over-Sampling Ratio* as

$$OSR = \frac{f_s}{2 \cdot f_B} = \frac{f_s}{f_N} \tag{3}$$

where f_S is the modulator sampling frequency (f_{OS} in Figure 1), f_B is the input maximum frequency component, and f_N is the Nyquist frequency. This way, the OSR represents "how many times is the modulator sampled, compared with the Nyquist frequency."

A. Higher Order Delta-Sigma Modulator

As mentioned earlier, noise shaping combined with oversampling has shown to be a technique that increases the *Signal to Quantization Noise Ratio* (SQNR) over specific bandwidths when discretizing an analog signal. Intuitively, it can be concluded that the higher the oversampling rate (OSR), the more significant the increase in SQNR. By integrating the power spectral density of quantization noise within the signal bandwidth (q_{rms}), this relationship can be expressed as,

$$q_{rms}^2 = \frac{\pi^2}{3} \frac{e_{rms}^2}{OSR^3} \tag{4}$$

Where "e_{rms}" represents the quantization noise rms value (signal dependent). As expected, the in-band noise decreases with increasing OSR. However, this decrease is relatively slight; doubling the OSR reduces the noise only by 9 dB, enhancing the ENOB by only about 1.5 bits. Of course, another way to increase the modulator SQNR is to increase the loop filter order. Figure 5 shows the second order $\Delta\Sigma$ modulator.

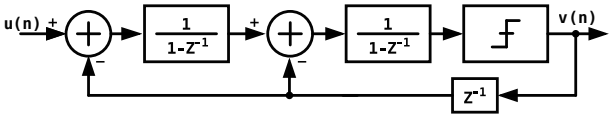


Fig. 5. Second Order Delta-Sigma Modulator

By solving the equations for this system, the signal ($STF(z)$) and noise ($NTF(z)$) transfer functions can be found given by

$$V(z) = STF(z) \cdot U(z) + NTF(z) \cdot E(z)$$

$$V(z) = U(z) + (1 - z^{-1})^2 \cdot E(z) \tag{5}$$

Note that in this case, $NTF(z)$ now corresponds to the transfer function of a second-order high-pass filter. It is intuitive to think that by adding one more stage of integration (For a 3rd order $\Delta\Sigma$ modulator), the output $V(z)$ is given by

$$V(z) = U(z) + (1 - z^{-1})^3 \cdot E(z) \tag{6}$$

In this way, it can be generalized that for an L-order modulator, the quantization noise transfer function is

$$NTF(z) = (1 - z^{-1})^L \tag{7}$$

And the quantization noise in the signal band of equation 4 results in

$$q_{rms}^2 = \frac{\pi^{2L} \cdot e_{rms}^2}{(2L+1) \cdot OSR^{2L+1}} \tag{8}$$

As the order of the filter increases, the trade-off of doubling the OSR becomes more favorable, increasing the ENOB by $L + 0.5$ bits.

Figure 6 graphically shows how quantization noise is reduced in a bandwidth close to 0 by increasing the order of the loop filter. As the filter slope increases, the noise of the interest band decreases.

B. $\Delta\Sigma$ Modeling

In the previous subsections, an analysis of the modulator at the system level has been carried out. On the other hand, in the following sections, the design of the blocks that make up the modulator is presented one by one. However, to ensure that the modulator works correctly, it is necessary to analyze how it behaves in the face of non-idealities of the circuits that make it up. These non-idealities added to the dependence of the input signal on quantization noise, resulting in a highly complex analysis to define circuit specifications theoretically. For this reason, a simulation is developed in MATLAB: SIMULINK,

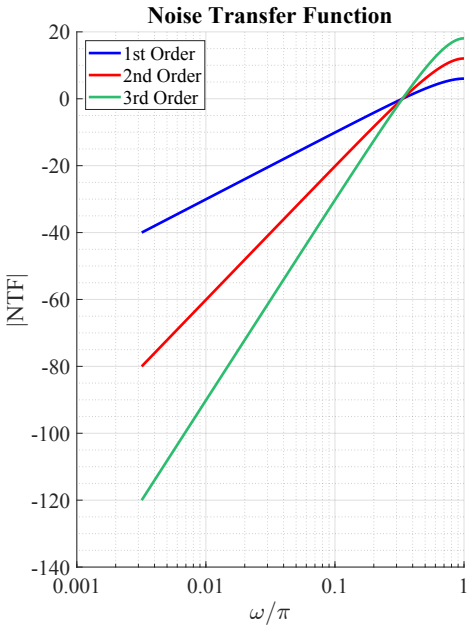


Fig. 6. $NTF(z)$ increasing the loop filter order.

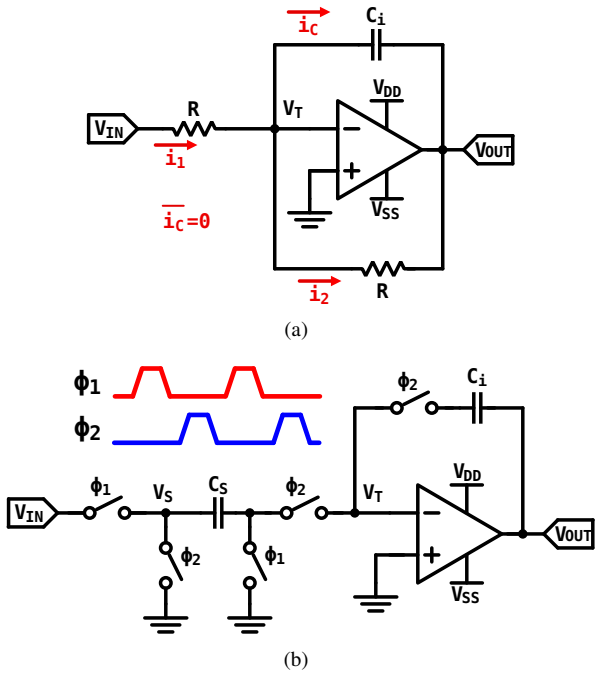


Fig. 7. Conventional integrator topologies. (a) RC integrator. (b) Switched Capacitors Integrator.

which evaluates the most relevant non-idealities of each element and establishes a table of minimum specifications for each, which guarantees that the modulator can satisfy table I.

The starting point for the design is the choice of loop filter order and oversampling ratio. For this purpose, simulations suggest that at a system level, specifications can be achieved with a 2nd order modulator with an OSR of 128. That is, to achieve the bandwidth of the specification, it is necessary for the system to operate at a sampling frequency (i.e., clock frequency) of

$$f_S(f_{CLK}) = OSR \cdot 2BW = 128 \cdot 40k = 5.12MHz$$

III. Loop Filter Implementation

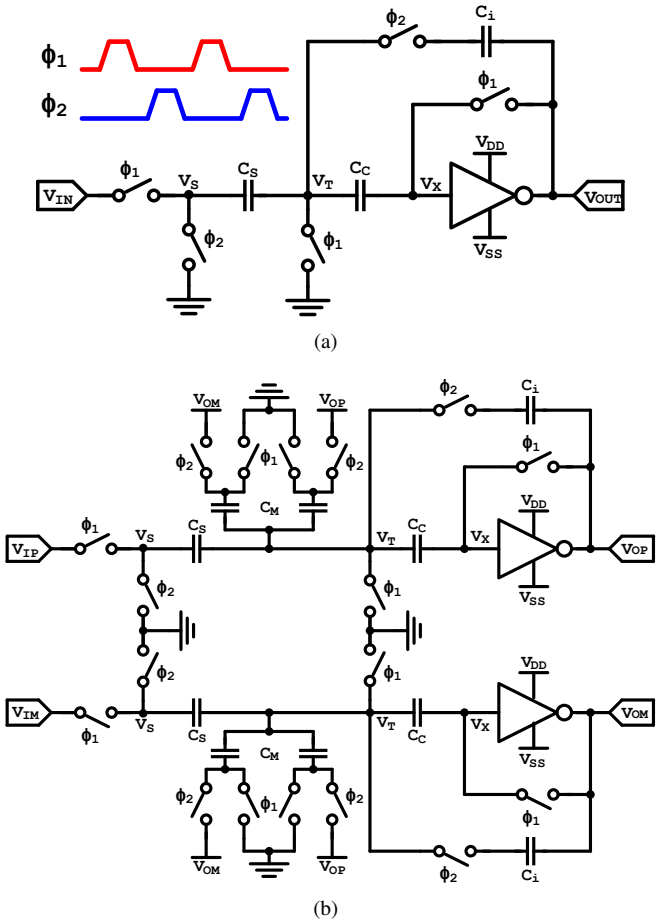
As mentioned in the previous section, the loop filter is the most relevant system in the design of the modulator because it depends on how "good" the noise shaping will be. That is, the quality of the slopes in Figure 6 depends on the accuracy of this system. Figure 7 shows the core of the two most commonly used topologies for implementing this loop filter. The circuit shown in a) is a continuous-time integrator (RC), while that in b) is a discrete-time integrator (switched capacitors).

Continuous-time modulators are highly linear and capable of achieving good resolutions with wide bandwidths at the cost of power consumption in the order of mW, or higher [3] [4]. Continuous-time integrators also have an inherent low-pass filter that functions as an anti-aliasing filter. However, as integrated technology reduces its dimensions, CMOS devices are smaller but not resistors. The area used by resistors against transistors increases. Extra layers to increase the materials' resistivity also increases the chip cost. [5] presents an alternative to this filter, with Gm-C integration topology, eliminating the need for resistors at the cost of limited output excursion ranges, limiting input excursion range. This last factor is critical when reducing the supply voltage.

On the other hand, discrete-time modulators implement switched capacitor integration filters, eliminating the need for resistors and reducing their power consumption [6] [7]. However, these filters require two non-overlapping clock phases to develop integration, so the opamp's ability to respond in just under half of the clock period limits the maximum frequency at which they can operate. In addition, since their operation is based on moving charges from one capacitor to another, the use of CMOS switches can contribute additional charges that generate noise at the filter output.

One of the power reduction techniques implemented is reducing the supply voltage to the maximum that circuits can tolerate to function correctly. As evidenced in Figure 2b), the input stage of opamps is often one of the most compromised when doing this. Due to this need, [8] proposes an alternative integrator based on inverters as an amplifier in a switched capacitor circuit, taking advantage of the low consumption of the topology and reducing the supply voltage to values less than $|V_{THP}| + V_{THN}$. Figure 8 shows this SC integrator topology based on the inverter as an amplifier, in a) its single-ended implementation and in b) its pseudo-differential implementation with a group of capacitors (C_M) for common mode feedback ($CMFB$) [9]. The inverter can be designed to force node V_T to signal virtual ground by implementing the auto-zero offset cancellation technique, as do the opamps in Figure 7.

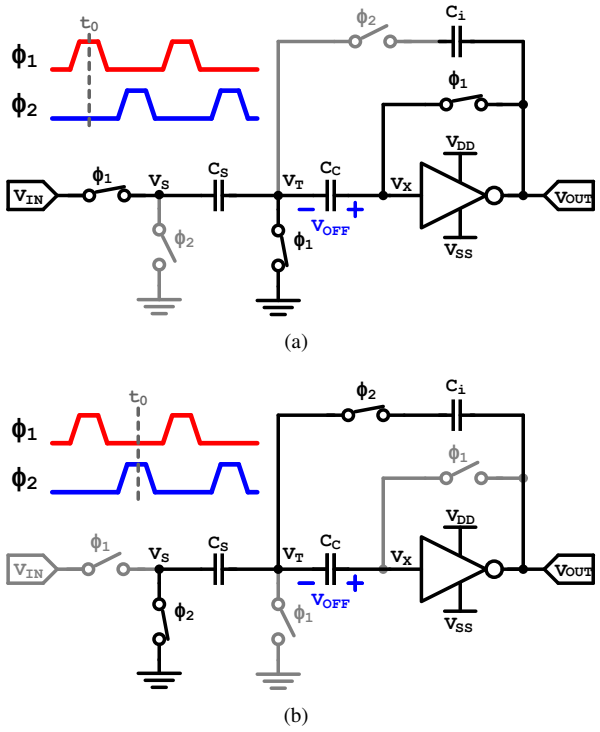
To explain this circuit's behavior, the integration process's



(a)

(b)

Fig. 8. Inverter-Based switched capacitors integrator. (a) Single-Ended. (b) pseudo-differential.



(a)

(b)

Fig. 9. Inverter-Based switched capacitors integrator stages. (a) Sampling Stage. (b) Integration Stage.

different stages can be seen in Figure 9. First, in 9a), assuming any time t_0, when $\phi 1$ is high, and $\phi 2$ is low, C_S stores a charge $Q_{CS} = V_{IN} \cdot C_S$ and C_i, as one of its terminals is floating, keep the charge stored in the previous clock cycle, let us call it $Q_{Ci}(n-1)$. Note that the inverter is connected in unity feedback. For this circuit, the inverter is designed in a nominal corner to set $V_X = V_{OUT} = 0$ (signal ground). However, due to variations in the manufacturing process, device sizing, supply voltage, and voltage threshold, V_X may have an offset from signal ground. Then, the voltage drop across the capacitor C_C is $V_X - V_{REF} = V_{OFF}$.

Then, in the next phase 9b), when $\phi 1$ is low and $\phi 2$ is high, node V_S is switched to signal ground, and due to the charge previously stored in C_S and C_C, nodes V_T and V_X will instantly change to $-V_{IN}$ and $-V_{IN}+V_{OFF}$, respectively, but due to the feedback through capacitor C_i and the opamp gain, these nodes tends to return to signal ground and V_{OFF}. From the previous phase, voltage across capacitor C_C was V_{OFF}, and because no current flows to the inverter input, the voltage across this remains constant during this second phase. As V_T recovers, the charges are distributed. At the end of the phase, as $V_{CS} = 0$, the charge initially stored in C_S moves to C_i. Thus, over the clock cycles, the charge stored in C_S due to the input is accumulated in C_i, developing a "charge integration." Given the behavior of the circuit, Figure 9a) is called *sampling stage* and Figure 9b) *integration stage*.

From the previous analysis, V_{OUT} is calculated using the principle of charge conservation,

$$Q_i = Q_f$$

Where Q_i corresponds to the total charge stored by the capacitors at the end of the sampling stage and Q_f the total charge of the capacitors at the end of the integration stage, so that,

$$\begin{aligned} V_{IN} \cdot C_S + V_{OFF} \cdot C_C + Q_{Ci}(n-1) = \\ V_{OFF} \cdot C_C + V_{OUT} \cdot C_i \end{aligned} \tag{9}$$

As $Q_{Ci}(n-1)$ represents the charge stored by C_i in the previous integration stage, it can be seen that.

$$Q_{Ci}(n-1) = V_{OUT}(n-1) \cdot C_i$$

By replacing this value in Eq. 9, the output at the end of the n-th clock cycle is obtained as

$$V_{OUT}(n) = V_{OUT}(n-1) + \frac{C_S}{C_i} \cdot V_{IN}(n) \tag{10}$$

This equation is the differential equation of a system $H(z)$ given by

$$H(z) = \frac{V_{OUT}(z)}{V_{IN}(z)} = \frac{p}{1 - z^{-1}} \tag{11}$$

Where,

$$p = \frac{C_S}{C_i}$$

A. The Inverter as Amplifier

The inverter is not a commonly used alternative as an amplifier because it presents various design challenges due to its non-linearities, such as limited gain, parasitic capacitances between input and output, excursion range, and more. However, [8] presents a comprehensive analysis of its implementation and demonstrates how cascode inverters drive the main challenges. Cascode inverters can offer the necessary gain and isolate input and output nodes. In addition, implementing a pseudo-differential architecture (as shown in Figure 8b)) improves the system PSRR.

TABLE II
INVERTER'S SPECIFICATIONS.

Specification	Expected	Achieved
Supply Voltage (V)	0.9	0.9
Common Mode (V)	450m	450m
Gain min (V/V)	-100	-100
Vout Swing (V)	>600m	606m
SR($V/\mu s$)	>19	21.3
CL (pF)	1.1	1.1
Power Consumption	units of uW	8.1 uW[1]

Figure 10 shows the the implemented cascode inverter schematic whit biasing. The design of this circuit starts with Table II, which presents the minimum specifications of the inverter. This design is limited to meeting these specifications in a typical corner. In slow mobility corners, CMOS transistors increase their V_{TH}, making their operation at V_{DD} of $0.9V$ very precarious. The critical point for the design of this circuit is the excursion range at the output of the inverter. The output range is defined by $2 \cdot Vdsatn$ downwards and $2 \cdot Vdsatp$ upwards to meet the specification. It is necessary to guarantee that M9 and M10 are saturated when $V_{OUT} = 150mV$ and M12 and M13 are saturated when $V_{OUT} = 750mV$. The transistors are biased in weak inversion to achieve a low $Vdsat$, leaving $Vds = 70mV < Vdsat$ for M9 and M13 and $Vds = 80mV$ for M12 and M10 when the output pushes them. With $V_{THN} \approx 550mV$ and $V_{THP} \approx 565mV$ in a typical case, $Vb1 = V_{THN} + Vdsat = 620mV$ is chosen, and $Vb1 = VDD - V_{THN} - Vdsat = 280mV$.

The $pmos2v\_mac$ and $nmos2v\_mac$ devices from TSMC CMOS 180nm PDK have been characterized. For both devices to drive the same current under the same voltages, with the same length, the $W_P \approx (\pi - 1) \cdot W_N$, this relation is needed to guarantee the $V_{CM} \approx \frac{V_{DD}}{2}$. To achieve the slew rate from the specification, the inverter must deliver a current of

$$I_{OUT} = SR \cdot CL = 21\mu A$$

However, this slew rate must be achieved when at the beginning of the integration stage (Figure 9 b) V_X instantly changes to $-V_{IN} + V_{OFF}$, which, depending on the signal, forces P or N transistors into strong inversion, increasing their SR, allowing to keep a low static current flowing through the branch to keep a high gain.

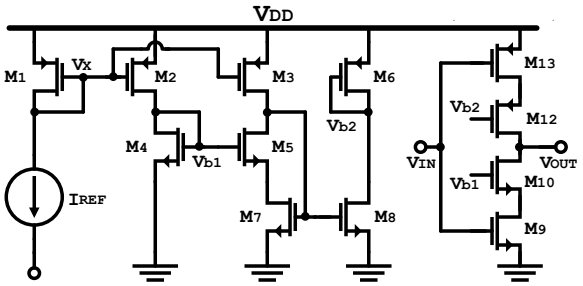


Fig. 10. Cascode inverter schematic, and its biasing circuit.

First Approximation of Design: For when $V_{OUT} = V_X = V_{CM}$, it is chosen that a current of $5\mu A$ passes through the inverter branch. To reach the desired speed, $Lmin = 180n$ is used in transistors M9 ($W/L = 5.2um/180nm$) and M13 ($W/L = 11.5um/180nm$), which control the current of the branch. On the other hand, for cascode devices $L = 2L_{min}$ is used: M10 ($W/L = 4.7um/360nm$) and M12 ($W/L = 10.2um/360nm$). These dimensions report an SR of $22.51V/\mu s$, and $VCM = 446.4mV$ with $I_D = 4.6uA$, but their output range with gain greater than 100 V/V is limited to $575mV$

Fine Tuning: From the first approximation, it is concluded that it is necessary to increase DC gain, and for this, it is necessary to increase transistor lengths. From here, a more precise modification converges in

$$(W/L)_9 = 7.3um/250nm$$

$$(W/L)_{13} = 16um/250nm$$

$$(W/L)_{10} = 6.5um/500nm$$

$$(W/L)_{12} = 14.2um/500nm$$

With these values, the specifications achieved are observed in table II. A decisive advantage of this inverter is its great slew without static current since the current flow that charges the output capacitor occurs at the beginning of the integration phase. Once charged, its consumption returns to static.

IV. Comparator design and Considerations

In this section, the design of the system's quantizer is developed. For practicality and reduction of complexity and system consumption, a 1-bit quantizer is chosen, a dynamic comparator. For this, it is necessary to clarify the minimum specifications that it must meet to guarantee its correct operation in the system. These specifications are presented in Table III.

Although the power consumption specification defined as "To Be Minimized" may be redundant, it is a crucial point when choosing the comparator architecture. For this work, a Strong-Arm comparator, presented in Figure 11, stands out

TABLE III
COMPARATOR'S SPECIFICATIONS.

Specification	Required Min	Required Typ	Required Max	Achieved Min	Achieved Typ	Achieved Max
Supply Voltage (V)	$900m$	$910m$	$920m$	$900m$	$910m$	$920m$
Input Common Mode (V)	$450m$	-	-	$400m$	-	-
Clock Frequency (MHz)	5.12	-	-	5.12	-	-
Propagation delay (ns)	-	-	9.8	4.4	5.4	8.8
Offset Voltage (V @ 3σ)		$< 5m$			$3.73m$	
Input Referred Noise (V)		$< 1m$			$240\mu V$	
Load Cap (fF)		≈ 12 (Buffer)				
Power Consumption (μW)		To Be Minized		0.823	0.977	1.225

for having characteristics such as zero static current (due to the shutdown of M3 or M4 and M5 or M6 once the value of V_X and V_Y is established). A dynamic current limitation is given by the tail transistor M7 [10]. Although this last current limitation can also limit the response speed, the modulator will be limited in speed due to the response of the inverter presented in the previous section. In this way, the comparator is not required at its maximum possible speed.

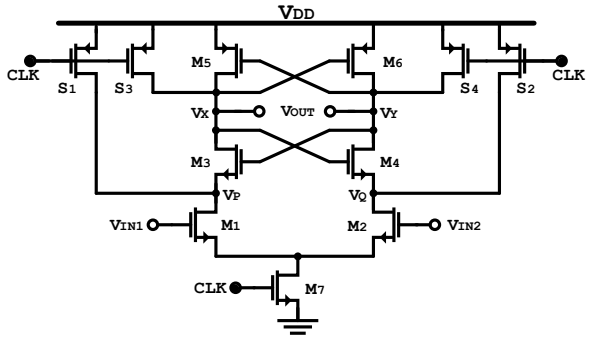


Fig. 11. Strong-Arm Comparator Core

A. Basic behavior

As described in [10], this comparator works by charging and discharging the nodes V_P, V_Q, V_X and V_Y. The CLK clock signal, starting at a low voltage (V_{SS}), turns off the tail transistor M7 and turns on switches S1-4. These switches charge all nodes to V_{DD}, turning off transistors M1-6, so while $CLK = V_{SS}$, no static current flows from V_{DD} to V_{SS}. At the moment that CLK switches to a high voltage (V_{DD}), the switches turn off, releasing all nodes at an initial voltage of V_{DD}, so M3-6 start in OFF state and $V_{DS} \approx 0$ for M7. At this point, the "race" to define the output begins. The nodes V_P and V_Q will be discharged through transistors M1 and M2, biased by voltages V_{IN1} and V_{IN2}, if $V_{IN1} > V_{IN2}$ then $ID_1 > ID_2$ and therefore node V_P discharges faster than node V_Q.

This discharge of V_P and V_Q continues until these nodes reach a value of $VDD - V_{TH3,4}$, transistors M3 and M4 turn on, and a small positive feedback begins. The nodes V_X and V_Y begin to discharge due to the current of M3 and M4. As one of the two nodes discharges faster, the other does so more slowly.

The circuit behaves this way until V_X or V_Y drop to $VDD - V_{TH5,6}$. In this last stage, the strong positive feedback of the cross-coupled transistors M4-6 forces these nodes to be defined. If $V_{IN1} > V_{IN2}$ then V_X will be forced to V_{SS} and V_Y to V_{DD}. If we define $V_{OUT} = V_Y - V_X$ then the behavior of the output is

$$V_{OUT} = V_{IN1} > V_{IN2} \tag{12}$$

Note that when $V_X = V_{DD}$ is established, M4 is turned on, but M6 is turned off, so M6 acts as an open switch, and in this way, there is no conduction of static current through the branch. At the same time, the opposite occurs in the other branch, as $V_Y = V_{SS}$, M5 is turned on, but M3 is turned off.

B. Device Sizing

A methodology based on [11] is developed for the circuit design. As mentioned earlier, since speed is not a specification of concern for this circuit, the channel lengths of the transistors are set as $L = 2L_{min} = 360nm$. First, the most critical point is the operation of M1 and M2 since, as mentioned in the introduction, a differential pair input stage has complications in operating in a circuit powered by a voltage as low as $0.9V$. This problem is solved by implementing low V_{TH} transistors ($\approx 320mV$) only in M1 and M2 (Figure 11) to ensure that they can turn on correctly with V_{CM} at the input of $0.45V$. In addition, these will be mainly responsible for the comparator's $OFFSET$, so they are dimensioned with $W_{1,2} = 20\mu m$. Second, the system speed will be limited by transistor M7, which operates in a deep triode. An initial value of $W_7 = 12\mu m$ is chosen to ensure acceptable speed in all corners. Third, the cross-coupled transistors do not require large dimensions; a 5th part of M1 and M2 is sufficient for a typical design [11], that is, $W_{3,4} = 4\mu m$. However, intending to make the rise and fall times of nodes V_X and V_Y symmetrical, $W_{5,6} = 5\mu m$ is established. Finally, the switches must be able to completely reset the circuit nodes to V_{DD} in less than half the clock phase. An initial value of $W_S = 2\mu m$ can guarantee this condition by far.

C. Output Stage

Finally, it is necessary to highlight from Figure 11 that when CLK returns to V_{SS}, the nodes are reset to V_{DD} through switches S1-4, erasing the comparator's response. Thus, an SR latch is implemented as an output stage for the output to be maintained, as shown in Figure 12. Digital inverters are used to speed up the response of the Strong-Arm and ultimately define the signals to the latch. To force a known latch state as the starting point of the conversion, a reset logic is implemented

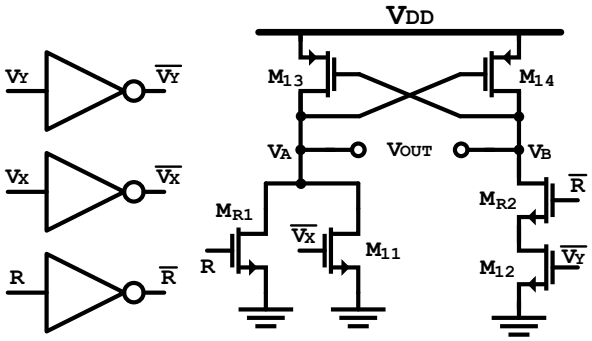


Fig. 12. Latch SR output stage, with Reset logic (R)

with transistors MR1 and MR2. When the reset signal is high, regardless of the state of $\overline{V_X}$, node, V_A is forced to V_{SS} due to MR1. This voltage causes M14 to try to force node V_B to V_{DD}. To avoid the struggle between M14 and M12, transistor MR2 separates M12 from node V_B. In this way, if we define $V_{OUT} = V_A - V_B$, the comparator output still satisfies Eq. 12 throughout the entire clock cycle.

For the sizing of the devices in this output stage, the fact that the comparator's load will be a buffer with an input capacitance of around $12fF$ is taken into account, so these devices do not need to conduct a high current to respond to the output. Therefore, a length of $500nm$ is chosen for all devices except for M12 and MR2. Unlike MR1, which turns on with the reset signal high and does not affect the regular operation of the latch, MR2 is on all the time in the latch's daily operation. For this reason, to keep the fall times of both nodes V_A and V_B symmetrical, it is necessary to establish $2 \cdot L_{R2,12} = L_{11}$. Through simulation, the values of W for transistors M11-14 that meet the propagation delay requirements of Table III are easily reached. Thus, it is finally defined that $W_{11,12} = 1.5\mu m$, $W_{R1,R2} = 1.5\mu m$ and $W_{13,14} = 2\mu m$.

V. Switching design and Considerations

This delta-sigma modulator implements switching capacitors circuits, using MOSFET transistors in their application as switches. In deep, MOSFET transistors are not ideal switches. For example, in the sample and hold circuit shown in Figure 13 a), either during charging or discharging of the capacitor, when $V_G = V_{DD}$ and V_{DS} approaches zero or, in other words, when $V_{DS} \ll 2(V_G - V_{TH})$ at the end of the charge or discharge cycle, the transistor can be modeled as a resistance:

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_G - V_{IN} - V_{TH})}$$

Then, the transistor propagates the input value to the output. However, the situation is more complex because parasitic capacitances are associated with the MOS device. These capacitances cause offset and distortion effects. In this section, the most representative non-idealities: channel charge injection and clock feedthrough, are presented. These effects limit the modulator performance due to errors introduced to the charge stored in the capacitors [12]. Whereas in Figure 13 b), when $V_G = V_{SS}$, the transistor can be seen as an open circuit, preventing the input signal from propagating to the output.

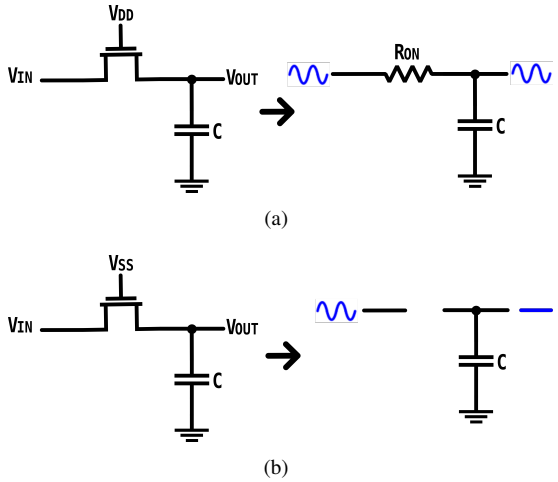


Fig. 13. Transistor as a switch. (a) Transistor as a resistor (ON) (b) Transistor as an open circuit (OFF).

Channel Charge Injection. As shown in Figure 14, applying a HIGH voltage to the gate of the MOS transistor to turn it on, a charge build-up occurs at the transistor channel. When off, the load is shifted to the drain and source terminals. In Figure 14, the input absorbs load moving to the left, which does not introduce any error into the signal. However, the charge flowing to the right is absorbed by capacitor C, causing a variation in the voltage sampled by this component.

No defined model specifies how much charge goes to V_{IN} or to the capacitor. Consider the worst case where the capacitor absorbs the entire channel charge and V_{th} is constant for any input, approximating the output as:

$$V_{out} = V_{in}\left(1 + \frac{WLC_{ox}}{C}\right) - \frac{WLC_{ox}}{c}(V_{CLK} - V_{TH})$$

It follows that the optimal output value is influenced by a non-unitary gain, in this case, equal to $1 + WLC_{ox}/C$, and a constant offset voltage of $-WLC_{ox}(V_{CLK} - VTH/C$. In addition, a dependence on the WL factor is present in both non-idealities. Considering the body effect, a non-linear relationship of V_{th} on V_{IN} is found [13].

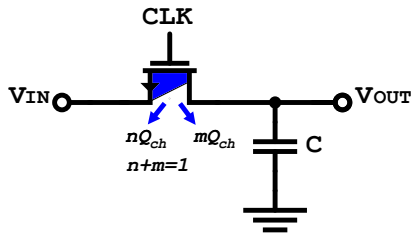


Fig. 14. Charge injection when a switch turns off

Clock Feedthrough, Refers to the coupling of clock transitions through the overlap capacitance between the gate and

the drain or source. As illustrated in Figure 15, when the gate voltage changes to turn the transistor on or off, the signal is coupled to the channel and affects the voltage level at the drain or source. Assuming the overlap capacitance is constant:

$$\Delta V_{OUT} = V_{CLK} \frac{WC_p}{WC_p + C}$$

This effect is independent of the input level and provides a constant offset between input and output. for a more detailed discussion of this phenomenon, see [14] and [13].

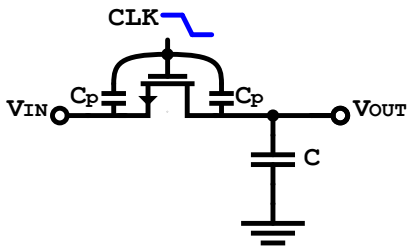


Fig. 15. Clock feedthrough in a sampling circuit.

A. Driving non-idealities

The effects previously mentioned introduce an error to the modulator signal path. This section also presents the commonly used techniques to drive these non-idealities.

Dummy Switch, The principle of this technique consists of using a second transistor, connected as shown in Figure 16. This transistor is responsible for removing the charge induced by M1. To do this, M2 must turn on when M1 turns off so that M2 absorbs the excess charges left in C by M1 [14], noted that this technique provides an effective cancellation of the clock feedthrough if M2 is twice that of M1 which means that the overlap capacitance of M1 on the capacitor side will be equal to the sum of the overlap capacitances of M2.

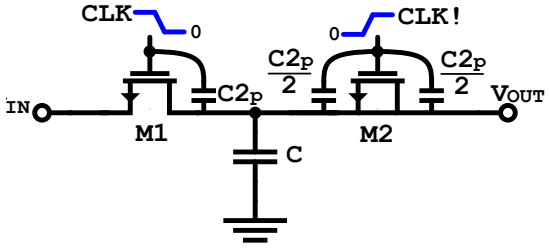


Fig. 16. Dummy device to reduce charge injection and clock feedthrough.

A limitation of this technique is that accurate cancellation is not guaranteed. Due to the uncertainty in the charge distribution in M1 between the drain and source, it is difficult to size M2 for effective charge injection cancellation. In addition, factors such as manufacturing process variations and other non-idealities can further affect cancellation accuracy. This technique also requires an additional clock for proper operation, which increases power consumption and the area occupied by the switching transistors.

Complementary Switch, This consists of implementing a PMOS and an NMOS in the configuration illustrated in Figure 17. Allows for a given value of Δ_{q1} of electrons, there to be an opposite charge Δ_{q2} that counteracts the effect of Δ_{q1}. However, this charge cancellation depends on the input value, which means that the transistors can only configure to nullify the effect of charge injection at a specific input level. In addition, this technique presents certain complications, such as the need for an additional clock signal and more transistors, which also increases power consumption and occupied area.

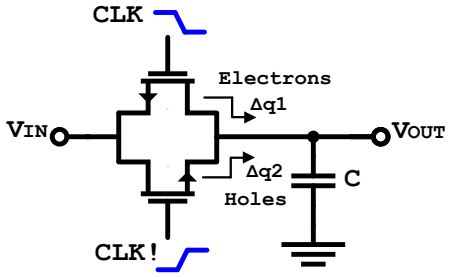


Fig. 17. Complementary switches to reduce charge injection.

Let's Make it Differential, The well-documented advantages of differential circuits suggest that their implementation will completely mitigate the problem of charge injection. Upon examining Figure 18, we can determine that $\Delta_{q1} = WLC_{ox}(V_{DD} - V_{in1} - V_{th1})$ and $\Delta_{q2} = WLC_{ox}(V_{DD} - V_{in2} - V_{th2})$. From this, it follows that $\Delta_{q1} = \Delta_{q2}$ only if $V_{in1} = V_{in2}$. That is, the differential signals do not eliminate all generated errors. However, it does manage to eliminate the part corresponding to the constant offset error introduced by the clock feedthrough and the charge injection [13].

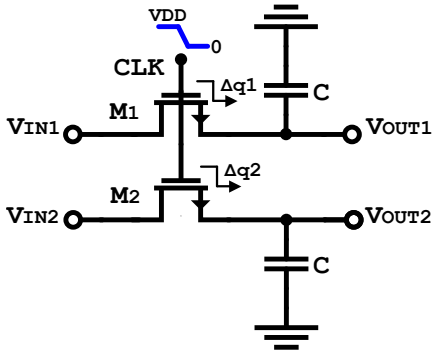


Fig. 18. Diferential sampling topology.

Selection Process: To select the switch implementation, we use a pseudo-differential integrator block like the one in Figure 8 to compare. The goal is to evaluate the error introduced by different switches. For this purpose, we use a differential input of $V_{in} = 450 + / - 50mV$ or 100mV total amplitude. Due to the low supply voltage, the switches implement a clock amplitude twice the global supply voltage (1.8V).

In Figure 19, the error of each of these architectures to the expected value in each integration cycle is evident. The

N Switch and the dummy transistor Switch have very similar performance, with the N Switch being slightly better.

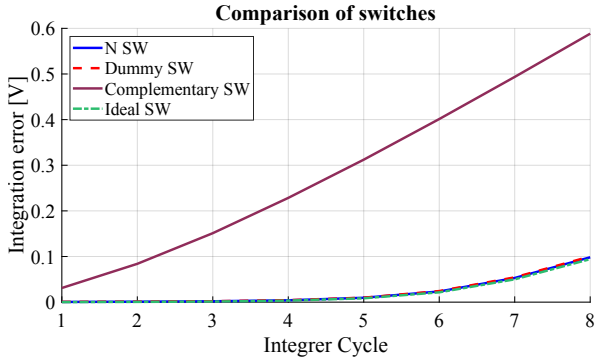


Fig. 19. Comparison between NMOS, Dummy, and Complementary switches for minimum technology dimensions.

Taking into account the above and referring back to Figure 13 a), we can make an approximation of $\tau = R_{ON}C$. To consider a valid value for R_{ON}, with an input ranging from 0 to 0.9V, a VG of 1.8V to ensure proper transistor activation and a transistor with L=180n and W=220n. The worst-case load capacitance within the circuit was analyzed to be at least 900fF, yielding the results presented in Figure 20.

From the worst and best case for the nominal corner, $V_{ONmin} = 2.36k\Omega$ and $V_{ONmax} = 8.78k\Omega$, thus $\tau_{min} = 2.12ns$ and $\tau_{max} = 7.902ns$. For an estimated operating frequency of $5.12MHz$ and 10% non-overlapping clock, we would have a maximum settling time of $87.89ns$. Therefore, under these conditions, an SW with minimum dimensions does not pose any speed-related issues for the circuit.

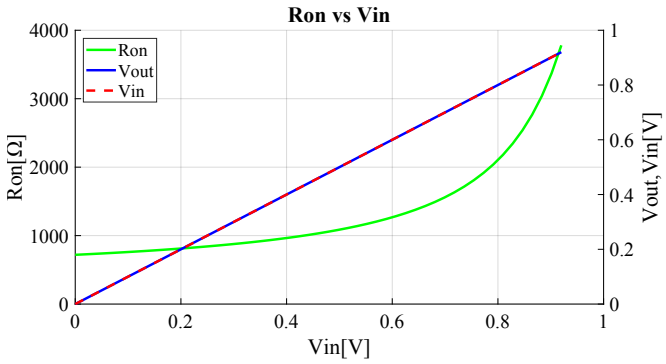


Fig. 20. Transfer curves NMOS2VMAC, VG=1.8V. R_{on} vs V_{IN}.

For our implementation, we have decided to use a single Switch with minimum dimensions in the TSMC180 technology node for nmos2vmac transistors. By doing this, we save area and power consumption without sacrificing performance.

VI. Other Required Elements

A. Non-Overlapping Clock Generator

Section III of the document shows that it is necessary to operate the implemented correctly switched capacitor integrator circuit (Figure 9) to have two clock phases $\phi 1$ and $\phi 2$ without overlap. I.e., phase $\phi 1$ must be fully established at V_{SS} before phase $\phi 2$ begins its transition from V_{SS} to V_{DD} and vice versa. This configuration ensures there is no moment when both switches of $\phi 1$ and those of $\phi 2$ are activated simultaneously, preventing the charge stored in the capacitors from flowing into unwanted paths.

However, a single clock signal with a frequency of $5.12MHz$ and a duty cycle of 50% is supplied to the modulator. A clock generation circuit shown in Figure 21 is implemented to generate the two phases. In this circuit, digital cells with a specific propagation delay (marked in the figure as "SLOW") are designed, and to precisely define the output and input, buffers with negligible delay (marked as "BUFFER") are implemented.

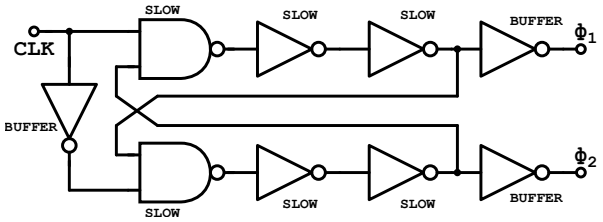


Fig. 21. Non-Overlaping Clock Generator.

This circuit operates by taking advantage of the propagation delay of digital cells to generate a dead time between the two clock phases. This value is determined by the sum of the delay of the NAND gate and two times the delay of the slow inverter.

Choosing the appropriate dead time for the design of the modulator is challenging. Selecting a prolonged time ensures that the switches do not overlap but reduces the duty cycle of the phases, resulting in a decrease in the response time available for the integrators. In addition, the comparator must respond within this time to continue with the next sampling stage of the integrators. Considering these factors, an appropriate dead time should be greater than 5% of the clock cycle and less than 10%, that is, between approximately 10 and 20 ns.

Simulations through corners of the implemented circuit report a minimum value of $12.1ns$, a typical value of $15.6ns$, and a maximum value of $18.0ns$. In addition, it reports an average consumption of $2.6\mu W$ in a typical corner, $2.4\mu W$ as a minimum, and $3.5\mu W$ as a maximum.

B. Clock Boosting

As Section 5 of the document mentions, implementing switches at low VDD presents various challenges. One of the main strategies to combat these challenges is creating "another voltage domain." That is, switches will be actuated by clock signals that reach twice the maximum voltage of the rest of the system. This ensures the correct connection between any two nodes in the system using only NMOS transistors as switches. This technique is known as *Clock Boosting*.

The circuit used to implement clock boosting is shown in Figure 22, where CLK corresponds to the clock signal

provided as input and $CLKD$ to the doubled clock signal provided as output, in phase with the original signal.

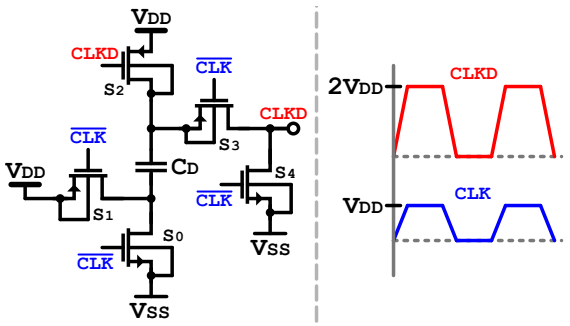


Fig. 22. Clock Boosting circuit.

To understand the operation of the circuit, initially consider that $CLK = V_{SS}$. Switches S_0, S_2 and S_4 are activated and S_4 forces $CLKD = V_{SS}$. Capacitor C_D is charged to V_{DD}, with its upper terminal as positive. When CLK switches to V_{DD}, S_1 and S_3 are activated, connecting the lower terminal of the capacitor with V_{DD} and the upper terminal with $CLKD$. Therefore, the voltage seen by node $CLKD$ is

$$V_{CLKD} = V_{DD} + V_{CD} = 2V_{DD}$$

However, it is essential to note that a finite load capacitance value (C_L) can affect the performance of this system, as it absorbs part of the charge previously stored in C_D. Therefore, a more appropriate output voltage value is

$$V_{CLKD} = \frac{2 \cdot V_{DD}}{1 + \frac{C_L}{C_D}} \tag{13}$$

Implementing this capacitor C_D with an NMOS transistor of dimensions $W/L = 15\mu m/15\mu m$ is sufficient to handle a load of more than 50 switches (the modulator has approximately 34 in each phase) with a reduction of less than 1% in any corner.

C. Half-Delays implementation

Finally, the modulator requires half-sample delays for feedback signals to the integrators. This work implements a D-type Flip-Flop driven by the phase opposite to that of the comparator. A functional implementation of this D-type Flip-Flop is a very relaxed version of the comparator presented in Section IV. From Figure 11, $(W/L)_{1-4} = 2\mu m/360nm$, $(W/L)_{5-7} = 3\mu m/360nm$, and $(W/L)_{S1-4} = 1\mu m/360nm$ are defined. The same output stage is used for this Flip-Flop.

VII. Simulations Results

As a result of this work, a 2nd order $\Delta\Sigma$ modulator described by the block diagram in Figure 25a) and a 3rd order $\Delta\Sigma$ modulator described by the block diagram in Figure 25b) are implemented. Figure 25c) shows the circuit implementation of the third-order modulator. The circuit implementation of the second-order modulator is the same as shown in 25c), but without an integration stage.

Two validation tests show the implemented modulators' performance: input range validation and validation against process variations. For both tests, the OSR is set to 128, which translates to a clock frequency of $5.12MHz$.

A. Input Range Validation

This validation aims to show how the modulator performs against different input amplitudes, intending to find the overload point of the modulator and its dynamic input range. The modulator is subjected to a transient simulation with sinusoidal input to do this. Sixteen thousand three hundred eighty-four clock cycles are simulated in a typical corner. A sweep is made over the amplitude of the input signal from $14mV$ differential to $1.262V$ differential. The results can be seen in Figure 23, where a) shows the Input Range for the second order $\Delta\Sigma$ Mod with an SNDR peak of $76dB@922mVDiff$ and a Dynamic Range of $53dB$. And b) the Input Range for the third order $\Delta\Sigma$ Mod with an SNDR peak of $90dB@718mVDiff$ and a Dynamic Range of $71dB$.

B. Validation Against Process Variations

For this test, modulators are simulated against process variations: variations in the mobility of n-type charge carriers, variations in the mobility of p-type charge carriers, variations in passive device values, variations in the supply voltage of 1% over $910mV$, and temperature variations from $-40C$ to $125C$. This simulation is carried out with a differential input amplitude of 500 mV. The results of these simulations are presented in Figure 24. In a), the corners show a variation in the output resolution, oscillating between $57dB$ and $75dB$. On the other hand, in b), the corners show considerable variations in the final resolution of the output signal, varying between $52dB$ and $86dB$. This can be observed in the presence of the third harmonic.

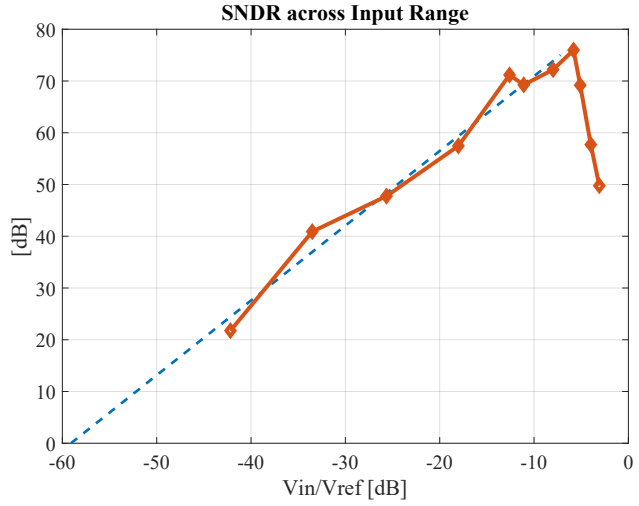
Simulation results are summarized in Table IV.

TABLE IV
Modulators Results.

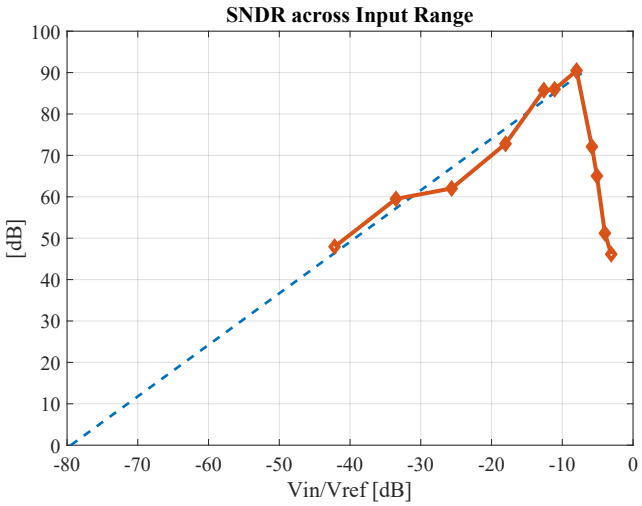
Specification	2nd Order Modulador			3rd Order Modulator		
	Min	Typ	Max	Min	Typ	Max
Supply Voltage (V)	$900m$	$910m$	$920m$	$900m$	$910m$	$920m$
Sampling Frequency (MHz)		5.12			5.12	
Bandwidth (kHz)		20			20	
Order		2			3	
Peak SNDR (dB)		76			90	
DR (dB)		53			71	
Power Consumption (μW)	17.16	81.4	250	17.48	105	337

VIII. Future Work

This work leaves a solid experience in the design of low-supply voltage Delta-Sigma modulators. However, different opportunities exist for improvement and optimization of this

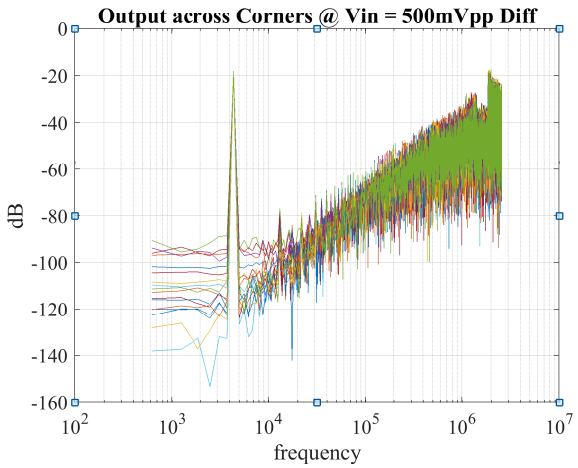


(a)

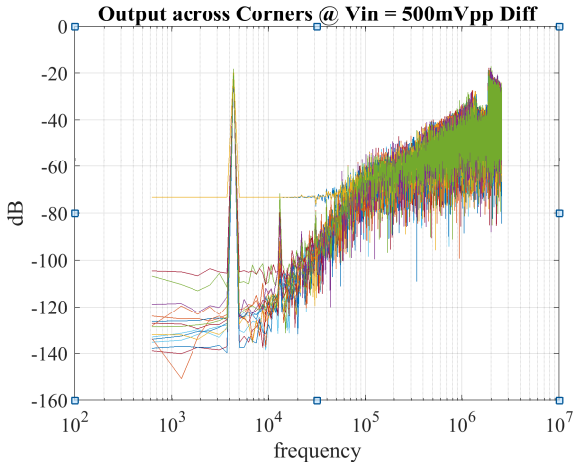


(b)

Fig. 23. SNDR for an amplitude sweep at the modulator input. a) 2nd order $\Delta\Sigma$ modulator. b) 3rd order $\Delta\Sigma$ modulator



(a)



(b)

Fig. 24. Output PSD at $500mV$ diff across corners. a) 2nd order $\Delta\Sigma$ modulator. b) 3rd order $\Delta\Sigma$ modulator

implementation. This section discusses some improvement options for this project.

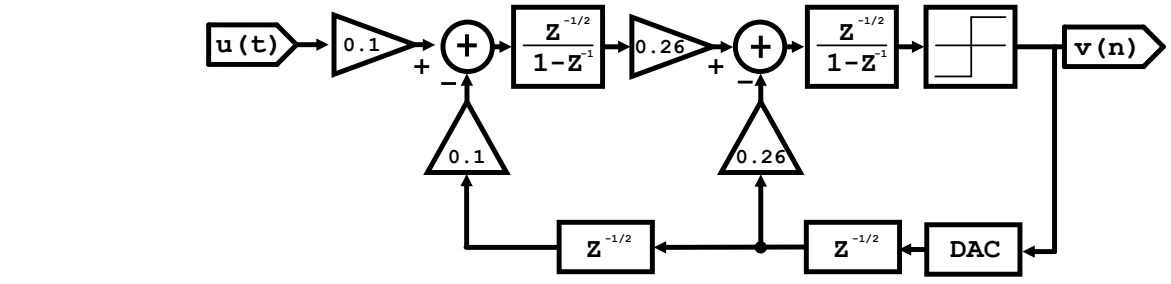
A. FeedForeward Architecture

One of the biggest challenges was fighting against the excursion ranges of the integrator amplifier, which in this project was more challenging than usual when using inverters as amplifiers. This problem is related to the implemented modulator architecture. [15] proposes an architecture called *Reduced Integrator Swing Range* (RISR), shown in Figure 26a). This architecture uses a feedforward loop to make the output of the integrators process only quantization noise for noise shaping. On the other hand, [16] proposes an improvement to this architecture by inserting a 1-sample delay in the feedforward feedback path, as shown in Figure 26b). This delay reduces the demands on the comparator's response, which conventionally must respond fully in the clock's death time.

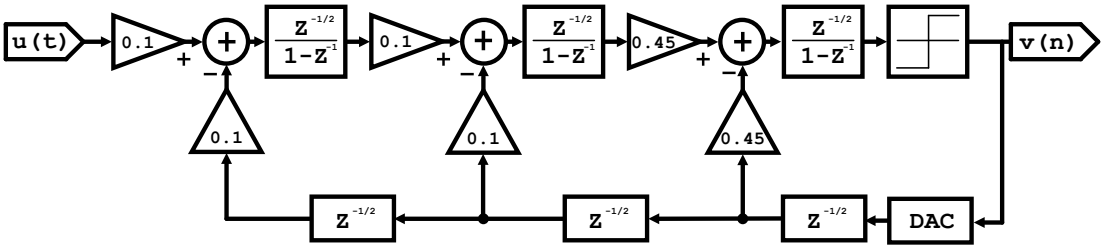
The primary power consumption for this work is to guarantee that the inverters can achieve the specifications for all process variations. This feedforward architecture is shown as a great candidate to continue reducing the system's power. By decreasing the excursion ranges of the integrators, the amount of charge that the inverters must provide to the integration capacitors is reduced.

B. Matlab Modeling

One branch to be explored in this project is the complete and robust modeling of the statistical process variations that technology may present. A design methodology based on high-level modeling using MATLAB has been implemented for this work. Throughout the design of these modulators, the common practice of using fast behavioral models to more accurately predict the response of the system's internal blocks in state-of-the-art is observed. Continuous feedback between the behavioral model and circuit-level simulation results is an option that significantly facilitates the design of a Delta Sigma modulator.



(a)



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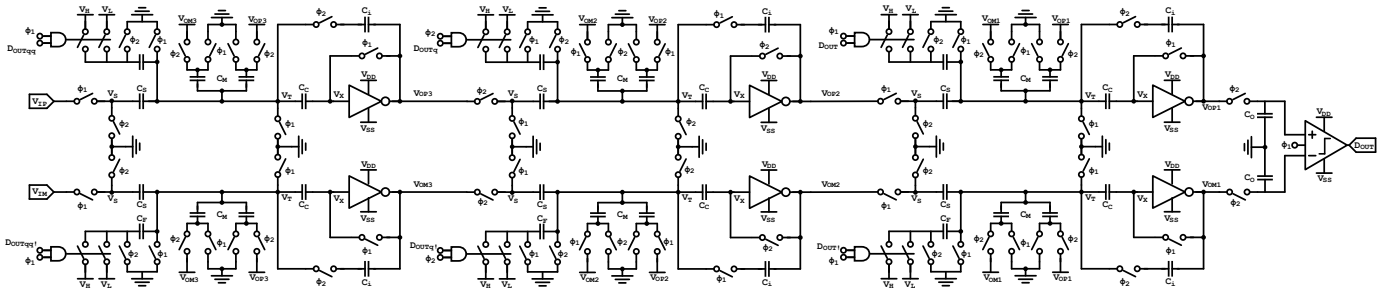
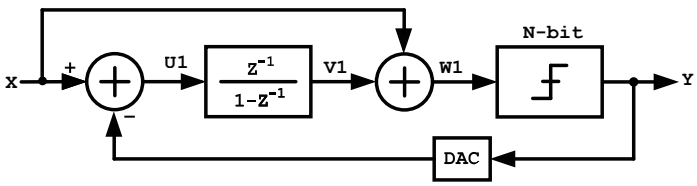
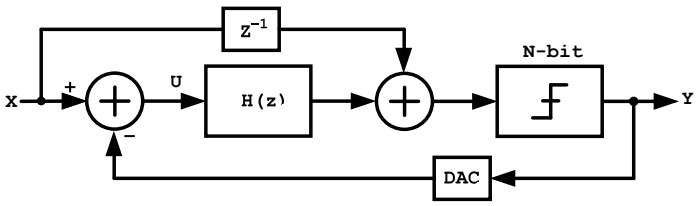


(c)

Fig. 25. Block diagrams and Schematic for implemented $\Delta\Sigma$ modulators. a) Block diagram for implemented 2nd order $\Delta\Sigma$ modulator. b) Block diagram for implemented 3rd order $\Delta\Sigma$ modulator c) Schematic for implemented 3rd order $\Delta\Sigma$ modulator



(a)



(b)

Fig. 26. Feedfoward Architecture. a) RISR topology [15]. b) Relaxed Timing constrains topology [16]

IX. Summary

This project presents the design of two classic FeedBack architecture $\Delta\Sigma$ modulators, implementing a methodology that relates behavioral simulation with circuit simulation. This project focuses on reducing these systems' power consumption as much as possible without affecting the final resolution. The techniques implemented for reducing the power consumption of the modulator were:

A. Switched capacitor integrators

The implementation of switched capacitor integrators (Figure 7b)) reduces the power consumption of the system by removing passive elements with active power consumption that dissipate heat during operation.

B. Reduced supply voltage

Reducing the supply voltage is one of the most direct techniques for reducing power consumption. However, this significantly challenges biasing and correct operation of devices throughout the circuit. These challenges are solved by implementing inverters as switch integrators and clock boosters. With this, a supply voltage as low as $0.9V$ is achieved, which is lower than the sum of the threshold voltages of CMOS transistors ($|V_{THP}| + V_{THN}$).

C. Current reduction in typical design

Each element, except for the inverter operating as an amplifier, was designed to minimize current consumption as much

as possible to meet specifications. Note that in some cases, this reduction will have a cost in the area.

In addition to these techniques, implementing a Feed-Forward architecture is proposed to reduce integrators' excursion range requirements and the speed requirements of the quantizer, thus reducing power consumption.

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