**Modeling and Simulation: Mini project**

# Project Description

My master project will consist of the design and implementation of a temperature sensor for low power consumption and high-resolution applications, within this, there will be a voltage comparison block (A comparator), which will possibly be replicated several times. I would like to propose an analysis of the system to equations that define the performance of the comparator for various aspects such as offset, power consumption, speed, among others. With this create a relationship between the parameters of the transistors and the required specifications. From this would be to create the objective function that receives as input the physical parameters of the CMOS transistors W, L (and perhaps also Vgs, Vds, or others, depending on the analysis to be done) to optimize the values of the comparator specifications. This objective function may converge to a Figure of Merit proposed by me, based on the requirements of the system.

# Derivables Proposed

In this order of ideas, I could suggest these steps for the development of my proposal:

1. Definition of the comparator architecture and workspace (folder structure) of this project **(May 17)**
2. Analysis of the comparator as a system, to determine the relationship between the behavioral parameters of the transistor (such as Idsat, gm, Id, r0, etc) and the specifications of the full comparator (such as offset, power consumption, response speed, among others). This comes from Razavi's paper (there are two I think).
3. Definition of the CMOS transistor model to be used, to calculate the behavioral parameters (such as Idsat, gm, r0, etc) from the physical parameters that the transistor receives as input (such as W, L, Id, Vgs, Vds, ...). In IC design this is known as defining the bias of the device, in transistor technologies of size in the order of tens of nanometers or less this is not a trivial task at all and therein lies the power of this mini project **(May 24).**
4. Definition of the objective function (or Figure of Merit) which will be the function to be optimized. This would be a function f: Rn -> R1. This "n" would be equal to the number of parameters per transistor multiplied by the number of relevant transistors in the system **(May 24).**
5. Test different optimization algorithms for the calculation of the physical parameters of the transistor (such as W, L, Id, Vgs, Vds, ...) that optimize the previously defined objective function. **(May 31)**
6. Verification by SPICE simulation of the transistors as defined by the optimization to corroborate the design specifications. If necessary, some manual calibration **(June 07).**

# Development

## Definition of the Comparator Architecture

This design will be based on [1] B. Razavi, "The Design of a Comparator [The Analog Mind]," in IEEE Solid-State Circuits Magazine, vol. 12, no. 4, pp. 8-14, Fall 2020. Then, the architecture for this comparator is defined in Fig 1.

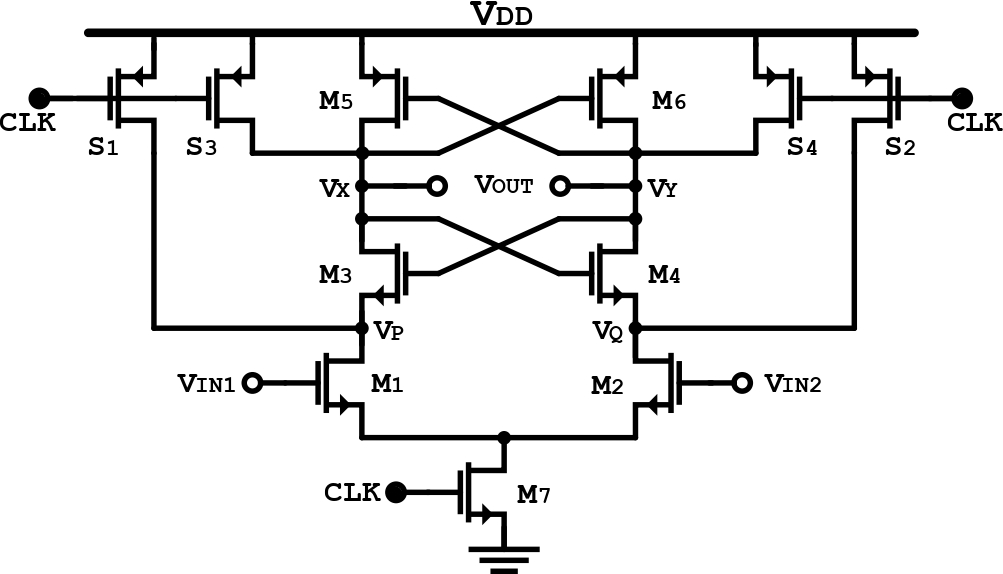


Fig 1. Strong-Arm Comparator Core

## Design Equations.

In an ADC environment, we are interested in the following comparator design parameters: input offset, speed, power consumption, metastability, kickback noise, and input-referred electronic noise. The design begins with the selection of target values for some of these parameters. Here, I aim for an input offset lower than 5 mV; a clock rate, , of 5 MHz; and a power consumption of 1 μW.

I selected the Strong-Arm latch as the comparator core. Shown in Fig 1, this topology offers several desirable attributes: it requires a single clock phase; draws no static power; exhibits an input offset that arises primarily from the input pair, M1 and M2; and delivers rail-to-rail output swings.

The behavior of this Strong-Arm Core is explained in detail by Razavi at [1]

# References

[1] B. Razavi, “The StrongARM Latch [a circuit for all seasons],” IEEE Solid State Circuits Mag., vol. 7, no. 2, pp. 12–17, Spring 2015.