The Field Effect Transistor

1. Introduction

The Field Effect Transistor (FET) has a long story from concept to the first physical implementation. The idea of a field effect transistor was first presented and patented in 1926 by the physicist Julius Edgar Lilienfeld. In 1935, the electrical engineer and inventor Oskar Heil described the possibility of controlling the resistance in a semiconducting material with an electric field in a British patent. A team from Bell Labs formed by John Bardeen and Walter Houser Brattain under the supervision of William Shockley observed and described the transistor effect in 1947. Their trying to build a working FET was unsuccessful, but they accidentally discovered the point-contact transistor. This epochal invention was followed by Shockley's bipolar junction transistor (BJT) in 1948.
In 1945, Heinrich Welker patented for the first time a Junction Field Effect Transistor (JFET). A Japanese team formed by Y. Watanabe and professor Jun-Ichi Nishizawa of Tohoku University patented the Static Induction Transistor (SIT) in 1950. The device controlled current flow by means of the static induction or electrostatic field surrounding two opposed gates (it was conceived as a solid-state analog of the vacuum-tube triode, and the first SIT's were produced in 1970 by several Japanese companies).
In 1952 William Shockley presented theoretical aspects regarding the JFET structure and its operation. Then, the first JFET was produced as a practical device by George Clement Dacey and Ian Munro Ross from Bell Labs in 1953, under the supervision of William Shockley.
In 1959, Mohamed M. Atalla and Dawon Kahng from Bell Labs invented the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). This is the basic component used in digital electronics, and is the most frequently manufactured device in the history (about 1.3×10^{22} MOSFETs were manufactured between 1960 and 2018).

2. FET brief theory

Currently, there are two types of Field Effect Transistors (FET's) that are manufactured on a large scale: the Junction Field Effect Transistor (JFET) and the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The basic material used to produce these transistors is silicon. Depending on the impurities introduced into the silicon in the manufacturing process, there are 2 types of field effect transistors: with n channel and with p channel. Thus, a single type of charge carriers will circulate through a device: electrons for n-channel transistors, and holes for p-channel transistors. For this reason the field effect transistors are called unipolar devices. Because the mobility of the electron is greater than the mobility of the hole, n-channel transistors (through which the electrons flow) are faster than p-channel transistors (through which the holes flow), and therefore are manufactured in greater numbers.

a. The Junction Field Effect Transistor (J-FET)

The JFET is a three terminal device, which presents an area of doped silicon (n-type for n-channel JFET, p-type for p-channel JFET) with two diffusions of the opposite doping (p-type diffusion for n-channel JFET, n-type diffusion for n-type JFET). To allow a symmetrical control of the flow of electrical charges through the channel, the flow control electrode (the gate) is built on both sides of the channel and it is connected to the opposite doping areas (Fig.1).

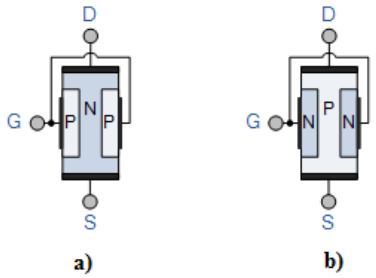

Fig.1.The internal structure for a JFET: a) n-channel J-FET; b) p-chanel J-FET
The terminals are: D-Drain; S-Source; G-Gate

The symbols for the n and p channel JFETS are represented in Fig.2. Although the J-FET is a symmetric device (the source and the drain may be interchanged), there are some situations when, for a discrete component, reversing the terminals (D and S) can damage the device. This can be identified by consulting the part datasheet given by the manufacturer. The drain and the source are connected at either end of the channel region.

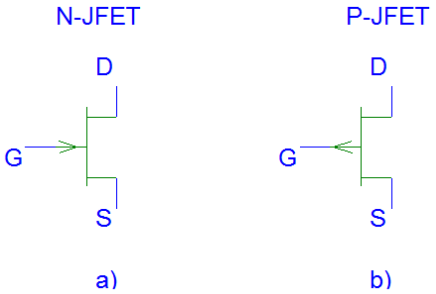

Fig.2.The electrical symbol for the JFET: a) n-channel J-FET; b) p-chanel J-FET
The terminals are: D-Drain; S-Source; G-Gate

The JFET operation is based on changing the drain current (I_D) as a function of the bias voltage applied on the *pn* junction between the gate and the channel (V_{GS}) (Fig.3). Because the gate contacts are internally connected, we have two *pn* junctions in parallel. The *pn* junctions are in reverse bias, so the gate current is very small (order of pico-amps, $I_G \approx 0$).

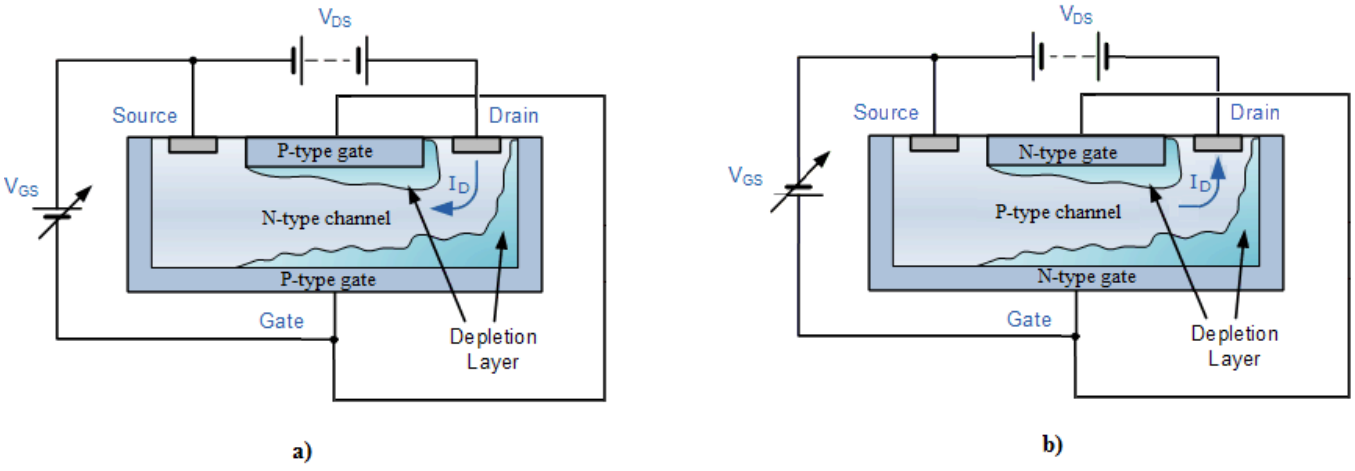

Fig.3.The DC bias for J-FET transistor: a) n-channel J-FET; b) p-channel J-FET

For optimal operation, the transistor needs to be biased from two external DC voltage sources: a drain-source

voltage source (V_{DS}) and a gate-source voltage source (V_{GS}). The V_{GS} source has an inverse polarity compared to the V_{DS} source. When a voltage is applied between the drain and the source, the current will flow through the channel. By changing the V_{GS}, the thickness of the channel is adjusted, and therefore a greater or lesser number of electrical charges (electrons for n-JFET, or holes for p-JFET) will pass through the channel, starting from the source to the drain. If V_{GS}=0V, the device is in a normally on state and a maximum number of electrical charges will pass through the channel. To decrease the drain current, we must apply an appropriate voltage to the gate and use the depletion region created at the junction to control the channel width. In conclusion, it can be seen that the JFET is a voltage controlled device. The drain and the source currents are equal (I_D=I_S) (Fig.4).

1. *Effects on changing V_{GS} (V_{DS}=ct)*

In Fig.4 is represented the schematic diagram with a JFET biased from 2 voltage sources: a constant and small V_{DS} (the width of the channel is almost constant), and a variable V_{GS}. The increasing width of the pn junction depletion region (illustrated from yellow to red to blue), is due to the increasing reverse bias of the junction resulting from the application of a $|V_{GS}|$ of increasing magnitude. As the depletion widths increase, the channel width decreases, resulting in a lower conductivity (higher resistivity) of the channel. As $|V_{GS}|$ is increased, a value of V_{GS} is reached for which the channel is completely depleted (no free carriers) and no current will flow regardless of the applied V_{DS}. This is called the **threshold**, or **pinch-off**, **voltage** and occurs at V_{GS}= V_T = V_P. The threshold voltage is negative for a n-channel JFET($V_p < 0$) and positive for a p-channel JFET($V_p > 0$) .

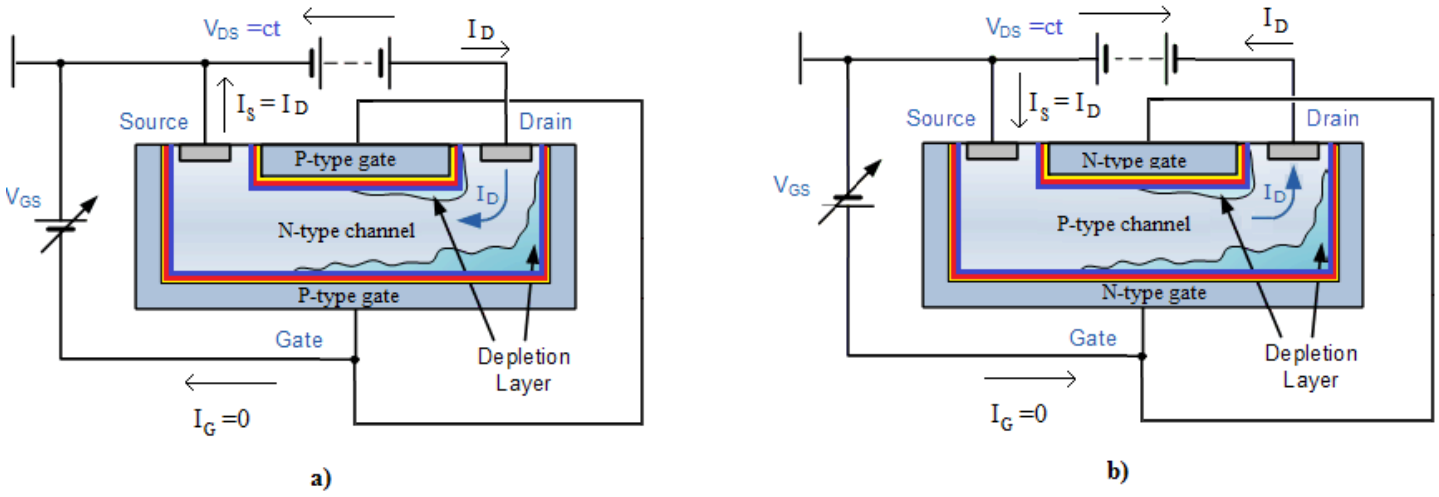

Fig.4.The DC bias analysis at variable V_{GS} for J-FET transistor: a) n-channel J-FET; b) p-channel J-FET

2. *Effects on changing V_{DS} (V_{GS}=0)*

In Fig.5 is represented the circuit which bias the JFET with a variable V_{DS} while V_{GS}=0V. The V_{DS} voltage is positive for a n-channel JFET and negative for a p-channel JFET. We assume a constant doping so that the voltage variation in the channel is linear. When V_{DS} is very small, the voltage variation in the channel is very small and it has no effect on the channel shape. For this case, the depletion region is only due to the pn junction as shown in yellow in the figure. As $|V_{DS}|$ increases, the increasing potential at the drain reverse biases the pn junctions. Since the voltage drop across the channel increases from source to drain, the reverse bias of the pn junction also increases from source to drain. Since the depletion region is a function of bias, the depletion region also gets wider from source to drain, causing the channel to become tapered as shown in red in the figure. The current still increases with increasing V_{DS}, however there is no longer a linear relationship between V_{DS} and I_D since the channel resistance is a function of its width. Further increases in V_{DS}, for example, blue in the figure, result in a more tapered shape to the channel and increasing nonlinearities in the I_D - V_{DS}

relationship. This process continues until a V_{DS} is reached where the depletion regions from the pn junctions merge. Analytically, this occurs when the gate-to-drain voltage V_{GD} is less than some threshold $V_T=V_p$ and is known as the **pinch-off point**. At this point, the drain current saturates and further increases in V_{DS} result in little (ideally zero) change in I_D. For the case $v_{GG}=v_{GS}=0$, the drain current at pinch-off is called the **drain-source saturation current - I_{DSS}**. Operation beyond the pinch-off point ($V_{DS} > |V_{GS}=V_P|$) defines the **normal operating** or **saturation region** of the JFET.

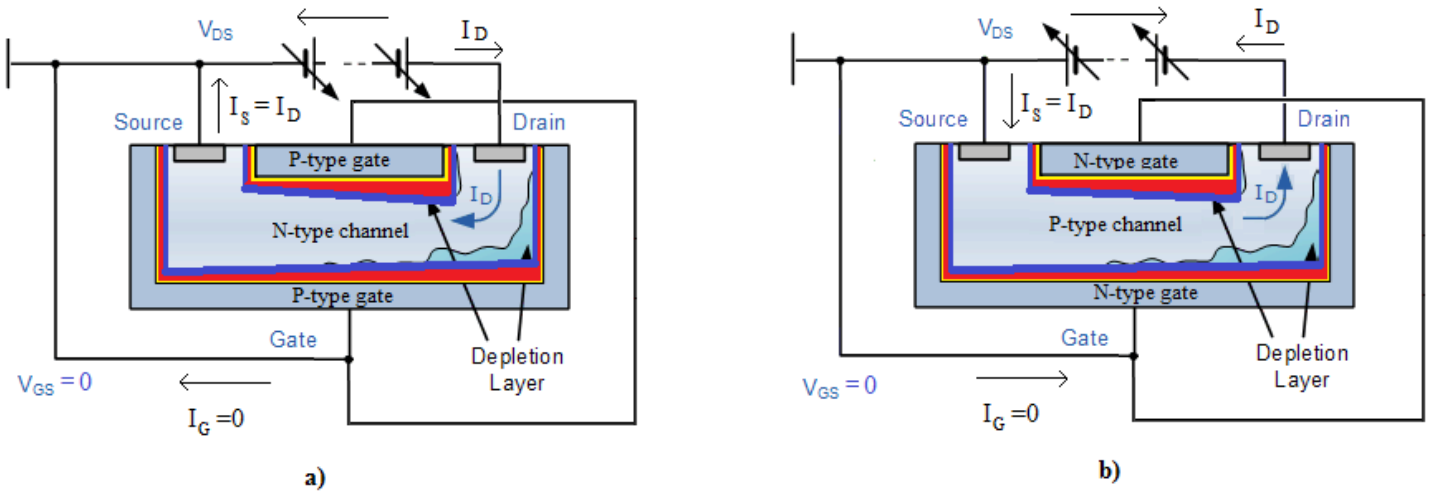

Fig.5.The DC bias analysis at a variable V_{DS} and V_{GS} =0 for J-FET transistor:
a) n-channel J-FET; b) p-channel J-FET

If the V_{DS} variation effect is applied, we can see that pinch-off will occur for lower values of V_{DS} since we have less of a channel to start with (resulting in lower values of I_D at pinch-off). By combining the effect of V_{DS} and V_{GS} variations, a family of characteristic curves will be generated for the JFET (Fig.6).

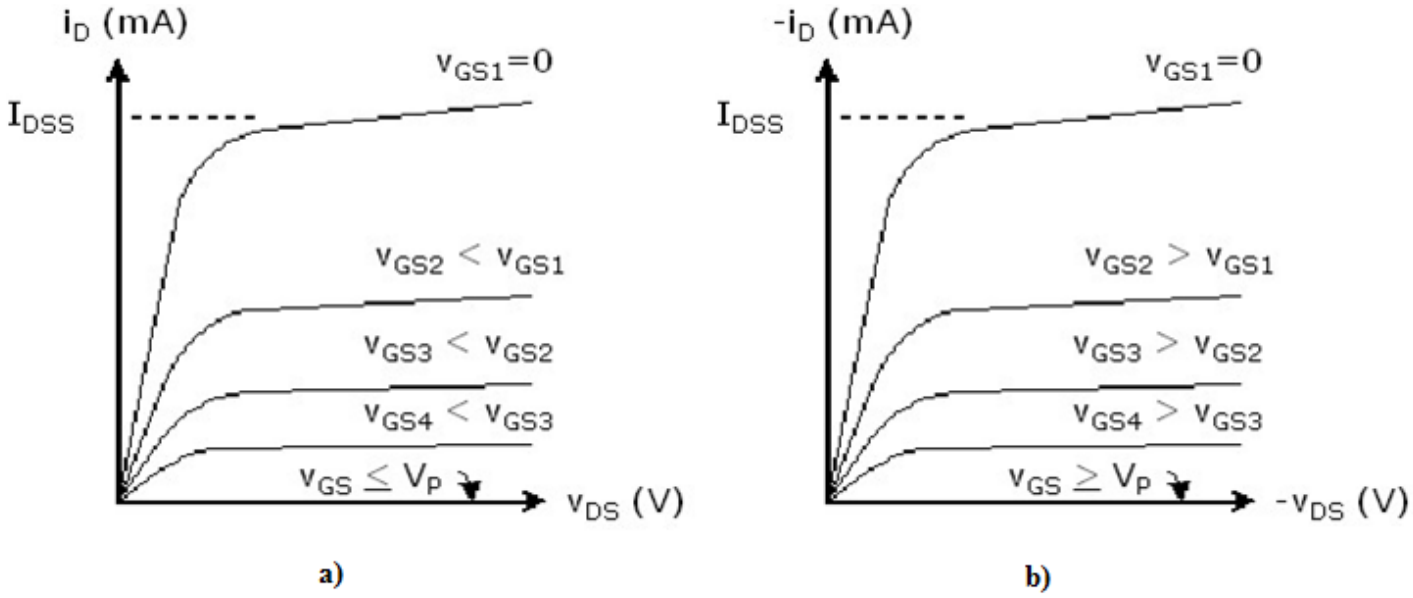

Fig.6.The DC output characteristics at a variable V_{DS} and several values of V_{GS} =ct for J-FET transistor:
a) n-channel J-FET; b) p-channel J-FET

The output characteristic for a n-channel J-FET with detailed explanations is presented in Fig.7. After the JFET reaches saturation, I_D remains relatively constant with a very small slope for further increases in V_{DS} (the slope of the curves would be zero for an ideal device).

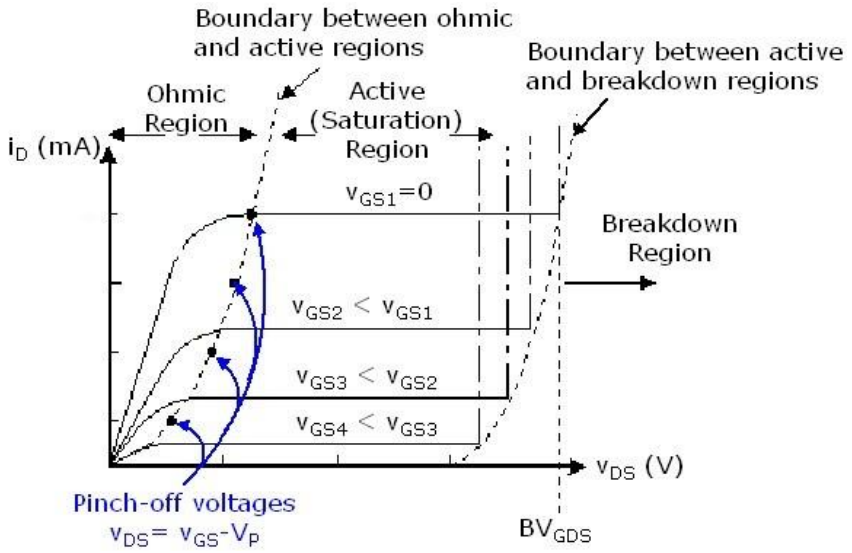

Fig.7.The complete DC output characteristics for n-channel J-FET

The transfer characteristics for n and p channel JFET's are presented in Fig. 8.

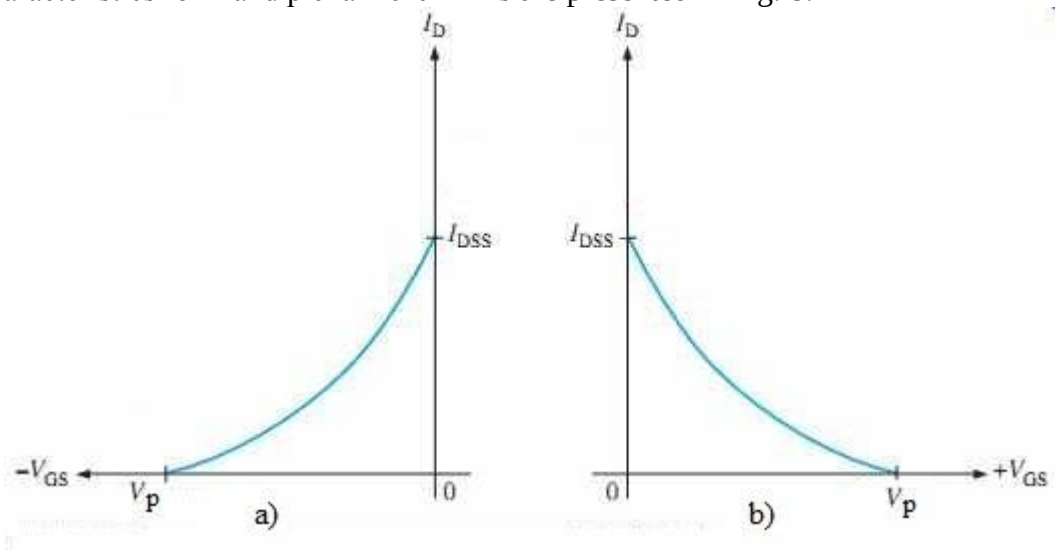

Fig.8.The transfer characteristics for J-FET: a) n-channel J-FET; b) p-channel J-FET

Below pinch-off, the channel essentially behaves like a constant resistance. This linear region of operation is called **ohmic** (or sometimes triode), and is where the JFET may be used as a voltage controlled resistor (the control voltage in V_{GS}). As the magnitude of V_{GS} increases, the range of V_{DS} where the transistor may be operated as an ohmic resistor decreases. In the ohmic region, the potentials at all three terminals strongly affect the drain current. The drain current is:

$$I_D = I_{DSS}\left[2\left(\frac{V_{GS}}{V_P}-1\right)\frac{V_{DS}}{V_P}-\left(\frac{V_{DS}}{V_P}\right)^2\right] \quad (1)$$

Beyond the knee of the ohmic region, the curves become essentially flat in the **active** (or **saturation**) **region** of operation. The transistor may be used as an amplifier in this region. To **operate in the linear region**, it is standard practice to **define the dc bias current as between 30% and 70% of I_{DSS}.** This locates the DC operating point in the most linear region of the characteristic curves.

The drain current in the saturation region may be defined by using the Shockley equation:

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \cdot \left(1+\lambda \cdot V_{DS}\right) \tag{2}$$

The λ is known as the channel length modulation parameter. Usually, especially for large-signal analysis or biasing, λ is small enough that $|\lambda \cdot V_{DS}| << 1$. The parameters I_{DSS} and V_P (sometimes called V_T or $V_{GS(OFF)}$ on the data sheets) are generally given by the manufacturer.

The JFET small signal AC model at low frequencies

The AC small signal model for low frequencies (below 10KHz) of the JFET is given in Fig.9. The transconductance (g_m) and the output resistance of the device (r_o) are:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)\left(1+\lambda V_{DS}\right) \tag{3}$$

$$r_O = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \cdot \lambda} \tag{4}$$

The channel length modulation parameter may be neglected in some situations.

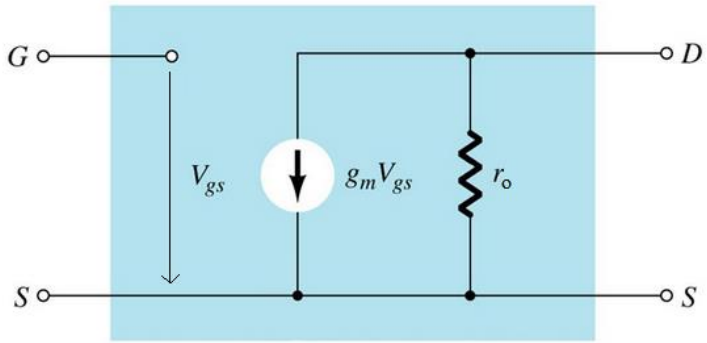

Fig.9.The AC equivalent circuit for J-FET

3. **Laboratory activity**

a. JFET transfer characteristics

Consider the circuit given in Fig.10. The components are described in *Table 4* from Annex 1. It is required to draw and to simulate the circuit. VGS and VDS are DC voltage supplies.

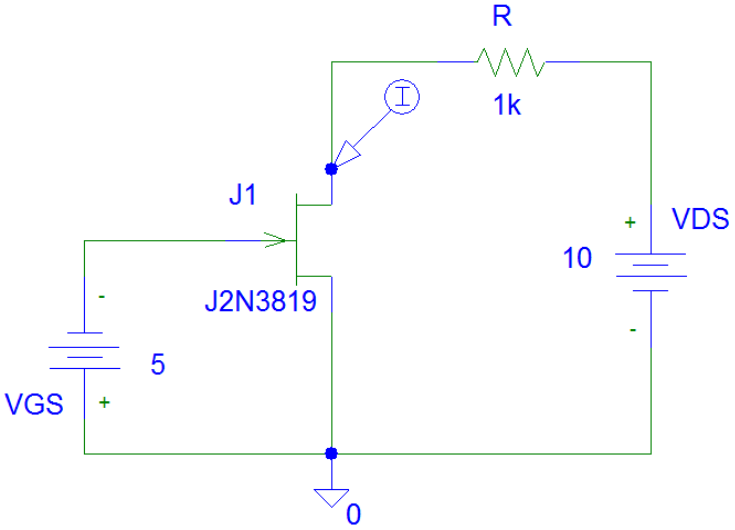

Fig.10 JFET schematic for measuring the transfer characteristics

The drain current (I_D) will be measured as a function of the gate-source voltage (V_{GS}). To do this task, a *DC Sweep…* analysis will be accomplished. The primary DC Sweep voltage is VGS. It will be varied between 0 and 5V with an increment of 0.1V (Fig.11).

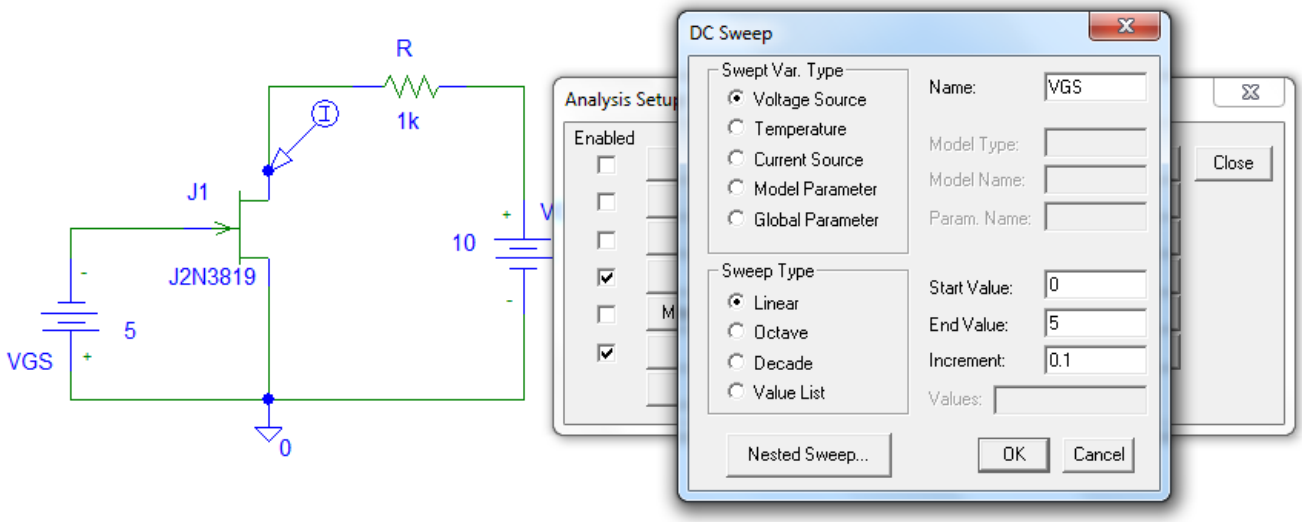

Fig.11 Adjusting VGS for measuring the transfer characteristics

The secondary DC sweep voltage (*Nested Sweep….*) is VDS. It will be varied between 5 and 25V with an increment of 8V. The *Enable Nested Sweep* option will be checked (Fig.12).

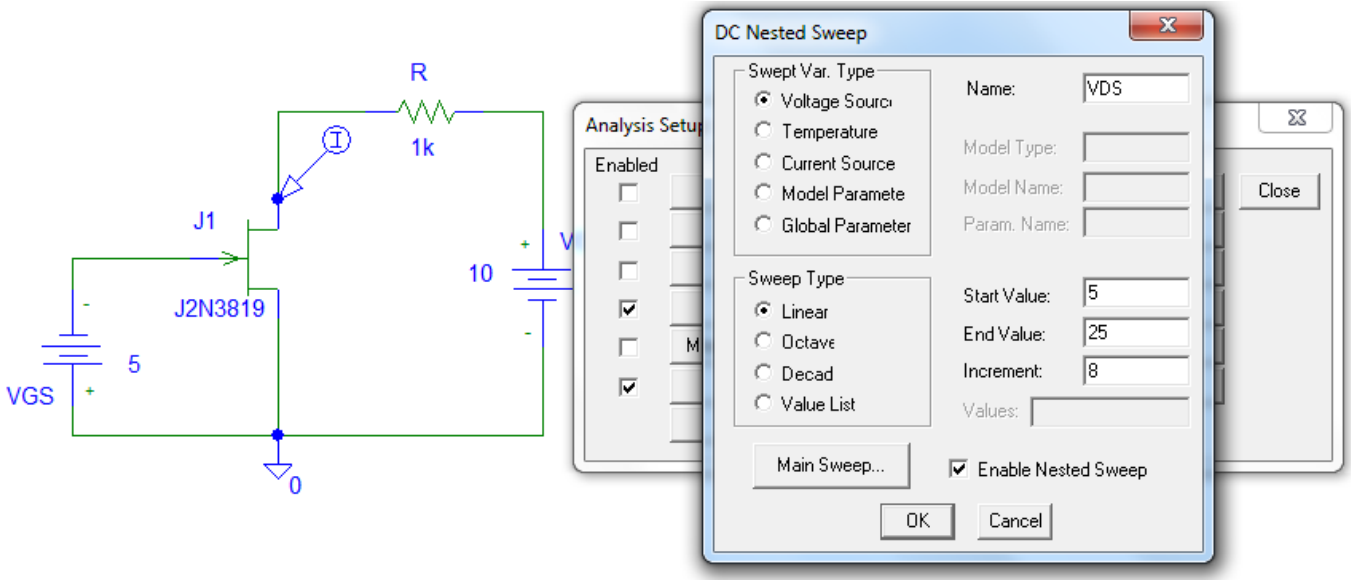

Fig.12 Adjusting VDS for measuring the transfer characteristics

After running the simulation (F11), the drain current will be displayed on Y axis. For the X axis, the selected parameter will be the gate-source voltage which is -V_VGS: *Plot-Axis Settings…-X Axis-Axis Variable….-V_VGS* (Fig.13).

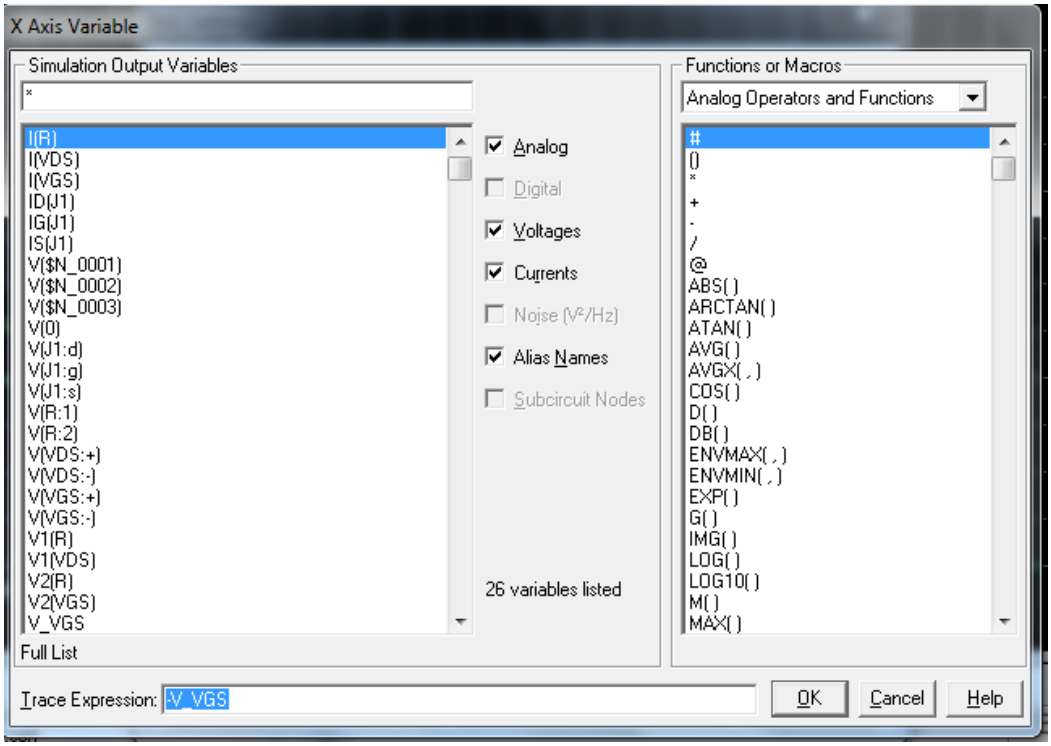

Fig.13 Selecting gate-source voltage on X axis for measuring the transfer characteristics

By selecting the Toggle Cursor, the simulation results may be displayed. For the first two I_D –V_{GS} characteristics, the current saturation occurs because of the drain resistor (R) (Fig.14).

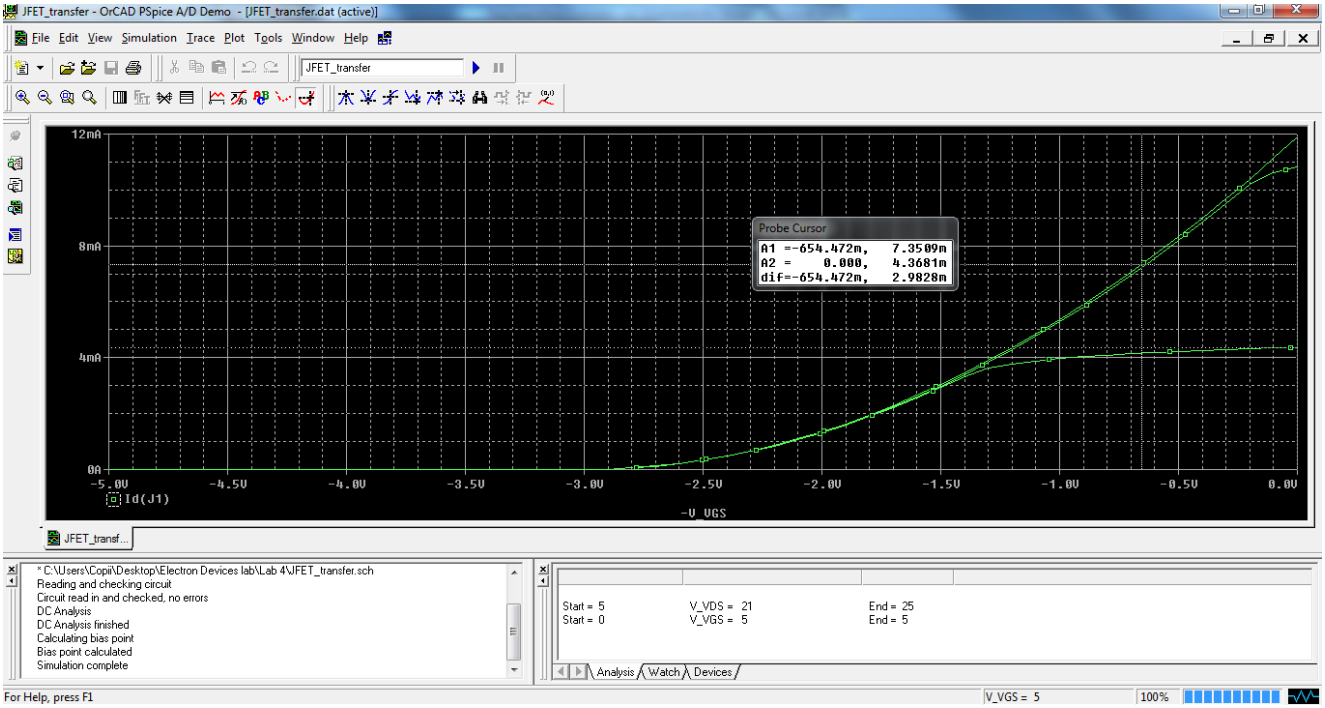

Fig.14.The measurement of the transfer characteristics I_D –V_{GS} for the n-channel JFET

Replace R (1K) by 100 ohms (100) and run the simulation again. Compare the results and complete Table 1.

Table 1 – JFET transfer characteristics

V_{DS}(V)	V_{GS}(V)	I_D(mA)
5	-5	
	-4	
	-2.8	
	-1	
	-0.5	
	0	
13	-5	
	-4	
	-2.8	
	-1	
	-0.5	
	0	
21	-5	
	-4	
	-2.8	
	-1	
	-0.5	
	0	

b. JFET output characteristics

Draw the circuit from Fig.15. It is the same circuit from Fig.10, except some minor changes. VGS and VCC are DC voltage sources.

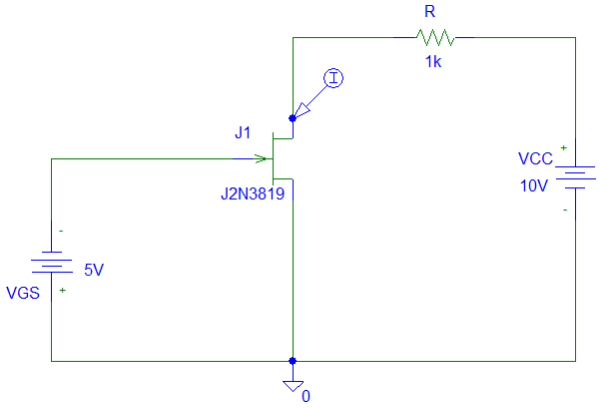

Fig.15 The schematic for measuring the JFET output characteristics

The drain current (I_D) will be measured as a function of the drain-source voltage (V_{DS}). To do this task, a *DC Sweep…* analysis will be accomplished. The primary DC Sweep voltage is VCC. It will be varied between 0 and 25V with an increment of 1V (Fig.16).

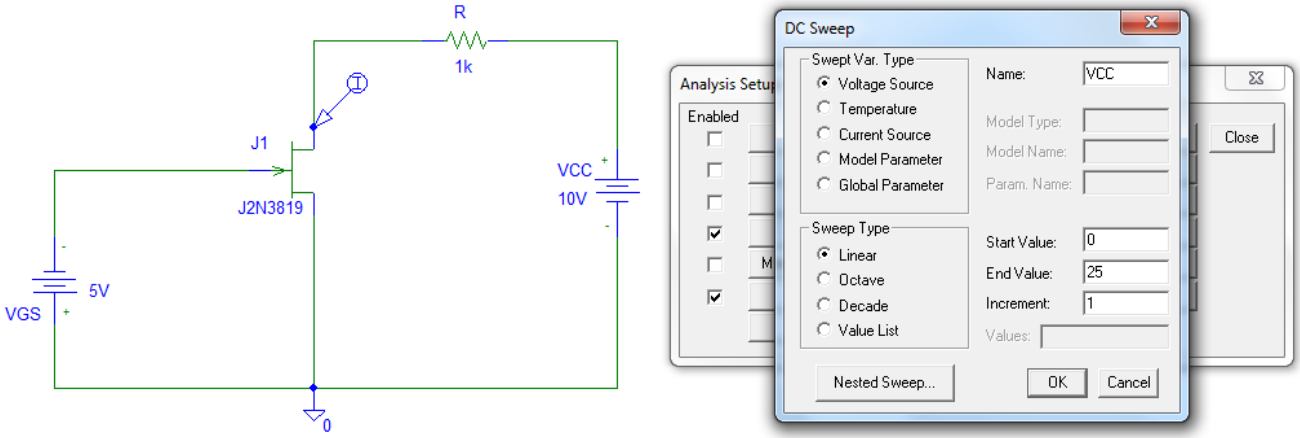

Fig.16 Adjusting VCC for measuring the output characteristics

The secondary DC sweep voltage (*Nested Sweep….*) is VGS. It will be varied between 0 and 3V with an increment of 1V. The *Enable Nested Sweep* option will be checked (Fig.17).

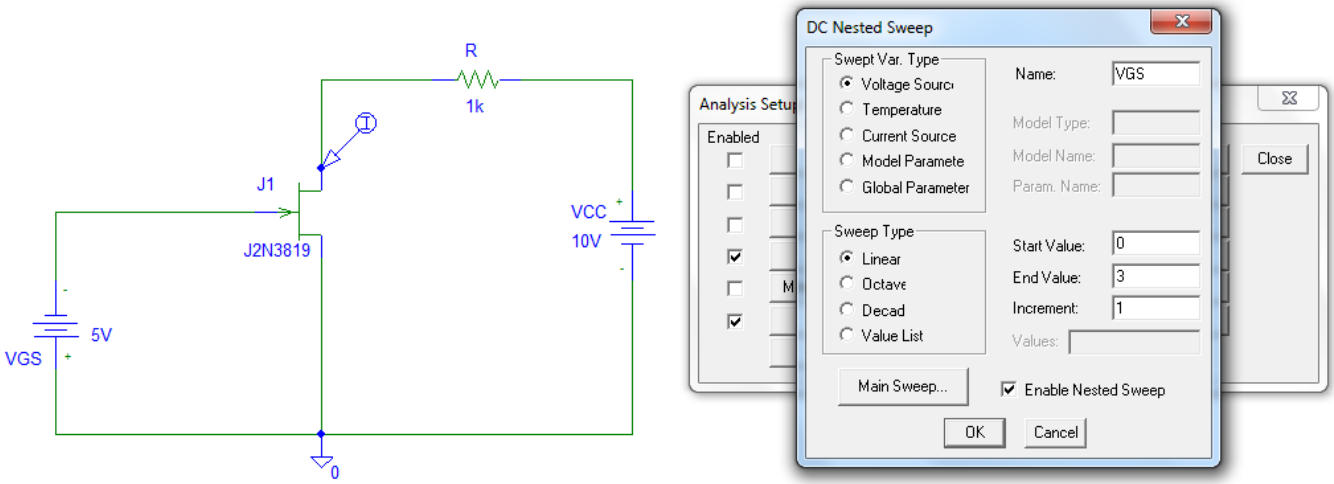

Fig.17 Adjusting VGS for measuring the output characteristics

Then, the simulation may be run (F11). The results are displayed in Fig.18.

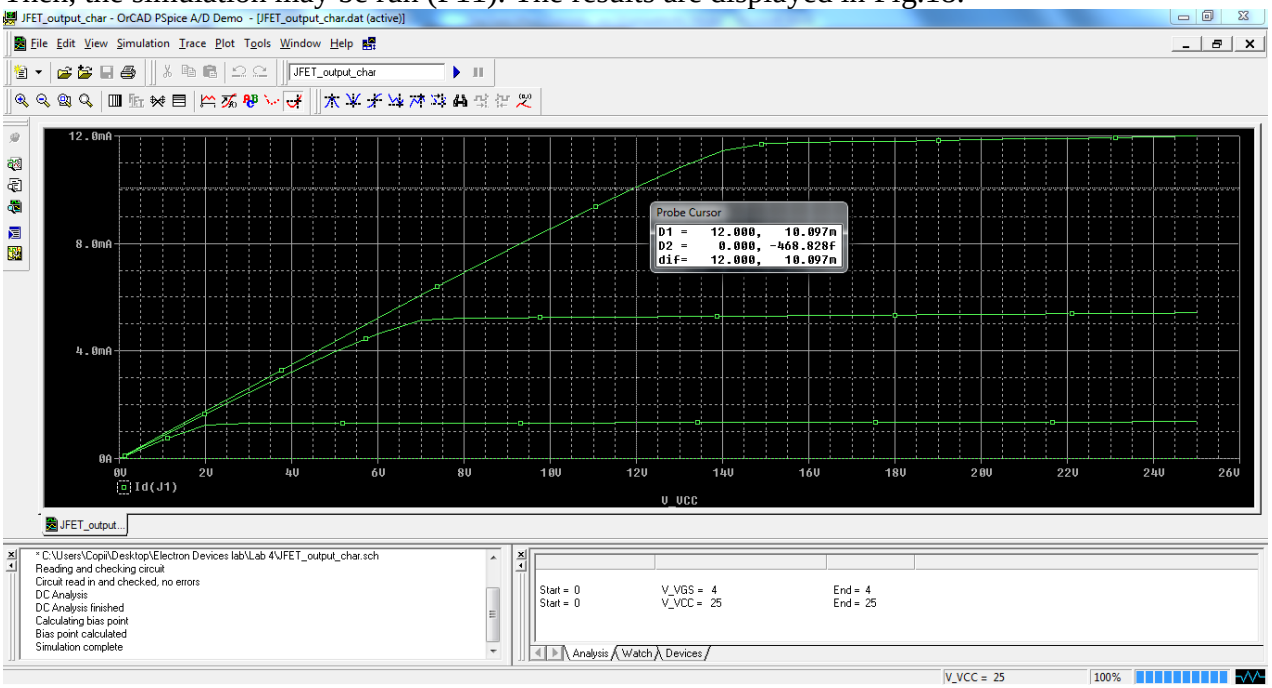

Fig.18.The output characteristics for the n-channel JFET

Replace R by 100 ohms value and run the simulation again. In the Probe window (*Orcad PSpice A/D Demo*), VDS (*V(J1:d)*) has to be represented on X-axis. The simulation results should be written in *Table 2*.

Table 2 – JFET output characteristics

V_{GS}(V)	V_{DS}(V)	I_D(mA)
0	0	
	2	
	4	
	6	
	8	
	10	
	12	
	14	
	16	
	20	
	23.74	
-1	0	
	2	
	4	
	6	
	8	
	10	
	12	
	14	
	16	
	18	
	20	
	24	

-2	0	
	2	
	4	
	6	
	8	
	10	
	12	
	14	
	16	
	18	
	20	
	24	
-3	0	
	2	
	4	
	6	
	8	
	10	
	12	
	14	
	16	
	18	
	20	
	24	

c. JFET AC amplifier

Consider the small signal AC amplifier which uses a n-channel JFET in the common source configuration (Fig.19). The gate bias is made by 2 voltage sources connected in series: a negative DC voltage source (V_{GS}) with a value of -1V and a sine-wave voltage source (Vac), VSIN, with the parameters: VOFF =0, VAMPL=10mV, FREQ=1k, TD=0, DF=0, PHASE=0.

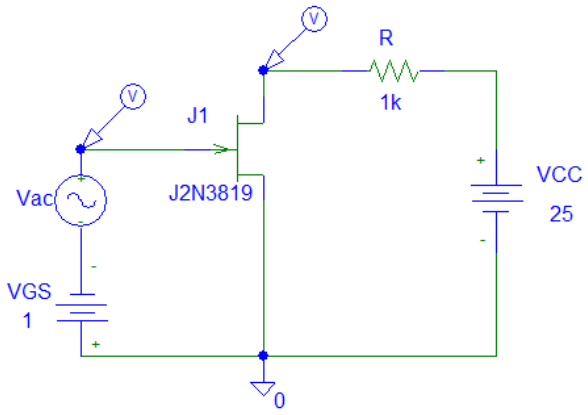

Fig.19.A small signal AC amplifier with n-channel JFET

The simulation should be performed in the time domain (*Transient*), for a time of about 10ms.

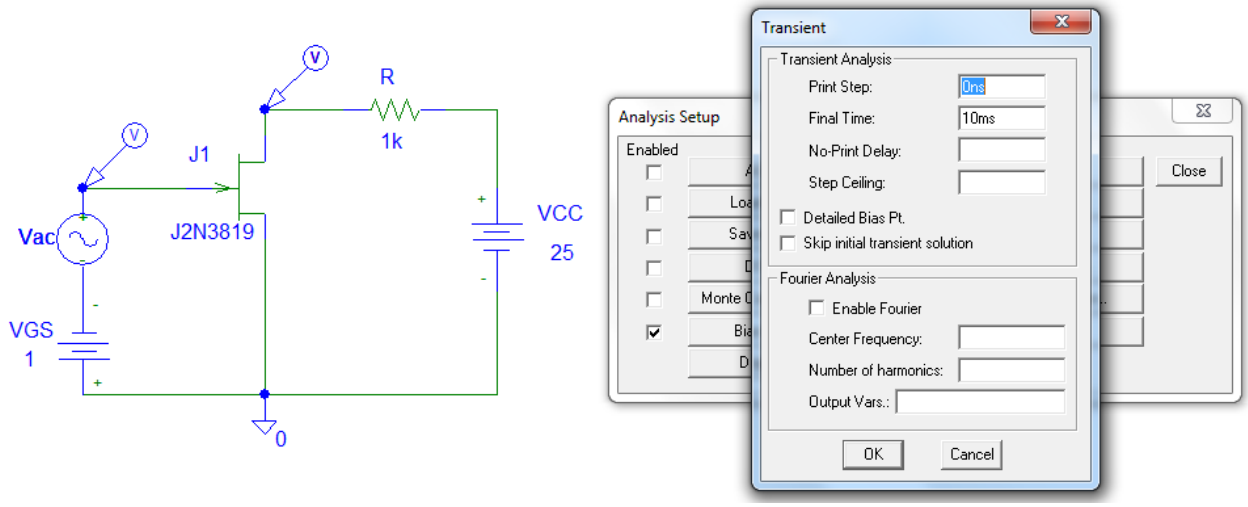

Fig.20. Selecting the Transient simulation for the small signal AC amplifier with n-channel JFET

The output signal may be viewed in the *Probe window*: *OrCAD PSpice A/D Demo* (Fig.21).

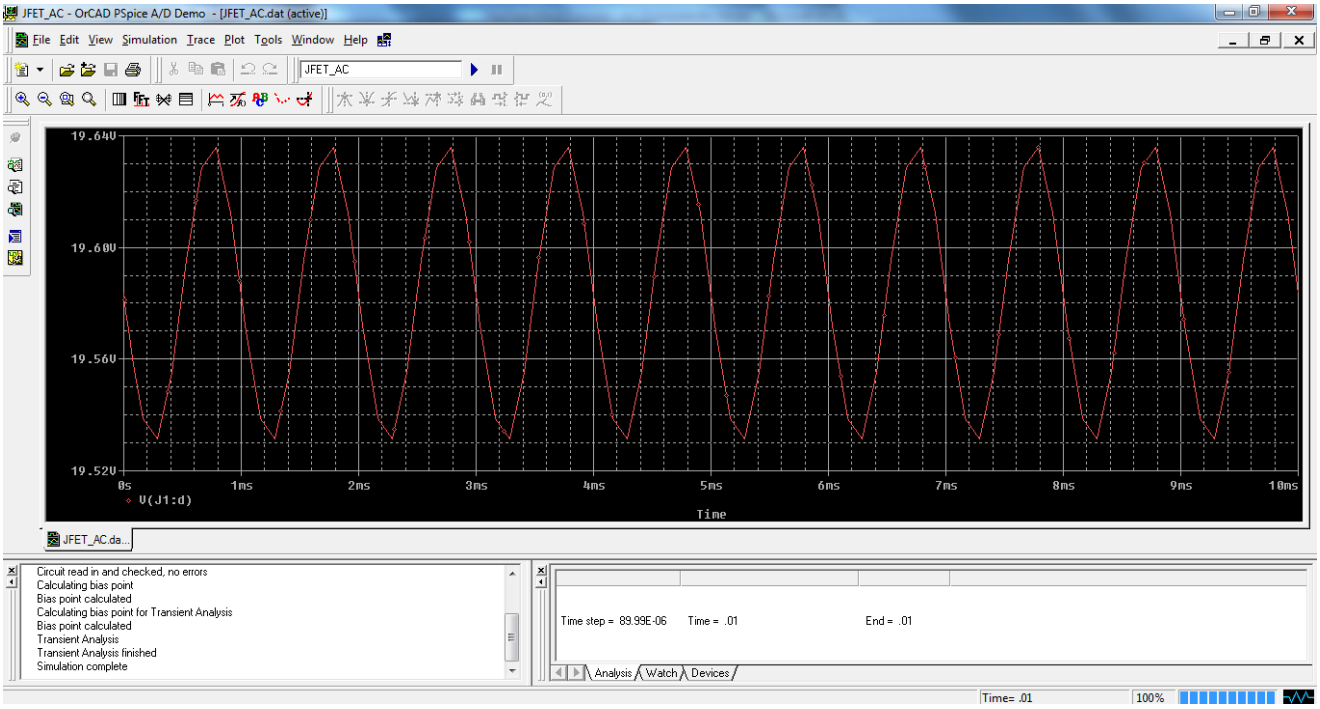

Fig.21.The output signal for the AC amplifier with n-channel JFET transistor

The RMS values for the input (gate) and output (drain) amplitudes may be monitored by selecting: *(MAX(V(J1:g))- MIN(V(J1:g)))/(2*SQRT(2))* for the gate terminal and:
*(MAX(V(J1:d))- MIN(V(J1:d)))/(2*SQRT(2))* for the drain terminal (Fig.22).

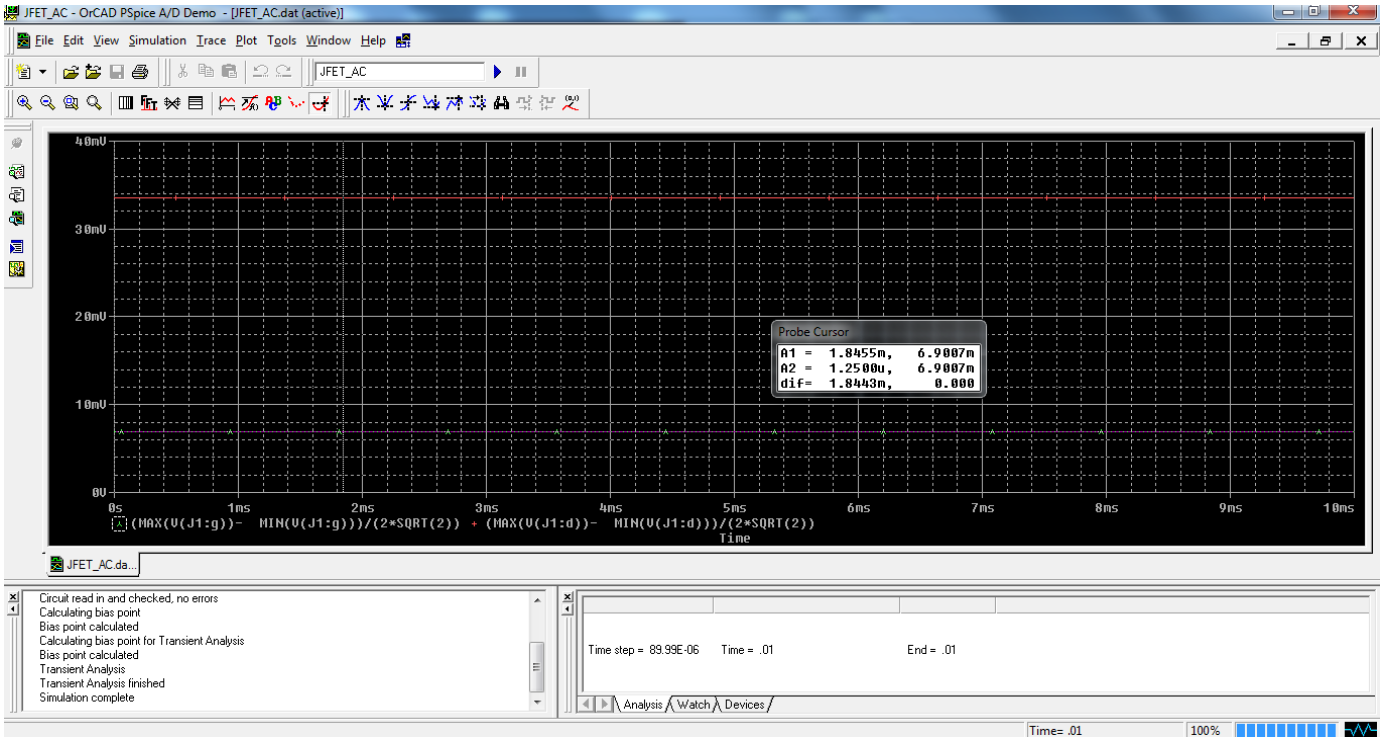

Fig.22.The simulation of the small signal AC amplifier with n-channel JFET transistor (RMS values)

The voltage AC gain is:

$$A_v = \frac{\underline{V_o}}{\underline{V_i}} = \frac{\underline{V_d}}{\underline{V_g}} \tag{16}$$

The current gain is:

$$A_i = \frac{\underline{I_o}}{\underline{I_i}} = \frac{\underline{I_d}}{\underline{I_g}} \tag{17}$$

The transimpedance gain is:

$$A_Z = \frac{\underline{V_o}}{\underline{I_i}} = \frac{\underline{V_d}}{\underline{I_g}} \tag{18}$$

The transadmitance gain is:

$$A_Y = \frac{\underline{I_o}}{\underline{V_i}} = \frac{\underline{I_d}}{\underline{V_g}} \tag{19}$$

Measure the voltages and calculate the AC gains for the amplifier. Compare the phase between the signals. The results should be depicted in *Table 3*.

Table 3

RMS values	A_V	A_I	$A_Z(k\Omega)$	$A_Y(k\Omega^{-1})$
$\underline{V_g}$(mV)=				
$\underline{V_d}$(mV) =				
$\underline{I_g}$(mA) =				
$\underline{I_d}$(mA) =				

Annex 1

Table 4

Pos.	Component type	Value	Library
1.	R (resistor)	Numerical value is taken from the laboratory platform. - Mili-ohms if *m* is written after the numerical value - Ohms if nothing is written after the numerical value - Kilo-ohms if *k* is written immediately after the numerical value - Mega-ohms if *meg* is written immediately after the numerical value	Analog.slb
2.	J1	J2N3819 (n-JFET)	Eval.slb
3.	M1	IRF150 (n-MOSFET)	Eval.slb
4.	VSIN (used to function as a signal generator, sine-wave voltage source for time domain analysis)	- **DC**: the DC component of the sine wave - **AC**: the AC value of the sine wave. - **VOFF**: the DC offset value (set to zero if you need a pure sinusoid). - **VAMPL**: the undamped amplitude of the sinusoid; i.e., the peak value measured from zero if there were no DC offset value. - **FREQ**: the frequency in Hz of the sinusoid. - **TD**: the time delay in seconds (set to zero for the normal sinusoid). - **DF**: damping factor (set to zero for the normal sinusoid). - **PHASE**: phase advance in degrees (set to 90 if you need a cosine wave form). Note: the normal usage of this source type is to set **VOFF**, **TD** and **DF** to zero as this will give you a 'nice' sine wave.	Source.slb
5.	VDC (simple DC voltage source)	- Value in volts.	Source.slb
6.	GND_ANALOG	- Ground (node potential is 0 volts). - It is **mandatory** to be used in any PSpice schematic!	Port.slb

Bibliography

1. Cadence Design Systems, PSpice User's guide, Second Edition, 31 May 2000, Portland, Oregon, USA
2. https://coefs.uncc.edu/dlsharer/files/2012/04/J3a.pdf
3. https://coefs.uncc.edu/dlsharer/files/2012/04/J3b.pdf