ECE 6463 Advanced Hardware Design

Homework 1

Video Link:

https://drive.google.com/file/d/1B2GUOuFfFVl6NRDnb2j3m88rvoSbWjh5/view?usp=sharing

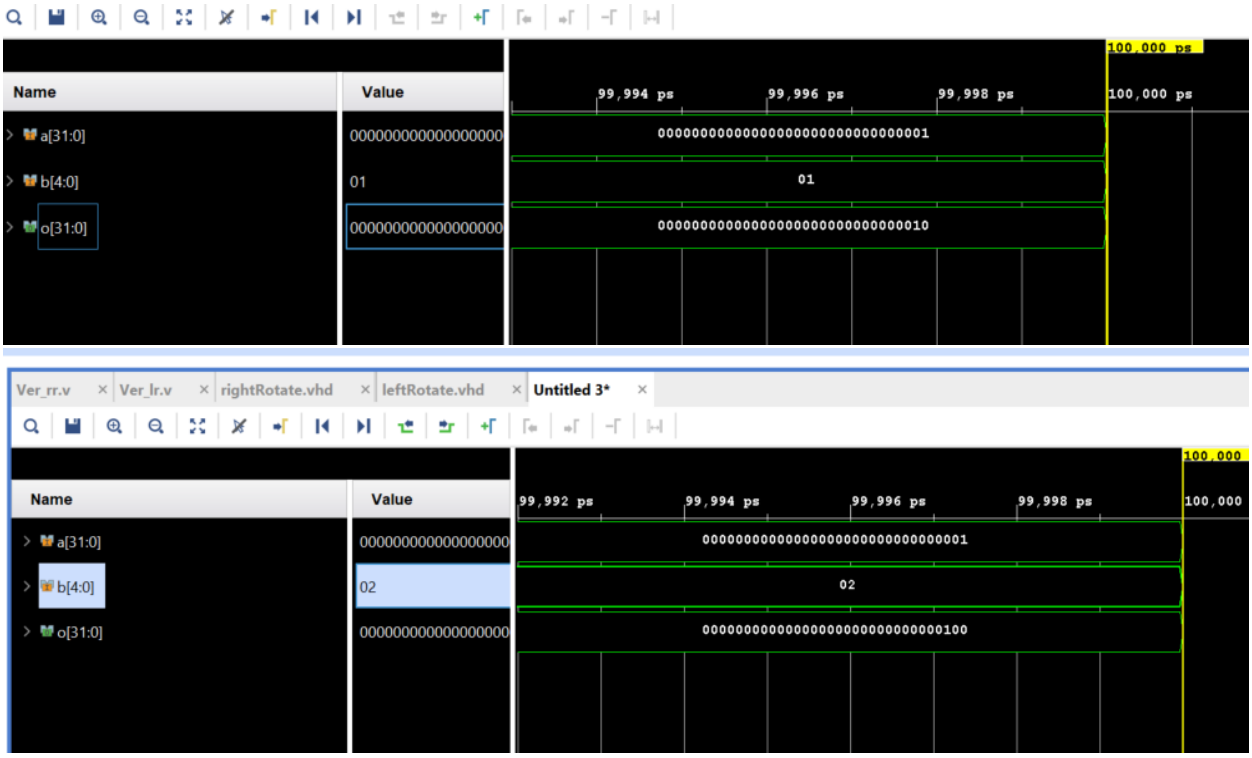
Screenshots of the simulation output:

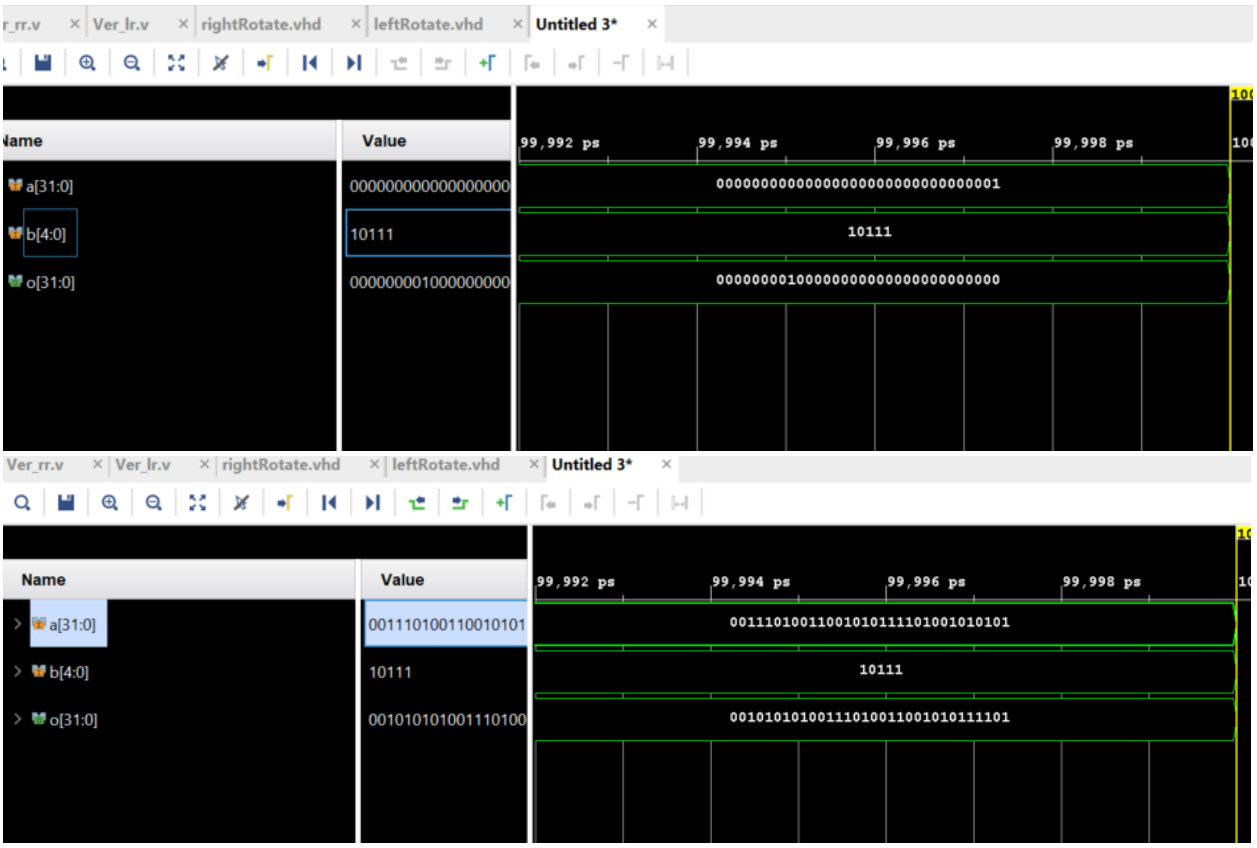
For my test cases, I am only showing a couple of different tests I have done that will indicate the code is working properly.

For the first three cases, the input for a is 1(all zeros and the last digit is 1), the input for b will be 1, 2 and some random value. The last test case all inputs will be random, therefore it can be hard to read from grading perspective, but it will show the output correctness rate.

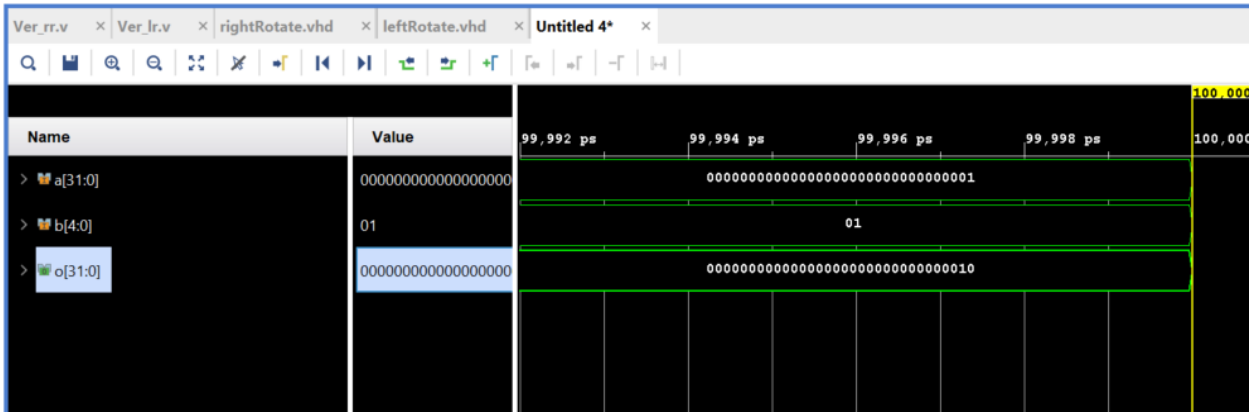
Left Rotate:

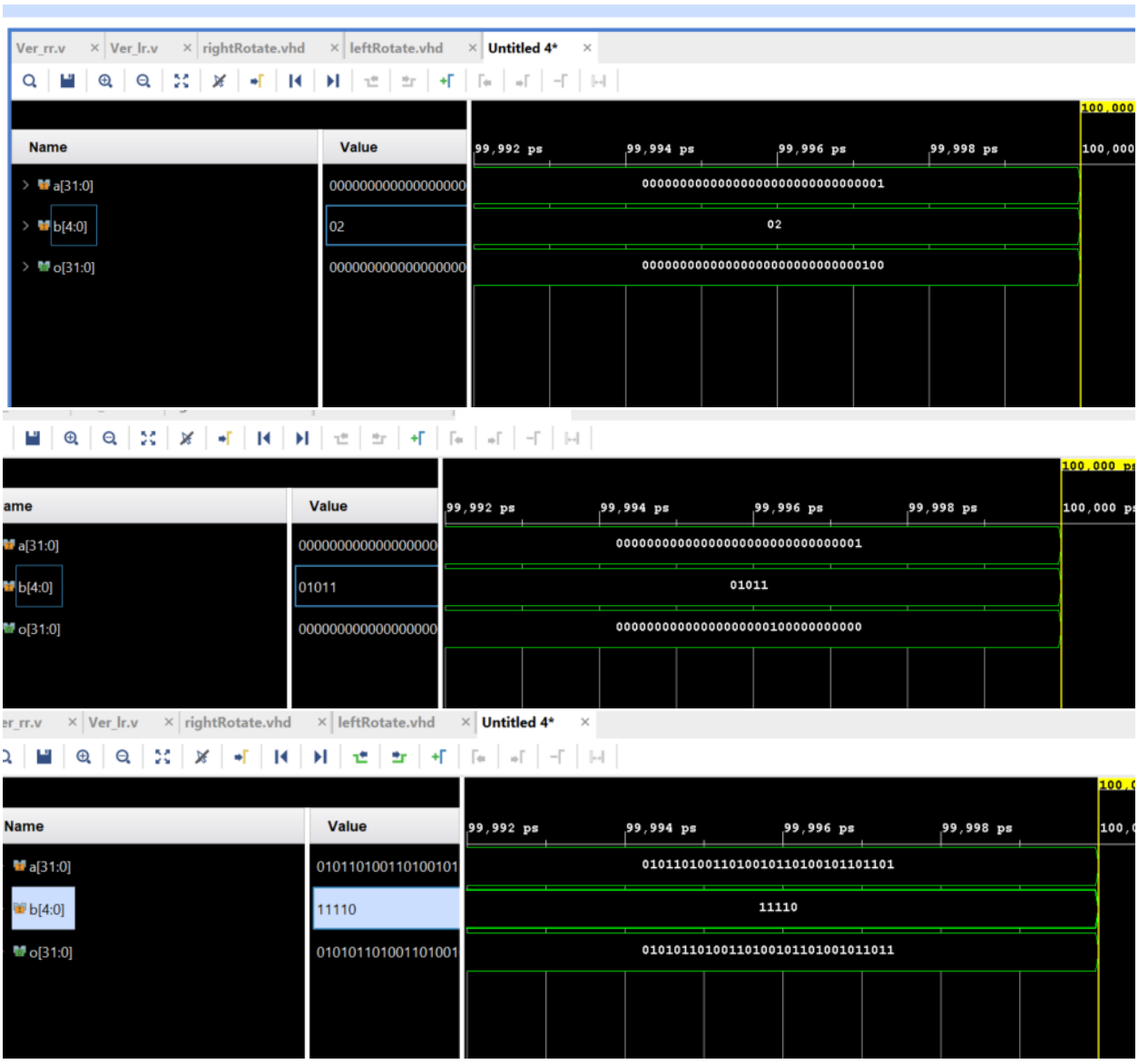
1. VHDL




r_rr.v
Ver_lr.v
rightRotate.vhd
leftRotate.vhd
Untitled 3*
Name
Value
a[31:0]
b[4:0]
o[31:0]
00000000000000000000
10111
00000000100000000000
99,992 ps
99,994 ps
99,996 ps
99,998 ps
00000000000000000000000000000001
10111
00000000100000000000000000000000
Ver_rr.v
Ver_lr.v
rightRotate.vhd
leftRotate.vhd
Untitled 3*
Name
Value
a[31:0]
b[4:0]
o[31:0]
00111010011001010111
10111
00101010100111010011
99,992 ps
99,994 ps
99,996 ps
99,998 ps
00111010011001010111101001010101
10111
00101010100111010011001010111101

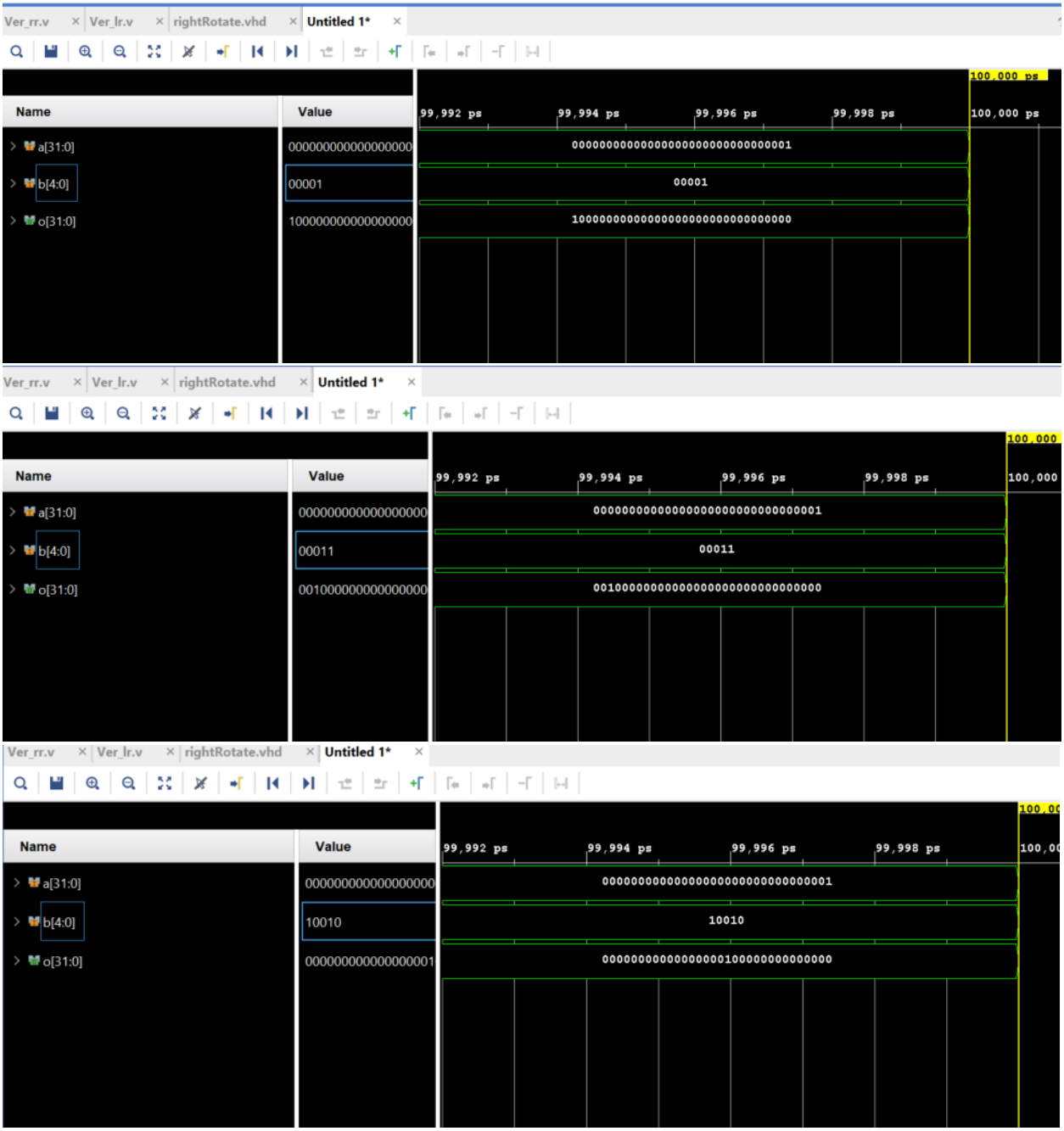
Verilog:

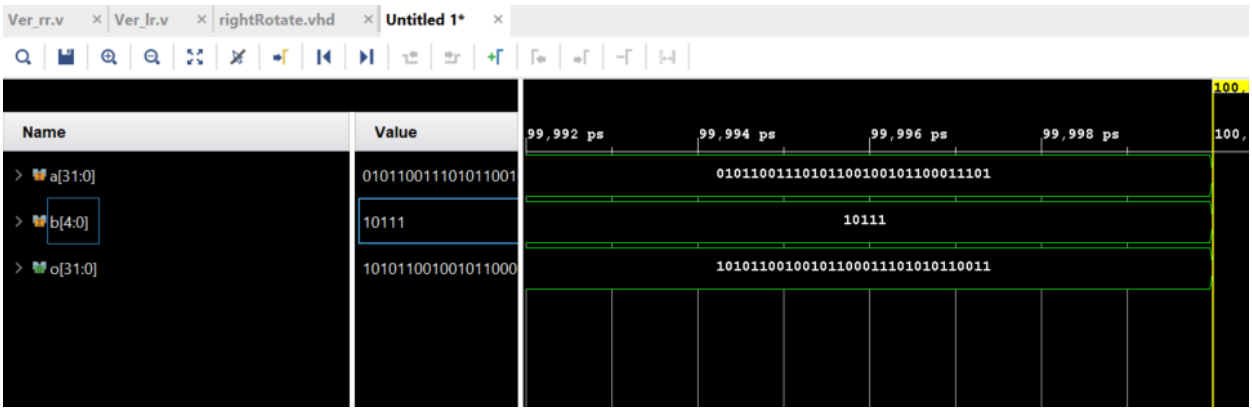

Ver_rr.v
Ver_lr.v
rightRotate.vhd
leftRotate.vhd
Untitled 4*
Name
Value
a[31:0]
b[4:0]
o[31:0]
00000000000000000000
01
00000000000000000000
99,992 ps
99,994 ps
99,996 ps
99,998 ps
00000000000000000000000000000001
01
00000000000000000000000000000010


Ver_rr.v
Ver_lr.v
rightRotate.vhd
leftRotate.vhd
Untitled 4*
Name
Value
a[31:0]
b[4:0]
o[31:0]
00000000000000000000000000000000
02
00000000000000000000000000000100
99,992 ps
99,994 ps
99,996 ps
99,998 ps
100,000
00000000000000000000000000000001
01011
00000000000000000000100000000000
01011010011010010110100101101101
11110
01010110100110100101101001011011

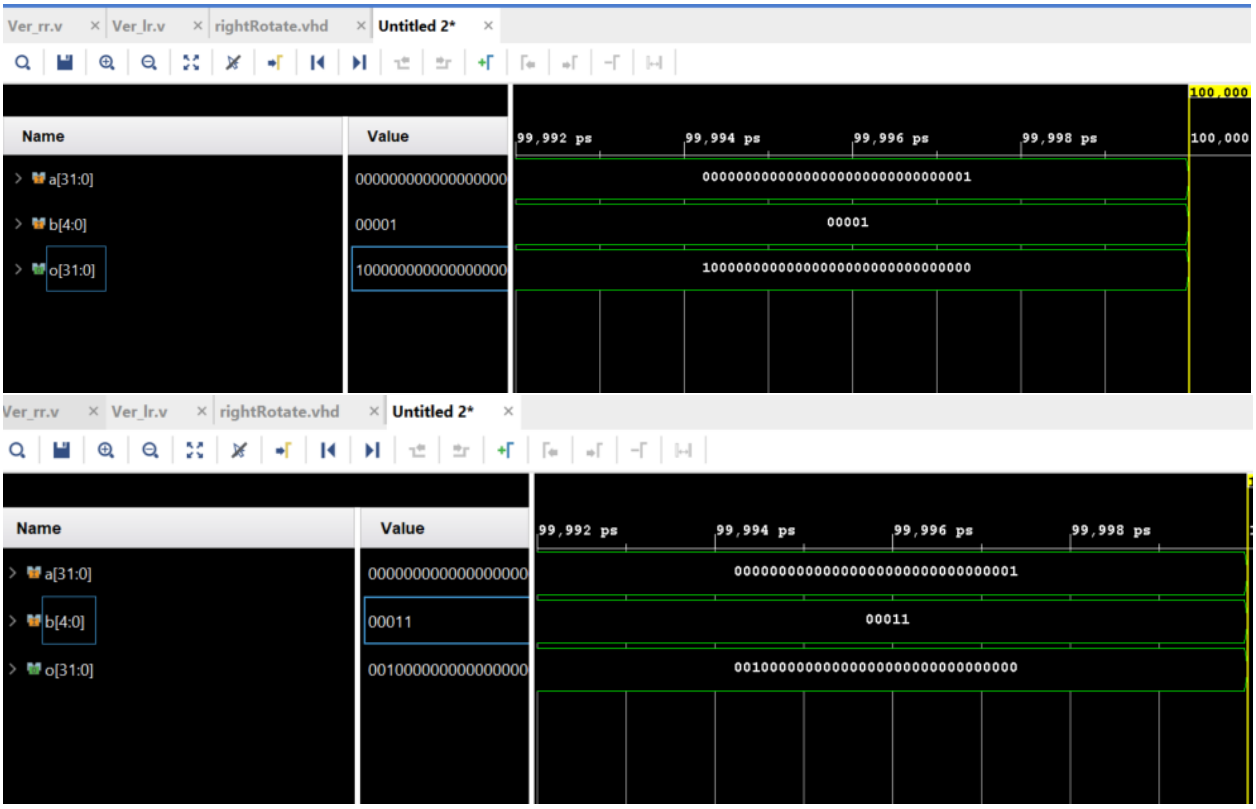
Right Rotate:

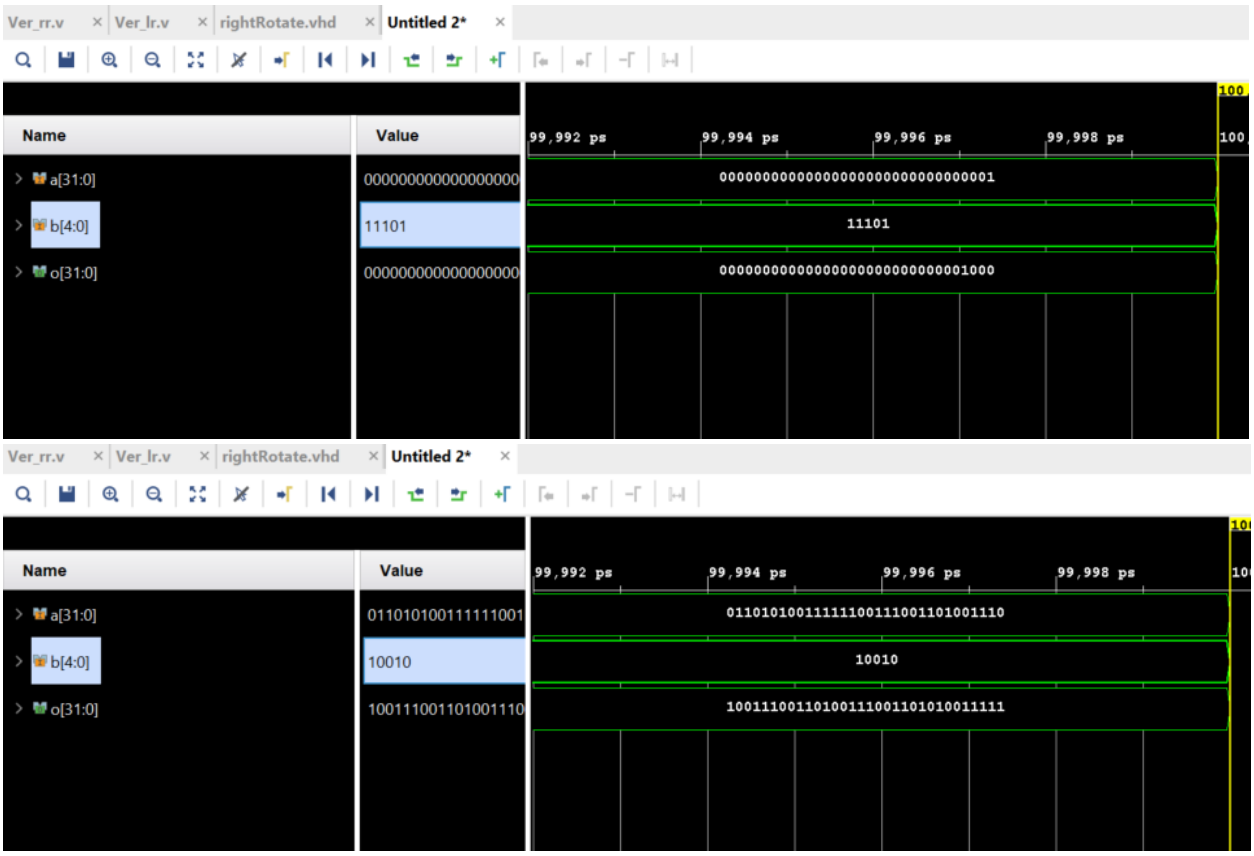
VHDL:




Ver_rr.v
Ver_lr.v
rightRotate.vhd
Untitled 1*
Name
Value
a[31:0]
b[4:0]
o[31:0]
01011001110101100100101100011101
10111
10101100100101100011101010110011
99,992 ps
99,994 ps
99,996 ps
99,998 ps

Verilog:

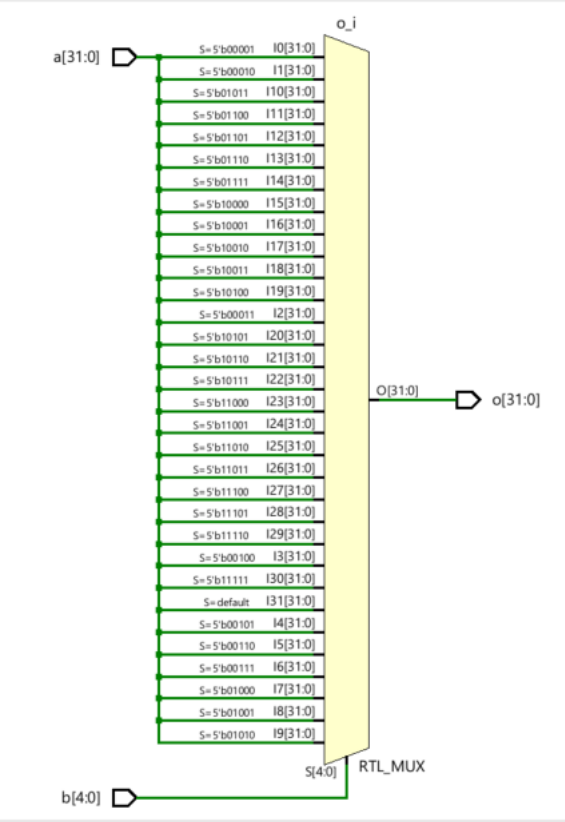

Ver_rr.v
Ver_lr.v
rightRotate.vhd
Untitled 2*
Name
Value
a[31:0]
b[4:0]
o[31:0]
00000000000000000000000000000001
00001
10000000000000000000000000000000
00011
00100000000000000000000000000000
99,992 ps
99,994 ps
99,996 ps
99,998 ps
100,000


Ver_rr.v
Ver_lr.v
rightRotate.vhd
Untitled 2*
Name
Value
a[31:0]
b[4:0]
o[31:0]
00000000000000000
11101
00000000000000000
99,992 ps
99,994 ps
99,996 ps
99,998 ps
00000000000000000000000000000001
11101
00000000000000000000000000001000
Ver_rr.v
Ver_lr.v
rightRotate.vhd
Untitled 2*
Name
Value
a[31:0]
b[4:0]
o[31:0]
01101010011111100
10010
10011100110100111
99,992 ps
99,994 ps
99,996 ps
99,998 ps
01101010011111100111001101001110
10010
10011100110100111001101010011111

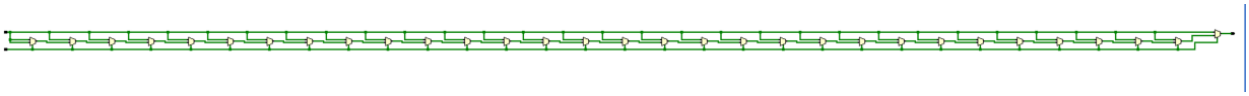
Screen shots of the block diagram:

Left Rotate:

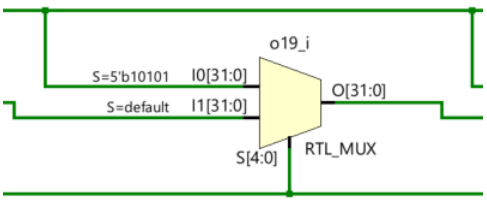
VHDL:



Verilog:

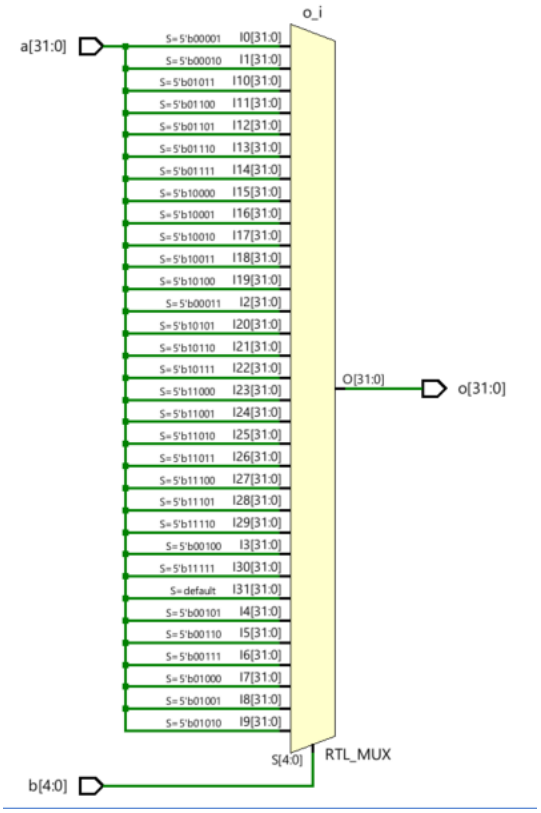


below are one of the MUX screens shot zoomed in for clear reading

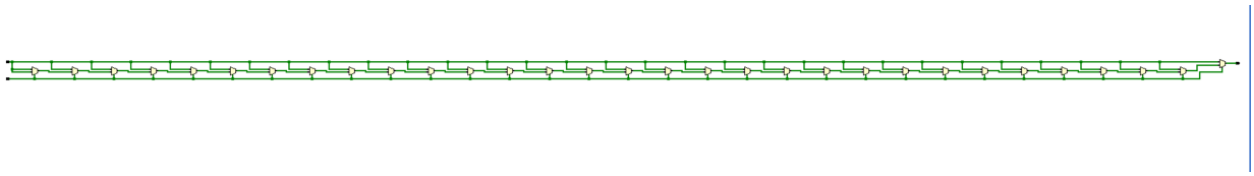


Right Rotate:

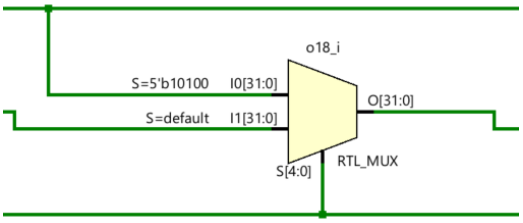
VHDL:



Verilog:



below are one of the MUX screens shot zoomed in for clear reading



Question: Are the logic gates derived from the Verilog and VHDL equivalent?

Answer: It is not equivalent as we can see from the block diagram screenshots.