Report Week 9

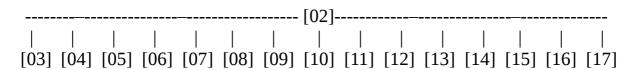
Achievements:

Parallelism achieved:

```
10%
                                        50%
                                                                               100%
2017-11-21 18:32:03 INFO: Time 0:00:00.348487 taken by RouterProvenanceGatherer
Getting profile data
                                        50%
                                                                               100%
2017-11-21 18:32:03 INFO: Time 0:00:00.004204 taken by ProfileDataGatherer
2017-11-21 18:32:03 INFO: 0, 0, 2 > 15
2017-11-21 18:32:03 INFO: 0, 0, 3 > 1
2017-11-21 18:32:03 INFO: 0, 0, 4 > 1
2017-11-21 18:32:03 INFO: 0, 0, 4 > 1
2017-11-21 18:32:03 INFO: 0, 0, 5 > 1
2017-11-21 18:32:03 INFO: 0, 0, 6 > 1
2017-11-21 18:32:03 INFO: 0, 0, 7 > 1
2017-11-21 18:32:03 INFO: 0, 0, 8 > 1
2017-11-21 18:32:03 INFO: 0, 0, 9 > 1
2017-11-21 18:32:03 INFO: 0, 0, 10 > 1
2017-11-21 18:32:03 INFO: 0, 0, 11 > 1
2017-11-21 18:32:03 INFO: 0, 0, 12 > 1
2017-11-21 18:32:03 INFO: 0, 0, 13 > 1
2017-11-21 18:32:03 INFO: 0, 0, 14 >
2017-11-21 18:32:03 INFO: 0, 0, 15 >
2017-11-21 18:32:03 INFO: 0, 0, 16 > 1
2017-11-21 18:32:03 INFO: 0, 0, 17 > 1
```

The leader (core 0,0,2) sends an integer with value 1 to all other cores at the same time, and all of those cores return the integer back to the leader simultaneously. Then, the leader takes all of those returned integers and adds them up before returning the result to the host.

Here, the communication structure looks as follows:



Considering problems of scalability

The next logical steps in building the database would be:

- 1. implementing the previously discussed histogram functioning
- 2. connecting several chips

In theory, implementing point 1 and 2 is easily doable with the current results. Unfortunately, there are several problems with scalability; for instance unique identifiers for every entry within SDRAM can only take up to 64Kbytes of TCM, which puts a limit on the number of entries that can be managed by the cores using this method.

Different issues have to be addressed in the foreseeable future, such as an alternative to using integer Ids, string size management and many more, including the problem of instability that comes with using UDP connections.

	Memory per processor				
	Bits	Bytes	KB	МВ	GB
SDRAM	8,589,934,592	8,388,608	8,192	8	0.00781
TCM	67,108,864	65,536	64	0.06250	0.00006
	Memory per chip (1	SDRAM, 16 proc	essors)		
SDRAM	137,438,953,472	134,217,728	131,072	128	0.12500
TCM	1,073,741,824	1,048,576	1,024	1	0.00098
	Memory per board (48 chips)			
SDRAM	6,597,069,766,656				6
TCM	51,539,607,552	50,331,648	49,152	48	0.04688
Stri	ng sizes and maximu	m amount of pos	sible entries in t	his format	
Number of ASCII	Bits	Bytes	Max num strings p		per SDRAM*
4	32	-		16,384	
8	64	. 8		8,192	
12	96	12		5,461	5,592,405
16	128	16		4,096	4,194,304
20	160	20		3,277	3,355,443
24	192	24		2,731	2,796,203
28	224	. 28		2,341	2,396,749
32	256	32		2,048	2,097,152
	Distribution of	string entries o	n SDRAM slices		
Number of ASCII	SDRAM/16	5 Columns		20 Columns	50 Columns
4	1,048,576				
8	524,288				
12	349,525		34,953		
16	262,144	52,429	26,214	13,107	5,243
20	209,715	41,943	20,972	10,486	4,194
24	174,763	34,953	17,476	8,738	3,495
28	149,797	29,959			2,996
32	131,072			6,554	
Р	ossible number of in	tegers in TCM		*Here, we use	50% of
Number of Columns	32 int per TCM		8 int per TCM	SDRAM for storing	
1	2,097,152			the data entries – part of	
2	1,048,576			SDRAM has	•
4	524,288			for other purp	
8	262,144			writing output, storing connection data, jobuf	
16	131,072				
32	65,536			1	- ~~~
64	32,768			1	
128	16,384			1	