

Table 1. SHA-256d

Chip	Algorithm	Package	Process, nm	Frequency, MHz	Voltage, V	Power, W	Hash Rate, GH/s	W/GH/s	Release date
ASC53E4390	SHA-256d	LBGA 81	28	650	0.72	30.83	68.20	0.452	2Q 2014
ASC54F5201	SHA-256d	LFBGA 144	28	900	0.65	24.12	96.11	0.251	1Q 2015
ASC55A9918	SHA-256d	TFBGA 324	16	1250	0.55	18.23	198.10	0.092	2Q 2016

- Optimized hashing cores in single chip (up to 192)
- Custom package with power bars for low voltage, high current feeding
- 2xUART communication interface
- Chain mode, max. 112 chips per chain
- Fully adjustable clock frequency
- Hardware addressing and software addressing
- High effective thermal specifications

Table 2. Scrypt

Chip	Algorithm	Package	Process, nm	Frequency, MHz	Voltage, V	Power, W	Hash Rate, MH/s	W/MH/s	Release date
ASC53E4592	Scrypt	LFBGA 112	28	1100	0.75	9.24	2.03	4.55	3Q 2014
ASC55A9009	Scrypt	TFBGA 361	16	1000	0.56	5.34	4.52	1.18	3Q 2016

- Optimized hashing cores in single chip (up to 128)
- Custom package with power bars for low voltage, high current feeding
- UART communication interface
- Chain mode, max. 72 chips per chain
- Fully adjustable clock frequency
- Hardware addressing and software addressing
- High effective thermal specifications