

Nios® II Release Notes

RN-1138 2017.05.08







Contents

Introduction	. 3
2 Nios II Release Notes for 17.0	4
B Nios II Release Notes for 16.1	6
Document Revision History for the Nios II Release Notes	7



1 Introduction

These release notes cover the new features and bug fixes for the 17.0 version and the last version of the Nios[®] II Embedded Design Suite (EDS), Nios II processor, and Embedded Intellectual Property (IP) cores.

For more information about the Nios II Processor, refer to the "Nios II Processor" web page.

For other important information, refer to:

- The "Knowledge Base" web page on the Intel FPGA website to search for errata based on the product version affected, as well as other criteria
- The "Nios II Embedded Design Suite Release Notes" web page to access past versions of the Nios II Embedded Design Suite (EDS), Nios II processor, and Embedded IP release notes

Related Links

- Archived Nios II Release Notes
- Intel FPGA Knowledge Base

For more information about errata and other potential issues, enter a keyword in the search field.

Nios II Processor and EDS New Features



2 Nios II Release Notes for 17.0

Nios II Processor IP Revisions

Enhancements:

Added support for the Nios II processor in Quartus® Prime Pro Edition, and Qsys Pro

Nios II Embedded Design Suite Revisions

Enhancements:

Nios II Software Build Tools (SBT)—Windows 10 support added in Quartus Prime Pro Edition



Embedded IP Revisions

New Features:

- Added new Streaming (Avalon-ST) Freeze Bridges for Partial Reconfiguration (PR) support
- New improved data performance Serial flash controller II and Generic Quad SPI controller II IPs
- Added Avalon-ST Freeze Bridges as PR solution IP
- All embedded IPs now support Cyclone[®] 10 device compilation

• Bug Fixes:

- I²C Slave to Avalon-MM Master—MM master write data corruption due to overrun of internal I2C slave RX shifting logic issue fixed
- Altera Avalon FIFO IP —Incorrect back pressure behavior during reset state and data loss when FIFO is almost full issue fixed
- EPCQ Controller—Incorrect back pressure behavior during reset state issue fixed

Enhancements:

- Generic QSPI Controller IP:
 - Modified to enable support for multiple instances in one Qsys design
 - · N25Q016 flash device now supported
- Serial Flash Controller IP—EPCS4 flash device now supported
- The following IP (from Standard version) are not present in the Pro version:
 - Altera Avalon New SDRAM Controller
 - Altera SDRAM Tristate Controller
 - Altera Avalon EPCS Flash Controller
 - Altera Avalon Compact Flash Controller
 - Altera Avalon Half Rate Bridge
 - Altera Avalon Pixel Converter
 - Altera Avalon Video Sync Generator
 - Altera Avalon LCD 16207
 - Altera Avalon SGDMA
 - Altera Avalon DMA
 - Altera Modular ADC
 - Altera SM Bus Controller



3 Nios II Release Notes for 16.1

Nios II Processor IP Revisions

• New Features:

- The Nios II Processor is supported as a pre-release (beta) version in Quartus Prime Pro Edition due to the changes required to support IP components in Qsys Pro.
- Nios II Classic is no longer supported in Quartus Prime Pro Edition.

Nios II Embedded Design Suite Revisions

New Features:

 The GCC (Nios II) toolchain has been upgraded to version 5.3 (other upgrades include gdb binutils v2.25, gdb v7.10, newlib v2.2).

Bug Fixes:

- The handling of the -mgpopt=option setting has been changed. It is now under the full control of the BSP editor and there is a flag for it in the public.mk file.
- nios2-app-compile no longer fails when -mgpopt is set to "global" and loglevel is set to "-1".

Embedded IP Revisions

New Features:

- $-\,$ A new IP core named Avalon $^{\rm \tiny IP}$ I $^{\rm \tiny C}$ Master has been added to the Qsys IP library.
- The 16550 UART IP has been enhanced to support a user defined TX FIFO level trigger.
- Freeze controller and bridges IPs have been added to the IP library.

Related Links

GCC, the GNU Compiler Collection website

For more information about the GCC releases, refer to the GCC, the GNU Compiler Collection website.



4 Document Revision History for the Nios II Release Notes

Date	Version	Changes
May 2017	2017.05.08	Documented the new features and bug fixes for the 17.0 release of the Nios II Processor, Nios II EDS, and Embedded IP cores.
November 2016	2016.11.07	Documented the new features and bug fixes for the 16.1 release of the Nios II Processor, Nios II EDS, and Embedded IP cores.
June 2016	2016.06.17	Initial release of the combined Nios II release notes.

Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.