White Paper

Optimize System Flexibility by Integrating Custom Microprocessors Into FPGAs

Introduction

Microprocessors and microcontrollers are some of the most ubiquitous components in digital electronic systems. However, despite the large number of vendors and offerings available for these components, embedded system designers are often challenged to find the exact processor or microcontroller that will fit their need. This difficulty arises mainly from the fact that, for many applications, no commercial off-the-shelf (COTS) product provides an optimal combination of performance, peripherals (both type and number), price, packaging, and persistence (life cycle). As a result, embedded systems designers often make compromises in their choices of these components.

Programmable-logic-based soft-core processors like the Altera® Nios® II embedded processor overcome the limitations of COTS processors and microcontrollers by enabling users to specify and only pay for the exact functionality they require. Nios II processor users often customize the type and number of peripherals, an easy modification with the available development tools. This paper documents two examples of first-time Nios II processor users who initially chose Altera's soft-core processors to overcome the inflexibility of COTS microprocessors and microcontrollers. Their success with these projects led them to adopt the Nios II processor as their processor of choice for similar projects going forward, shortening their time-to-market, increasing their product differentiation, and providing a number of other benefits.

Nios II Processor Overview

Altera's Nios II family of embedded processors features a general-purpose RISC CPU architecture designed to address a wide range of embedded applications. The Nios II processor family consists of three cores—fast (Nios II/f), economy (Nios II/e), and standard (Nios II/s) cores—each optimized for a specific price and performance range. All three cores share a common 32-bit instruction set architecture (ISA) and are 100 percent binary code-compatible. Designers can easily add Nios II processors to their systems by using the SOPC Builder tool included in Altera's tool for programmable logic design, the Quartus® II design software.

Nios II processors use an interface bus called the Avalon® switch fabric, which provides a set of pre-defined signal types with which a user can easily connect additional functions such as peripherals, memory interfaces, and other Nios II processors. With user input, Altera's SOPC Builder system development tool automatically generates the Avalon switch fabric logic. The Avalon switch fabric logic includes capabilities for data-path multiplexing, address decoding, wait-state generation, dynamic-bus sizing, interrupt-priority assigning, slave-side arbitration, multi-processor systems, and advanced switch fabric transfers.

Nios II processors and their associated Avalon switch fabric are implemented using the programmable logic resources in Altera field-programmable gate arrays (FPGAs), such as the Cyclone™ and Stratix® series devices. These FPGAs offer the logic and memory resources needed to create highly integrated, customized systems within a single device. The smallest of Altera's FPGAs can implement single-processor designs, and the largest can host hundreds of Nios II processors. Table 1 shows the logic available in Cyclone and Stratix series devices measured in logic elements (LEs), the basic building block of Altera FPGAs, and the logic required for each of the three Nios II cores.

Table 1. Nios II Processor Logic Utilization in Various Altera Device Families

Device Family	Available LEs Across Entire Family	Nios II/f Logic Utilization (LEs)	Nios II/s Logic Utilization (LEs)	Nios II/e Logic Utilization (LEs)
Stratix II	15,600 – 179,400	1,723	1,286	603
Stratix	10,570 – 79,040	1,808	1,170	529
Cyclone II	4,608 – 68,416	1,595	1,033	542
Cyclone	2,910 – 20,060	1,679	1,145	522

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Table 2 lists the DMIPS for a Nios II processor design implemented in Altera Stratix and Cyclone series devices with the following elements:

- Fast version of Nios II processor (Nios II/f processor, version 1.01)
- JTAG UART
- 64-Kbyte on-chip memory (Cyclone designs use 1 Mbyte of off-chip SDRAM)

Table 2. Nios II Processor Performance in Altera Device Families

Device Family	Device Speed Grade	Nios II/f Performance (DMIPS)	Nios II/s Performance (DMIPS)	Nios II/e Performance (DMIPS)
Stratix II	-3	225	133	31
Stratix	-5	157	99	23
Cyclone II	-6	105	57	22
Cyclone	-6	101	57	16

Notes:
(1) The fastest speed grade offered in each family. DMIPS reported were obtained using the Dhrystone benchmark version 2.1.

COTS Processor Inflexibility, Need for Greater Capability Force Change

When the right combination of peripherals, packaging, price, performance, and other features are not available in any single COTS processor, embedded designers often rely on additional external devices, including discrete and/or programmable logic, to implement the needed functionality. The Nios II processor enables embedded designers to avoid this situation by allowing the designer to easily integrate the processor and any desired peripherals into a single device. The experience of two companies, Toolrama, a developer of automotive diagnostic and performance equipment, and Host Automation, a developer of hardware for industrial programmable logic controllers (PLCs), demonstrates how Altera's Nios II processor delivers these and other significant advantages over COTS processors.

Toolrama's first experience with Altera's soft-core processor solution came during their project to upgrade their DiabloSport Predator, a high-performance tuning flash programmer. The Predator is used to advance a vehicle's timing and optimize the air/fuel ratio, as well as remap the transmission shift points in automatic transmissions. The goal of the upgrade was to add support for a larger LCD with more attractive graphics, provide TCP/IP connectivity, add a USB port, and change from SRAM to less expensive SDRAM. The prior Predator design used a 32-bit Motorola processor, but upgrading to a higher-end Motorola processor required to support these additional features would have resulted in non-competitive pricing for the Predator.

In Host Automation's case, the project that led them to choose the Altera solution was a 100Base-T Ethernet controller for a PLC. This was a natural extension of their prior products, which included one of the first 10Base-T Ethernet controller interfaces for a PLC and also fiber optic-based Ethernet PLC communications modules. Host Automation needed a custom interface from the processor to a proprietary PLC backplane (a common feature of a PLC), and a small package to occupy as little board space as possible on the 3.2" x 2.5" printed circuit board. After spending two years researching and developing prototypes that used ARM7-based processors and a TI processor, Host Automation concluded that there was no COTS processor that would meet their requirements, including their performance, package, life cycle, and cost targets.

Altera Cyclone Series FPGA + Nios Processor = Low-Cost, Flexible Processor

Both Toolrama and Host Automation evaluated and adopted the combination of Altera's low-cost Cyclone series of FPGAs and the first-generation Nios embedded processor for their respective projects. Toolrama developed a dedicated, custom LCD peripheral for their Cyclone design, which provided 90-frames-per-second support while making very small demands on the processor, enabling them to integrate all of their needed functionality into a single device that met their cost needs.

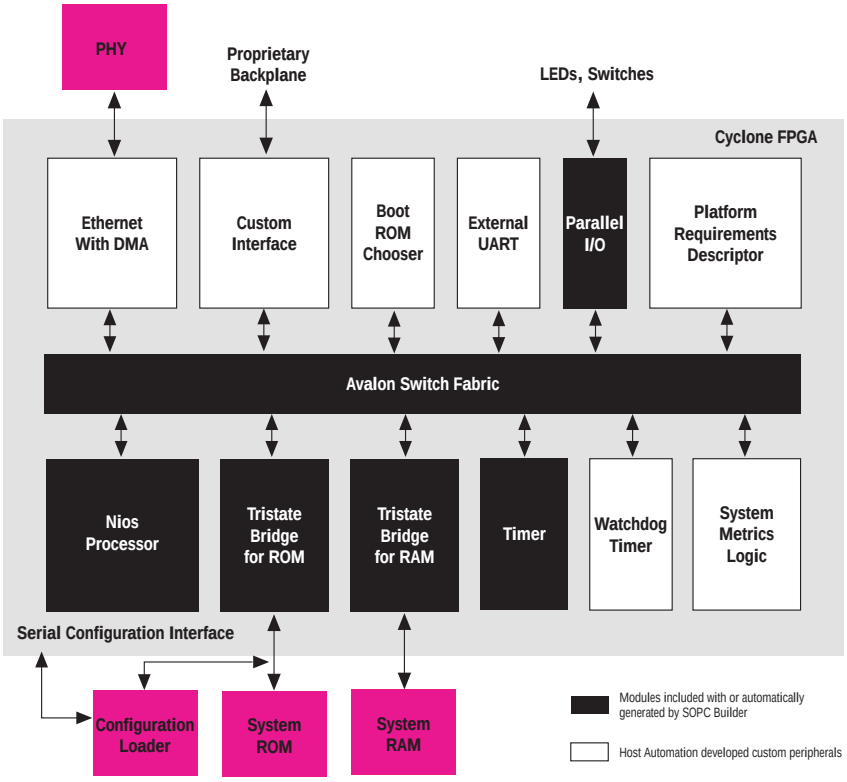
Host Automation also developed a custom peripheral to interface with the PLC backplane, as well as additional customizations as shown in Table 3.

Table 3. Nios Processor System Customizations Developed by Host Automation

Customization	Benefit
"Lightweight" Ethernet MAC With DMA	Reduces device utilization by providing only the needed functionality
Custom Interface to Proprietary Backplane	Integrated communication with PLC
Boot ROM Chooser	Supports in-field upgrades by determining choice of FPGA configuration
Register-Programmable UART Supports Variable Bit Lengths & Parities	Communication with industrial devices
Platform Requirements Descriptor	Ensures in-field upgrades are compatible with the board by checking system ID
System Metrics Logic	Records reliability data
Watchdog Timer	Failsafe mechanism for catastrophic errors; shuts down equipment connected to controller if software or hardware fails

Figure 1 shows Host Automation's complete processor system implemented in the Altera Cyclone FPGA, as well as the FPGA configuration loader, which is implemented in an Altera MAX® 3000 CPLD. The white blocks show the custom peripherals that Host Automation developed, and the black blocks show the modules included with or automatically generated by SOPC Builder. The remaining blocks are external to the Cyclone FPGA design.

Figure 1. Host Automation Processor System Block Diagram



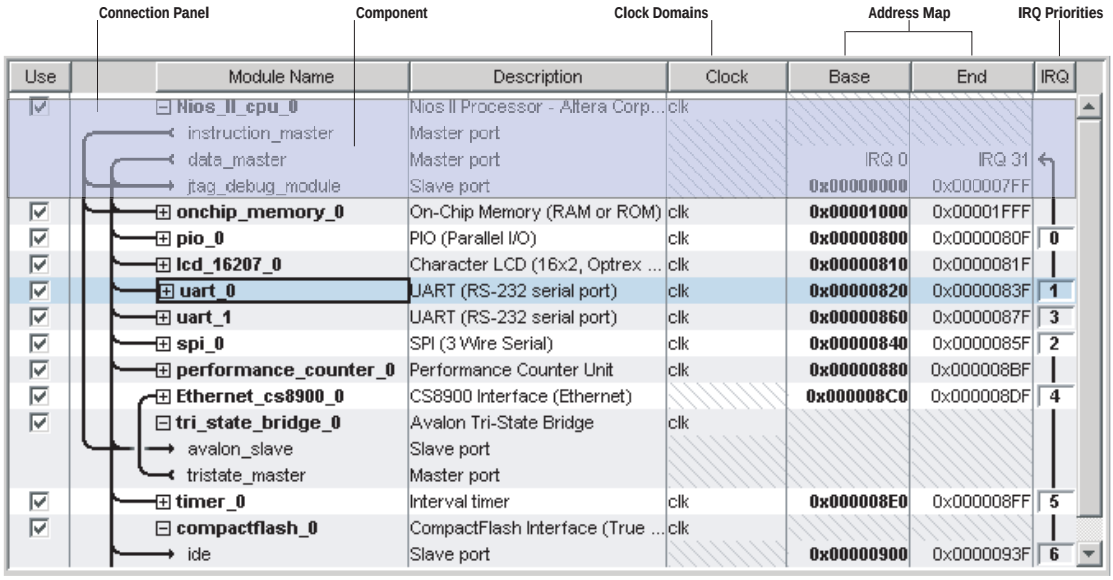
Powerful, Easy-to-Use Development Tools Shorten Time-to-Market

Despite being first-time Nios processor users, Toolrama was able to complete an assembled prototype of their new product within two months of starting their upgrade project. Only one week later, it was up and working with application software loaded. It cost only US$2,000 and 100 hours of engineering time to produce this functioning

prototype. Similarly, Host Automation completed their first working prototypes of their T1H-EBC100 Ethernet base controller in three months. Both companies credit Altera's SOPC Builder tool with accelerating their development process and shortening the time it would normally take to come up to speed using a new processor.

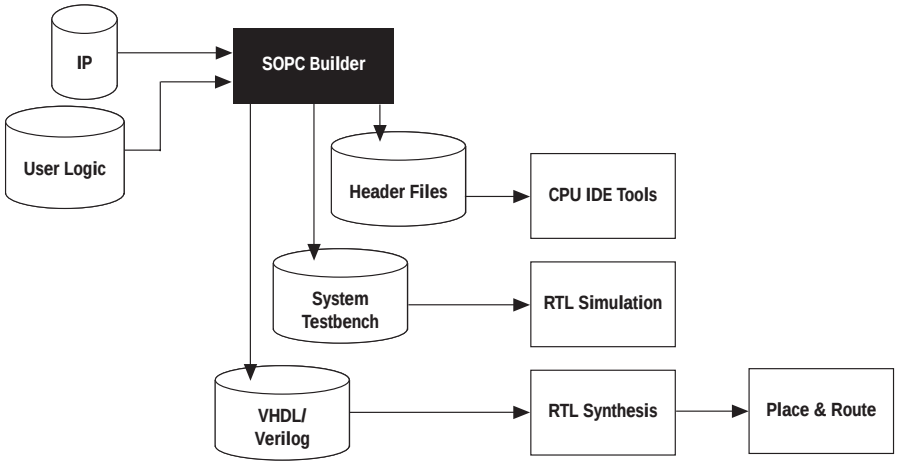
The SOPC Builder tool enables users to quickly configure their Nios II processor system with a GUI that guides them through the choice of processor type, instruction and data cache sizes, and any additional peripherals or interfaces needed for the overall system. The SOPC Builder presents designers with a library of available compatible functions called components, which can be masters or slaves. As components are selected, they are added to a connection panel in the GUI. For each master component in the system, the table gets one vertical line, which can be connected to one or more available slave components. Slave components can be dedicated to a particular master or shared between multiple master components. Users also specify clock domains, address map, and IRQ priorities, as shown in the SOPC Builder tool screen shot in Figure 2.

Figure 2. SOPC Builder Tool



SOPC Builder generates a HDL-based file that includes the Nios II processor system and corresponding interconnect based on the selected components and the selection of specific masters connected to specific slaves. This HDL file is used by Altera's Quartus II design software to synthesize, place, and route the design into an Altera FPGA. SOPC Builder also outputs a system test bench for verification and a set of C/C++ header files with memory map information so the software engineers can write code to work with the generated system. These SOPC Builder tool inputs and outputs are shown in Figure 3.

Figure 3. SOPC Builder Inputs & Outputs



Altera offers an extensive list of peripherals for building Nios II processor-based systems, including timers, memory controllers, DMA controllers, UARTs, parallel I/O, and a variety of interfaces. SOPC Builder makes design reuse easy by enabling users to simply add their intellectual property (IP) to SOPC Builder so it can be integrated into future projects. Host Automation has developed over 20 entries in SOPC Builder, and this design reuse helped shorten their product development cycle for subsequent products, including the H2-EBC100 Ethernet base controller module and H2-ECOM100 Ethernet communication module, to a third of what it had originally been.

Nios II Processors Deliver Possibilities Not Available With COTS Processors

Host Automation took advantage of the reconfigurability of the Cyclone FPGA to add support for in-field upgrades of their products. With this capability, they can change the functionality of their product while it is deployed in the field simply by updating the FPGA configuration file in the main system Flash ROM. Host Automation can also add new hardware-based functionality to these products or quickly develop new variations on these products based on customer demand, an option not available to them had they used COTS processors. Possible updates/variations include:

- Updating the Ethernet controller and OS to support upcoming protocols based on TCP/IP
- Adding digital filtering to clean up noisy inputs
- Accelerating the Nios processor to shorten turn-around time for PLC messages or I/O cycles

Host Automation also leveraged the flexibility of their Cyclone FPGA-Nios processor platform in other PLC products. In an upcoming product, they use a custom instruction in a Nios processor to address system bottlenecks by implementing custom algorithms in hardware versus software. In prior versions of this product based on a COTS processor, the highest performance they could achieve for a critical, complex counter pulse-output function was 35 KHz, even when using assembly language code to get the best execution speed. Using a custom instruction with a Nios processor in a Cyclone FPGA, they achieved over 1-MHz operation for the same component cost as their COTS processor-based implementation. By their estimation, using a higher performance COTS processor to achieve the 1-MHz operation would have increased their component costs by 10 percent, without providing any of the flexibility benefits of the Altera solution. In Host Automation's view, this performance boost is a key product differentiator that would not have been possible with COTS processors.

Toolrama has also leveraged the Cyclone FPGA-Nios processor platform they created for their DiabloSport Predator to develop custom processor systems for upcoming products. Table 4 shows some of the customizations Toolrama is

developing that are difficult or in some cases impossible to achieve with COTS processors without additional custom devices.

Table 4. Nios II Processor System Customizations Developed by Toolrama

Customization	Benefit
6-bit I/O Port With 6 Separate Interrupts	Enables simultaneous independent monitoring of each keypad button
Multiple LCD Controllers	Offloads display control from processor
Engine Control Unit (ECU) Programming Module	Enables programming of automotive ECU EEPROMs
Multiple Independent Serial Peripheral Interface (SPI) Ports (as Many as 11 in a Single Product)	Reduces processor overhead for reading multiple SPI ports simultaneously; not often available on low-cost processors
Modified SPI Port for SD Card Interface	Generates interrupts based on card insertion and write protection
Multiple, Independent Hardware-Controlled UARTs With Flexible Baud Rates	Allows communication with various ECUs with low processor overhead
ECU Sensor Modification Peripheral	Enables complex sensor reading and translation scheme, uses two SPI ports and a look-up table (LUT) to generate modified sensor value for ECU while making original sensor data available to processor with no processor intervention
Enhanced Controller Area Network (CAN) Bus Interfaces	Enables implementation of exact number of CAN bus interfaces required, also addition of features helpful for communicating with embedded systems in automobiles

Reduce Inventory & Manufacturing Costs With Obsolescence-Proof Designs

Nios II processor users can reduce the number of unique parts in their products and inventory by achieving higher integration and using the same hardware platform for some or all of their designs. This reduced component count eases the collective purchasing effort, simplifies manufacturing, and increases product reliability, saving overall costs. Altera's FPGA families also offer vertical migration, which enables users to choose different logic densities within the same package. This option allows Nios II processor users to upgrade their products with greater capability in higher density FPGAs without forcing a board redesigning.

Also, issues involving processor or microcontroller obsolescence are avoided. Nios II processor users can migrate their designs to a new Altera FPGA, use the same IP, and still offer the same product for those who demand continuity in a fast-changing world. This is especially important in Host Automation's market since it is expected that their products be offered for at least 15 years. IP lasts forever and is replaced only when a market need exists for something better.

Ease RoHS Transition With Altera Lead-Free Products

Altera maintains one of the most extensive lead-free product offerings in the industry, with over 1200 products in lead-free packages. As a preeminent supplier of environmentally friendly programmable logic solutions, Altera has shipped over 25 million lead-free products since 2002. Altera’s lead-free devices comply with the maximum concentration restrictions, as required in the EU Directive on the Restriction of Hazardous Substances (“RoHS Directive”) No.2002/95 with respect to lead (Pb), mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE). Help ease your RoHS transition by integrating non-compliant ASSPs with Altera’s PLDs.

Conclusion

After developing successful products based on the first-generation Nios processor, Host Automation and Toolrama adopted the Nios II processor as their processor of choice in its performance class. Host Automation's H2-EBC100 and H2-ECOM100 products were recognized with Control Engineering's Editor's Choice Awards. Both companies discovered that the Nios II processor delivers flexibility to embedded designers that is unavailable from COTS processors, and they leveraged this flexibility to deliver compelling product differentiation. In the process, they gained a powerful means for processor system design that will continue to provide significant benefits in their product development going forward.

Resources

For additional information, refer to the following resources on the Altera website.

- Toolrama's DiabloSport Predator in the Altera Customer Showcase:
  www.altera.com/corporate/cust_successes/customer_showcase/csh-toolrama.html
- Host Automation's H2-EBC100 Ethernet Interface Module in the Altera Customer Showcase:
  www.altera.com/corporate/cust_successes/customer_showcase/csh-host-engineering.html
- Host Automation's H2-ECOM100 Ethernet Interface Module in the Altera Customer Showcase:
  www.altera.com/corporate/cust_successes/customer_showcase/csh-host-engineering2.html
- More System Integration Solutions:
  www.altera.com/technology/integration/int-index.html
- More Information on the Nios II Processor:
  www.altera.com/products/ip/processors/nios2/ni2-index.html
- Nios II Processor Online Demos:
  www.altera.com/education/demonstrations/online/embedded-processor/onl-nios2.html
- More Information on SOPC Builder:
  www.altera.com/products/software/products/sopc/sop-index.html

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