White Paper

Creating Low-Cost Intelligent Display Modules With an FPGA and Embedded Processor

Introduction

LCDs are fast becoming a standard part of the automotive interior. As demand for LCD technology increases, so do methodologies for controlling and creating the displayed graphical content. Traditionally, character-based LCDs and vacuum florescent (VF) displays have been used for low-cost automotive infotainment applications, but low-cost color thin film transistors (TFTs) quickly are becoming a bright alternative.

Incorporating a color TFT within existing low-cost application architectures can, however, be challenging. Most low-cost platforms lack sufficient processing bandwidth or, specifically, a processor with an LCD controller to control and drive a color TFT LCD. Additionally, most existing architectures do not contain enough dynamic and non-volatile memory to cover the graphical content required by the LCD. Compounding the design problem further are the ineffective design processes for creating and managing the graphical content or graphical user interfaces (GUIs) now possible with a color TFT LCD. In general, without proper design resources, it is difficult to physically contain the supporting hardware for the LED backlight driver, touch-panel control, and sheer number of I/Os required to control a TFT.

There is now a solution to these challenges, available in the form of a modular expansion platform called the Thomas II board (Figure 1) that includes a low-cost Altera® Cyclone® III FPGA and a Nios® II embedded processor. Using this platform, automotive electronics designers can easily add color TFTs to their existing system architectures and create low-cost intelligent display modules.

Figure 1. The Thomas II Demo Platform

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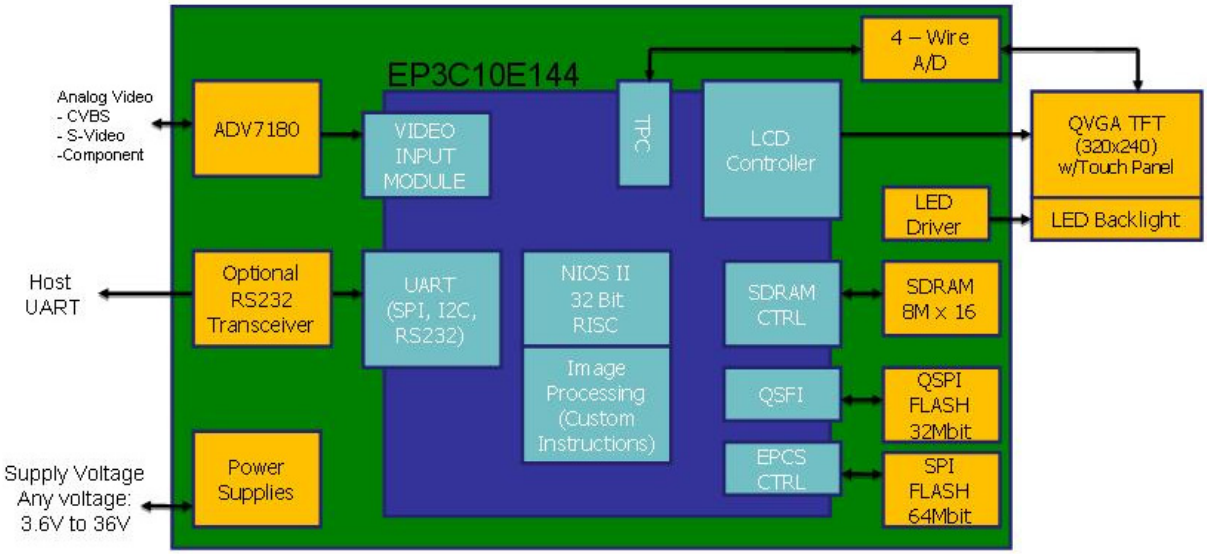
Inside the Modular Expansion Concept

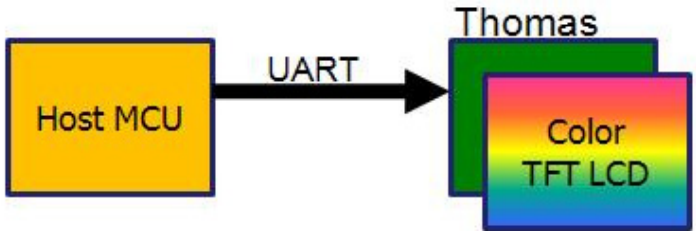
The modular expansion design concept is based on the Thomas II board, which was developed jointly by Momiji Design LLC and Altera Corporation. The design is built around a low-cost Cyclone III FPGA (EP3C10 or EP3C5) in a low-pincount E144 QFP package that enables the layout to be contained easily within a four-layer PCB. In applications, the Thomas II design (shown in Figure 2) can be used as a standalone module complete with power supplies and support peripherals, or integrated into an existing design architecture.

Figure 2. Thomas II Design Block Diagram



A Nios II embedded processor is at the core of the architecture, and is used for both system control and graphic creation. The embedded processor enables the system to operate as a standalone or as a coprocessor to an existing microcontroller unit (MCU), which allows the Thomas II design to function as a modular extension for low-cost infotainment designs. Through a simple UART, the FPGA becomes the graphic display controller for the system. It manages and controls all the graphic content creation and manipulation, thereby off-loading those tasks from the host MCU. The UART block within the FPGA design can easily be replaced or modified with any serial or parallel communications interface, even those standards which are custom or proprietary. For example, a communication protocol typically used to address a VF or character-based LCD could easily be reused to control a TFT based on the Thomas II concept. The compelling attribute is that the host architecture and system design can basically remain the same, as shown in Figure 3.

Figure 3. Design Reuse

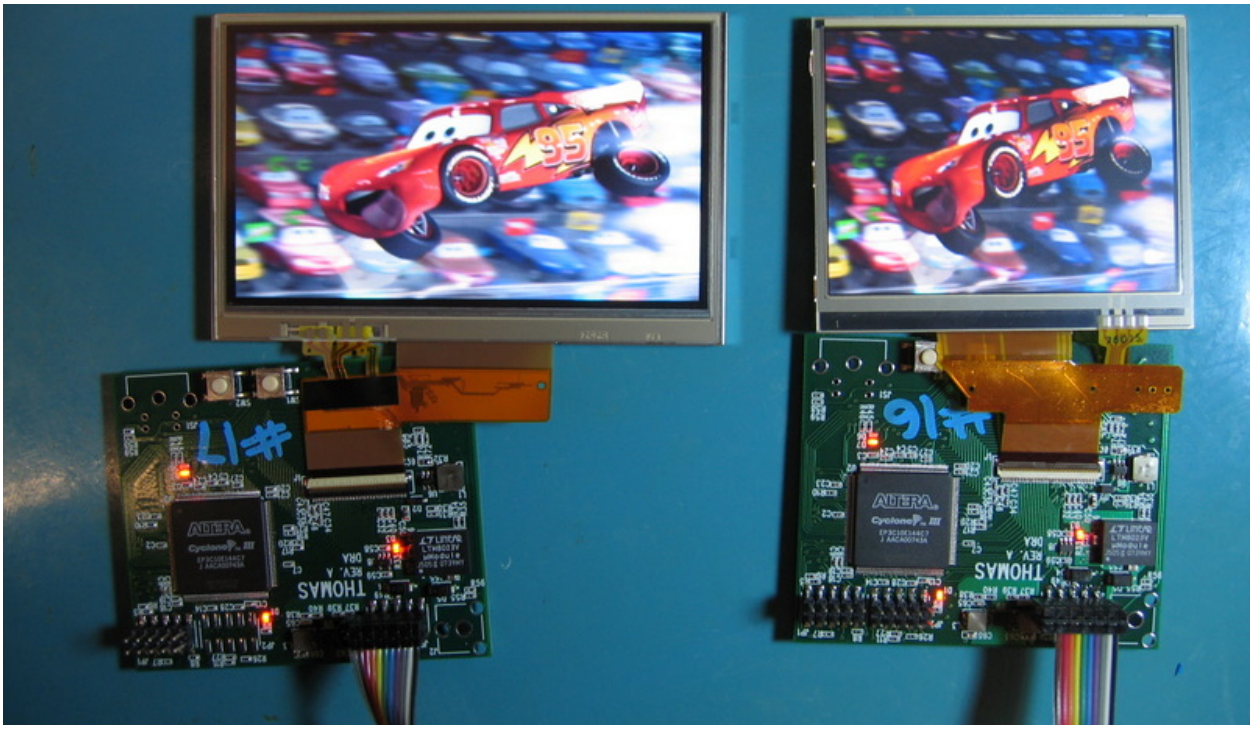


Single Hardware Design for Multiple Products

Eliminating or minimizing system changes translates to both hardware and software design savings. With the Thomas II concept, a designer can use the same core hardware design for multiple products. The GUI can be updated or changed based upon the product requirements, without a need to modify or update the core system software. In addition, the resolution of the LCD and underlying graphics can scale based on application requirements.

The LCD controller design within the FPGA easily adapts to a variety of standard and custom LCD resolutions (see Figure 4). It also has the ability to address dual-view, multi-view, and other nonstandard LCD formats. The intrinsic benefit of the LCD controller within the FPGA is that it can be customized or adapted to create any data or timing format required by the LCD.

Figure 4. Thomas II Board Applied to WQVGA and QVGA LCDs



Note: Images courtesy of and copyright © Disney/Pixar.

The LCD controller module is a multi-layer LCD controller, containing two 16-bit color image layers and one alpha layer. Each layer is formed and controlled by a separate DMA master. This enables efficient partitioning of the external DRAM-based frame buffer. In essence, each DMA master may read from the frame buffer whenever it requires data. This enables the LCD controller module to read any frame resolution or image size stored in the external memory. As each layer master reads from memory, the LCD controller module combines (or flattens) the layers into one combined frame that is then output to the LCD. As the LCD controller module combines the layers, each layer has the option to be combined with an alpha layer or "transparency layer." The alpha layer enables overlay graphics to have transparency or the appearance of being blended with the layer content below. Additionally, each layer may be turned completely on or off, enabling layers to be activated or deactivated as desired. An example of this concept is overlay graphics used for menus applied above a video capture layer.

Touch-Panel Controller Simplifies User Interaction

To enable interaction with a user, the Thomas II design also employs a touch-panel controller within the FPGA. The design supports a four-wire resistive touch-panel controller that can control any standard four-wire touch panel. The Nios II embedded processor manages and acquires user event data from the touch panel and accordingly draws or executes commands based upon the GUI and overall system design. To facilitate and accelerate GUI creation, the embedded processor easily integrates into Altia's graphic development tool chain.

Altia's graphic development tools enable artists, interaction designers, engineers, and programmers to quickly build concept prototypes, models, and deployable code, without risk of misinterpreting the overall graphic design or graphical interaction. From concept to code, these tools can reduce the overall development cycle drastically while

preserving the artistic integrity of the graphic design. Altia also offers a plug-in to Adobe Photoshop called PhotoProto, which enables graphic designers to easily export their visual composition to Altia Design, shown in Figure 5. Within Altia Design, developers can add functionality and behavior to the graphic design. The prototype model or concept developed in Altia Design then generates, via a tool called Deep Screen, everything about the graphics and behavioral logic to a linkable library for the Nios II embedded processor. The Nios II processor then executes the Altia model, and manages the physical interaction of the user with the model.

Figure 5. Altia Design, PhotoProto, and Deep Screen Tools

Video Capture and Image Processing

One of the additional features realized within the FPGA-based design shown in Figure 2 is video capture. The video input module, compatible with the ITU-R BT.656 digital video standard, performs the following operations: color space conversion (CSC), clipping, de-interlacing, scaling, and an RGB 565 pack. Each operation is performed sequentially and is parameterized by registers controlled by the Nios II embedded processor. Optionally, the video inputs may be clipped and scaled (up or down) depending on the desired output format. The registers enable the system to be customized for various display resolutions and input video formats such as NTSC, PAL, and SECAM. Video data from the module is transferred via a 32-bit DMA to an external SDRAM frame buffer. The pixel data is packed to a 565 format to enable two pixels to be transferred as one word during the DMA. This greatly increases video bandwidth and overall efficiency of the memory access.

The Thomas II design uses the standard SDRAM memory controller available within Altera's Quartus® II design software. SDRAM provides sufficient video bandwidth and overall memory bandwidth as a lower priced alternative to DDR (for the required density). Additionally, utilizing SDRAM minimizes the complexity of the board layout, which in turn reduces the overall system cost. Functionally, the DRAM provides a shared memory space for the video and image frame buffers as well as for the program memory of the Nios II embedded processor. The Avalon® system interconnect fabric connects the SDRAM controller to the Nios II processor and other system modules, and provides arbitration for memory access and memory management.

One compelling feature of the Cyclone III FPGA is the possibility for future migration to other memory topologies and technologies. If required, the design can be modified easily to incorporate a DDR or DDR2 memory controller, or the SDRAM interface can be widened to accommodate a 32-bit SDRAM device. This is enabled by the flexible I/O ring of the FPGA and the variety of memory controllers within the SOPC Builder tool.

The Thomas II design also enables video and image processing. With the source video buffered and stored in SDRAM, image processing algorithms are performed by the Nios II processor. The advantage and flexibility of the Cyclone III FPGA, however, is that the algorithms can be executed as software, hardware, or as a mixture of both.

Altera's Nios II C-to-Hardware (C2H) acceleration compiler can be used to profile the software algorithm and then transfer functions into hardware accelerated custom instructions. The Nios II processor then can execute the custom instructions without iterative processing cycles. Building upon the custom instructions, designers can take advantage of the parallel processing nature of the Cyclone III FPGA fabric. The inherent digital signal processing (DSP) functionality can be used to perform a variety of image processing algorithms, one example being fisheye correction.

Conclusion

By incorporating a color TFT to a low-cost system architecture, automotive electronics designers can bring to market an array of visually and functionally compelling applications. The Thomas II board, developed with a modular expansion approach and based on a low-cost, low-pincount FPGA, provides a platform to accomplish this. The accompanying design software and tools support a fast development process, and they also help preserve the integrity of the GUI design. In addition, a single FPGA integrates a variety of functions, without requiring alteration to the host architecture and system design. The reprogrammable technology also brings flexibility to migrate the design to a larger-density FPGA if needed.

Further Resources

Altera

- Thomas II board design software and tools: www.momijidesign.com/thomas.html
- Nios II C-to-Hardware acceleration compiler: www.altera.com/products/ip/processors/nios2/tools/c2h/ni2-c2h.html
- *Implementing a Flexible CPLD-Only Digital Dashboard for Automobiles:* www.altera.com/literature/wp/wp-01072-implementing-flexible-cpld-only-digital-dashboard-automobiles.pdf
- *A Flexible Architecture for Fisheye Correction in Automotive Rear-View Cameras:* www.altera.com/literature/wp/wp-01073-flexible-architecture-fisheye-correction-automotive-rear-view-cameras.pdf
- *Applying Graphics to FPGA-Based Solutions*: www.altera.com/literature/wp/wp-01075-applying-graphics-to-fpga-based-solutions.pdf
- *Using LEDs as Light-Level Sensors and Emitters*: www.altera.com/literature/wp/wp-01076-leds-as-light-level-sensors-and-emitters.pdf

Altia

- Altia graphic development tool chain: www.altia.com/products.php
- Altia Design: www.altia.com/products_design.php
- Altia PhotoProto: www.altia.com/products_photoproto.php
- Altia Deep Screen: www.altia.com/products_ds.php

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