Proiect C.I.D.

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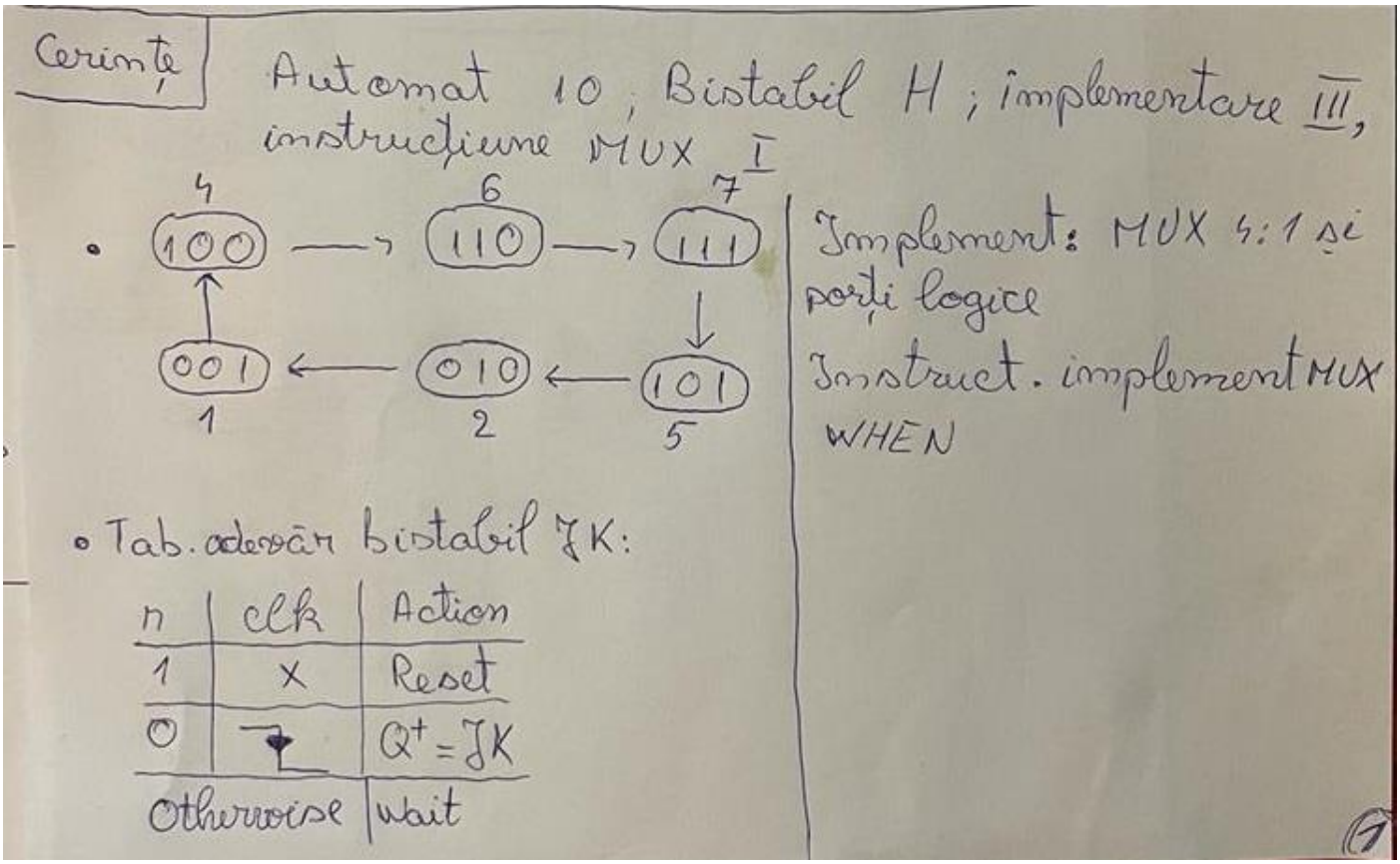
Grupa 2126

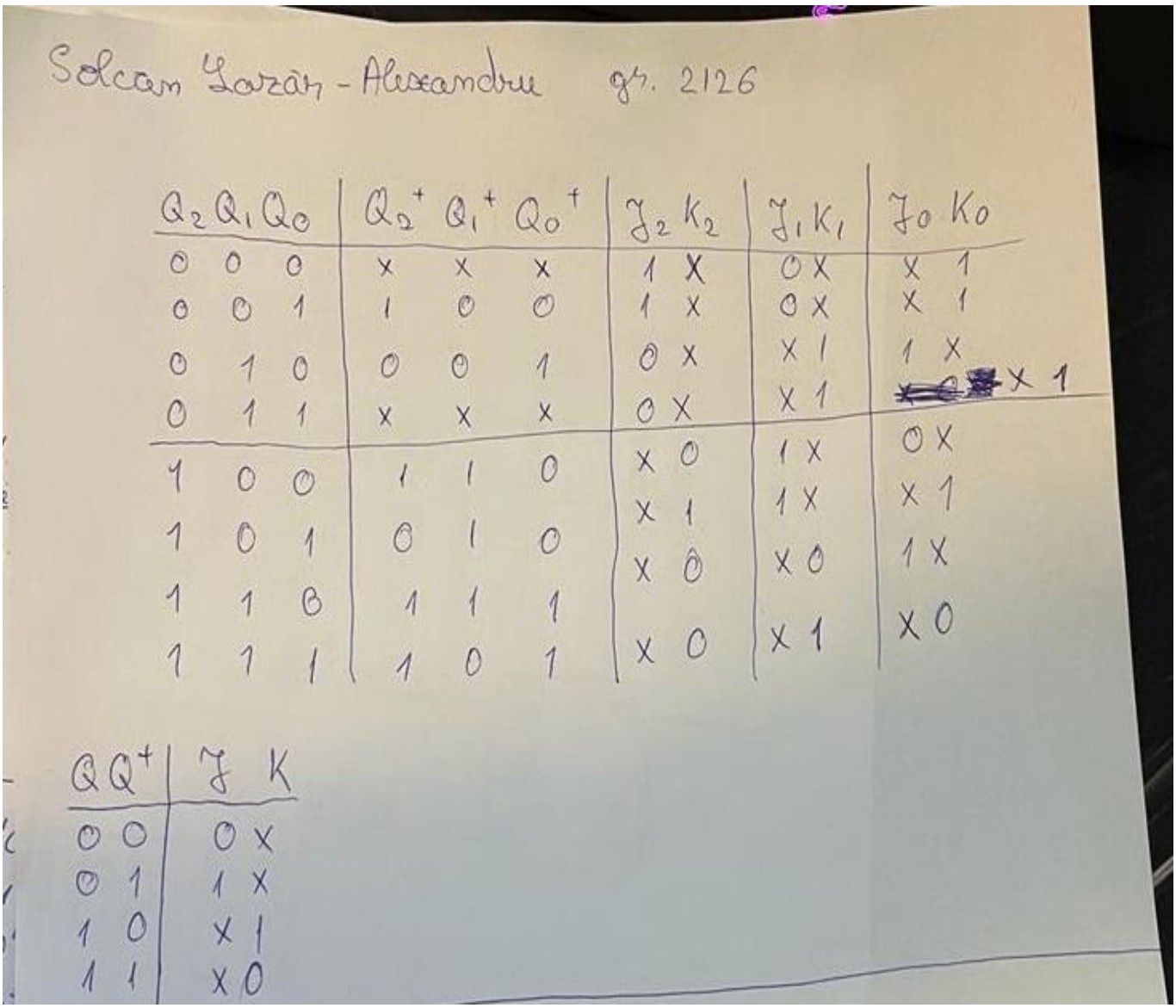
Proiect C.I.D

Cuprins:

1. Rezolvarea temei de proiect pe hârtie
   a) Cerințe



b) Rezolvarea tabelului de adevăr folosind bistabile JK

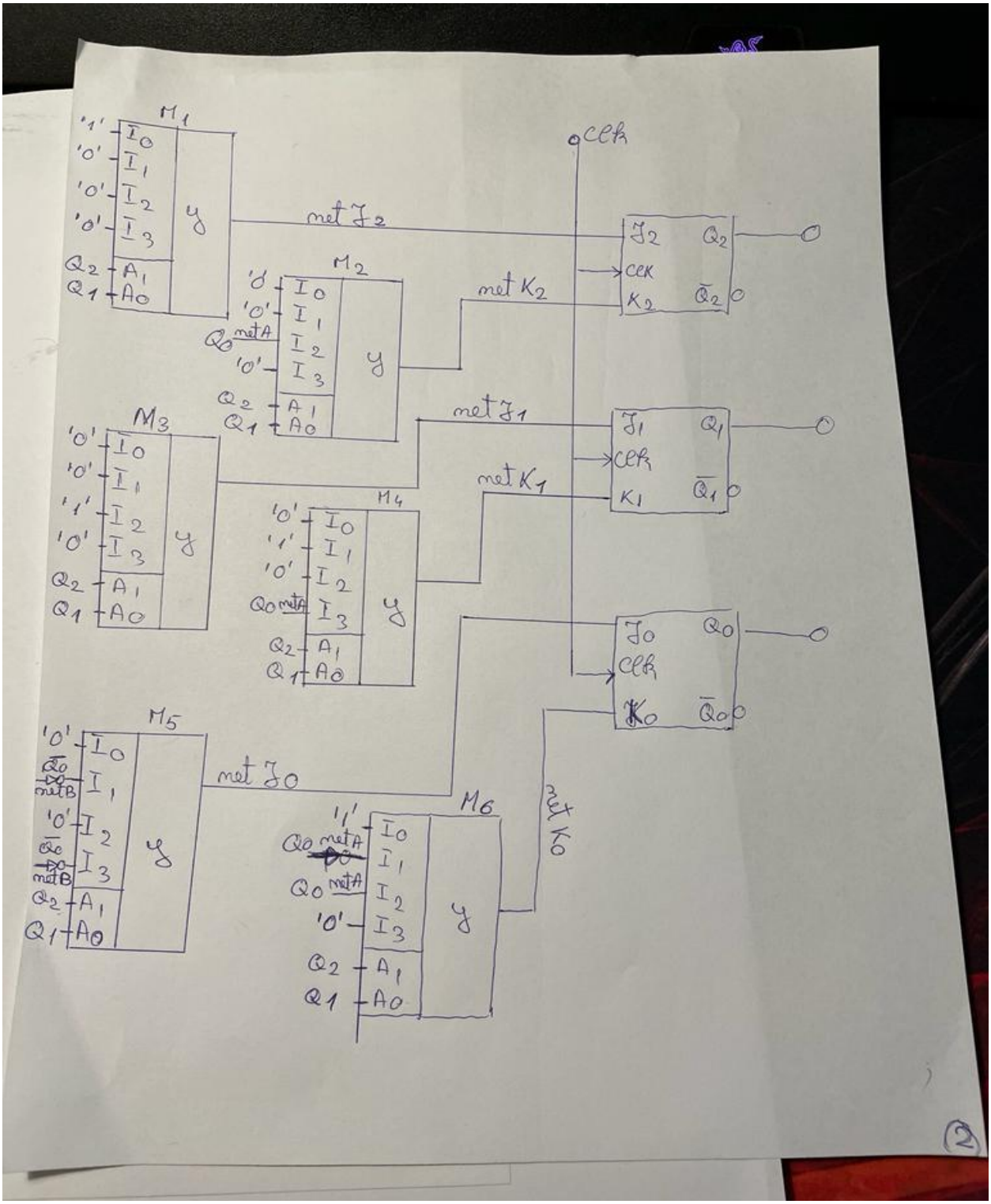


Solcan Sorân - Alexandru gr. 2126

Q_2 Q_1 Q_0	Q_2^+ Q_1^+ Q_0^+	J_2 K_2	J_1 K_1	J_0 K_0
0 0 0	x x x	1 X	0 X	X 1
0 0 1	1 0 0	1 X	0 X	X 1
0 1 0	0 0 1	0 X	X 1	1 X
0 1 1	x x x	0 X	X 1	X 1
1 0 0	1 1 0	X 0	1 X	0 X
1 0 1	0 1 0	X 1	1 X	X 1
1 1 0	1 1 1	X 0	X 0	1 X
1 1 1	1 0 1	X 0	X 1	X 0

QQ^+	J K
0 0	0 X
0 1	1 X
1 0	X 1
1 1	X 0

c) Proiectarea designului automatului



2. Circuitele combinaționale

a) Sursa de design a Multiplexorului 4:1

Project Summary | bistabil.vhd | mux4.vhd | inv.vhd | automat.vhd | neinversor.vhd | sursa_sim_automat.vhd | sursa_sim_bistabil.vhd

C:/Users/hop/poatededataastamerge/poatededataastamerge.srcs/sources_1/new/mux4.vhd

```
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity mux4 is
35      Port ( i0 : in STD_LOGIC;
36             i1 : in STD_LOGIC;
37             i2 : in STD_LOGIC;
38             i3 : in STD_LOGIC;
39             a1 : in STD_LOGIC;
40             a0 : in STD_LOGIC;
41             y : out STD_LOGIC);
42  end mux4;
43
44  architecture Behavioral of mux4 is
45
46  signal adr : std_logic_vector (1 downto 0);
47
48  begin
49
50  adr <= a1 & a0;
51
52     with adr select
53       y <= i0 when "00",
54            i1 when "01",
55            i2 when "10",
56            i3 when "11",
57            i0 when others;
58
59  end Behavioral;
60
```

b) Sursa de simulare a MULTIPLEXORULUI 4:1

Proiect C.I.D

Project Summary | bistabil.vhd | mux4.vhd | inv.vhd | automat.vhd | neinversor.vhd

C:/Users/hop/poatededataastamerge/poatededataastamerge.srcs/sim_1/new/sursa_sim_mux4.vhd

```
34  entity sursa_sim_mux4 is
35  --  Port ( );
36  end sursa_sim_mux4;
37
38  architecture Behavioral of sursa_sim_mux4 is
39
40  component  mux4 is
41      Port ( i0 : in STD_LOGIC;
42             i1 : in STD_LOGIC;
43             i2 : in STD_LOGIC;
44             i3 : in STD_LOGIC;
45             a1 : in STD_LOGIC;
46             a0 : in STD_LOGIC;
47             y : out STD_LOGIC);
48  end component mux4;
49
50  signal i0: std_logic :='0';
51  signal i1: std_logic :='0';
52  signal i2: std_logic :='0';
53  signal i3: std_logic :='0';
54  signal a1: std_logic :='0';
55  signal a0: std_logic := '0';
56
57  signal y: std_logic;
58
59
60  begin
61
62  ut: mux4 port map(i0 => i0,
63                    i1 => i1,
64                    i2 => i2,
65                    i3 => i3,
66                    a1 => a1,
67                    a0 => a0,
68                    y => y);
69  process
70  begin
71
72  i0 <= '0';
73  i1 <= '0';
74  i2 <= '0';
75  i3 <= '0';
76  a1 <='0';
77  a0 <= '0';
```

Source File P

```
78
79    wait for 10 ns;
80
81    i0 <= '1';
82    i1 <= '1';
83    i2 <= '1';
84    i3 <= '1';
85    a1 <= '1';
86    a0 <= '1';
87
88    wait for 10 ns;
89
90    i0 <= '1';
91    i1 <= '0';
92    i2 <= '0';
93    i3 <= '1';
94    a1 <= '1';
95    a0 <='1';
96
97    wait for 10 ns;
98
99    i0 <= '1';
100   i1 <= '0';
101   i2 <= '1';
102   i3 <= '1';
103   a1 <='1';
104   a0 <= '1';
105
106   wait for 10 ns;
107
108   i0 <= '0';
109   i1 <= '1';
110   i2 <= '0';
111   i3 <= '0';
112   a1 <= '0';
113   a0 <= '1';
114   wait for 10 ns;
115
116   end process;
117   end Behavioral;
118
```

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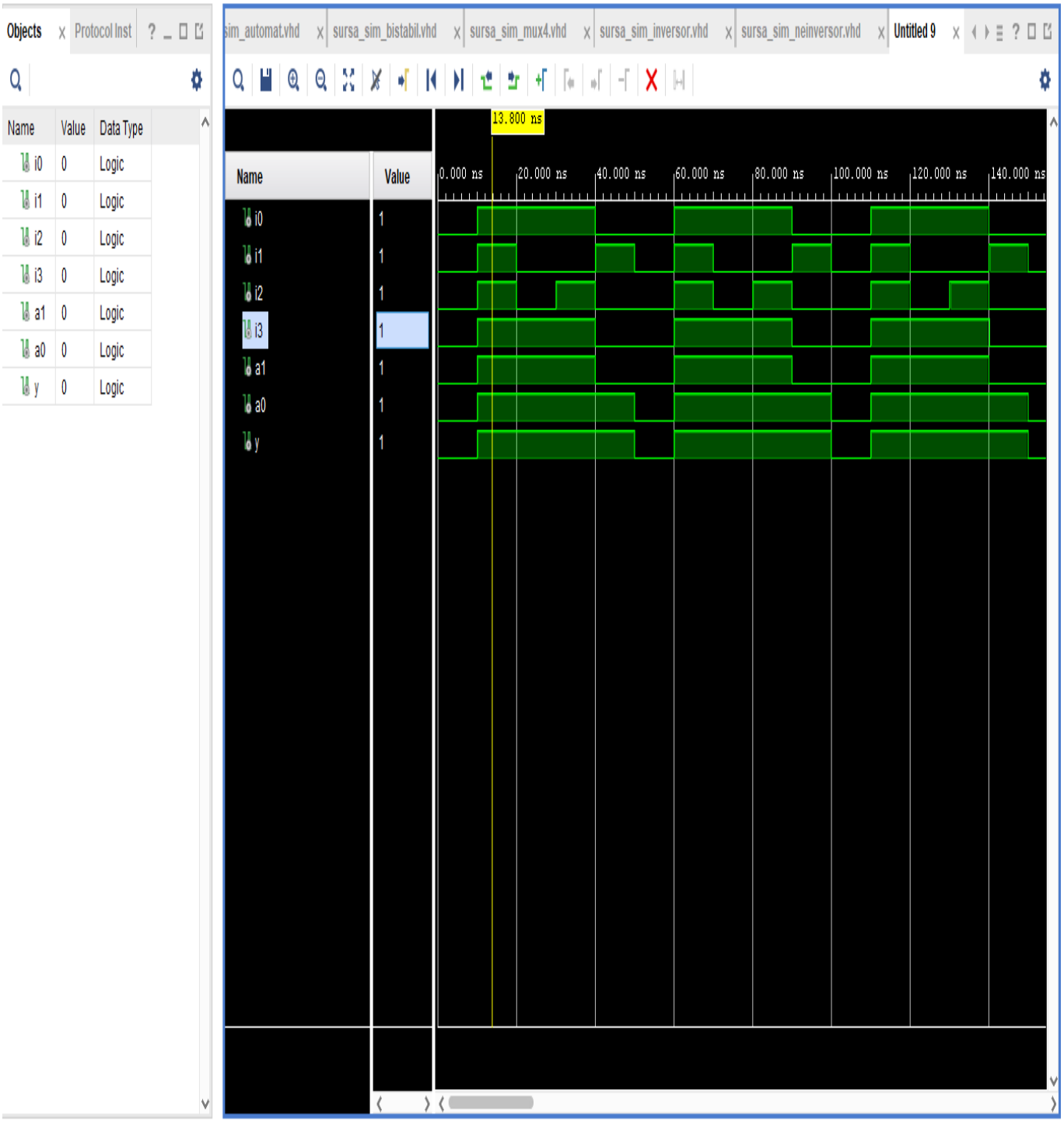
c) Simularea MULTIPLEXORULUI 4:1



Proiect C.I.D

d) Sursa de design a inversorului

Source File Properties

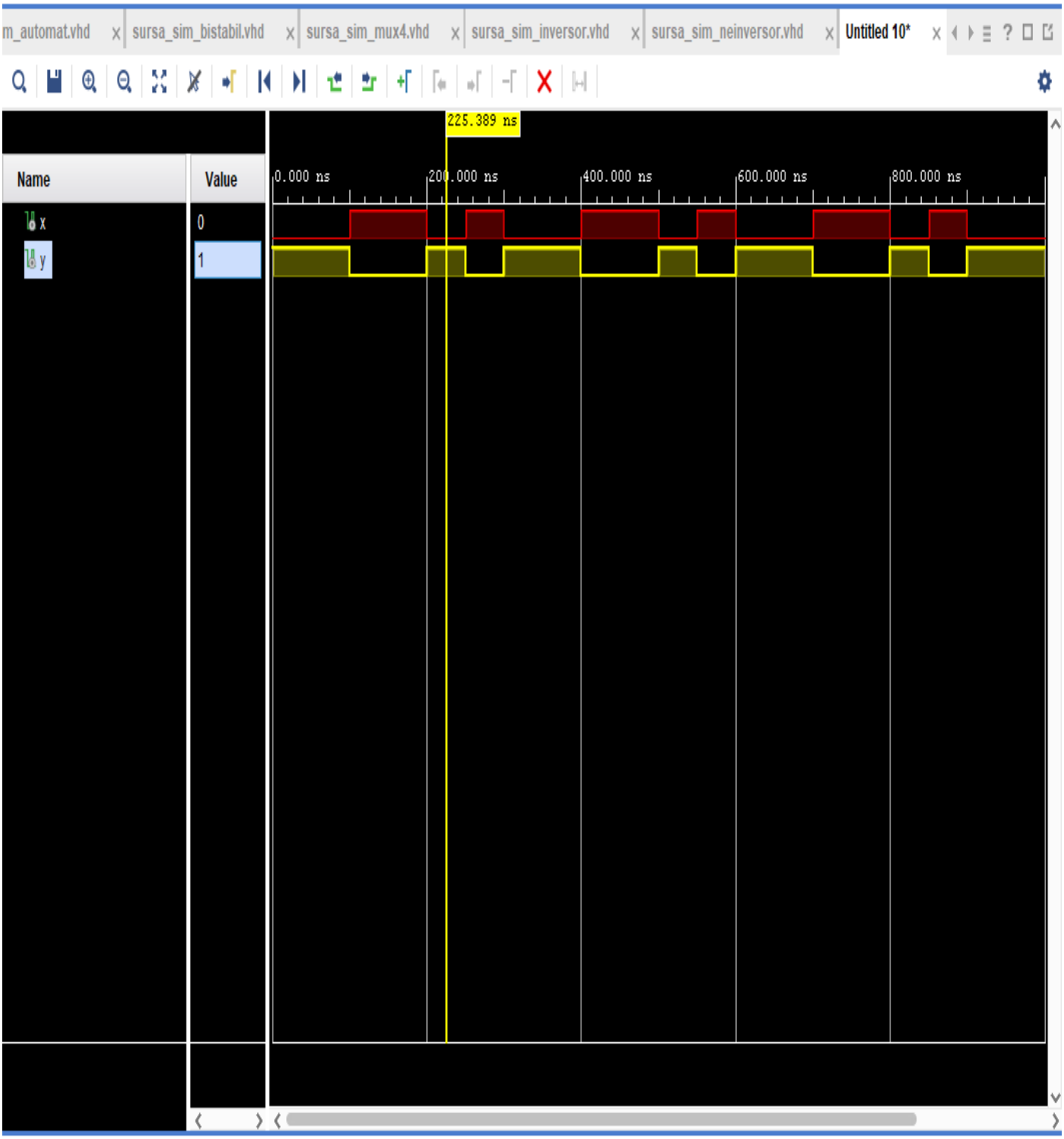
```
7   -- Module Name: inv - Behavioral
8   -- Project Name:
9   -- Target Devices:
10  -- Tool Versions:
11  -- Description:
12  --
13  -- Dependencies:
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------
20
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity inv is
35      Port ( x : in STD_LOGIC;
36             y : out STD_LOGIC);
37  end inv;
38
39  architecture Behavioral of inv is
40
41  begin
42
43  process(x)
44  begin
45
46  y <= not x;
47
48  end process;
49  end Behavioral;
50
```

e) Sursa de simulare a inversorului

```
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity sursa_sim_inversor is
35  --  Port ( );
36  end sursa_sim_inversor;
37
38  architecture Behavioral of sursa_sim_inversor is
39
40  component inv is
41      Port ( x : in STD_LOGIC;
42             y : out STD_LOGIC);
43  end component inv;
44
45  signal x :std_logic;
46  signal y:  std_logic;
47
48  begin
49
50  ut: inv port map (x => x, y => y);
51
52  process
53  begin
54
55  x <= '0'; wait for 100 ns;
56  x <= '1'; wait for 100 ns;
57  x <= '0'; wait for 50 ns;
58  x <= '1'; wait for 50 ns;
59
60  end process;
61  end Behavioral;
62
```

Proiect C.I.D

f) Simularea inversorului



g) Sursa de design a neinversorului

```
 7  -- Module Name: neinv - Behavioral
 8  -- Project Name:
 9  -- Target Devices:
10  -- Tool Versions:
11  -- Description:
12  --
13  -- Dependencies:
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------
20
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity neinv is
35      Port ( x : in STD_LOGIC;
36             y : out STD_LOGIC);
37  end neinv;
38
39  architecture Behavioral of neinv is
40
41  begin
42
43  process(x)
44  begin
45
46  y <= x;
47
48  end process;
49  end Behavioral;
50
```

h) Sursa de simulare a neinversorului

```
19  ----------------------------------------------------------------------------------
20
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity sursa_sim_neinversor is
35  --  Port ( );
36  end sursa_sim_neinversor;
37
38  architecture Behavioral of sursa_sim_neinversor is
39  component neinv is
40      Port ( x : in STD_LOGIC;
41             y : out STD_LOGIC);
42  end component neinv;
43
44  signal x : std_logic;
45  signal y : std_logic;
46
47  begin
48
49  ut: neinv port map ( x => x, y => y);
50
51  process
52  begin
53
54  x <= '0'; wait for 100 ns;
55  x <= '1'; wait for 100 ns;
56  x <= '0'; wait for 50 ns;
57  x <= '1'; wait for 50 ns;
58
59  end process;
60  end Behavioral;
61
```

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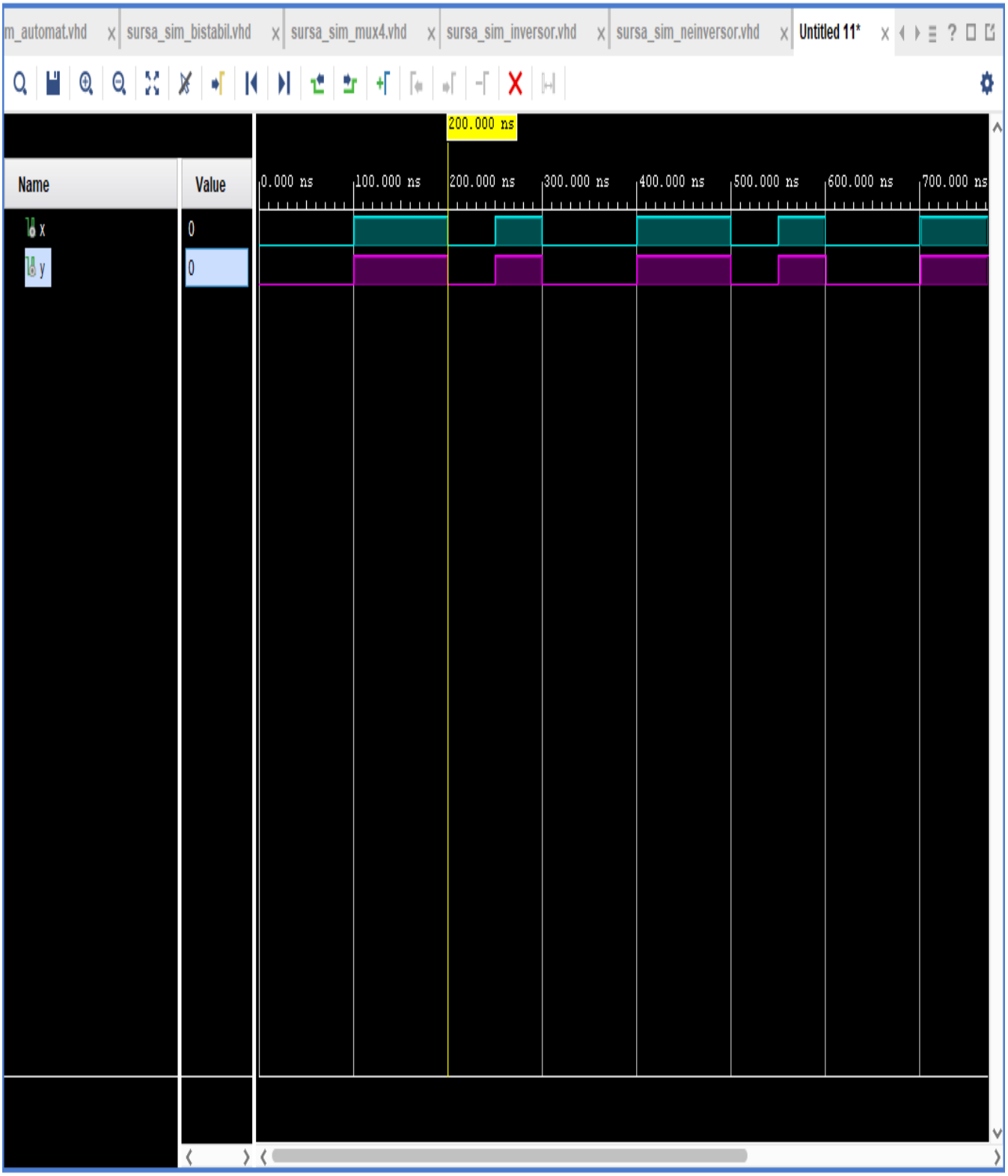
i) Simularea neinversorului



3. Circuitul secvențial

a) Sursa de design a bistabilului JK

```
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity bistabil is
35      Port ( j : in STD_LOGIC;
36             k : in STD_LOGIC;
37             clk : in STD_LOGIC;
38             r : in STD_LOGIC;
39             q : out STD_LOGIC;
40             qn : out STD_LOGIC);
41  end bistabil;
42
43  architecture Behavioral of bistabil is
44
45  signal stare : std_logic;
46  signal input : std_logic_vector (1 downto 0);
47
48  begin
49
50  input <= j&k;
51
52  process(clk,r)
53  begin
54  if r = '1' then
55    stare <= '0';
56  else
57    if falling_edge(clk) then
58       case input is
59          when "00" => stare <= stare;
60          when "01" => stare <= '0';
61          when "10" => stare <= '1';
62          when "11" => stare <= not stare;
63          when others => stare <= stare;
64       end case;
65       end if;
66       end if;
67       end process;
68
69       q <= stare;
70       qn <= not stare;
71
72  end Behavioral;
73
```

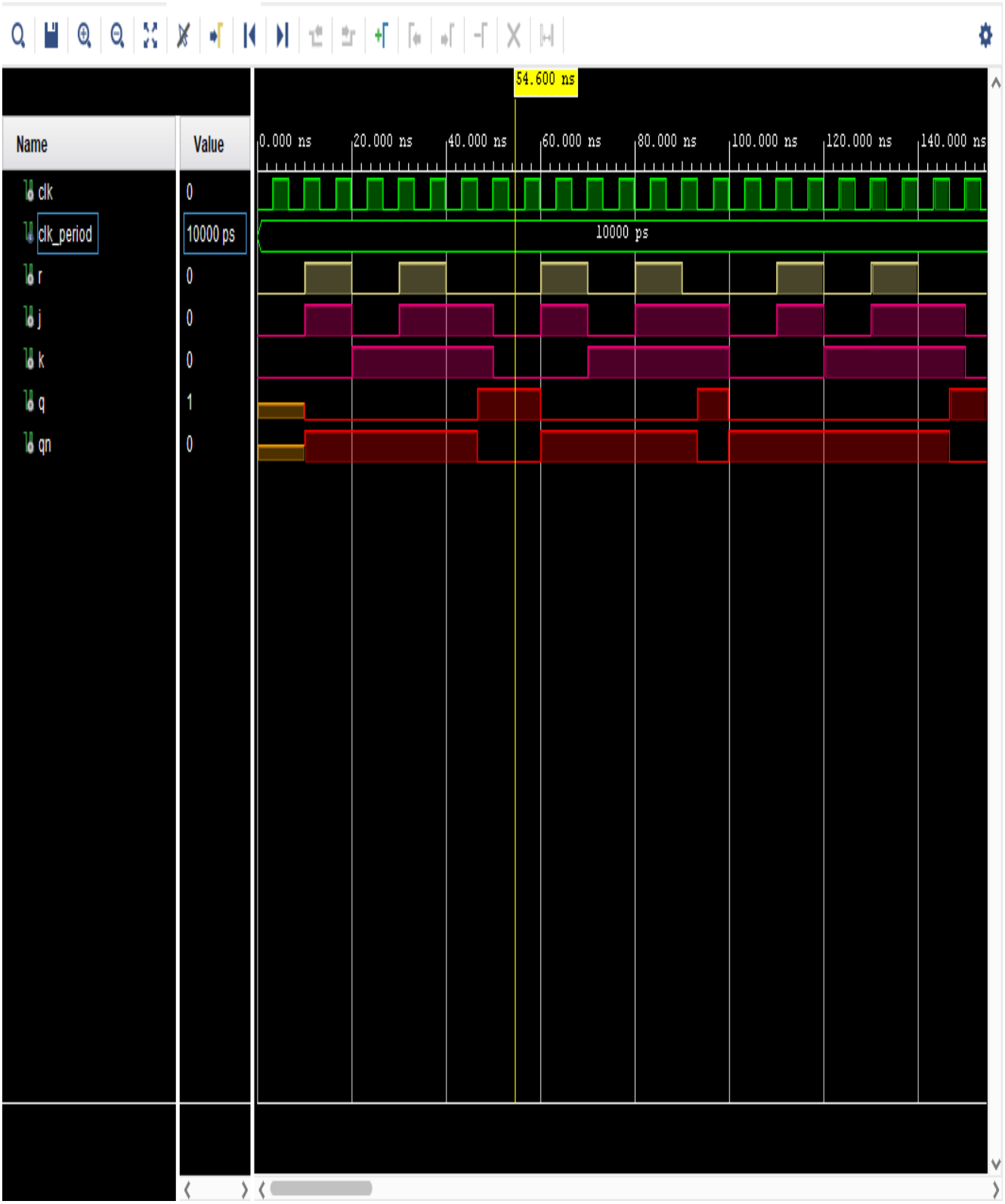
b) Sursa de simulare a bistabilului JK

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity sursa_sim_bistabil is
--  Port ( );
end sursa_sim_bistabil;

architecture Behavioral of sursa_sim_bistabil is

component bistabil is
    Port ( j : in STD_LOGIC;
           k : in STD_LOGIC;
           clk : in STD_LOGIC;
           r : in STD_LOGIC;
           q : out STD_LOGIC;
           qn : out STD_LOGIC);
end component bistabil;


signal clk: std_logic := '0';
signal r: std_logic := '0';
signal j: std_logic := '0';
signal k: std_logic := '0';

signal q: std_logic;
signal qn: std_logic;

constant clk_period : time := 10 ns;

begin

uut: bistabil port map(clk => clk,
                       r => r,
```

```
64                                  j => j,
65                                  k => k,
66                                  q => q,
67                                  qn => qn);
68
69      process
70      begin
71      clk <= '0';wait for clk_period/3;
72      clk <= '1';wait for clk_period/3;
73      end process;
74
75      process
76      begin
77
78      r <= '0';
79      j <= '0';
80      k <= '0';
81
82      wait for clk_period;
83
84      r <= '1';
85      j <= '1';
86      k <= '0';
87
88      wait for clk_period;
89
90      r <= '0';
91      j <= '0';
92      k <= '1';
93
94      wait for clk_period;
95
96      r <= '1';
97      j <= '1';
98      k <= '1';
99
100     wait for clk_period;
101
102     r <= '0';
103     j <= '1';
104     k <= '1';
105
106     wait for clk_period;
```

```
107
108     r <= '1';
109     j <= '0';
110     k <= '0';
111
112     end process;
113     end Behavioral;
114
```

c) Simularea bistabilului



4. Implementarea finala a automatului

a) Sursa de design a automatului

```
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity automat is
35      Port ( clk : in STD_LOGIC;
36             r : in STD_LOGIC;
37             q : out STD_LOGIC_VECTOR (2 downto 0));
38  end automat;
39
40  architecture Behavioral of automat is
41
42  component mux4 is
43      Port ( i0 : in STD_LOGIC;
44             i1 : in STD_LOGIC;
45             i2 : in STD_LOGIC;
46             i3 : in STD_LOGIC;
47             a1 : in STD_LOGIC;
48             a0 : in STD_LOGIC;
49             y : out STD_LOGIC);
50  end component mux4;
51
52  component bistabil is
53      Port ( j : in STD_LOGIC;
54             k : in STD_LOGIC;
55             clk : in STD_LOGIC;
56             r : in STD_LOGIC;
57             q : out STD_LOGIC;
58             qn : out STD_LOGIC);
59  end component bistabil;
60
61  component inv is
62      Port ( x : in STD_LOGIC;
63             y : out STD_LOGIC);
64  end component inv;
```

```
65
66  component neinv is
67      Port ( x : in STD_LOGIC;
68             y : out STD_LOGIC);
69  end component neinv;
70
71  signal netJ2, netJ1, netJ0, netK2, netK1, netK0: std_logic;
72  signal qint: std_logic_vector(2 downto 0);
73  signal netA, netB:std_logic;
74
75  begin
76
77  q <= qint;
78
79  JK2: bistabil port map(clk => clk,
80                         r => r,
81                         j => netJ2,
82                         k => netK2,
83                         q => qint (2));
84  JK1: bistabil port map(clk => clk,
85                         r => r,
86                         j => netJ1,
87                         k => netK1,
88                         q => qint (1));
89  JK0: bistabil port map(clk => clk,
90                         r => r,
91                         j => netJ0,
92                         k => netK0,
93                         q => qint (0));
94
95  M1: mux4 port map (i0 =>'1',
96                     i1 => '0',
97                     i2 => '0',
98                     i3 => '0',
99                     a1 => qint(2),
100                    a0 => qint(1),
101                    y => netJ2);
102
103 M2: mux4 port map (i0 => '0',
104                    i1 => '0',
105                    i2 => netA,
106                    i3 => '0',
107                    a1 => qint (2),
108                    a0 => qint(1),
```

```
109                      y => netK2);
110
111   M3: mux4 port map (i0 => '0',
112                      i1 => '0',
113                      i2 => '1',
114                      i3 => '0',
115                      a1 => qint (2),
116                      a0 => qint (1),
117                      y => netJ1);
118
119   M4: mux4 port map(i0 => '0',
120                     i1 => '1',
121                     i2 => '0',
122                     i3 => netA,
123                     a1 => qint(2),
124                     a0 => qint(1),
125                     y => netK1);
126
127   M5: mux4 port map(i0 => '0',
128                     i1 => netB,
129                     i2 => '0',
130                     i3 => netB,
131                     a1 => qint(2),
132                     a0 => qint(1),
133                     y => netJ0);
134
135   M6: mux4 port map (i0 => '1',
136                      i1 => netA,
137                      i2 => netA,
138                      i3 => '0',
139                      a1 => qint(2),
140                      a0 => qint(1),
141                      y => netK0);
142
143   I: inv port map(x => qint(0), y => netB);
144
145   NEI: neinv port map(x => qint(0), y => netA);
146   end Behavioral;
```

b) Sursa de simulare a automatului

```
19  ----------------------------------------------------------------------------------
20
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity sursa_sim_automat is
35  --  Port ( );
36  end sursa_sim_automat;
37
38  architecture Behavioral of sursa_sim_automat is
39  component automat is
40      Port ( clk : in STD_LOGIC;
41             r : in STD_LOGIC;
42             q : out STD_LOGIC_VECTOR (2 downto 0));
43  end component automat;
44
45  signal clk,r:std_logic;
46  signal q:std_logic_vector (2 downto 0);
47
48  begin
49
50  UT: automat port map (clk,r,q);
51
52  process
53  begin
54
55  clk <= '0'; wait for 1.2 ns;
56  clk <= '1'; wait for 1.2 ns;
57
58  end process;
59
60  r <= '1' after 0 ns, '0' after 2.2 ns;
61  end Behavioral;
62
```

Proiect C.I.D

c) Simularea automatului