1) A copy of the new Verilog code you used to implement the design. The Verilog code should be complete with useful comments (5 pts).

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09/24/2025 10:02:24 AM
// Design Name:
// Module Name: decoder
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module decoder_structural(
    input [2:0] sw,
    output [7:0] led
    );


    wire nsw_0, nsw_1, nsw_2;//creates wires for the not gates

    not not_gate0 (nsw_0, sw[0]);//creates a not gate for s0
    not not_gate1 (nsw_1, sw[1]);//creates a not gate for s1
    not not_gate2 (nsw_2, sw[2]);//creates a not gate for s2

    and and_gate0 (led[0], nsw_2, nsw_1, nsw_0);//if sw= 000 then led0 turns on
    and and_gate1 (led[1], nsw_2, nsw_1, sw[0]);//if sw= 001 then led1 turns on
    and and_gate2 (led[2], nsw_2, sw[1],  nsw_0);//if sw= 010 then led2 turns on
    and and_gate3 (led[3], nsw_2, sw[1],  sw[0]);//if sw= 011 then led3 turns on
    and and_gate4 (led[4], sw[2],  nsw_1, nsw_0);//if sw= 100 then led4 turns on
    and and_gate5 (led[5], sw[2],  nsw_1, sw[0]);//if sw= 101 then led5 turns on
    and and_gate6 (led[6], sw[2],  sw[1],  nsw_0);//if sw= 110 then led6 turns on
    and and_gate7 (led[7], sw[2],  sw[1],  sw[0]);//if sw= 111 then led7 turns on
```

endmodule

2) A brief description of the unique (new) tools, technologies, or methods used to implement this lab (5 pts).

-In the first part of the lab I copied and pasted some code of what I believe as a flip flop. Then in the second part i got the chance to actually code it using wires, "and" and "or" gates. I have never used Verlog before in 240 I used system Verlog so I had to use gemini for some help with the code and then I was able to finish implementing it. I also looked into the elaborated design and sw all the not, and, and or gates used to create the decoder.

3) Images of implemented schematic or other useful images (5 pts).
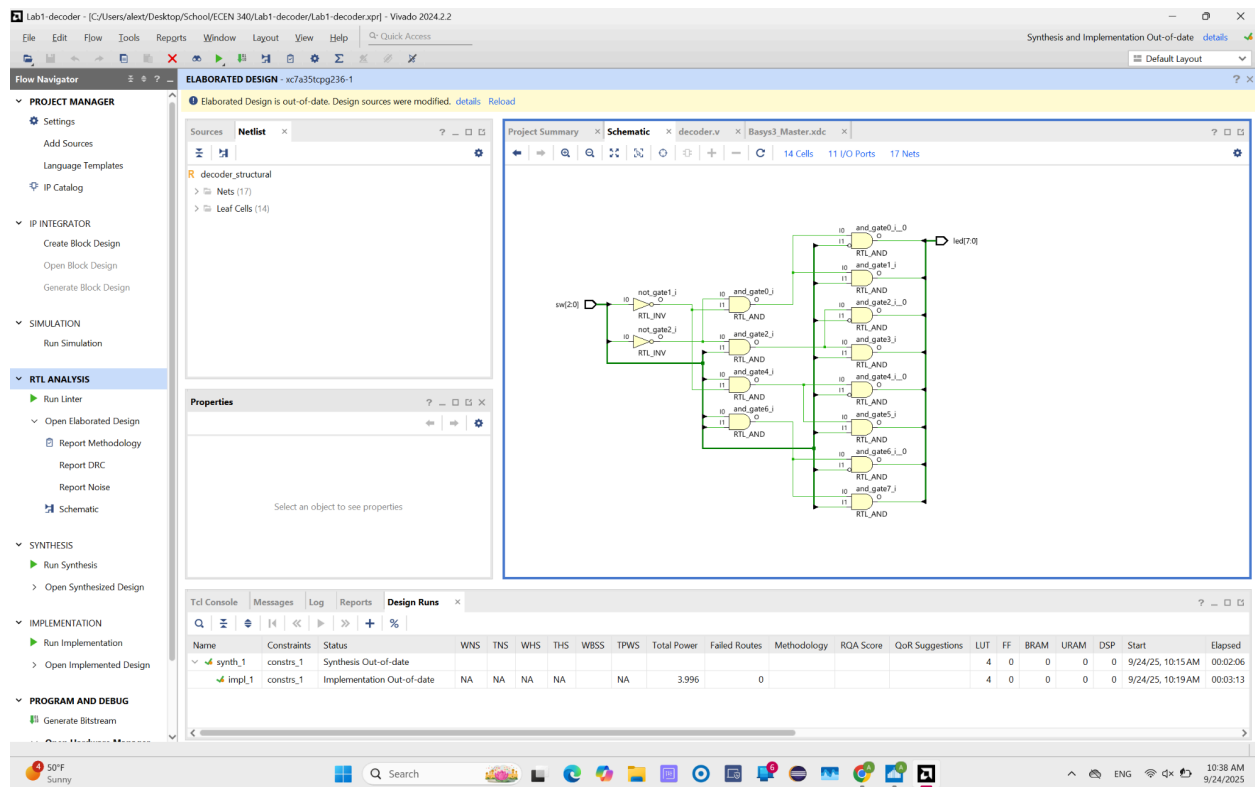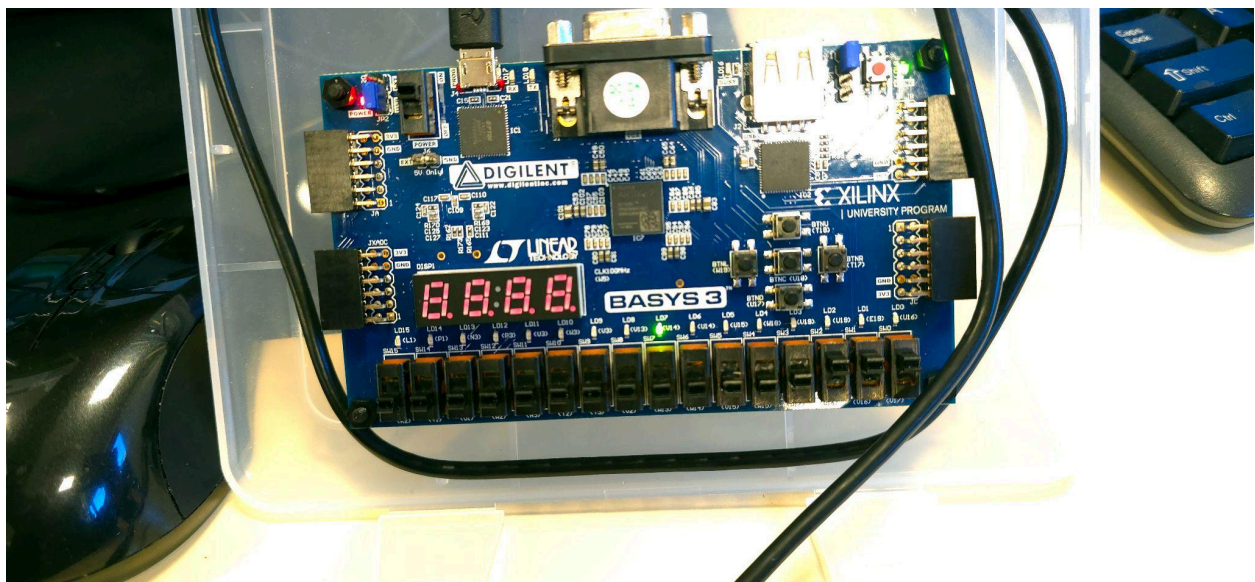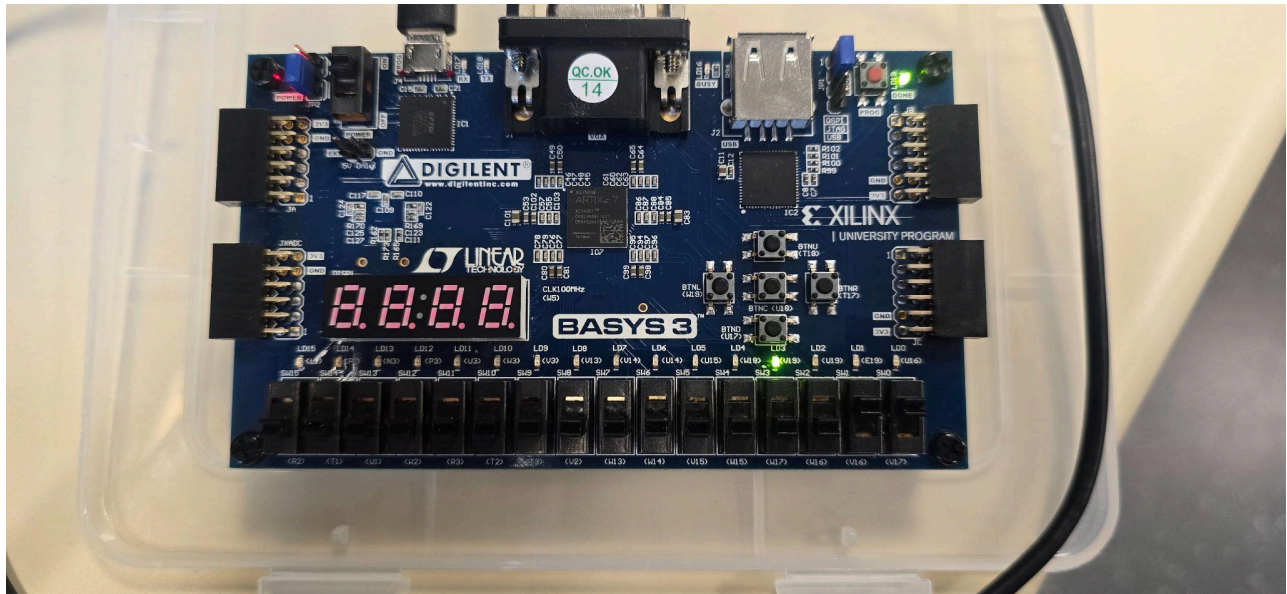
4) The report should be professional quality—meaning it will be neat and
use proper English (5 pts).

-I assume I am to leave this blank as it seems to refer to the document as a whole. If I am wrong
my apologies and please leave a comment so I can include something here in the next lab.

5) In your conclusion statement, discuss your results, the method of
testing, and include the level of functionality (percent functional) of the lab (5 pts).

-   In this lab there were two parts. The first part was primarily used to help ensure that we
    understood how vivado worked and to get a working circuit. The second part was more
    independent where we wrote our own code rather than just copy and pasted it. I was

able to create all the circuitry using not, and, and nor gates. Afterwards I was able to look into the elaborated design and saw all of the gates in use and saw that it looks like a decoder. I then programmed the board and was able to experiment with the switches to ensure that all of the correct LEDS lit up when the correct switches were flipped.