1) A copy of the Verilog code used to implement the design(s). The Verilog code should be complete with useful comments (5 pts).

seg7.v

```verilog
//`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 10/06/2025 10:15:19 AM
// Design Name:
// Module Name: seg7
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module seg7(
    input [3:0] sw,
    output reg [6:0] seg,
    output [3:0] an,
    output dp
    );

    assign an = 4'b1110;

    assign dp = 1'b1;

    always @(sw)
      case (sw)
        4'h0: seg = 7'b1000000;
        4'h1: seg = 7'b1111001;
        4'h2: seg = 7'b0100100;
        4'h3: seg = 7'b0110000;
        4'h4: seg = 7'b0011001;
        4'h5: seg = 7'b0010010;
```

```verilog
        4'h6: seg = 7'b0000010;
        4'h7: seg = 7'b1111000;
        4'h8: seg = 7'b0000000;
        4'h9: seg = 7'b0010000;
    endcase
endmodule
```

seg7_tb.v

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 10/08/2025 09:16:38 AM
// Design Name:
// Module Name: seg7_tb
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module seg7_tb(
    );

    reg [3:0] sw;
    wire [6:0] seg;
    wire [3:0] an;
    wire dp;

    seg7 uut (
        .sw(sw),
        .seg(seg),
        .an(an),
        .dp(dp)
    );
```

```verilog
    initial
    begin
        sw = 4'h0;

        #100

        for (integer i = 0; i < 10; i = i + 1)
        begin
            sw = i;
            #10;
        end

        $finish;
    end

endmodule
```

2) A brief description of the unique (new) tools, technologies, or methods used to implement this lab (5 pts).

      -We learned to write testbenches. And how they are used for testing code so that we can make sure all is well before moving onto the next step of production. We also learned how to simulate our design and verify the functionality of our design.

3) The report should be professional quality—meaning it will be neat and use proper English. You may include Vivado screen shots to make it easier to document your work (5 pts).
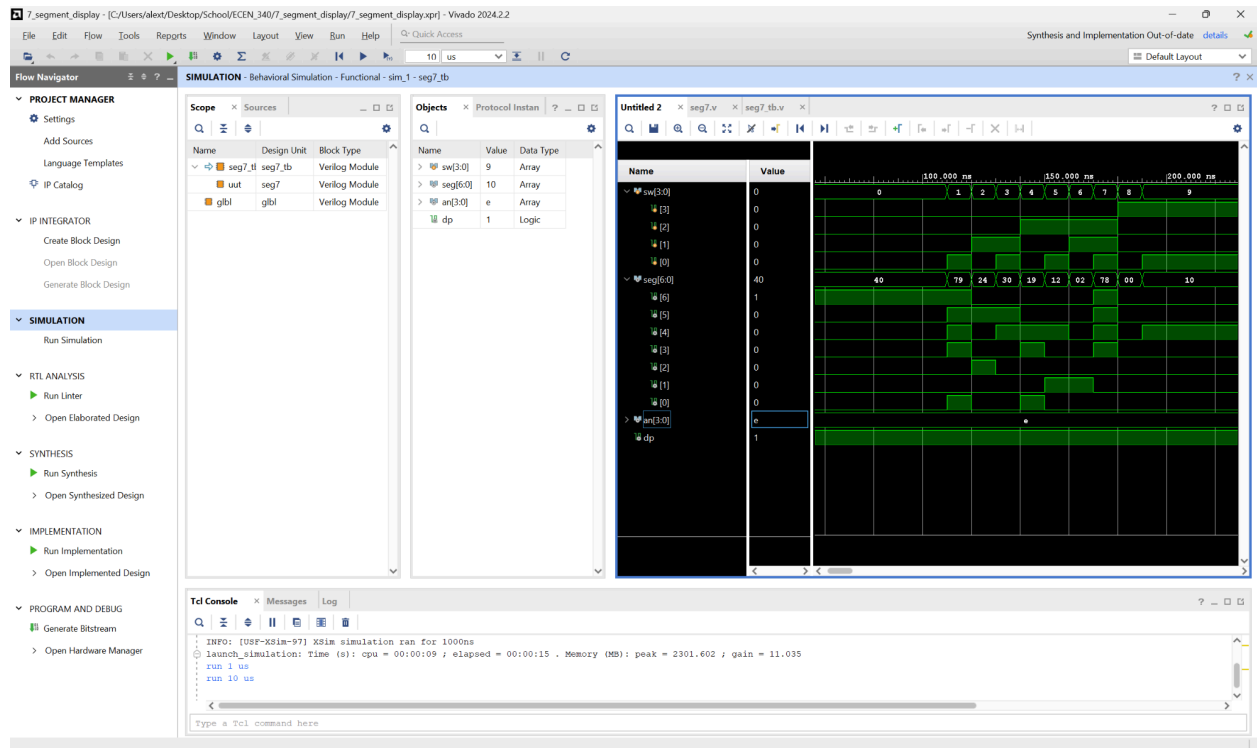
4) In your conclusion statement, you will discuss your results, the method of testing, and include the level of functionality of the lab (10 pts).

- I was able to successfully complete all portions of the lab. My design was able to correctly run not only on the board but via simulation as well. When running my program through the board I was able to use the four first switches to toggle between the correct numbers on the 7 seg displays. I was then able to simulate this same functionality via simulation by creating a test bench that ran through all of the possible switch values and testing that the correct leds in the display lit up.