ALEX LI

Bellevue, Washington | alexxuanqili@gmail.com | (703) 981-4596 | linkedin.com/in/alex-li12 | AlexXLi12.github.io

RELEVANT SKILLS

- **Programming Languages:** Python, C/C++, Assembly, SQL, Java, JavaScript, SystemVerilog, HTML/CSS
- **Frameworks/Libraries:** Flask, Spring Boot, Express, React, Next, PyTorch, NumPy, pandas
- **Technologies:** Linux, Git, Make, SQLite, MariaDB, PostgreSQL, JDBC, FPGAs, ModelSim, AWS

EDUCATION

University of Washington, Seattle, WA — Expected June 2027
B.S., Computer Science — GPA: 3.7

Relevant Coursework: Discrete Mathematics, Linear Algebra, Data Structures and Parallelism, Hardware/Software Interface, Systems Programming, Digital Circuit Design, Mathematical Methods for Quantitative Finance, Machine Learning, Distributed Systems, Data Management
Awards: Best Use of AI + Best Finance/Data Analytics Project (HackTech 2025), **1st Place** DubHacks 2023 (Synergy Track), **Futureforce Selectee** (Salesforce Data Cloud), Dean's List (2023–24)

RELEVANT EXPERIENCE

Chewy, Inc. | *Spring Boot, Terraform, AWS, Mockito, Guice* — June 2025 – August 2025
Software Engineering Intern

- **Owned the architecture and deployment** of a report scheduler to replace Kevel (3rd party) for Chewy Ads to enable in-house scheduling, authorization, and report delivery via S3 and email pipelines using AWS Lambda, SQS, and DynamoDB.
- Led design reviews with senior engineers, incorporating **fault-tolerant patterns** such as exponential backoff, DLQs, and deduplication through SHA-256 hashing.
- Owned back-end infrastructure and API development to support **scalable, idempotent reporting workflows** with consistency guarantees across retries and failures.

UW Sensor Systems Lab | *FPGAs, Verilog, GTKWave, Python, Serial Interfaces* — Dec 2024 – Present
Undergraduate Research Assistant

- Built low-level drivers for FPGA-controlled acoustic levitation arrays; Optimized the UART protocol from scratch to replace I^2C and boost throughput on the **primary signal pipeline**.
- Programmed transducer synchronization code to serialize phase-angle control across **100+ actuators** in real-time object manipulation experiments.
- Enhanced hardware stability and reliability through custom Verilog timing logic and signal integrity improvements.

PROJECTS

Distributed Key-Value Store (Multi-Paxos, Sharded) | *Java, Multi-Paxos, Sharding*

- Implemented a fault-tolerant, linearizable **sharded key-value store** using Multi-Paxos for log consensus and dynamic shard rebalancing.
- Wrote node logic for **leader election**, shard replication, and consensus-driven reconfiguration. Verified correctness with an adversarial distributed test suite.
- Authored a detailed specification covering architecture, consensus, and failure semantics under partitioned networks and crash faults.

C++ Web Server | *C/C++, Networking, Multiprocessing*

- Built an HTTP server from scratch using **low-level sockets, process-based concurrency**, and POSIX-compliant file I/O.
- Designed a custom query processor and a memory-safe caching layer to minimize search latency across static files.

FPGA Flappy Bird | *DE1-SoC, SystemVerilog, ModelSim*

- Prototyped a modular FPGA Flappy Bird clone using **LFSRs, clock dividers**, and **two-stage flip-flop synchronizers** for button input.
- Verified functional units through targeted test benches and deployed to DE1-SoC with 7-segment display and LED output.