A Charge-Trapping Model for the Fast Component of Positive Bias Temperature Instability (PBTI) in High-κ Gate-Stacks

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***Abstract*— We propose a physical model for the fast component (<1 s) of the positive bias temperature instability (PBTI) process in SiO_x/HfO_2 gate-stacks. The model is based on the electron–phonon interaction governing the trapping/emission of injected electrons at the preexisting defects in the dielectric stack. The model successfully reproduces the experimental time dependences of the V_{TH} shift on both stress voltage and temperature. Simulations allow the extraction of the physical characteristics of the defects contributing to PBTI, which are found to match those assisting the leakage current in these stacks (i.e., oxygen vacancies).**

***Index Terms*— Charge trapping, device modeling, high-κ dielectric, positive bias temperature instability (PBTI).**

I. Introduction

THE positive bias temperature instability (PBTI), i.e., the positive threshold voltage (V_{TH}) shift observed in n-channel MOSFETs subjected to positive voltage stress, affects the performances of high-k gate oxide stacks, especially in devices fabricated in the gate-first process scheme. The physical mechanisms governing PBTI have been discussed in many experimental and simulation studies [1]–[15]. The V_{TH} shift was reported exhibiting qualitatively different features for short and long stress times [5], [7]. At short stress times, the V_{TH} shift (ΔV_{TH}) exhibits a weak dependency on the temperature (T), and it can be recovered to a large degree by applying a negative bias. This behavior has been attributed to the charge trapping and detrapping at preexisting defects in the high-k dielectric. However, the defects responsible for the V_{TH} shift have never been unambiguously identified, and their possible contribution to other reliability issues such as leakage current and drain current noise remains unaddressed.

On the other hand, the V_{TH} shift observed at longer stress times ($t > \approx 1$ s) depends on temperature and, differently from the case of short time stresses, it cannot be recovered completely [5]. In [4], [6], and [7], the slow V_{TH} increase was attributed to charge trapping into defects with properties different from those contributing to the fast V_{TH} instability. In [5] and [13], the long-term V_{TH} increase was suggested to be caused by the stress-induced generation of new traps, which subsequently trap electrons. The reaction–diffusion mechanism was also invoked to explain the slow PBTI component [13]. Most of the attempts to describe the kinetics of the V_{TH} shift over different time scales rely on semiempirical models. A quantitative evaluation of the charge trapping process requires a quantum mechanical description of the electron transport through the dielectric, including the charge transfer via the defects accounting for the trap-to-trap tunneling processes [16]–[19].

In this paper, we model the electron trapping in SiO_x/HfO_2 gate-stacks by explicitly considering the coupling of the injected electrons with the displacements of the lattice atoms (i.e., phonons), which accompanies the charge carrier trapping/detrapping at the defect sites in the dielectric. This allows reproducing the measured ΔV_{TH} kinetics, explaining its dependence on stress voltage and temperature. Furthermore, the simulations connect the V_{TH} instability to the atomic characteristics of the defect parameters, enabling the optimization of the fabrication process.

This paper is organized as follows. The quantum-mechanical model that includes the electron–phonon coupling, developed to simulate the transient charge trapping phenomena in the HfO_2 stack, is described in Section II. Devices and experimental techniques adopted to monitor the V_{TH} shift are discussed in Section III. In Section IV, the results of the simulation of the V_{TH} transients under dc and ac stress and their dependences on the temperature/voltage are compared with the experimental data.

II. Physics-Based Model of Charge Trapping

To study the charge trapping/emission transients, we employed a physical–statistical description for the charge trapping process [19]–[21]. The dominant charge transport mechanism through the dielectric stack was shown to be the trap-assisted tunneling (TAT) assisted by oxygen vacancy defects [19]. In this paper, the defects are considered to be randomly distributed throughout the dielectric stack, and every

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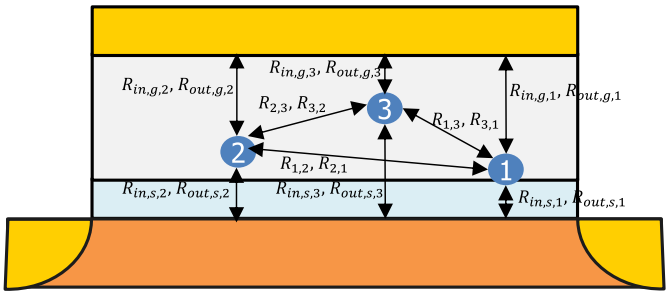

Fig. 1. Schematic illustration of the transition rates in the case of three traps in the dielectric stack.

electron transition between the multiple traps, traps and Si substrate, and traps and metal gate is considered, as shown in Fig. 1. The transition rates are calculated in the framework of the multiphonon TAT theory [16]–[19]. These rates depend on two parameters related to the chemical/physical nature of the defect, i.e., the thermal ionization energy (E_T) and the relaxation energy (E_{REL}). The relaxation energy controls the carrier–phonon interaction, and it represents the energy associated with the displacements of lattice atoms accompanying a charge trapping/emission event.

The average occupancy F_j of each trap is calculated through the charge balance equation

$$\frac{\partial F_j}{\partial t} = R_{\mathrm{in},j}(t)\cdot(1-F_j(t)) - R_{\mathrm{out},j}(t)\cdot F_j(t) \qquad (1)$$

where $R_{\mathrm{in},j}$ and $R_{\mathrm{out},j}$ are the input and output rates to and from the jth trap, respectively. They are calculated by considering every possible charge transition, as shown in Fig. 1

$$R_{\mathrm{in},j}(t) = R_{\mathrm{in},s,j} + R_{\mathrm{in},g,j} + \sum_{k=1}^{N_T} F_k(t)\cdot R_{k,j} \qquad (2)$$

$$R_{\mathrm{out},j}(t) = R_{\mathrm{out},s,j} + R_{\mathrm{out},g,j} + \sum_{k=1}^{N_T} R_{j,k}(1-F_k(t)). \qquad (3)$$

N_T is the total number of traps; $R_{\mathrm{in},s,j}$ and $R_{\mathrm{out},s,j}$ ($R_{\mathrm{in},g,j}$ and $R_{\mathrm{out},g,j}$) are the capture and emission rate of the jth trap from and to the substrate (gate), respectively; $R_{i,j}$ is the transition rate from the ith trap to the jth trap. The transition rates are calculated considering the tunneling probability through the dielectric barrier and the phonon-assisted electron capture/emission at the trap sites, as described in [19] and [20]. Equation (1) is solved numerically by discretizing the simulation time. At each discrete time t_n, the occupancy of each trap is calculated through

$$F_j(t_{n+1}) = F_j(t_n) + [R_{\mathrm{in},j}(t_n)\cdot(1-F_j(t_n)) - R_{\mathrm{out},j}(t_n)\cdot F_j(t_n)]\cdot(t_{n+1}-t_n). \qquad (4)$$

The initial trap occupancy $F_j(0)$ is set to its equilibrium value calculated using the Fermi–Dirac occupation probability, by considering that the stack is initially unbiased, i.e., $V_G = 0$ V.

The electric field in the device is calculated by solving Poisson's equation accounting for the charge trapped at the defect sites. At every discrete time t_n, the transition rates are calculated using the updated electric field.

The threshold voltage shift ΔV_{TH} is calculated from the instantaneous trap occupancy values $F_j(t)$

$$\Delta V_{\mathrm{TH}}(t) = \sum_{j=1}^{N_T} \Delta V_{\mathrm{TH},j}\cdot(F_j(t)-F_j(0)) \qquad (5)$$

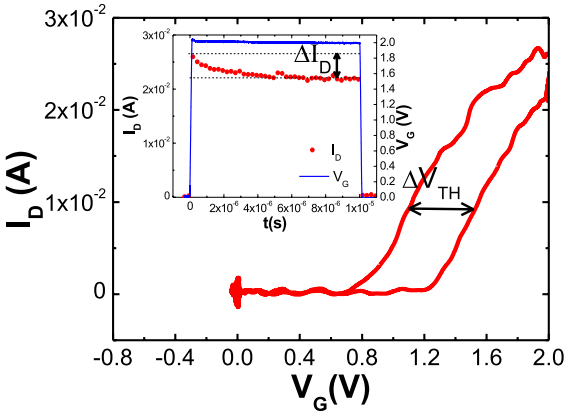

Fig. 2. Drain current I_D versus gate voltage V_G measured under a 10 μs/2 V voltage pulse in the 1-nm IL/5-nm HfO_2 stack. Inset: corresponding I_D and V_G time transients.

where $\Delta V_{\mathrm{TH},j}$ is the threshold voltage shift due to the filling of the jth trap, calculated within the charge sheet approximation.

The transient gate current, which neglects for simplicity the contribution of the displacement current, is calculated as

$$I_G(t) = q\cdot\left[\sum_{j=1}^{N_T} R_{\mathrm{in},s,j}\cdot(1-F_j(t)) - \sum_{j=1}^{N_T} R_{\mathrm{out},s,j}\cdot F_j(t)\right] + I_{\mathrm{DT}}(t) \qquad (6)$$

where $I_{\mathrm{DT}}(t)$ is the direct tunneling current.

The steady-state values reached by the trap occupancies at $t\to\infty$ can be calculated as

$$F_{j,\mathrm{SS}} = \frac{R_{\mathrm{in},j,\mathrm{SS}}}{R_{\mathrm{in},j,\mathrm{SS}} + R_{\mathrm{out},j,\mathrm{SS}}}. \qquad (7)$$

$R_{\mathrm{in},j,\mathrm{SS}}$ and $R_{\mathrm{out},j,\mathrm{SS}}$ are the steady-state input and output rates to and from the jth trap, respectively. They depend on the steady-state occupancies of the other traps

$$R_{in,j,\mathrm{SS}}(t) = R_{in,s,j} + R_{in,g,j} + \sum_{k=1}^{N_T} F_{k,\mathrm{SS}}(t)\cdot R_{k,j} \qquad (8)$$

$$R_{\mathrm{out},j,\mathrm{SS}}(t) = R_{\mathrm{out},s,j} + R_{\mathrm{out},g,j} + \sum_{k=1}^{N_T} R_{j,k}(1-F_{k,\mathrm{SS}}(t)). \qquad (9)$$

Equations (7)–(9) constitute a system of N_T equations, whose solution allows determining the N_T unknown steady-state trap occupancies $F_{j,\mathrm{SS}}$ ($j = 1\ldots N_T$) [22].

III. Devices and Experiments

Measurements were performed on n-MOSFETs with a TiN electrode and gate-first stacks comprised of an atomic layer deposition HfO_2 film of various thicknesses deposited on a 1-nm chemically grown SiO_x interfacial layer. The V_{TH} transients were measured by applying a pulsed I–V stress [23] with varying pulsewidths. The pulse rising and falling times are very fast (100 ns), as required to minimize the charge trapping/emission processes.

Fig. 2 shows the drain current (I_D) versus gate voltage (V_G) measured during the application of a 10-μs 2 V pulse on a 1-nm IL/5-nm HfO_2 stack. The charge trapping induces a hysteresis in the I_D–V_G characteristics. By plotting I_D in the time domain, a significant reduction of the drain current

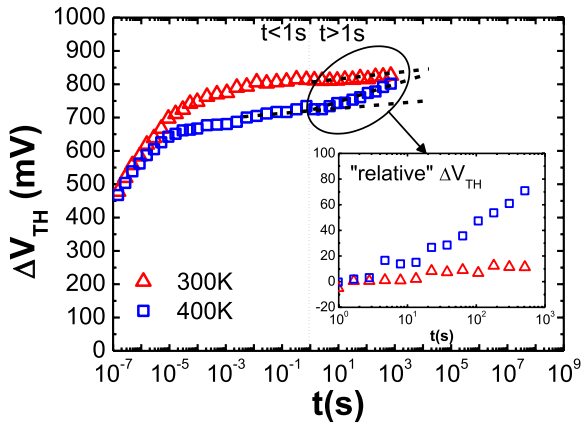

Fig. 3. $\Delta V_{\rm TH}$ versus stress time transients measured at different temperatures at $V_G = 2.5$ V on the 1-nm IL/5-nm HfO_2 stack. Inset corresponding $V_{\rm TH}$ shift observed at long times, $\Delta V_{{\rm TH},L}(t) = V_{\rm TH}(t) - V_{\rm TH}(1s)$, determined by subtracting the contribution due to the fast threshold voltage shift, $V_{\rm TH}(1s)$.

ΔI_D is observed, as shown in the inset of Fig. 2. The $V_{\rm TH}$ shift induced by the voltage pulse with respect to the $V_{\rm TH}$ value at $t = 0$, can be extracted from the shift between the I_D–V_G curves observed at pulse rise and fall times [24]. However, the $V_{\rm TH}$ shift derived using this approach is sensitive to the $V_{\rm TH}$ recovery due to charge emission, which might occur during the pulse fall period [25]. We addressed this issue by extracting the $V_{\rm TH}$ shift directly from the I_D decrease during the voltage pulse (on-the-fly method), as shown in the inset in Fig. 2 [6]

$$V_{\rm TH} - V_{\rm TH}(t_0) = -\frac{I_D - I_D(t_0)}{I_D(t_0)} \cdot (V_G - V_{\rm TH}(t_0)). \quad (10)$$

The $V_{\rm TH}$ shift is calculated with respect to the time t_0, which is required to acquire the first I_D point after the positive voltage is applied [26]. This method is not sensitive to $V_{\rm TH}$ recovery since I_D is measured without voltage stress interruption.

Fig. 3 shows the $V_{\rm TH}$ shifts, measured using the described technique, from 1 μs to 1000 s on the 1-nm IL/5-nm HfO_2 stack at two temperatures, i.e., 300 and 400 K. In agreement with [5], [7], and [11], qualitatively different features of the $V_{\rm TH}$ dependence on the stress conditions are observed during short ($t < 1$ s) and long ($t > 1$ s) stress periods. For simplicity, the $V_{\rm TH}$ shift observed through the first 1 s of stress is termed fast PBTI, while the threshold voltage increase occurring on a longer time scale, i.e., for the stress times > 1 s is called slow PBTI.

At short times ($t < 1$ s), $\Delta V_{\rm TH}$ slightly reduces with T, whereas other studies report a temperature-independent $V_{\rm TH}$ transient on the same time scale [5], [7], [11]. This trend, as explained in Section IV, is caused by the charge trapping and emission processes, which govern the fast PBTI $V_{\rm TH}$ time dependency. At longer stress times ($t > 1$ s), the $V_{\rm TH}$ shift computed by subtracting the contribution due to the fast PBTI component, $\Delta V_{{\rm TH},L} = V_{\rm TH}(t) - V_{\rm TH}(t_0 = 1s)$, is shown to increase with T in the inset in Fig. 3, consistent with [5], [7], and [11].

The $V_{\rm TH}$ trends observed at short (fast PBTI) and long (slow PBTI) stress times are analyzed separately in Section IV.

TABLE I
MATERIAL SIMULATION PARAMETERS

Parameter	SiO_X IL	HfO_2
Electron affinity	0.95eV	2.4eV
Band gap	8.9eV	5.8eV
Relative permittivity	6.6	21
Electron effective mass	$0.5m_0$	$0.3m_0$
Phonon effective energy ($\hbar\omega_0$)	0.06eV	0.07eV

TABLE II
DEFECT SIMULATION PARAMETERS

Parameter	SiO_X IL	HfO_2
ρ	$5{\cdot}10^{19}{\cdot}$d	$1{\cdot}10^{20}cm^{-3}$
r_T	2A	2A
E_T	2.6±0.3eV	1.35±0.25eV
E_{REL}	0.36±0.18eV	1.19±0.3eV

ρ is the average trap density; r_T is the trap radius; E_T is the thermal ionization energy to the conduction band; E_{REL} is the relaxation energy, d is the distance from Si/IL interface [nm]. Both E_T and E_{REL} are random variables uniformly distributed between the indicated ranges.

IV. $V_{\rm TH}$ SHIFT SIMULATION RESULTS

The charge-trapping model described in Section II is used to simulate the $V_{\rm TH}$ shift measured under transient (<1 s) and ac conditions by considering a single set of material and trap parameters for the electron traps (Tables I and II). The trap parameters are consistent with those derived from *ab initio* calculations for negatively and positively charged oxygen vacancy defects in SiO_2 and HfO_2, respectively [27], [28]. We consider that the defect density in the SiO_x IL increases linearly approaching the SiO_x/HfO_2 interface, in agreement with charge-pumping measurements [29] and leakage-current simulations [19]. In the HfO_2 film, defects are considered to be uniformly distributed.

A. V_{TH} Shift Observed During the Application of a V_G Pulse

Fig. 4 shows the $V_{\rm TH}$ shift transients measured and simulated by applying different gate voltages to a 1-nm IL/5-nm HfO_2 stack. A higher V_G induces a larger final $\Delta V_{\rm TH}$ because it allows filling deeper traps and a significantly faster transient, i.e., $V_{\rm TH}$ reaches saturation in shorter times. As shown in Fig. 5, the traps responsible of the $V_{\rm TH}$ shift are mostly located in the HfO_2 region close to the SiO_x interface. Consistently, the $\Delta V_{\rm TH}$ simulations performed by considering the defects in the SiO_x interfacial layer only (see the dashed lines in Fig. 4) fail in reproducing the measured $V_{\rm TH}$ shift, confirming the role played by HfO_2 defects [9].

To further investigate the contribution played by the two layers in the high-κ gate-stack, we simulated the $V_{\rm TH}$ shifts in a stack with a thicker (7 nm) HfO_2 (Fig. 6). The applied gate voltages induce the same electric fields considered for the 5-nm HfO_2 stack case. Despite the same electric fields, the $V_{\rm TH}$ shift is considerably larger in the stack with thicker HfO_2. The simulation of the $V_{\rm TH}$ shift in both stacks (performed by considering the same defect parameters reported in Table II) confirms the validity of the modeling approach, which allows identifying the contributions of IL and HfO_2 defects to the overall $V_{\rm TH}$ shift.

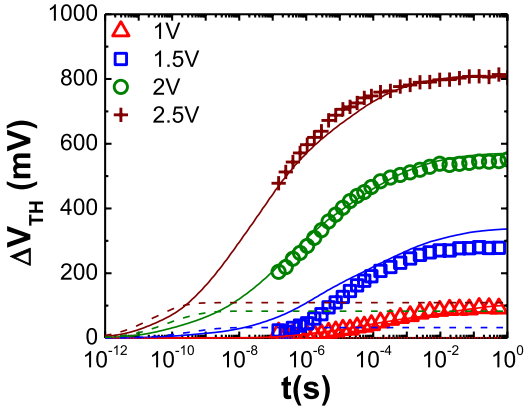

Fig. 4. ΔV_{TH} versus time measured (symbols) and simulated (solid lines) at different voltages at 300 K on the 1-nm IL/5-nm HfO_2 stack. The ΔV_{TH} transients simulated ignoring the traps in the HfO_2 film (dashed lines) are also shown for comparison.

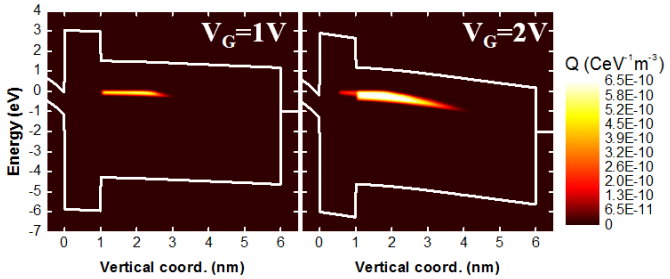

Fig. 5. Band diagram plot illustrating the simulated space-energy distribution of the trapped charge in steady-state conditions at $V_G = 1$ V and $V_G = 2$ V in the 1-nm IL/5-nm HfO_2 stack.

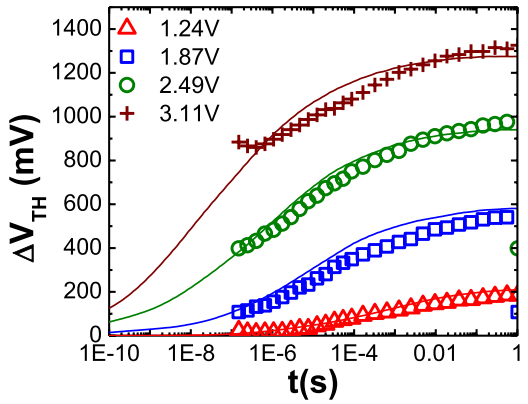

Fig. 6. ΔV_{TH} versus time measured (symbols) and simulated (solid lines) at different stress voltages at 300 K, in the 1-nm IL/7-nm HfO_2 stack.

We investigated the trend of the fast V_{TH} shift component with the scaling of HfO_2/IL stacks. Fig. 7 shows the measured and simulated fast ΔV_{TH} component at saturation (i.e., ~1 s) plotted versus the HfO_2 thickness in 1-nm-IL/HfO_2 stacks. The fast ΔV_{TH} component reduces in thinner HfO_2 stacks. The simulation projection indicates that the fast PBTI component should completely disappear for the HfO_2 thicknesses below 1.5 nm because the higher emission rates strongly reduce the defect occupation probability. The V_{TH} shift transient spans over several decades in time (i.e., from ps to ms, as shown in Figs. 4 and 6), indicating a very wide distribution of the electron input rates R_{in}. This is due to the random distribution of the defect properties: the trap distance from the

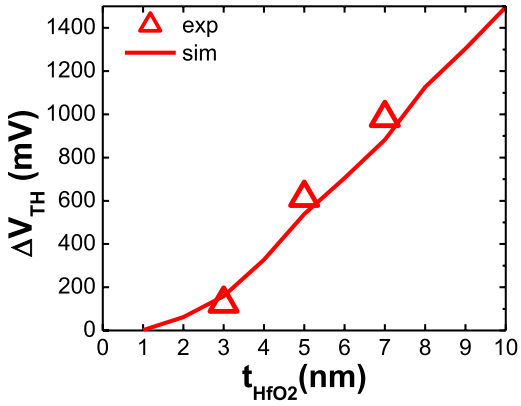

Fig. 7. Measured (symbols) and simulated (solid lines) ΔV_{TH} at saturation versus HfO_2 thickness (in a 1-nm SiO_x IL-HfO_2 stack) at the stress voltages corresponding to an equivalent field (V_G/EOT) of 13.2 MV/cm, i.e., 7.78 MV/cm for the SiO_x IL and 2.44 MV/cm for the HfO_2.

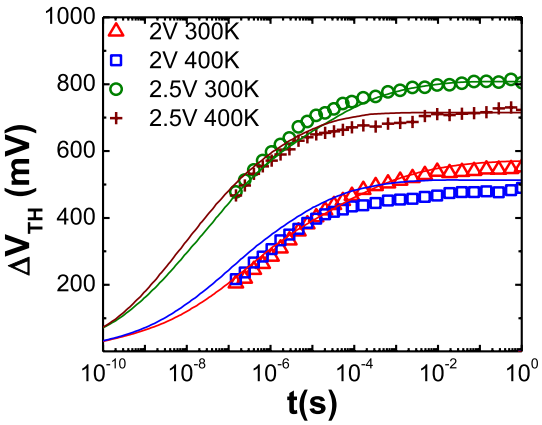

Fig. 8. ΔV_{TH} versus time measured (symbols) and simulated (solid lines) in the 1-nm IL/5-nm HfO_2 stack at $V_G = 2$, 2.5 V and $T = 300$, 400 K.

substrate interface controls the tunneling probability, while the thermal ionization and relaxation energies affect the phonon assisted capture and emission time constants [17]. Due to the amorphous/polycrystalline nature of the dielectric layers, we considered that such energies are distributed around certain average values (Table II) related to their atomistic nature [19].

B. Temperature Dependence of Fast V_{TH} Shift

Fig. 8 shows the V_{TH} shifts measured and simulated at two different temperatures on the 1-nm IL/5-nm HfO_2 stack. The ΔV_{TH} steady-state value decreases slightly with T. This trend, not reported previously, is observed only for the fast PBTI component, and it is due to the different temperature dependence of the charge trapping and emission processes, which are correctly reproduced by the model. A deeper understanding of this phenomena can be achieved with the help of Fig. 9, which shows the steady-state trap occupancy $F_{T,SS}$, and the input and output rates (R_{in} and R_{out}) calculated at $V_G = 2$V, $T = 300$K and 400K for a HfO_2 trap, as a function of its distance (z) from the SiO_x interface. R_{in}, which is determined by the electron capture by the trap, decreases as the trap position approaches the gate. On the other hand, R_{out}, which is dominated by the electron emission to the gate (the emission back to the substrate is also considered

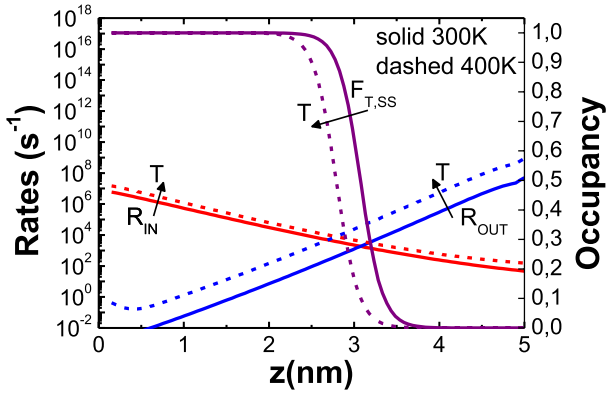

Fig. 9. Input, R_{in}, and output, R_{out}, rates and steady-state occupancy, $F_{T,SS}$, at $T = 300$ K (solid lines) and $T = 400$ K (dashed lines), calculated for a HfO_2 trap located at the distance z from the IL interface in the IL/5-nm HfO_2 stack. The thermal ionization energy is $E_T = 1.4$ eV, while the other trap parameters are reported in Table II.

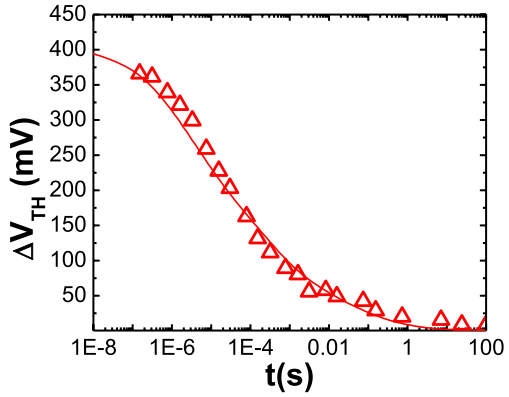

Fig. 10. Measured (symbols) and simulated (solid lines) ΔV_{TH} versus time at zero-bias and 300 K, after a 2 V/1-s stress pulse on the 1-nm IL/3-nm HfO_2 stack.

by the model), follows the opposite trend with z. According to (7), the steady-state trap occupancy $F_{T,\text{SS}}$ approaches 1 (i.e., trap filled) when $R_{\text{in}} \gg R_{\text{out}}$. This condition holds for the HfO_2 region closer to the IL interface, Fig. 9, which is filled by electrons and determines the V_{TH} shift. The electron capture and emission are both thermally activated processes: the lattice displacement accompanying the charge trapping and emission requires to overcome energy barriers, i.e., $E_{\text{ACT,IN}}$ and $E_{\text{ACT,OUT}}$, respectively. $E_{\text{ACT,IN}}$ is lower than $E_{\text{ACT,OUT}}$ because the electron energy dissipated at the trap sites (due to the misalignment between the substrate Fermi level and the trap state) reduces the energy barrier associated to the capture process. The higher R_{out} enhancement with T results in a significant decrease of the region, where $F_{T,\text{SS}} \cong 1$, Fig. 9, causing the reduction of the steady-state ΔV_{TH} with T.

C. Simulations of V_{TH} Recovery

We used the above model to simulate the V_{TH} recovery. Fig. 10 shows the V_{TH} recovery transient measured and simulated on the 1-nm IL/3-nm HfO_2 stack after a $V_G = 2$ V/1-s pulse. Simulations are performed using the same defect parameters adopted to describe the V_{TH} increase. The emission of the trapped charge occurring when the voltage is removed (i.e., $V_G = 0$ V) reproduces accurately the experimental ΔV_{TH} recovery kinetics. The wide distribution of the emission time constants observed in the recovery transient [8] is caused by the random distributions of the trap spatial positions and energies, as reported in Table II.

D. Simulations of V_{TH} Under AC Stress Conditions

The charge-trapping model is used also to simulate the V_{TH} shift while applying an ac voltage stress. Fig. 11(a) shows the ΔV_{TH} transient measured and simulated on the 1-nm IL/5-nm HfO_2 stack under the square-wave voltage stress of different duty cycles. Simulations reproduce the V_{TH} increase over time and its dependency on the duty cycles. The simulations reproduce also the dependency of ΔV_{TH} at saturation on the duty cycles at different voltage pulse amplitudes, as shown in Fig. 11(b) [30], [31]. AC stresses performed at different

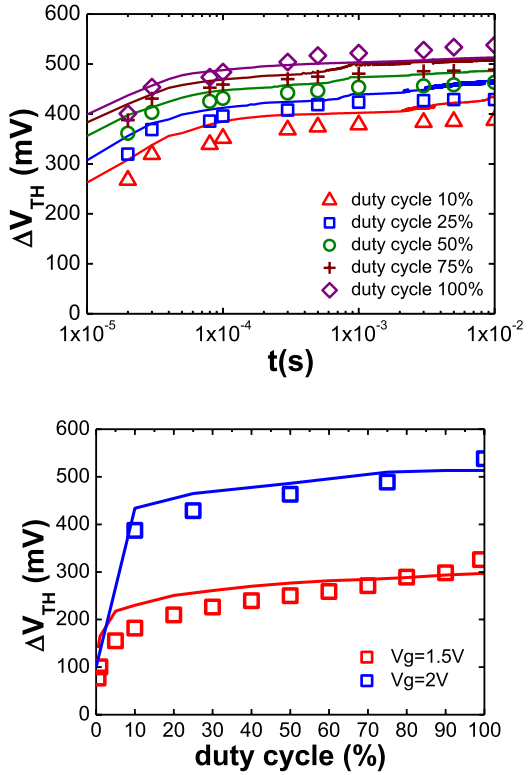

Fig. 11. (a) ΔV_{TH} measured (symbols) and simulated (solid lines) in the 1-nm IL/5-nm HfO_2 stack under ac square-wave voltage stresses. (a) ΔV_{TH} versus time at different duty cycles and min/max amplitudes of 0/2 V, at 300 K and 10 KHz. (b) ΔV_{TH} at saturation versus the duty cycle at 300 K and 100 KHz, considering two different max amplitudes of 1.5 and 2 V. Simulations were performed by considering the defect parameters reported in Table II.

frequency (in the range 10 KHz–1 MHz) do not show any significant frequency dependency on the V_{TH} shift, as correctly demonstrated by the simulations (the data are not shown for brevity).

E. Correlation Between V_{TH} Shift and Leakage Current

To understand whether the same defects involved in the fast V_{TH} shift are responsible also for the leakage current through the dielectric stack, which was shown to be governed by the TAT charge transport process [19], [32], we simulated the dc gate current through the 1-nm IL/5-nm HfO_2 stack by using

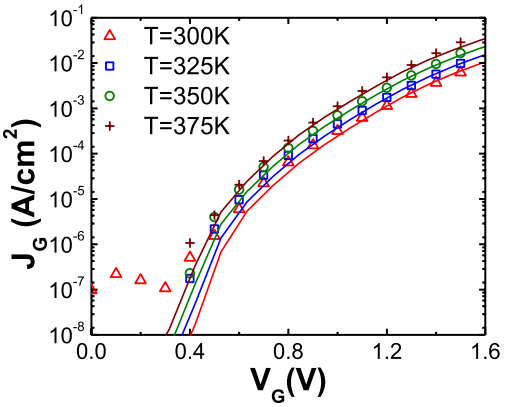

Fig. 12. Measured (symbols) and simulated (solid lines) gate current densities J_G–V_G curves at different temperatures in the 1-nm IL/5-nm HfO_2 stack.

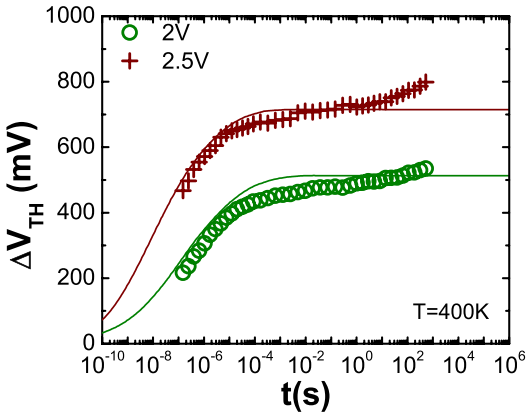

Fig. 13. ΔV_{TH} versus time measured (symbols) and simulated (lines) on the 1-nm IL/5-nm HfO_2 stack at 400 K at different V_G. Simulations are performed by considering the defects responsible for fast threshold voltage shift.

the same set of defect parameters considered in the V_{TH} shifts simulations. The I_G current is calculated using (6) at the dc limit (i.e., $t \rightarrow \infty$). The agreement between the simulated and the experimental gate currents at different temperatures in Fig. 12 confirms that the same defect type is responsible for both the fast V_{TH} shift and the leakage current on these stacks.

F. Long-Time V_{TH} Shift Component

We employed the charge-trapping model described in Section II to simulate the stress time-dependent V_{TH} increase observed on a longer time scale (>1 s). As shown in Fig. 13, the V_{TH} versus time curves simulated by considering the defect parameters corresponding to O vacancies (Table II) cannot describe the long-term V_{TH} increase, as they saturate within ~1 s. We used the model to verify whether the charge trapping at defects of different natures could be responsible of this V_{TH} increase. We found that to reproduce the low rate of the long-term V_{TH} increase, the defects have to exhibit a very high relaxation energy, not associated with known defect configurations in SiO_2 and HfO_2. This seems to exclude the possibility that a charge trapping process alone is responsible for the slow ΔV_{TH} shift. However, this does not exclude that a more complex physical process involving charge trapping at traps generated by the voltage stress could be responsible for the long-term V_{TH} increase. In this framework, the process leading to the generation of new defects should dominate the dynamics of the process, being responsible of the slow rate of the V_{TH} increase. This process should be due to a reversible mechanism, as a significant recovery takes place after the removal of the voltage stress. This excludes physical mechanisms related to the irreversible structural modification of the lattice typical of hard dielectric breakdown [33], [34]. Instead, the defect generation might be related to either the diffusion of atomic species such as H and O upon the voltage application, or the activation of defect precursors present within the dielectric, which can be due to a change of the defect configuration occurring via a metastable state upon trapping electrons [14] or electric-field and thermal-assisted defect transformation [15]. All the above options require deep investigation and independent confirmation from material structural modeling.

V. Conclusion

The V_{TH} shift observed on $SiO_x/HfO_2/TiN$ gate-stacks is described by a capture/emission model, which includes electron tunneling to/from the trap and electron-phonon coupling occurring at the trap site. Simulations of the charge trapping/emission at preexisting defects successfully reproduce the voltage and temperature dependency of the fast component of the V_{TH} shift (<1 s) and the subsequent V_{TH} recovery in high-k/metal gate dielectric stacks. The parameters employed for the traps in the SiO_2 IL and HfO_2 are consistent with those calculated for the oxygen vacancy defects, which were shown to assist the leakage current through the same stacks. Simulations reveal also that the long-term component of the V_{TH} shift cannot be described by a simple charge trapping process into known defect configurations in SiO_2 and HfO_2. A mechanism involving a stress-induced activation or generation of new defects is required to describe the slow rate of the long-term V_{TH} shift.

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