TEXAS INSTRUMENTS

LMK61E2-100M, LMK61E2-125M, LMK61E2-156M, LMK61E2-312M
LMK61A2-100M, LMK61A2-125M, LMK61A2-156M, LMK61A2-312M, LMK61I2-100M

SNAS676A – OCTOBER 2015 – REVISED NOVEMBER 2015

LMK61XX High-Performance Ultra-Low Jitter Oscillator

1 Features

- Ultra-low Noise, High Performance
  - Jitter: 90 fs RMS typical Fout > 100 MHz
  - PSRR: -70 dBc, robust supply noise immunity
- Supported Output Format
  - LVPECL up to 1 GHz
  - LVDS up to 900 MHz
  - HCSL up to 400 MHz
- Total Frequency Tolerance of ± 50 ppm
- 3.3 V Operating Voltage
- Industrial Temperature Range (-40ºC to +85ºC)
- 7 mm x 5 mm 6-pin Package that is Pin-compatible with Industry Standard 7050 XO Package

2 Applications

- High-Performance Replacement for Crystal-, SAW-, or Silicon-based Oscillators
- Switches, Routers, Network Line Cards, Base Band Units (BBU), Servers, Storage/SAN
- Test and Measurement
- Medical Imaging
- FPGA, Processor Attach

3 Description

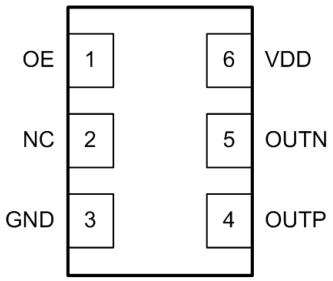
The LMK61XX is an ultra-low jitter oscillator that generates a commonly used reference clock. The device is pre-programmed in factory to support any reference clock frequency; supported output formats are LVPECL up to 1 GHz, LVDS up to 900 MHz, and HCSL up to 400 MHz. Internal power conditioning provide excellent power supply ripple rejection (PSRR), reducing the cost and complexity of the power delivery network. The device operates from a single 3.3 V ± 5% supply.

Device Information(1)

PART NUMBER	OUTPUT FREQ (MHz) AND FORMAT	PACKAGE	BODY SIZE (NOM)
LMK61A2-100M00SIA	100 LVDS	6-pin QFM	7.0 mm x 5.0 mm
LMK61A2-125M00SIA	125 LVDS		
LMK61A2-156M25SIA	156.25 LVDS		
LMK61A2-312M50SIA	312.5 LVDS		
LMK61E2-100M00SIA	100 LVPECL		
LMK61E2-125M00SIA	125 LVPECL		
LMK61E2-156M25SIA	156.25 LVPECL		
LMK61E2-312M50SIA	312.5 LVPECL		
LMK61I2-100M00SIA	100 HCSL		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Pinout



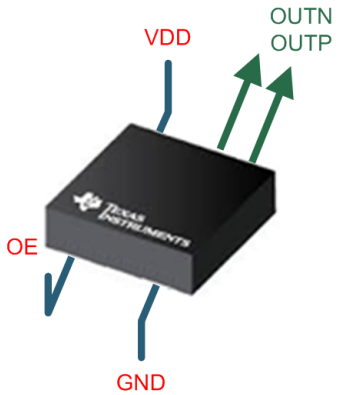


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2015) to Revision A	Page
• Product Preview to Production Data Datasheet	1

5 Pin Configuration and Functions

SIA Package
6 pin QFM

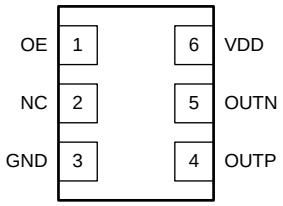


Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
POWER			
GND	3	Ground	Device Ground.
VDD	6	Analog	3.3 V Power Supply.
OUTPUT BLOCK			
OUTP, OUTN	4, 5	Universal	Differential Output Pair (LVPECL, LVDS or HCSL).
DIGITAL CONTROL / INTERFACES			
NC	2	N/A	No Connect.
OE	1	LVCMOS	Output Enable (internal pullup). When set to low, output pair is disabled and set at high impedance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD	Device Supply Voltage	-0.3	3.6	V
V_{IN}	Output Voltage Range for Logic Inputs	-0.3	VDD + 0.3	V
V_{OUT}	Output Voltage Range for Clock Outputs	-0.3	VDD + 0.3	V
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device Supply Voltage	3.135	3.3	3.465	V

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Ambient Temperature	-40	25	85	°C
T_J	Junction Temperature			125	°C
t_{RAMP}	VDD Power-Up Ramp Time	0.1		100	ms

6.4 Thermal Information

THERMAL METRIC(1)		LMK61XX (2) (3) (4) QFM (SIA) 6 PINS			UNIT
		Airflow (LFM) 0	Airflow (LFM) 200	Airflow (LFM) 400	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.2	46.4	43.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.6	n/a	n/a	
$R_{\theta JB}$	Junction-to-board thermal resistance	37.7	n/a	n/a	
ψ_{JT}	Junction-to-top characterization parameter	11.3	17.6	22.5	
ψ_{JB}	Junction-to-board characterization parameter	37.7	41.5	40.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal resistance is calculated on a 4 layer JEDEC board.
(3) Connected to GND with 3 thermal vias (0.3-mm diameter).
(4) ψJB (junction to board) is used when the main heat flow is from the junction to the GND pad. Please refer to Thermal Considerations section for more information on ensuring good system reliability and quality.

6.5 Electrical Characteristics - Power Supply(1)

VDD = 3.3 V ± 5%, T_A = -40C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Device Current Consumption	LVPECL(2)		162	208	mA
		LVDS		152	196	
		HCSL		155	196	
IDD-PD	Device Current Consumption when output is disabled	OE = GND		136		

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) On-chip power dissipation should exclude 40 mW, dissipated in the 150 ohm termination resistors, from total power dissipation.

6.6 LVPECL Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output Frequency(2)		10		1000	MHz
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})(2)		700	800	1200	mV
$V_{OUT, DIFF, PP}$	Differential Output Peak-to-Peak Swing			2 x $\lvert V_{OD}\rvert$		V
V_{OS}	Output Common Mode Voltage			VDD – 1.55		V
t_R / t_F	Output Rise/Fall Time (20% to 80%)(3)			120	200	ps
PN-Floor	Output Phase Noise Floor (f_{OFFSET} > 10 MHz)	156.25 MHz		-165		dBc/Hz

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(3) Ensured by characterization.

LVPECL Output Characteristics(1) (continued)

VDD = 3.3 V ± 5%, T_A = -40C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ODC	Output Duty Cycle(3)		45%		55%	

6.7 LVDS Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output Frequency(1)		10		900	MHz
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})(1)		300	390	480	mV
$V_{OUT, DIFF, PP}$	Differential Output Peak-to-Peak Swing			2 x $\|V_{OD}\|$		V
V_{OS}	Output Common Mode Voltage			1.2		V
t_R / t_F	Output Rise/Fall Time (20% to 80%)(2)			150	250	ps
PN-Floor	Output Phase Noise Floor (f_{OFFSET} > 10 MHz)	156.25 MHz		-162		dBc/Hz
ODC	Output Duty Cycle(2)		45%		55%	
R_{OUT}	Differential Output Impedance			125		Ohm

(1) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(2) Ensured by characterization.

6.8 HCSL Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output Frequency		10		400	MHz
V_{OH}	Output High Voltage		600		850	mV
V_{OL}	Output Low Voltage		-100		100	mV
V_{CROSS}	Absolute Crossing Voltage(2)(3)		250		475	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS}(2)(3)		0		140	mV
dV/dt	Slew Rate(4)		0.8		2	V/ns
PN-Floor	Output Phase Noise Floor (f_{OFFSET} > 10 MHz)	100 MHz		-164		dBc/Hz
ODC	Output Duty Cycle(4)		45%		55%	

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) Measured from -150 mV to +150 mV on the differential waveform with the 300 mVpp measurement window centered on the differential zero crossing.
(3) Ensured by design.
(4) Ensured by characterization.

6.9 OE Input Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage		1.4			V
V_{IL}	Input Low Voltage				0.6	V
I_{IH}	Input High Current	V_{IH} = VDD	-40		40	uA
I_{IL}	Input Low Current	V_{IL} = GND	-40		40	uA
C_{IN}	Input Capacitance			2		pF

6.10 Frequency Tolerance Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_T	Total Frequency Tolerance	All output formats, frequency bands and device junction temperature up to 125°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and aging (10 years)	-50		50	ppm

(1) Ensured by characterization.

6.11 Power-On/Reset Characteristics (VDD)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{THRESH}	Threshold Voltage(1)		2.72		2.95	V
V_{DROOP}	Allowable Voltage Droop(2)				0.1	V
$t_{STARTUP}$	Startup Time (1)	Time elapsed from VDD at 3.135 V to output enabled			10	ms
t_{OE-EN}	Output enable time(2)	Time elapsed from OE at V_{IH} to output enabled			50	us
t_{OE-DIS}	Output disable time(2)	Time elapsed from OE at V_{IL} to output disabled			50	us

(1) Ensured by characterization.
(2) Ensured by design.

6.12 PSRR Characteristics(1)

VDD = 3.3 V, T_A = 25°C, FS[1:0] = NC, NC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Spurs Induced by 50 mV Power Supply Ripple(2)(3) at 156.25 MHz output, all output types	Sine wave at 50 kHz		-70		dBc
		Sine wave at 100 kHz		-70		
		Sine wave at 500 kHz		-70		
		Sine wave at 1 MHz		-70		

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) Measured max spur level with 50 mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD pin
(3) DJ_{SPUR} (ps, pk-pk) = [2*10(SPUR/20) / (π*f_{OUT})]*1e6, where PSRR or SPUR in dBc and f_{OUT} in MHz.

6.13 PLL Clock Output Jitter Characteristics(1)(2)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ	RMS Phase Jitter(3) (12 kHz – 20 MHz) (1 kHz – 5 MHz)	f_{OUT} ≥ 100 MHz, Integer-N PLL, All output types		100	200	fs RMS

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).
(3) Ensured by characterization.

6.14 Typical 156.25 MHz Output Phase Noise Characteristics(1)(2)

VDD = 3.3 V, T_A = 25°C, Output Type = LVPECL/LVDS/HCSL

SYMBOL	PARAMETER	OUTPUT TYPE			UNITS
		LVPECL	LVDS	HCSL	
phn_{10k}	Phase noise at 10 kHz offset	-143	-143	-143	dBc/Hz
Phn_{20k}	Phase noise at 20 kHz offset	-143	-143	-143	dBc/Hz
phn_{100k}	Phase noise at 100 kHz offset	-144	-144	-144	dBc/Hz
Phn_{200k}	Phase noise at 200 kHz offset	-145	-145	-145	dBc/Hz

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).

Typical 156.25 MHz Output Phase Noise Characteristics[1][2] (continued)

VDD = 3.3 V, T_A = 25°C, Output Type = LVPECL/LVDS/HCSL

SYMBOL	PARAMETER	OUTPUT TYPE			UNITS
		LVPECL	LVDS	HCSL	
phn_{1M}	Phase noise at 1 MHz offset	-150	-150	-150	dBc/Hz
phn_{2M}	Phase noise at 2 MHz offset	-154	-154	-154	dBc/Hz
phn_{10M}	Phase noise at 10 MHz offset	-165	-162	-164	dBc/Hz
phn_{20M}	Phase noise at 20 MHz offset	-165	-162	-164	dBc/Hz

6.15 Additional Reliability and Qualification

PARAMETER	CONDITION / TEST METHOD
Mechanical Shock	MIL-STD-202, Method 213
Mechanical Vibration	MIL-STD-202, Method 204
Moisture Sensitivity Level	J-STD-020, MSL3

6.16 Typical Performance Characteristics

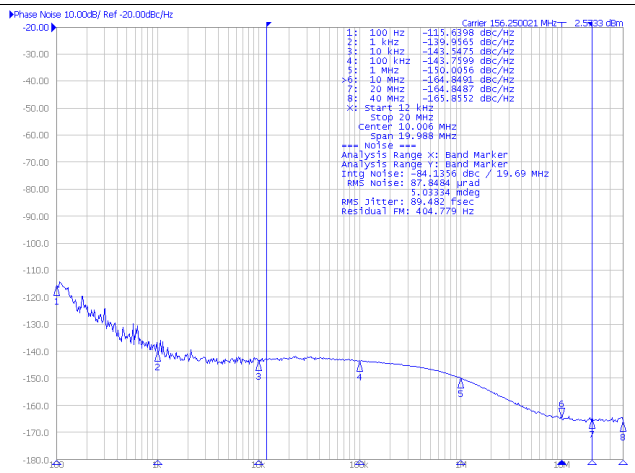


Figure 1. Phase Noise of 156.25 MHz LVPECL Differential Output

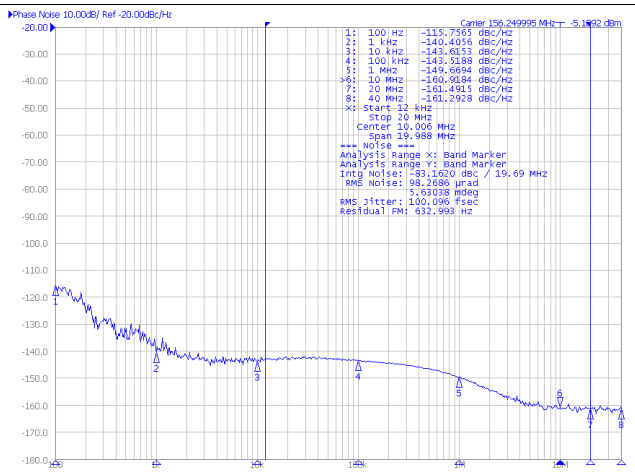


Figure 2. Phase Noise of 156.25 MHz LVDS Differential Output

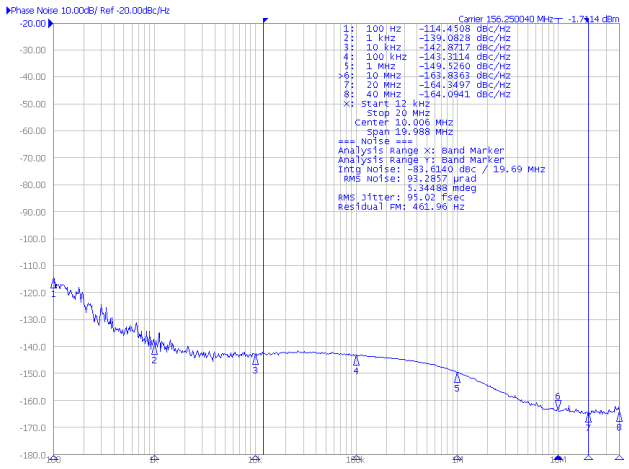


Figure 3. Phase Noise of 156.25 MHz HCSL Differential Output

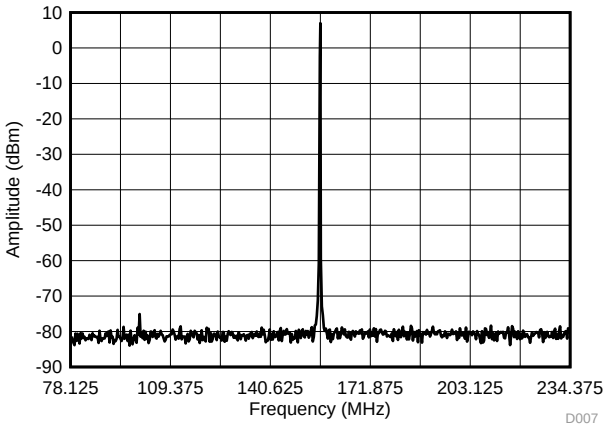


Figure 4. 156.25 ± 78.125 MHz LVPECL Differential Output Spectrum

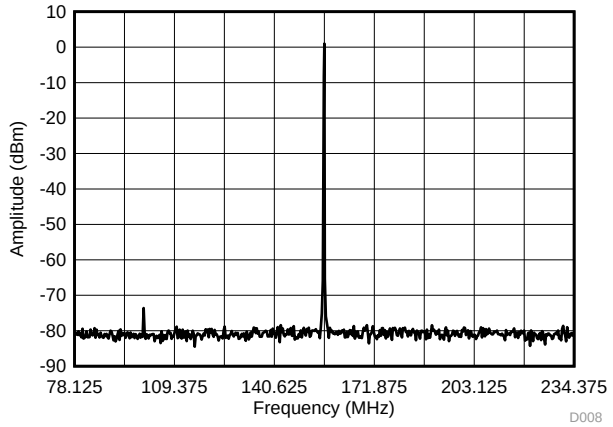


Figure 5. 156.25 ± 78.125 MHz LVDS Differential Output Spectrum

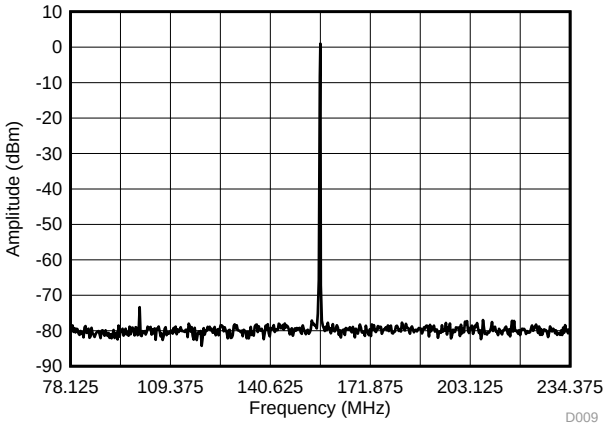


Figure 6. 156.25 ± 78.125 MHz HCSL Differential Output Spectrum

Typical Performance Characteristics (continued)

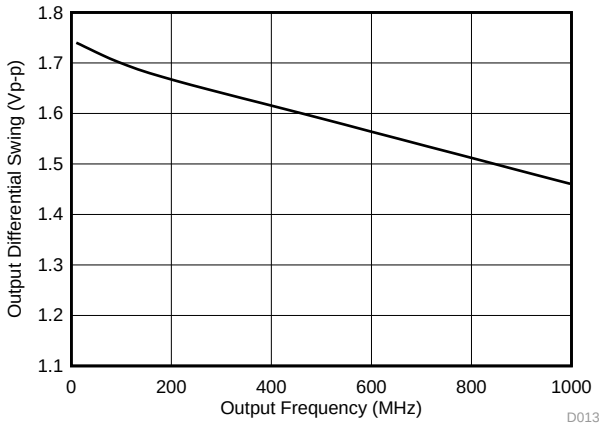


Figure 7. LVPECL Differential Output Swing vs Frequency

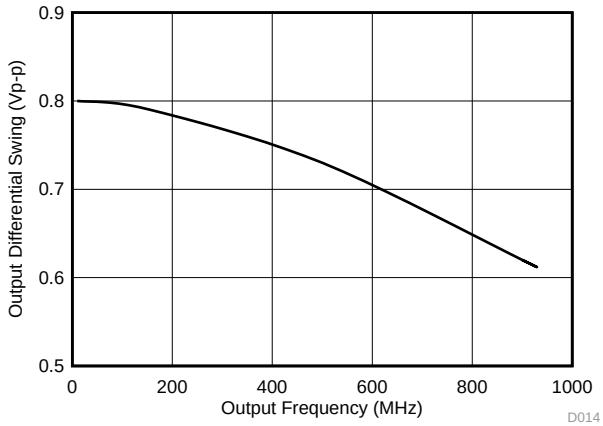


Figure 8. LVDS Differential Output Swing vs Frequency

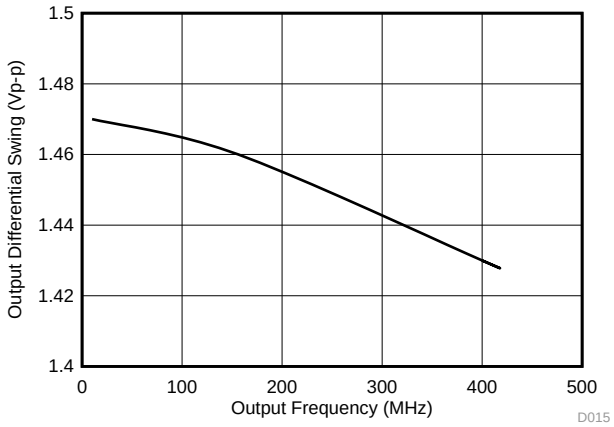


Figure 9. HCSL Differential Output Swing vs Frequency

7 Parameter Measurement Information

7.1 Device Output Configurations

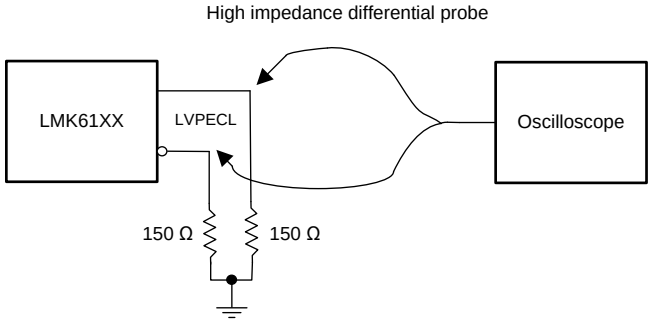


Figure 10. LVPECL Output DC Configuration during Device Test

Device Output Configurations (continued)

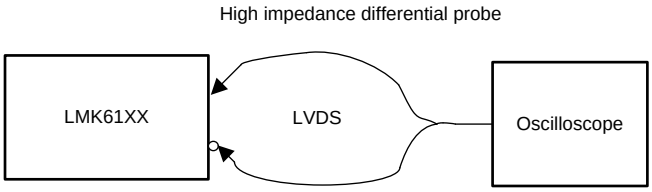


Figure 11. LVDS Output DC Configuration during Device Test

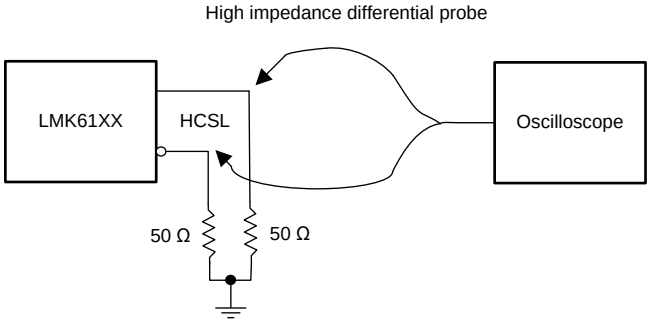


Figure 12. HCSL Output DC Configuration during Device Test

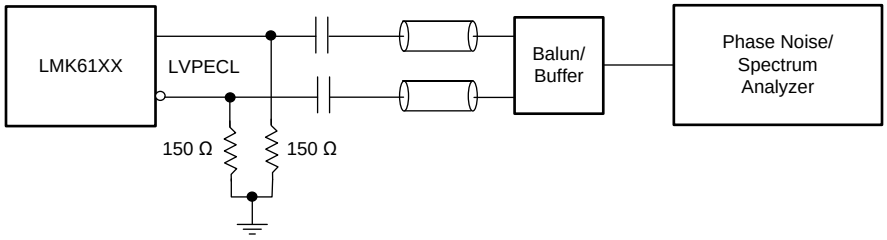


Figure 13. LVPECL Output AC Configuration during Device Test

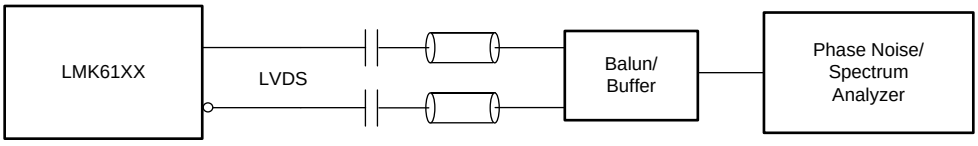


Figure 14. LVDS Output AC Configuration during Device Test

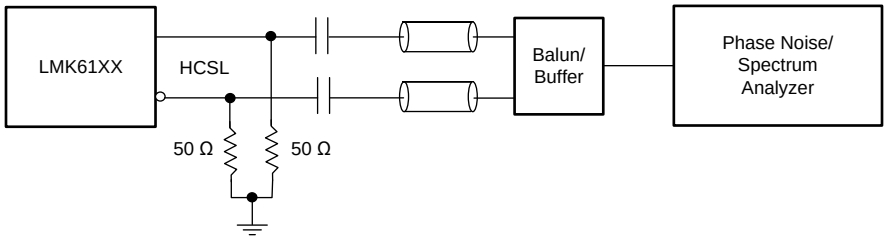


Figure 15. HCSL Output AC Configuration during Device Test

Device Output Configurations (continued)

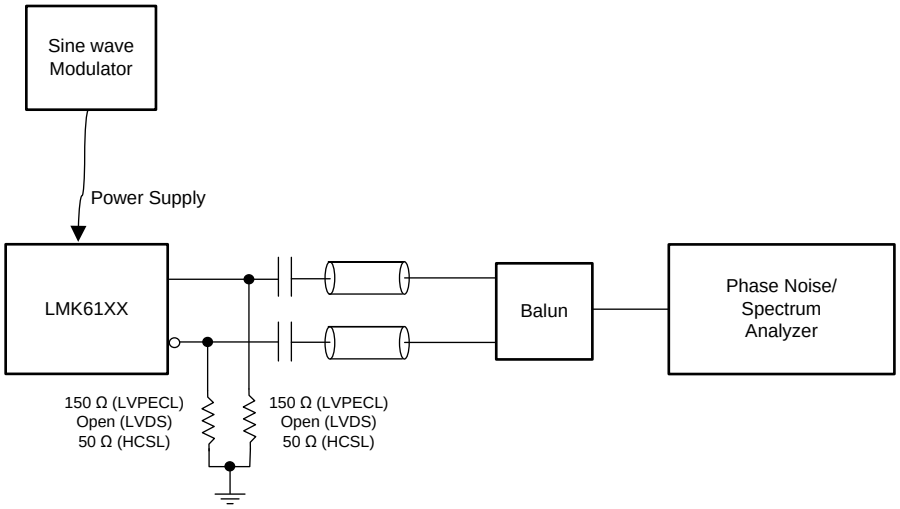


Figure 16. PSRR Test Setup

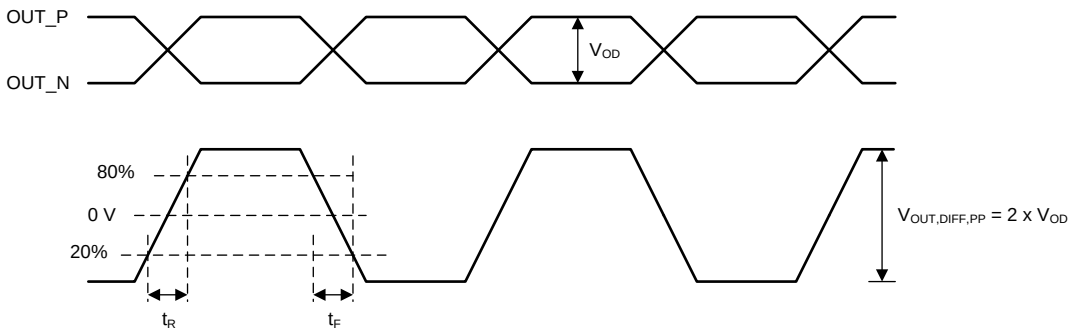


Figure 17. Differential Output Voltage and Rise/Fall Time

8 Power Supply Recommendations

For best electrical performance of LMK61XX, it is preferred to utilize a combination of 10 uF, 1 uF and 0.1 uF on its power supply bypass network. It is also recommended to utilize component side mounting of the power supply bypass capacitors and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. Figure 18 shows the layout recommendation for power supply decoupling of LMK61XX.

9 Layout

9.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile and power supply bypassing when using LMK61XX to ensure good thermal / electrical performance and overall signal integrity of entire system.

9.1.1 Ensuring Thermal Reliability

The LMK61XX is a high performance device. Therefore careful attention must be paid to device configuration and printed circuit board (PCB) layout with respect to power consumption. The ground pin needs to be connected to the ground plane of the PCB through three vias or more, as shown in Figure 18, to maximize thermal dissipation out of the package.

Equation 1 describes the relationship between the PCB temperature around the LMK61XX and its junction temperature.

$$T_B = T_J - \Psi_{JB} * P \quad (1)$$

where

- T_B: PCB temperature around the LMK61XX
- T_J: Junction temperature of LMK61XX
- Ψ_{JB}: Junction-to-board thermal resistance parameter of LMK61XX (37.7°C/W without airflow)
- P: On-chip power dissipation of LMK61XX

In order to ensure that the maximum junction temperature of LMK61XX is below 125°C, it can be calculated that the maximum PCB temperature without airflow should be at 99°C or below when the device is optimized for best performance resulting in maximum on-chip power dissipation of 0.68 W.

9.1.2 Best Practices for Signal Integrity

For best electrical performance and signal integrity of entire system with LMK61XX, it is recommended to route vias into decoupling capacitors and then into the LMK61XX. It is also recommended to increase the via count and width of the traces wherever possible. These steps ensure lowest impedance and shortest path for high frequency current flow. Figure 18 shows the layout recommendation for LMK61XX.

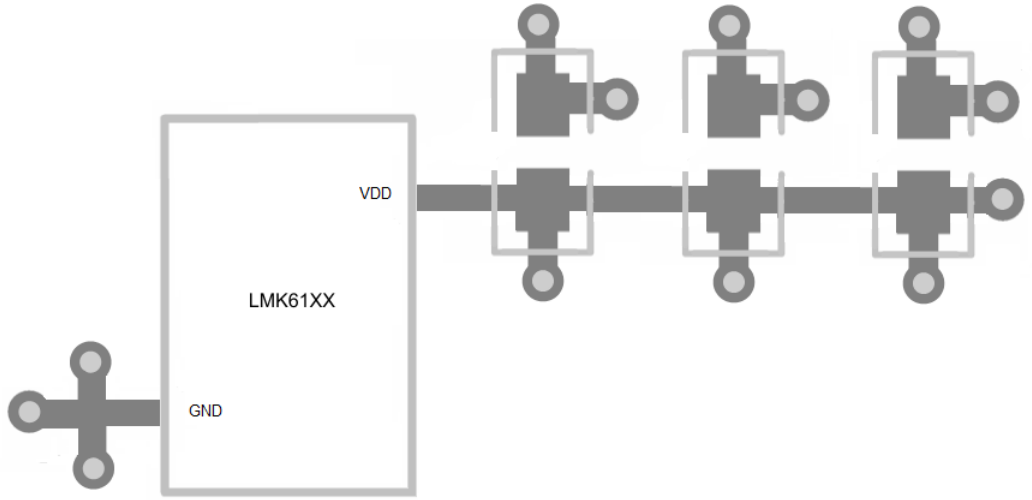


Figure 18. LMK61XX Layout Recommendation for Power Supply and Ground

Layout Guidelines (continued)

9.1.3 Recommended Solder Reflow Profile

It is recommended to follow the solder paste supplier's recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. It is preferrable for the LMK61XX to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well solder manufactures recommended profile, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

10 Device and Documentation Support

10.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMK61E2-100M	Click here	Click here	Click here	Click here	Click here
LMK61E2-125M	Click here	Click here	Click here	Click here	Click here
LMK61E2-156M	Click here	Click here	Click here	Click here	Click here
LMK61E2-312M	Click here	Click here	Click here	Click here	Click here
LMK61A2-100M	Click here	Click here	Click here	Click here	Click here
LMK61A2-125M	Click here	Click here	Click here	Click here	Click here
LMK61A2-156M	Click here	Click here	Click here	Click here	Click here
LMK61A2-312M	Click here	Click here	Click here	Click here	Click here
LMK61I2-100M	Click here	Click here	Click here	Click here	Click here

10.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.3 Trademarks

E2E is a trademark of Texas Instruments.

10.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK61A2-100M00SIAT	PREVIEW	QFM	SIA	6	250	TBD	Call TI	Call TI	-40 to 85		
LMK61A2-125M00SIAT	PREVIEW	QFM	SIA	6	250	TBD	Call TI	Call TI	-40 to 85		
LMK61A2-156M25SIAT	PREVIEW	QFM	SIA	6	250	TBD	Call TI	Call TI	-40 to 85		
LMK61A2-312M50SIAT	PREVIEW	QFM	SIA	6	250	TBD	Call TI	Call TI	-40 to 85		
LMK61E2-100M00SIAR	PREVIEW	QFM	SIA	6	2500	Green (RoHS & no Sb/Br)	Call TI | NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 100M00	
LMK61E2-100M00SIAT	PREVIEW	QFM	SIA	6	250	Green (RoHS & no Sb/Br)	Call TI | NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 100M00	
LMK61E2-125M00SIAR	PREVIEW	QFM	SIA	6	2500	Green (RoHS & no Sb/Br)	Call TI | NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 125M00	
LMK61E2-125M00SIAT	PREVIEW	QFM	SIA	6	250	Green (RoHS & no Sb/Br)	Call TI | NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 125M00	
LMK61E2-156M25SIAR	PREVIEW	QFM	SIA	6	2500	Green (RoHS & no Sb/Br)	Call TI | NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 156M25	
LMK61E2-156M25SIAT	PREVIEW	QFM	SIA	6	250	Green (RoHS & no Sb/Br)	Call TI | NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 156M25	
LMK61E2-312M50SIAR	PREVIEW	QFM	SIA	6	2500	Green (RoHS & no Sb/Br)	Call TI | NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 312M50	
LMK61E2-312M50SIAT	PREVIEW	QFM	SIA	6	250	Green (RoHS & no Sb/Br)	Call TI | NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 312M50	
LMK61I2-100M00SIAT	PREVIEW	QFM	SIA	6	250	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

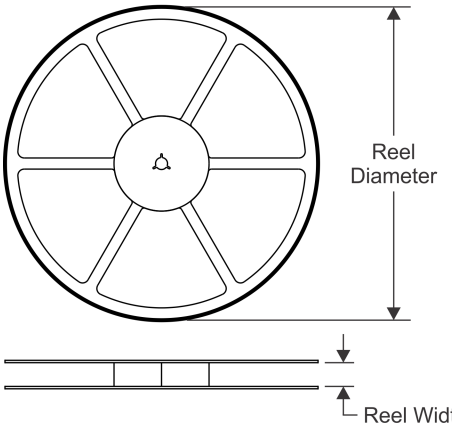
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

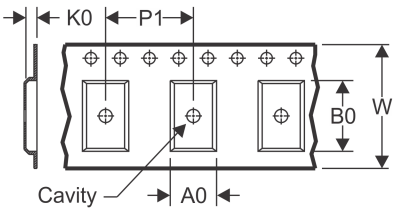
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

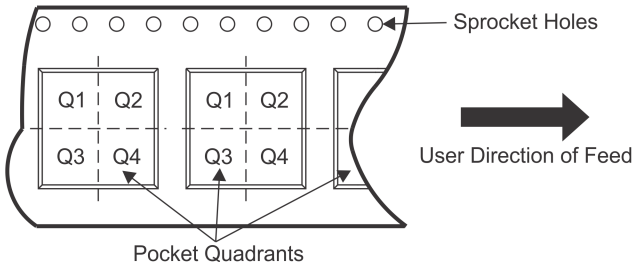


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

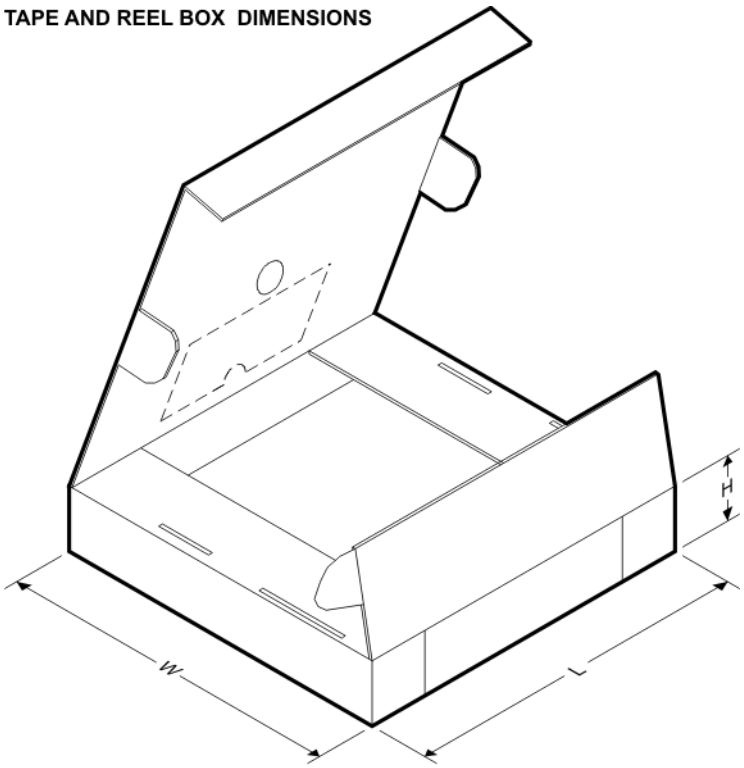
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

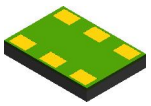
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK61E2-100M00SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2-100M00SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2-125M00SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2-125M00SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2-312M50SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2-312M50SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK61E2-100M00SIAR	QFM	SIA	6	2500	367.0	367.0	38.0
LMK61E2-100M00SIAT	QFM	SIA	6	250	213.0	191.0	55.0
LMK61E2-125M00SIAR	QFM	SIA	6	2500	367.0	367.0	38.0
LMK61E2-125M00SIAT	QFM	SIA	6	250	213.0	191.0	55.0
LMK61E2-312M50SIAR	QFM	SIA	6	2500	367.0	367.0	38.0
LMK61E2-312M50SIAT	QFM	SIA	6	250	213.0	191.0	55.0

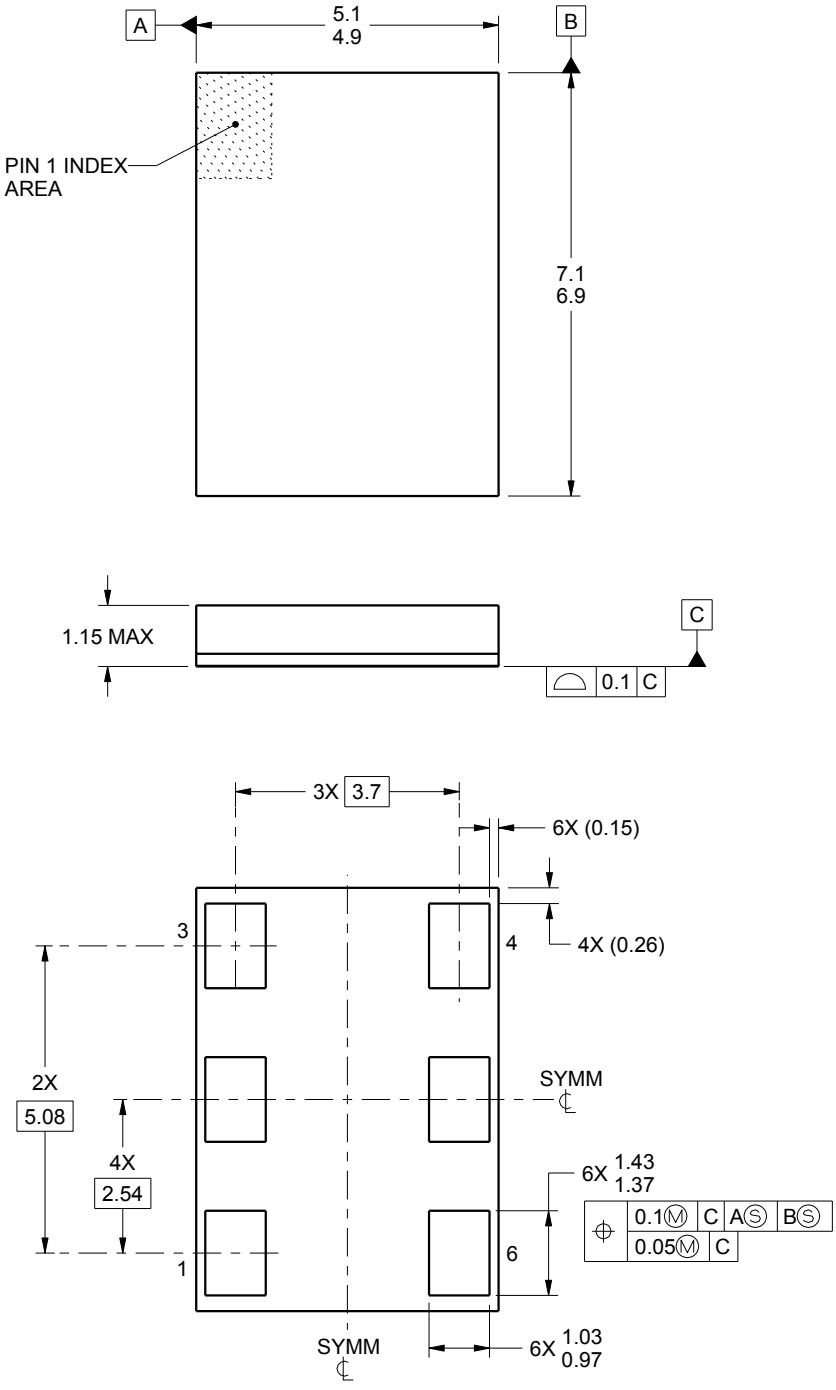


PACKAGE OUTLINE

SIA0006A

QFM - 1.15 mm max height

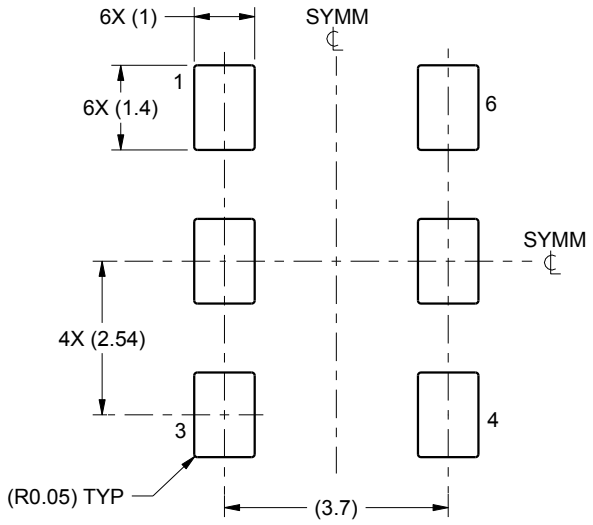
QUAD FLAT MODULE



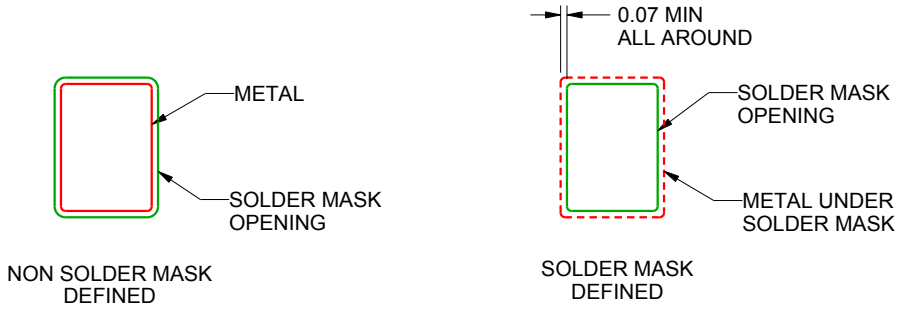
4222361/B 10/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PACKAGE SOLDER PADS
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

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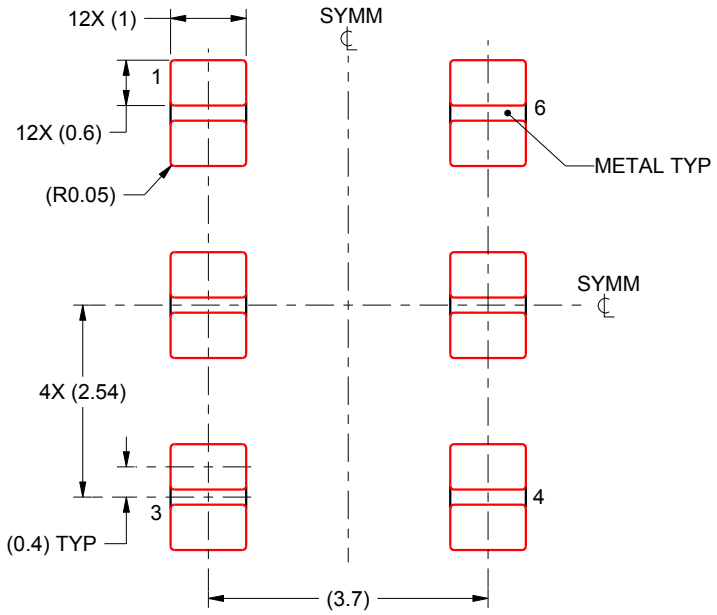
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
ALL PADS: 86%
SCALE:10X

4222361/B 10/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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