Alexander Feng

Sunnyvale, California — afeng42@gatech.edu — (669)-609-0901 — US Citizen

EDUCATION

Georgia Institute of Technology, Atlanta, GA — Expected 2027
B.S. in Electrical Engineering, Minor in Quantum Sciences and Technology, GPA: 4.00

Homestead High School, Cupertino, CA — 2024
Valedictorian, National Merit Finalist, AP Scholar with Distinction, Unweighted GPA: 4.00

SKILLS

Languages: Verilog, SystemVerilog, VHDL, RISC-V, C, Python, MATLAB
Software: Quartus Prime, Synopsys VCS & Verdi, Icarus Verilog, Magic VLSI, Linux (Ubuntu), Git/GitHub
Hardware: Analog Discovery 3, Raspberry Pi, mbed LPC1768, Altera FPGA, Logic Analyzer, Oscilloscope

EXPERIENCE

SiliconJackets, Digital Designer & Design Verification — Fall 2024 – Present
- Wrote SystemVerilog testbenches to verify RTL modules of our custom RISC-V CPU.
- Simulated using Synopsys VCS across test vectors and used Verdi for coverage analysis; over 95% code coverage.
- Designed 32-bit signed/unsigned multiplier in SystemVerilog by implementing the Karatsuba algorithm.

Integrated Computational Electronics Laboratory — Spring 2025 – Present
- Designed schematics and layouts of Field-programmable Analog Array (FPAA) standard cells on SkyWater 130nm process with open-source tools (XSchem, Ngspice, Magic VLSI, Netgen), using DRC and LVS for accuracy.
- Cells include pFET array (W/L ratios from 1 to 100) with multi-finger geometry to meet space constraints.
- Rewriting analog high level synthesis tools targeting ASIC layout generation and FPAA programming.

Georgia Tech School of Physics — Summer 2025 – Present
Researching theoretical particle physics (quantum chromodynamics) with Dr. Sa de Melo. Analyzing dynamics of color-orbit coupled SU(3) fermions.

Quantum Engineering (Vertically Integrated Projects) — Spring 2025 – Present
Optimize trapped-ion quantum computer electrode placement using electromagnetic finite element analysis (FEA).

PROJECTS

LED Control Peripheral — 2025
Peripheral interfacing with processor I/O designed in VHDL to control LEDs on FPGA board. Features gamma-corrected pulse width modulation to control brightness and ability to change multiple LED states in one instruction.

Five-stage Pipelined Processor — 2025
Pipelined processor written in SystemVerilog supporting subset of RISC-V instructions, including arithmetic operations, load/store to memory, and jumps. Hazards resolved using stalling, flushing, and forwarding.

CalHacks 11: Resilink, devpost.com/software/resilink — 2024
Node-based communication network independent of cellular. Won "Hack for Impact" and Skylo track award.

RELEVANT COURSEWORK

Digital Systems Design & Lab, Circuit Analysis, Digital Signal Processing, C/RISC-V Programming, Quantum Mechanics I & II, MATLAB, Python, Abstract Algebra I, Discrete Math, Differential Equations, Linear Algebra
In Progress: Microelectronic Circuits, Electromagnetics, Computer Organization and Design, Quantum Information

AWARDS

USA Physics Olympiad: Honorable Mention — 2024
Top ∼250 out of 6000 students; included EM-Radiation, Circuit Analysis, Frequency Filters.

Georgia Tech Physics Challenge, E&M Category: 1st Place — Spring 2025

Georgia Tech Faculty Honors — Fall 2024, Spring 2025