Computer Architecture, EITF20
Final Exam

LUND
UNIVERSITY
Electrical and Information Technology
DATE

The exam consists of 5 problems with a total of 50 points.
Grading: 20 p $\leq$ grade 3 $<$ 30 p $\leq$ grade 4 $<$ 40 p $\leq$ grade 5

Instructions:

- Turn off and put away your mobile phone – **No mobile phones**
- You may use a pocket calculator and an English dictionary on this exam, but no other aids
- Please start answering each problem on a new sheet – **New problem $\Longrightarrow$ New sheet**
- Write your anonymous code on each sheet of paper that you hand in – **Code on each sheet**
- You must motivate your answers thoroughly.
  Show all your calculations.
  If there, in your opinion, is not enough information to solve a problem, you can make reasonable assumptions that you need in order to solve the problem.
  State your assumptions clearly!

GOOD LUCK :-)

Problem 1

a) Pair each concept from table **I** with the concept from table **II** that is most closely associated. (Each answer should be a number-letter pair.) (10)

I		II	
1.	BTB	A.	output dependency
2.	WAR	B.	large, cheap, slow
3.	Trace cache	C.	addressing mode
4.	Displacement	D.	Amdahl's law
5.	Little-endian	E.	static optimization for memory system
6.	RAID	F.	jump prediction technique
7.	CDB	G.	the least significant unit is stored at the lowest memory address
8.	ROB	H.	precise exception
9.	Procedure inlining	I.	virtual memory
10.	Interleaved	J.	hard disk performance and reliability
		K.	reduce miss rate
		L.	reduce hit time
		M.	the least significant unit is stored at the highest memory address
		N.	hazard/conflict
		O.	forwarding
		P.	higher memory bandwidth

Problem 2

a) Describe the concept "memory hierarchy", and state why it is important. (1)

b) Which are the 4 principal memory hierarchy design issues (questions)? Give design guidelines for each of these issues for Virtual memory. (2)

c) Why do we have different guidelines for these issues for different levels of the memory hierarchy (take Virtual memory and L1 Cache as example)?. (2)

d) Describe TLB - principle, concept, and implementation.

Which problem does it solve?

Why is the technology working? (3)

e) Describe multi-level page table:

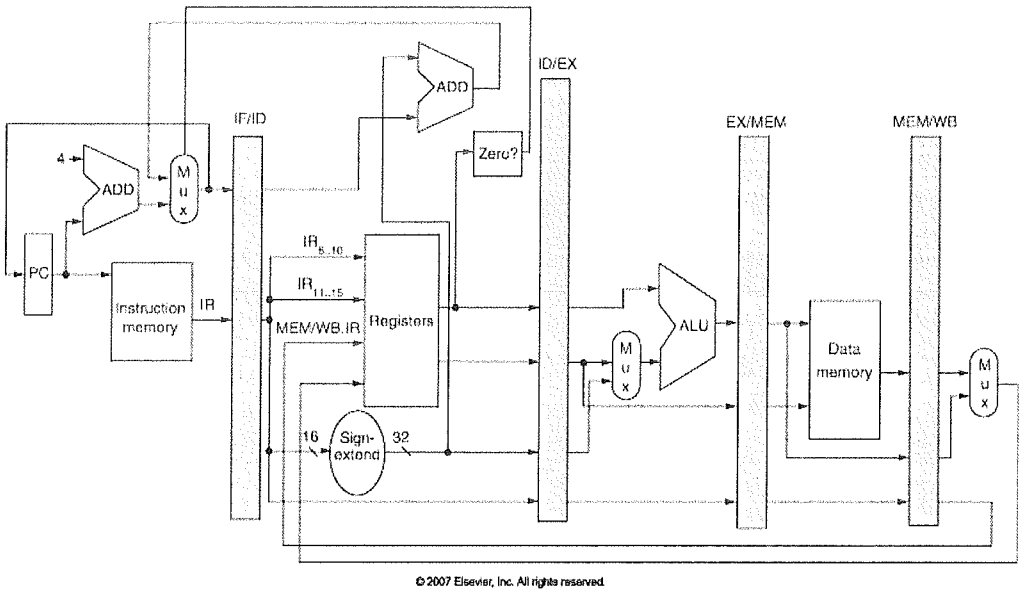
Which problem does it solve?

Why is the technology working? (2)

Problem 3

Consider the following (MIPS) program and pipeline:

```
1. DADD R1,R2,R3   ; R1 = R2 + R3
2. DSUB R4,R1,R5
3. AND  R6,R1,R7
4. OR   R7,R1,R8
5. XOR  R4,R1,R9
```



a) What is the difference between a dependency and a hazard? (1)

b) Identify and state all dependencies in the program. Which of these dependencies leads to hazards? (4)

c) What changes to the pipeline can eliminate the data hazards caused by the data dependencies in the code? (2)

d) If extend the basic pipeline to have multiple function units: integer unit (1-cycle exe), add unit (4-cycle exe), and multiplication unit (7-cycle exe). Assume single-port memory. Identify the potential structure hazard in the following code and explain why. (3)

	Clock cycle number										
Instruction	1	2	3	4	5	6	7	8	9	10	11
MUL.D F0,F4,F6	IF	ID	M1	M2	M3	M4	M5	M6	M7	MEM	WB
...		IF	ID	EX	MEM	WB					
...			IF	ID	EX	MEM	WB				
ADD.D F2,F4,F6				IF	ID	A1	A2	A3	A4	MEM	WB
...					IF	ID	EX	MEM	WB		
...						IF	ID	EX	MEM	WB	
L.D F2,0(R2)							IF	ID	EX	MEM	WB

Problem 4

Compute the average memory bandwidth needed by an in-order execution CPU running at 2.5 GHz. The average CPI= 2.3 for all instructions and the average frequency (ratio) of each operation type is shown in the following table. Assume no stalls, data and instructions are 32-bit words. (2)

Instruction mix	
instruction type	**% of all instructions**
load	23.75
store	9.66
uncond branch	5.84
cond branch	18.45
int computation	42.30
fp computation	0.00

Now we add a unified cache to the CPU. The cache has 128 sets and associativity 1. The cache system has a miss-penalty of 50 clock cycles. We are interested to quickly compare improvements (in average) of 3 mutually exclusive enhancements to the CPU.

Enhancements and data regarding our intended application are:

1. Enhancing integer computation performance by a factor 1.8 (assume no effects on miss-ratio and clock cycle time)
2. Decreasing execution time for data access instructions by a factor 2 (assume no effects on miss-ratio and clock cycle time)
3. Changing cache associativity from 128 sets, associativity 1 to 32 sets, associativity 4.

Cache miss-ratio			
No. of sets	**Associativity**		
	1	**2**	**4**
16	0.778109	0.594727	0.303048
32	0.597252	0.312289	0.136385
64	0.397689	0.145433	0.083915
128	0.207784	0.088052	0.051590

Clock cycle time dependence on associativity is:

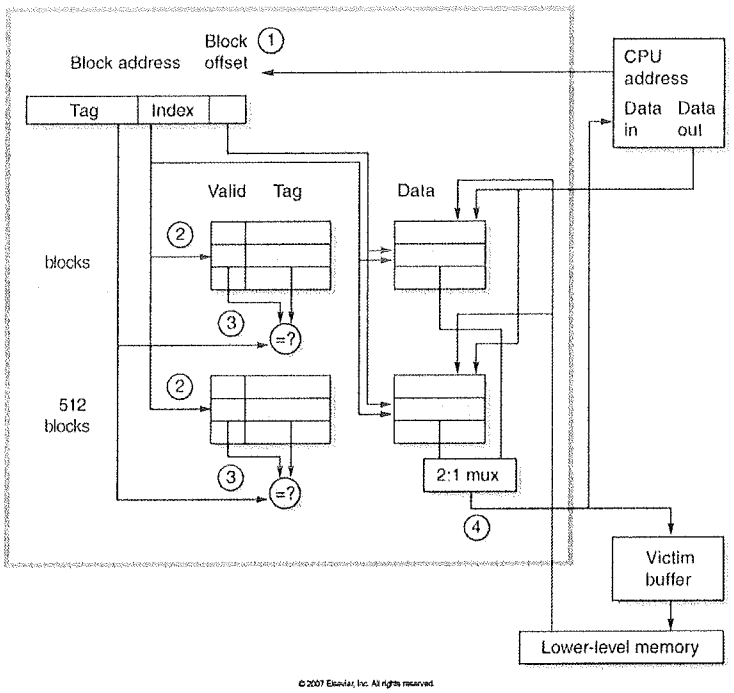
	Associativity		
	1	**2**	**4**
relative clock cycle time	1	1.04	1.1

Which of the 3 enhancements will give the highest speedup?(**Show all calculations!**) (8)

Problem 5

a) Show the address bit partitioning into fields for a memory system with parameters:
Memory size = 1GB
Cache size = 512 KB
Block size = 32 Bytes
Set associative with 4 blocks per set. (2)

b) List the micro-operations (4 steps in the following picture) done during a successful cache access (2)



c) Algorithm 0 is running with several different cache options. Table 1 is the default parameter setting.

Find any questionable results in Table 2 and explain why (assume the result for default parameter setting is correct). (3)

Fill in the missing information in Table 2 and comment on your answer. (3)

(no calculation needed, more concept check)

Table 1: Default cache parameters

	I-Cache	**D-Cache**	**Memory**
Default settings	cache size =16 block size = 2 blocks in set = 1	cache size =16 block size = 2 blocks in set = 1	read cycles = 50, write cycles = 50 writepolicy = WriteThrough write buffersize = 0 replacementpolicy = Random

Table 2: Experiment results

Settings	**Algorithm**	**I-Cache Hit rate**	**D-Cache Hit rate**	**Simulation time**
All default	Algorithm 0	0.5	0.8	177123
I- and D-cache size=32 Others: default	Algorithm 0	0.4	0.9	37321
Blocksize = 8 Others: default	Algorithm 0	0.8		
D-cache replacementpolicy =FIFO. Others: default	Algorithm 0	0.5	0.7	155103