600V high current HighSpeed 3 IGBT

Optimized for high-switching speed

About this document

Scope and purpose

This application note provides guidelines and suggestions for a design using Infineon's high-current class HighSpeed 3rd generation (H3) products. It includes a brief introduction to the H3 product family and the new current classes available in the product portfolio. It also addresses two of the key challenges engineers face during the design process:

- Effect of lead inductance on turn-on losses
- Selection of the appropriate gate driver based on electrical characteristics of the device

Intended audience

The document is intended for power electronics engineers having a basic knowledge of power semiconductor devices.

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1 Introduction

IGBTs can operate at high current density and, therefore, offer a cost-effective solution when higher power density and lower costs are required. The newer generations of IGBTs have optimized features that enable the expansion of the application range to higher switching frequencies, even in hard-switching topologies. Above 20 kHz, switching losses typically dominate total losses, so reducing E_{on} and E_{off} without significantly degrading V_{cesat} has become a development goal [2].

Switching losses in a device are affected by stray inductances in the loop that change the current and voltage waveforms during the switching transition. Generally, the parasitic inductances in a circuit are caused by the bond wire, the package leg, and the traces on the printed circuit board (PCB). The lead inductance of the device package significantly affects the switching behavior when the device current changes rapidly. This means that a rapid increase in the device current results in a significant voltage induced across the lead inductance. This reduces the voltage available at the gate driver output that in turn reduces the rate of change of the device current (di/dt).

In addition to losses in the device itself, the switching operation of a device also results in losses in the gate driver circuitry. The gate driver losses are caused by the charging or discharging of a device's input capacitance that requires a certain amount of charge to be transferred to the capacitors to change the voltage across them. The amount of charge required to turn the IGBT on or off is determined by its typical gate charge characteristics. With an insight into the proper design of a high-speed gate driver, switching losses can be reduced by minimizing the duration of the switching transition.

Infineon's new high-speed IGBT families enable system designers to increase the switching frequency of power transistors without changing cooling requirements. This lowers the system costs by reducing both the cost of power switches and the size and cost of passive components. Infineon's 3rd generation high-speed IGBTs are optimized for high switching frequencies even in hard-switching applications such as switched mode power supply (SMPS), welding, solar, and uninterruptable power supply (UPS) applications [2]. This application note provides guidelines and suggestions for a design using HighSpeed 3rd generation (H3) high-current class products and addresses some of the challenges associated with the design process.

2 Short description of the product family

The HighSpeed 3rd generation (H3) product family is an evolution of the IGBT3 technology—popularly known as the TRENCHSTOP™ technology. It combines the advantages of both trench-gate and field-stop structure, resulting in low V_{cesat} and short tail current.

H3 devices are optimized for high switching frequencies above 40 kHz that offer smooth switching behavior combined with reduced switching losses. Target applications are high-switching frequency, hard-switching applications such as UPS, welding, power factor correction (PFC), and solar inverters.

The product portfolio extension includes high-current class devices—60, 75, and 100 A single IGBTs and 60 and 75 A DuoPack; both available in the 600 V voltage class and the TO-247 package.

Table 1 Product portfolio

	Current class	Part number
Single IGBT	60 A	IGW60N60H3
	75 A	IGW75N60H3
	100 A	IGW100N60H3
DuoPack	60 A	IKW60N60H3
	75 A	IKW75N60H3

For more information on electrical features and switching parameters, please refer to the 2010 article "High Speed IGBT with MOSFET-like switching behavior" written by D. Chiola, H. Hüsken, and Thomas Kimmer from Infineon Technologies AG.

3 Lead inductance impact on turn-on losses

High speed IGBTs are highly sensitive to extra inductance at the lead of the device package. Figure 1 shows a double-pulse measurement setup with the IKW60N60H3 as the device under test (DUT) connected on the low side and its co-packed diode connected on the high side as a freewheeling diode. This measurement setup, shown in Figure 1 (left) demonstrates how a very long lead package causes an additional inductance, which, as mentioned, has a greater effect on switching performance in high-current devices.

In addition, a larger lead inductance results in a higher voltage oscillation peak in the measured gate voltage. A voltage is induced across the parasitic inductance due to the rate of change of current (dI/dt) in the device, which is added to the actual voltage at gate of the device. The induced voltage due to the stray inductance caused by the long traces on the PCB and long lead length causes the switching speed to slow down.

Practical suggestions to limit this effect are as follows:

- Insert the device as far into the circuit board as possible (to shorten the lead length)
- Place the gate driver and load circuits as close to the device as possible (to reduce the stray and gate drive path loop inductance)

The comparison between the two different test setups shows the impact of parsitics on the switching behaviors and illustrates how lower parasitic inductance can lead to improved switching performance. As shown in the test setup on the right side of Figure 1, an external connection to the emitter pin using a crocodile clip shortens the path length. This reduces the stray inductance due to shorter path length and the lead inductances as it is placed closest to the device package. This has a direct impact, especially on the turn-on losses.

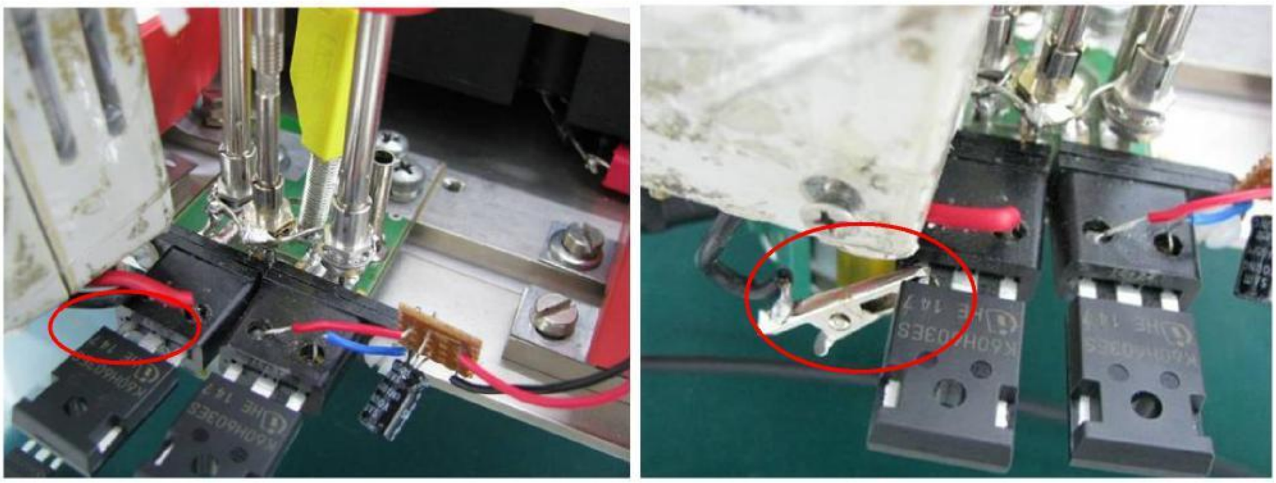

Figure 1 The left side shows the standard connection. The right-hand side shows the connection with a crocodile clip on the emitter pin that lowers the lead inductance

Figure 2 shows the switching curves at turn-on, measured for IKW75N60H3 and IKW60N60H3 for both the simple plug-in connection and the crocodile clip connection. The left side shows the gate voltage signals and the right side shows the current and voltage waveforms.

When the effective stray inductance is minimized, the coupling of the load current to the gate drive is reduced and faster switching is observed, as evidenced by a faster rate of rise in the load current (higher di/dt). The sensing of the gate signal is identical for both setups and is located at the end of the socket for both the standard and clip connection of the gate drive. Thus, an increase in the gate signal voltage by 4 V for clip connection should not be interpreted as higher gate voltage in the device but rather as an indication that faster switching has been achieved. The gate voltage at the device is fixed at the Miller voltage.

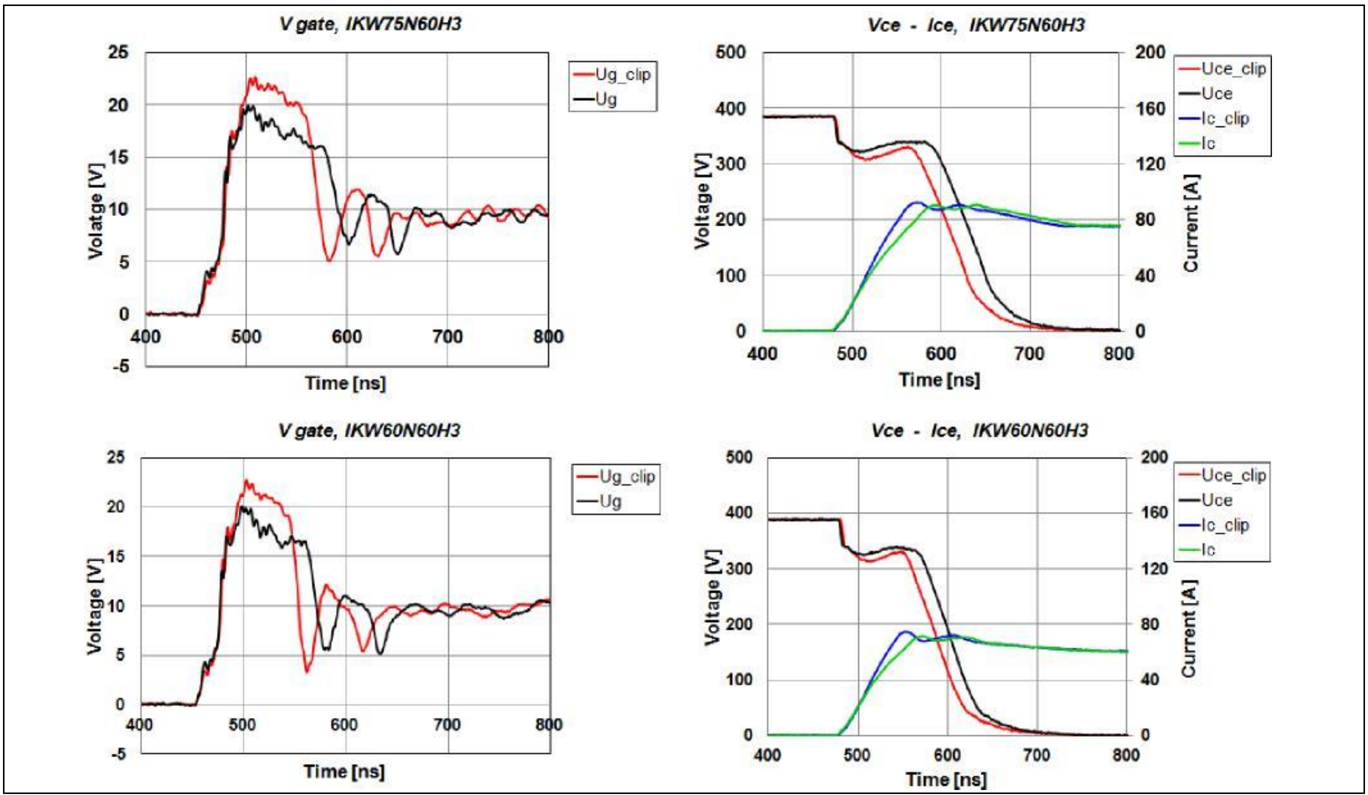

Figure 2 IKW75N60H3 and IKW60N60H3 turn-on switching waveforms: Comparison between simple plug-in and crocodile clip connections

Table 2 provides a quantitative evaluation of the reduction in turn-on losses due to the different connections. In particular, it contains measured values for E_{on} in the two different conditions that were tested.

Table 2 Measured values of the turn-on losses and percentage improvement due to lead inductance reduction

Device	E_{on} [mJ]	E_{on} [mJ] with clip	Percentage difference
IKW60N60H3	2.1517	1.8847	-14.1667
IKW75N60H3	3.2699	2.7924	-17.1

Based on measured waveforms and the turn-on energy loss values listed in Table 2, it can be concluded that reducing the emitter lead inductance will reduce losses by a factor of over 10%.

4 Gate driver requirements

This chapter provides a method to evaluate and select an appropriate driver based on the electrical features of the device.

An assessment of IGBT2 (SGW50N60HS) and HighSpeed 3 (IGW50N60H3) devices in the same current and voltage class was performed to compare and define the driver specifications for these two technologies.

The parts selected were 50 A current class devices—the highest current class available in the IGBT2 portfolio.

To determine the driver specification, input data such as device gate charge Q_g, switching frequency of operation f_{sw}, IGBT collector emitter voltage V_{CEmax}, and gate resistance R_g is required.

Table 3 lists the electrical parameters and operating conditions for the application for the two devices.

Table 3 Input data for calculation

Input data	SGW50N60HS	IGW50N60H3
IGBT gate charge Q_g (V_{CC}=480V, I_C=50A, V_{GE}=15V)	179 nC	315 nC
Gate voltage swing ΔV_g	15 V (V_{GG}= 0V, V_{GG}= +15V)	15 V (V_{GG}= 0V, V_{GG}= +15V)
Switching frequency f_{sw}	40 kHz	40 kHz
Gate resistance R_g	7 Ω	7 Ω

Using the values given in Table 3, both the average output current I_{outAV} and the peak output current $I_{outPEAK}$ of the driver can be determined.

I_{outAV} is obtained by multiplying the gate charge Q_g and operating switching frequency f_{sw}, while $I_{outPEAK}$ is determined by dividing the gate voltage swing ΔV_g by R_g.

Table 4 lists the results obtained.

Table 4 Calculated output data

Output data	SGW50N60HS	IGW50N60H3
Average output current I_{outAV}	7.2 mA	12.6 mA
Peak output current $I_{outPEAK}$	~ 2.2 A	~ 2.2 A

As the definition of $I_{outPEAK}$ does not depend on the electrical features of the device, the required $I_{outPEAK}$ value is the same (approximately 2.2 A) for both the selected devices. On the other hand, I_{outAV} that is related to the gate charge of the device is higher by 5.4 mA for HighSpeed 3 and therefore has different requirements for the driver.

The total power losses computed as $\Delta V_g * Q_g * f_{sw}$ are approximately 40% higher for HighSpeed 3 because of the higher gate charge, as shown in Figure 3. Therefore, a suitable gate driver system that considers both thermal and electrical characteristics to achieve higher performance in terms of switching losses and efficiency is required.

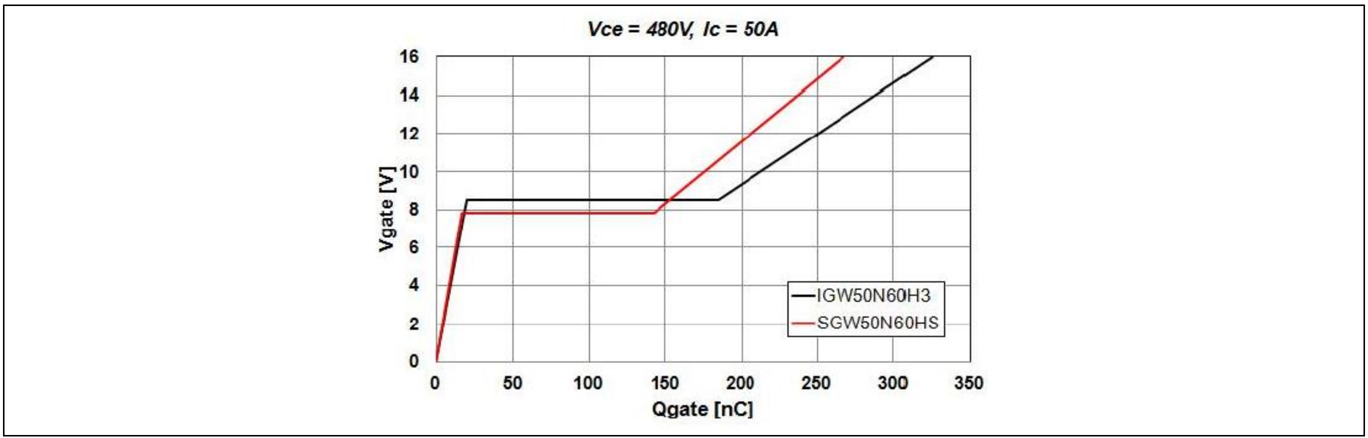

Figure 3 Gate charge curves

5 Conclusion

This application note provided an introduction to the HighSpeed 3rd generation (H3) products available in the high current class and the design challenges associated with these devices. To summarize:

- Switching behavior and turn-on losses are highly sensitive to lead inductance in high-current and high-speed devices. It is possible to improve performance by minimizing the lead inductance at the emitter pin either by an external connection or by plugging the device into the board, and by placing the gate driver and load circuits as close to the device as possible
- HighSpeed 3 provides higher performance at the cost of higher driver requirements in terms of average output and peak output current compared to IGBT2

6 References

[1] Infineon Technologies AG: “1200V HighSpeed 3 IGBT, A new family optimized for high-switching speed”, D. Chiola, H. Hüsken, May 2010

[2] “High Speed IGBT with MOSFET-like switching behavior”, D. Chiola, H. Hüsken, T. Kimmer, 2010 Infineon Technologies AG

Revision history

Document version	Date of release	Description of changes
V 1.0	Nov. 2012	First release
V 2.0	29 Aug. 2022	- Template update - Added the “Introduction” section - Revised all sections

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