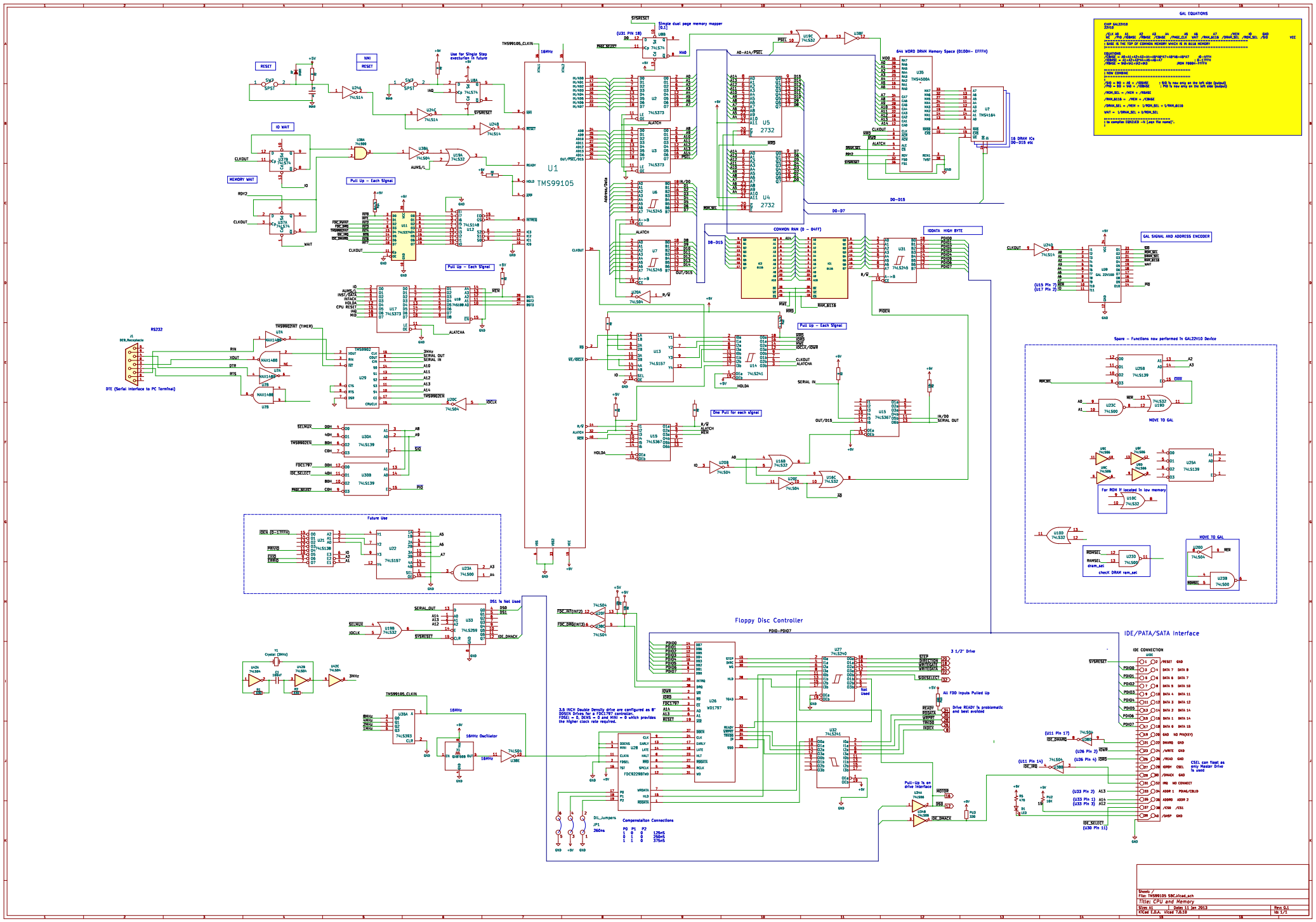
GAL EQUATIONS
Single dual page memory mapper
64k WORD DRAM Memory Space (0100H- EFFFH)
16 DRAM ICs D0-D15 etc
COMMON RAM (D - 04FF)
IODATA HIGH BYTE
GAL SIGNAL AND ADDRESS ENCODER
Spare - Functions now performed in GAL22V10 Device
MOVE TO GAL
For ROM if located in low memory
check DRAM ram_sel
RESET
NMI
IO WAIT
MEMORY WAIT
Pull Up - Each Signal
RS232
DTE (Serial interface to PC Terminal)
TMS99902RT (TIMER)
Future Use
Floppy Disc Controller
IDE/PATA/SATA Interface
3 1/2" Drive
All FDD inputs Pulled Up
Drive READY is problematic and best avoided
Pull-Up is on drive interface
CSEL can float as only Master Drive is used
3.5 INCH Double Density drive are configured as 8" DRIVEN Drives for a FDC1797 controller. FDSEL = 0, DCHS = 0 and MINI = 0 which provides the higher clock rate required.
Compensation Connections
Dil_Jumpers
16MHz Oscillator
Crystal (3MHz)
One Pull for each signal
Sheet: /
File: TMS99105 SBC.kicad_sch
Title: CPU and Memory
Size: A1
Date: 11 Jan 2013
Rev: 0.1
KiCad E.D.A. kicad 7.0.10
Id: 1/1