

[illegible]

Diagram illustrating the pin-to-pin mapping between two 8-pin headers:

Pin Header J10	Pin Header J4
1 Dt0	D0 1
2 Dt1	D1 2
3 Dt2	D2 3
4 Dt3	D3 4
5 Dt4	D4 5
6 Dt5	D5 6
7 Dt6	D6 7
8 Dt7	D7 8

The diagram illustrates a circuit for interfacing a DAC pin socket with a 4-bit data bus. It features four 74LS573 shift registers (U2, U3, U4, U5) and a DAC pin socket (J7).

Components and Connections:

- Shift Registers (U2, U3, U4, U5):** All four 74LS573 chips are configured with VCC to pin 20 and GND to pins 10 and 11. The Load (OE) pins (pin 1) are connected to GND.
- Data Out Header (J9):** An 8-pin header providing data inputs Dt0 through Dt7. Dt0-Dt3 are connected to the D0-D3 inputs of U2. Dt4-Dt7 are connected to the D0-D3 inputs of U5.
- Ctrl Header (J8):** A 3-pin header providing control signals. Pin 1 (Sel0) is connected to the Load (OE) pin of U2. Pin 2 (LD_Master) is connected to the Load (OE) pin of U5. Pin 3 (Sel1) is connected to the Load (OE) pin of U4.
- DAC Pin Socket (J7):** An 18-pin socket where the DAC is inserted. Pins 1-4 are connected to the Q0-Q3 outputs of U2. Pins 5-8 are connected to the Q0-Q3 outputs of U5. Pins 9-12 are connected to the Q0-Q3 outputs of U3. Pins 13-16 are connected to the Q0-Q3 outputs of U4. Pins 17 and 18 are connected to VCC.

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