DRAM 256 K x 16 DRAM
EDO PAGE MODE

FEATURES

- X16 organization
- EDO (Extended Data-Output) access mode
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- Single 5V (±10%) power supply
- TTL-compatible inputs and outputs
- 512-cycle refresh in 8ms
- Refresh modes : $\overline{RAS}$ only, $\overline{CAS}$ BEFORE $\overline{RAS}$ (CBR) and HIDDEN
- JEDEC standard pinout
- Key AC Parameter

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-25	25	8	43	10
-35	35	10	65	14

ORDERING INFORMATION - PACKAGE

40-pin 400mil SOJ
44 / 40-pin 400mil TSOP (TypeII)

PRODUCT NO.	PACKING TYPE	COMMENTS
M11B416256A-25JP	SOJ	Pb-free
M11B416256A-35TG	TSOPII	Pb-free

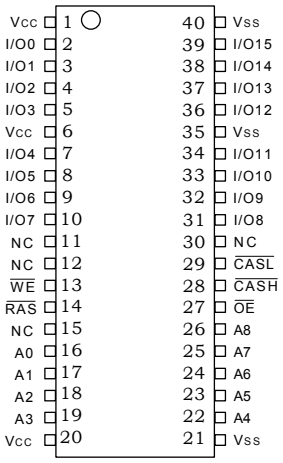
GENERAL DESCRIPTION

The M11B416256A is a randomly accessed solid state memory, organized as 262,144 x 16 bits device. It offers Extended Data-Output , 5V(±10%) single power supply. Access time (-25,-35) and package type (SOJ, TSOP II) are optional features of this family. All these family have $\overline{CAS}$ - before - $\overline{RAS}$, $\overline{RAS}$ -only refresh and Hidden refresh capabilities.

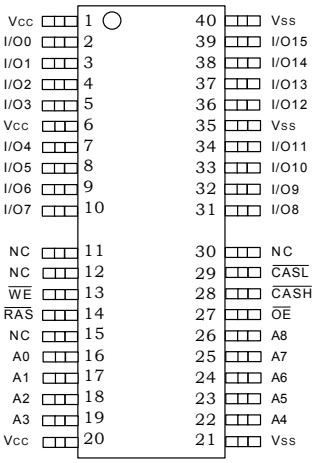
Two access modes are supported by this device : Byte access and Word access. Use only one of the two $\overline{CAS}$ and leave the other staying high will result in a BYTE access. WORD access happens when two $\overline{CAS}$ ($\overline{CASL}$, $\overline{CASH}$) are used. $\overline{CASL}$ transiting low during READ or WRITE cycle will output or input data into the lower byte (IO0~IO7), and $\overline{CASH}$ transiting low will output or input data into the upper byte (IO8~15).

PIN ASSIGNMENT

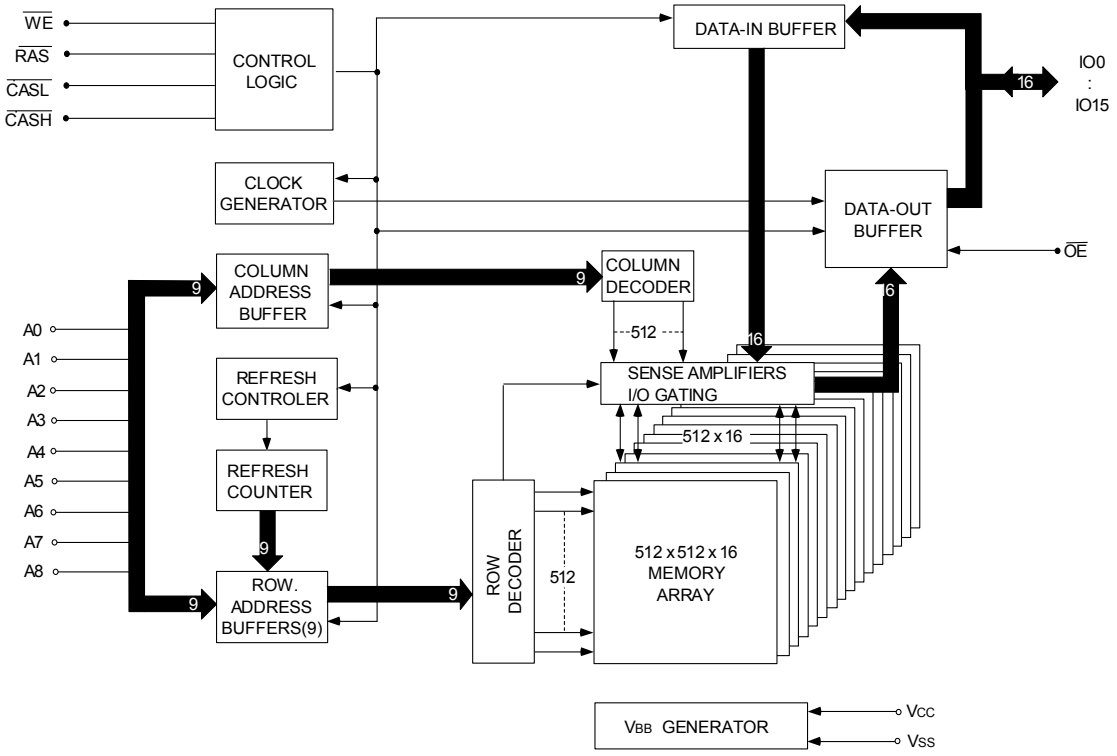
SOJ Top View



TSOP (TypeII) Top View



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	PIN NAME	TYPE	DESCRIPTION
16~19,22~26	A0~A8	Input	Address Input Row Address : A0~A8 Column Address : A0~A8
14	$\overline{RAS}$	Input	Row Address Strobe
28	$\overline{CASH}$	Input	Column Address Strobe / Upper Byte Control
29	$\overline{CASL}$	Input	Column Address Strobe / Lower Byte Control
13	$\overline{WE}$	Input	Write Enable
27	$\overline{OE}$	Input	Output Enable
2~5,7~10,31~34,36~39	I/O0 ~ I/O15	Input / Output	Data Input / Output
1,6,20	V_{CC}	Supply	Power, 5V
21,35,40	V_{SS}	Ground	Ground
11,12,15,30	NC	-	No Connect

ABSOLUTE MAXIMUM RATINGS

Voltage on Any pin Relative to Vss … ……-1V to +7V
Operating Temperature, T_A (ambient) ….0 °C to +70 °C
Storage Temperature (plastic) …….-55 °C to +150 °C
Power Dissipation ……1.43W
Short Circuit Output Current ……50mA

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation of the device above those conditions indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS ($0\,°C \le T_A \le 70\,°C$; $V_{CC} = 5V \pm 10\%$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Supply Voltage		V_{SS}	0	0	V	
Input High Voltage		V_{IH}	2.4	V_{CC} +0.3	V	1
Input Low Voltage		V_{IL}	-0.3	0.8	V	1
Input Leakage Current	$0V \le V_{IN} \le V_{IH}$ (max)	I_{LI}	-10	10	μA	
Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ Output(s) disable	I_{LO}	-10	10	μA	2
Output High Voltage	I_{OH} = -5 mA	V_{OH}	2.4	-	V	
Output Low Voltage	I_{OL} = 4.2 mA	V_{OL}	-	0.4	V	

Note : 1.All Voltages referenced to V_{SS}

2. $0V \le V_{OUT} \le 5.0V$, $VCC \le 5.0V$

PARAMETER	CONDITIONS	SYMBOL	MAX		UNITS	NOTES
			-25	-35		
Operating Current	$\overline{RAS}$, $\overline{CAS}$ cycling , t_{RC} =min	I_{CC1}	210	150	mA	1,2
Standby Current	TTL interface , $\overline{RAS}$, $\overline{CAS}$ = V_{IH} , D_{OUT} =High-Z	I_{CC2}	4	4	mA	
	CMOS interface, $\overline{RAS}$, $\overline{CAS}$ $\ge V_{CC}$-0.2V		2	2	mA	
$\overline{RAS}$ only refresh Current	t_{RC} = min	I_{CC3}	210	150	mA	2
EDO Page Mode Current	t_{PC} = min	I_{CC4}	210	150	mA	1,3
Standby Current	$\overline{RAS}$ =V_{IH}, $\overline{CAS}$ = V_{IL}	I_{CC5}	5	5	mA	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	t_{RC} = min	I_{CC6}	210	150	mA	

Note : 1. ICC max is specified at the output open condition.
2. Address can be changed twice or less while $\overline{RAS}$ =V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ =V_{IH} .

CAPACITANCE (Ta = 25 °C , V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	TYP	MAX	UNIT
Input Capacitance (address)	C_{I1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CASH}$, $\overline{CASL}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	-	7	pF
Output capacitance (I/O0~I/O15)	$C_{I/O}$	-	10	pF

AC ELECTRICAL CHARACTERISTICS (Ta = 0 to 70 °C , V_{CC} =5V ± 10%, V_{SS} = 0V) (note 14)

Test Conditions
Input timing reference levels : 0V, 3V
Output reference level : V_{OL}= 0.8V, V_{OH}=2.0V
Output Load : 2TTL gate + CL (50pF)
Assumed t_T = 2ns

PARAMETER	SYMBOL	-25		-35		UNIT	Notes
		MIN	MAX	MIN	MAX		
Read or Write Cycle Time	t_{RC}	43		65		ns	
Read Write Cycle Time	t_{RWC}	65		95		ns	
EDO-Page-Mode Read or Write Cycle Time	t_{PC}	10		14		ns	22
EDO-Page-Mode Read-Write Cycle Time	t_{PCM}	32		42		ns	22
Access Time From $\overline{RAS}$	t_{RAC}		25		35	ns	4
Access Time From $\overline{CAS}$	t_{CAC}		8		10	ns	5,20
Access Time From $\overline{OE}$	t_{OAC}		8		10	ns	13,20
Access Time From Column Address	t_{AA}		12		18	ns	
Access Time From $\overline{CAS}$ Precharge	t_{ACP}		14		20	ns	20
$\overline{RAS}$ Pulse Width	t_{RAS}	25	10K	35	10K	ns	
$\overline{RAS}$ Pulse Width (EDO Page Mode)	t_{RASC}	25	100K	35	100K	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	8		10		ns	25
$\overline{RAS}$ Precharge Time	t_{RP}	15		25		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	4	10K	5	10K	ns	24
$\overline{CAS}$ Hold Time	t_{CSH}	21		30		ns	19
$\overline{CAS}$ Precharge Time	t_{CP}	4		5		ns	6,23
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	10	17	10	25	ns	7,18
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		ns	19
Row Address Setup Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	5		5		ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	8	13	8	17	ns	8
Column Address Setup Time	t_{ASC}	0		0		ns	18
Column Address Hold Time	t_{CAH}	5		5		ns	18
Column Address Hold Time (Reference to $\overline{RAS}$)	t_{AR}	22		30		ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	12		18		ns	

(Continued)

PARAMETER	SYMBOL	-25		-35		UNIT	Notes
		MIN	MAX	MIN	MAX		
Read Command Setup Time	t_{RCS}	0		0		ns	15,18
Read Command Hold Time Reference to $\overline{CAS}$	t_{RCH}	0		0		ns	9,15,19
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0		0		ns	9
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	3		3		ns	20
Output Buffer Turn-off Delay From $\overline{CAS}$ or $\overline{RAS}$	t_{OFF1}	3	15	3	15	ns	10,17,20
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}		6		8	ns	17,26
Write Command Setup Time	t_{WCS}	0		0		ns	11,15,18
Write Command Hold Time	t_{WCH}	5		5		ns	15,25
Write Command Hold Time (Reference to $\overline{RAS}$)	t_{WCR}	22		30		ns	15
Write Command Pulse Width	t_{WP}	5		5		ns	15
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	7		9		ns	15
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	5		7		ns	15,19
Data-in Setup Time	t_{DS}	0		0		ns	12,20
Data-in Hold Time	t_{DH}	5		5		ns	12,20
Data-in Hold Time (Reference to $\overline{RAS}$)	t_{DHR}	22		30		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	34		51		ns	11
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	21		34		ns	11
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	17		26		ns	11,18
Transition Time (rise or fall)	t_T	1.5	50	2.5	50	ns	2,3
Refresh Period (512 cycles)	t_{REF}		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	10		10		ns	
$\overline{CAS}$ Setup Time(CBR REFRESH)	t_{CSR}	5		10		ns	1,18
$\overline{CAS}$ Hold Time(CBR REFRESH)	t_{CHR}	7		10		ns	1,19
$\overline{OE}$ Hold Time From $\overline{WE}$ During Read-Mode-Write Cycle	t_{OEH}	4		4		ns	16
$\overline{OE}$ Low to $\overline{CAS}$ High Setup Time	t_{OES}	4		4		ns	
$\overline{OE}$ High Hold Time From $\overline{CAS}$ High	t_{OEHC}	2		2		ns	
$\overline{OE}$ Precharge Time	t_{OEP}	2		2		ns	
$\overline{OE}$ Setup Prior to $\overline{RAS}$ During Hidden Refresh Cycle	t_{ORD}	0		0		ns	
Last $\overline{CAS}$ Going Low to First $\overline{CAS}$ Returning High	t_{CLCH}	4		5		ns	21
Data Output Hold After $\overline{CAS}$ Returning Low	t_{COH}	3		3		ns	
Output Disable Delay From $\overline{WE}$	t_{WHZ}	3	7	3	7	ns	

Notes :

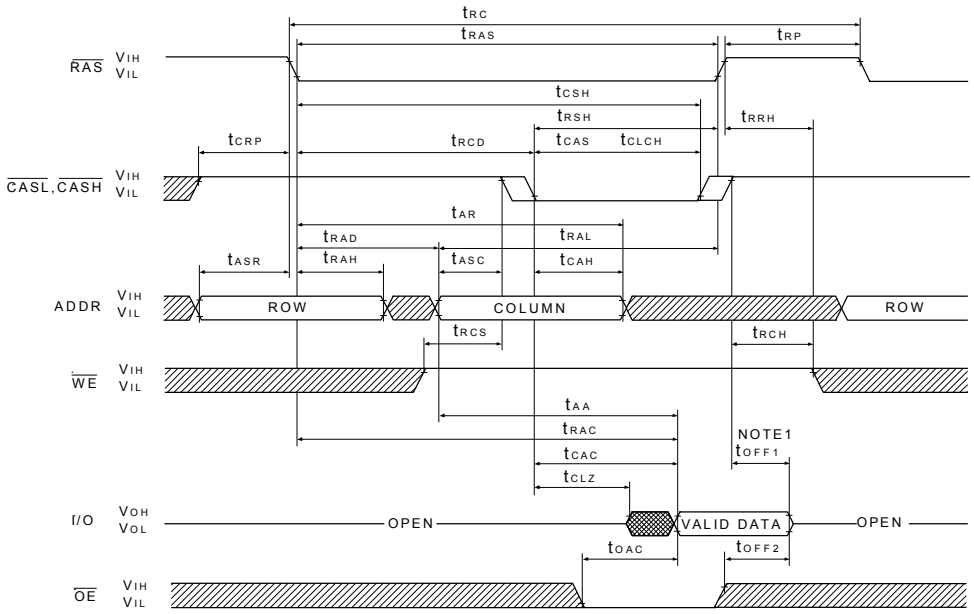
1. Enables on-chip refresh and address counters.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. In addition to meet the transition rate specification, all input signals must transit between V_{IH} and V_{IL} in a monotonic manner.
4. Assume that $t_{RCD} < t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assume that $t_{RCD} \geq t_{RCD}$ (max)
6. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, data-out will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed high.
7. Operation within the t_{RCD} limit ensures that t_{RCD} (max) can be met, t_{RCD} (max) is specified as a reference point only ; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled by t_{CAC}.
8. Operation within the t_{RAD} limit ensures that t_{RAD}(max) can be met. t_{RAD}(max) is specified as a reference point only ; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled by t_{AA}.
9. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
10. t_{OFF1}(max) defines the time at which the output achieves the open circuit condition ; it is not a reference to V_{OH} or V_{OL}.
11. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CWD} \geq t_{CWD(min)}$, the cycle is READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held high and $\overline{WE}$ taken low after $\overline{CAS}$ goes low result in a LATE WRITE ($\overline{OE}$ -controlled) cycle.
12. Those parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY- WRITE cycles.
13. During a READ cycle, if $\overline{OE}$ is low then taken HIGH before $\overline{CAS}$ goes high, I/O goes open, if $\overline{OE}$ is tied permanently low, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
14. An initial pause of 200µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
15. WRITE command is defined as $\overline{WE}$ going low.
16. LATE WRITE and READ-MODIFY-WRITE cycles must have both tOFF2 and t_{OEH} met ($\overline{OE}$ high during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycles.
17. The I/Os open during READ cycles once t_{OFF1} or t_{OFF2} occur.
18. Referenced to the earlier $\overline{CAS}$ falling edge.
19. Referenced to the latter $\overline{CAS}$ rising edge.
20. Output parameter (I/O) is referenced to corresponding $\overline{CAS}$ input, IO0~7 by $\overline{CASL}$ and IO8~15 by $\overline{CASH}$.
21. Last falling $\overline{CAS}$ edge to first rising $\overline{CAS}$ edge.
22. Last rising $\overline{CAS}$ edge to next cycle's last rising $\overline{CAS}$ edge.
23. Last rising $\overline{CAS}$ edge to first falling $\overline{CAS}$ edge.
24. Each $\overline{CAS}$ must meet minimum pulse width.
25. Referenced to the latter $\overline{CAS}$ falling edge.
26. All IOs controlled by $\overline{OE}$, regardless $\overline{CASL}$ and $\overline{CASH}$.

TRUTH TABLE

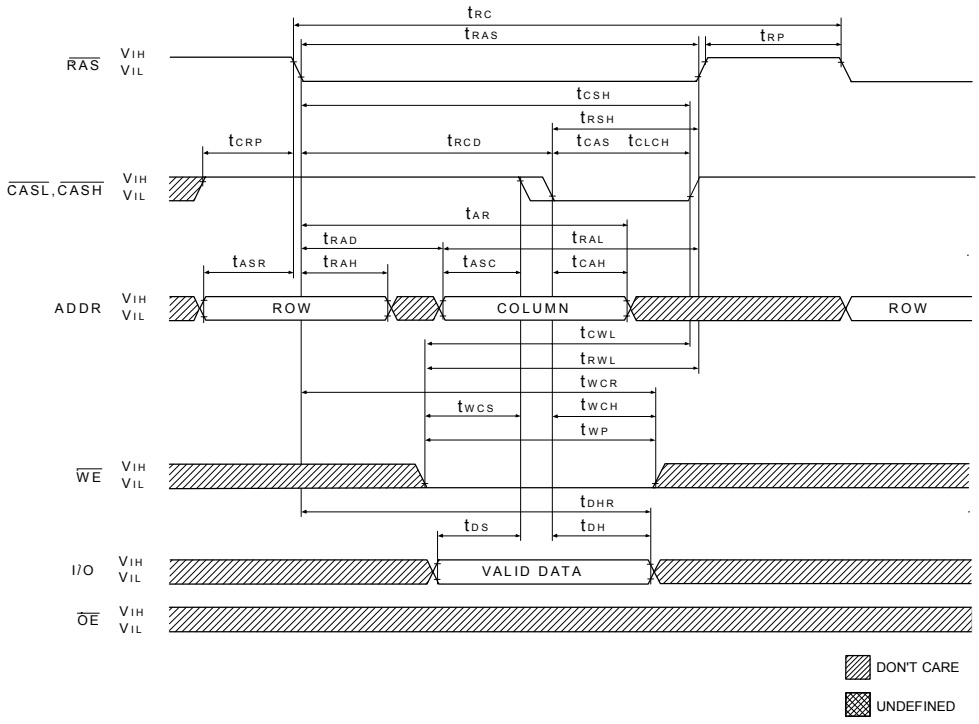
FUNCTION		$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DQs	NOTES
							ROW	COL		
Standby		H	H→X	H→X	X	X	X	X	High-Z	
Read : Word		L	L	L	H	L	ROW	COL	Data-Out	
Read : Lower Byte		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out	
Read : Upper Byte		L	H	L	H	L	ROW	COL	Upper Byte, Data-Out	
Write : Word (Early Write)		L	L	L	L	X	ROW	COL	Data-In	
Write : Lower Byte (Early)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In , Upper Byte, High-Z	
Write : Upper Byte (Early)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z , Upper Byte, Data-In	
Read-Write		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
EDO-Page-Mode Read	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L		COL	Data-Out	2
	Any Cycle	L	L→H	L→H	H	L			Data-Out	2
EDO-Page-Mode Write	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X		COL	Data-In	1
EDO-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H		COL	Data-Out, Data-In	1, 2
Hidden Refresh		L→H→L	L	L	H	L	ROW	COL	Data-Out	2
$\overline{RAS}$ -Only Refresh		L	H	H	X	X	ROW		High-Z	
CBR Refresh		H→L	L	L	H	X	X	X	High-Z	3

*Note : 1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
3. Only one $\overline{CAS}$ must be active ($\overline{CASL}$ or $\overline{CASH}$).

READ CYCLE

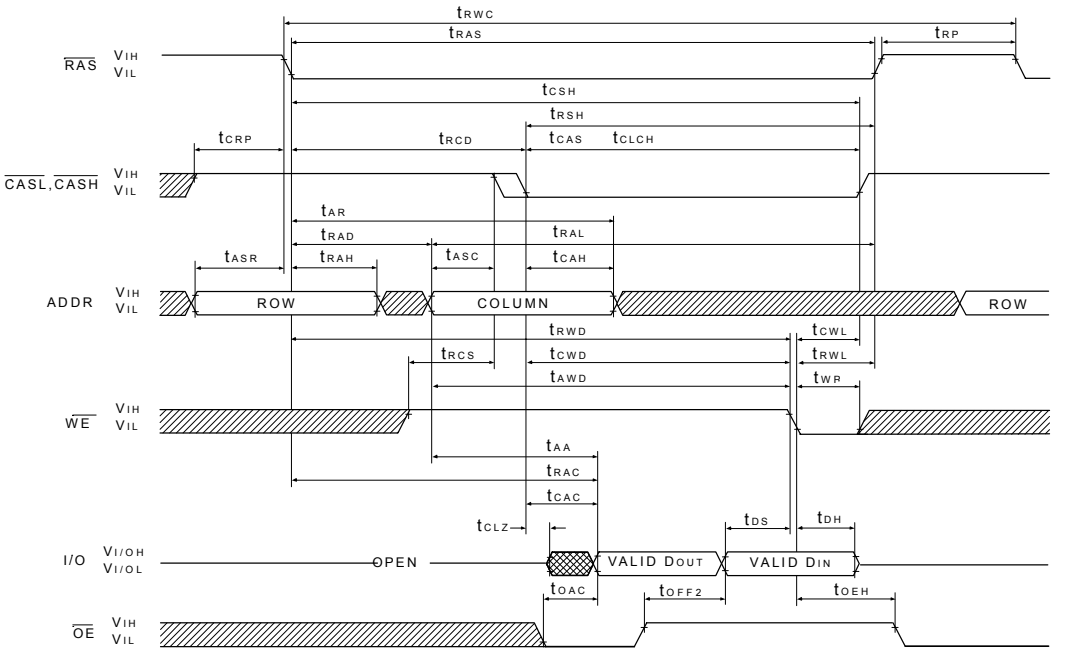


EARLY WRITE CYCLE

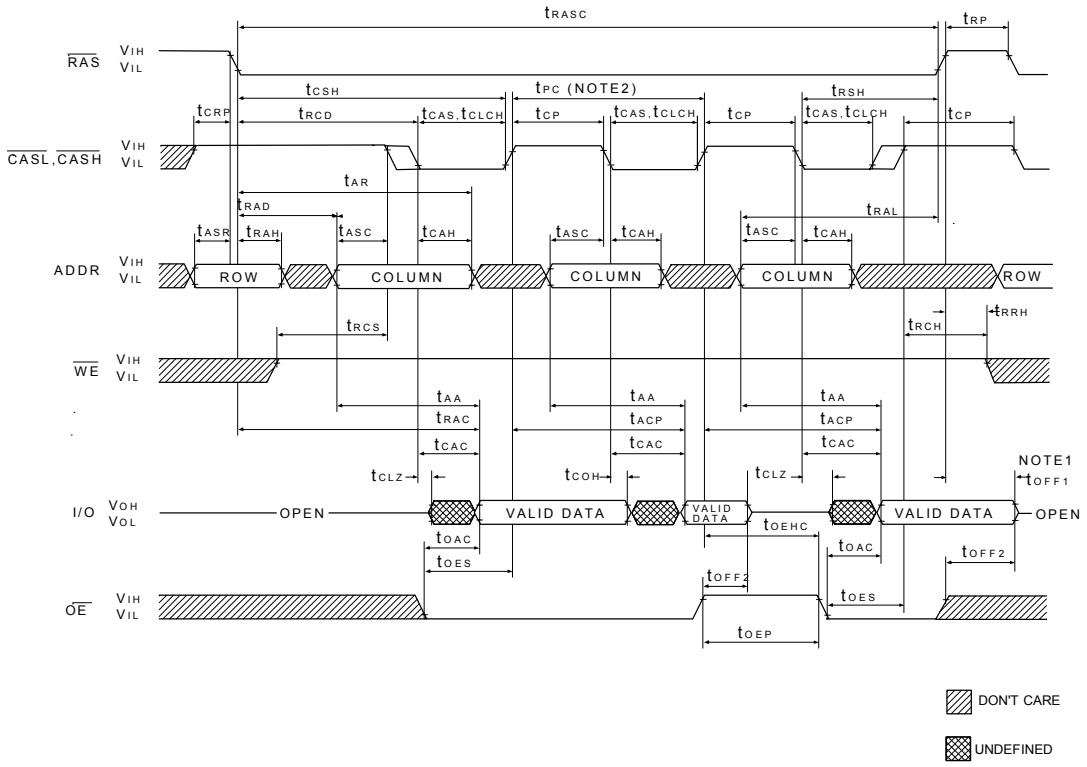


Note: 1. t_{OFF1} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



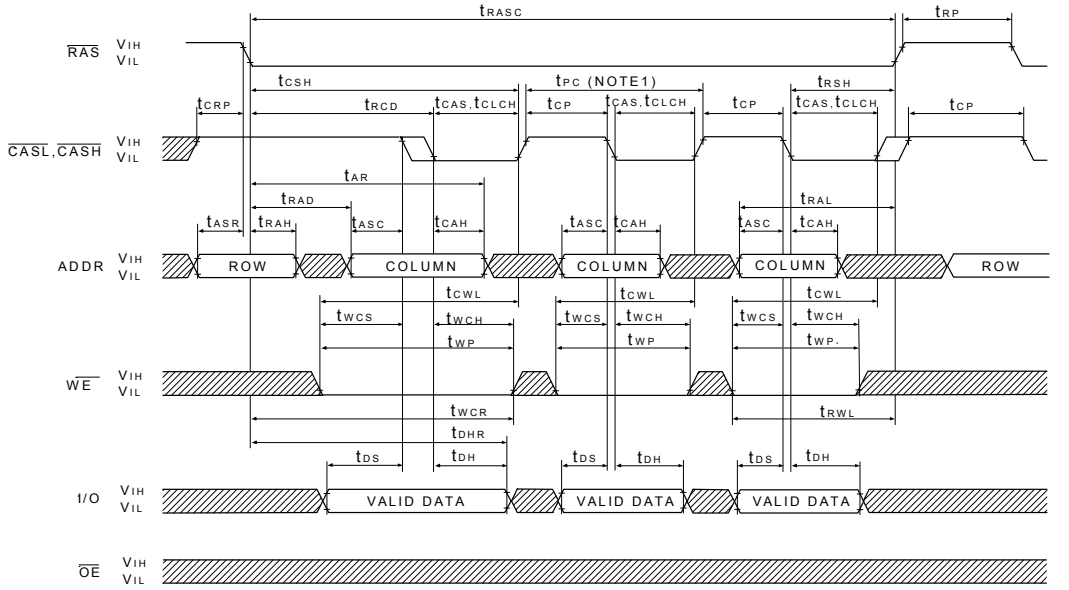
EDO-PAGE-MODE READ CYCLE



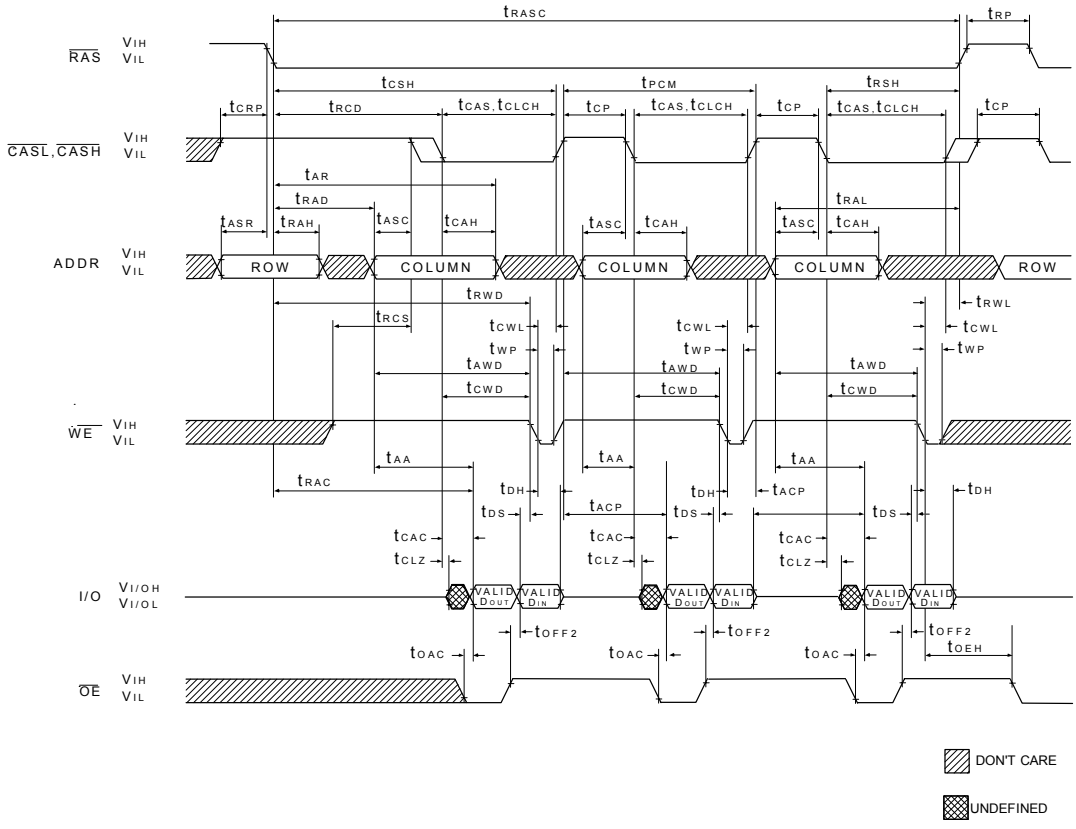
*NOTE : 1. t_{OFF1} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

2. t_{PC} can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{CAS}$. Both measurements must meet the t_{PC} specification.

EDO-PAGE-MODE EARLY-WRITE CYCLE

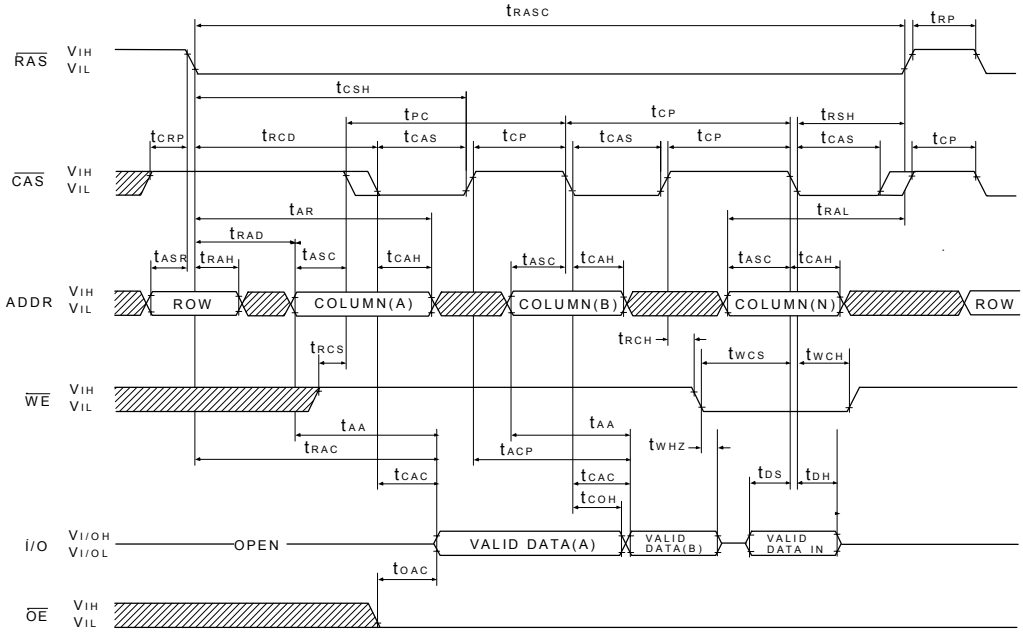


EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)

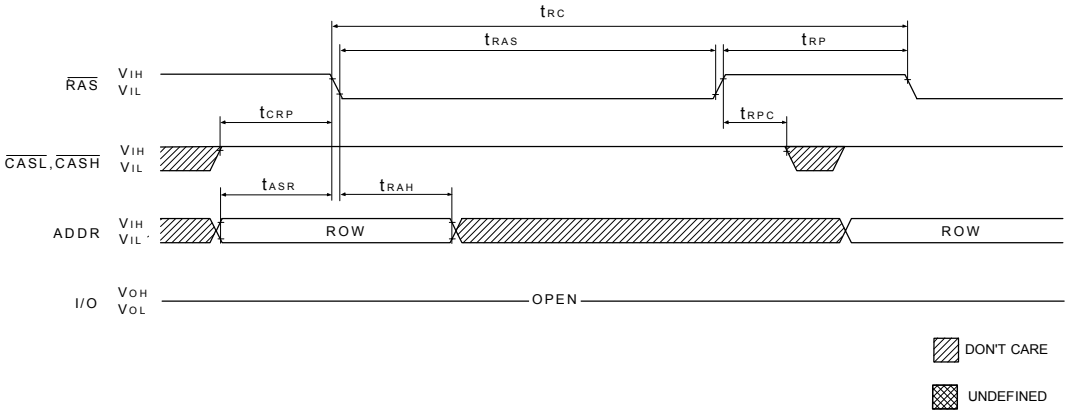


Note : 1. t_{PC} can be measured from falling edge to falling edge of $\overline{CAS}$, or from rising edge to rising edge of $\overline{CAS}$. Both measurements must meet the t_{PC} specification.

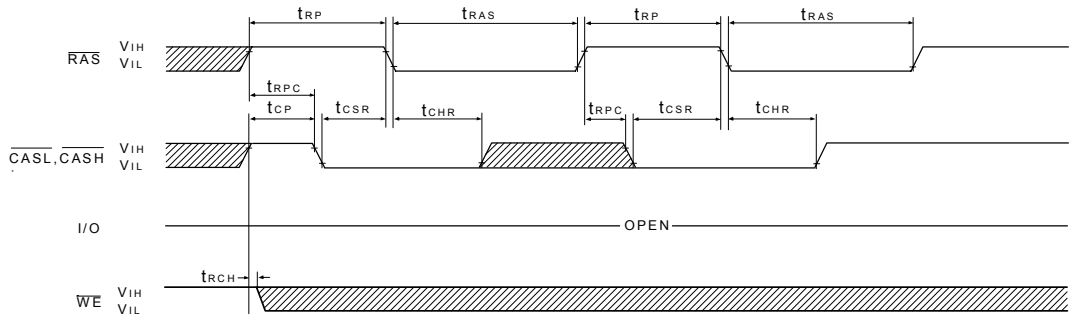
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Psuedo READ-MODIFY-WRITE)



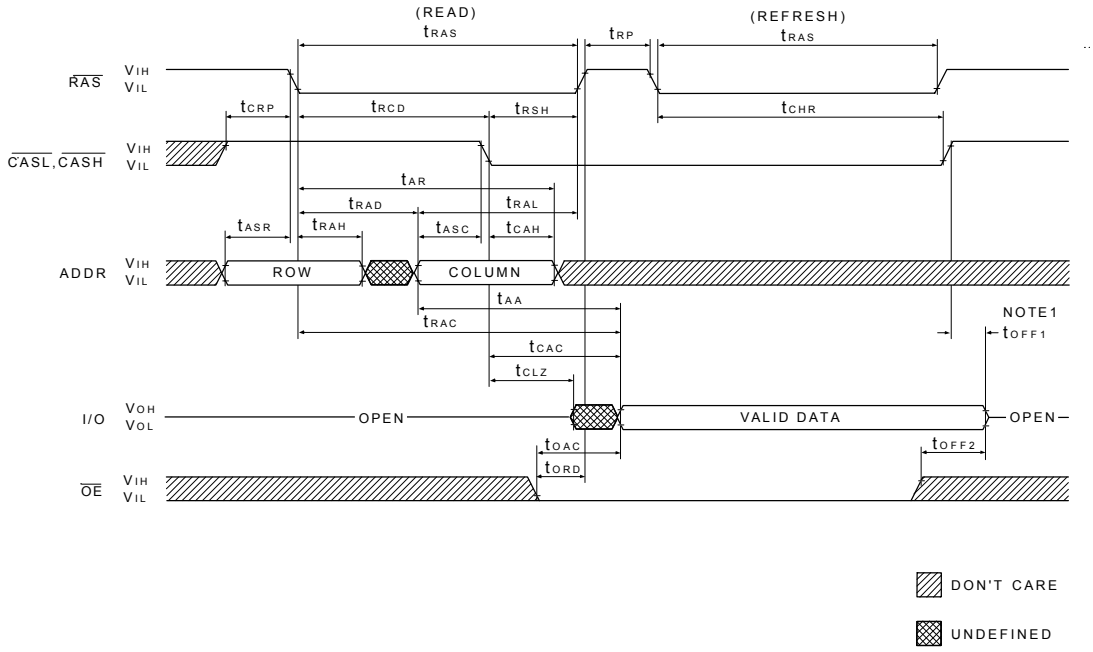
RAS ONLY REFRESH CYCLE
(ADDR = A0~A8 ; OE , WE = DON'T CARE)



CBR REFRESH CYCLE
(A0~A8 ; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH ; $\overline{OE}$ = LOW)

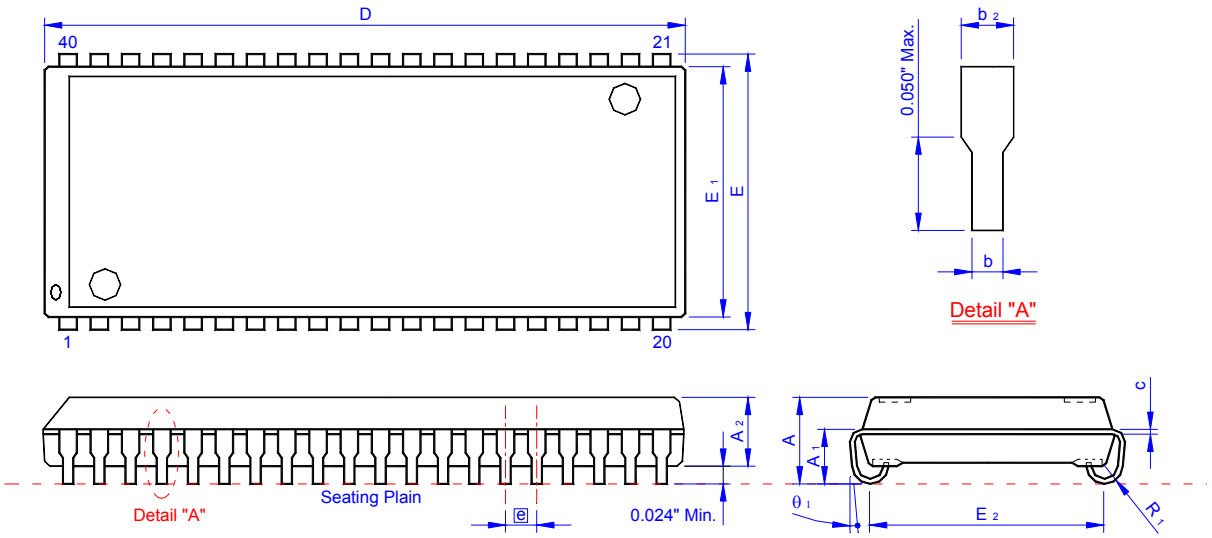


Note : 1. t_{OFF1} is reference from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

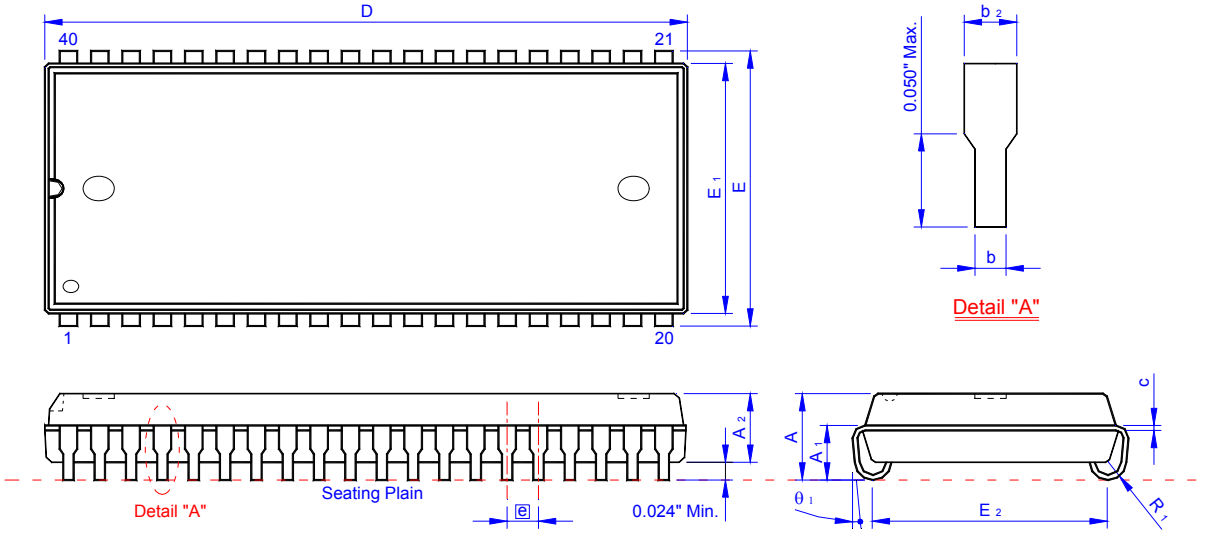
PACKING DIMENSIONS

40-LEAD SOJ(400mil)

SECTION I



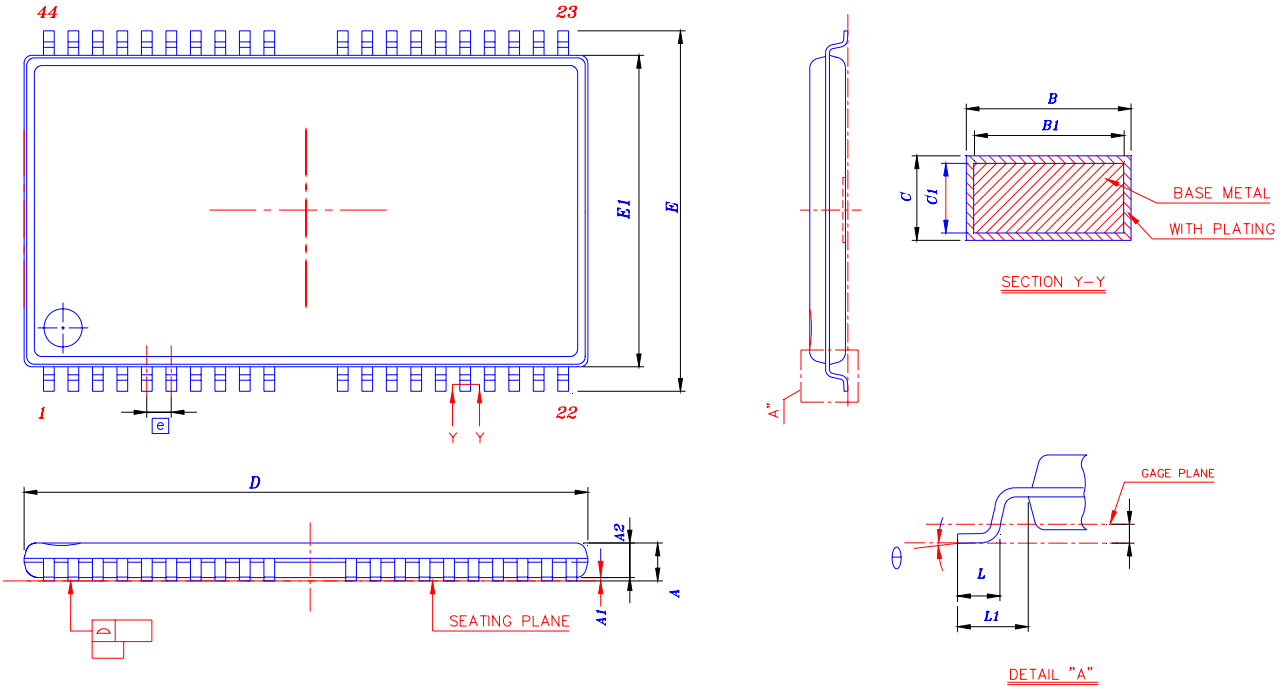
SECTION II



Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	3.250	3.510	3.760	0.128	0.138	0.148	E	10.920	11.176	11.430	0.430	0.440	0.450
A 1	2.080	___	___	0.082	___	___	E 1	10.030	10.160	10.290	0.395	0.400	0.405
A 2	2.790 REF			0.110 REF			E 2	9.40 BSC			0.370 BSC		
b	0.380	0.460	0.560	0.015	0.018	0.022	R 1	0.760	0.890	1.020	0.030	0.035	0.040
b2	0.635 REF			0.025 REF			θ 1	0°	___	10°	0°	___	10°
c	0.180	0.250	0.360	0.007	0.010	0.014	D	25.91	26.040	26.290	1.02	1.025	1.035
e	1.270 BSC			0.050 BSC									

PACKING **DIMENSIONS**

40 / 44-LEAD **TSOP(II)** **DRAM(400mil)**



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	——	——	1.20	——	——	0.047
A1	0.05	——	0.15	0.002	——	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.042
b	0.30	——	0.45	0.012	——	0.018
b1	0.30	0.35	0.40	0.012	0.014	0.016
c	0.12	——	0.21	0.005	——	0.008
c1	0.10	——	0.16	0.004	——	0.006
D	18.28	18.41	18.54	0.720	0.725	0.730
ZD	0.805 REF			0.0317 REF		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.4
L	0.40	0.59	0.69	0.016	0.023	0.027
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.0315 BSC		
θ	O° ~ 7° REF			O° ~ 7° REF		

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