

Alexander Martinez

EGCP281

Multiplexer: Binary to Hexadecimal

Mux.vhd

```
Mux_official.vhd  x Mux_TB .vhd  x Top_official.vhd  x Untitled 4  x |  
/home/alex/Downloads/Mux_official.vhd  
Q | S | ← | → | X | D | C | X | // | E | ? |  
28  
29      -- Uncomment the following library declaration if instantiating  
30      -- any Xilinx leaf cells in this code.  
31      --library UNISIM;  
32      --use UNISIM.VComponents.all;  
33  
34  entity Mux is  
35      Port ( Mux_in : in STD_LOGIC_VECTOR (7 downto 0);  
36          Sel : in STD_LOGIC_VECTOR (2 downto 0);  
37          Mux_out : out STD_LOGIC );  
38 end Mux;  
39  
40  architecture Behavioral of Mux is  
41  
42  begin  
43  
44  O Mux_out <= Mux_in(0) when sel = "000" else  
45          Mux_in(1) when sel = "001" else  
46          Mux_in(2) when sel = "010" else  
47          Mux_in(3) when sel = "011" else  
48          Mux_in(4) when sel = "100" else  
49          Mux_in(5) when sel = "101" else  
50          Mux_in(6) when sel = "110" else  
51  
52  
53  
54  
55  
56  
57          Mux_in(7);  
58  
59 end Behavioral;  
60
```

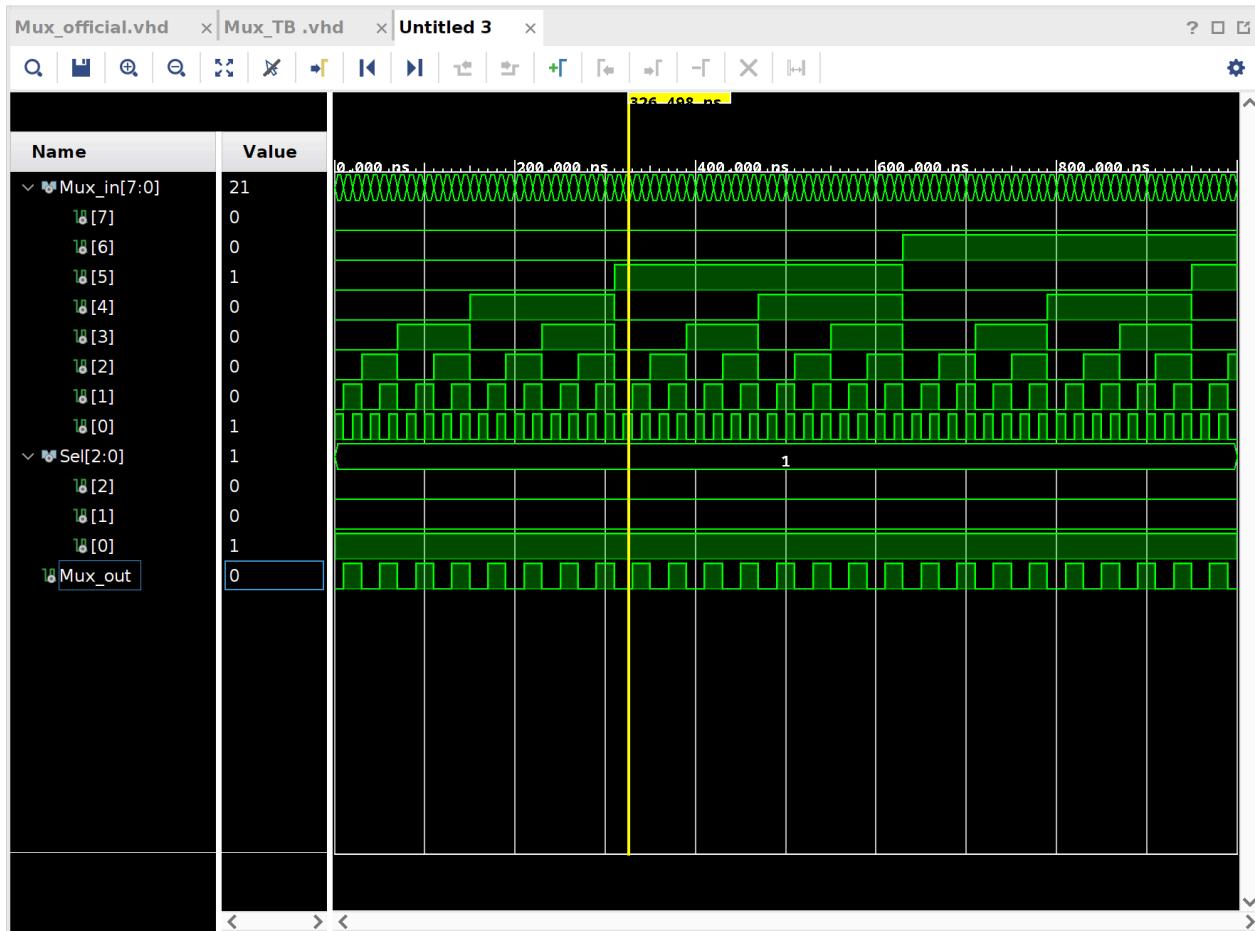
Top.vhd

```

3 ;
4 entity Top is
5     Port ( W, X, Y, Z : in STD_LOGIC;
6         AN : out STD_LOGIC_VECTOR (7 downto 0);
7         Cath : out STD_LOGIC_VECTOR (7 downto 0));
8 end Top;
9 ;
0 architecture Behavioral of Top is
1 component Mux is
2     Port ( Mux_in : in STD_LOGIC_VECTOR (7 downto 0);
3         Sel : in STD_LOGIC_VECTOR (2 downto 0);
4         Mux_out : out STD_LOGIC );
5 end component;
6 signal N_Z: std_logic:= '0';
7 begin
8     AN <= "11111110";
9     N_Z <= not Z;
0     --- please change below circuit based on Tech#0, Tech#1 or Tech #2
1     Unit_A: Mux port map (Mux_in(0)>= Z, Mux_in(1)>= '0', Mux_in(2)>= N_Z, Mux_in(3)>= '0', Mux_in(4)>= '0', Mux_in(5)>= Z, Mux_in(6)>= Z, Mux_in(7)>= '0',
2     Sel(0) => Y , Sel(1) => X, Sel(2) => W, Mux_out => Cath(0) );
3     Unit_B: Mux port map (Mux_in(0)>= '0', Mux_in(1)>= '0', Mux_in(2)>= Z, Mux_in(3)>= N_Z, Mux_in(4)>= '0', Mux_in(5)>= Z, Mux_in(6)>= N_Z, Mux_in(7)>= '1',
4     Sel(0) => Y, Sel(1) => X, Sel(2) => W, Mux_out => Cath(1) );
5     Unit_C: Mux port map (Mux_in(0)>= '0', Mux_in(1)>= N_Z, Mux_in(2)>= '0', Mux_in(3)>= '0', Mux_in(4)>= '0', Mux_in(5)>= '0', Mux_in(6)>= N_Z, Mux_in(7)>= '1',
6     Sel(0) => Y, Sel(1) => X, Sel(2) => W, Mux_out => Cath(2) );
7     Unit_D: Mux port map (Mux_in(0)>= Z, Mux_in(1)>= '0', Mux_in(2)>= N_Z, Mux_in(3)>= Z, Mux_in(4)>= '0', Mux_in(5)>= N_Z, Mux_in(6)>= '0', Mux_in(7)>= Z,
8     Sel(0) => Y, Sel(1) => X, Sel(2) => W, Mux_out => Cath(3) );
9     Unit_E: Mux port map (Mux_in(0)>= Z, Mux_in(1)>= Z, Mux_in(2)>= '1', Mux_in(3)>= Z, Mux_in(4)>= Z, Mux_in(5)>= '0', Mux_in(6)>= '0', Mux_in(7)>= '0',
0     Sel(0) => Y, Sel(1) => X, Sel(2) => W, Mux_out => Cath(4) );
1     Unit_F: Mux port map (Mux_in(0)>= Z, Mux_in(1)>= '1', Mux_in(2)>= '0', Mux_in(3)>= Z, Mux_in(4)>= '0', Mux_in(5)>= '0', Mux_in(6)>= Z, Mux_in(7)>= '0',
2     Sel(0) => Y, Sel(1) => X, Sel(2) => W, Mux_out => Cath(5) );
3     Unit_G: Mux port map (Mux_in(0)>= '1', Mux_in(1)>= '0', Mux_in(2)>= '0', Mux_in(3)>= Z, Mux_in(4)>= '0', Mux_in(5)>= '0', Mux_in(6)>= N_Z, Mux_in(7)>= '0',
4     Sel(0) => Y, Sel(1) => X, Sel(2) => W, Mux_out => Cath(6) );
5     Unit_DP: Mux port map (Mux_in(0)>= '1', Mux_in(1)>= '1', Mux_in(2)>= '1', Mux_in(3)>= '1', Mux_in(4)>= '1', Mux_in(5)>= '1', Mux_in(6)>= '1', Mux_in(7)>= '1',
6     Sel(0) => Y, Sel(1) => X, Sel(2) => W, Mux_out => Cath(7) );
7 ;
8 ;
9 end Behavioral;
0 ;

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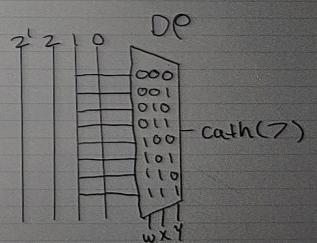
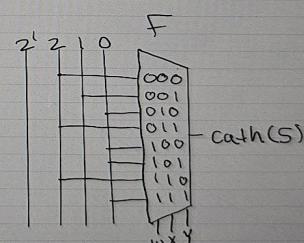
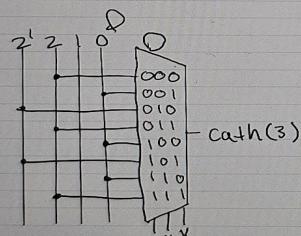
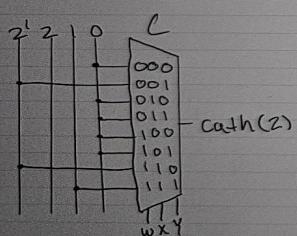
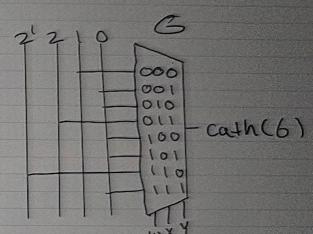
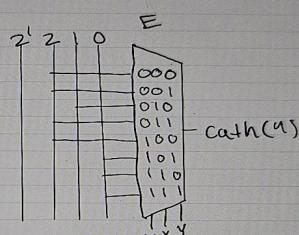
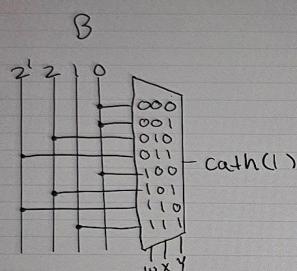
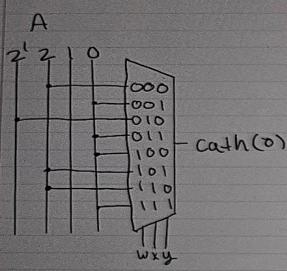
Simulation Waveform



W	X	Y	Z	A	B	C	D	E	F	G	Dp
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	1
0	0	1	1	0	0	0	0	1	1	0	1
0	1	0	0	1	0	0	1	1	0	0	1
0	1	0	1	0	1	0	0	1	0	0	1
0	1	1	0	0	1	0	0	0	0	0	1
0	1	1	1	0	0	0	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1
1	0	1	0	0	0	0	1	0	0	0	1
1	0	1	1	1	1	0	0	0	0	0	1
1	1	0	0	0	1	1	0	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0	1
1	1	1	0	0	1	1	0	0	0	0	1
1	1	1	1	1	0	1	1	0	0	0	1

A

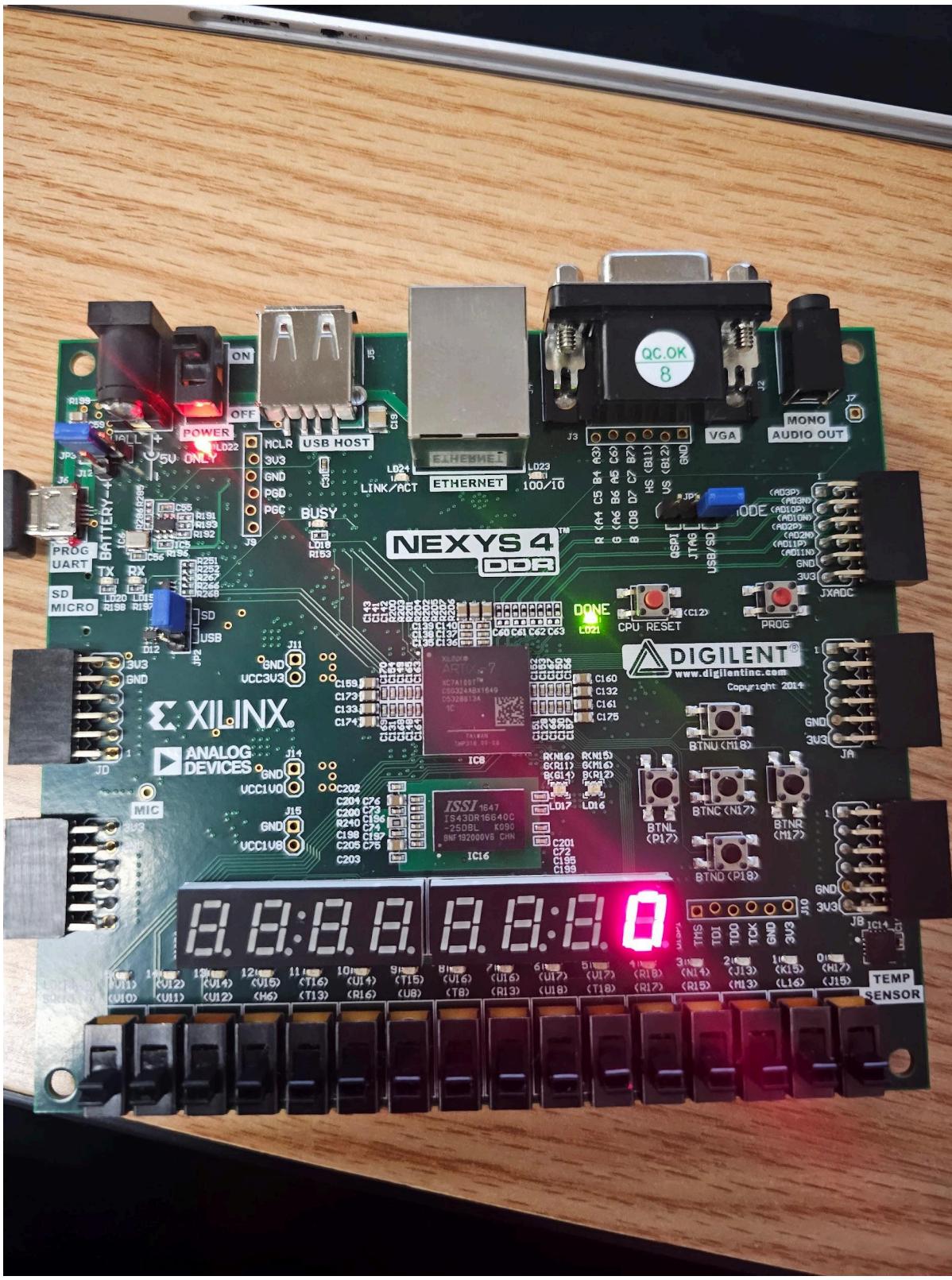
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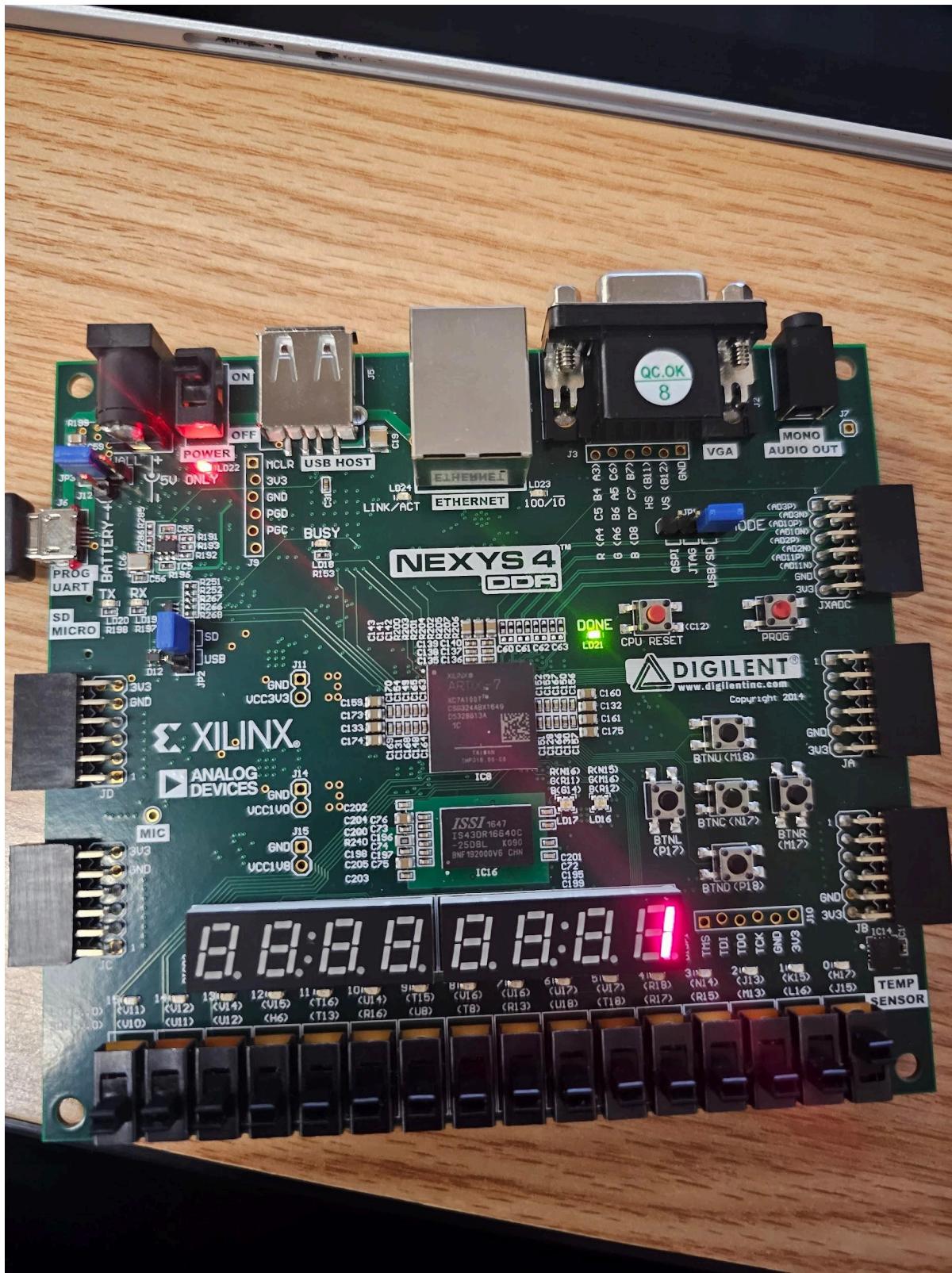


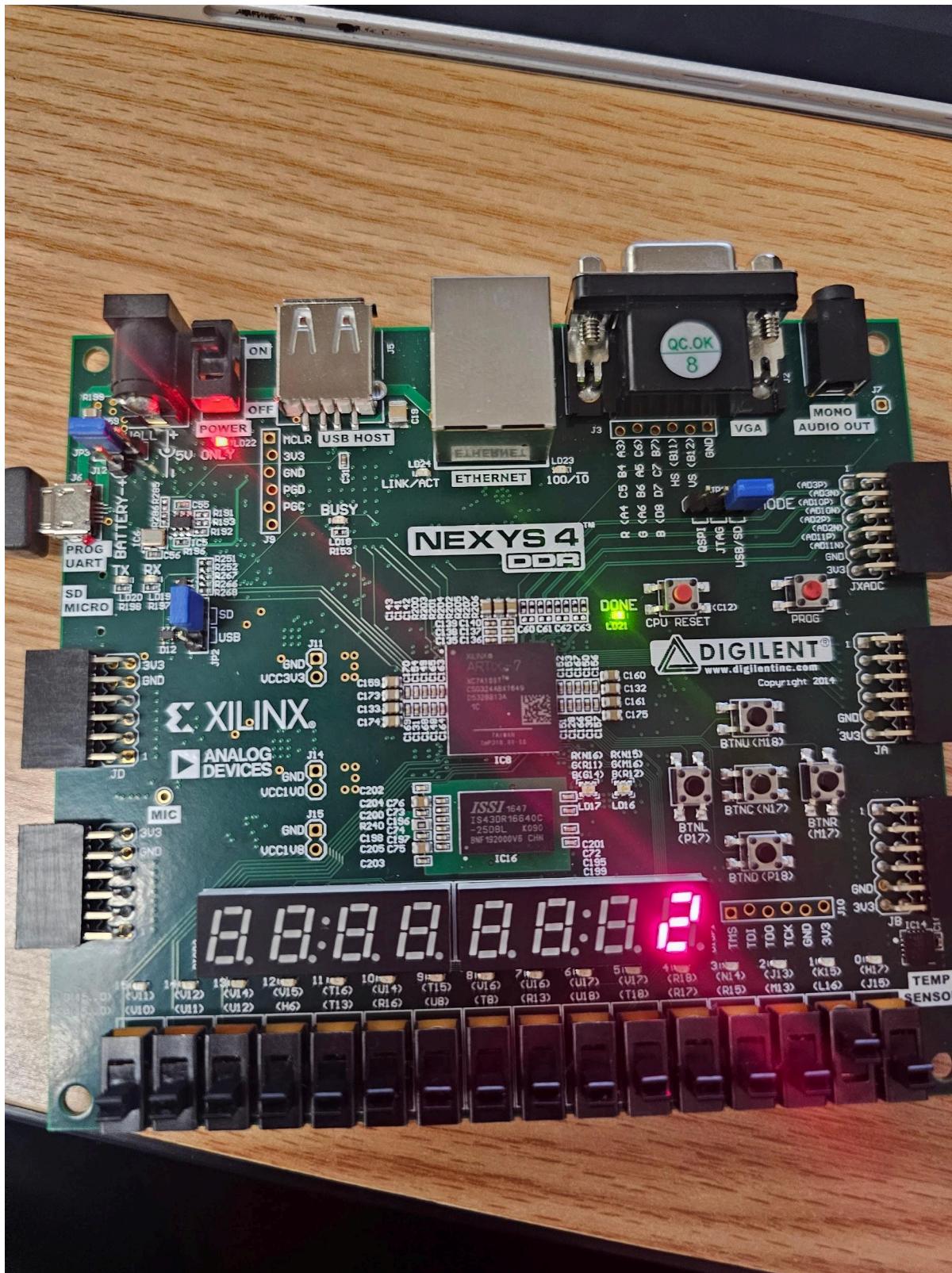
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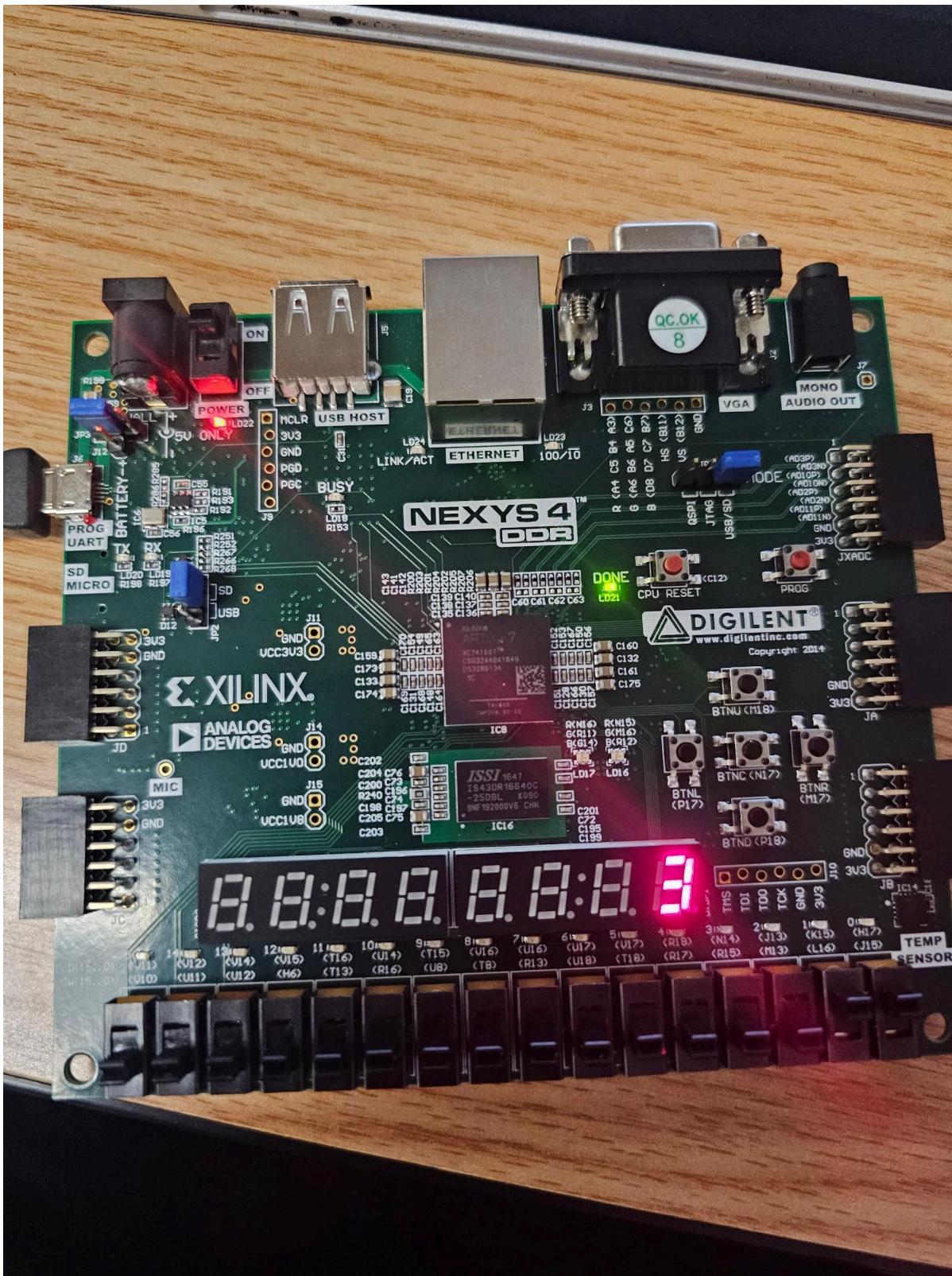
1  set_property PACKAGE_PIN M13 [get_ports X]
2  set_property PACKAGE_PIN L16 [get_ports Y]
3  set_property PACKAGE_PIN R15 [get_ports W]
4  set_property IOSTANDARD LVCMOS18 [get_ports {Cath[7]}]
5  set_property IOSTANDARD LVCMOS18 [get_ports {Cath[6]}]
6  set_property IOSTANDARD LVCMOS18 [get_ports {Cath[5]}]
7  set_property IOSTANDARD LVCMOS18 [get_ports {Cath[4]}]
8  set_property IOSTANDARD LVCMOS18 [get_ports {Cath[3]}]
9  set_property IOSTANDARD LVCMOS18 [get_ports {Cath[2]}]
10 set_property IOSTANDARD LVCMOS18 [get_ports {Cath[1]}]
11 set_property IOSTANDARD LVCMOS18 [get_ports {Cath[0]}]
12 set_property IOSTANDARD LVCMOS18 [get_ports {An[7]}]
13 set_property IOSTANDARD LVCMOS18 [get_ports {An[6]}]
14 set_property IOSTANDARD LVCMOS18 [get_ports {An[5]}]
15 set_property IOSTANDARD LVCMOS18 [get_ports {An[4]}]
16 set_property IOSTANDARD LVCMOS18 [get_ports {An[3]}]
17 set_property IOSTANDARD LVCMOS18 [get_ports {An[2]}]
18 set_property IOSTANDARD LVCMOS18 [get_ports {An[1]}]
19 set_property IOSTANDARD LVCMOS18 [get_ports {An[0]}]
20 set_property PACKAGE_PIN T10 [get_ports {Cath[0]}]
21 set_property PACKAGE_PIN R10 [get_ports {Cath[1]}]
22 set_property PACKAGE_PIN K16 [get_ports {Cath[2]}]
23 set_property PACKAGE_PIN K13 [get_ports {Cath[3]}]
24 set_property PACKAGE_PIN P15 [get_ports {Cath[4]}]
25 set_property PACKAGE_PIN T11 [get_ports {Cath[5]}]
26 set_property PACKAGE_PIN L18 [get_ports {Cath[6]}] [get_ports {Cath[6]}]
27 set_property PACKAGE_PIN H15 [get_ports {Cath[7]}]
28 set_property PACKAGE_PIN J15 [get_ports {An[0]}]
29 set_property PACKAGE_PIN J18 [get_ports {An[1]}]
30 set_property PACKAGE_PIN T9 [get_ports {An[2]}]
31 set_property PACKAGE_PIN J14 [get_ports {An[3]}]
32 set_property PACKAGE_PIN P14 [get_ports {An[4]}]
33 set_property PACKAGE_PIN T14 [get_ports {An[5]}]
34 set_property PACKAGE_PIN K2 [get_ports {An[6]}]
35 set_property PACKAGE_PIN U13 [get_ports {An[7]}]
36 set_property IOSTANDARD LVCMOS18 [get_ports X]
37 set_property IOSTANDARD LVCMOS18 [get_ports Y]
38 set_property IOSTANDARD LVCMOS18 [get_ports W]
39 set_property IOSTANDARD LVCMOS18 [get_ports Z]
40
41 set_property IOSTANDARD LVCMOS18 [get_ports {AN[7]}]
42 set_property IOSTANDARD LVCMOS18 [get_ports {AN[6]}]
43 set_property IOSTANDARD LVCMOS18 [get_ports {AN[5]}]
44 set_property IOSTANDARD LVCMOS18 [get_ports {AN[4]}]
45 set_property IOSTANDARD LVCMOS18 [get_ports {AN[3]}]
46 set_property IOSTANDARD LVCMOS18 [get_ports {AN[2]}]
47 set_property IOSTANDARD LVCMOS18 [get_ports {AN[1]}]
48 set_property IOSTANDARD LVCMOS18 [get_ports {AN[0]}]
49 set_property PACKAGE_PIN J15 [get_ports Z]
50 set_property PACKAGE_PIN J17 [get_ports {AN[0]}]
51 set_property PACKAGE_PIN J18 [get_ports {AN[1]}]
52 set_property PACKAGE_PIN T9 [get_ports {AN[2]}]
53 set_property PACKAGE_PIN J14 [get_ports {AN[3]}]
54 set_property PACKAGE_PIN P14 [get_ports {AN[4]}]
55 set_property PACKAGE_PIN T14 [get_ports {AN[5]}]
56 set_property PACKAGE_PIN K2 [get_ports {AN[6]}]
57 set_property PACKAGE_PIN I113 [get_ports {AN[7]}]

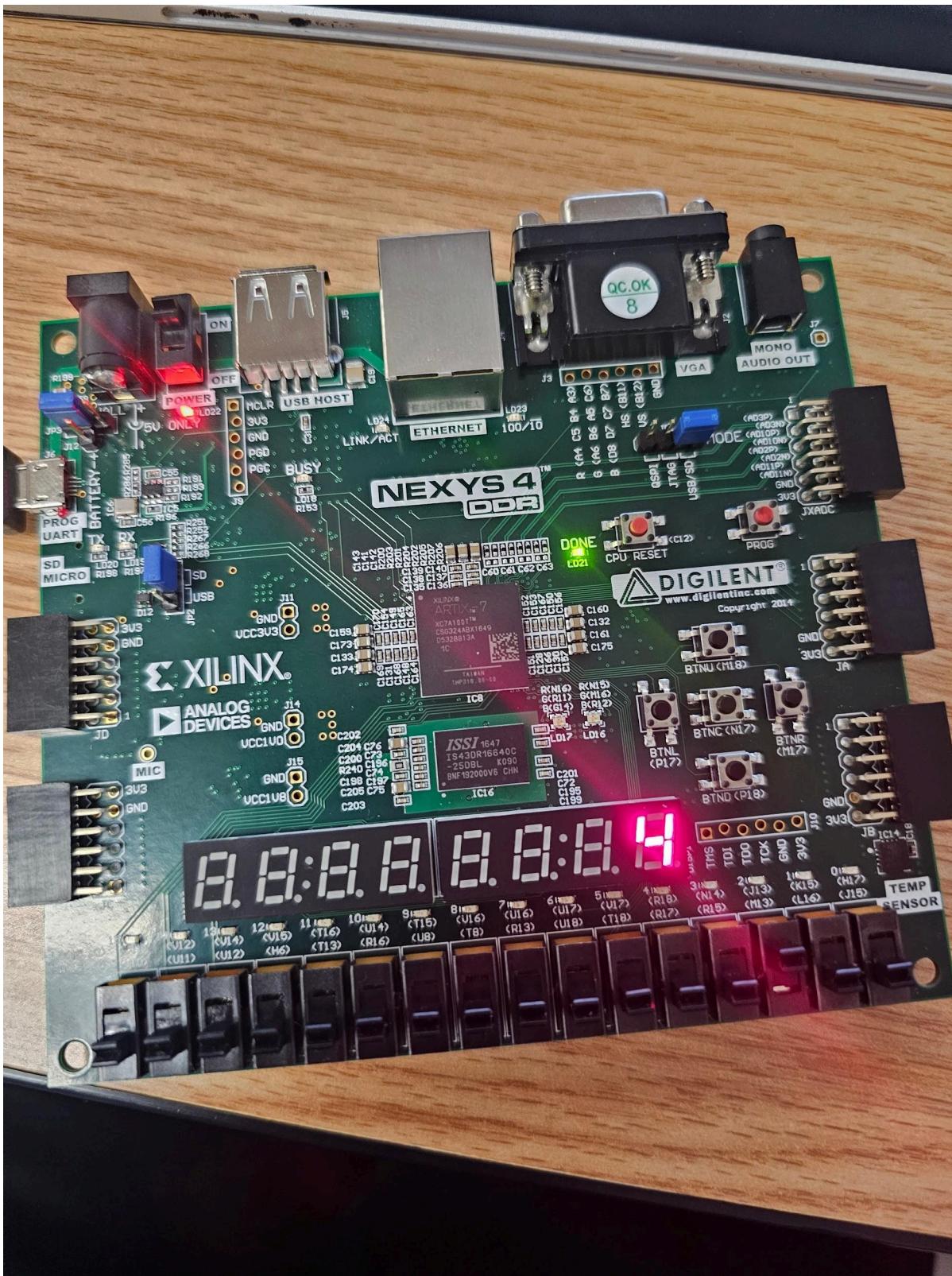
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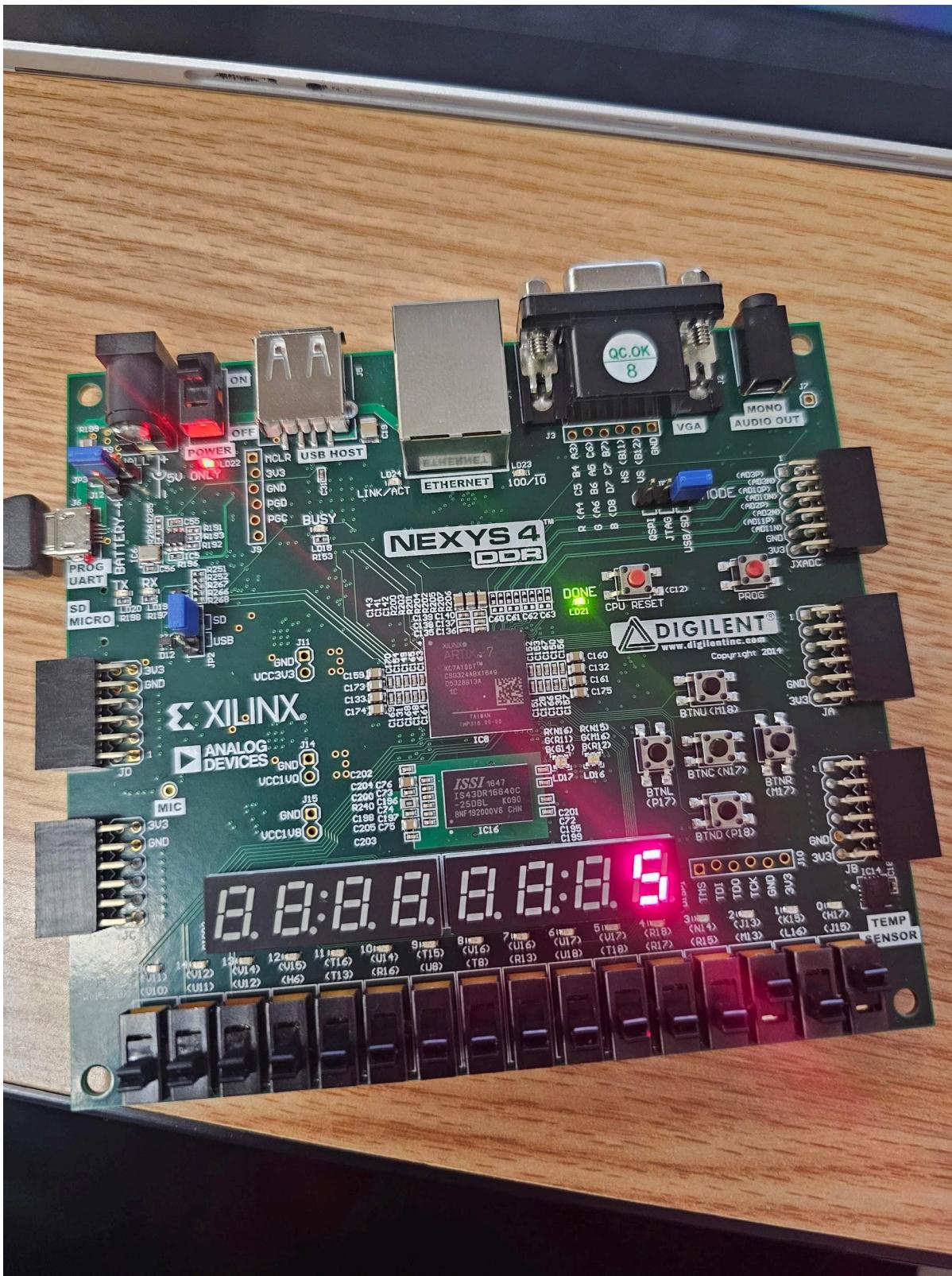


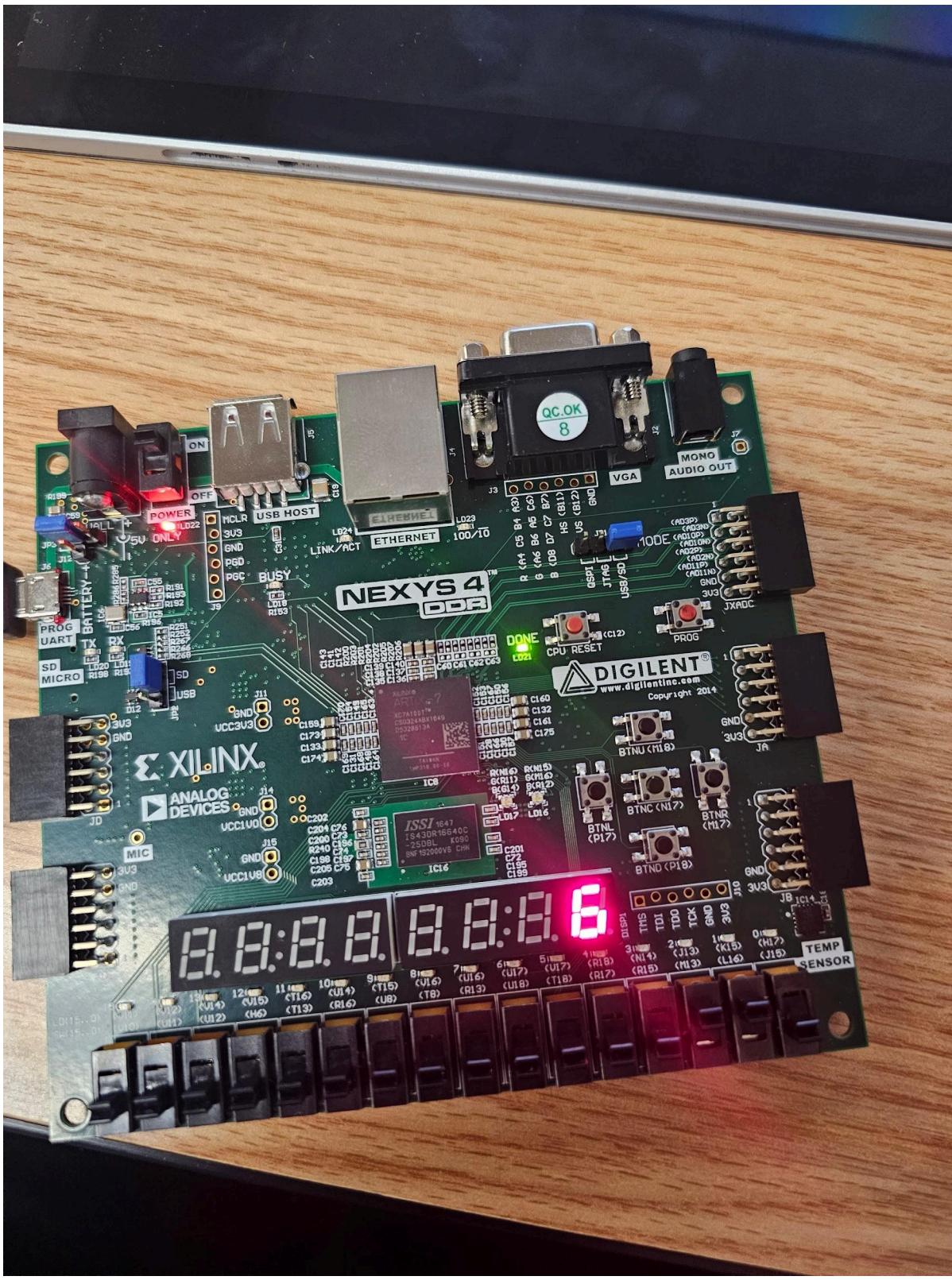


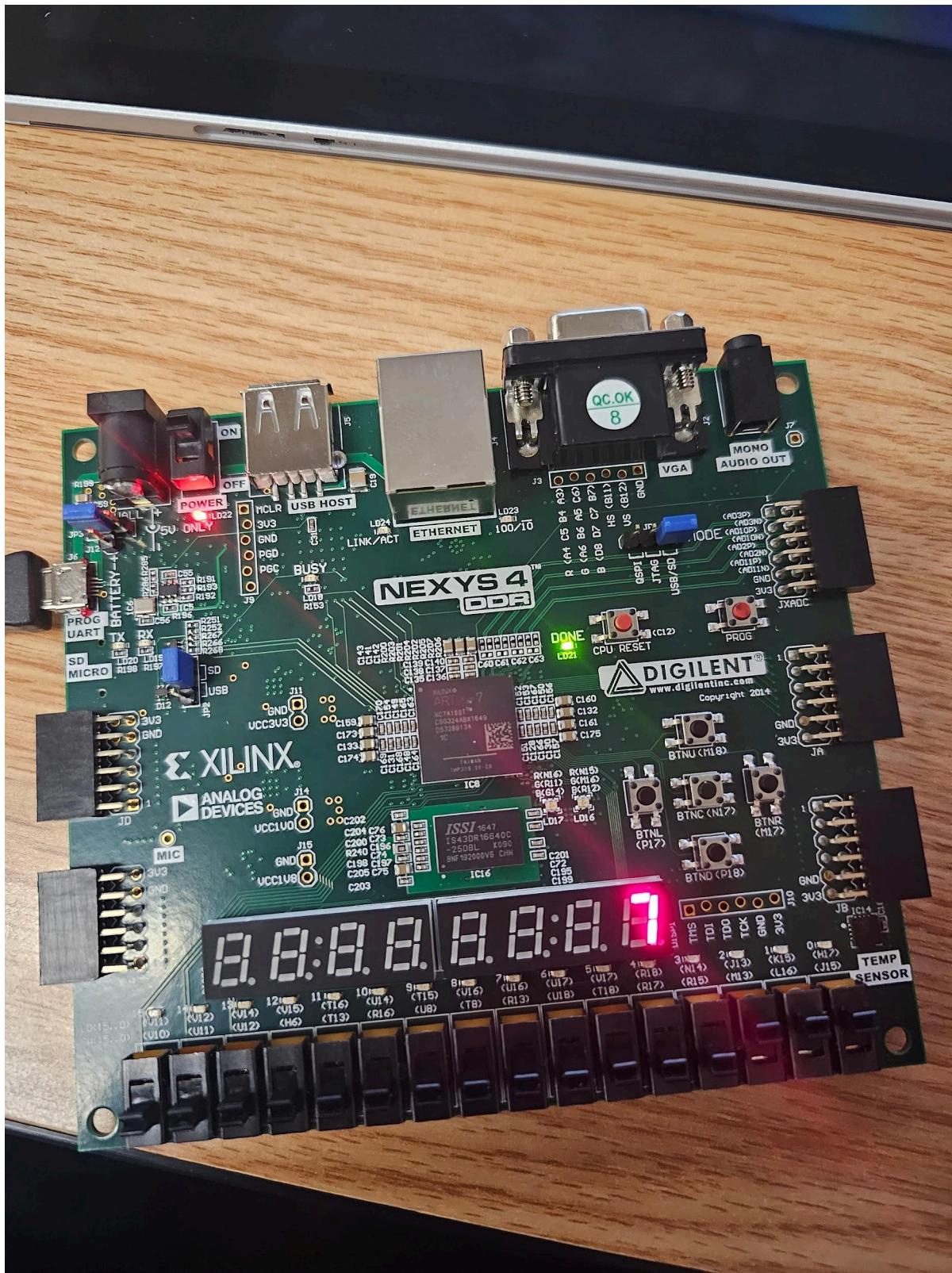


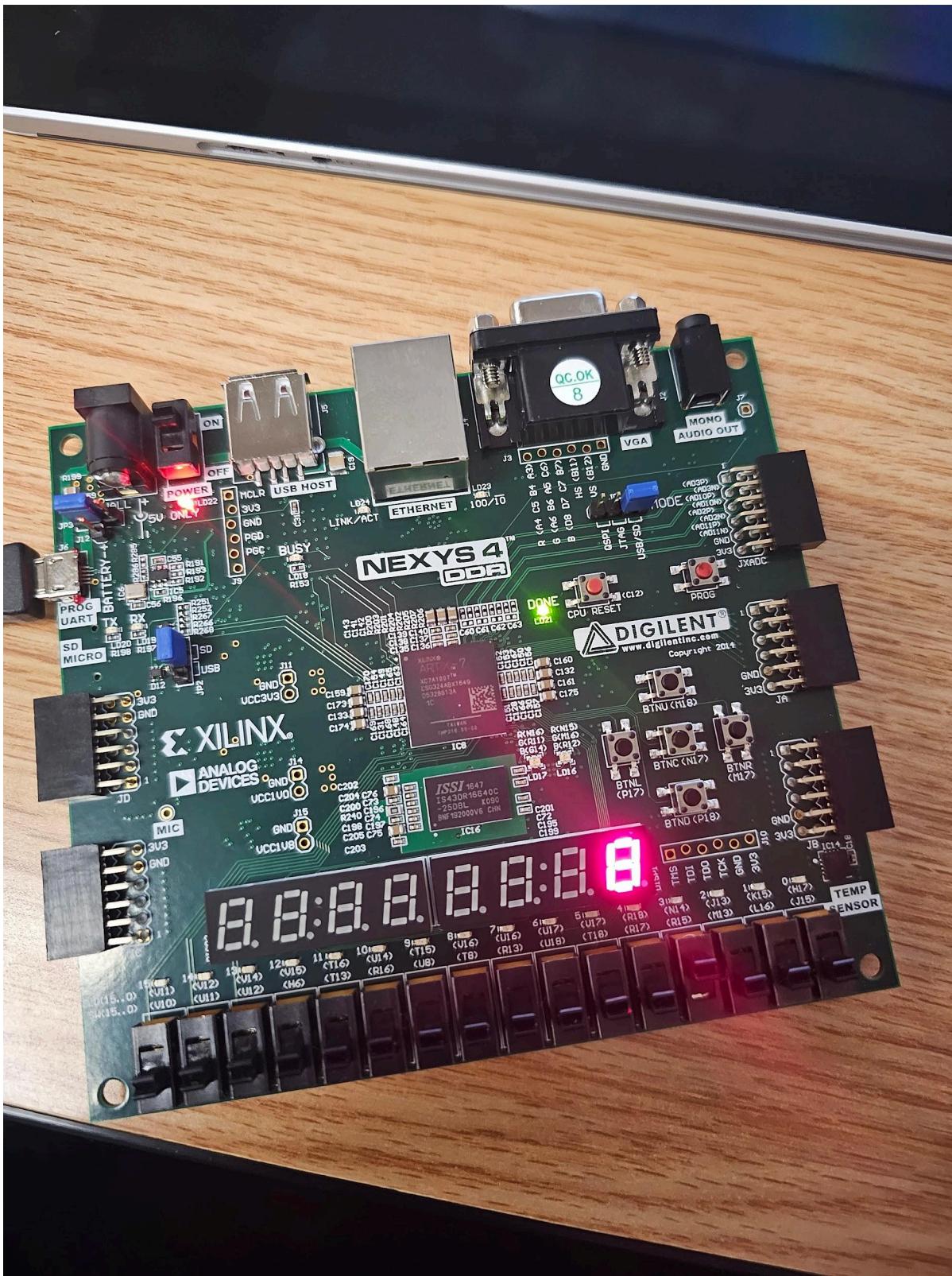


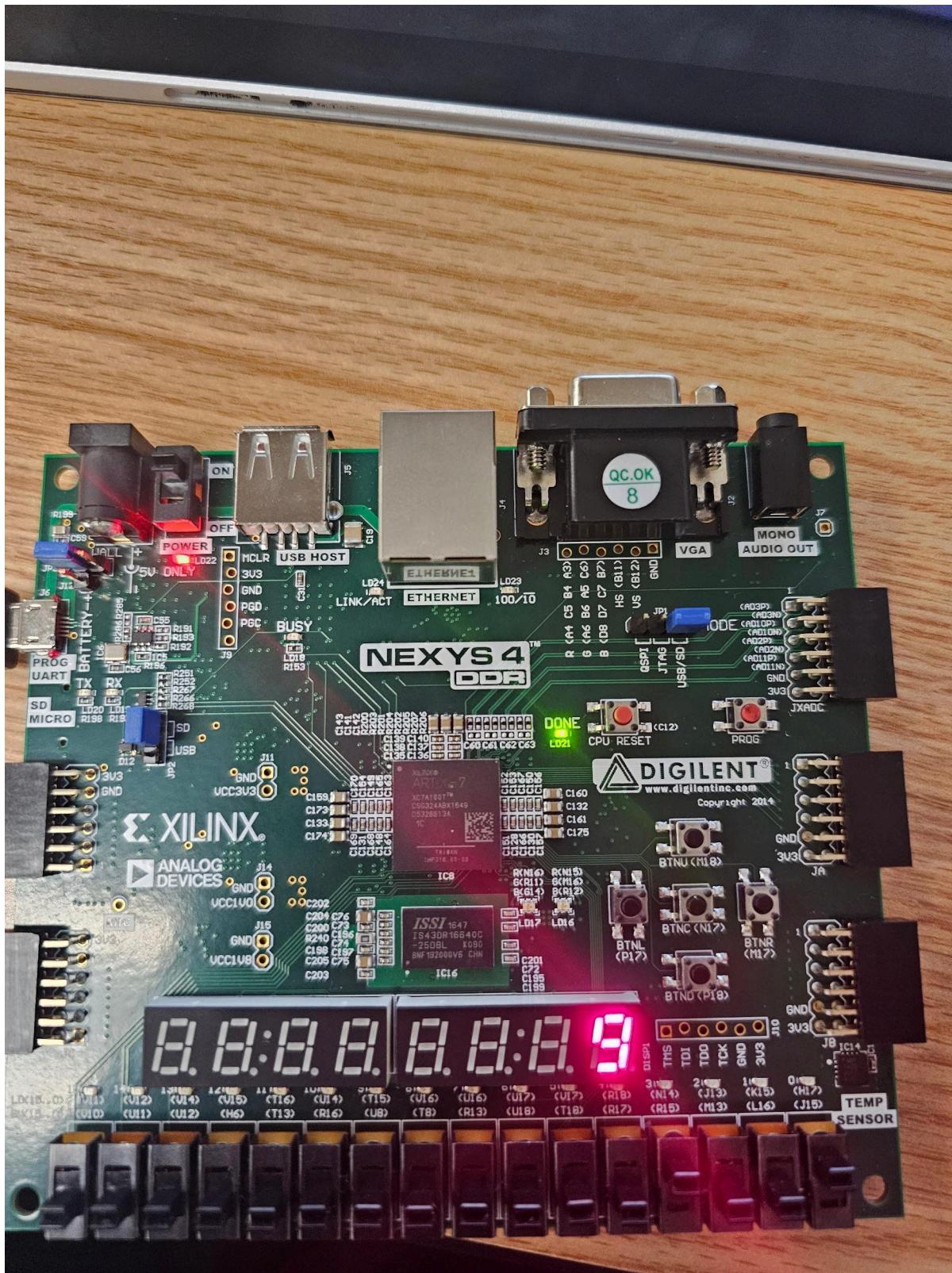


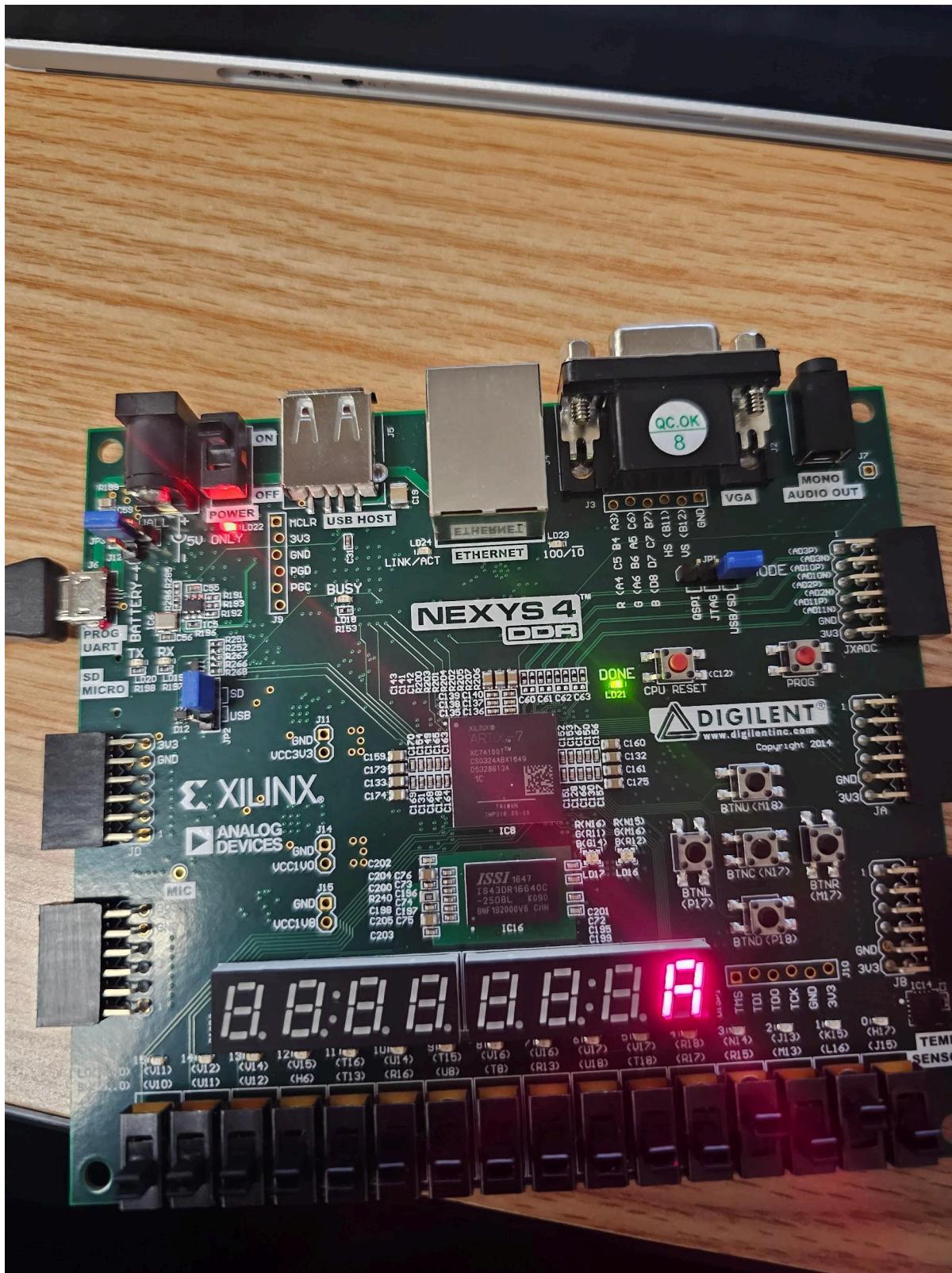


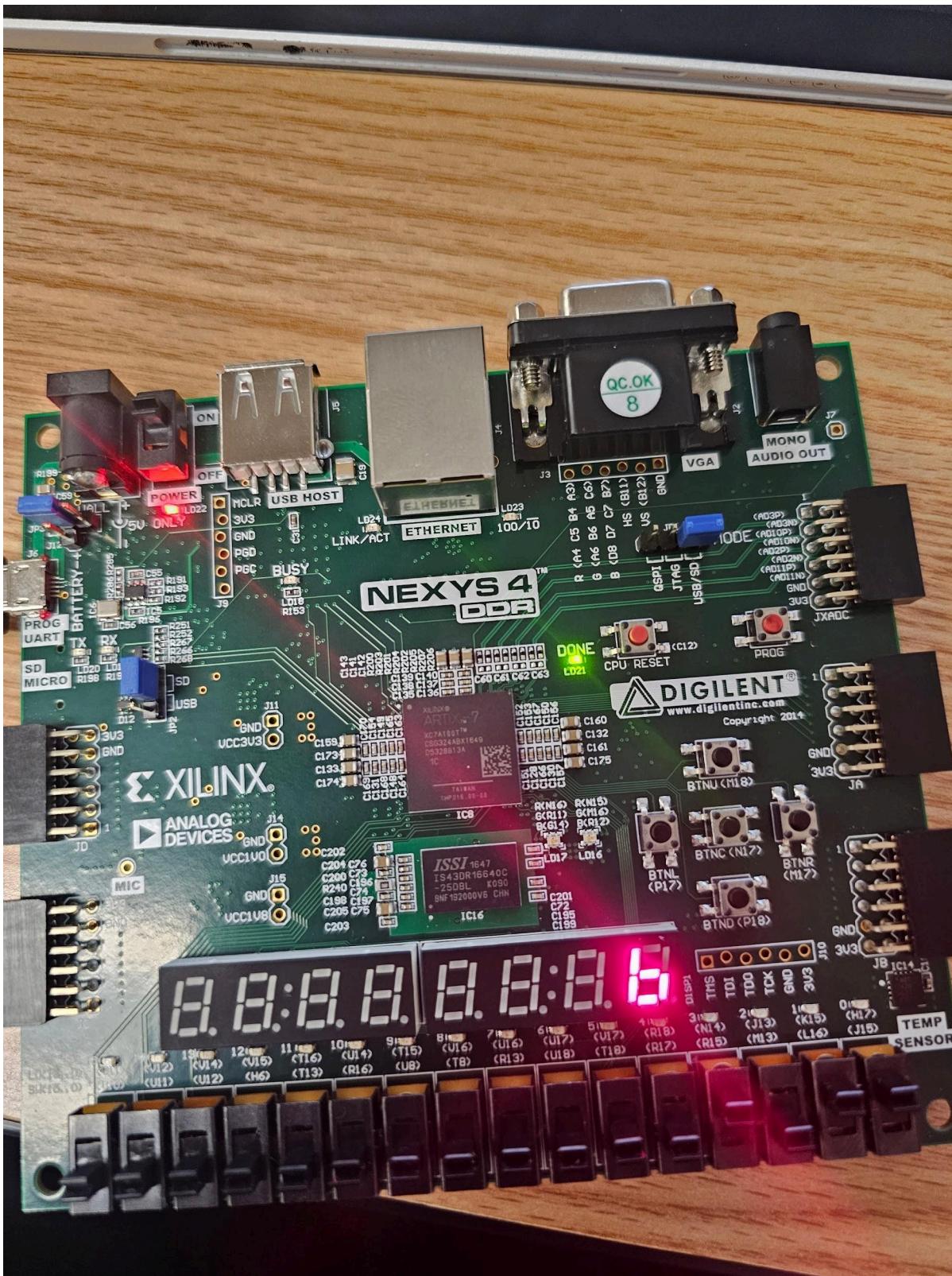


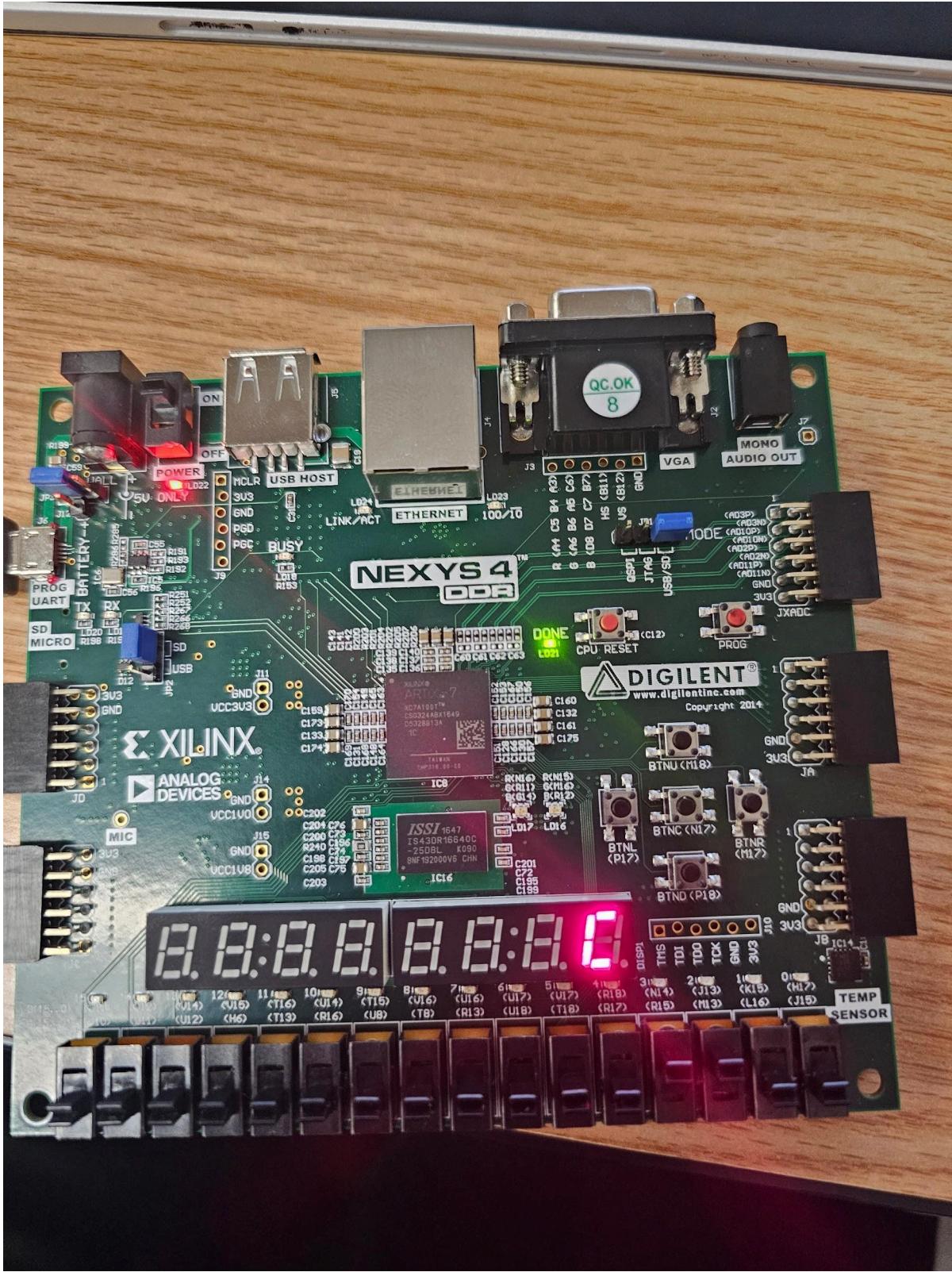


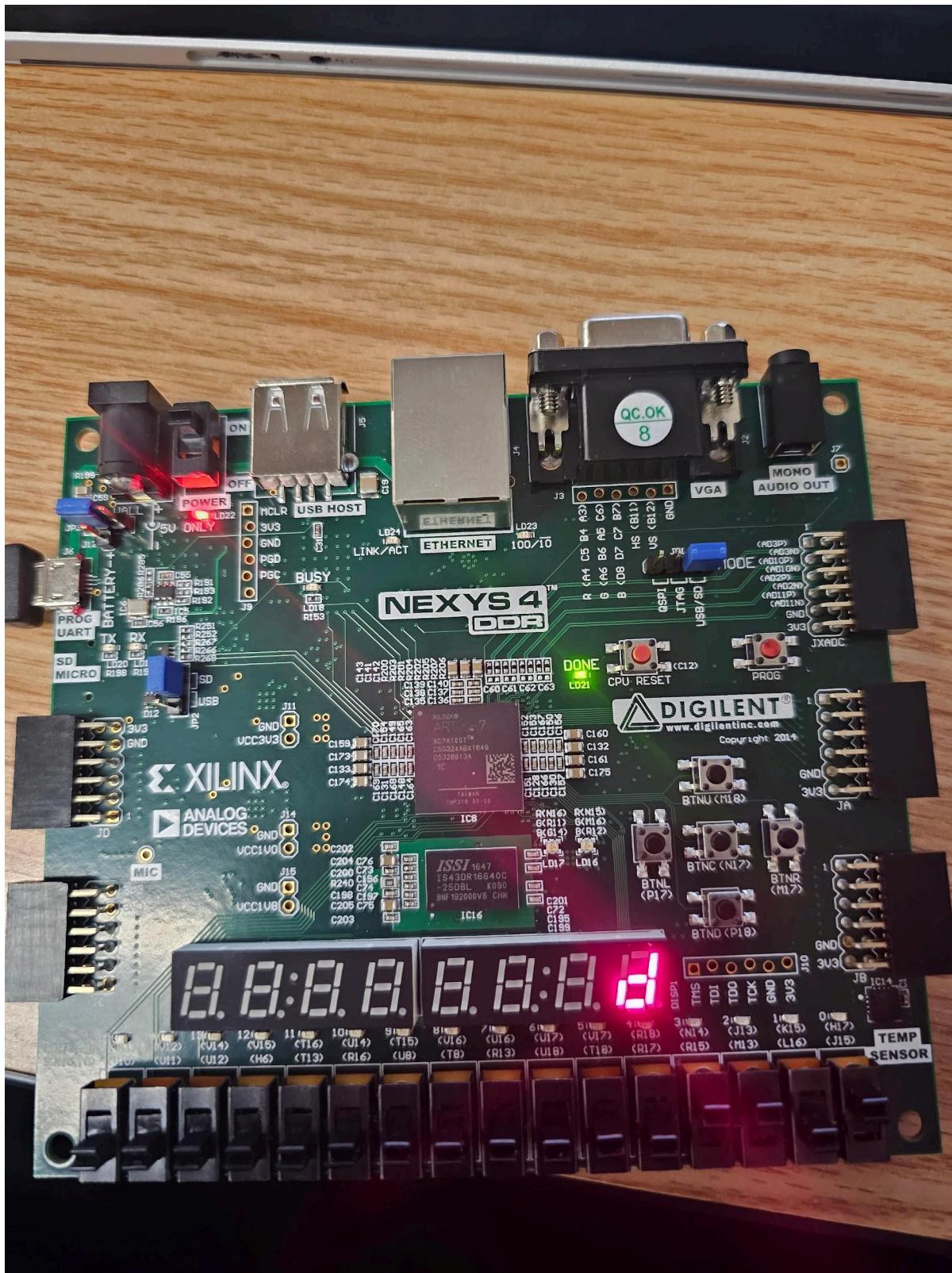


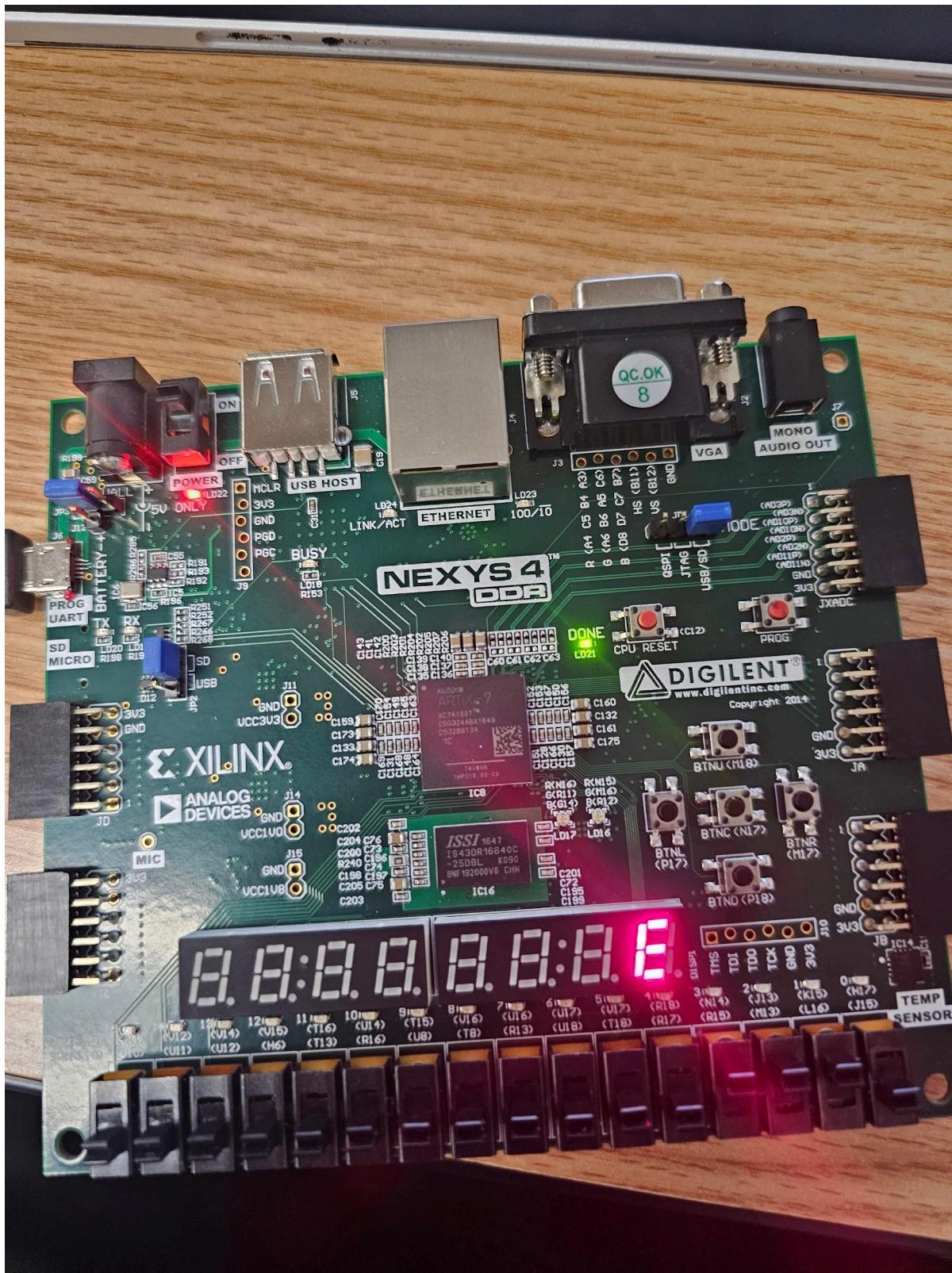


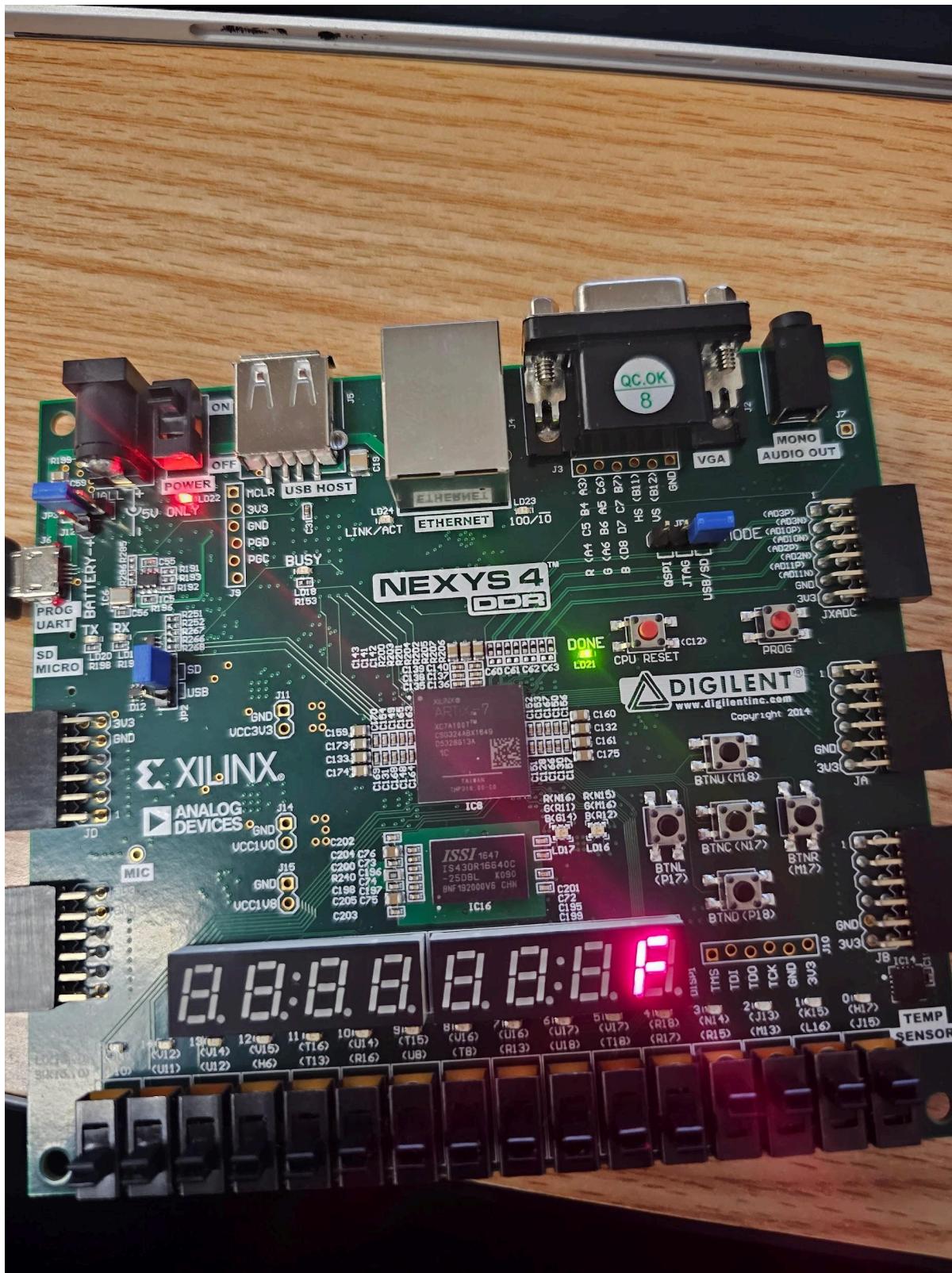












So the work I completed was about making a table that represented binary numbers in hexadecimal form. Then I used a multiplexer to know which inputs to select from either being, N_Z, Z, 0, or 1. And I also coded the Mux output and all of its possible combinations. THe only problems I had was when I added both the files at the same time so I was not able to get the correct waveform but inserting first the mux then the top was able to get me the right waveform.