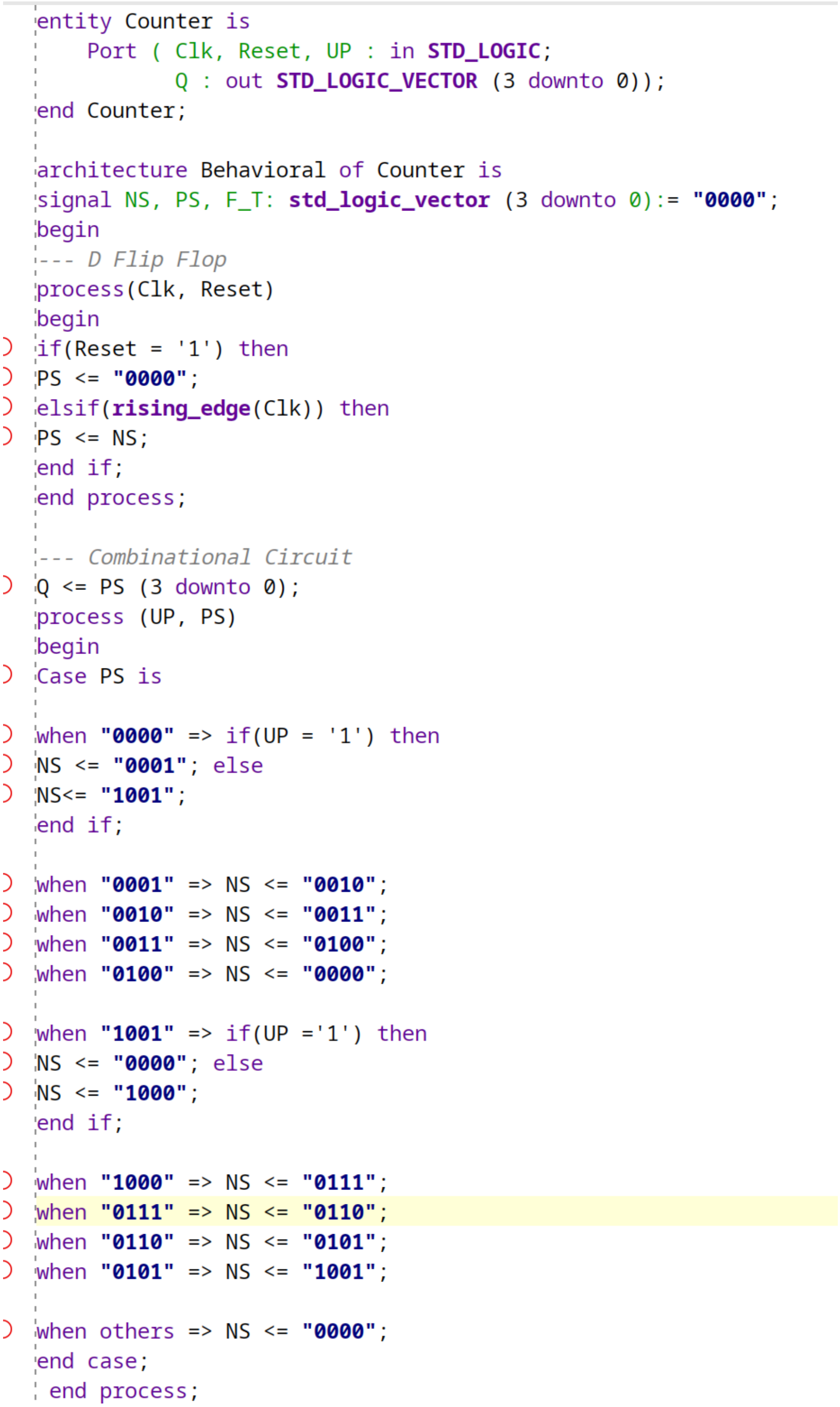
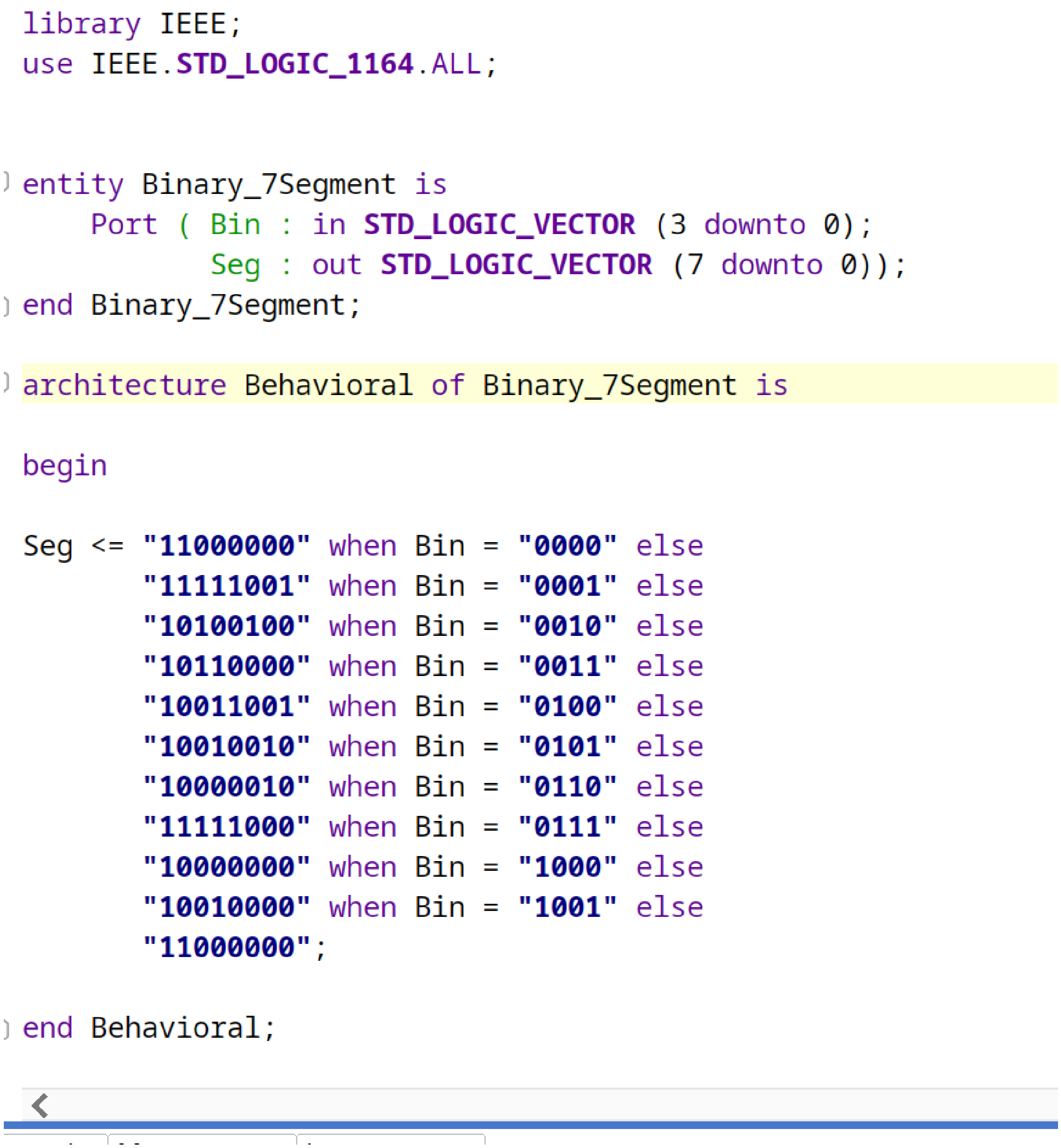
Alexander Martinez

EGCP281

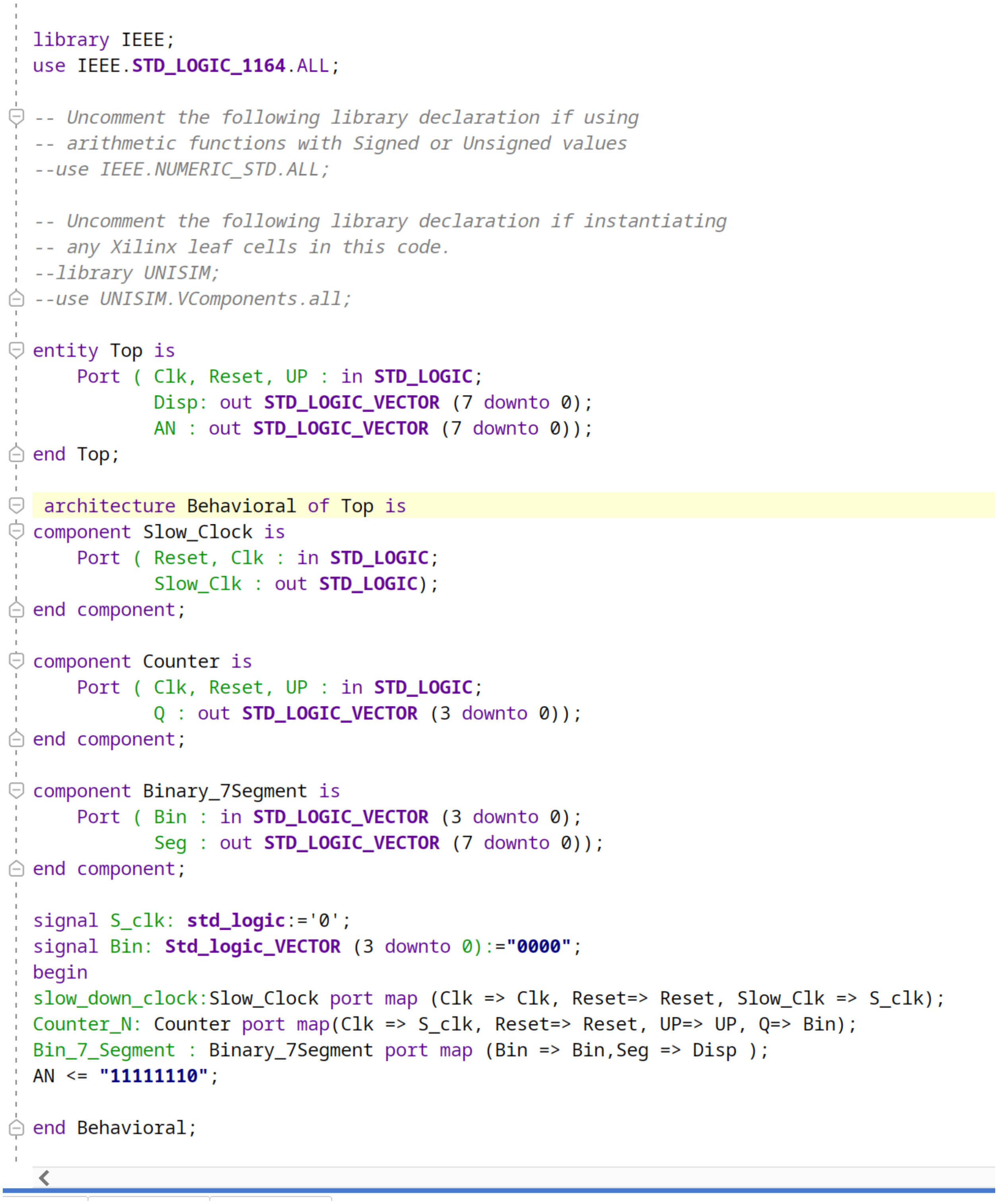
Mealy and Moore Machine



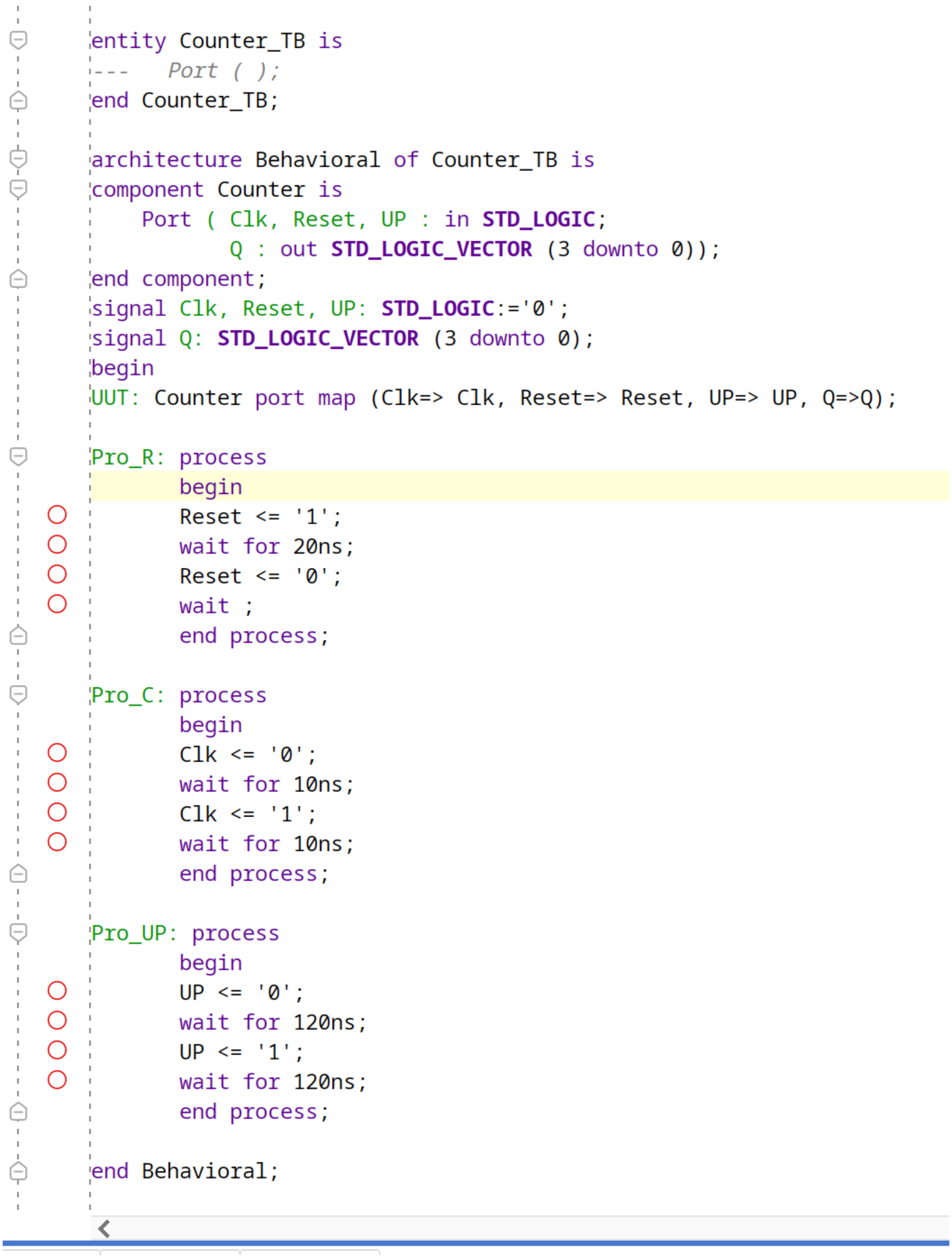
```
entity Counter is
    Port ( Clk, Reset, UP : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (3 downto 0));
end Counter;

architecture Behavioral of Counter is
signal NS, PS, F_T: std_logic_vector (3 downto 0):= "0000";
begin
--- D Flip Flop
process(Clk, Reset)
begin
if(Reset = '1') then
PS <= "0000";
elsif(rising_edge(Clk)) then
PS <= NS;
end if;
end process;

--- Combinational Circuit
Q <= PS (3 downto 0);
process (UP, PS)
begin
Case PS is

when "0000" => if(UP = '1') then
NS <= "0001"; else
NS<= "1001";
end if;

when "0001" => NS <= "0010";
when "0010" => NS <= "0011";
when "0011" => NS <= "0100";
when "0100" => NS <= "0000";

when "1001" => if(UP ='1') then
NS <= "0000"; else
NS <= "1000";
end if;

when "1000" => NS <= "0111";
when "0111" => NS <= "0110";
when "0110" => NS <= "0101";
when "0101" => NS <= "1001";

when others => NS <= "0000";
end case;
 end process;
```



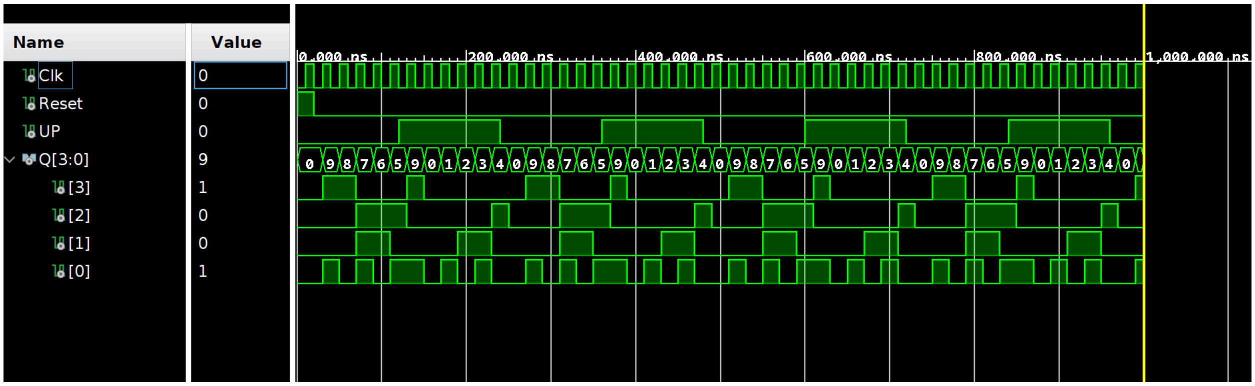
```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity Binary_7Segment is
    Port ( Bin : in STD_LOGIC_VECTOR (3 downto 0);
           Seg : out STD_LOGIC_VECTOR (7 downto 0));
end Binary_7Segment;

architecture Behavioral of Binary_7Segment is

begin

Seg <= "11000000" when Bin = "0000" else
       "11111001" when Bin = "0001" else
       "10100100" when Bin = "0010" else
       "10110000" when Bin = "0011" else
       "10011001" when Bin = "0100" else
       "10010010" when Bin = "0101" else
       "10000010" when Bin = "0110" else
       "11111000" when Bin = "0111" else
       "10000000" when Bin = "1000" else
       "10010000" when Bin = "1001" else
       "11000000";

end Behavioral;
```

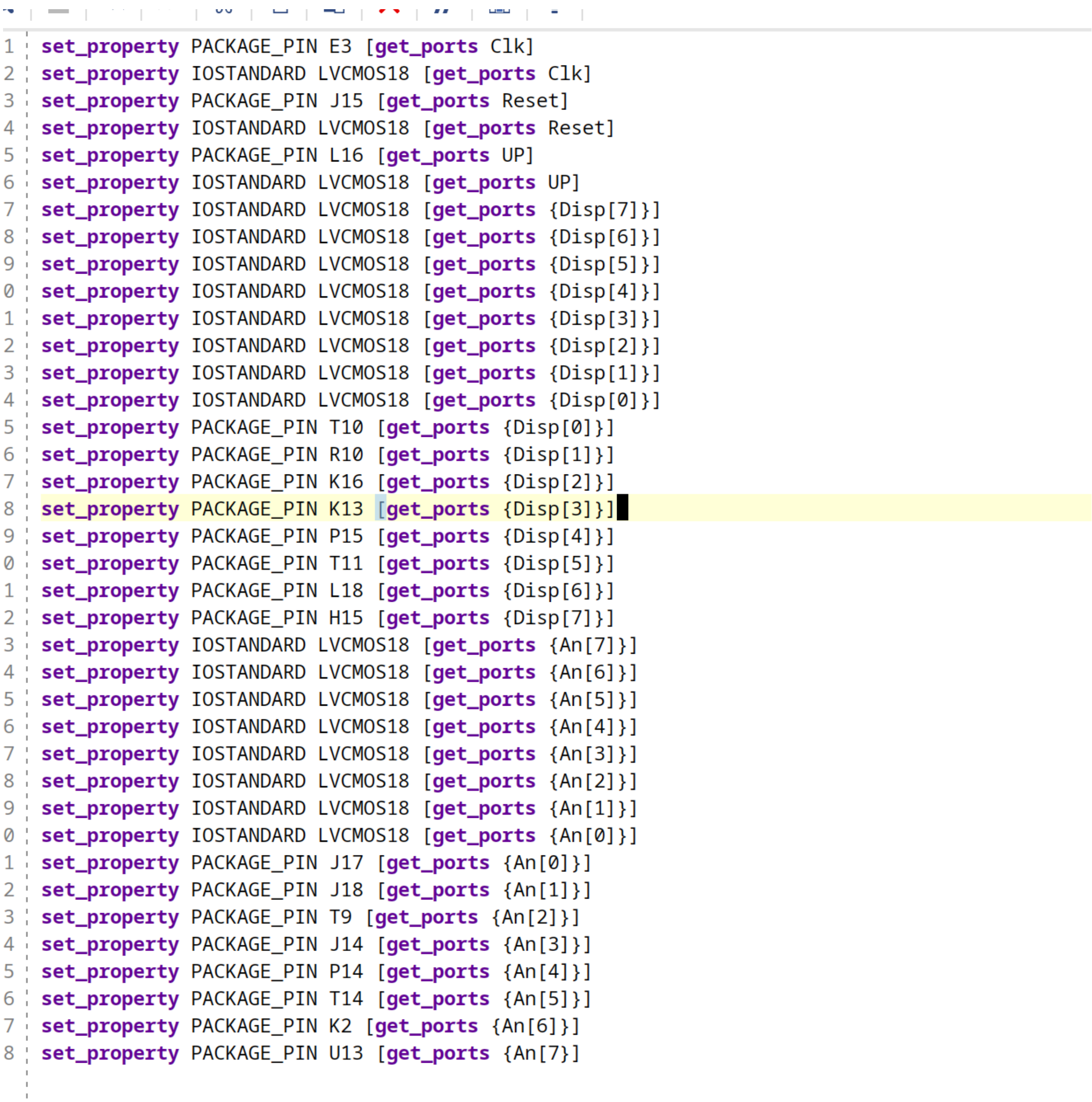


```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Top is
    Port ( Clk, Reset, UP : in STD_LOGIC;
           Disp: out STD_LOGIC_VECTOR (7 downto 0);
           AN : out STD_LOGIC_VECTOR (7 downto 0));
end Top;

 architecture Behavioral of Top is
component Slow_Clock is
    Port ( Reset, Clk : in STD_LOGIC;
           Slow_Clk : out STD_LOGIC);
end component;

component Counter is
    Port ( Clk, Reset, UP : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (3 downto 0));
end component;

component Binary_7Segment is
    Port ( Bin : in STD_LOGIC_VECTOR (3 downto 0);
           Seg : out STD_LOGIC_VECTOR (7 downto 0));
end component;

signal S_clk: std_logic:='0';
signal Bin: Std_logic_VECTOR (3 downto 0):="0000";
begin
slow_down_clock:Slow_Clock port map (Clk => Clk, Reset=> Reset, Slow_Clk => S_clk);
Counter_N: Counter port map(Clk => S_clk, Reset=> Reset, UP=> UP, Q=> Bin);
Bin_7_Segment : Binary_7Segment port map (Bin => Bin,Seg => Disp );
AN <= "11111110";

end Behavioral;
```

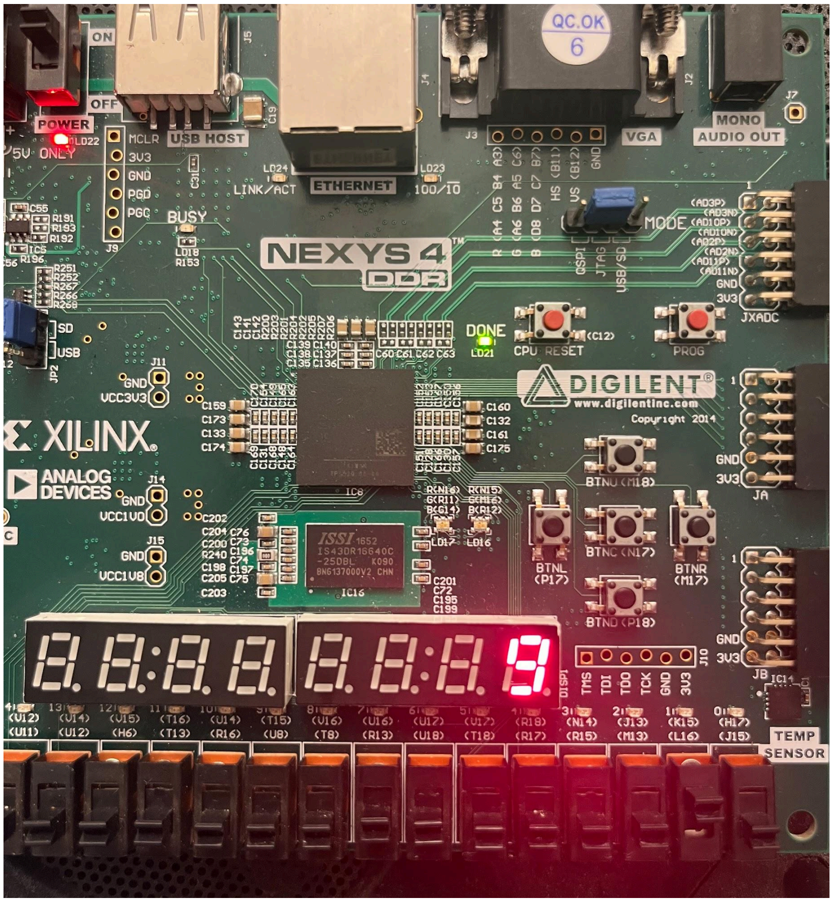


```
entity Counter_TB is
---   Port ( );
end Counter_TB;

architecture Behavioral of Counter_TB is
component Counter is
    Port ( Clk, Reset, UP : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (3 downto 0));
end component;
signal Clk, Reset, UP: STD_LOGIC:='0';
signal Q: STD_LOGIC_VECTOR (3 downto 0);
begin
UUT: Counter port map (Clk=> Clk, Reset=> Reset, UP=> UP, Q=>Q);

Pro_R: process
       begin
       Reset <= '1';
       wait for 20ns;
       Reset <= '0';
       wait ;
       end process;

Pro_C: process
       begin
       Clk <= '0';
       wait for 10ns;
       Clk <= '1';
       wait for 10ns;
       end process;

Pro_UP: process
       begin
       UP <= '0';
       wait for 120ns;
       UP <= '1';
       wait for 120ns;
       end process;

end Behavioral;
```





```
set_property PACKAGE_PIN E3 [get_ports Clk]
set_property IOSTANDARD LVCMOS18 [get_ports Clk]
set_property PACKAGE_PIN J15 [get_ports Reset]
set_property IOSTANDARD LVCMOS18 [get_ports Reset]
set_property PACKAGE_PIN L16 [get_ports UP]
set_property IOSTANDARD LVCMOS18 [get_ports UP]
set_property IOSTANDARD LVCMOS18 [get_ports {Disp[7]}]
set_property IOSTANDARD LVCMOS18 [get_ports {Disp[6]}]
set_property IOSTANDARD LVCMOS18 [get_ports {Disp[5]}]
set_property IOSTANDARD LVCMOS18 [get_ports {Disp[4]}]
set_property IOSTANDARD LVCMOS18 [get_ports {Disp[3]}]
set_property IOSTANDARD LVCMOS18 [get_ports {Disp[2]}]
set_property IOSTANDARD LVCMOS18 [get_ports {Disp[1]}]
set_property IOSTANDARD LVCMOS18 [get_ports {Disp[0]}]
set_property PACKAGE_PIN T10 [get_ports {Disp[0]}]
set_property PACKAGE_PIN R10 [get_ports {Disp[1]}]
set_property PACKAGE_PIN K16 [get_ports {Disp[2]}]
set_property PACKAGE_PIN K13 [get_ports {Disp[3]}]
set_property PACKAGE_PIN P15 [get_ports {Disp[4]}]
set_property PACKAGE_PIN T11 [get_ports {Disp[5]}]
set_property PACKAGE_PIN L18 [get_ports {Disp[6]}]
set_property PACKAGE_PIN H15 [get_ports {Disp[7]}]
set_property IOSTANDARD LVCMOS18 [get_ports {An[7]}]
set_property IOSTANDARD LVCMOS18 [get_ports {An[6]}]
set_property IOSTANDARD LVCMOS18 [get_ports {An[5]}]
set_property IOSTANDARD LVCMOS18 [get_ports {An[4]}]
set_property IOSTANDARD LVCMOS18 [get_ports {An[3]}]
set_property IOSTANDARD LVCMOS18 [get_ports {An[2]}]
set_property IOSTANDARD LVCMOS18 [get_ports {An[1]}]
set_property IOSTANDARD LVCMOS18 [get_ports {An[0]}]
set_property PACKAGE_PIN J17 [get_ports {An[0]}]
set_property PACKAGE_PIN J18 [get_ports {An[1]}]
set_property PACKAGE_PIN T9 [get_ports {An[2]}]
set_property PACKAGE_PIN J14 [get_ports {An[3]}]
set_property PACKAGE_PIN P14 [get_ports {An[4]}]
set_property PACKAGE_PIN T14 [get_ports {An[5]}]
set_property PACKAGE_PIN K2 [get_ports {An[6]}]
set_property PACKAGE_PIN U13 [get_ports {An[7}]
```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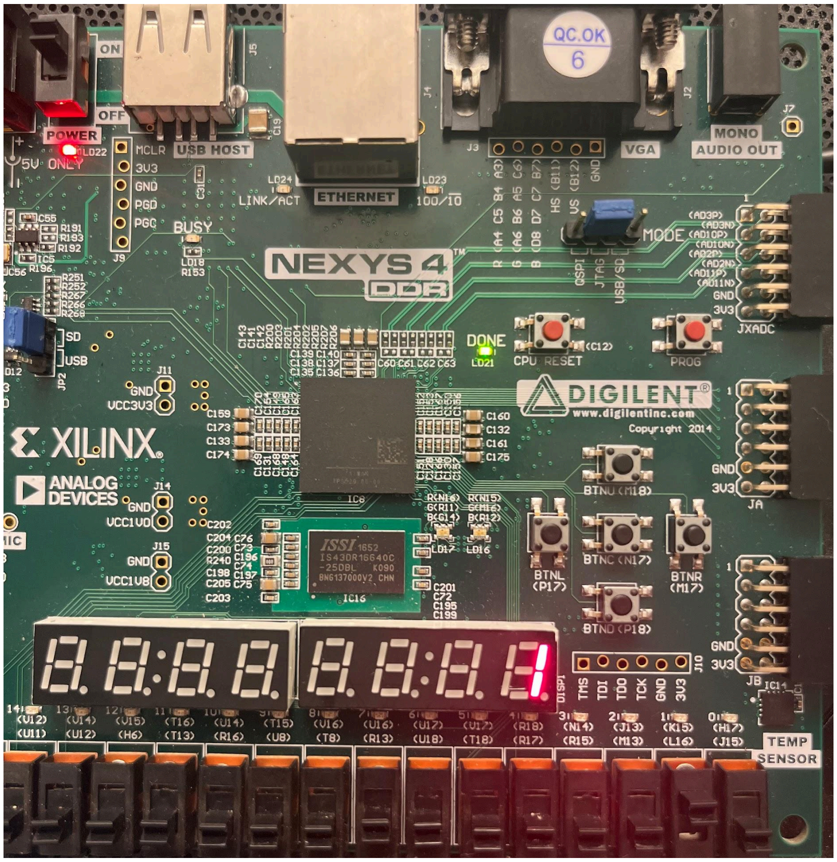
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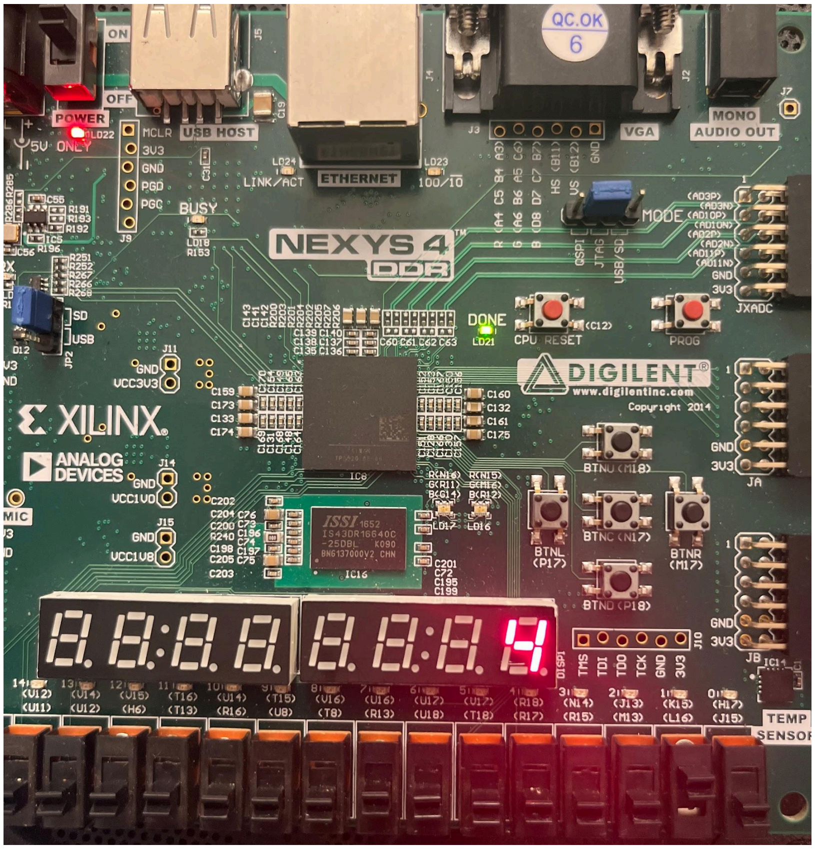
BTNR (M17)
BTND (P18)
TEMP SENSOR
1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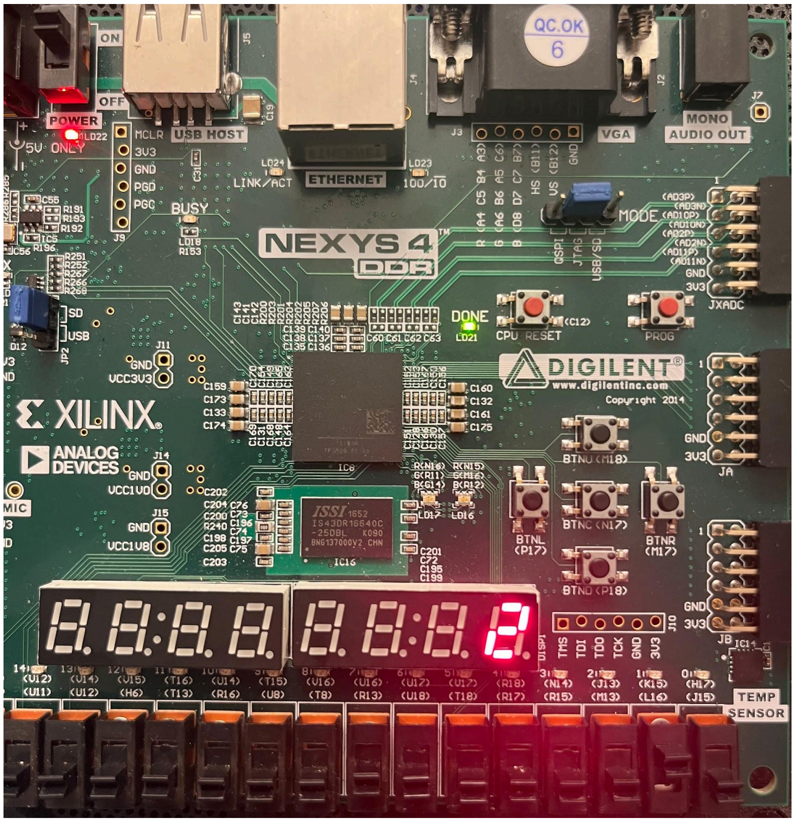
TEMP SENSOR
4



I have made another more complex state machine and counter. It controls whether it goes up or down depending on the external output Up. And so I programmed it to where if up is 1 it counts up but if up is 0 it counts down.