AK4493
Application Note

1. General Description

This Application Note is intended to assist in designing systems using the AK4493.

2. Table of Contents

3. Block Diagram

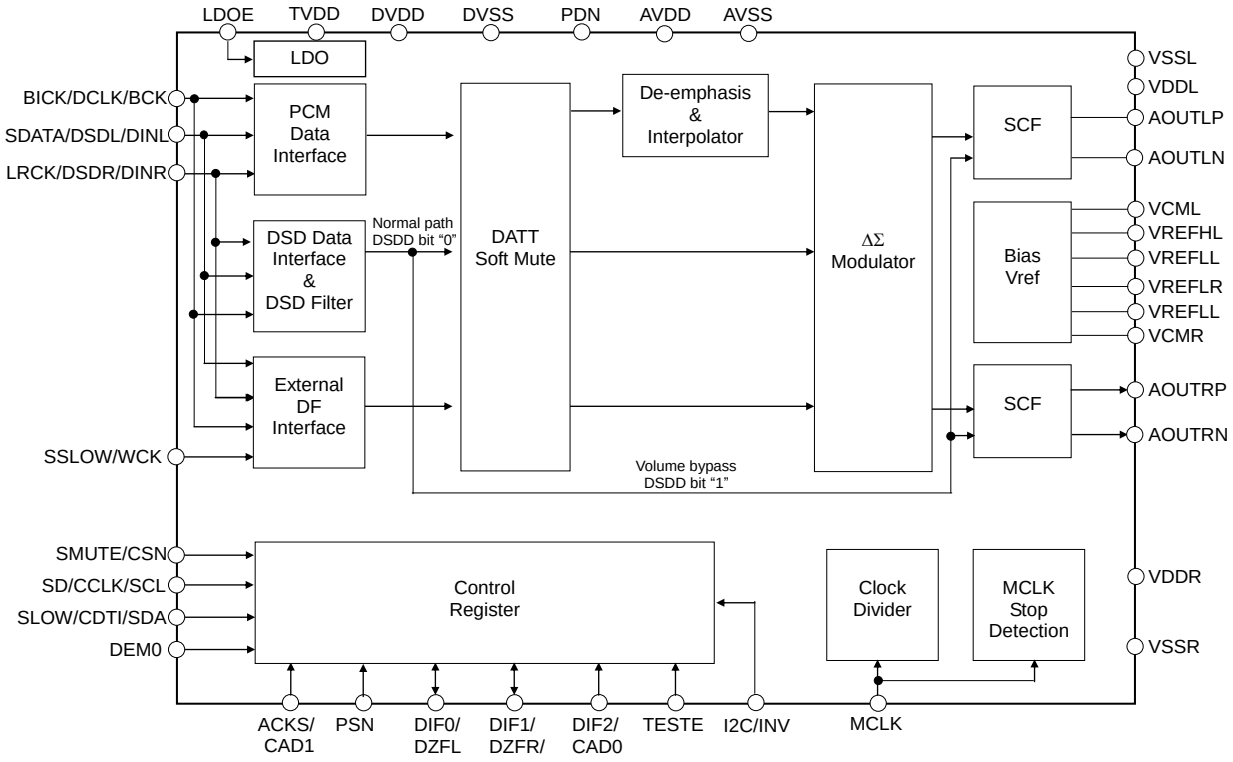

Figure 1. AK4493 Block Diagram

4. Comparison Table of D/A Converters

4.1. Premium DACs Comparison Table

Table 1 shows a comparison table of Premium DACs featuring AKM's LSI manufacturing process for premium audio.

Table 1. AKM Premium DAC Comparison Table (Y: Available, N/A: Not available)

	AK4499	AK4497	**AK4493**	AK4462	AK4468
AVDD	4.75–5.25 V	1.7–3.6 V	1.7–3.6 V	3.0–5.5 V	3.0–5.5 V
VDDL/R	4.75–5.25 V	4.75–5.25 V	4.75–5.25 V	-	-
TVDD	1.7–3.6 V	1.7–3.6 V	1.7–3.6 V	1.7–3.6 V	1.7–3.6 V
Channels	4	2	2	2	8
Output type	Balanced	Balanced	Balanced	Balanced	Balanced
PCM sampling rate	8–768 kHz	8–768 kHz	8–768 kHz	8–768 kHz	8–768 kHz
DSD sampling rate (max.)	DSD512	DSD512	DSD512	DSD512	DSD512
DoP sampling rate (max.)	N/A	N/A	N/A	DoP256	N/A
S/N	134 dB	128 dB	123 dB	117 dB	117 dB
THD+N	−124 dB	−116 dB	−113 dB	−107 dB	−107 dB
Digital Filter (PCM mode)	6 types	6 types	6 types	6 types	6 types
External Filter Mode	Y	Y	Y	N/A	N/A
TDM	Y	Y	Y	Y	Y
Daisy Chain	Y	Y	N/A	N/A	Y
Automatic Switching (PCM/DSD mode)	Y	N/A	Y	Y	Y
Automatic Switching (PCM/DoP mode)	N/A	N/A	N/A	Y	N/A
Power Consumption	667 mW	343 mW	188 mW	70 mW	245 mW
Package	128-pin HTQFP	64-pin HTQFP	48-pin LQFP	24-pin QFN	48-pin QFN

4.2. High-End Stereo DACs Comparison Table

The comparison table of High-End Stereo DAC Series is shown in Table 2.

Table 2. Function and Characteristics Comparison Table of AK4490 and AK4493
(Y: Available, N/A: Not available)

		AK4490	**AK4493**
LSI Process for Premium Audio		N/A	Y
VDDL, VDDR		4.75–7.2 V	4.75–5.25 V
AVDD		3.0–3.6 V	1.7–3.6 V
TVDD		3.0–3.6 V	1.7–3.6 V
Power Consumption		145 mW	188 mW
Output type		Balanced	Balanced
PCM sampling rate		8–768 kHz	8–768 kHz
DSD sampling rate (max.)		DSD256	DSD512
S/N	Normal mode	120 dB	123 dB
	Large Amplitude mode	N/A	125 dB
THD+N	Normal mode	−112 dB	−113 dB
	Large Amplitude mode	N/A	−110 dB
Digital Filter (PCM mode)		5 types	6 types
De-emphasis Filter		Y	Y
TDM		N/A	Y
Daisy Chain		N/A	N/A
Clock Synchronization Function		Y	Y
Automatic Mode Switching (PCM/DSD mode)		N/A	Y
Package (Note 1)		48-pin LQFP	48-pin LQFP
Pin/Register control select		Y	Y

Note 1. The AK4493 is pin compatible with the AK4490.

4.3. AK4493 Register Map (Compared with AK4490)

Register maps of the AK4493 and the AK4490 are shown in Table 3 and Table 4.
※yellow: Added in the AK4493 blue: Removed in the AK4493

Table 3. AK4493 Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	DP	ADP	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
03H	Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
04H	Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
05H	Control 4	INVL	INVR	0	0	0	0	DFS2	SSLOW
06H	DSD1	DDM	DML	DMR	DDMOE	DDMT1	DDMT0	DSDD	DSDSEL0
07H	Control 5	0	0	0	0	GC2	GC1	GC0	SYNCE
08H	Sound Control	0	0	0	0	0	SC2	SC1	SC0
09H	DSD2	0	0	0	0	0	0	DSDF	DSDSEL1
0AH	Control 6	TDM1	TDM0	SDS1	SDS2	0	PW	0	0
0BH	Control 7	ATS1	ATS0	0	SDS0	0	0	0	TEST
0CH	Reserved	0	0	0	0	0	0	0	0
0DH	Reserved	0	0	0	0	0	0	0	0
0EH	Reserved	0	0	0	0	0	0	0	0
0FH	Reserved	0	0	0	0	0	0	0	0
10H	Reserved	0	0	0	0	0	0	0	0
11H	Reserved	0	0	0	0	0	0	0	0
12H	Reserved	0	0	0	0	0	0	0	0
13H	Reserved	0	0	0	0	0	0	0	0
14H	Reserved	0	0	0	0	0	0	0	0
15H	Control 8	ADPE	ADPT1	ADPT0	0	0	0	0	0

Table 4. AK4490 Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	DP	0	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	Control4	INVL	INVR	0	0	0	0	DFS2	SSLOW
06H	Control5	DDM	DML	DMR	DMC	DMRE	0	DSDD	DSDSEL0
07H	Control6	0	0	0	0	0	0	0	SYNCE
08H	Control7	0	0	0	0	0	0	SC1	SC0
09H	Control8	0	0	0	0	0	0	DSDF	DSDSEL1

■The functions added in the AK4493

・02H D6: ADP
Readback register for internal PCM/DSD operation mode. This bit is valid when ADPE bit = "1".

・06H D4: DDMOE
Output Flag selection from the DZF pin

・06H D2[3:2]: DDMT[1:0]
DSD Signal Full-scale Detection Time setting

・07H D[3:1] :GC[2:0]
PCM, DSD mode Gain Control

・08H D2:SC[2]
Sound control

・0AH D[7:6] :TDM[1:0]
TDM Mode Select

・0AH D[5:4], 0BH D4 :SDS[2:0]
Output Data Slot selection of each channel

・0BH D[7:6] :ATS[1:0]
Transition Time between Set Values of ATTL/R[7:0] bits

・15H D7: ADPE
PCM/DSD Automatic Mode Switching function enable bit

・15H D[6:5]: ADPT[1:0]
Time until PCM/DSD mode detection when input data becomes zero

5. AK4493 Function List

Table 5 shows the functions available in PCM/EXDF/DSD modes. For details on how to use each function, refer to the corresponding pages of the AK4493 datasheet in Datasheet Page column.
In Pin Control mode, only a few functions are available. Refer to P35 in the datasheet for the functions available in Pin Control mode.

Table 5. Function List of PCM/EXDF/DSD mode @Register Control Mode
(Y: Available, N/A: Not available)

Function	Addr	Bit	PCM	EXDF	DSD		Data-sheet Page
					Normal	Volume Bypass	
PCM/DSD/EXDF Mode Selection	00, 02H	EXDF DP	Y	Y	Y	Y	37
System Clock Setting @PCM mode	00, 01, 05H	ACKS DFS[2:0]	Y	N/A	N/A	N/A	39–42
System Clock Setting @DSD mode	02H	DCKS DSDSEL[1:0]	N/A	N/A	Y	Y	43
System Clock Setting @EXDF mode	00H	ECS	N/A	Y	N/A	N/A	44
Digital Filter Selection @PCM mode	01, 02, 05H	SD, SLOW SSLOW	Y (Note 2)	N/A	N/A	N/A	55
Digital Filter Selection @DSD mode	09H	DSDF	N/A	N/A	Y	N/A	55
De-emphasis Filter	01H	DEM[1:0]	Y (Note 3)	N/A	N/A	N/A	55
Path Selection @ DSD mode	06H	DSDD	N/A	N/A	Y	Y	43
Audio Data Interface Format @ PCM mode, EXDF mode	00H	DIF[2:0]	Y	Y	N/A	N/A	45–51, 54
TDM Interface Format	0AH	TDM[1:0]	Y	N/A	N/A	N/A	45–53
Attenuation Level	03, 04H	ATTL/R[7:0]	Y	Y	Y	N/A	56
Data Zero Detection Enable	01H	DZFE	Y	Y	Y	N/A	57–58
Inverting Enable of DZF	02H	DZFB	Y	Y	Y	N/A	58
Mono/Stereo Mode Selection	02H	MONO	Y	Y	Y	Y	59
Data Invert Mode Selection	05H	INVL/R	Y	Y	Y	Y	59
Data Selection of L channel and R channel	02H	SELLR	Y	Y	Y	Y	59
Sound Color Selection	08H	SC[2:0]	Y	Y	Y	Y	59
DSD Mute Function @ Full Scale Detected	06H	DDM	N/A	N/A	Y	Y	60–62
Soft Mute	01H	SMUTE	Y	Y	Y	Y	71
RSTN	00H	RSTN	Y	Y	Y	Y	77–79
Clock Synchronization Function	07H	SYNCE	Y	Y	N/A	N/A	80–81
Automatic Mode Switching (PCM/DSD, EXDF/DSD)	15H	ADPE	Y	Y	Y	Y	63–70
Gain Control	07H	GC[2:0]	Y	Y	Y	Y	57

Note 2. The digital filter is fixed to super slow roll-off filter in Oct Speed Mode and Hex Speed Mode.
Note 3. Available in Normal Speed Mode, Double Speed Mode and Quad Speed Mode.

6. Recommended States when Changing Clock Frequency or Pin/Register Setting

Power Down, Power OFF and Reset functions of the AK4493 are controlled by PDN pin, PW bit, MCLK and RSTN bit (Table 6).

Table 6. Power Down, Standby, and Reset function (x: do not care)

ステート	PDN pin	MCLK Input	PW bit	RSTN bit	Analog Output
Power Down	L	x	x	x	Hi-Z
Power OFF	H	No	x	x	Hi-Z
	H	Yes	0	x	Hi-Z
Reset	H	Yes	1	0	VCML/R
Normal Operation	H	Yes	1	1	Signal output

This chapter describes which states the AK4493 should be in when changing clock frequency, control pin settings and register settings.

6.1. Clock Frequency

Table 7 shows the states that are allowed when changing the clock frequencies or are stopped.

Table 7. Permitted States When Changing Clock Frequencies
(Y: Permitted, N/A: Not Permitted)

Clock	Power Down	Power OFF	Reset	Normal Operation	Notes
MCLK frequency	Y	Y	Y	N/A	-
BICK frequency	Y	Y	Y	N/A	Note 4 Note 5
LRCK frequency	Y	Y	Y	N/A	Note 4 Note 5
DCLK frequency	Y	Y	Y	N/A	Note 5

Note 4. When ACKS bit = “0”, BICK and LRCK frequencies must be changed in the Power OFF or reset state. It is possible to change BICK and LRCK frequencies during normal operation when ACKS bit = “1”, but click noise may occur. This click noise can be avoided by the external mute circuit.

Note 5. When the AK4493 is in the auto-switching functions (ADPE bit = "1"), being in reset state is not necessarily required for switching the D/A conversion mode. Use these functions according to the procedures described in P63-70 in the datasheet.

6.2. Control Pin Setting (Pin Control Mode)

Table 8 shows the states that are allowed when changing the pin settings in pin control mode.

Table 8. Permitted States When Changing Control Pin Settings (Pin Control Mode)
(Y: Permitted, N/A: Not Permitted)

Pin	Power Down	Power OFF	Normal Operation	Notes
SMUTE	Y	Y	Y	-
DIF0/1/2	Y	Y	N/A	-
DEM0	Y	Y	Y	Note 6
INV	Y	Y	Y	Note 6
SD, SLOW, SSLOW	Y	Y	N/A	Note 7 Note 8
ACKS	Y	Y	N/A	-

Note 6. When switching in the normal operation state, it is recommended to switch at zero-data input or soft-mute state by SMUTE pin = "H" in order to avoid click noise during switching.

Note 7. Click noise may occur when the digital filter setting is changed. If click noise can be avoided by the external mute circuit, digital filter setting can be changed during normal operation.

Note 8. When changing from the Super slow roll-off filter to any other filter or vice versa in normal operation, the latency may deviate from the expected value (see section 7.1). To avoid this, change setting of these pins in Power Down or Power OFF state.

6.3. Register Setting (Register Control Mode)

Table 9 shows the states that are allowed when changing register settings in register control mode.

Table 9. Permitted States When Changing Register Settings (Register Control Mode)
(Y: Permitted, N/A: Not Permitted)

Register	Power OFF	Reset	Normal Operation	Notes
DIF[2:0]	Y	Y	N/A	-
ECS	Y	Y	N/A	-
EXDF	Y	Y	N/A	-
ACKS	Y	Y	N/A	-
SMUTE	Y	Y	Y	-
DEM[1:0]	Y	Y	Y	Note 9
DFS[2:0]	Y	Y	N/A	-
SD, SLOW, SSLOW	Y	Y	N/A	Note 10 Note 11
DZFE, DZFM	Y	Y	Y	
SELLR	Y	Y	Y	Note 9
DZFB	Y	Y	Y	-
MONO	Y	Y	Y	Note 9
DCKB	Y	Y	N/A	-
DCKS	Y	Y	N/A	-
DP	Y	Y	N/A	-
ATTL[7:0], ATTR[7:0]	Y	Y	Y	-
INVL, INVR	Y	Y	Y	Note 9
DSDSEL[1:0]	Y	Y	N/A	-
DSDD	Y	Y	N/A	-
DDMT[1:0]	Y	Y	N/A	-
DDMOE	Y	Y	Y	-
DDM	Y	Y	N/A	-
SYNCE	Y	Y	N/A	-
GC[2:0]	Y	Y	N/A	-
SC[2:0]	Y	Y	N/A	-
DSDF	Y	Y	Y	Note 9
SDS[2:0]	Y	Y	Y	Note 9
TDM[1:0]	Y	Y	N/A	-
ATS[1:0]	Y	Y	Y	Note 12
ADPT[1:0]	Y	Y	N/A	-
ADPE	Y	Y	N/A	-

Note 9. When switching in the normal operation state, it is recommended to switch at zero-data input or soft-mute state by SMUTE bit = "1" in order to avoid click noise during switching.

Note 10. Click noise may occur when the digital filter setting is changed. If click noise can be avoided by the external mute circuit, digital filter setting can be changed during normal operation.

Note 11. When changing from the Super slow roll-off filter to any other filter or vice versa in normal operation, the latency may deviate from the expected value (see section 7.1). To avoid this, change setting of these bits in Power OFF or Reset state.

Note 12. Do not change the ATS[1:0] bits while operating gain transition by SMUTE bit, ATTL[7:0] bits and ATTR[7:0] bits switching.

7. Latency in Each Playback Mode

Latency is the internal processing time it takes for the input digital data to be output as an analog signal.

7.1. PCM mode

Latency in PCM mode is the time from when the impulse data is set in the input register until the peak of the analog signal is output (Figure 2). The latency at PCM mode is the sum of the digital filter group delay and the other operational delays shown below.

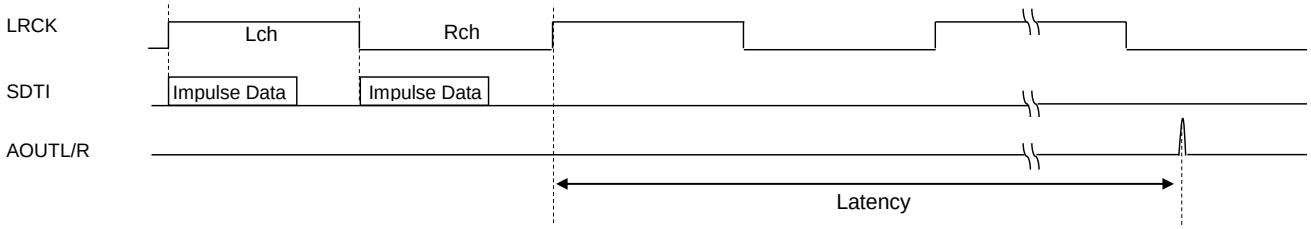

Figure 2. PCM mode Latency

In PCM mode, group delays such as Table 10 occur according to the settings of the digital filter.

Table 10. Group Delay (PCM mode)

SSLOW bit	SD bit	SLOW bit	Mode	Group Delay (Note 13)	
0	0	0	Sharp roll-off filter	29.2/fs	
0	0	1	Slow roll-off filter	6.5/fs	
0	1	0	Short delay sharp roll-off filter	6.0/fs	(default)
0	1	1	Short delay slow roll-off filter	5.0/fs	
1	0	x	Super slow roll-off filter	0.6/fs–2.5/fs (Note 14)	
1	1	x	Low dispersion short delay filter	10/fs	

Note 13. When the AK4493 is in Oct Speed Mode or Hex Speed Mode, Super Slow roll-off filter is selected regardless of SSLOW/SD/SLOW bit setting.

Note 14. 0.6/fs in Normal Speed Mode. It varies in the range of 0.6/fs-2.5/fs depending on the Sampling Speed setting.

When PCM/DSD automatic mode switching function is used (ADPE bit = "1"), a delay of 18/fs occurs due to internal operation (Table 11).

Table 11. Operational Delay Caused by ADPE Setting (PCM mode)

ADPE bit	Operation Delay	
0	0/fs	(default)
1	18/fs	

In addition, in PCM mode, there is a delay error due to the timing of capturing data at the data interface. The delay error depends on the Synchronization Function (SYNCE bit) setting (Table 12).

Table 12. Delay Error at the Data Interface (PCM mode)

SYNCE bit	Delay Error	
0	<±1/fs	
1	<±0.3 μs	(default)

(e.g.) Latency when PCM mode, fs = 44.1 kHz, Sharp Roll-off filter, ADPE bit = “1” and SYNCE bit = “0”

Latency = (29.2 + 18 ± 1)/fs = (47.2 ± 1)/fs = 1070 ± 23 μs

7.2. DSD mode

Latency in DSD mode is approximately 8 µs in DSD64 mode, which varies slightly depending on the operation rate and DSDF bit.

However, when the DSD full-scale detection function is used (DDM bit = "1"), a register delay described in Table 13 occurs according to DDMT[1:0] bits setting.

Table 13. Register Delay (DSD mode, x: Do not Care)

DDM bit	DDMT[1:0] bits	Register Delay	
0	xx	0	(default)
1	00	264 DCLK cycle	
1	01	520 DCLK cycle	
1	10	1032 DCLK cycle	
1	11	136 DCLK cycle	

(e.g.) Latency when DSD64 (DCLK = 2.8224 MHz), DSDF bit = "0", DDM bit = "1", and DDMT[1:0] bits = "00"

Latency = 8 µs + 264 DCLK = 102 µs

8. Design of Analog Output Post-Circuit

8.1. Calculation of the DC load resistance

The external circuit after the analog output pins (AOUTP, AOUTN) must be designed so that its DC load resistance (R_L) complies with the "Load Resistance" specifications given in chapter 8 in the datasheet. The R_L is the effective resistance between the analog output pins and the system analog ground (Figure 3). This section describes how to calculate the DC load resistance by referring to the circuit as shown in Figure 4.

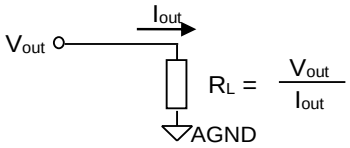

Figure 3. Schematic Diagram of the R_L

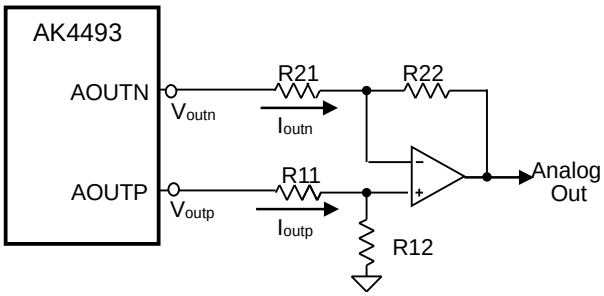

Figure 4. Example of Differential-to-Single Circuit

The R_L is determined by $R_L = V_a/I_a$ from I_a at full-scale current output and output voltage V_a of AOUTx pin (Figure 5). For normal operation of the AK4493, both the R_{Lp} (R_L of AOUTP pin) and the R_{Ln} (R_L of AOUTN pin) must satisfy the specification ($R_L \geq 450\ \Omega$).

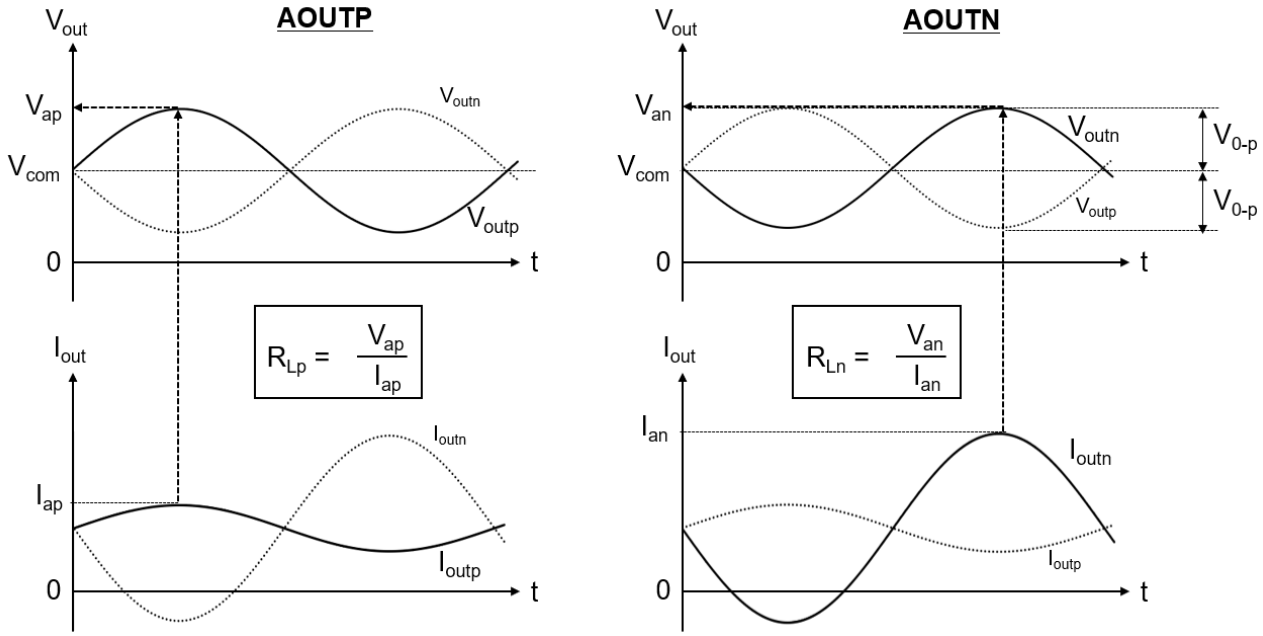

Figure 5. R_{Lp} and R_{Ln} in the Figure 4 Schematic

In Figure 4 case, the R_{Lp} and the R_{Ln} are,

$$R_{Lp} = \frac{V_{ap}}{I_{ap}} = R_{11} + R_{12}$$

$$R_{Ln} = \frac{V_{an}}{I_{an}} = \frac{\left(V_{com} + V_{0-\mathrm{p}}\right)(R_{11} + R_{12})R_{21}}{R_{11}V_{com} + (R_{11} + 2R_{12})V_{0-\mathrm{p}}}$$

Where,

$$V_{COM} = 0.5(VREFH - VREFL)$$

$$V_{0-\mathrm{p}} = 0.28(VREFH - VREFL)$$

8.2. Filter Design

The formula for calculating the parameters of the second-order low-pass filter shown in Figure 6 is shown below.

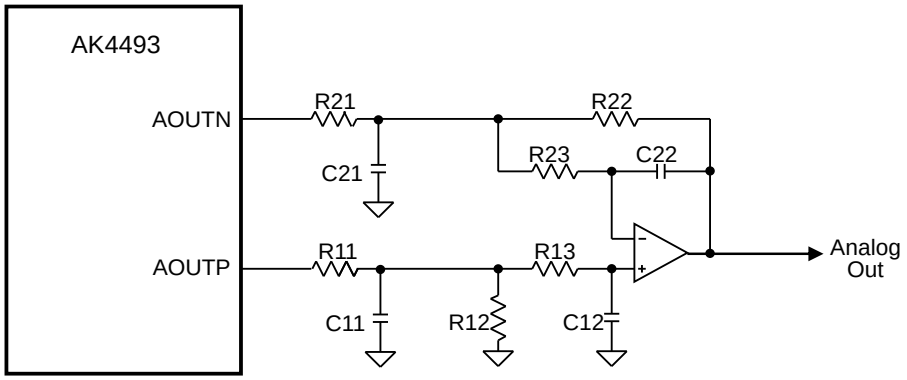

Figure 6. Second-Order Low-Pass Filter Circuit Example

$$DC\ Gain = \frac{0.5(R_{21}R_{12} + R_{11}R_{22}) + R_{12}R_{22}}{R_{21}(R_{11} + R_{12})}$$

$$f_{cp} = \frac{\omega_{0p}}{2\pi} \quad , \quad f_{cn} = \frac{\omega_{0n}}{2\pi}$$

$$\omega_{0p} = \frac{1}{\sqrt{C_{11}C_{12}R_{12}R_{13}}} \quad , \quad \omega_{0n} = \frac{1}{\sqrt{C_{21}C_{22}R_{22}R_{23}}}$$

$$Q_p = \frac{C_{11}\omega_{0p}}{\frac{1}{R_{11}} + \frac{1}{R_{12}} + \frac{1}{R_{13}}} \quad , \quad Q_n = \frac{C_{21}\omega_{0n}}{\frac{1}{R_{21}} + \frac{1}{R_{22}} + \frac{1}{R_{23}}}$$

$$R_{Lp} = \frac{V_{ap}}{I_{ap}} = R_{11} + R_{12}$$

$$R_{Ln} = \frac{V_{an}}{I_{an}} = \frac{(V_{com} + V_{0-\mathrm{p}})(R_{11} + R_{12})R_{21}}{R_{11}V_{com} + (R_{11} + 2R_{12})V_{0-\mathrm{p}}}$$

9. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
20/09/1	01	First Edition		

IMPORTANT NOTICE

0. Asahi Kasei Microdevices Corporation (“AKM”) reserves the right to make changes to the information contained in this document without notice. When you consider any use or application of AKM product stipulated in this document (“Product”), please make inquiries the sales office of AKM or authorized distributors as to current status of the Products.
1. All information included in this document are provided only to illustrate the operation and application examples of AKM Products. AKM neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of AKM or any third party with respect to the information in this document. You are fully responsible for use of such information contained in this document in your product design or applications. AKM ASSUMES NO LIABILITY FOR ANY LOSSES INCURRED BY YOU OR THIRD PARTIES ARISING FROM THE USE OF SUCH INFORMATION IN YOUR PRODUCT DESIGN OR APPLICATIONS.
2. The Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact, including but not limited to, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for the above use unless specifically agreed by AKM in writing.
3. Though AKM works continually to improve the Product’s quality and reliability, you are responsible for complying with safety standards and for providing adequate designs and safeguards for your hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of the Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption.
4. Do not use or otherwise make available the Product or related technology or any information contained in this document for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). When exporting the Products or related technology or any information contained in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. The Products and related technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
5. Please contact AKM sales representative for details as to environmental matters such as the RoHS compatibility of the Product. Please use the Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. AKM assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.
6. Resale of the Product with provisions different from the statement and/or technical features set forth in this document shall immediately void any warranty granted by AKM for the Product and shall not create or extend in any manner whatsoever, any liability of AKM.
7. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of AKM.

Rev.1