

Variational Satisfiability Solving

*Efficiently Solving Lots of
Related SAT Problems*

Empirical Software Engineering, 2022



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SAT solvers are used everywhere

SAT solvers are used everywhere

Bug finding

Finding Bugs Efficiently with a SAT Solver

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ABSTRACT

We present an approach for checking code against rich specifications, based on existing work that consists of encoding the program in a relational logic and using a constraint

concrete witnesses for bugs. However, testing approaches may miss problems due to incomplete coverage. Static analysis techniques over-approximate all program behaviors, and is capable of proving the absence of an error. However, static

Finding Bugs in an Alpha Microprocessor Using Satisfiability Solvers

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Abstract. We describe the techniques we have used to search for bugs in the memory subsystem of a next-generation Alpha microprocessor. Our

SAT solvers are used everywhere

Bug finding

Model checking

Bounded Model Checking

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Abstract. Symbolic model checking with Binary Decision Diagrams (BDDs) has been successfully used in the last decade for systems such as sequential circuits and protocols. Beginning of the 90's, it has been integrated in the design of several major hardware companies. The main bottleneck is that BDDs may grow exponentially, and hence the analysis restricts the size of circuits that can be verified efficiently. A technique called Bounded Model Checking (BMC) was introduced in 1999, BMC has been well received by the industry. It uses a SAT solver rather than BDD manipulation techniques. BMC is therefore widely perceived as a complementary technique to symbolic model checking.

Interpolation and SAT-based Model Checking

K. L. McMillan

Cadence Berkeley Labs

Abstract. We consider a fully SAT-based method of unbounded symbolic model checking based on computing Craig interpolants. In benchmark studies using a set of large industrial circuit verification instances, the proposed method compares favorably with existing SAT-based model checking techniques.

SAT-Based Model Checking Without Unrolling

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Abstract. A new form of SAT-based symbolic model checking is described. Instead of unrolling the transition relation, it incrementally generates the transition relation for the current state of the system.

ing temporal properties of

SAT solvers are used everywhere

Bug finding

Model checking

Bioinformatics

SAT in Bioinformatics: Making the Case with Haplotype Inference

Inês Lynce¹ and João Marques-Silva²¹ IST/INESC-ID, Technical University of Lisbon, Portugal
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Abstract. Mutation in DNA is the principal cause for many human diseases, and Single Nucleotide Polymorphisms (SNPs) are the most common mutations. Hence, a fundamental task in genomics is to map of haplotypes (which identify SNPs) in the human genome. Associated with this effort, a key computational problem is the inference of haplotype data from genotype data, since in practice, rather than haplotype data is usually obtained. Recent work has shown that SAT solvers can be used to solve this problem efficiently.

Lynx: A Programmatic SAT Solver for the RNA-folding Problem

Vijay Ganesh, Charles W. O'Donnell,
Mate Soos[†], Srinivas Devadas, Martin C. Rinard and Armando Solar-LezamaMassachusetts Institute of Technology, [†]Security Research Labs
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Abstract. This paper introduces Lynx, an incremental programmatic SAT solver that allows non-expert users to easily introduce domain-specific code into modern Conflict-driven Clause-learning (CDCL) SAT solvers, thus enabling users to control the behavior of the solver in ways that enables following user-research, and to file the power

Conference Paper

SAT-based protein design

December 2009 · [IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers](#)Source · [IEEE Xplore](#)

Conference: Computer-Aided Design - Digest of Technical Papers, 2009. ICCAD 2009. IEEE/ACM International Conference on

Authors:



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C. Coelho



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SAT solvers are used everywhere

Bug finding

Model checking

Bioinformatics

Scheduling

Software product-lines

Program Synthesis

Program Verification

Planning

A satisfiability (SAT) solver is a tool that solves the Boolean satisfiability problem

Given a formula in propositional logic: $f := (p \wedge q \Rightarrow r)$

Find an assignment such that f is *satisfied*:

$$p \rightarrow F$$

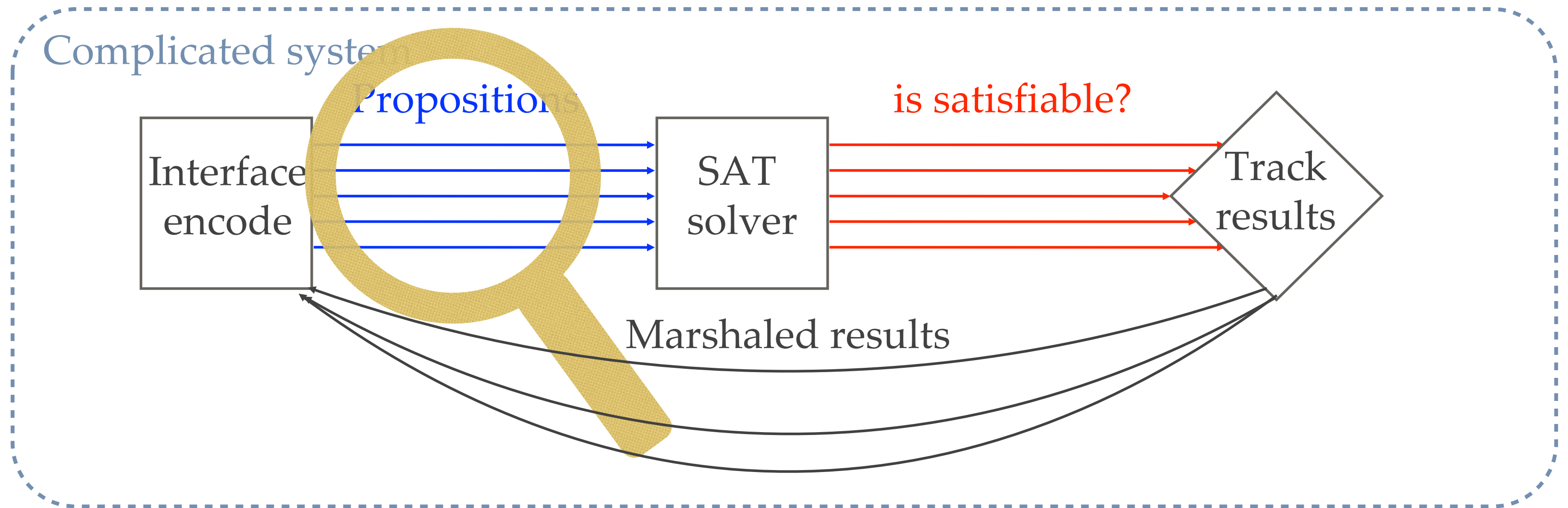
$$q \rightarrow T$$

$$r \rightarrow T$$

$$f = F \wedge T \Rightarrow T$$

$$f = F \Rightarrow T$$

$$f = T$$



This is great, however...

Propositions

$$\left\{ \begin{array}{l} FM \wedge c_1 \wedge c_2 \wedge \cdots \wedge c_n \\ FM \wedge c_1 \wedge c_{10} \wedge \cdots \wedge c_n \\ FM \wedge c_{10} \wedge c_2 \wedge \cdots \wedge c_n \end{array} \right.$$

When we want to solve sets of related problems it is likely we are re-evaluating several clauses or terms!

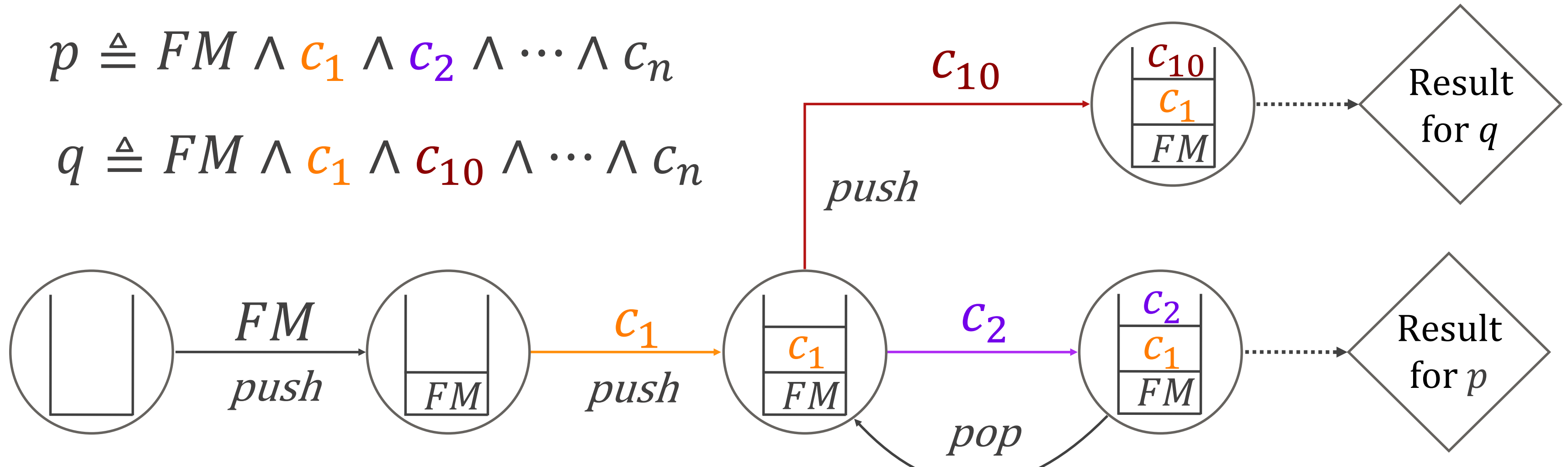
Incremental SAT: Add or remove clauses to the assertion stack

Push: Add a clause

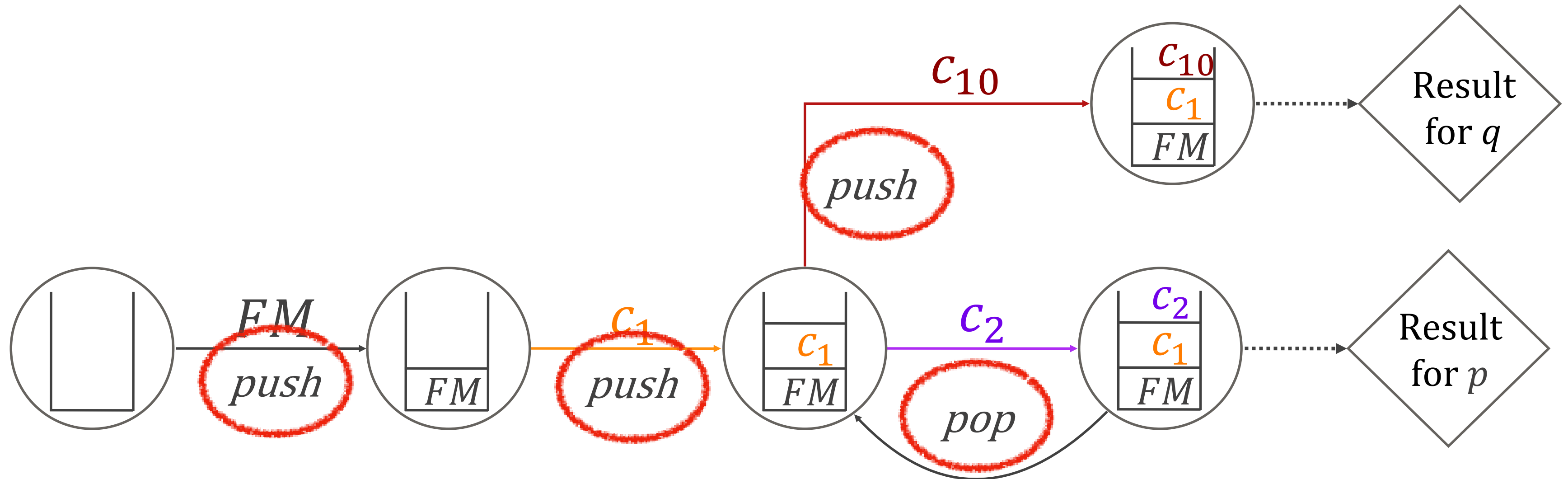
Pop: Remove the last clause

$$p \triangleq FM \wedge c_1 \wedge c_2 \wedge \cdots \wedge c_n$$

$$q \triangleq FM \wedge c_1 \wedge c_{10} \wedge \cdots \wedge c_n$$



Directly addresses redundancy and is efficient




But the solver is not aware of what is shared!

Push/pop do not denote meaning to the user

Hand-written program for each domain!

What do we mean by variation?



CORE MODELS
330i Sedan
2.0-liter BMW TwinPower Turbo inline 4-cylinder,
Rear-wheel drive




STARTING MSRP ⓘ
\$41,250

Build Your Own

choose red

choose blue

choose gray



Variants

All options have been chosen

Variational Artifact

That which can be configured to produce a variant



CORE MODELS

330i Sedan

2.0-liter BMW TwinPower Turbo inline 4-cylinder,
Rear-wheel drive

STARTING MSRP ?

\$41,250

Build Your Own

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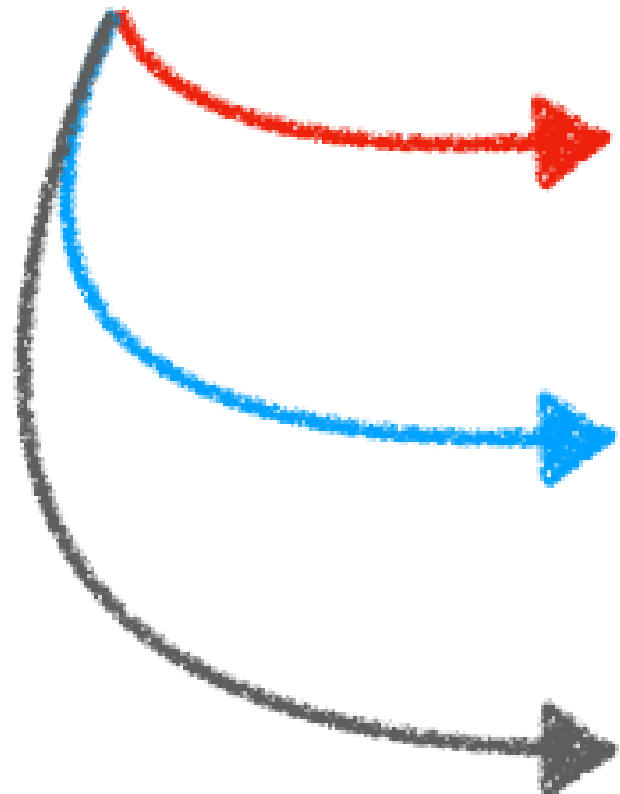
choose gray

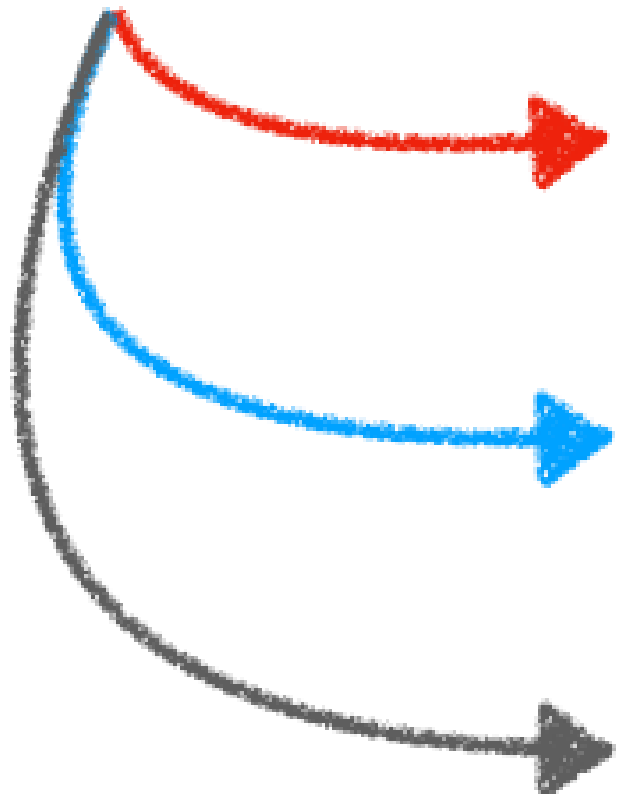


Variants

All options have been chosen

A variation-aware system is a system that operates on **variational artifacts**, *not* on **variants**.





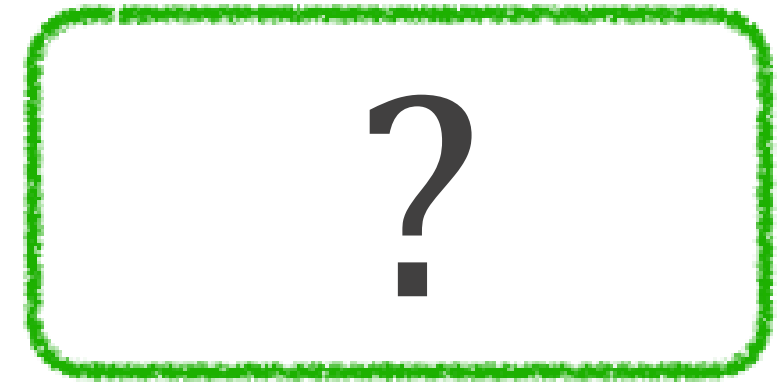
$$a \wedge b \wedge c \wedge e$$

$$a \wedge (b \vee \neg i) \wedge c$$

$$z \leftrightarrow (a \wedge b \wedge c \wedge e)$$

Modern SAT solvers
operate on variants

SAT solver that operates
on a variational artifact

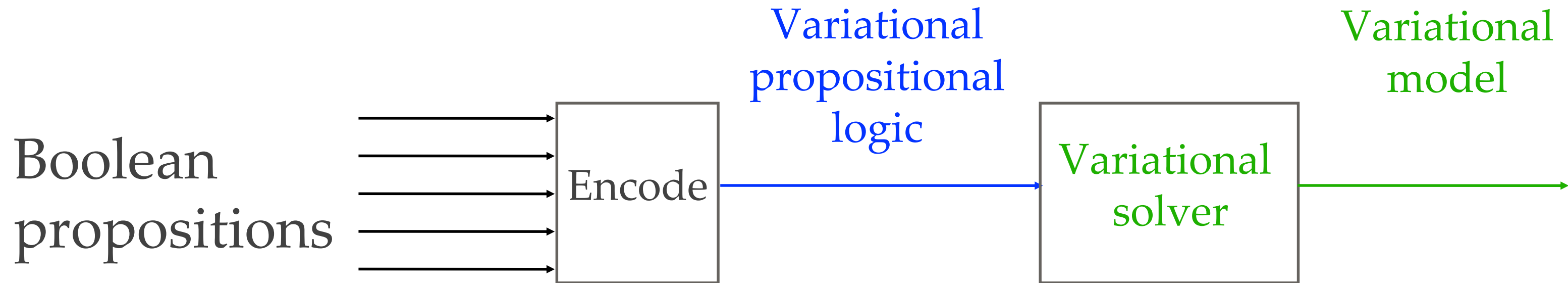


$$a \wedge b \wedge c \wedge e$$

$$a \wedge (b \vee \neg i) \wedge c$$

$$z \leftrightarrow (a \wedge b \wedge c \wedge e)$$

Build a satisfiability solver that is variation-aware



1. Define **variational propositional logic**

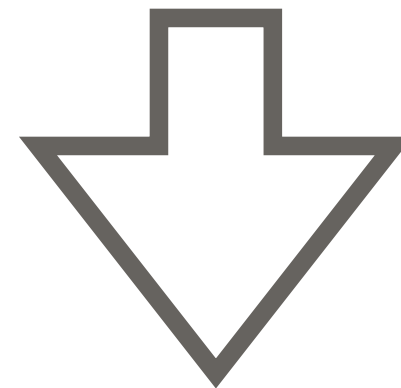
2. Develop a **prototype variational SAT solver**

3. Evaluate the solver on empirical data.
Show these ideas work in practice.

VPL = Propositional Logic + Choice Calculus

$$p \triangleq FM \wedge c_1 \wedge c_2 \wedge \cdots \wedge c_n$$

$$q \triangleq FM \wedge c_1 \wedge c_{10} \wedge \cdots \wedge c_n$$



New connective!
a Choice

$$p_or_q \triangleq FM \wedge c_1 \wedge A\langle c_2, c_{10} \rangle \wedge \cdots \wedge c_n$$

With choices, shared terms are statically explicit!



Plain

Dimension

$$p_{or_q} \triangleq FM \wedge c_1 \wedge A\langle c_2, c_{10} \rangle \wedge \cdots \wedge c_n$$

Left Alternative

Right Alternative

Configurations

Variants

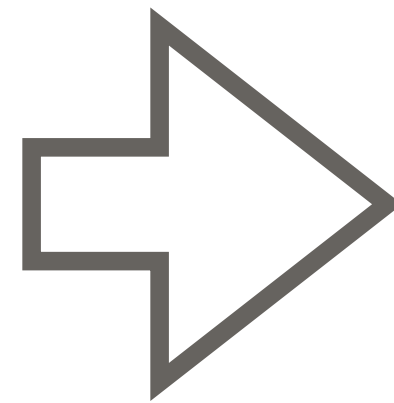
$$FM \wedge c_1 \wedge c_2 \wedge \cdots \wedge c_n$$

$$FM \wedge c_1 \wedge c_{10} \wedge \cdots \wedge c_n$$



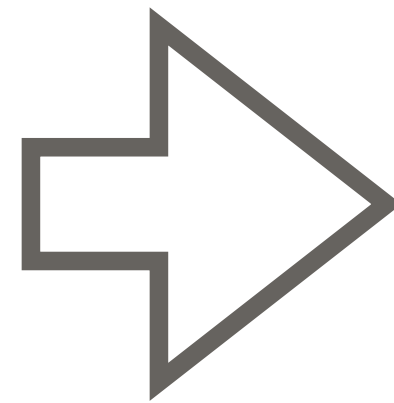
This is a compiler

VPL



SMTLIB2

$FM \wedge (c_1 \vee A\langle c_2, c_{10} \rangle \vee \neg(c_i \wedge c_j))$



```
(declare-const e1 Int)
(declare-const e2 Int)
(declare-const a1 (Array Int Int))
(declare-const a2 (Array Int Int))
(assert (= (store a2      3 A(1202,2718)) a2))
(assert (= (store A(a1,a2) 3 1729      ) a1))
(assert (= (select A(a1,a2) 3) e1))
(assert (= (select a2      3) e2))
(check-sat)
(get-model)
```

Goal:

Performance at least as good as a hand-written incremental program.

Given a
VPL formula:

$$FM \wedge (\textcolor{brown}{c}_1 \vee A\langle \textcolor{blue}{c}_2, \textcolor{red}{c}_{10} \rangle \vee \neg(c_i \wedge c_j))$$

Strategy: Define an intermediate language, solve in 3 modes

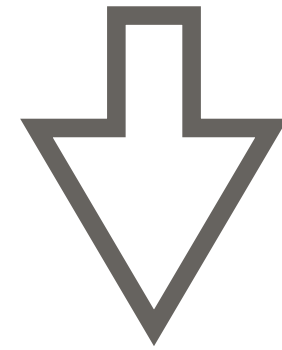
Evaluation Send terms to the solver if safe to do so

Accumulation Cache and combine plain terms for future use

Choice Removal Manipulate the configuration to remove choices

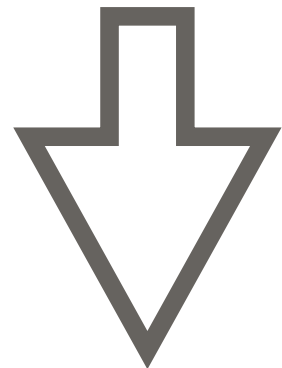
$$FM \wedge (\textcolor{brown}{c}_1 \vee A\langle \textcolor{blue}{c}_2, \textcolor{red}{c}_{10} \rangle \vee \neg(c_i \wedge c_j))$$

Evaluation



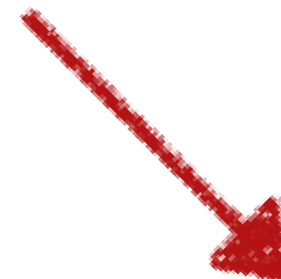
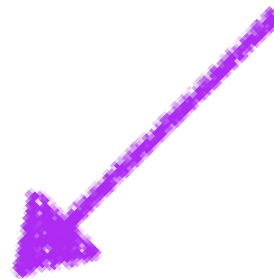
$$(\textcolor{brown}{c}_1 \vee A\langle \textcolor{blue}{c}_2, \textcolor{red}{c}_{10} \rangle \vee \neg(c_i \wedge c_j))$$

Accumulation



$$\dots \vee A\langle \textcolor{blue}{c}_2, \textcolor{red}{c}_{10} \rangle \vee \dots$$

Choice Removal



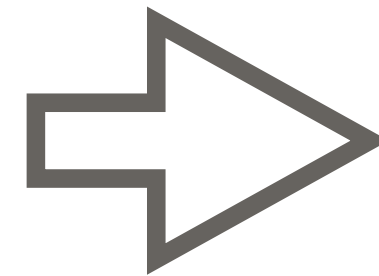
$$FM \wedge (\textcolor{brown}{c}_1 \vee A\langle \textcolor{violet}{c}_2, \textcolor{darkred}{c}_{10} \rangle \vee \neg(c_i \wedge c_j))$$

Model_{A=True}

$FM \rightarrow T$
 $\textcolor{brown}{c}_1 \rightarrow T$
 $\textcolor{violet}{c}_2 \rightarrow T$
 \vdots

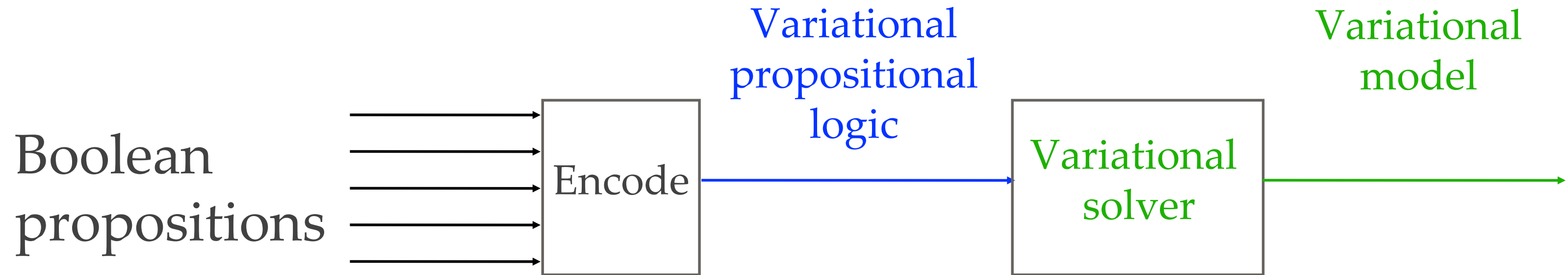
Model_{A=False}

$FM \rightarrow T$
 $\textcolor{brown}{c}_1 \rightarrow F$
 $\textcolor{darkred}{c}_{10} \rightarrow T$
 \vdots



Variational Model

$_Sat \rightarrow A \vee \neg A$
 $FM \rightarrow A \vee \neg A$
 $\textcolor{brown}{c}_1 \rightarrow A$
 $\textcolor{darkred}{c}_{10} \rightarrow \neg A$
 $\textcolor{violet}{c}_2 \rightarrow A$
 \vdots



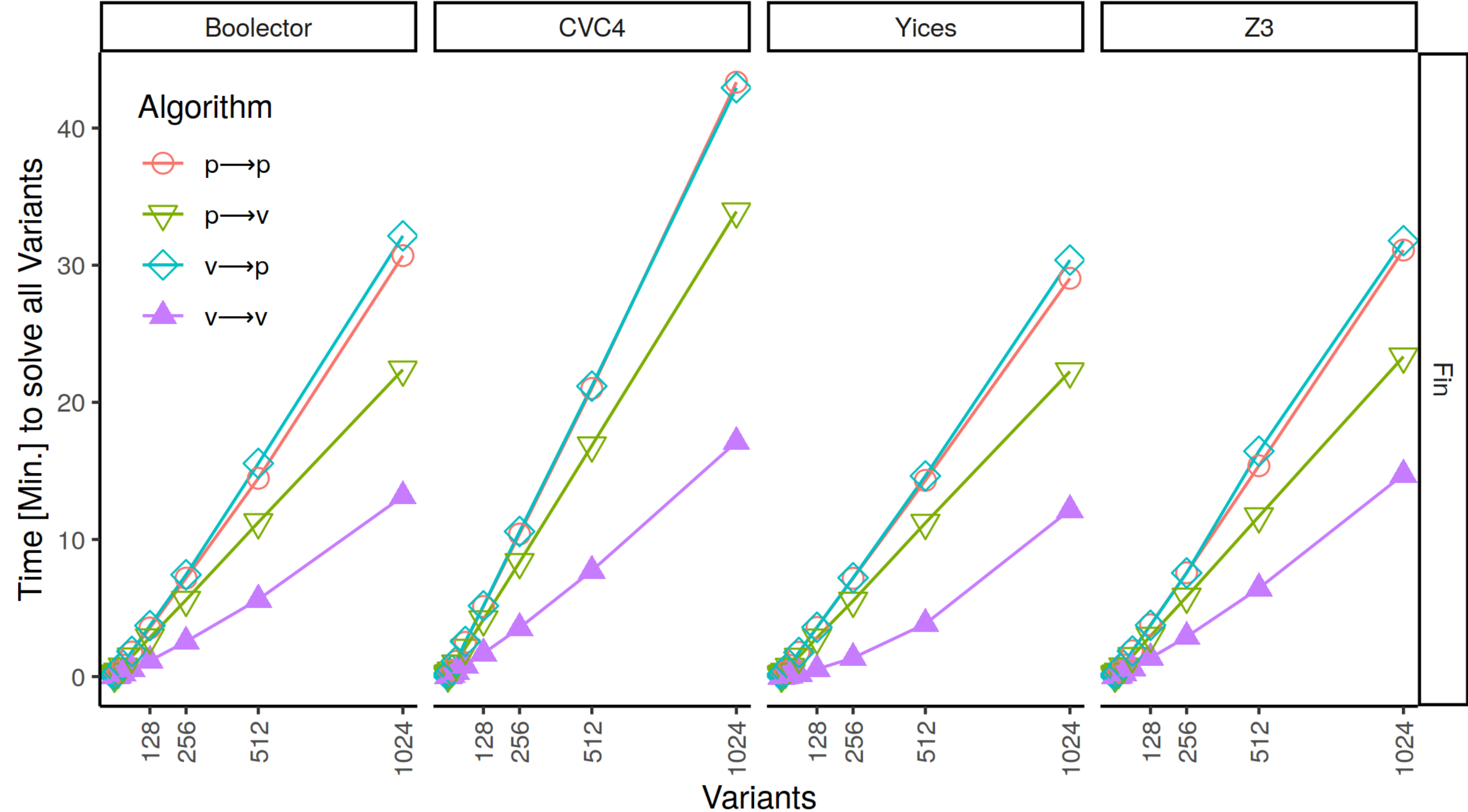
1. Define **variational propositional logic**

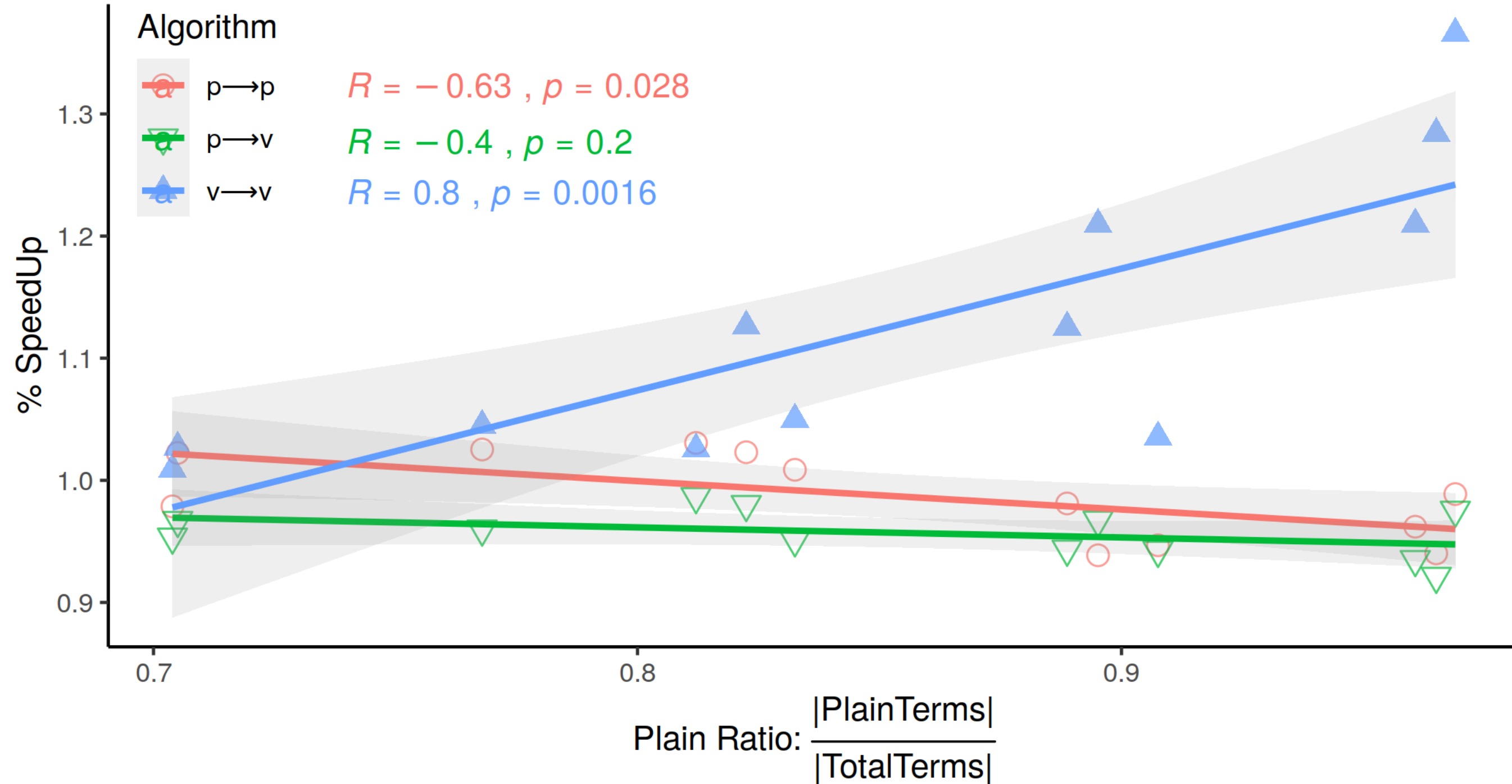
2. Develop a **prototype variational SAT solver**

3. Empirically evaluate the solver

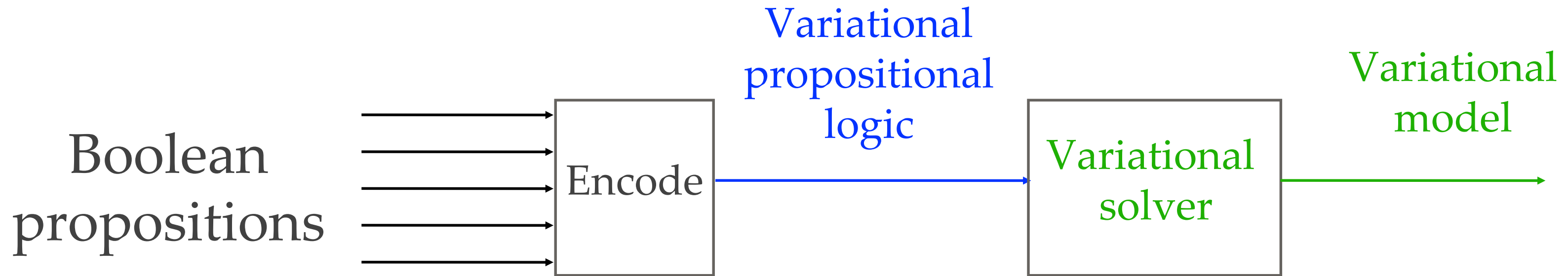
	Automotive02	FinancialServices01
# unique dimensions choices	4	10
# plain terms	26,088	1,441
# choices	4,212	3,809
Max. Obs. Speedup	2.6-3.5x	2.2-2.5x

*Datasets translated into VPL from Nieke et al, Anomaly Analyses for Feature-Model Evaluation





Plain ratio of a VPL formula is positively correlated to performance



Frequent need to solve many related satisfiability problems.

Our solution: variational satisfiability solving.

Must know all points of variation before solving.

Sharing impacts performance.