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NANOFABRICATION TECHNOLOGIES (IH2659)

MOSFET Interconnect Deposition and Reactive Ion Etching

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Contents

1 Abstract	2
2 Introduction	3
3 Experimental	4
3.1 SiO ₂ etching	4
3.2 Metal 1 deposition	5
3.3 Lithography	6
3.4 Metal etching	8
3.5 Resist stripping	9
4 Results	10
4.1 TiW 100 nm / Al 500 nm layer thickness	10
4.2 Finished MOSFET structure	10
5 Conclusions	12

1 Abstract

The last step of a MOSFET preparation process is the deposition and etching of the metal layer forming the contacts. The work was performed at the Electrum Laboratory, Kista, Sweden. A wafer with CMOS structures was provided and the contact holes were opened using a wet etch. The metal was deposited using a sputtering deposition technique and lithography was used to make the resist pattern on the metal layer. The metal was etched using RIE (Reactive Ion Etching) and the finished structure was inspected using LOM.

The structured revealed that the alignment of the resist using lithography was adequate for the specific structure process. The resolution target on the wafer structure showed that the highest resolution was $0.8 \mu\text{m}$ which was well below the smallest critical size $1 \mu\text{m}$ of the contact holes. A sheet resistance measurement of the deposited aluminium layer showed that the layer thickness was roughly 450 nm, which was close to the target thickness of 500 nm.

The conclusions from the lab were that the process has a good enough resolution for the specific process and that the layer thickness of the deposited metal can be closely controlled using sputtering deposition.

2 Introduction

The last step of a MOSFET preparation process on a CMOS wafer developed by the Department of Electronics at KTH Royal Institute of Technology is to add the metal contacts that allow the communication between CMOS transistors. The purpose of this lab was to get experience working in a cleanroom environment, as well as depositing the metal on transistor contact holes that were prepared by another lab group.

The laboratory work took place in the cleanroom in the Electrum Laboratory at Kista, Stockholm. Supervisors were Per-Erik Hellström and Alexey Metreveli. The wafer provided to the lab group was pre-processed with SOI CMOS structures. Figure 1 shows the structure before the laboratory work started. The contact holes were prepared the same day as the laboratory work by another lab group.

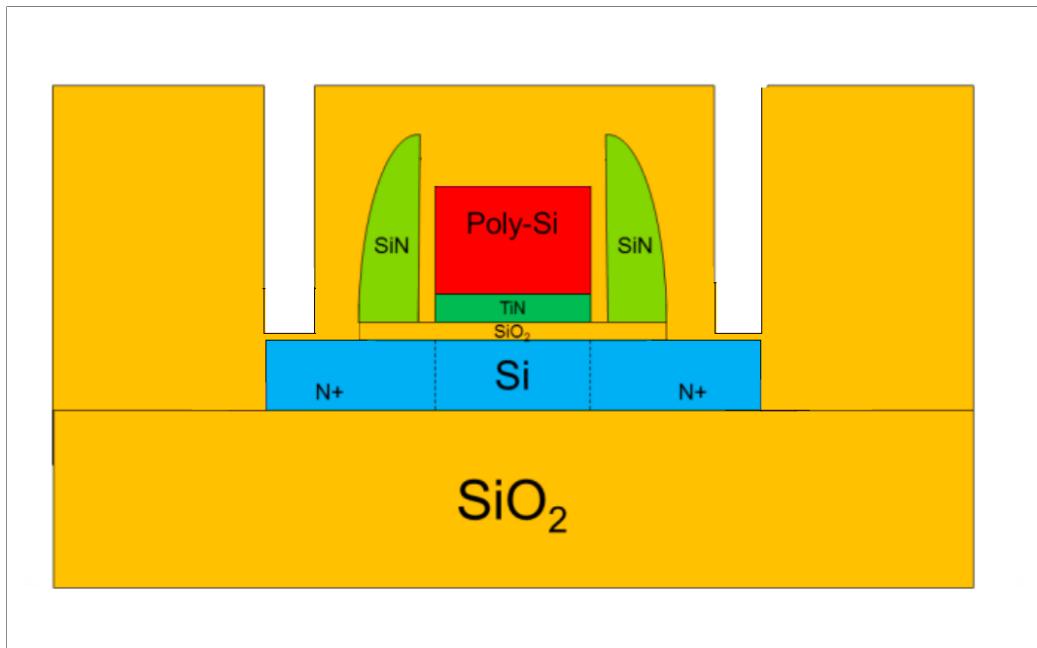


Figure 1: Cross-sectional schematic of the nMOSFET before the laboratory work started.

3 Experimental

3.1 SiO₂ etching

Since there was still a thin layer of oxide inside the contact holes, the first step of the laboratory work was to etch the last 20-30 nm of the oxide to reach the MOSFETs. Before starting the etch, a LOM-image was taken to assess the status of the structure. As can be seen in figure 2, the contact holes are roughly circular in shape and approximately 0.97 µm in diameter.

After the LOM-images were acquired, the etching of the remaining SiO₂ was performed. A 1% HF solution was used as the etchant. The wafer was placed on a spinning platform and was etched for 45 s and the process was abruptly stopped after the target time by rinsing with water. No probing was done to inspect if the contact holes were open, since the supervisor assured that they were.

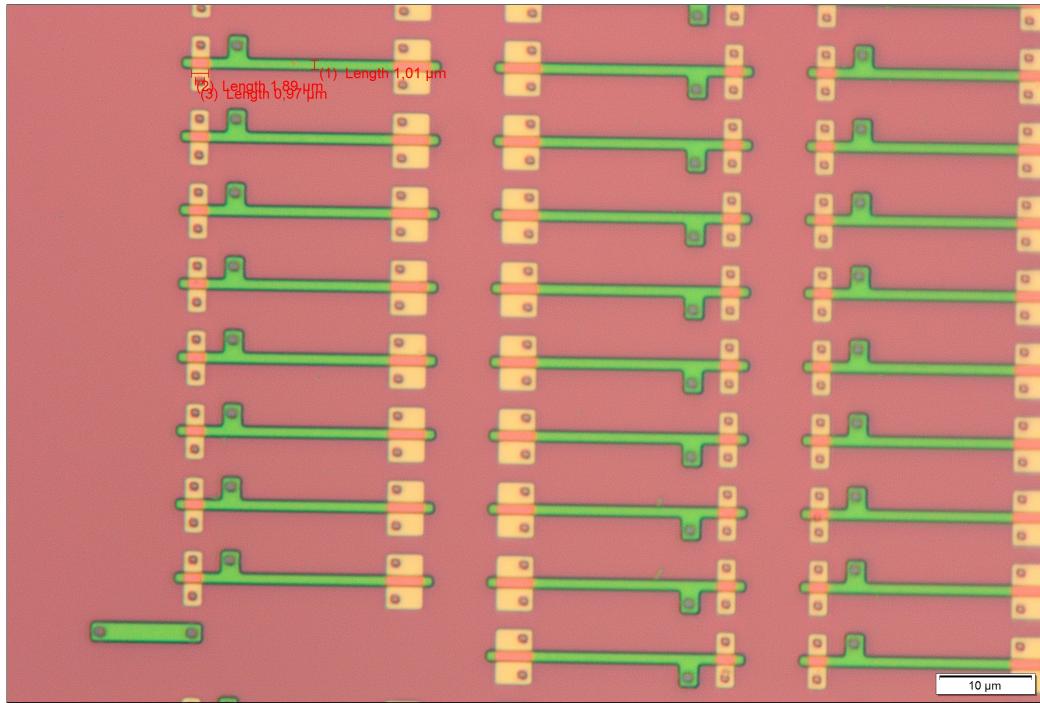


Figure 2: Top-view of the CMOS structure before metal deposition.

3.2 Metal 1 deposition

Once the contact holes were opened, it was time to deposit a layer of 100 nm TiW/500 nm Al. The wafer was placed in the Endura PVD system. The instrument contains two chambers to be able to load and process wafers simultaneously. The system was set to deposit 100 nm TiW/500 nm Al onto the wafer and the process was started. During the deposition, the pressure of the chamber is lowered and the wafer is moved through a series of chambers where the metals are deposited by a Physical Vapor Deposition (PVD) technique named sputtering deposition. The working principle of sputtering deposition is that a sputtering gas, often argon (Ar) is accelerated towards a cathode sputtering target [1]. The sputtered atoms will be accelerated towards an anode placed behind the substrate which will be coated by a thin film. Sputtering deposition has the advantage of being able to deposit metals of a very high melting temperature, such as tungsten (W), as opposed to vaporization deposition. It also gives rise to a high compositional uniformity of the film and the sputtered atoms normally have a good adhesion to the substrate. Figure 3 shows a cross-sectional schematic of the structure after metal deposition.

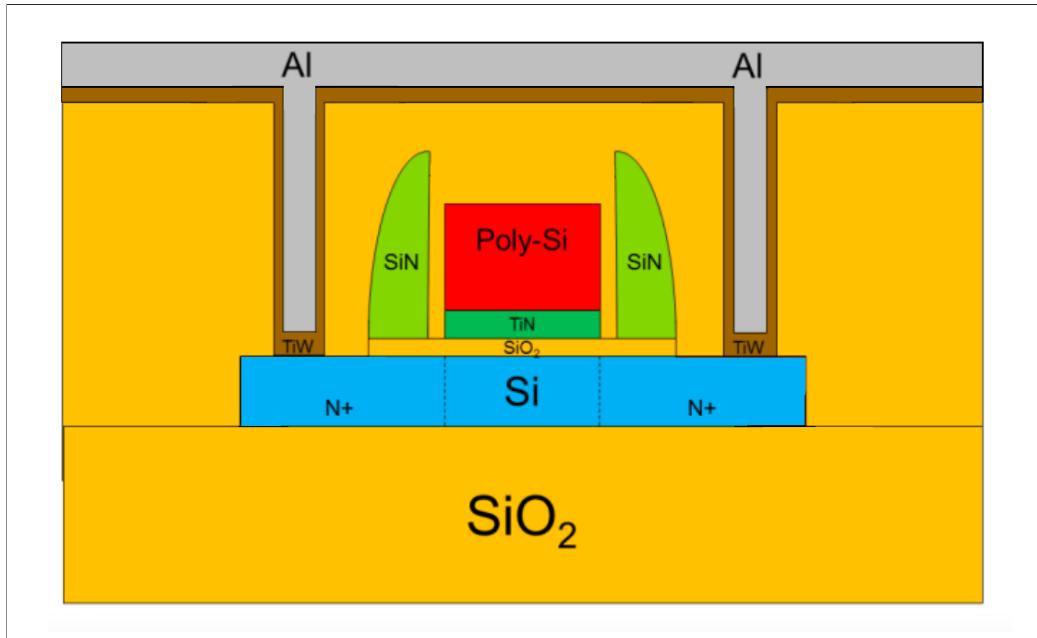


Figure 3: Cross-sectional view of the nMOSFET after metal deposition.

3.3 Lithography

The next step in the process was the remove the unwanted parts of the metal layer, which was done using lithography. The wafer was brought into a photolithography room, which uses yellow fluorescent ambient light in order not to affect the resist deposited on the wafer. The wafer was placed in an instrument that automatically picks up the wafer and places it onto a rotating platform. A small amount of resist was dropped in the center of the wafer at the same time as it was spinning, which evened out the layer across the surface. Lastly, about 5 mm of the resist on the edge of the wafer was removed with acetone in order to avoid sticking to other instruments that use pins to grab the edge of the wafer.

The deposition of resist was followed by a soft bake. The wafer was placed in a furnace at 90 °C for 60 s which was done to remove any residual moisture and solvent in the resist [1], as well as to improve adhesion between the wafer and the resist and to anneal any shear stresses that may have been introduced from spinning. Once the wafer was coated, the wafer was brought to the Nikon NSR Stepper which is a reduction projection exposure system. The system contains a number of different masks that can be employed. The wafer was placed inside the stepper and the correct mask was chosen, after which an automated alignment process was initiated. There were alignment indicators on the wafer structure that the stepper recognizes and uses to make a very precise alignment.

The lithography process was done using a positive resist, which means that the part of the resist that is exposed to light is removed during developing. The resist was developed using a solution that dissolves the exposed part of the resist. The wafer was not spinning after it had been exposed to the chemical agent used for developing in order to make sure that it penetrated into the smaller features of the structure. The resist was rapidly dissolved in the solution. Since even the resist that has not been exposed to light will also dissolve during developing, only much slower, the process was terminated after 60 s to maintain the integrity of the resist pattern. This is also the reason why the wafer is baked before developing [1], to make sure that the resist hardens and is less susceptible to unwanted dissolution.

Figure 4 shows the CMOS structure after lithography. The alignment of the resist was very accurate. A cross-sectional schematic of the structure after lithography is presented in figure 5.

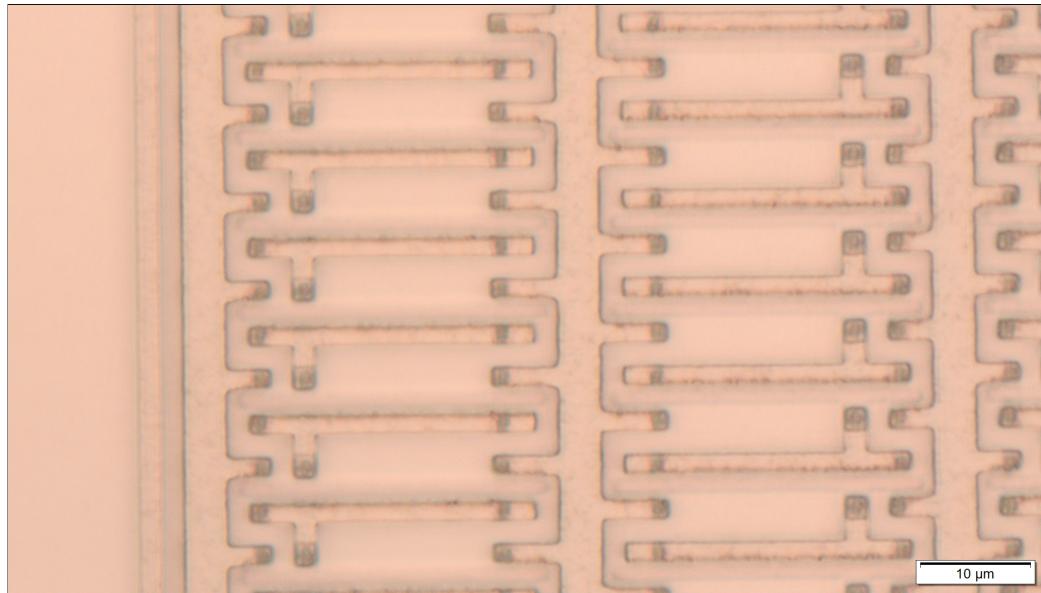


Figure 4: Top-view LOM image of the CMOS structure after lithography.

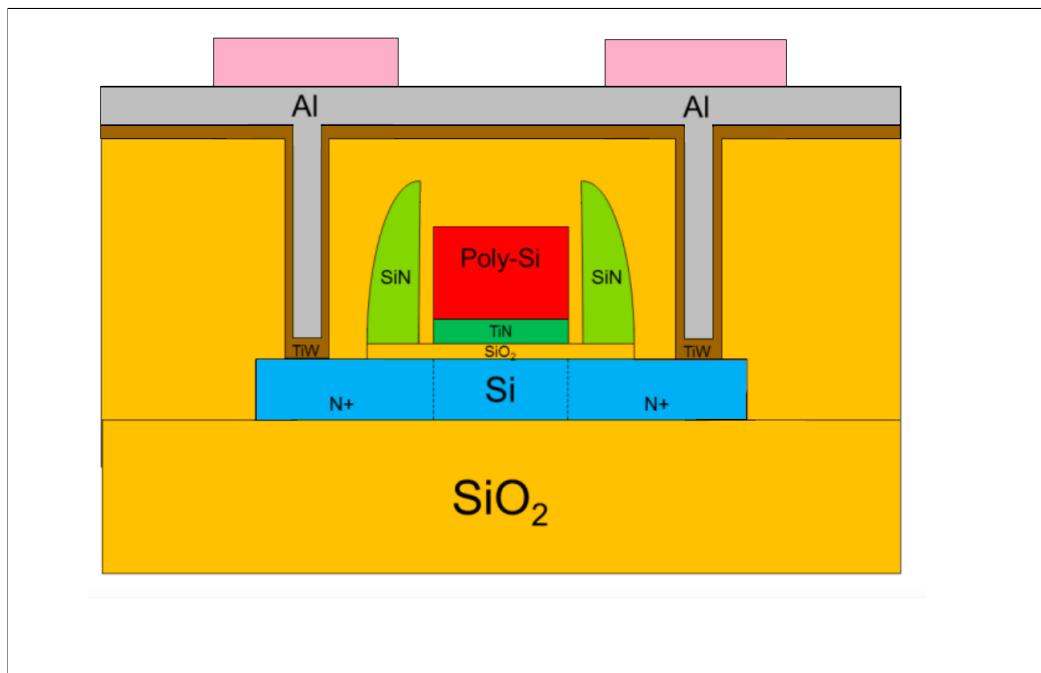


Figure 5: Cross-sectional view of the nMOSFET after developing the resist.

3.4 Metal etching

Since the alignment of the resist was very good, the metal etching could be performed. Before the etching was started, the resist was hard baked for 30 min at 110 °C to improve its physical, chemical and thermal stability. The metal etch was done using Reactive Ion Etching (RIE) which is a dry etching technique that has a very high selectivity and is highly anisotropic [1], which is needed in order to make sharp sidewalls of the structures. RIE uses a chemically reactive plasma formed between two electrodes. The gas introduced in the electric field is ionized and the ions are accelerated towards the substrate where they react with the exposed aluminium. This will also remove any Al₂O₃ that has been formed on the surface. A BCl₃ gas was used for etching. Cl ions are normally left on the sidewalls of the resist, which can lead to the formation of HCl upon exposure to air. To reduce the risk of acid corrosion, the wafer was removed from the RIE instrument and was rinsed for 5 min in de-ionized water at approximately 80 °C. This removes the residual Cl ions on the resist to an acceptable degree. Figure 6 shows the CMOS structure after metal etching.

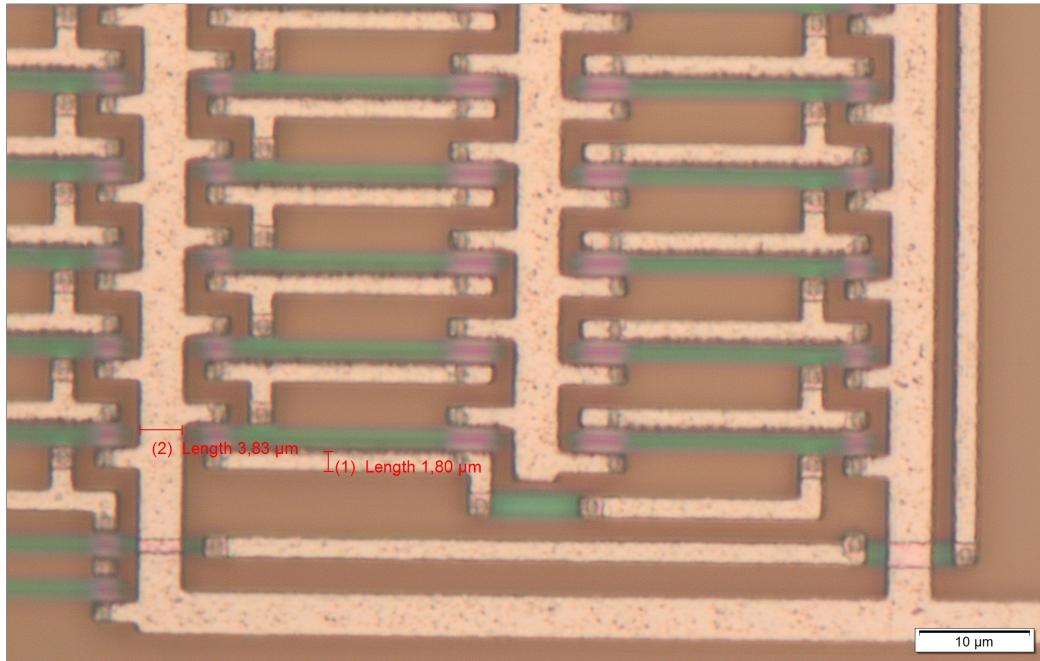


Figure 6: Top-view of the CMOS structure after metal etching.

3.5 Resist stripping

The metal etching was followed by inspection of the structure in the LOM. The laboratory work was finished with the resist layer still on the wafer, due to a lack of time. The resist was stripped by the supervisor with dry stripping using plasma etching equipment at an elevated temperature for 45 min. When stripping the resist, it is very important to have a high selectivity since the oxide of the structure is exposed [1]. Wet stripping has the risk of etching unwanted parts of the structure which is the reason why dry stripping was chosen. Figure 8 shows a cross-sectional schematic of the finished nMOSFET after stripping the residual resist on the metal layer.

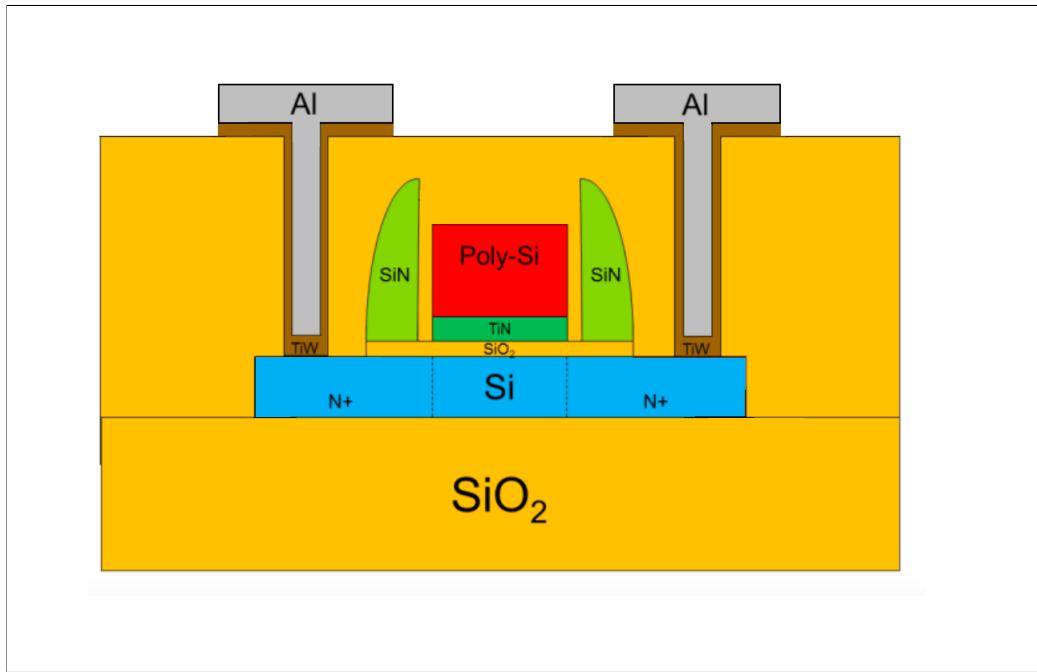


Figure 7: Cross-sectional view of the finished nMOSFET.

4 Results

4.1 TiW 100 nm / Al 500 nm layer thickness

To inspect the thickness of the metal layer, a sheet resistance measurement was performed. The instrument uses a small four-point probe that is gently inserted to the wafer. The assumption of the measurement is that

$$R_s = \rho \cdot t \frac{w}{l} = \rho t \quad (1)$$

where t , w , and l are the thickness, width and length of the wafer respectively. If w and l are assumed to be very large in comparison with thickness, they can be cancelled and the thickness can be calculated with the value of the sheet resistance. The average value from the instrument was $R_s = 59.9 \text{ m}\Omega$ and a resistivity of $\rho = 2.7 \times 10^{-6} \Omega \text{ cm}$ for aluminium was used. Assuming that transport of electrons only takes place in the surface of the Al-layer, the thickness could be calculated as

$$t = \left(\frac{2.7 \times 10^{-6}}{59.9 \times 10^{-3}} \right) = 45 \times 10^{-6} \text{ cm} \quad (2)$$

or 450 nm.

4.2 Finished MOSFET structure

The laboratory work was ended before the resist was stripped, so the LOM images of the finished CMOS structure were provided by the supervisor. Figure 8 shows a LOM image of the finished CMOS structure.

The resolution of the process was evaluated using a standardized resolution target structure. The numbers indicated on the individual targets depict the smallest size in μm that it is possible to clearly resolve. As can be seen in figure 9, the lines and holes on the $0.8 \mu\text{m}$ target are quite sharp and the targets at smaller sizes start to become more diffuse.

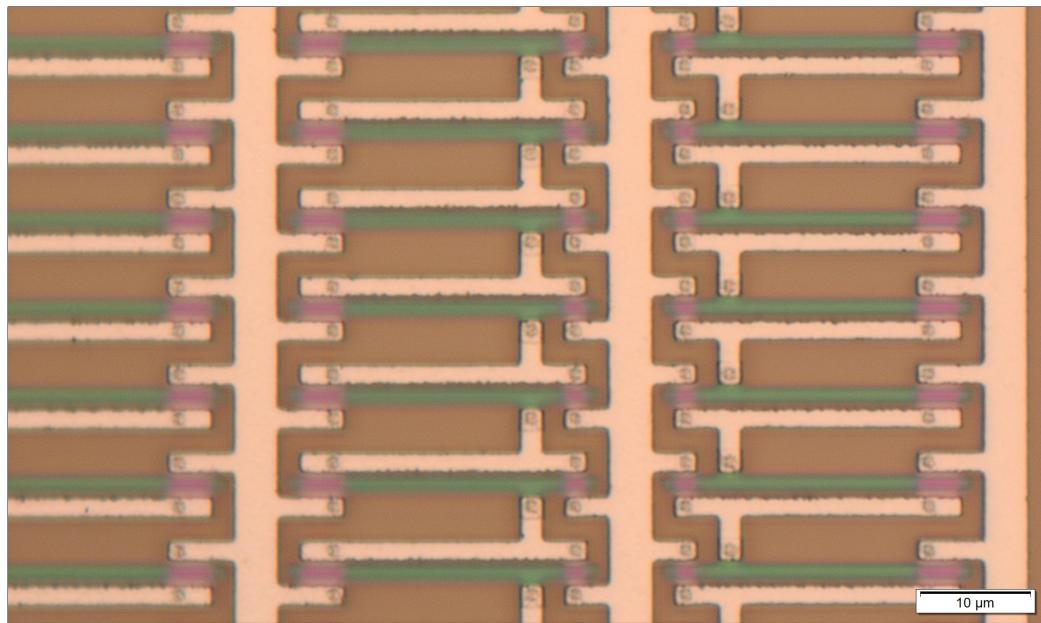


Figure 8: Top-view of the CMOS structure after the resist was stripped.

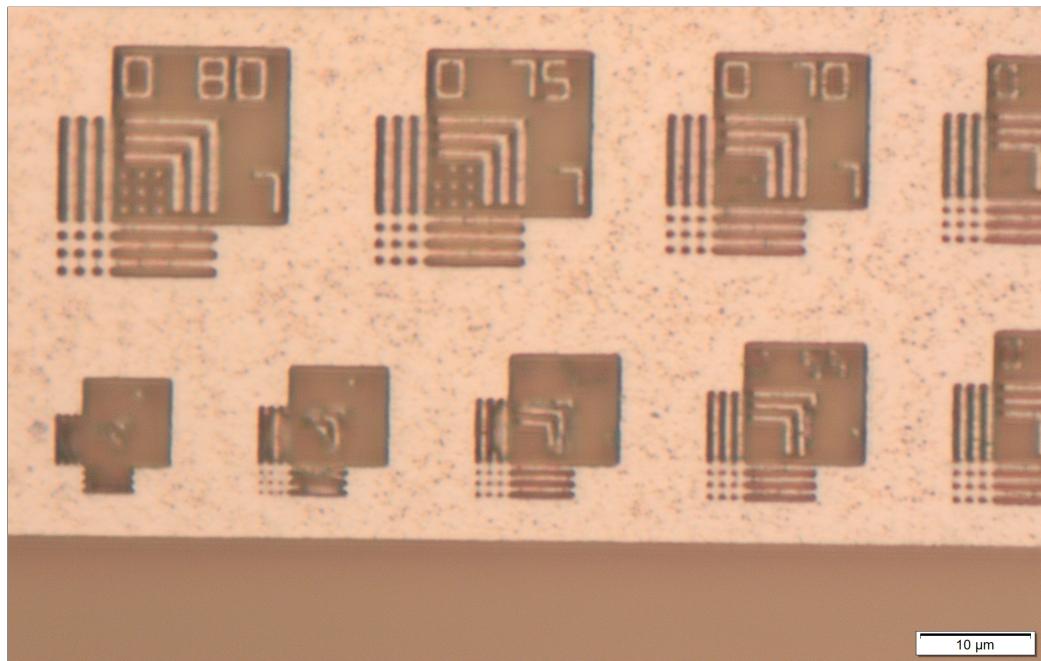


Figure 9: Resolution target of the wafer, showing the maximum resolution.

5 Conclusions

The CMOS preparation process developed at Electrum Laboratory at KTH Kista uses nanofabrication process integration to create precise structures at a resolution size of approximately $0.8\text{ }\mu\text{m}$. The size of the smallest features of the CMOS that can be regarded as critical, namely the contact holes, are designed to be $1\text{ }\mu\text{m}$, which indicates that the process has a high enough resolution to create the structure without running the risk of unwanted short-circuits.

The thickness of the metal layer was calculated using the sheet resistance to be 450 nm . Since the sheet resistance only measures the aluminium layer, which had a target thickness of 500 nm , the sputter deposition technique can be said to have a very good accuracy in terms of film thickness. The reason for the deviation is that the sheet resistance is measured using different points, and the average value of the points was not chosen for the calculations. A smaller average resistance would give a higher thickness.

Since the metal lines forming the contacts were close to the target thickness of $1\text{ }\mu\text{m}$, it can be assumed that the wet etch had a high enough degree of anisotropy. If the etch was too isotropic, the resist would have been etched in width as well as in depth and the metal lines would have a higher thickness than the target. The same train of logic can be applied to the RIE which also proved to have a good degree of anisotropy.

For a personal reflection on the lab, it was very interesting to see the steps described in literature in action. The biggest surprise was to see how well the different process steps actually work. Very often, what is presented in literature is very far from how it actually turns out in reality. Especially to see how accurately the stepper can align the patterns was very impressive. All in all, the lab was a great experience.

References

- [1] S. A. Campbell, *Engineering at the Micro- and Nanoscale*, 3rd ed. Oxford University Press, 2008.