Introduction to Embedded System Design using Zynq

Zynq
Vivado 2013.3 Version

Objectives

- **After completing this module, you will be able to:**
  - Define a Zynq All Programmable SoC (AP SoC) processor component
  - Enumerate the key aspects of the Zynq AP SoC processing system
  - Describe the embedded design flow
  - Understand the function of the IP Integrator tool
  - Indicate how the hardware design is linked to the software development environment

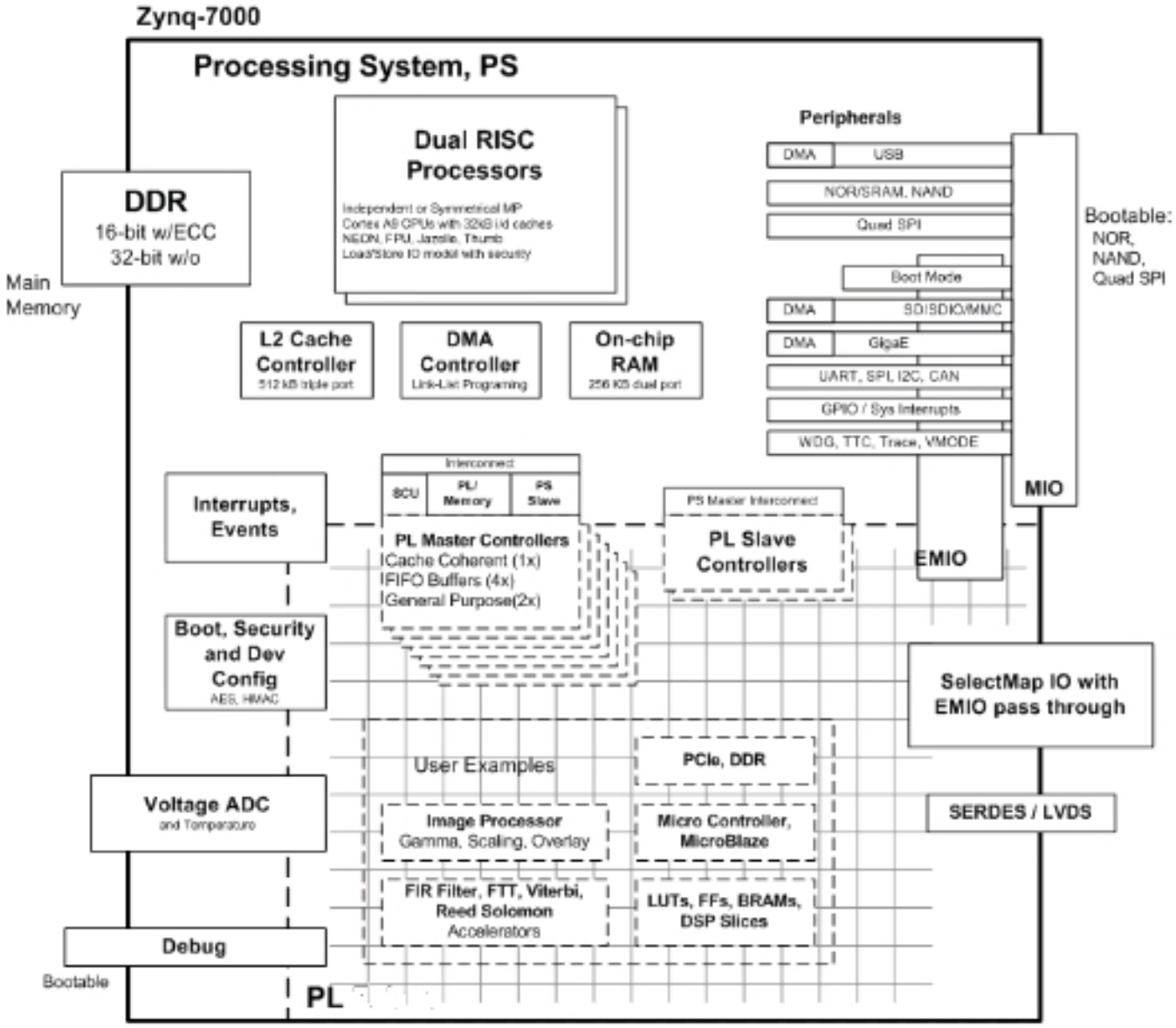
Outline

- ***Embedded Processor Component***
- **Overview of Vivado for Embedded System Design**
- **Embedded System Development Flow**
- **Hardware Platform Creation**
- **SDK Software Platform**
- **Summary**

Embedded Design Architecture in Zynq

- **Embedded design with Zynq is based on:**
  - Processor and peripherals
    - Dual ARM® Cortex™ -A9 processors of Zynq-7000 AP SoC
    - AXI interconnect
    - AXI component peripherals
    - Reset, clocking, debug ports
  - Software platform for processing system
    - Bare Metal Applications or OS's (e.g. Linux, FreeRTOS)
    - C language support
    - Processor services
    - C drivers for hardware
  - User application
    - Interrupt service routines (optional)

Zynq AP SoC PS and PL Block Diagram

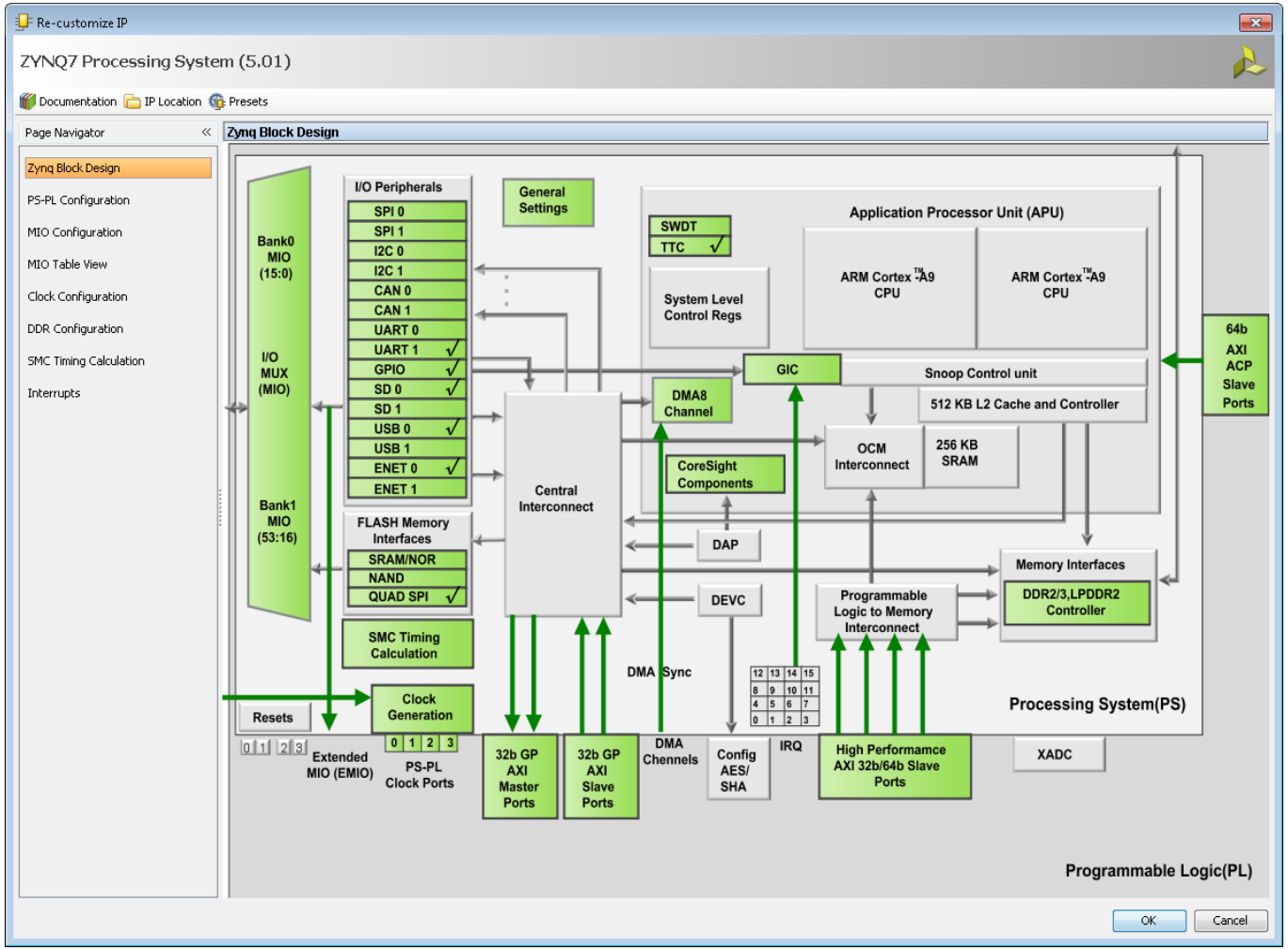


The PS and the PL

- **The Zynq-7000 AP SoC architecture consists of two major sections**
  - PS: Processing system
    - Dual ARM Cortex-A9 processor based
    - Multiple peripherals
    - Hard silicon core
  - PL: Programmable logic
    - Uses the same 7 series programmable logic
      - Artix™-based devices: Z-7010, Z-7015 and Z-7020 (high-range I/O banks only)
      - Kintex™-based devices: Z-7030, Z-7045, and Z-7100 (mix of high-range and high-performance I/O banks)

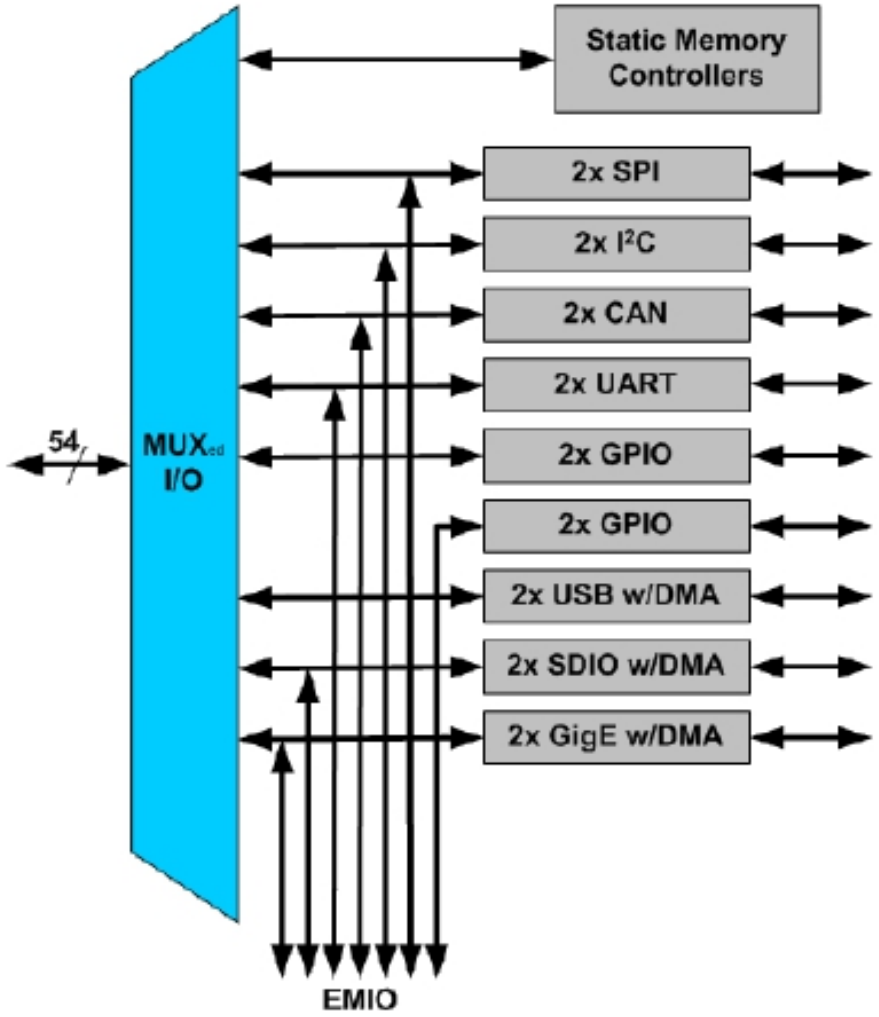
PS Components

- **The Zynq AP SoC processing system consists of the following blocks**
  - Application processing unit (APU)
  - I/O peripherals (IOP)
    - Multiplexed I/O (MIO), extended multiplexed I/O (EMIO)
  - Memory interfaces
  - PS interconnect
  - DMA
  - Timers
    - Public and private
  - General interrupt controller (GIC)
  - On-chip memory (OCM): ROM and RAM
  - Debug controller: CoreSight



Zynq Architecture Built-in Peripherals

- **Two USB 2.0 OTG/Device/Host**
- **Two Tri- Mode GigE (10/100/1000)**
- **Two SD/SDIO interfaces**
  - Memory, I/O and combo cards
- **Two CAN 2.0Bs, SPIs , I2Cs, UARTs**
- **Four GPIO 32bit Blocks**
  - 54 available through MIO; other available through EMIO
- **Multiplexed Input/Output (MIO)**
  - Multiplexed pinout of peripherals and static memories
- **Extended MIO**
  - Maps PS peripheral ports to the PL



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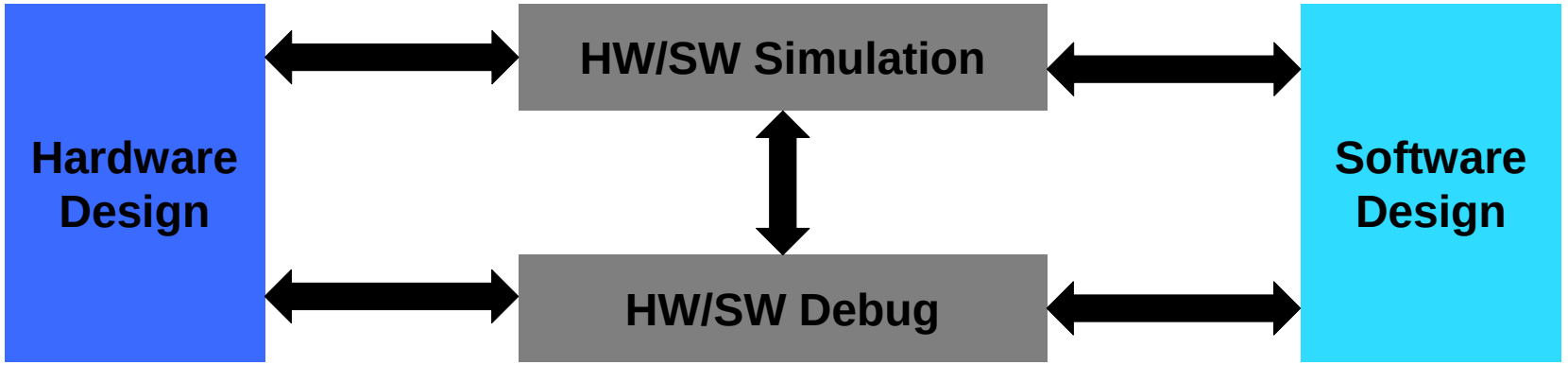
Vivado

- **What are Vivado, IP Integrator and SDK?**
  - Vivado is the tool suite for Xilinx FPGA design and includes capability for embedded system design
    - IP Integrator, is part of Vivado and allows block level design of the hardware part of an Embedded system
    - Integrated into Vivado
    - Vivado includes all the tools, IP, and documentation that are required for designing systems with the Zynq-7000 AP SoC hard core and/or Xilinx MicroBlaze soft core processor
    - Vivado + IPI replaces ISE/EDK
  - SDK is an Eclipse-based software design environment
    - Enables the integration of hardware and software components
    - Links from Vivado
- **Vivado is the overall project manager and is used for developing non-embedded hardware and instantiating embedded systems**
  - Vivado/IP Integrator flow is recommended for developing Zynq embedded systems using 2013.2 and later

Vivado Components

- **Vivado/IP Integrator**
  - Design environment for configuration of PS, and hardware design for PL
  - Hardware Platform (xml)
  - Platform, software, and peripheral simulation
  - Vivado logic analyzer integration
- **Software Development Kit (SDK)**
  - Project workspace
  - Hardware platform definition
  - Board Support Package (BSP)
  - Software application
  - Software debugging



Embedded System Tools: Hardware

- **Hardware and software development tools**
  - IP Integrator
  - IP Packager
  - Hardware netlist generation
  - Simulation model generation
  - Xilinx Microprocessor Debugger (XMD)
  - Hardware debugging using Vivado analyzer

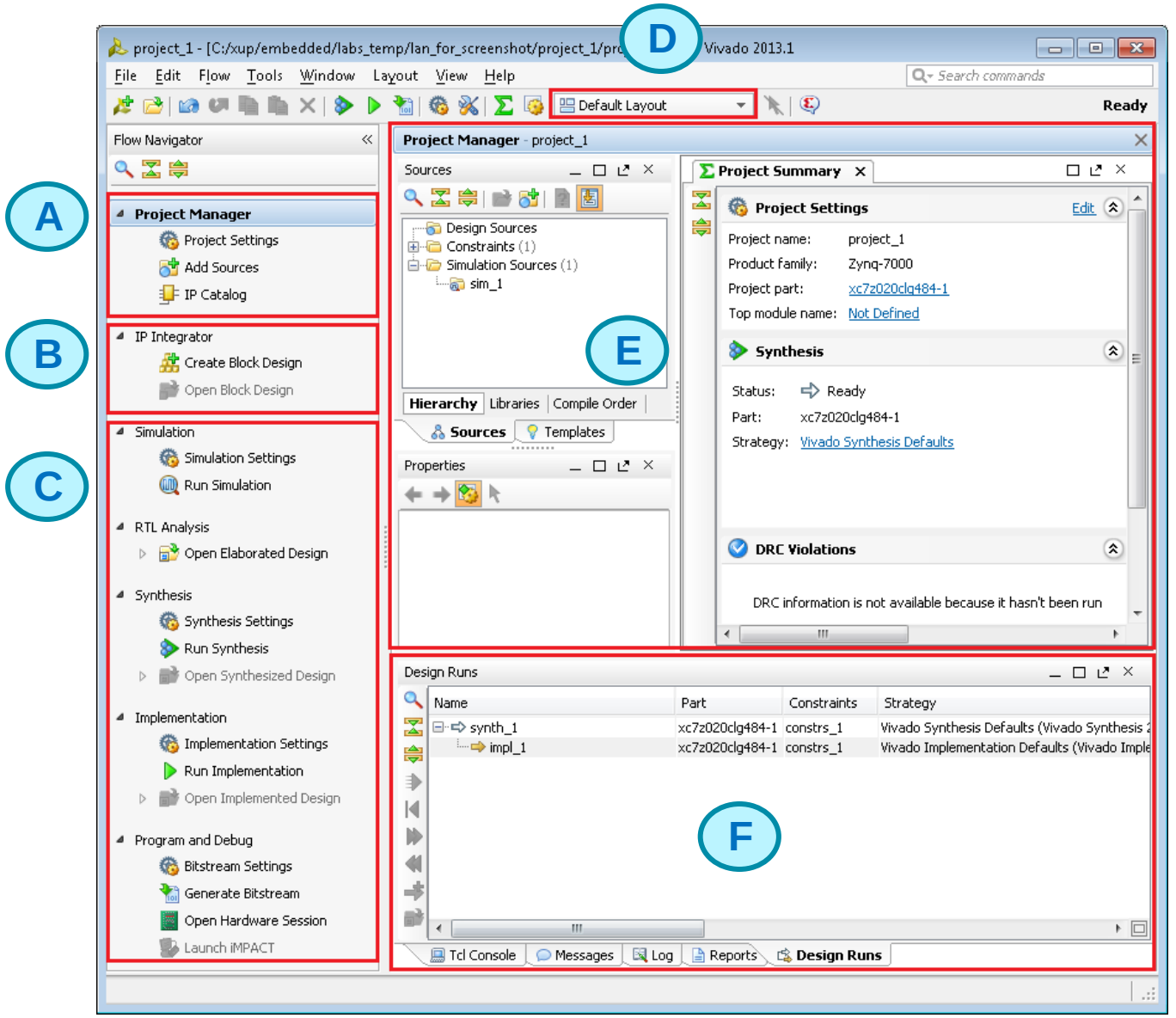
Embedded System Tools: Software

- **Eclipse IDE-based Software Development Kit (SDK)**
  - Board support package creation
  - GNU software development tools
  - C/C++ compiler for the MicroBlaze and ARM Cortex-A9 processors (gcc)
  - Debugger for the MicroBlaze and ARM Cortex-A9 processors (gdb)
  - TCF framework – multicore debug
- **Board support packages (BSPs)**
  - Stand-alone BSP
    - Free basic device drivers and utilities from Xilinx
    - NOT an RTOS

Vivado View

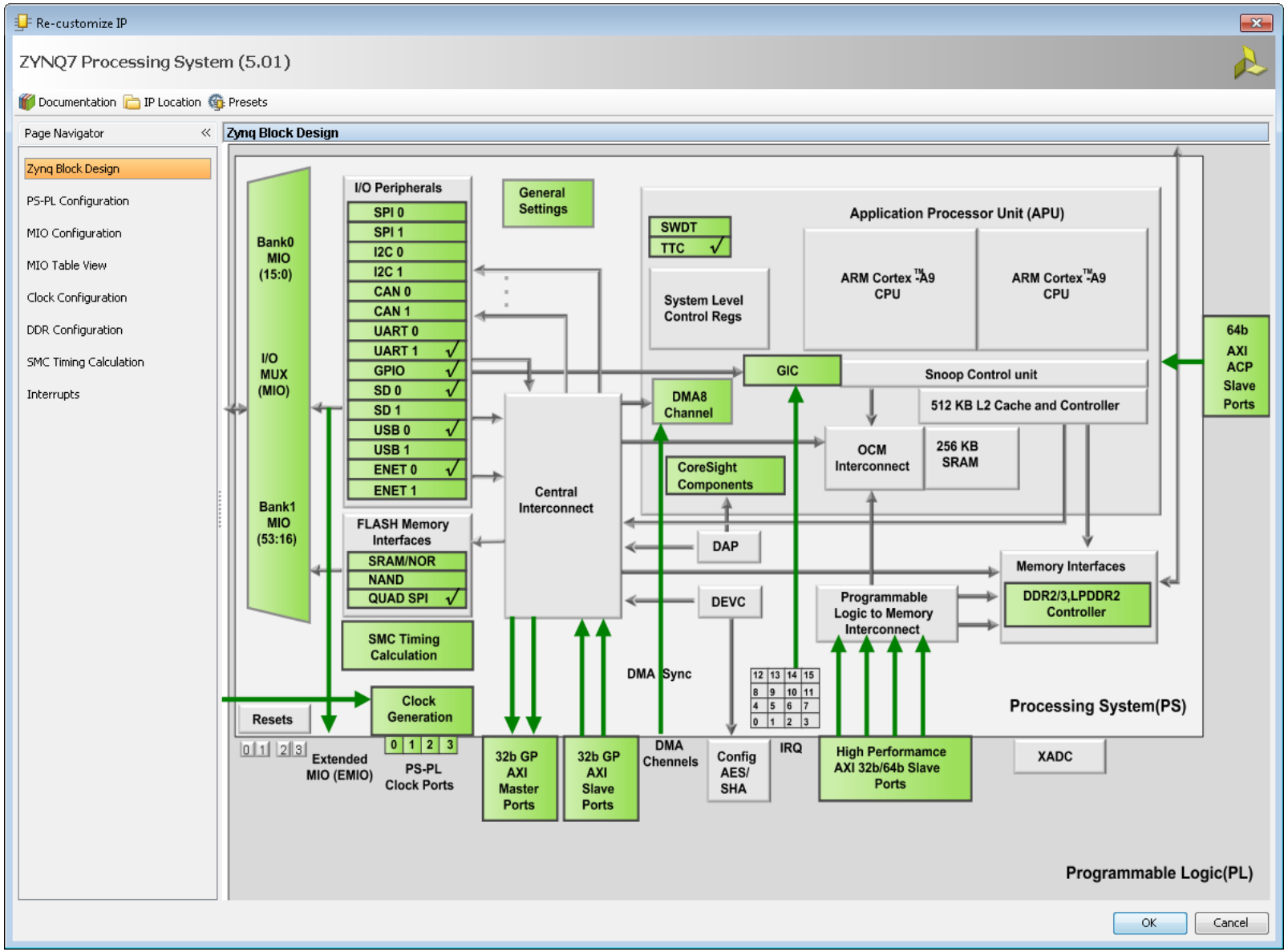
- Customizable panels

- A: Project Management
- B: IP Integrator (2013.2)
- C: FPGA Flow
- D: Layout Selection
- E: Project view/Preview Panel
- F: Console, Messages, Logs

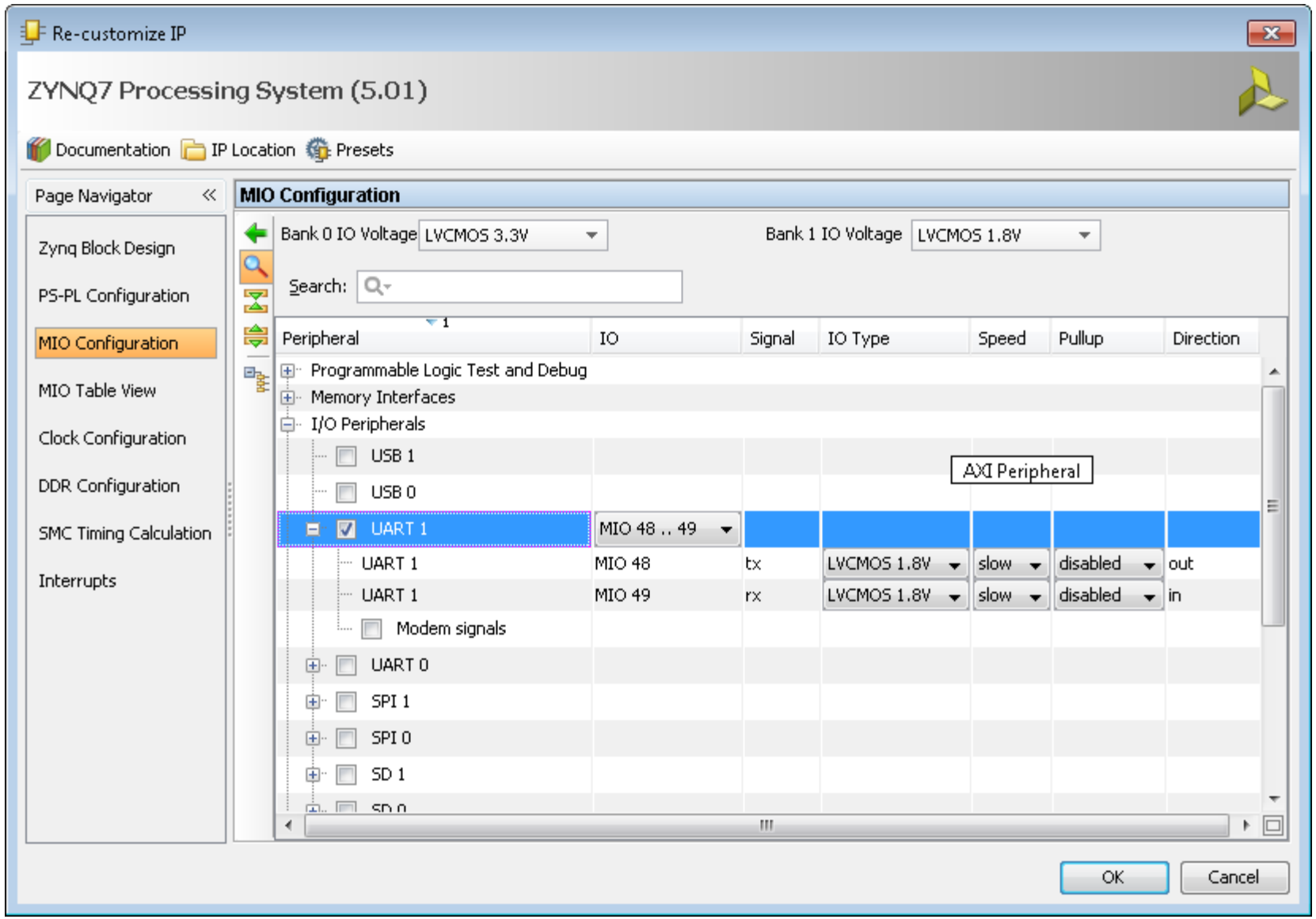


Zynq Customization Processing System

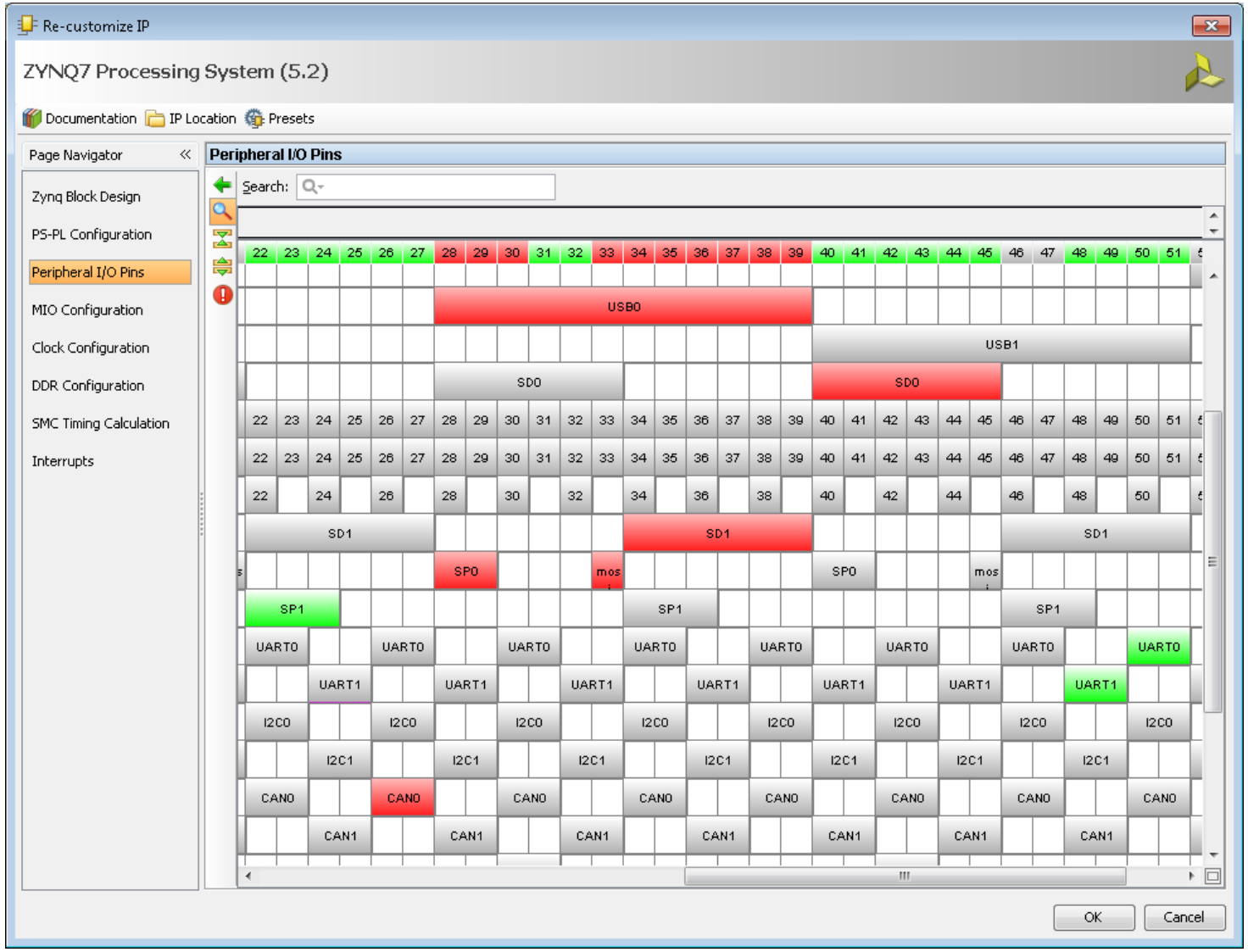
- Block Configuration
- PS-PL Interface Configuration
- MIO Configuration/Table View
- Clock Configuration
- DDR
- SMC Timing Calculation
- Interrupt Configuration



MIO Configuration

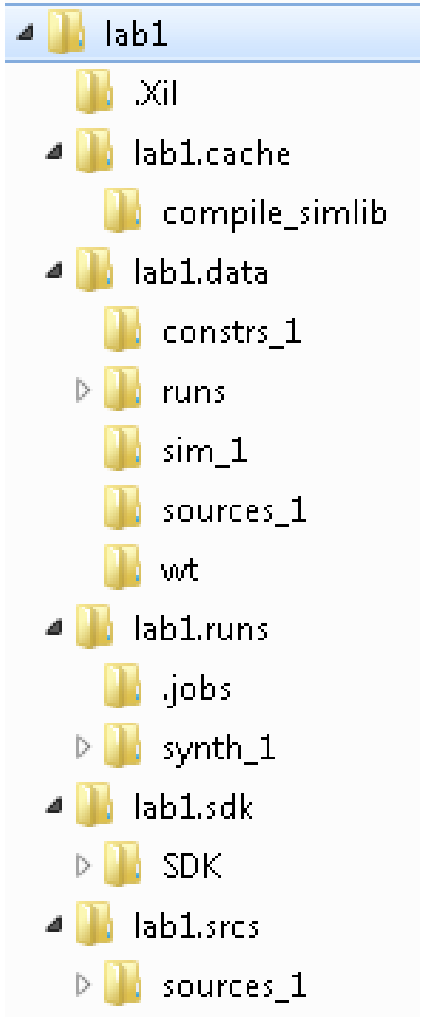


MIO Configuration…



Project Files

- **Top level Directory**
  - .xpr Vivado Project File (xml file), log files, journal
- **.srcs**
  - Project source files, IP Integrator files
- **.data**
  - Vivado database, internal data
- **.runs**
  - Synthesis, Implementation runs
- **.sdk**
  - SDK Export directory, Hardware Platform (xml)
- **.cache**
  - Temporary Files



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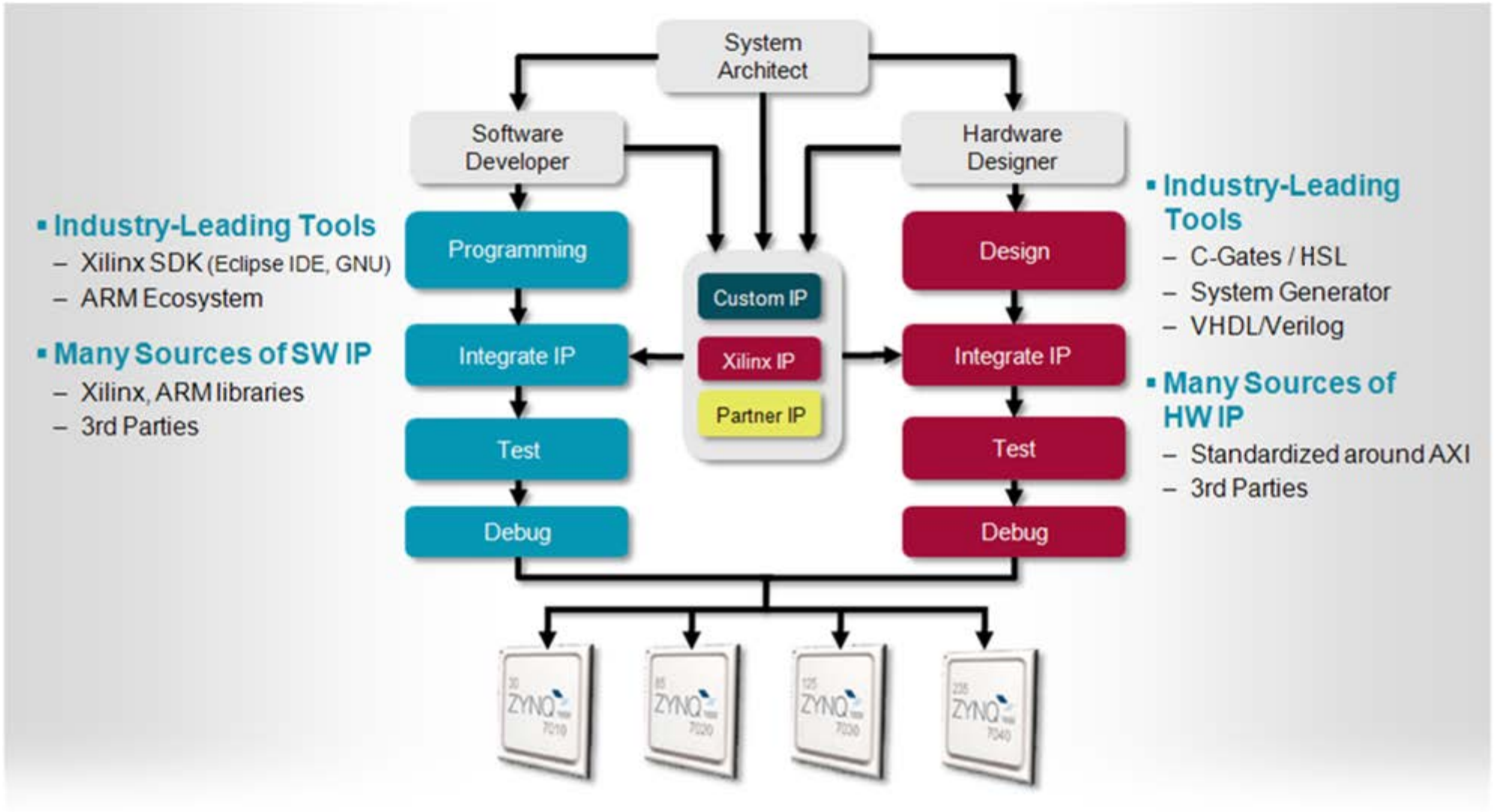
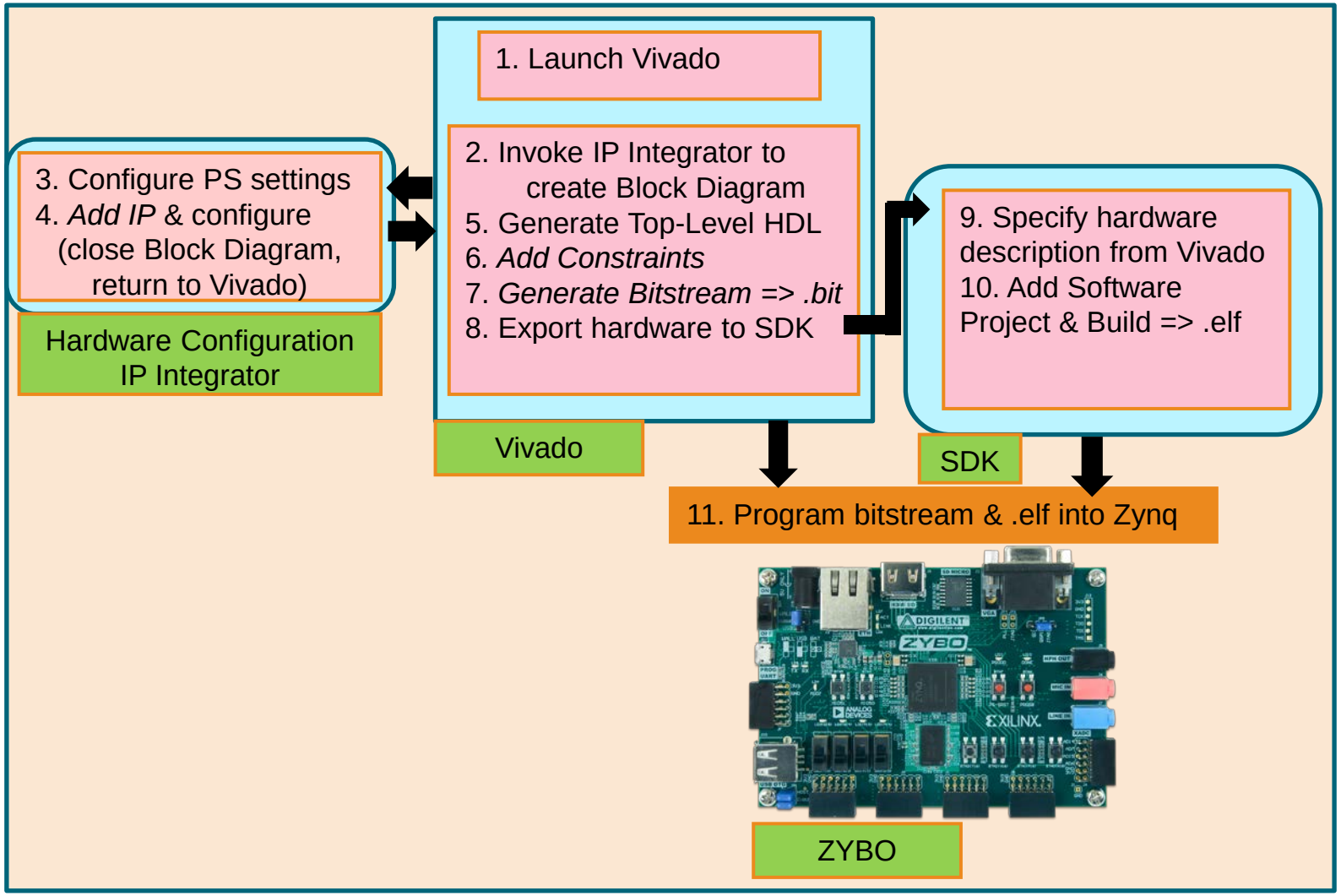
Embedded System Design Flow for Zynq-7000 AP SoC



Embedded System Design using Vivado

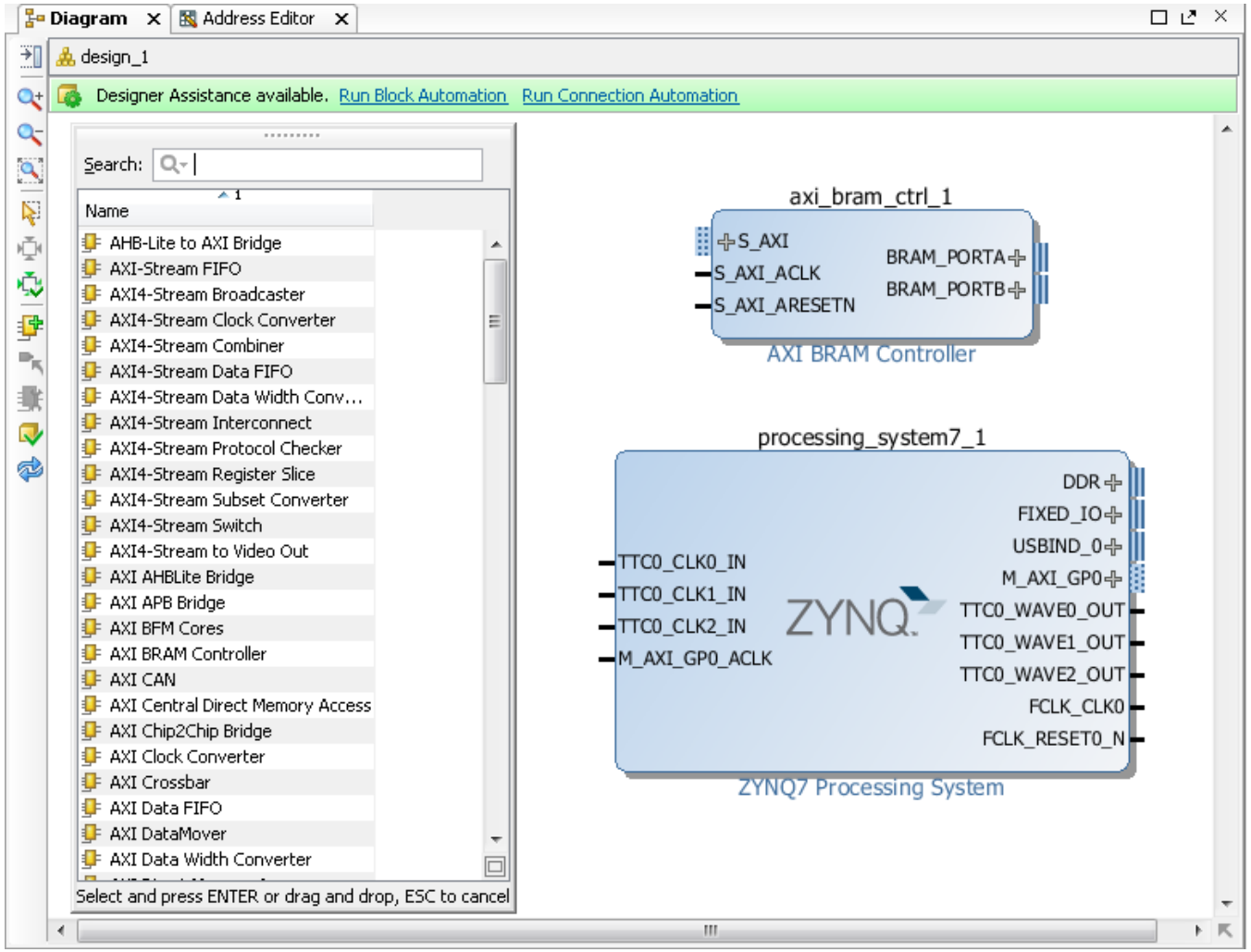
- Create a new Vivado project, or open an existing project
- Invoke IP Integrator
- Construct(modify) the hardware portion of the embedded design
- Create (Update) top level HDL wrapper
- [optional] Synthesize any non-embedded components and implement in Vivado
- Export the hardware description, and launch SDK
- Create a new software board support package and application projects in the SDK
- Compile the software with the GNU cross-compiler in SDK
- [optional] Download the programmable logic's completed bitstream using iMPACT
- [optional] Use SDK to download the program (the ELF file)

Embedded System Design using Vivado



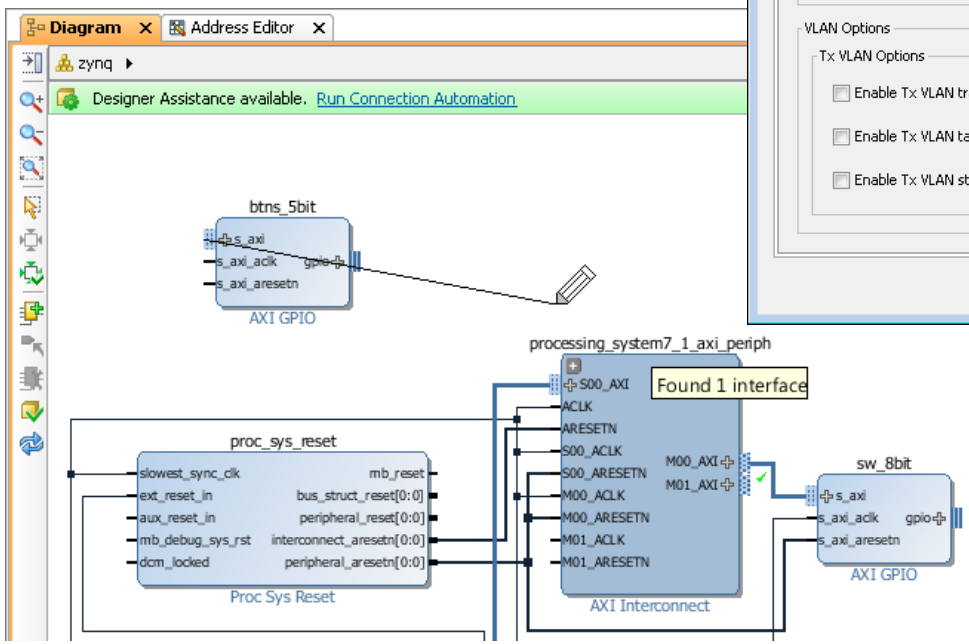
Add IP Integrator Block Diagram

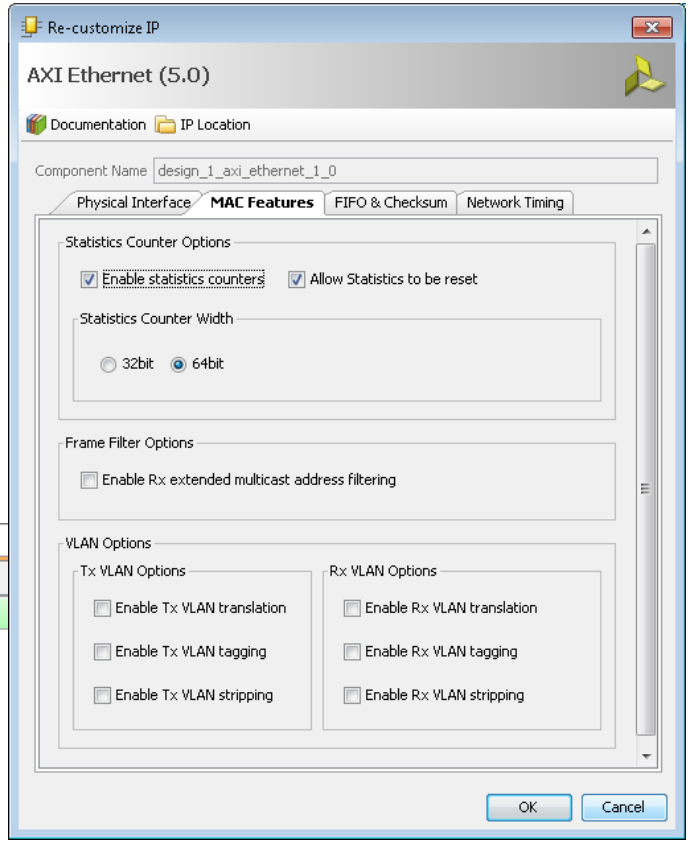
- **IP Integrator Block Diagram opens a blank canvas**
- **IP can be added from the IP catalog**
- **Drag and drop interface**
- **Intelligent Design environment**
  - Design Assistance
  - Connection automation
  - Highlights valid connections
  - Group, create hierarchal blocks
- **Can import custom IP using IP Packager**



Configuring Hardware in IP Integrator

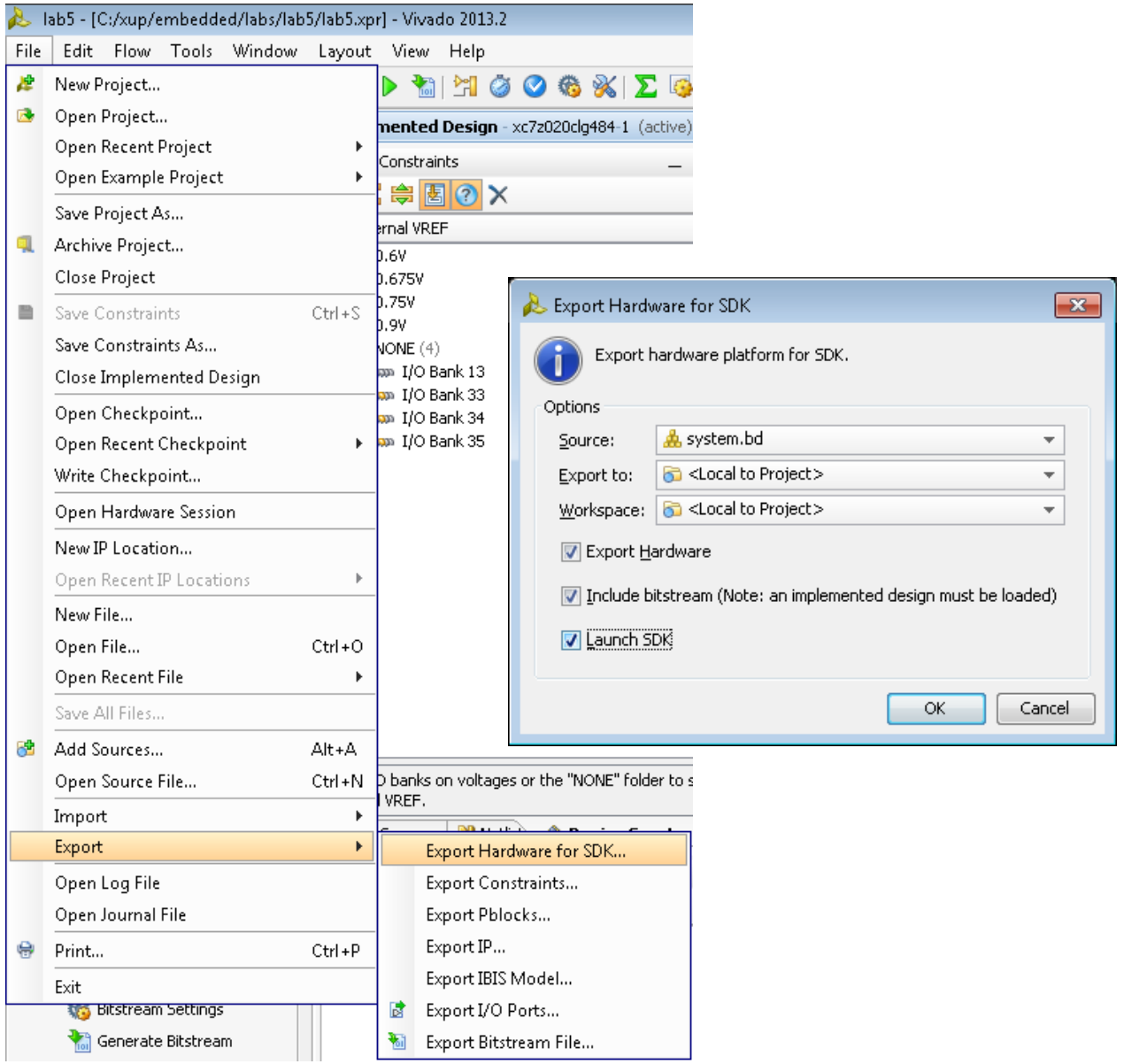
- **Double click blocks to access configuration options**
- **Drag pointer to make connections**
  - Highlights valid connections
- **Connection Automation**
  - Automatically connect recognised interfaces
- **Automatically Redraw system**





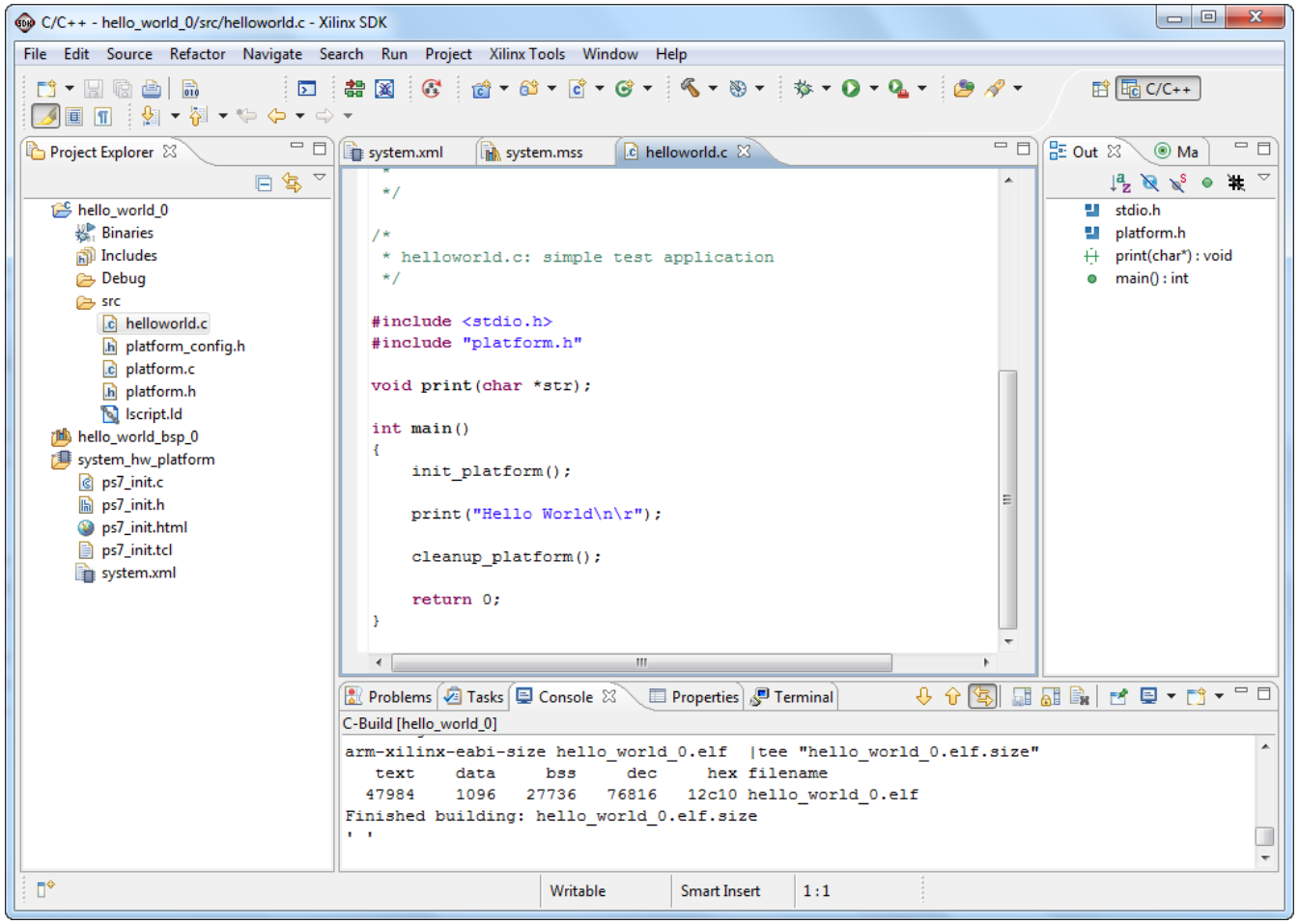
Exporting to SDK

- **Software development is performed with the Xilinx Software Development Kit tool (SDK)**
  - Hardware configuration in Vivado
- **An XML description of the hardware is exported to SDK**
  - The hardware platform is built on this description
  - Only one hardware platform for each SDK project
  - (Optionally export bitstream)
- **The SDK tool will then associate user software projects to hardware**



Software Development Flow

- **Create hardware platform project**
  - Automatically performed when SDK tool is launched from Vivado project
- **Create BSP**
  - System software, board support package
- **Create software application**
- **Create linker script**
- **Build project**
  - compile, assemble, link output file *<app_project>.elf*



Configuring FPGA and Downloading Application

- **Download the bitstream**
  - Only if PL is used
  - Input file *<top_name>.bit*
- **The Xilinx iMPACT tool downloads the bitstream to the target**
- **The bitstream can be downloaded from both tools**
  - Vivado
  - SDK
- **Requires that the download cable is connected**

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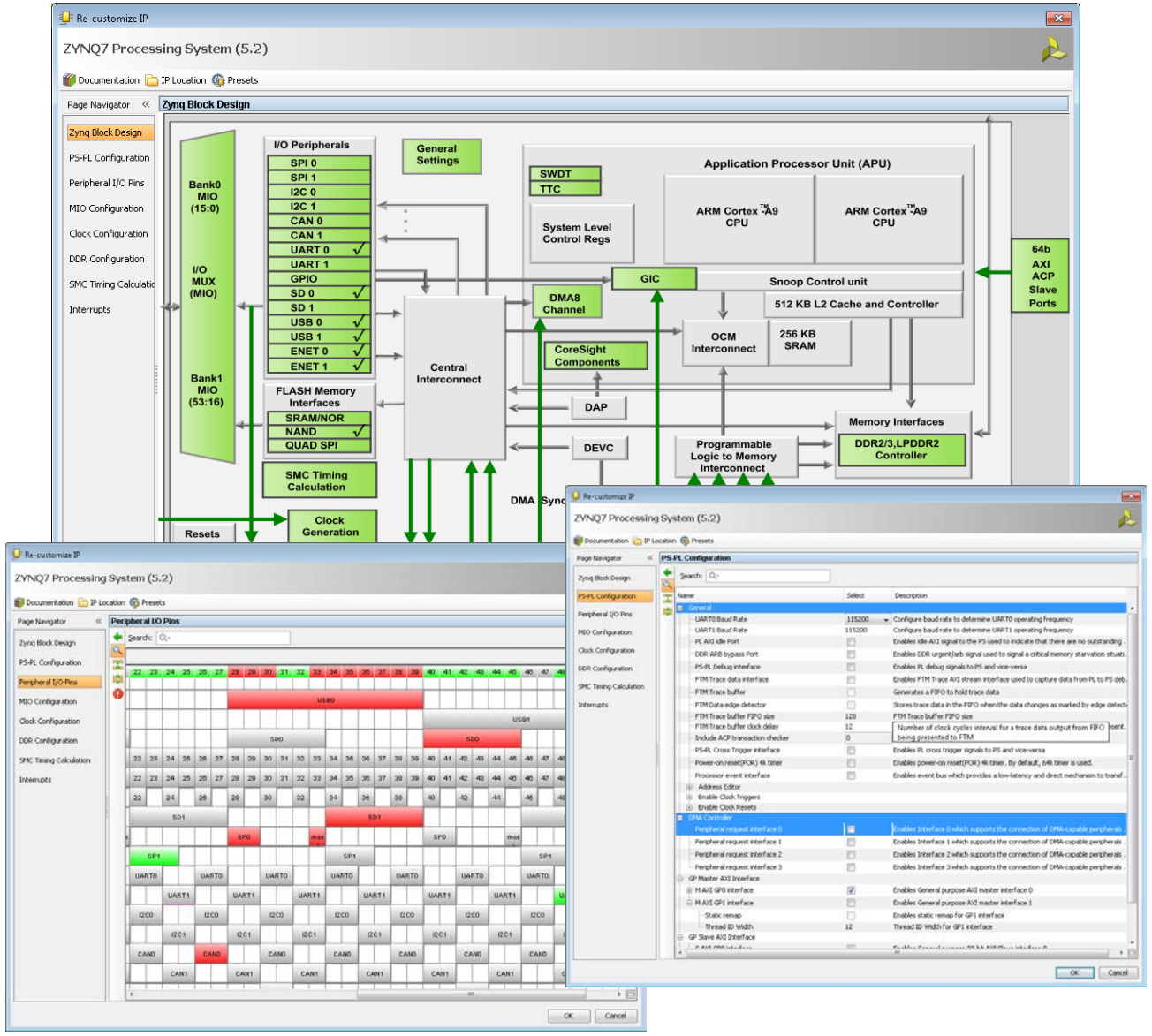
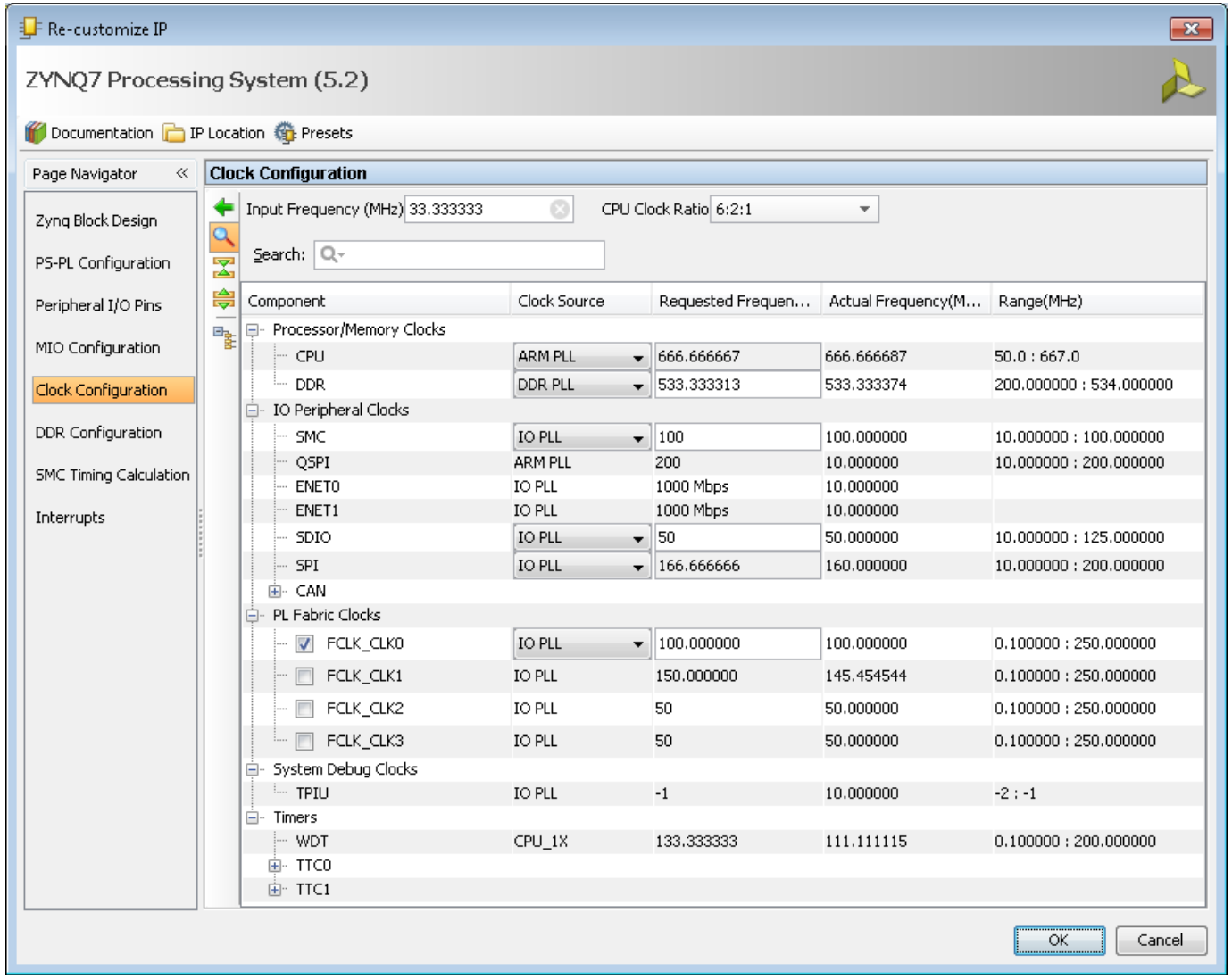
Zynq Configuration GUI

- **Provides a graphical view of the PS to configure**
  - ARM cores
  - I/O peripherals
  - DDR controller
  - Memory systems
- **I/O partitioning between dedicated PS pins and programmable logic I/O**
- **Zynq-7000 AP SoC PS is configured via a set of memory-mapped configuration registers**



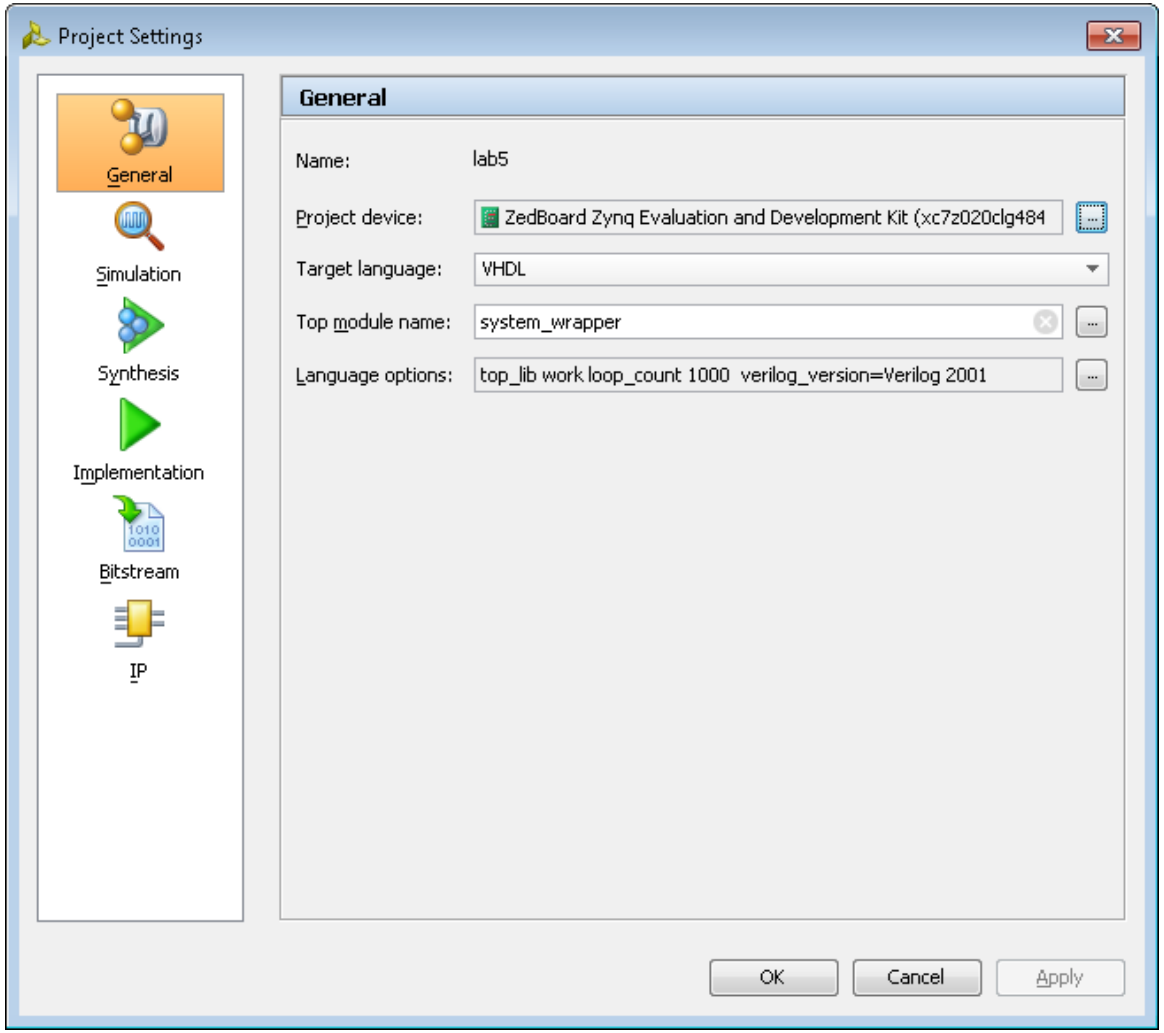
Clock configuration

- **Clock Configuration**
  - Input frequency can be set
    - Processor, DDR
  - All IOP clock frequencies can be set
  - Clock to PL configuration
  - Set Timers



Project Settings

- **Accessed from flow navigator**
- **Default settings are typically used**
- **Set/change target device**
  - Architecture, Device size, Package, Speed grade
- **Simulation, Synthesis, Implementation, Bitstream options**
- **IP repository directory**
  - Provide path to custom IP not present in the current project directory structure



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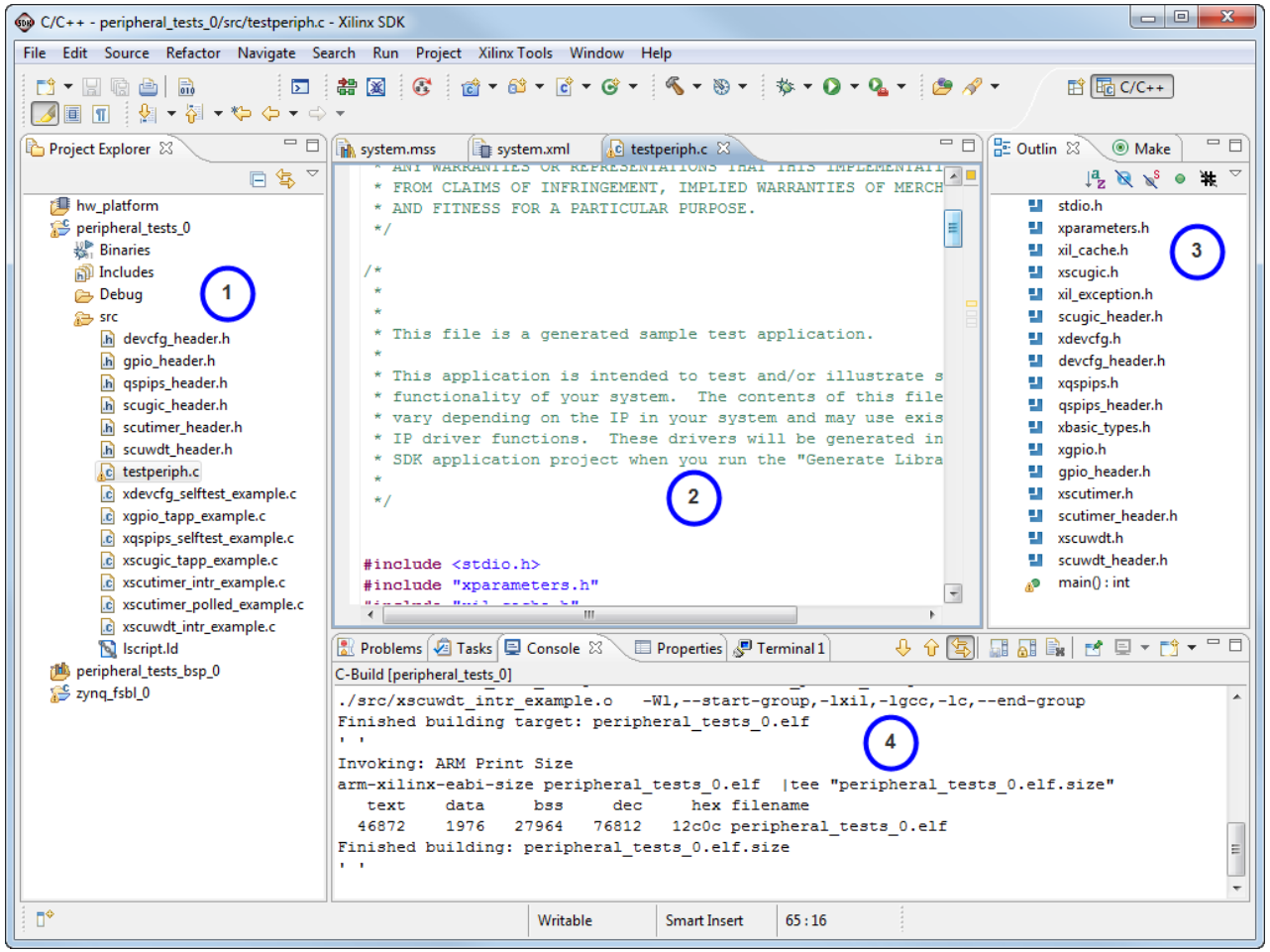
Software Development Kit (SDK)

- **Full-featured software design environment**
- **Separate tool from Vivado – can install standalone for SW teams**
- **Based on popular Eclipse open-source IDE**
- **Used for software applications only; hardware design and modifications are done in Vivado**
- **Well-integrated environment for seamless debugging of embedded targets**
- **Sophisticated software design environment with many options and features with support for**
  - Multiple processors
  - Multiple software platforms
  - Multiple software applications
- **Fully Featured C/C++ code editor and error navigator**

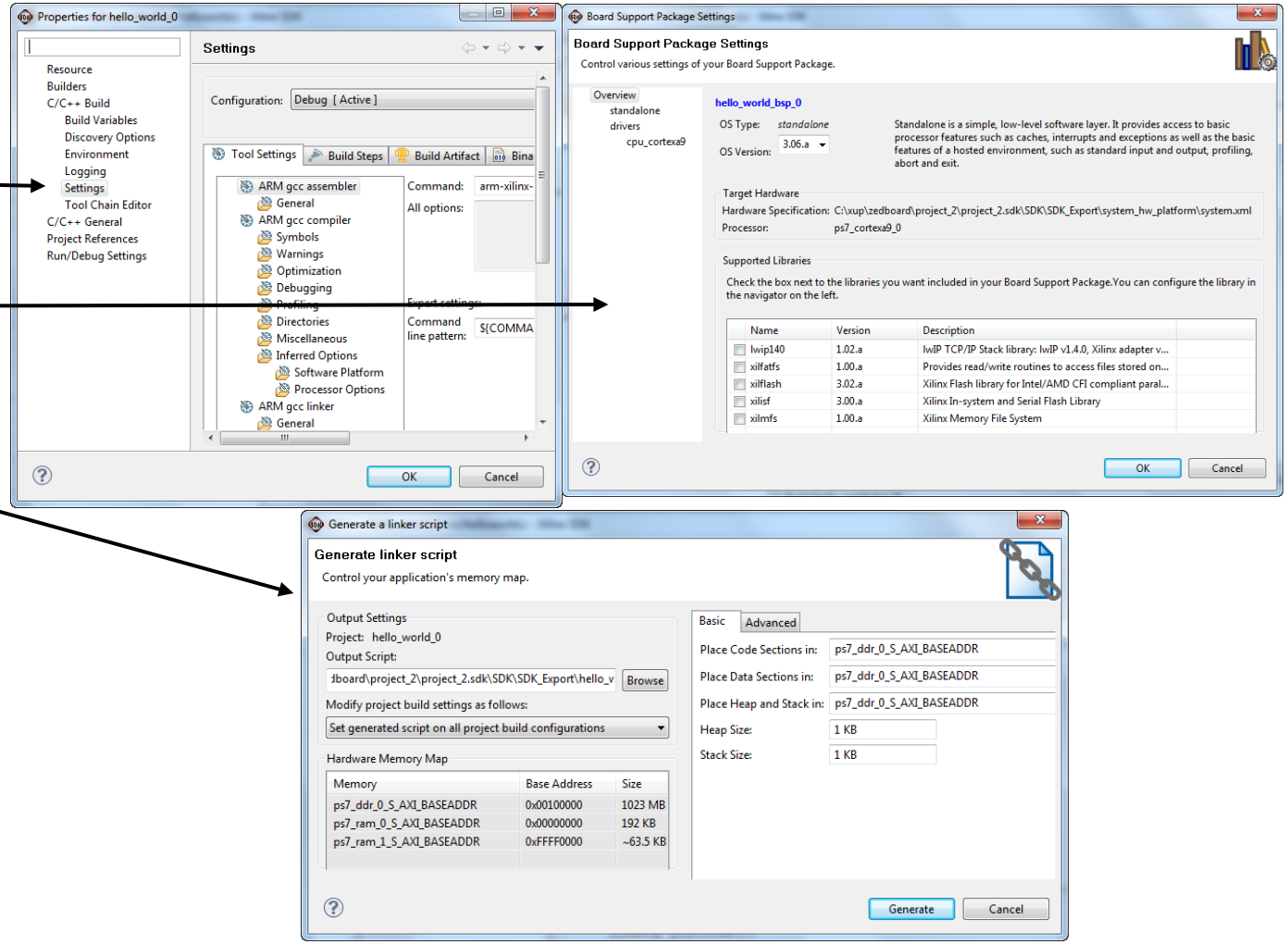
SDK Workbench Views

1. C/C++ project outline displays the elements of a project with file decorators (icons) for easy identification
2. C/C++ editor for integrated software creation
3. Code outline displays elements of the software file under development with file decorators (icons) for easy identification
4. Problems, Console, Properties views list output information associated with the software development flow



Software Management Settings

- **Software is managed in three major areas**
  - Compiler/Linker Options
    - Application program
  - Software Platform Settings
    - Board support package
  - Linker Script Generation
    - Assigning software to memory resources
- **Covered in more detail later**



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Summary

- Vivado includes all the tools, documentation, and IP necessary for building embedded systems
- IPI is a System Level design tool that increases productivity, allowing designs to be completed faster
- The Software Development Kit (SDK) is a comprehensive software development environment for software applications
- An embedded processing system component is built with IP provided in the IP Catalog. Designers can also add their own custom IP to this catalog
- The PS Configuration wizard permits access to several configurable features of PS