Notes on Average Determinant Project Lab.

Digital System Design

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1 Generating data files with random coefficients

```
./adet.exe 0 fName
```

Executing the `adet` program as shown will generate two files:

`fName.dat` - the file with the `INTI_xx` strings, to initialize the input memory MemIn, with random values for the matrices complex elements. Copy this `INTI_xx` strings for the corresponding initialization of the input memory in `MemIn.vhd` file. Each complex value of the matrices is packed as following (on each memory position):

4bits	12bits	4bits	12bits
0	Re (Q5.7)	0	Im (Q.5.7)

The different sets of the matrices values are stored on the following memory positions (address space of the 32bit port of the input memory):

Address	Content (32bits)	Matrix
0x00	X_{11}	0
0x01	X_{12}	0
0x02	X_{21}	0
0x03	X_{22}	0
0x04	X_{11}	1
0x05	X_{12}	1
0x06	X_{21}	1
0x07	X_{22}	1
⋮	⋮	⋮
0x1C	X_{11}	7
0x1D	X_{12}	7
0x1E	X_{21}	7
0x1F	X_{22}	7

`fName.itr` - a text file with the input values of all matrices and the computed results for each iteration the algorithm to determine each matrix determinant, its average and identify the matrices with lower and higher determinant. And considering a correct fix point representation on all the intermediate computations/results.
You can use this file to verify your simulation results.

If yout want to generate valies using a specific seed for the random number, replace the 0 with the seed number. For example:

```
./adet.exe 1385118182 fName
```

2 Comparing/verifying FPGA results

```
./adet.exe fName
```

When the program is executed with only one name parameter, it is expecting that following two files exist on the current directory:

`fName.dat` - the file that was previously generated with the values used to initialize the input memory on the FPGA.

`fName.out` - the file with 2048 bytes that was read (uploaded) from the FPGA output memory using USB cable. This will be used to check the values generated on the FPGA. The organization of the output memory assumed by the program consider that each result value is represented using 32bits (Q14.18). The following memory organization is assumed (considering the address space of the 8bit port of the output memory):

Address	Content (32bits)	Matrix
0x00	$detR_0[07:00]$	0
0x01	$detR_0[15:08]$	0
0x02	$detR_0[23:16]$	0
0x03	$detR_0[31:24]$	0
0x04	$detI_1[07:00]$	0
0x05	$detI_1[15:08]$	0
0x06	$detI_1[23:16]$	0
0x07	$detI_1[31:24]$	0
0x08	$detR_1[07:00]$	1
0x09	$detR_1[15:08]$	1
⋮	⋮	⋮
0x3A	$detR_7[23:16]$	7
0x3B	$detR_7[31:24]$	7
0x3C	$detI_7[07:00]$	7
0x3D	$detI_7[15:08]$	7
0x3E	$detI_7[23:16]$	7
0x3F	$detI_7[31:24]$	7
0x40	$averageDetR[07:00]$	
0x41	$averageDetR[15:08]$	
0x42	$averageDetR[23:16]$	
0x43	$averageDetR[31:24]$	
0x44	$averageDetI[07:00]$	
0x45	$averageDetI[15:08]$	
0x46	$averageDetI[23:16]$	
0x47	$averageDetI[31:24]$	

The output of the `adet` program in this situation will be the expected determinant value, the determinant value read from the FPGA memory (uploaded file) and the solutions difference/error. The program also show the same information for the average determinant and which matrices should be identified with lower and higher 1-norm determinant.

Optional two parameters numbers (Qi and Qf) can be added at the end of the command line. They defined the QI.F fix-point format to be used when converting the data read from the FPGA. Note that since the result must fit on 32 bits, the following restriction applies: Qi + Qf = 32 bits (default values are: Qi=14 Qf=18)

3 Reading data from the PFGA/Board

To read the data form the board/FPGA using the UART interface via the USB cable you need to have a serial term with file writing capabilities. Known working serial terminal with writing capabilities are:

Op. System	Terminal	Location
Windows	Tera Term	https://ttssh2.osdn.jp/index.html.en
Linux	CuteCom	http://cutecom.sourceforge.net
Linux	GTKTerm	https://github.com/Jeija/gtkterm

This terminals should be configured with the following values:

Parameter = Value
Baud Rate = 9600
Parity = none
Data bits = 8
Stopbits = 1
Flow Control = none

4 Final Notes

Students are advised to NOT CHANGE ANY OF THE SOFTWARE/HARDWARE, made available by the teacher to support the project development, until a complete working project on the board have been developed and validated.

The adet program can be used as it is, or it may be changed if other memory organization is used in the input memory, output memory or both. In this situation the new program should be submitted with the VHDL code on the Fenix.

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