HT MICRON
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iMCP HTLRBL32L - Product Specification

Data Brief for the HT Micron LoRaWAN® + Bluetooth® Low Energy System-in-Package

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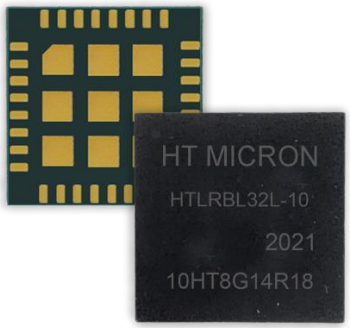
SUMMARY

1. PRODUCT OVERVIEW

iMCP – HTLRBL32L is a highly compact and low-power wireless communication device featuring LoRa® and Bluetooth® Low Energy capabilities. In a tiny 13x13x1.1 mm package it allows easy development of solutions for both long and short ranges, whilst requiring minimum power consumption enabling years-long battery life applications. The product integrates an ST Microelectronics BlueNRG SoC (ARM Cortex M0+ with Bluetooth® Low Energy radio) and a Semtech RF transceiver, with a full set of interfaces for analog and digital peripherals and ready for multi-region LoRaWAN® applications and wireless firmware update capability using Bluetooth® Low Energy 5.2.

FEATURES

- LoRaWAN® compliant
- Bluetooth® Low Energy 5.2 compliant
- 32-bit ARM Cortex M0+ up to 64MHz
- 256 KB flash
- 64 KB RAM
- 7 KB ROM
- Single power supply: 2.7 V to 3.6 V
- Operating temperature range: -20°C to +75°C
- LoRaWAN® frequency range: 433-960 MHz
- Bluetooth® Low Energy frequency range: 2400-2483.5 MHz
- Embedded 32 MHz crystals for LoRa® and Bluetooth® LE chipsets
- *LoRa® TX output power: +20.5 dBm
- *LoRa® RX sensitivity: -137 dBm
- *Bluetooth® LE TX output power: +6 dBm
- *Bluetooth® LE RX sensitivity level: -93 dBm @ 1 Mbps
- * Power consumption: 1uA (Sleep with RAM retained)
- Dimensions: 13x13x1.1 LGA – 32 pins
- Part number: HTLRBL32L-00
- LoRaWAN® Frequency plans:
  - EU863-870
  - US902-928
  - AU915-928
  - AS923
  - KR920-923
  - IN865-867
  - RU864-870
- Modulation schemes (Semtech RF Transceiver):
  - FSK, GFSK, MSK, GMSK and LoRa®



INTERFACES

- 1x DMA controller with 8 channels supporting ADC, SPI, I2C, USART and LPUART
- 1x SPI/I2S
- 1x I2C (SMBus/PMBus)
- 1x PDM (digital microphone interface)
- 1x LPUART
- 1x USART (ISO 7816 smartcard mode, IrDA, SPI Master and Modbus)
- 1x independent WDG
- 1x real time clock (RTC)
- 1x independent SysTick
- 1x 16-bit, 6 channel advanced timer
- Up to 32 fast I/Os: 28 of them with wake-up capability; 31 of them 5 V tolerant
- 12-bit ADC with 6 input channels, up to 16 bits with a decimation filter
- Battery monitoring
- Analog watchdog
- Analog Mic I/F with PGA

APPLICATIONS

- Smart Agriculture
- Smart buildings
- Smart cities
- Smart industry
- Smart logistics
- Smart utilities

*First prototype's performances. Working on improvements.

2. SYSTEM ARCHITECTURE

2.1. Block Diagram

The overall system is composed by the BlueNRG-355VC, by the SX1262 LoRaWAN® transceiver, 32MHz crystals and a hardware security module for the LoRa® messages, and there are RF paths designed to provide the appropriated load conditions to met the product's performance requirements. Figure 1 – iMCP HTLRBL32L System Block Diagram shows the block diagram of iMCP HTLRBL32L system architecture.

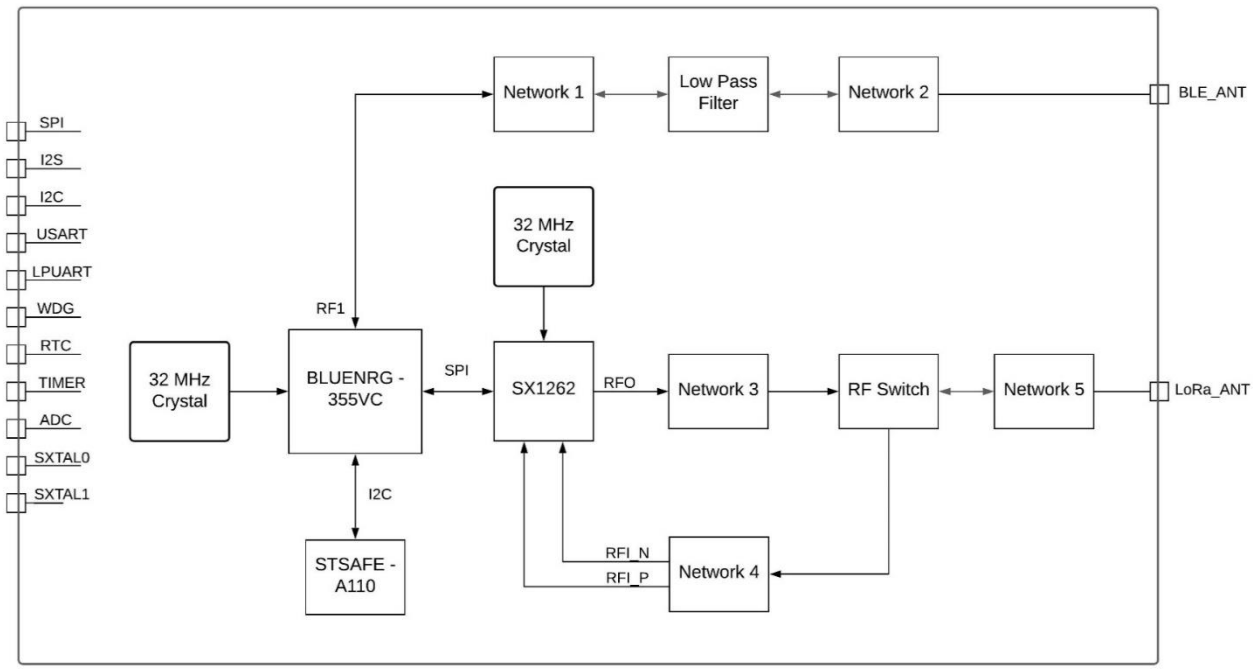


Figure 1 – iMCP HTLRBL32L System Block Diagram

2.2. BlueNRG-355VC

The BlueNRG-355VC is an ultra-low power programmable Bluetooth® Low Energy wireless SoC solution and it embeds a Cortex®-M0+ microcontroller that can operate up to 64MHz. The BlueNRG-355VC's radio transceiver is compliant with Bluetooth® Low Energy SIG core specification version 5.2 addressing point-to-point connectivity and Bluetooth® LE Mesh networking and allows large-scale device networks to be established in a reliable way. The BlueNRG-355VC is also suitable for 2.4 GHz proprietary radio wireless communication to address ultra-low latency applications.

2.3. SX1262

The SX1262 sub-GHz radio transceiver is ideal for long range wireless applications. The device is designed for long battery life with just 4.2 mA of active receive current consumption. The SX1262 can transmit up to +22 dBm with highly efficient integrated power amplifier. It supports LoRa® modulation for LPWAN use cases and (G)FSK modulation for legacy use cases. The device is highly configurable to meet different application requirements

utilizing the global LoRaWAN® standard or proprietary protocols. It is designed to comply with the physical layer requirements of the LoRaWAN® specification released by the LoRa Alliance®.

2.4. STSAFE-A110

The STSAFE-A110 is a highly secure solution that acts as a secure element providing authentication and secure data management services to a local or remote host. It consists of a full turnkey solution with a secure operating system running on the latest generation of secure microcontrollers.

3. SUMMARY OF PRODUCT SPECIFICATIONS

Part Number	HTLRBL32L
Operation Zones	EU863-870, US902-928, AU915-928, AS923, KR920-923, IN865-867, RU864-870
Package	LGA 32
LoRa® Transceiver	Semtech SX1262
MCU with integrated Bluetooth® LE Transceiver	STMicroelectronics BlueNRG-355VC
Memory	256 KB flash (for app code + stack)
GPIO	20 pins
Communication Interfaces	1x USART, 1x LPUART, 1x I2C, 1x SPI, 1x I2S
ADC	5x (12 bits)
Input Voltage	2.7 ~ 3.6 V
*LoRa® Max. TX Output Power	20.5dBm
*LoRa® RX Sensitivity Level	-137dBm
*Bluetooth® LE Max. TX Output Power	6dBm
*Bluetooth® LE RX Sensitivity Level	-93dBm
*Sleep Mode Consumption	1uA
*LoRa® Consumption @Max. TX Output Power	130mA
*LoRa® Consumption @RX Sensitivity Level	6.6mA
*Bluetooth® LE Consumption @Max. TX Output Power	6.4mA
*Bluetooth® LE Consumption @RX Sensitivity Level	6.5mA
Dimensions	13x13x1.1

*First prototype's performances. Working on improvements.

4. PACKAGE OUTLINE

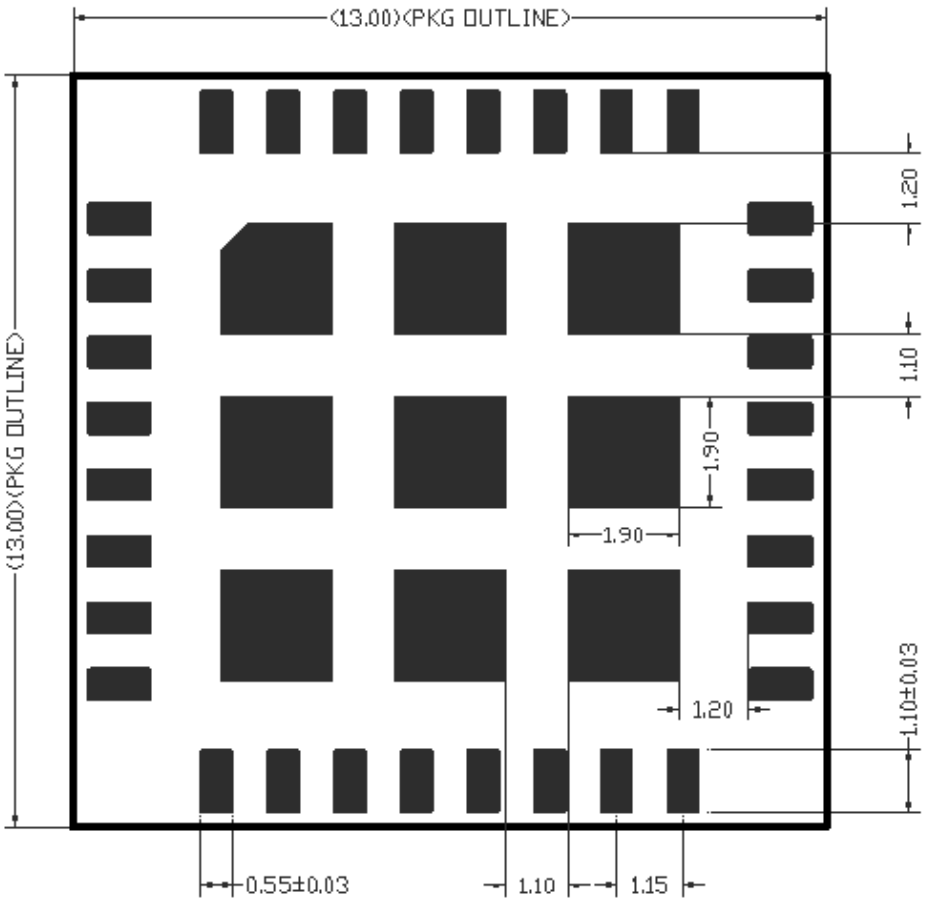


Figure 2. SiP Package Outline - TOP View

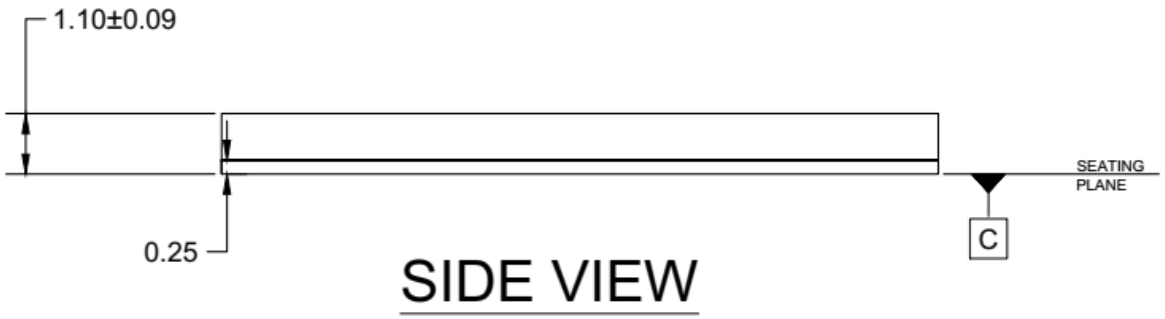


Figure 3. SiP Package Outline – Side View

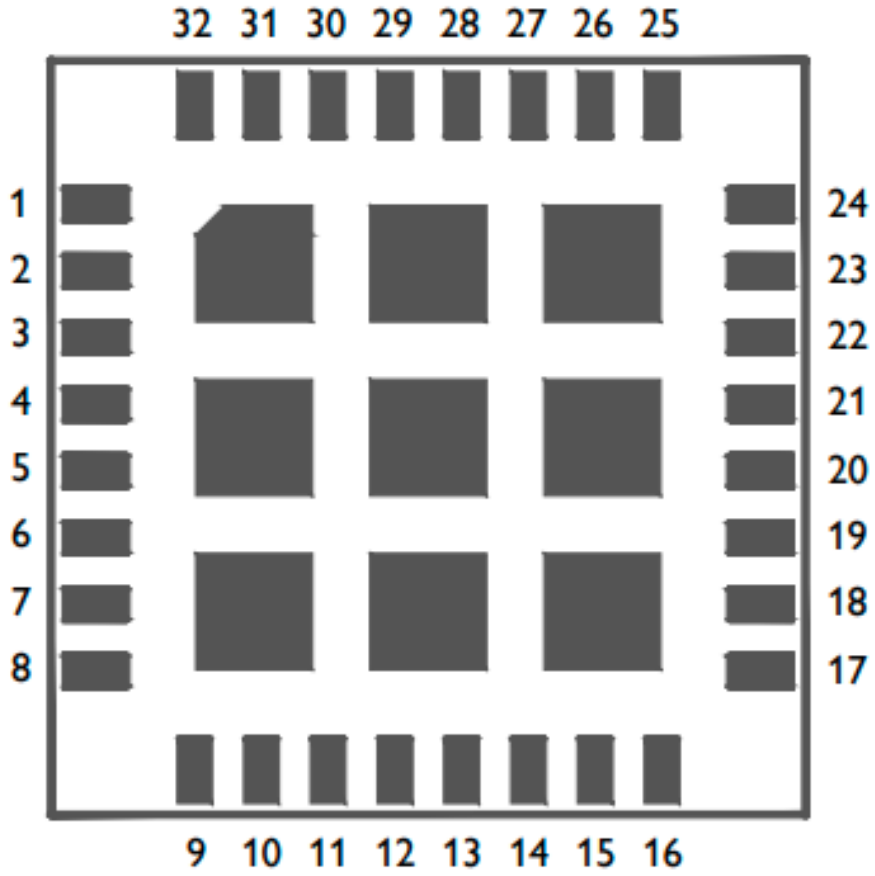


Figure 4. SiP Pinout – TOP View

5. PINOUT AND PIN DESCRIPTION

Table 1. iMCP HTLRBL32L-10 Pinout

Number	Symbol	Pin name	Description
1	BLE_ANT	Bluetooth® LE ANTENNA	Bluetooth® Low Energy RF input and output signal
2	GND	GND	Exposed pad connected to the ground of the application board
3	MCU-PA3	SWCLK	Serial Wire Debug clock output (SWD)
		USART_RTS_DE	RTS Flow Control (USART)
		TIM_BKIN2	Timer Break Input
		SPI3_SCK	Serial Clock (SPI)
		TIM1_CH6	Timer Channel
		I2S3_SCK	Continuous Serial Clock (I2S)
		Wake Up	External Wake Up Input
4	MCU-PA2	SWDIO	Serial Wire Debug Input/Output
		USART_CK	Clock line (USART)
		TIM_BKIN	Timer Break Input
		SPI3_MCK	Master Clock (SPI)
		TIM1_CH5	Timer Channel
		I2S3_MCK	Master Clock (I2S)

		Wake Up	External Wake Up Input
5	MCU-PA8	USART_RX	Receiver input (USART)
		SPI1_MOSI	Master Out Slave In (SPI)
		RX_SEQUENCE	RX Activity Alert
		SPI3_MISO	Master In Slave Out (SPI)
		TIM1_CH3	Timer Channel
		I2S3_MISO	Master In Slave Out (I2S)
		Wake Up	External Wake Up Input
		RTC_OUT	Real Time Clock Output
6	MCU-PA9	USART_TX	Transmitter Output (USART)
		SPI1_SCK	Serial Clock (SPI)
		RTC_OUT	Real Time Clock Output
		SPI3_NSS	Slave Select (SPI)
		TIM1_CH4	Timer Channel
		I2S3_WS	Word Select (I2S)
		Wake Up	External Wake Up Input
		LCO	Low Speed Clock Output
7	MCU-PB0	*	*
8	GND	GND	Exposed pad connected to the ground of the application board
9	LoRa_ANT	LoRa® ANTENNA	LoRa® input and output signal
10	GND	GND	Exposed pad connected to the ground of the application board
11	MCU-PB2	USART_RTS_DE	RTS Flow Control (USART)
		PDM_DATA	Data Line (Digital Microphone Interface)
		TIM1_CH3	Timer Channel
		ADC_VINM0	ADC external input M0
		Wake Up	External Wake Up Input
12	RSTN	RSTN	Reset
13	MCU-PB5	LPUART_RX	Receiver Input (LPUART)
		SPI2_MOSI	Master Out Slave In (SPI)
		PDM_CLK	Clock Line (Digital Microphone Interface)
		I2S2_SD	Serial Data (I2C)
		Wake Up	External Wake Up Input
14	MCU-PB1	SPI1_NSS	Slave Select (SPI)
		PDM_CLK	Clock Line (Digital Microphone Interface)
		TIM1_ETR	External Timer Reference
		ADC_VINP1	ADC external input P1
		Wake Up	External Wake Up Input
15	MCU-PB3	USART_CTS	CTS Flow Control (USART)
		LPUART_TX	Transmitter output (LPUART)
		TIM1_CH4	Timer Channel
		ADC_VINP0	ADC external input P0
		Wake Up	External Wake Up Input
16	GND	GND	Exposed pad connected to the ground of the application board
17	GND	GND	Exposed pad connected to the ground of the application board
18	MCU-PB6	I2C2_SCL	Serial Clock (I2S)
		SPI2_NSS	Slave Select (SPI)
		LPUART_TX	Transmitter output (LPUART)
		TIM1_CH1	Timer Channel
		I2S2_WS	Word Select (I2S)
		Wake Up	External Wake Up Input

19	MCU-PB7	I2C2_SDA	Serial Data (I2C)
		SPI2_SCK	Serial Clock (SPI)
		LPUART_RX	Receiver Input (LPUART)
		TIM1_CH2	Timer Channel
		I2S2_SCK	Serial Clock (I2S)
		Wake Up	External Wake Up Input
20	VDD3V3	VDD3V3	3.3 V power supply
21	MCU-PB9	USART_TX	Transmitter output (USART)
		LPUART_CTS	CTS Flow Control (LPUART)
		SPI2_MCK	Master Clock (SPI)
		TIM1_CH1N	Timer Channel
		TIM1_CH2N	Timer Channel
		I2S2_MCK	Master Clock (I2S)
		Wake Up	External Wake Up Input
22	MCU-PB12	SPI1_SCK	Serial Clock (SPI)
		LCO	Low Speed Clock Output
		PDM_DATA	Data Line (Digital Microphone Interface)
		TIM1_BKIN	Timer Break Input
		TIM1_CH3	Timer Channel
		SXTAL0	External clock source pin
23	MCU-PB13	SPI1_MISO	Master In Slave Out (SPI)
		I2C2_SCL	Serial Clock (I2C)
		PDM_CLK	Clock Line (Digital Microphone Interface)
		TIM1_BKIN2	Timer Break Input
		TIM1_CH4	Timer Channel
		SXTAL1	External clock source pin
24	GND	GND	Exposed pad connected to the ground of the application board
25	MCU-PA15	I2C2_SMBA	System Management Bus Alert (I2C)
		SPI1_MOSI	Master Out Slave In (SPI)
		TIM1_BKIN2	Timer Break Input
		ADC_VINP2	ADC external input P2
		Wake Up	External Wake Up Input
26	MCU-PA12	I2C1_SMBA	System Management Bus Alert (I2C)
		SPI1_NSS	Slave Select (SPI)
		SPI2_MOSI	Master Out Slave In (SPI)
		TIM1_CH1	Timer Channel
		I2S2_SD	Serial Data (I2C)
		ADC_VINM3	ADC external input M3
		Wake Up	External Wake Up Input
27	MCU-PA4	LCO	Low Speed Clock Output
		SPI2_NSS	Slave Select (SPI)
		LPUART_TX	Transmitter output (LPUART)
		TIM1_CH1	Timer Channel
		I2S2_WS	Word Select (I2S)
		Wake Up	External Wake Up Input
28	MCU-PA10	LCO	Low Speed Clock Output
		SPI1_MISO	Master In Slave Out (SPI)
		TX_SEQUENCE	TX Activity Alert
		SPI3_MCK	Master Clock (SPI)
		TIM1_CH5	Timer Channel

		I2S3_MCK	Master Clock (I2S)
		BOOT	Bootloader activation
		Wake Up	External Wake Up Input
29	MCU-PA7	LPUART_RTS_DE	RTS Flow Control (LPUART)
		SPI2_MISO	Master In Slave Out (SPI)
		SPI2_SCK	Serial Clock (SPI)
		TIM1_CH2	Timer Channel
		I2S2_MISO	Master In Slave Out (I2S)
		I2S2_SCK	Serial Clock (I2S)
		Wake Up	External Wake Up Input
		RTC_OUT	Real Time Clock Output
30	GND	GND	Exposed pad connected to the ground of the application board
31	MCU-PA5	MCO	High Speed Clock Output
		SPI2_SCK	Serial Clock (SPI)
		LPUART_RX	Receiver Input (LPUART)
		TIM1_CH2	Timer Channel
		I2S2_SCK	Serial Clock (I2S)
		Wake Up	External Wake Up Input
		LCO	Low Speed Clock Output
32	GND	GND	Exposed pad connected to the ground of the application board

REVISION HISTORY

Date	Version	Changes	Remark
05/23/2022	01	- Initial draft	
06/24/2022	02	- Added prototype v0 performances, system block diagram and core components brief descriptions	

CONTACT

HT MICRON SEMICONDUTORES S.A.
Av. Unisinos, 1550 | 93022-750 | São Leopoldo | RS | Brasil
support_iot@htmicron.com.br
www.htmicron.com.br

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