Projet RISC-V Zynq

Réunion de projet 5

Tâches effectuées

02/01/2024

- Installation de Vivado 2023.2 avec le support des boards ZYBO.

- Ajout des boards files contenant la Zybo Z7-20

03/01/2024

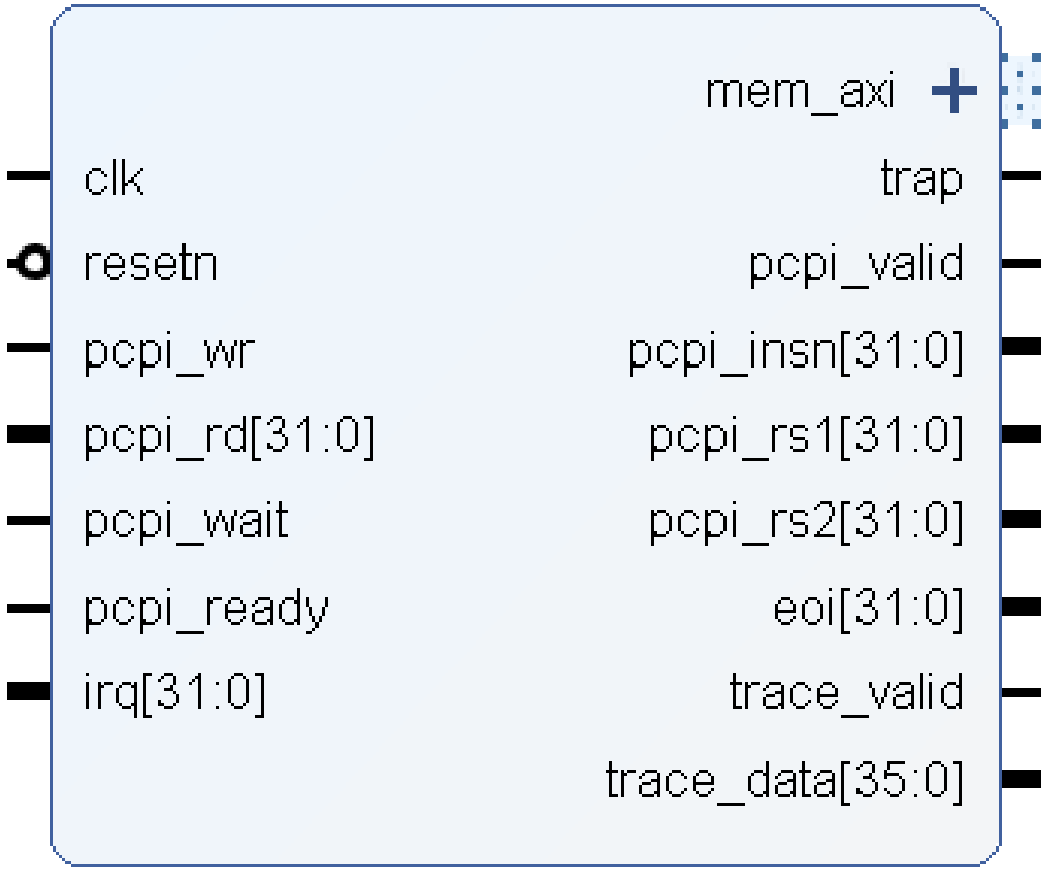
- Creation d'un projet vivado, packaging de l'IP picorv32_axi_0 et création d'un premier bloc design

04/01/2024
- Recherches sur l'IP du ZYNQ, comment connecter le picorv32 à la mémoire du processeur

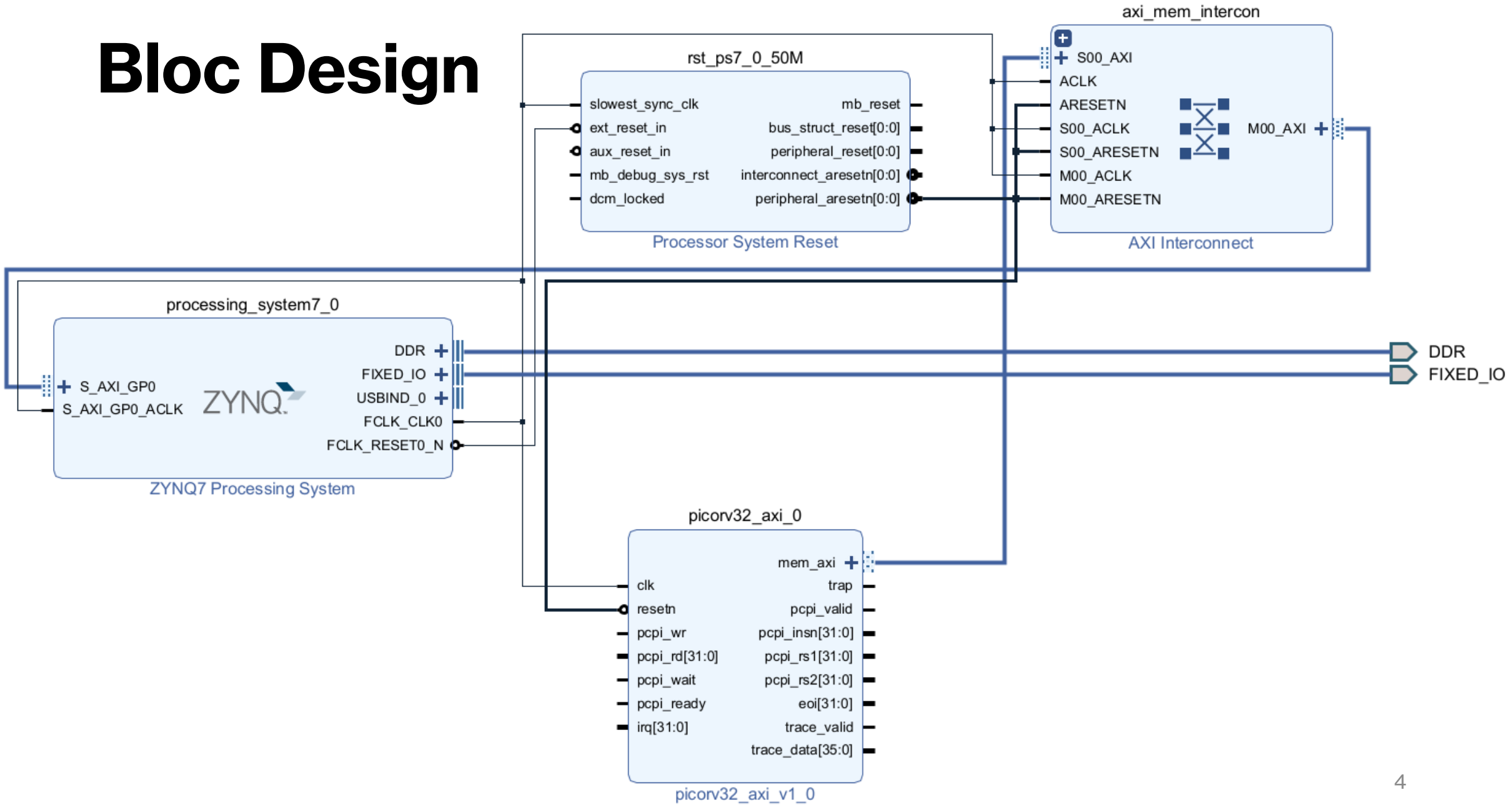
11/01/24
- Réunion de projet
- Découpe en tache :
    - Recherche AXI : Guicheteau
    - Recherche PCPI, si on désactive : Assier
    - Recherche Systeme : MORAL
- Install Vivado : Guicheteau

12/01/24 - 13/01/24
- Modification des PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY
- Modification des connexions entre l'axi interconnect et rst_ps7_0_50M
- Implémentation

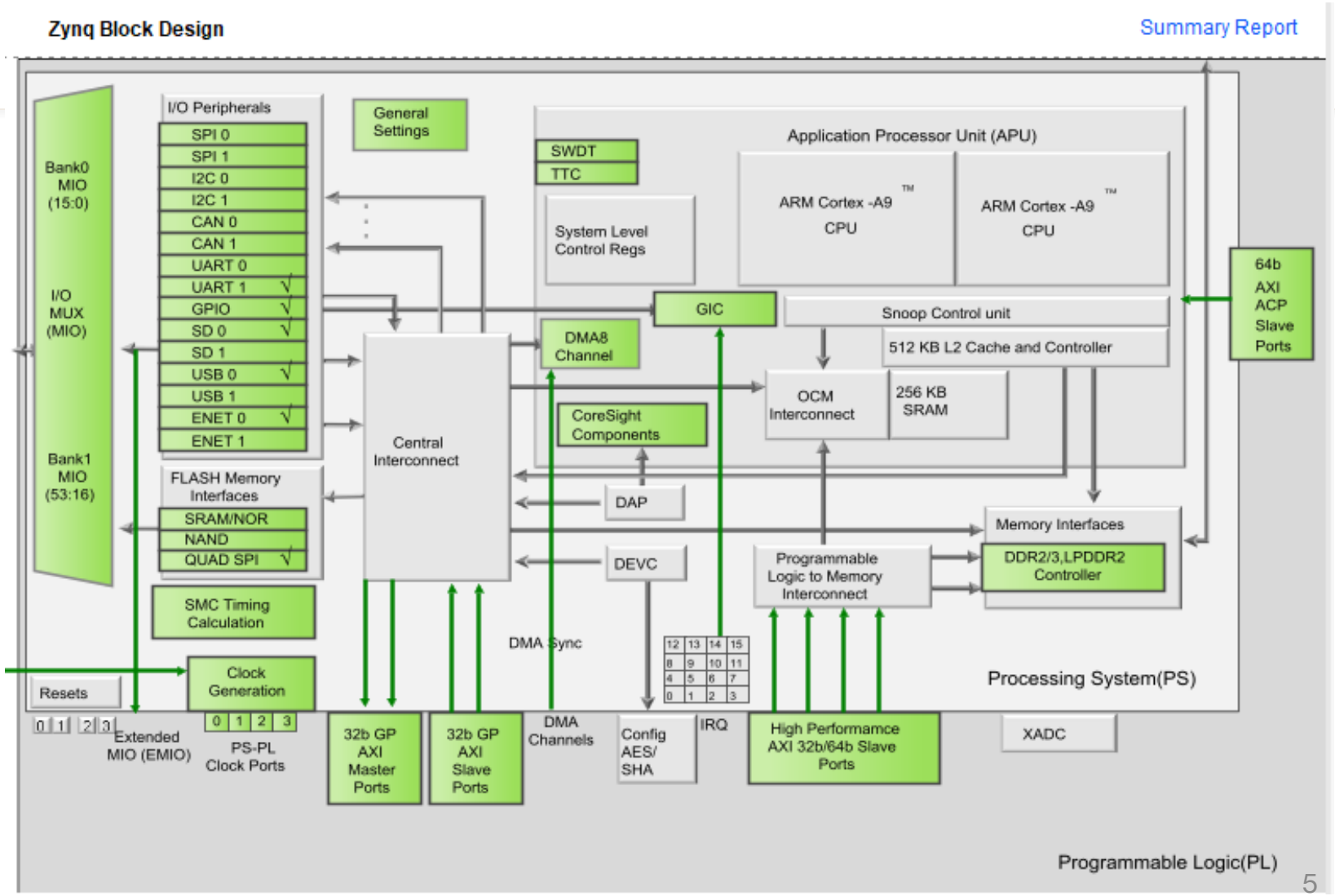
IP PicoRV32 AXI



Bloc Design


axi_mem_intercon
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
rst_ps7_0_50M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
processing_system7_0
S_AXI_GP0
S_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
USBIND_0
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
DDR
FIXED_IO
picorv32_axi_0
clk
resetn
pcpi_wr
pcpi_rd[31:0]
pcpi_wait
pcpi_ready
irq[31:0]
mem_axi
trap
pcpi_valid
pcpi_insn[31:0]
pcpi_rs1[31:0]
pcpi_rs2[31:0]
eoi[31:0]
trace_valid
trace_data[35:0]
picorv32_axi_v1_0

ZYNQ7 Processing System



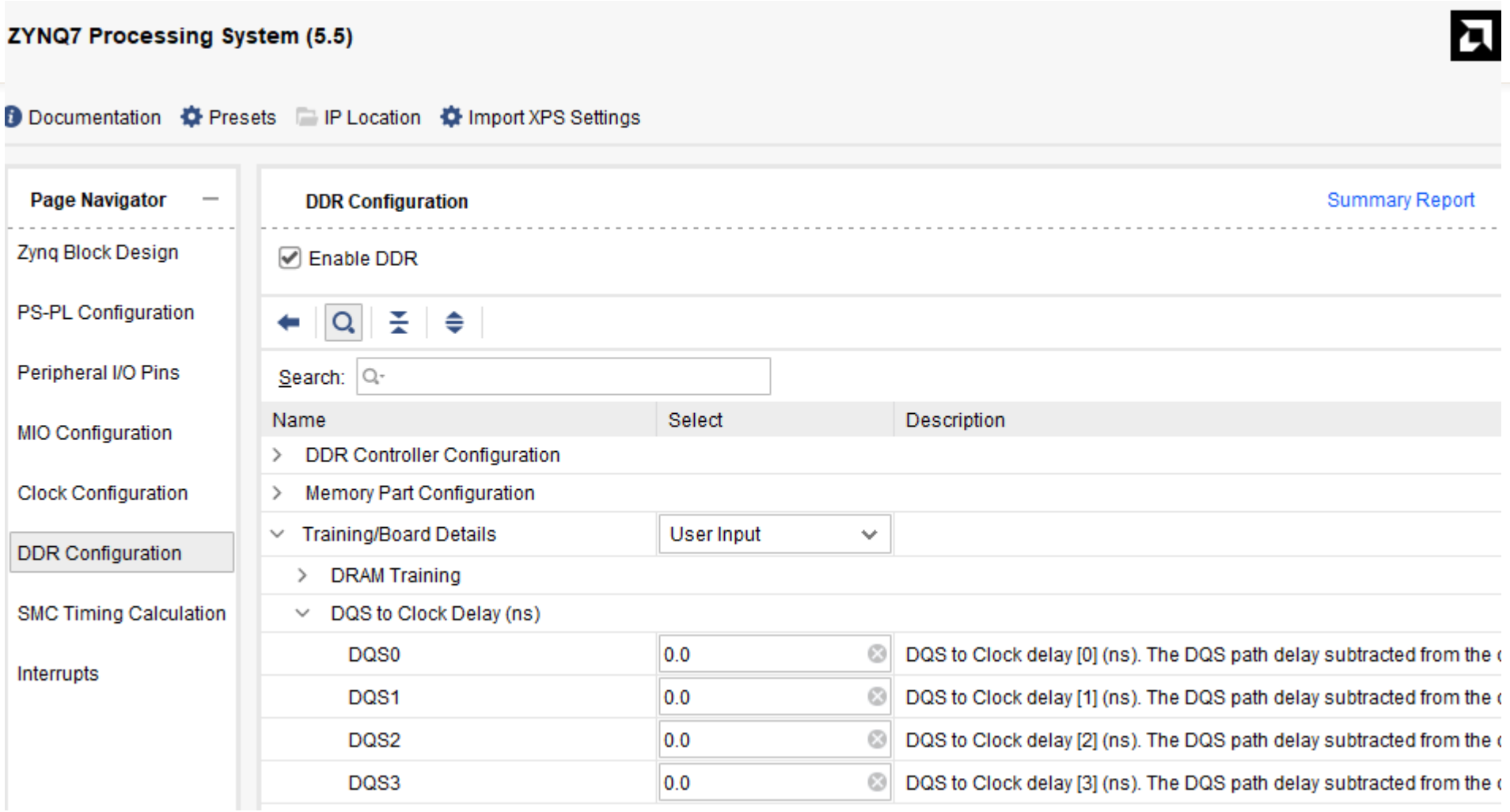
Problèmes rencontrés

- Les DDR sont des mémoires vives qui transfèrent des données rapidement, et les DQS sont des signaux d'horloge qui aident à synchroniser la transmission de ces données.

DDR TO CLK DELAY

```
CRITICAL WARNING: [PSU-1] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_0 has negative value -0.050 .
PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [PSU-2] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_1 has negative value -0.044 .
PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [PSU-3] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_2 has negative value -0.035 .
PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [PSU-4] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_3 has negative value -0.100 .
PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [PSU-1] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_0 has negative value -0.050 .
PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [PSU-2] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_1 has negative value -0.044 .
PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [PSU-3] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_2 has negative value -0.035 .
PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [PSU-4] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_3 has negative value -0.100 .
PS DDR interfaces might fail when entering negative DQS skew values.
```

Problèmes rencontrés



Problèmes rencontrés

Reset Source

```
[BD 41-1347] Reset pin /picorv32_axi_0/resetn (associated clock /picorv32_axi_0/clk) is connected to
asynchronous reset source /processing_system7_0/FCLK_RESET0_N.
This may prevent design from meeting timing. Instead it should be connected to reset source
/rst_ps7_0_50M/peripheral_aresetn.

[BD 41-1347] Reset pin /axi_mem_intercon/M00_ARESETN (associated clock /axi_mem_intercon/M00_ACLK) is
connected to asynchronous reset source /processing_system7_0/FCLK_RESET0_N.
This may prevent design from meeting timing. Instead it should be connected to reset source
/rst_ps7_0_50M/peripheral_aresetn.

[BD 41-1347] Reset pin /picorv32_axi_0/resetn (associated clock /picorv32_axi_0/clk) is connected to
asynchronous reset source /processing_system7_0/FCLK_RESET0_N.
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connected to asynchronous reset source /processing_system7_0/FCLK_RESET0_N.
This may prevent design from meeting timing. Instead it should be connected to reset source
/rst_ps7_0_50M/peripheral_aresetn.
```

Problèmes rencontrés

AVANT :
* processing_system7_0/FCLK_RESET0_N -> rst_ps7_0_50M/ext_reset_in
* processing_system7_0/FCLK_RESET0_N -> picorv32_axi_0/resetn
* processing_system7_0/FCLK_RESET0_N -> axi_mem_intercon/M00_ARESETN
* rst_ps7_0_50M/peripheral_aresetn -> axi_mem_intercon/ARESETN
* rst_ps7_0_50M/peripheral_aresetn -> axi_mem_intercon/S00_ARESETN

APRES :
* processing_system7_0/FCLK_RESET0_N -> rst_ps7_0_50M/ext_reset_in
* rst_ps7_0_50M/peripheral_aresetn -> picorv32_axi_0/resetn
* rst_ps7_0_50M/peripheral_aresetn -> axi_mem_intercon/ARESETN
* rst_ps7_0_50M/peripheral_aresetn -> axi_mem_intercon/S00_ARESETN
* rst_ps7_0_50M/peripheral_aresetn -> axi_mem_intercon/M00_ARESETN

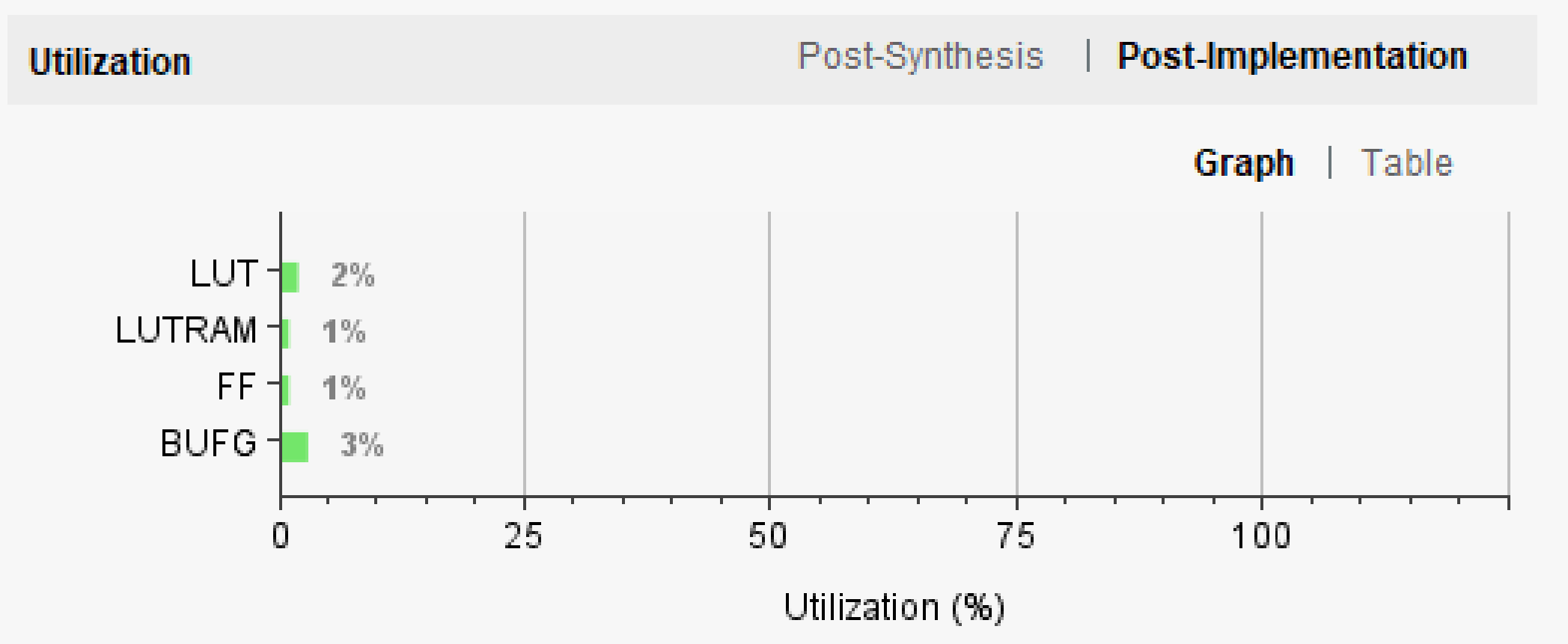
Problèmes rencontrés

PCPI

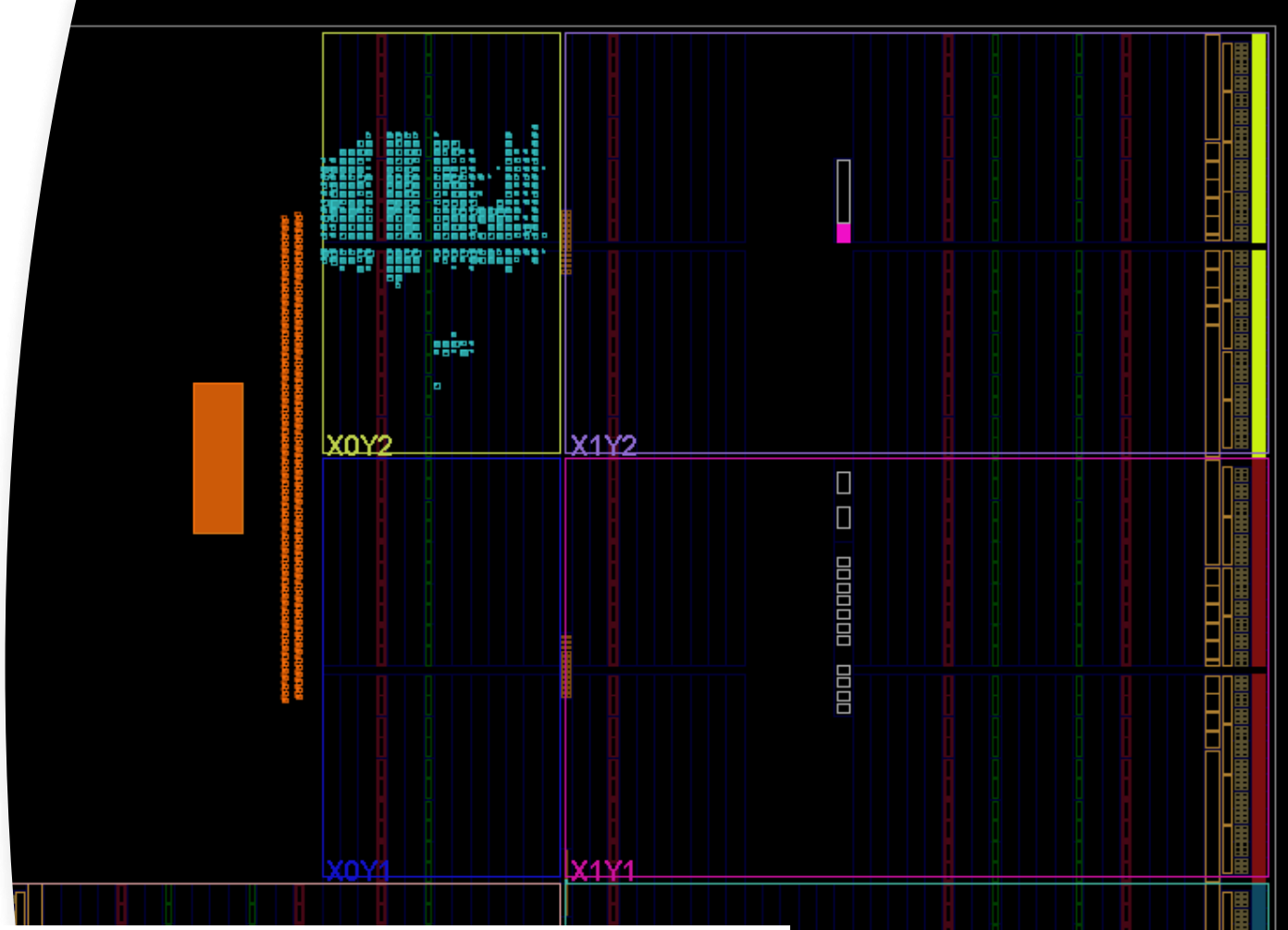
```
 [BD 41-759] The input pins (listed below) are either not connected or do not have a source port, and they don't have a tie-off specified. These pins are tied-off to all 0's to avoid error in Implementation flow.
Please check your design and connect them as needed:
/picorv32_axi_0/pcpi_wr
/picorv32_axi_0/pcpi_rd
/picorv32_axi_0/pcpi_wait
/picorv32_axi_0/pcpi_ready
/picorv32_axi_0/irq
```

Résultats première implémentation

Confirmation par l'implémentation le picorv32 correspond bien au projet



Résultats première implémentation

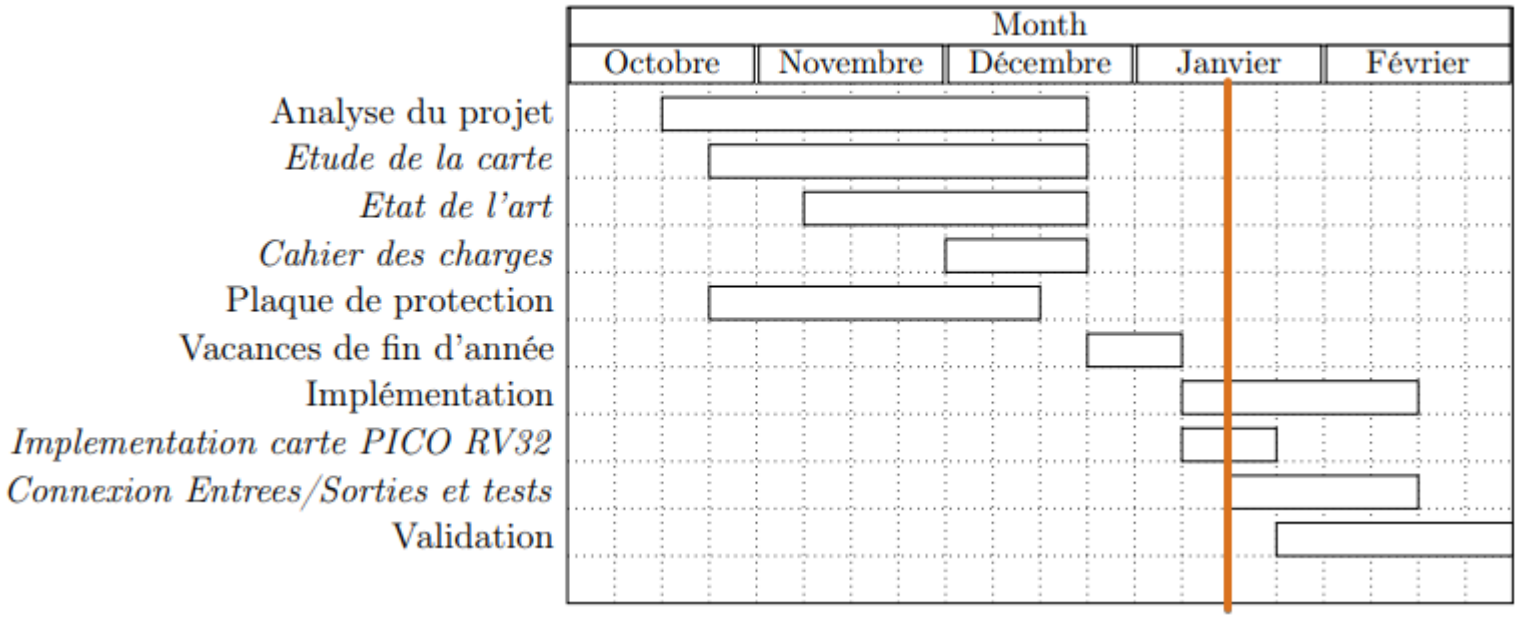


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	11,371 ns	Worst Hold Slack (WHS):	0,120 ns	Worst Pulse Width Slack (WPWS):	8,750 ns
Total Negative Slack (TNS):	0,000 ns	Total Hold Slack (THS):	0,000 ns	Total Pulse Width Negative Slack (TPWS):	0,000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1983	Total Number of Endpoints:	1983	Total Number of Endpoints:	702

All user specified timing constraints are met.

Gantt



- Comme prévu, la première semaine est surtout dédiée à implémenter le pico sur la carte