ADD Addition ADD

Syntax ADD A,src e.g. ADD A,#%11001010

Operation A <= A+ src

Description The source byte is added to the contents of the accumulator and the result is stored in the accumulator. The source is a memory or data byte.

Instruction overview

mnem	dst	src	Affected condition flags						
			V	I1	H	I0	N	Z	C
ADD	A	Mem	V	-	H	-	N	Z	C

V ⇒ $(A7.M7 + M7.\overline{R7} + \overline{R7}.A7) \oplus (A6.M6 + M6.\overline{R6} + \overline{R6}.A6)$
Set if the signed operation generates an overflow, cleared otherwise.

H ⇒ $A3.M3 + M3.\overline{R3} + \overline{R3}.A3$
Set if a carry occurred from bit 3 of the result, cleared otherwise.

N ⇒ R7
Set if bit 7 of the result is set (negative value), cleared otherwise.

Z ⇒ $\overline{R7}.\overline{R6}.\overline{R5}.\overline{R4}.\overline{R3}.\overline{R2}.\overline{R1}.\overline{R0}$
Set if the result is zero (0x00), cleared otherwise.

C ⇒ $A7.M7 + M7.\overline{R7} + \overline{R7}.A7$
Set if a carry occurred from bit 7 of the result, cleared otherwise.

Detailed description

dst	src	Asm	cy	lgth	Op-code(s)					ST7
A	#byte	ADD A,#$55	1	2		AB	XX			✗
A	shortmem	ADD A,$10	1	2		BB	XX			✗
A	longmem	ADD A,$1000	1	3		CB	MS	LS		✗
A	(X)	ADD A,(X)	1	1		FB				✗
A	(shortoff,X)	ADD A,($10,X)	1	2		EB	XX			✗
A	(longoff,X)	ADD A,($1000,X)	1	3		DB	MS	LS		✗
A	(Y)	ADD A,(Y)	1	2	90	FB				✗
A	(shortoff,Y)	ADD A,($10,Y)	1	3	90	EB	XX			✗
A	(longoff,Y)	ADD A,($1000,Y)	1	4	90	DB	MS	LS		✗
A	(shortoff,SP)	ADD A,($10,SP)	1	2		1B	XX			
A	[shortptr.w]	ADD A,[$10.w]	4	3	92	CB	XX			✗
A	[longptr.w]	ADD A,[$1000.w]	4	4	72	CB	MS	LS		
A	([shortptr.w],X)	ADD A,([$10.w],X)	4	3	92	DB	XX			✗
A	([longptr.w],X)	ADD A,([$1000.w],X)	4	4	72	DB	MS	LS		
A	([shortptr.w],Y)	ADD A,([$10.w],Y)	4	3	91	DB	XX			✗

See also: ADDW, ADC, SUB, SBC, MUL, DIV

LD Load LD

Syntax LD dst,src e.g. LD A,#$15

Operation dst <= src

Description Load the destination byte with the source byte. The dst and src can be a register, a byte (low/high) of an index register or a memory/data byte. When half of an index register is loaded, the other half remains unchanged.

Instruction overview

mnem	dst	src	Affected condition flags						
			V	I1	H	I0	N	Z	C
LD	Reg	Mem	-	-	-	-	N	Z	-
LD	Mem	Reg	-	-	-	-	N	Z	-
LD	Reg	Reg	-	-	-	-	-	-	-

N ⇒ R7
Set if bit 7 of the result is set (negative value), cleared otherwise.

Z ⇒ $\overline{R7}.\overline{R6}.\overline{R5}.\overline{R4}.\overline{R3}.\overline{R2}.\overline{R1}.\overline{R0}$
Set if the result is zero (0x00), cleared otherwise.

Detailed description

dst	src	Asm	cy	lgth	Op-code(s)					ST7
A	#byte	LD A,#$55	1	2		A6	XX			✗
A	shortmem	LD A,$50	1	2		B6	XX			✗
A	longmem	LD A,$5000	1	3		C6	MS	LS		✗
A	(X)	LD A,(X)	1	1		F6				✗
A	(shortoff,X)	LD A,($50,X)	1	2		E6	XX			✗
A	(longoff,X)	LD A,($5000,X)	1	3		D6	MS	LS		✗
A	(Y)	LD A,(Y)	1	2	90	F6				✗
A	(shortoff,Y)	LD A,($50,Y)	1	3	90	E6	XX			✗
A	(longoff,Y)	LD A,($5000,Y)	1	4	90	D6	MS	LS		✗
A	(shortoff,SP)	LD A,($50,SP)	1	2		7B	XX			
A	[shortptr.w]	LD A,[$50.w]	4	3	92	C6	XX			✗
A	[longptr.w]	LD A,[$5000.w]	4	4	72	C6	MS	LS		
A	([shortptr.w],X)	LD A,([$50.w],X)	4	3	92	D6	XX			✗
A	([longptr.w],X)	LD A,([$5000.w],X)	4	4	72	D6	MS	LS		
A	([shortptr.w],Y)	LD A,([$50.w],Y)	4	3	91	D6	XX			✗

CLR Clear CLR

Syntax CLR dst e.g. CLR A

Operation dst <= 00

Description The destination byte is forced to 00 value. The destination is either a memory byte location or the accumulator. This instruction is compact, and does not affect any register when used with RAM variables.

Instruction overview

mnem	dst	Affected condition flags						
		V	I1	H	I0	N	Z	C
CLR	Mem	-	-	-	-	0	1	-
CLR	A					0	1	

N: 0

Cleared

Z: 1

Set

Detailed description

dst	Asm	cy	lgth	Op-code(s)					ST7
A	CLR A	1	1		4F				✗
shortmem	CLR $10	1	2		3F	XX			✗
longmem	CLR $1000	1	4	72	5F	MS	LS		
(X)	CLR (X)	1	1		7F				✗
(shortoff.X)	CLR ($10,X)	1	2		6F	XX			✗
(longoff,X)	CLR ($1000,X)	1	4	72	4F	MS	LS		
(Y)	CLR (Y)	1	2	90	7F				✗
(shortoff,Y)	CLR ($10,Y)	1	3	90	6F	XX			✗
(longoff,Y)	CLR ($1000,Y)	1	4	90	4F	MS	LS		
(shortoff,SP)	CLR ($10,SP)	1	2		0F	XX			
[shortptr.w]	CLR [$10]	4	3	92	3F	XX			✗
[longptr.w]	CLR [$1000].w	4	4	72	3F	MS	LS		
([shortptr.w],X)	CLR ([$10],X)	4	3	92	6F	XX			✗
([longptr.w].X]	CLR ([$1000.w],X)	4	4	72	6F	MS	LS		
([shortptr.w],Y)	CLR ([$10],Y)	4	3	91	6F	XX			✗

See also: LD

JPF Jump far JPF

Syntax JPF dst e.g.:JPF test

Operation PC <= dst

Description The unconditional jump simply replaces the content of the PC by a destination with an extended address. Control then passes to the statement addressed by the program counter. For safe memory usage, this instruction must be used, when the operation crosses a memory section.

Instruction overview

mnem	dst	Affected condition flags						
		V	I1	H	I0	N	Z	C
JPF	Mem	-	-	-	-	-	-	-

Detailed description

dst	Asm	cy	lgth	Op-code(s)					ST7
extmem	JPF $2FFFFC	2	4		AC	ExtB	MS	LS	
[longptr.e]	JPF [$2FFC.e]	6	4	92	AC	MS	LS		

See also: JP, CALLF

SUB Subtraction SUB

Syntax SUB A,src e.g. SUB A,#%11001010

Operation A <= A- src

Description The source byte is subtracted from the contents of the accumulator/SP and the result is stored in the accumulator/SP. The source is a memory or data byte.

Instruction overview

mnem	dst	src	Affected condition flags						
			V	I1	H	I0	N	Z	C
SUB	A	Mem	V	-	-	-	N	Z	C
SUB	SP	Imm	-	-	-	-	-	-	-

V ⇒ (A7.M7 + A7.R7 + A7.M7.R7) ⊕ (A6.M6 + A6.R6 + A6.M6.R6)
Set if the signed operation generates an overflow, cleared otherwise.

N ⇒ R7
Set if bit 7 of the result is set (negative value), cleared otherwise.

Z ⇒ R7.R6.R5.R4.R3.R2.R1.R0
Set if the result is zero (0x00), cleared otherwise.

C ⇒ $\overline{A7}.M7 + \overline{A7}.R7 + A7.M7.R7$
Set if a borrow request occurred from bit 7, cleared otherwise.

Detailed description

dst	src	Asm	cy	lgth	Op-code(s)				ST7
A	#byte	SUB A,#$55	1	2		A0	XX		✗
A	shortmem	SUB A,$10	1	2		B0	XX		✗
A	longmem	SUB A,$1000	1	3		C0	MS	LS	✗
A	(X)	SUB A,(X)	1	1		F0			✗
A	(shortoff,X)	SUB A,($10,X)	1	2		E0	XX		✗
A	(longoff,X)	SUB A,($1000,X)	1	3		D0	MS	LS	✗
A	(Y)	SUB A,(Y)	1	2	90	F0			✗
A	(shortoff,Y)	SUB A,($10,Y)	1	3	90	E0	XX		✗
A	(longoff,Y)	SUB A,($1000,Y)	1	4	90	D0	MS	LS	✗
A	(shortoff,SP)	SUB A,($10,SP)	1	2		10	XX		
A	[shortptr.w]	SUB A,[$10.w]	4	3	92	C0	XX		✗
A	[longptr.w]	SUB A,[$1000.w]	4	4	72	C0	MS	LS	
A	([shortptr.w],X)	SUB A,([$10.w],X)	4	3	92	D0	XX		✗
A	([longptr.w],X)	SUB A,([$1000.w],X)	4	4	72	D0	MS	LS	
A	([shortptr.w],Y)	SUB A,([$10.w],Y)	4	3	91	D0	XX		✗
SP	#byte	SUB SP,#$9	1	2		52	XX		

See also: SUBW, ADD, ADC, SBC, MUL