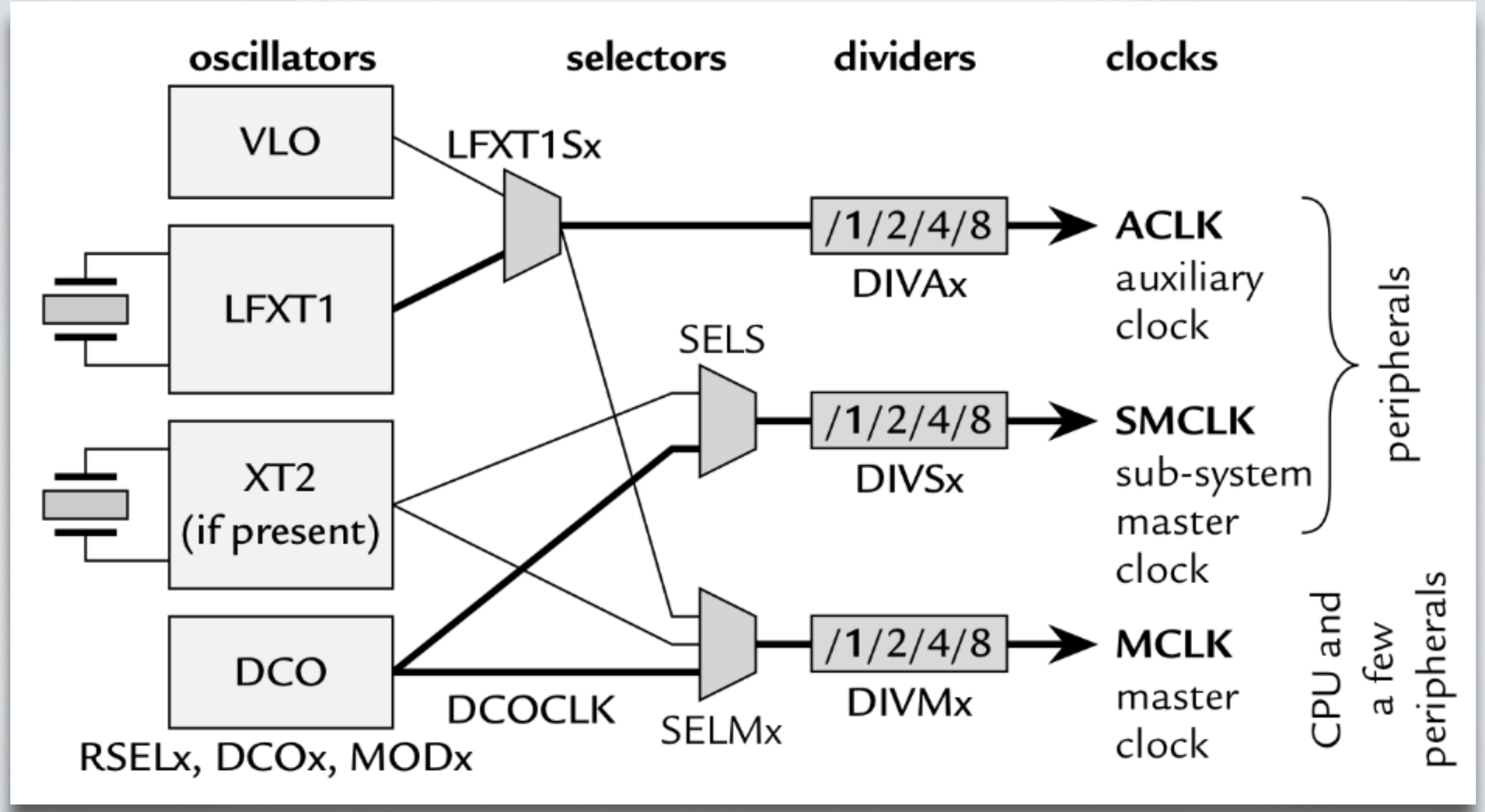
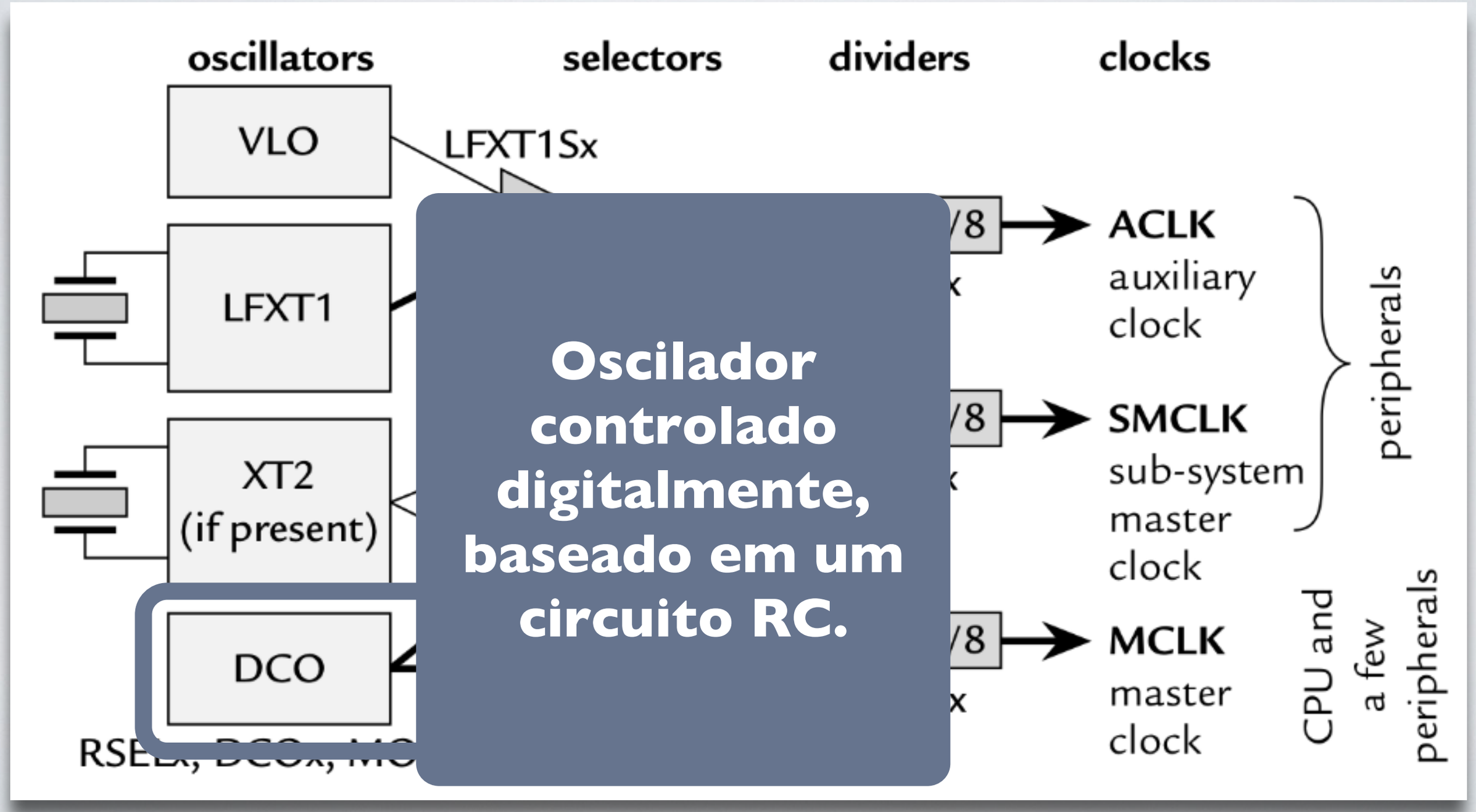
MICROPROCESSADORES E MICROCONTROLADORES

SISTEMA DE CLOCK

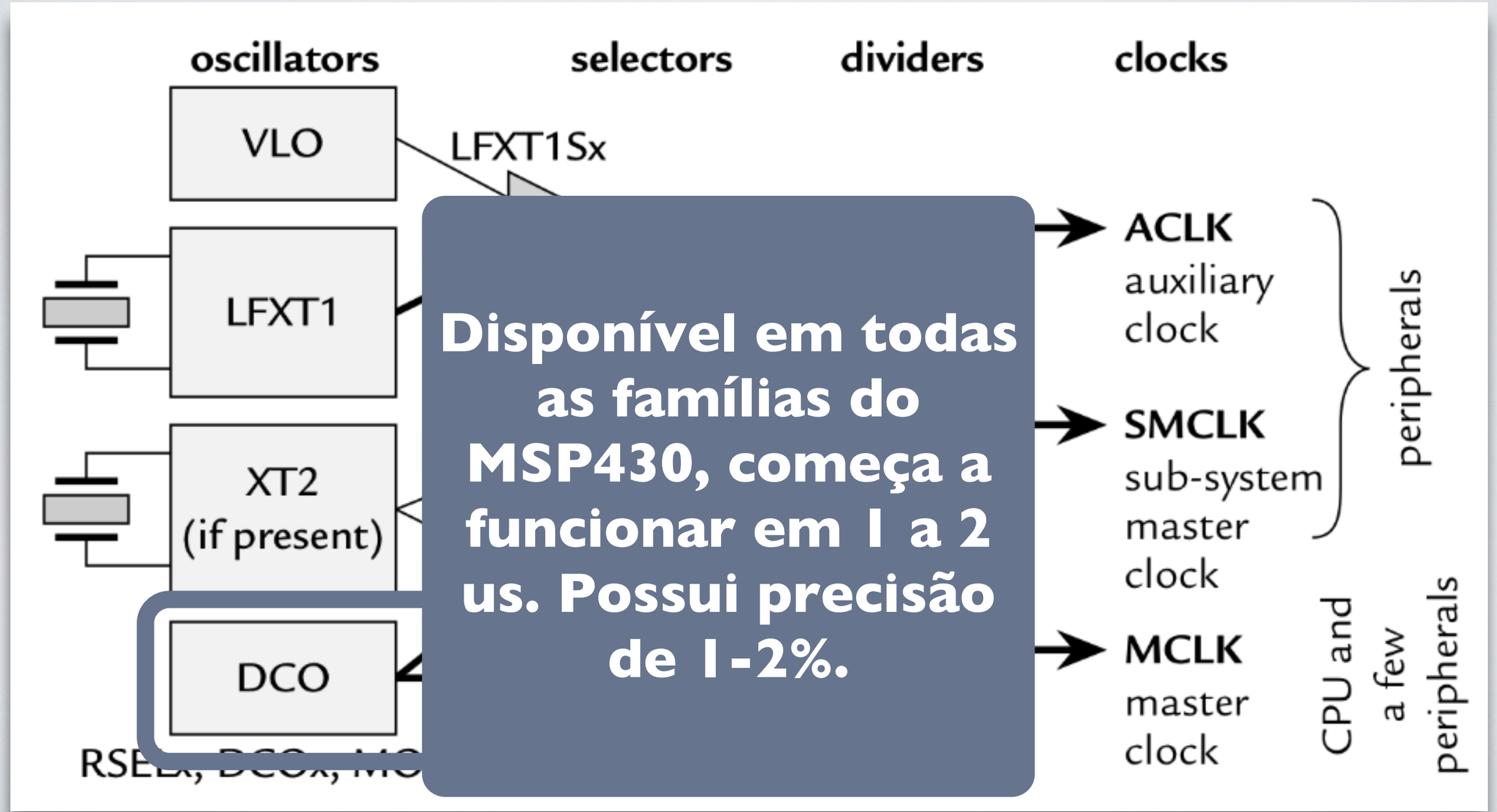


Basic Clock Module+ (BCM+)

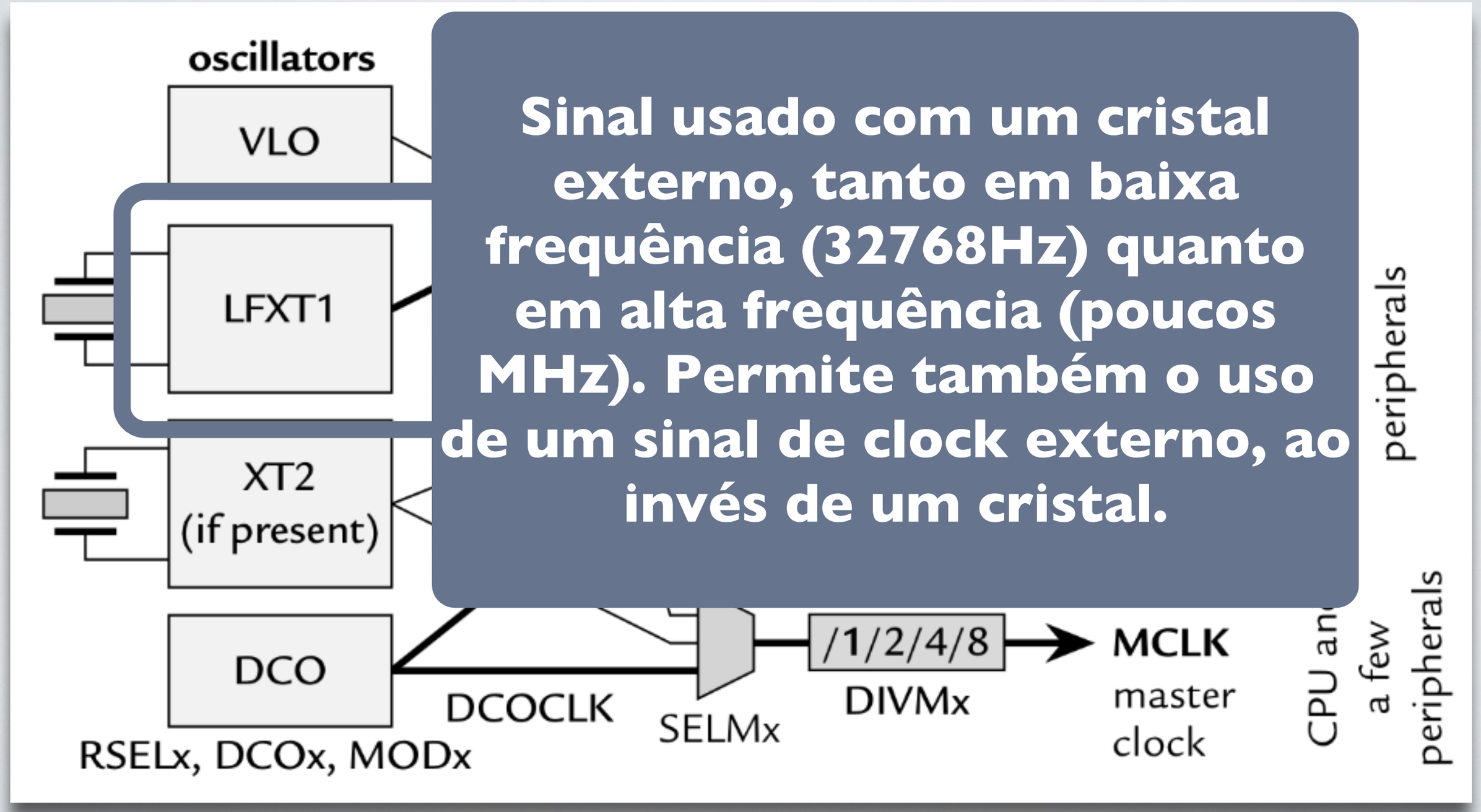
SISTEMA DE CLOCK



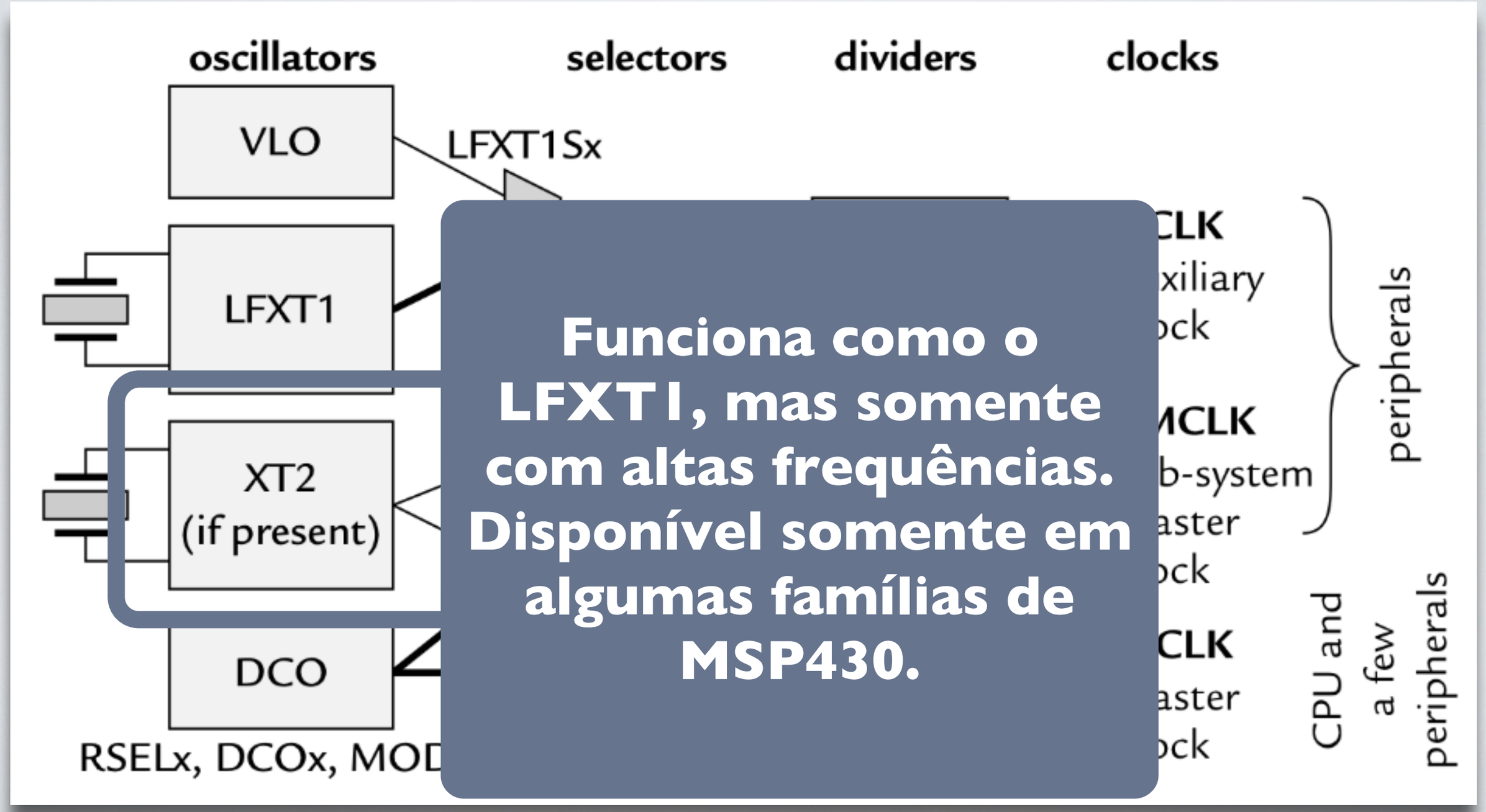
SISTEMA DE CLOCK



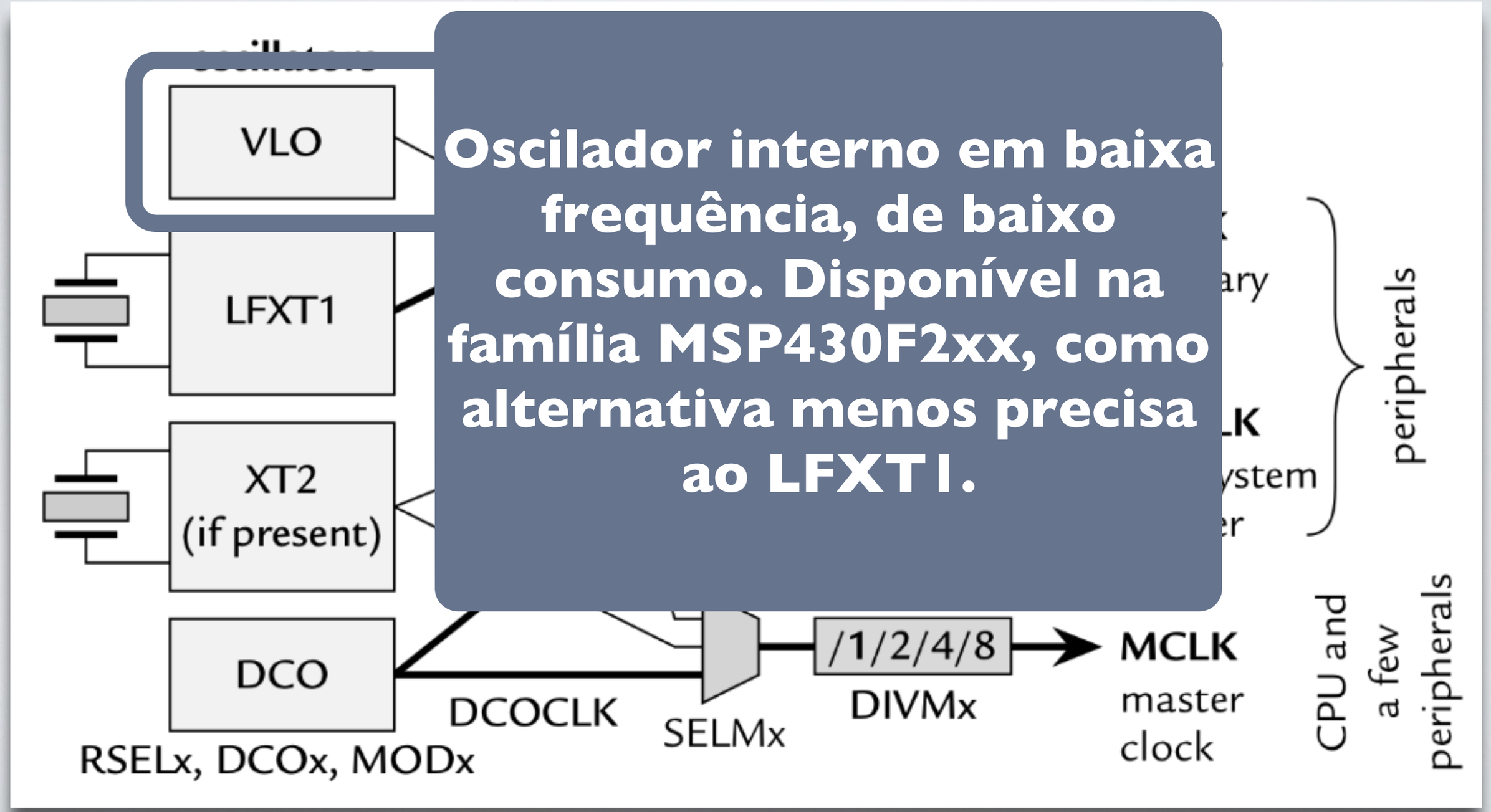
SISTEMA DE CLOCK



SISTEMA DE CLOCK

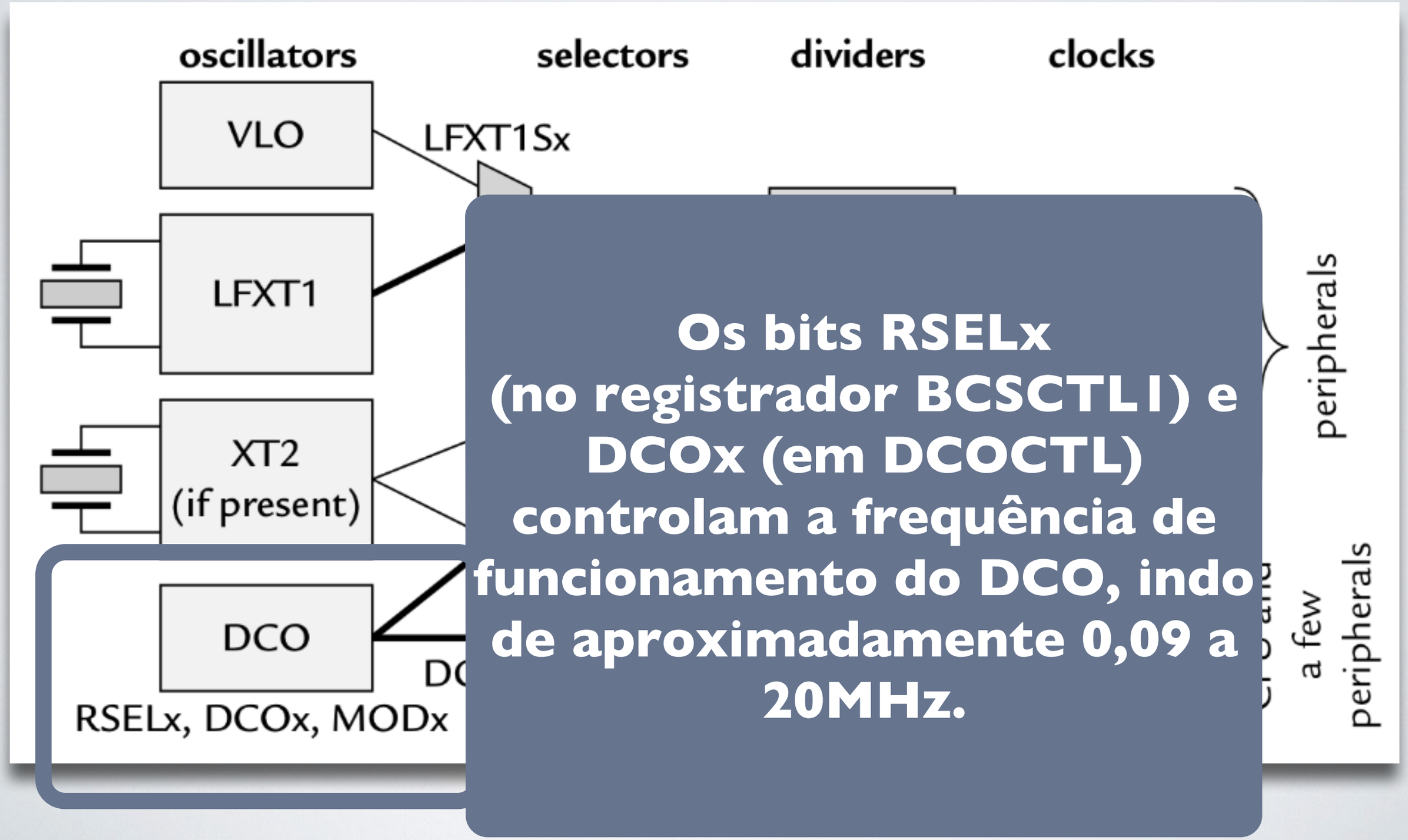


SISTEMA DE CLOCK



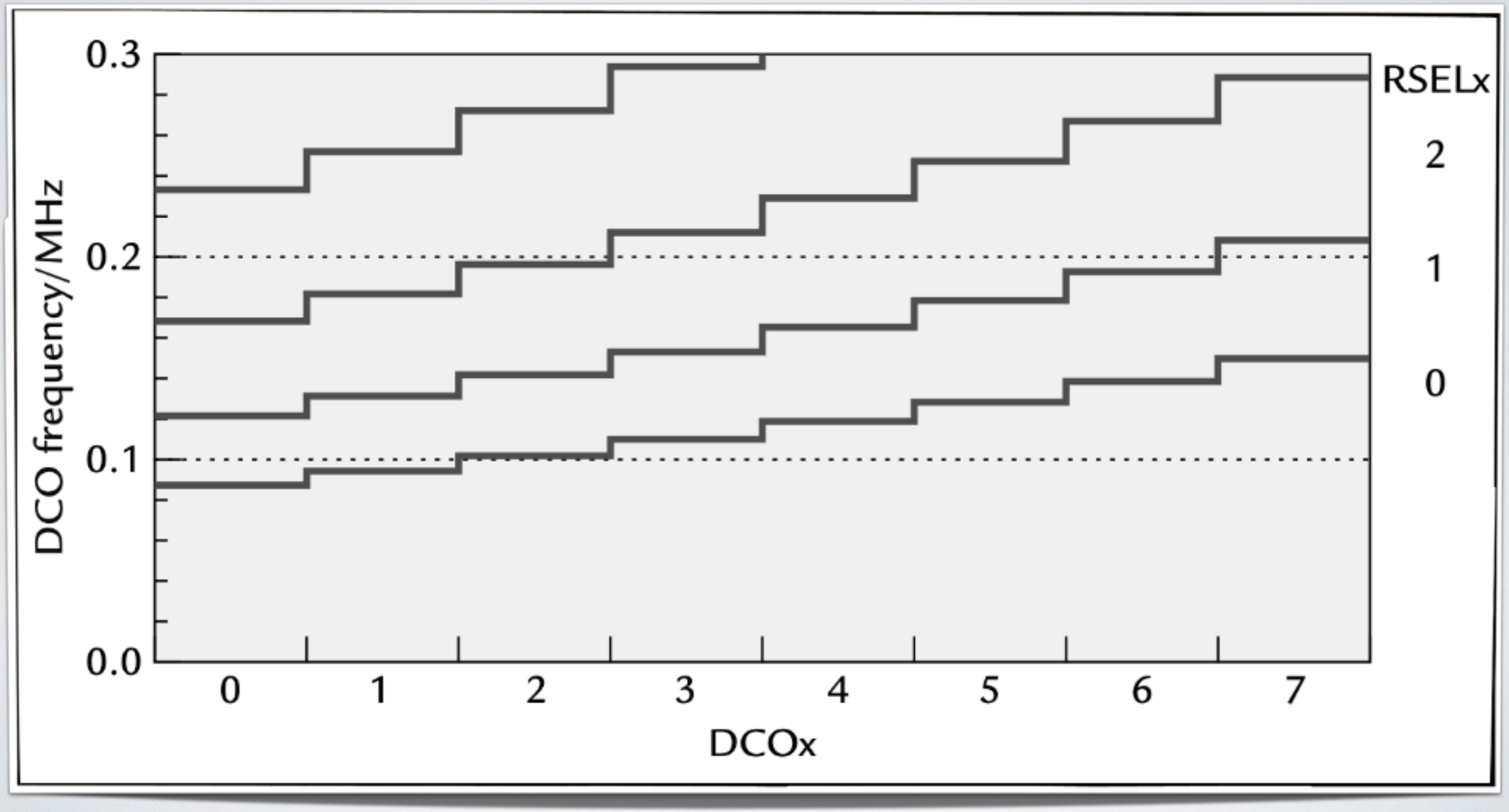
Oscilador interno em baixa frequência, de baixo consumo. Disponível na família MSP430F2xx, como alternativa menos precisa ao LFXT1.

SISTEMA DE CLOCK

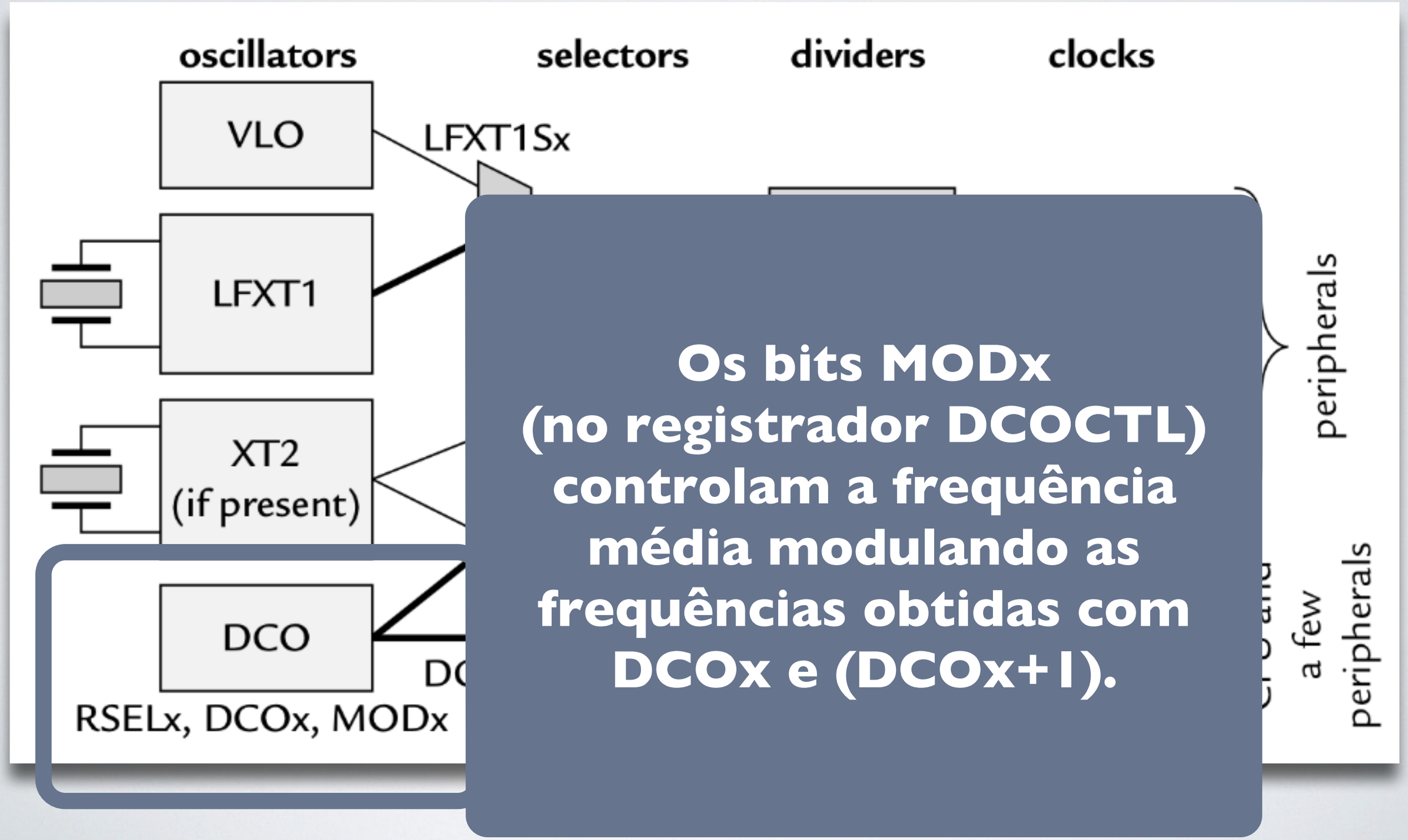


Os bits RSELx (no registrador BCSCTL1) e DCOx (em DCOCTL) controlam a frequência de funcionamento do DCO, indo de aproximadamente 0,09 a 20MHz.

SISTEMA DE CLOCK

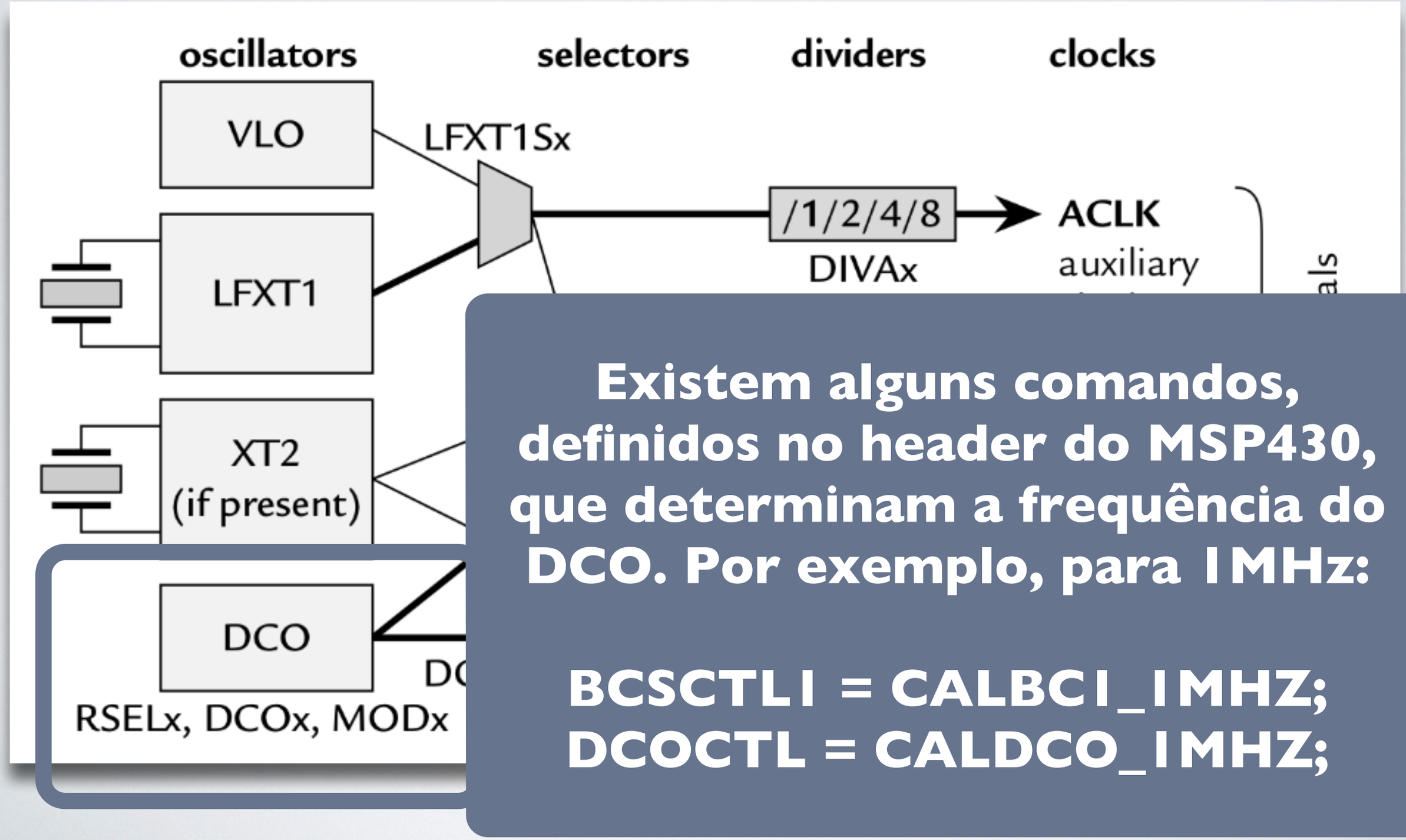


SISTEMA DE CLOCK



Os bits MODx (no registrador DCOCTL) controlam a frequência média modulando as frequências obtidas com DCOx e (DCOx+1).

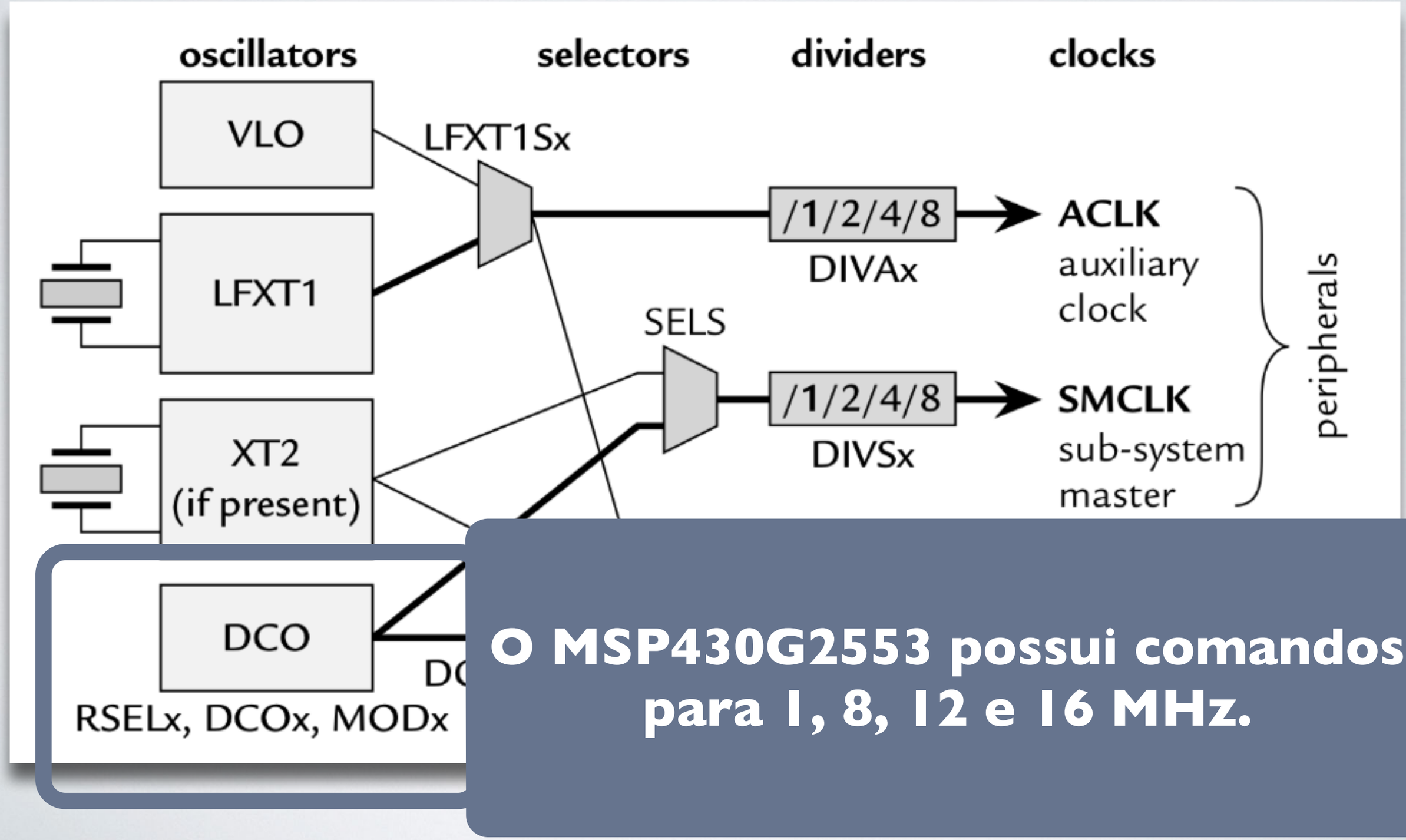
SISTEMA DE CLOCK



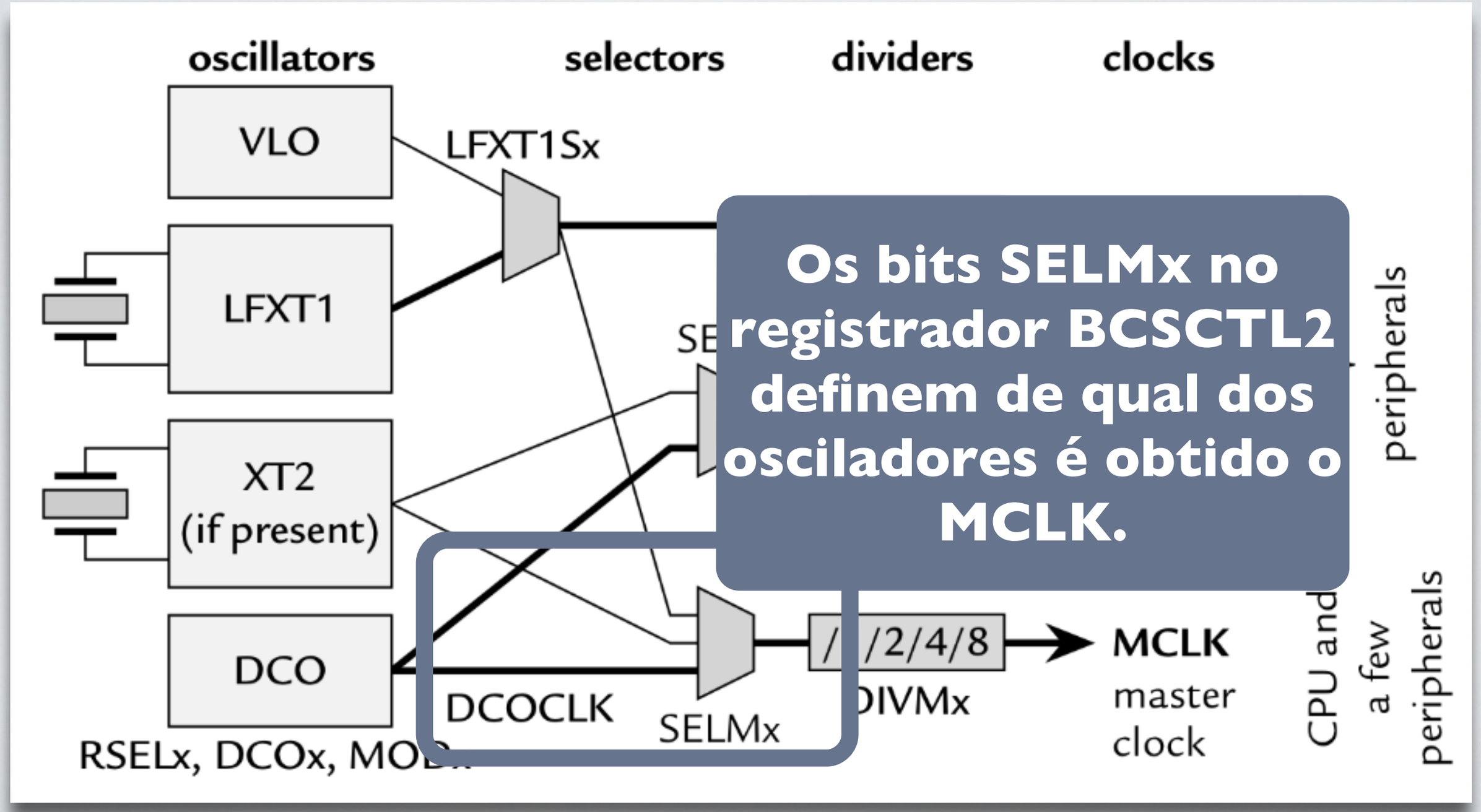
Existem alguns comandos, definidos no header do MSP430, que determinam a frequência do DCO. Por exemplo, para 1MHz:

```
BCSCTL1 = CALBC1_1MHZ;
DCOCTL = CALDCO_1MHZ;
```

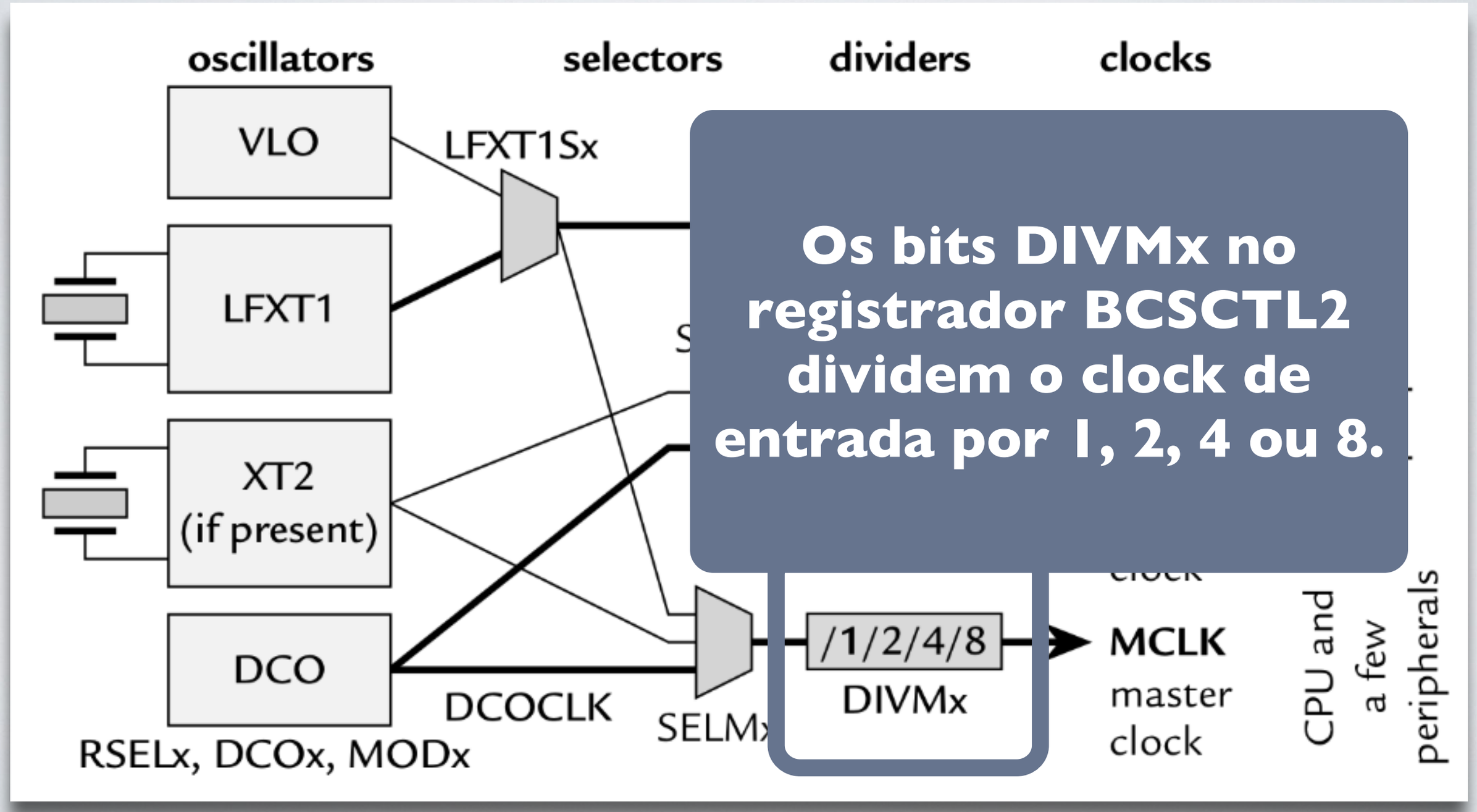
SISTEMA DE CLOCK



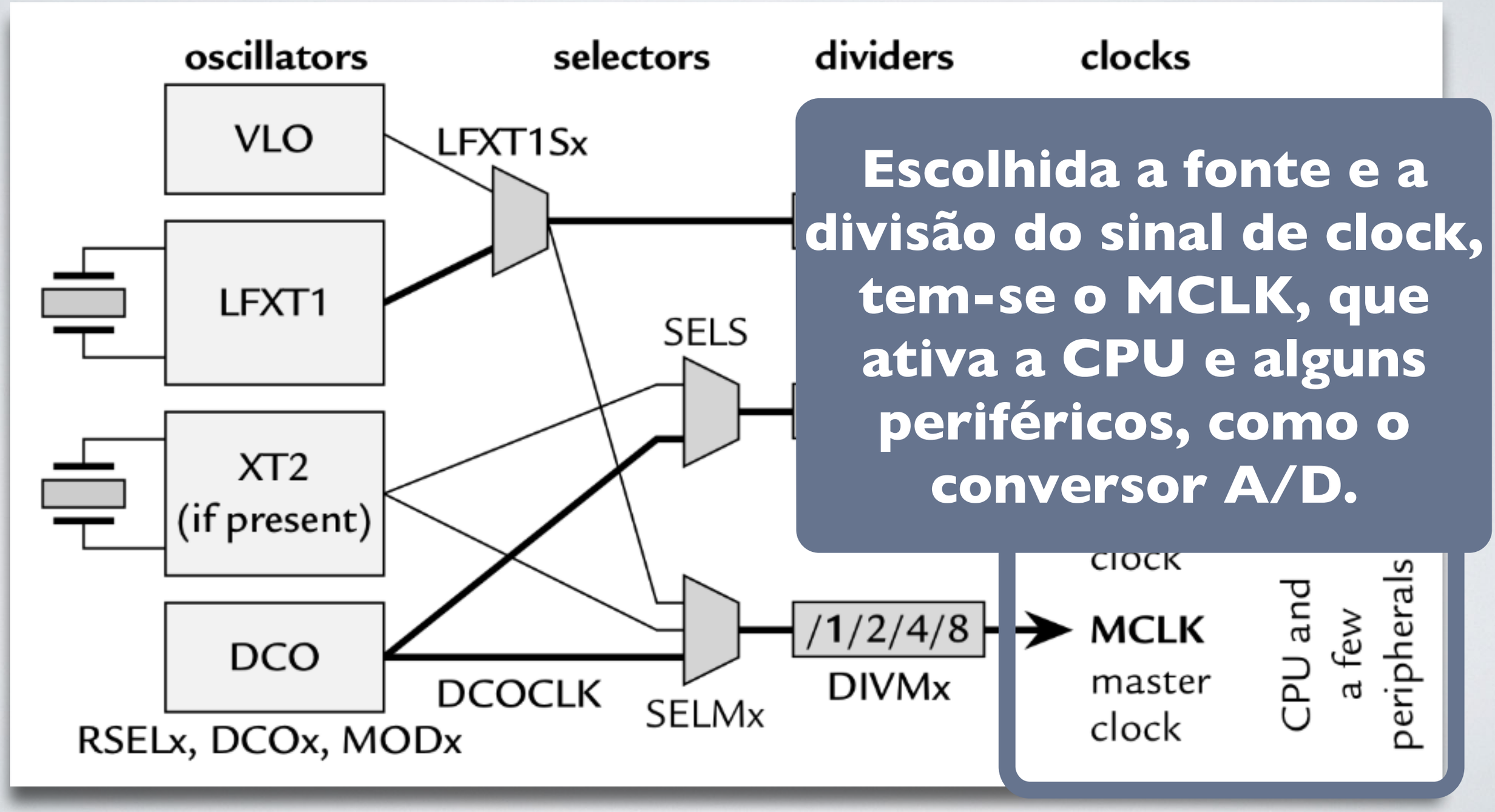
SISTEMA DE CLOCK



SISTEMA DE CLOCK



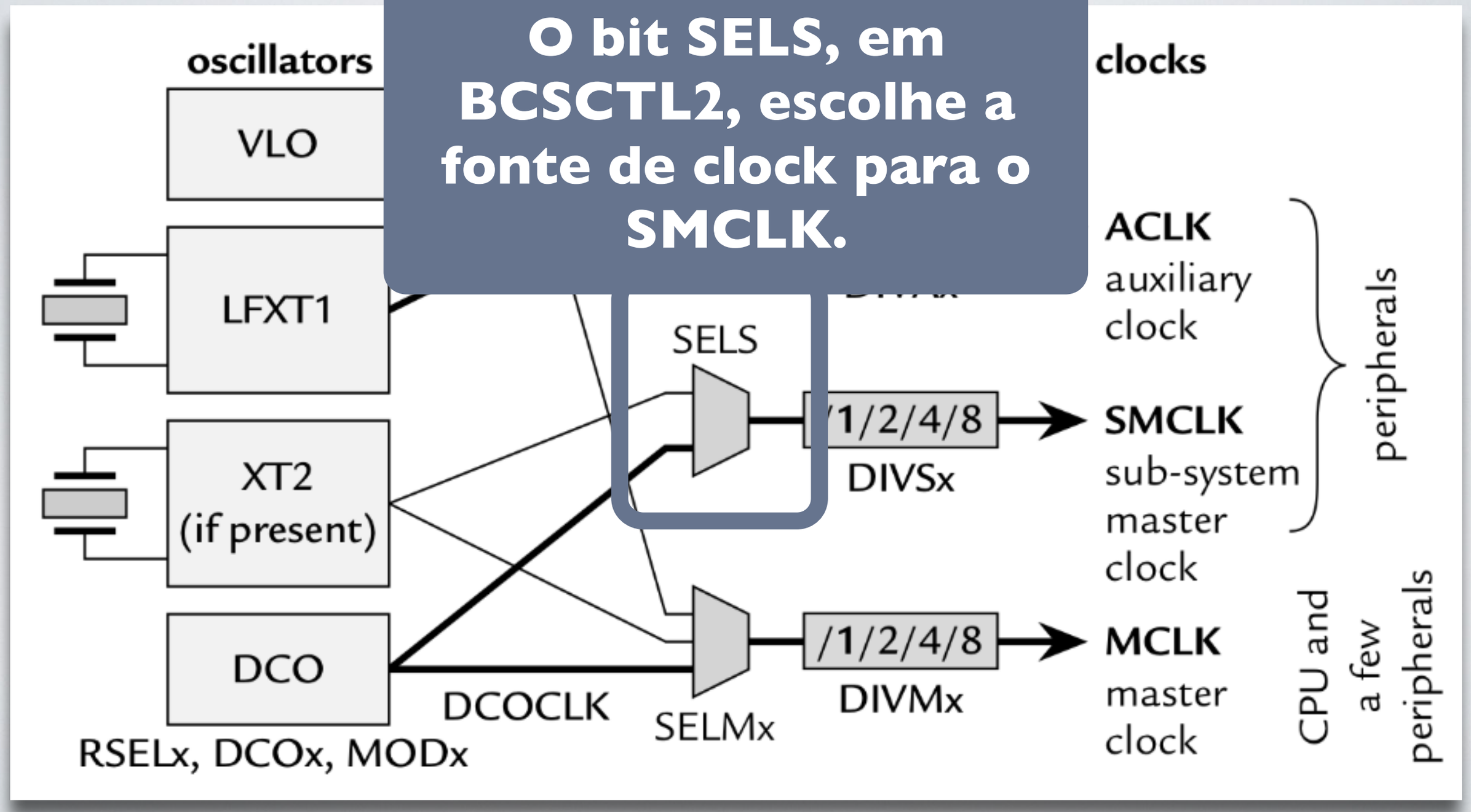
SISTEMA DE CLOCK



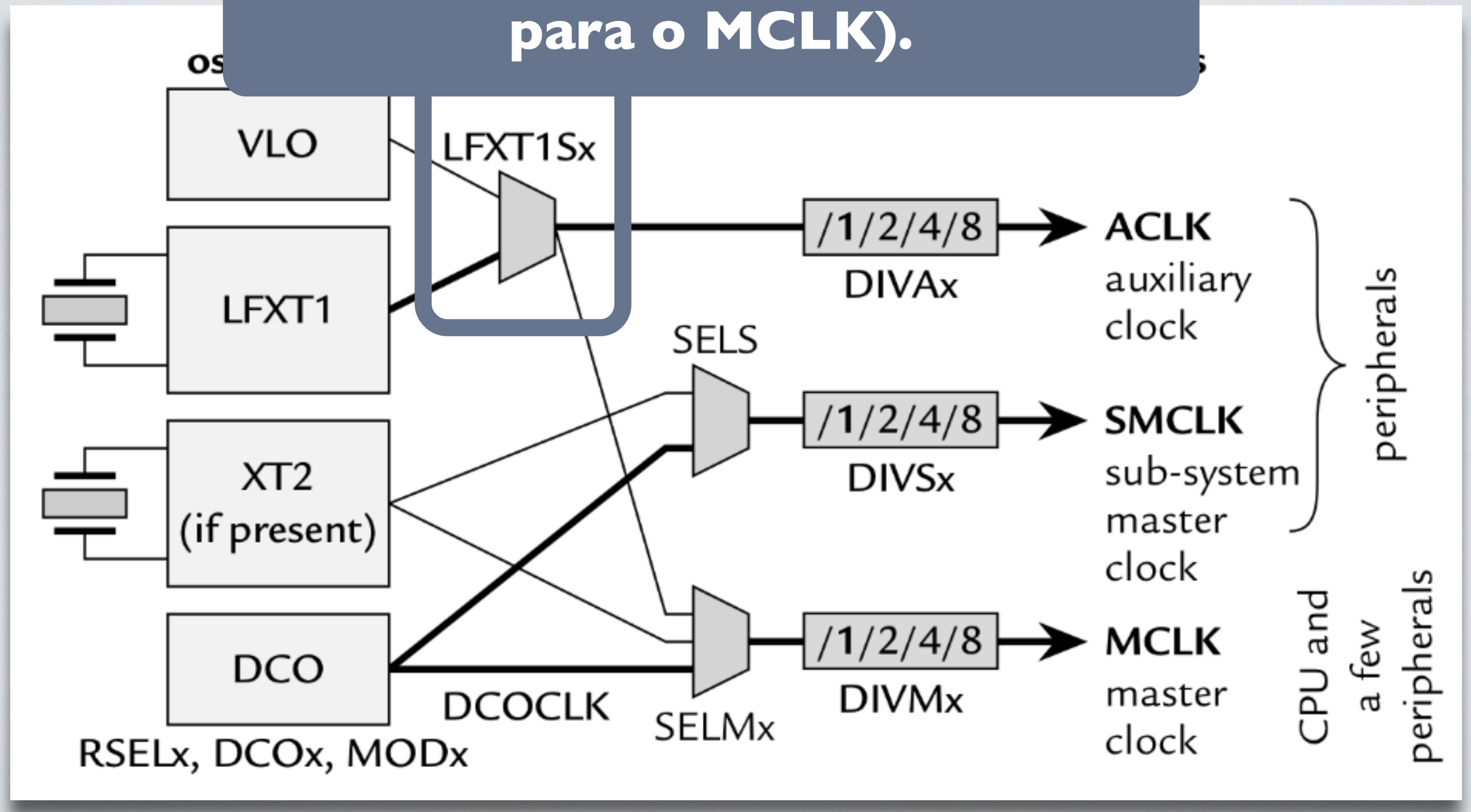
Escolhida a fonte e a divisão do sinal de clock, tem-se o MCLK, que ativa a CPU e alguns periféricos, como o conversor A/D.

SISTEMA DE CLOCK

O bit SELS, em BCSCTL2, escolhe a fonte de clock para o SMCLK.

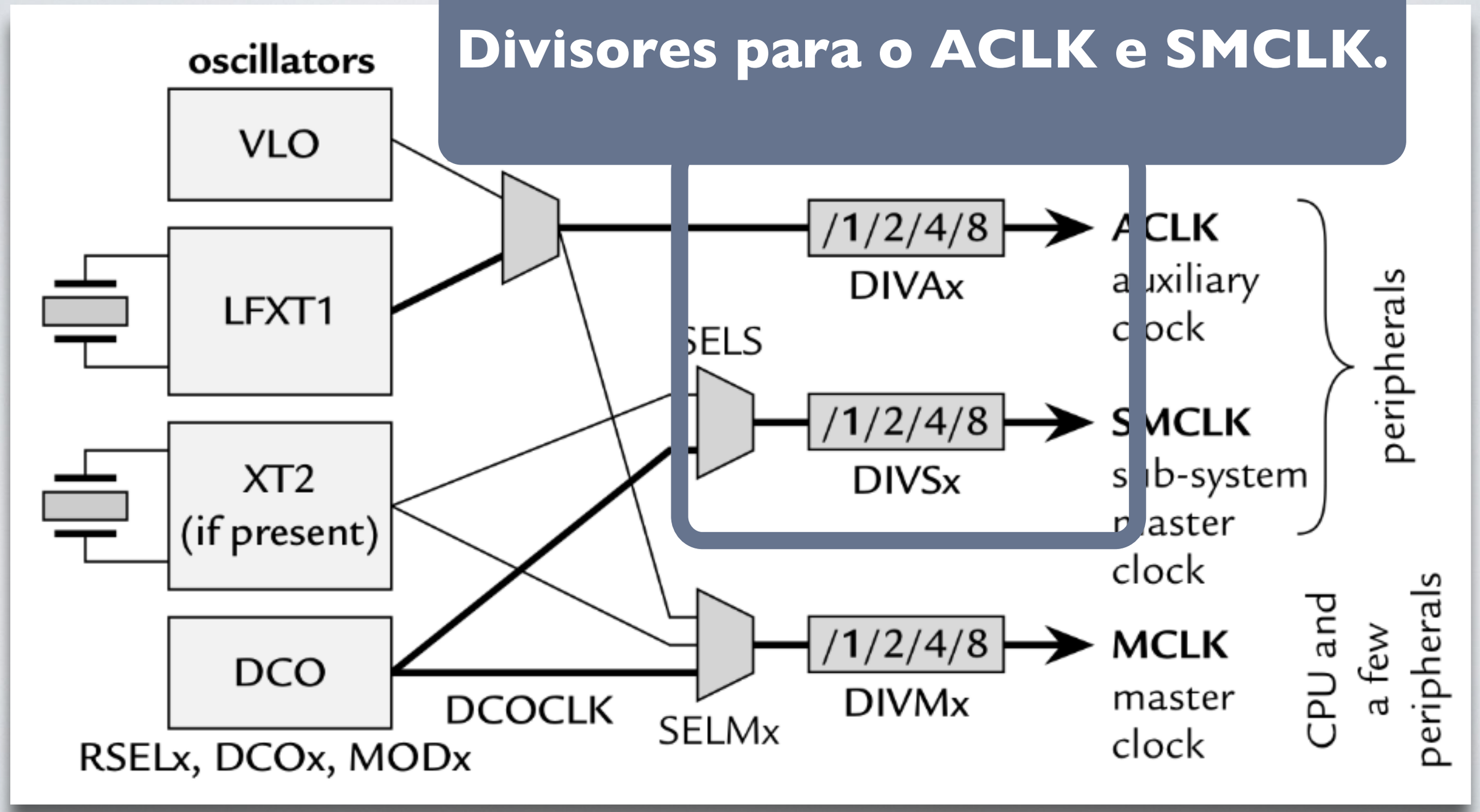


Os bits LFXT1Sx, em BCSCTL3, escolhem a fonte de clock para o ACLK (e também uma das opções para o MCLK).

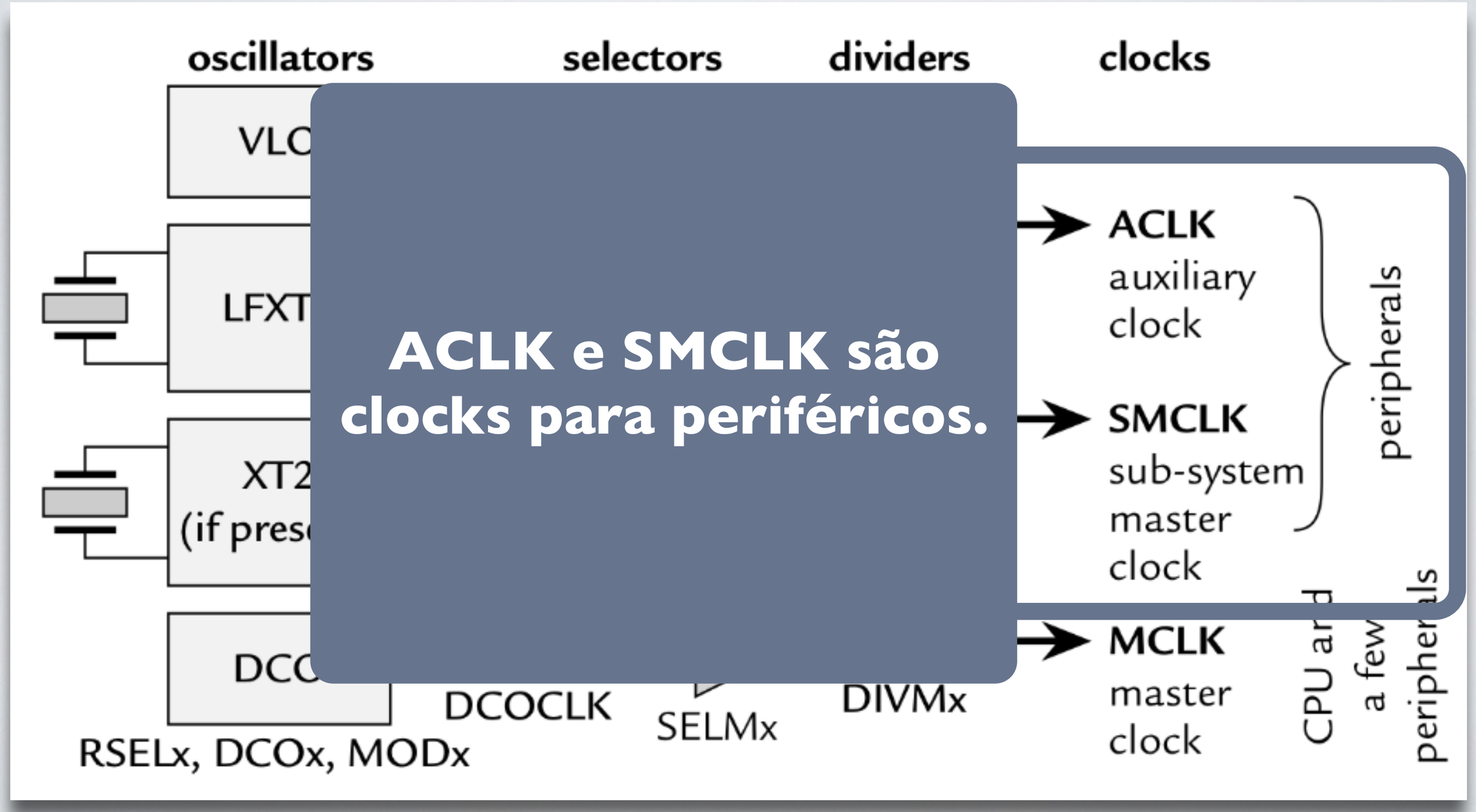


SISTEMA DE CLOCK

Divisores para o ACLK e SMCLK.



SISTEMA DE CLOCK



FALHAS NO SISTEMA DE CLOCK

Falhas nos clocks podem ser catastróficas. Cada oscilador tem uma flag para indicar falhas.

Qualquer falha ativa o bit OFIFG em IFG1, chamando uma interrupção não-mascarável, se esta estiver habilitada.

FALHAS NO SISTEMA DE CLOCK

Além disso, o MCLK troca para o DCO se este não estiver sendo usado. Isso garante que o software será executado.

FALHAS NO SISTEMA DE CLOCK

O bit OFIFG começa setado, de forma que o MCLK sempre é obtido do DCO quando o sistema inicia. Se o MCLK tiver de ser obtido de um cristal, deve-se fazer OFIFG=0 até o oscilador a cristal estabilizar.