MICROPROCESSADORES E MICROCONTROLADORES

TIMER_A

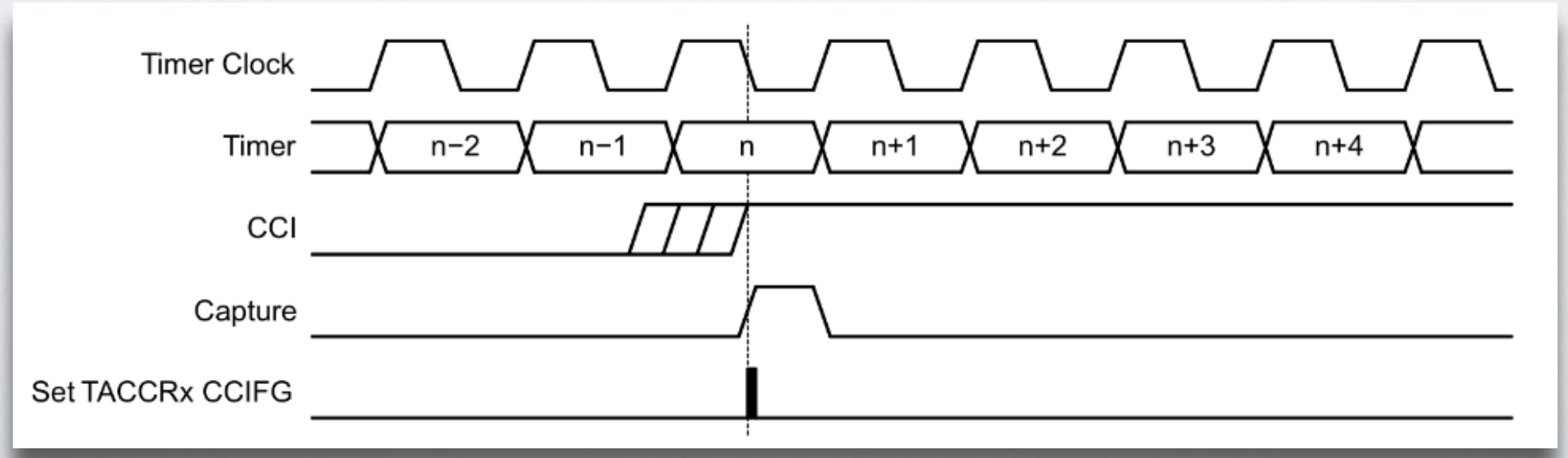
Timer mais completo do MSP430.

Registrador TAR, de 16 bits, é incrementado de acordo com o sinal de clock escolhido.

Quando TAR retorna a 0, a flag TAIFG é setada.

TIMER_A

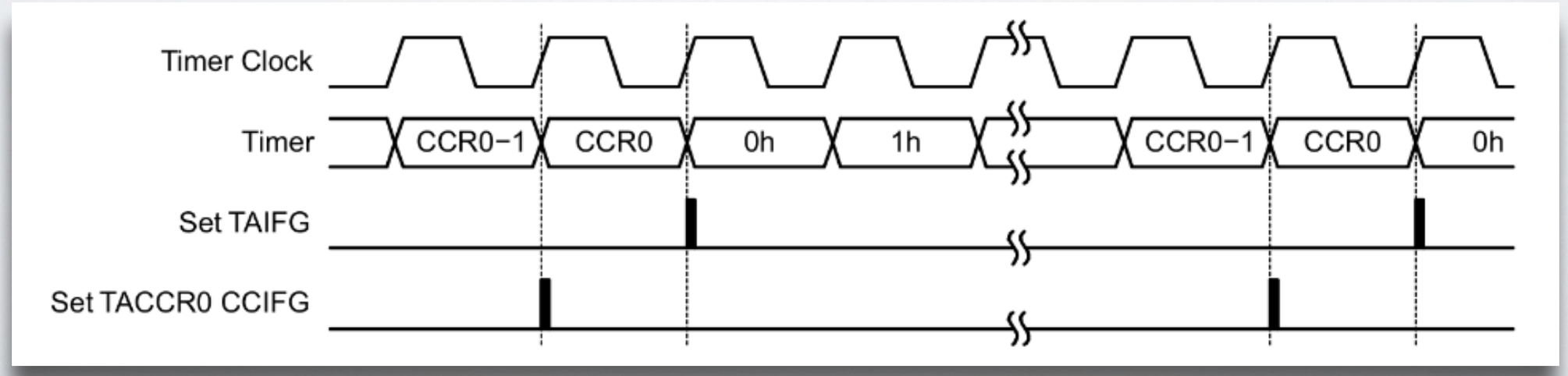
Canais de captura - é possível guardar nos registradores TACCRn o valor de TAR na transição de um sinal de escolha (interno ao MSP430 ou externo). Este evento pode também gerar um interrupção.



TIMER_A

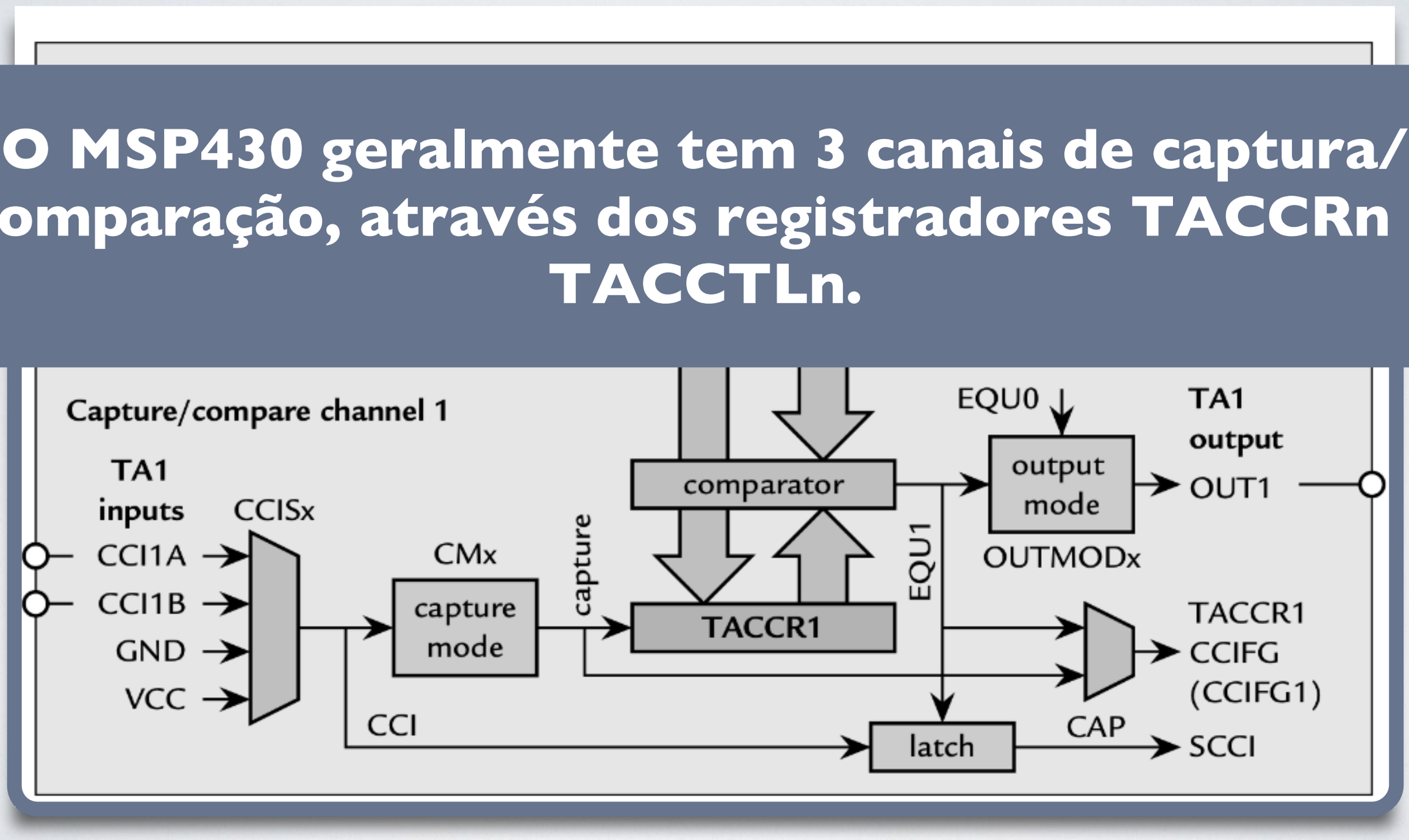
Canais de comparação - é possível mudar o valor de uma saída de escolha (interna ao MSP430 ou externa) quando TAR = TACCRn.

Este evento pode também gerar um interrupção.



CAPTURA/COMPARAÇÃO

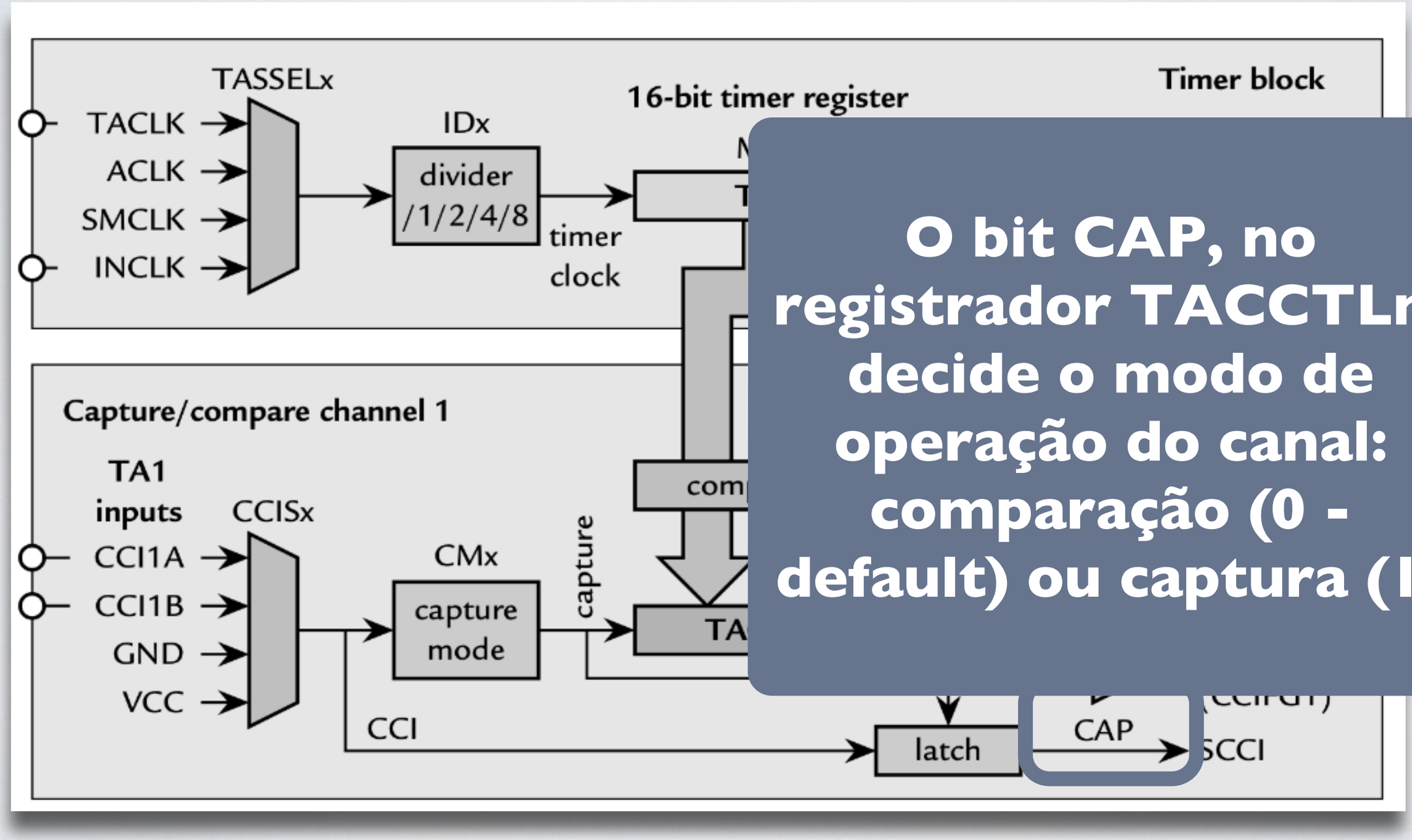
O MSP430 geralmente tem 3 canais de captura/comparação, através dos registradores TACCRn e TACCTLn.



CAPTURA/COMPARAÇÃO

O canal 0 não pode ser usado quando MC=1 ou MC=3 (modos Up e Up/Down), pois TACCR0 já está sendo utilizado para definir o período do Timer_A.

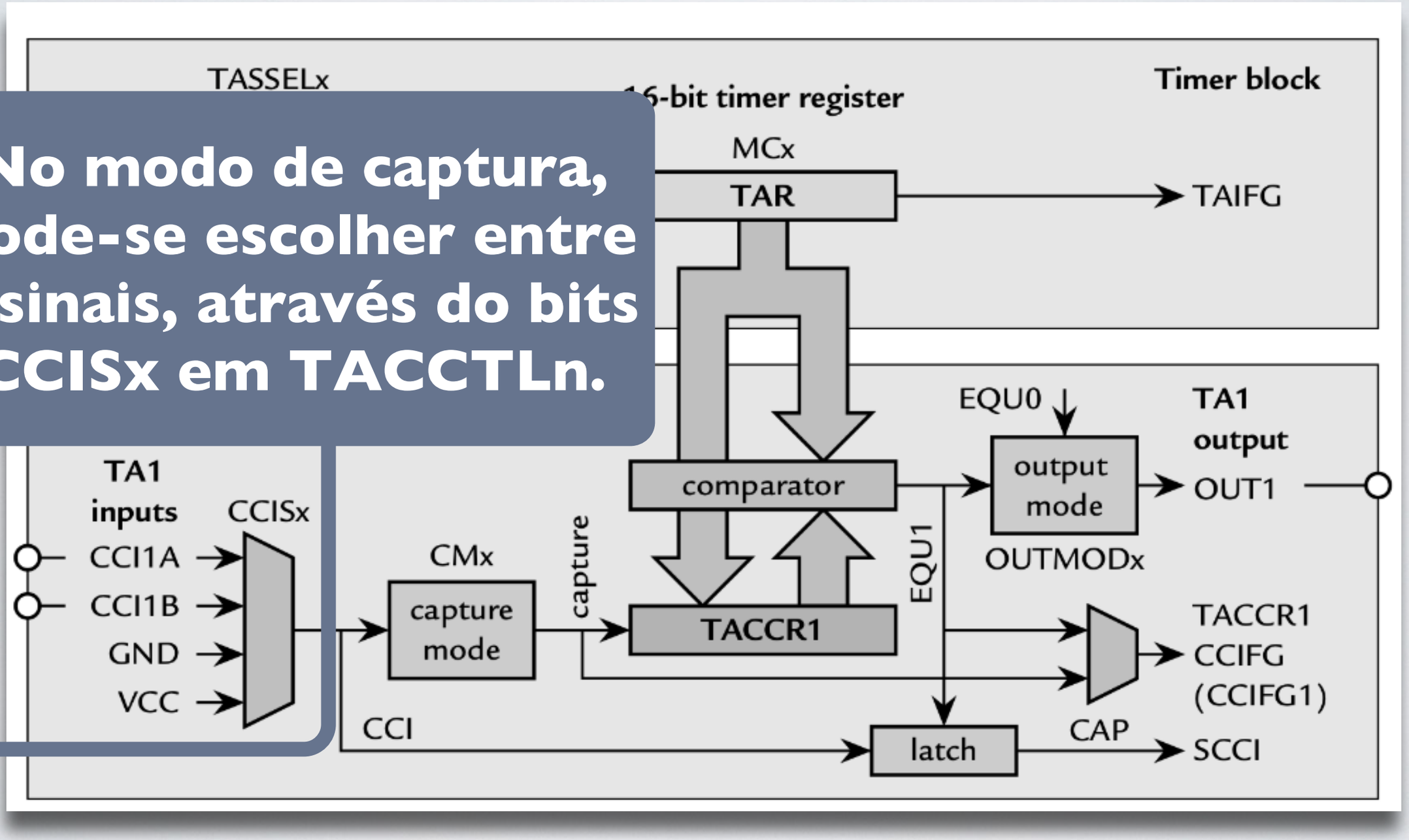
CAPTURA/COMPARAÇÃO



O bit CAP, no registrador TACCTLn, decide o modo de operação do canal: comparação (0 - default) ou captura (1)

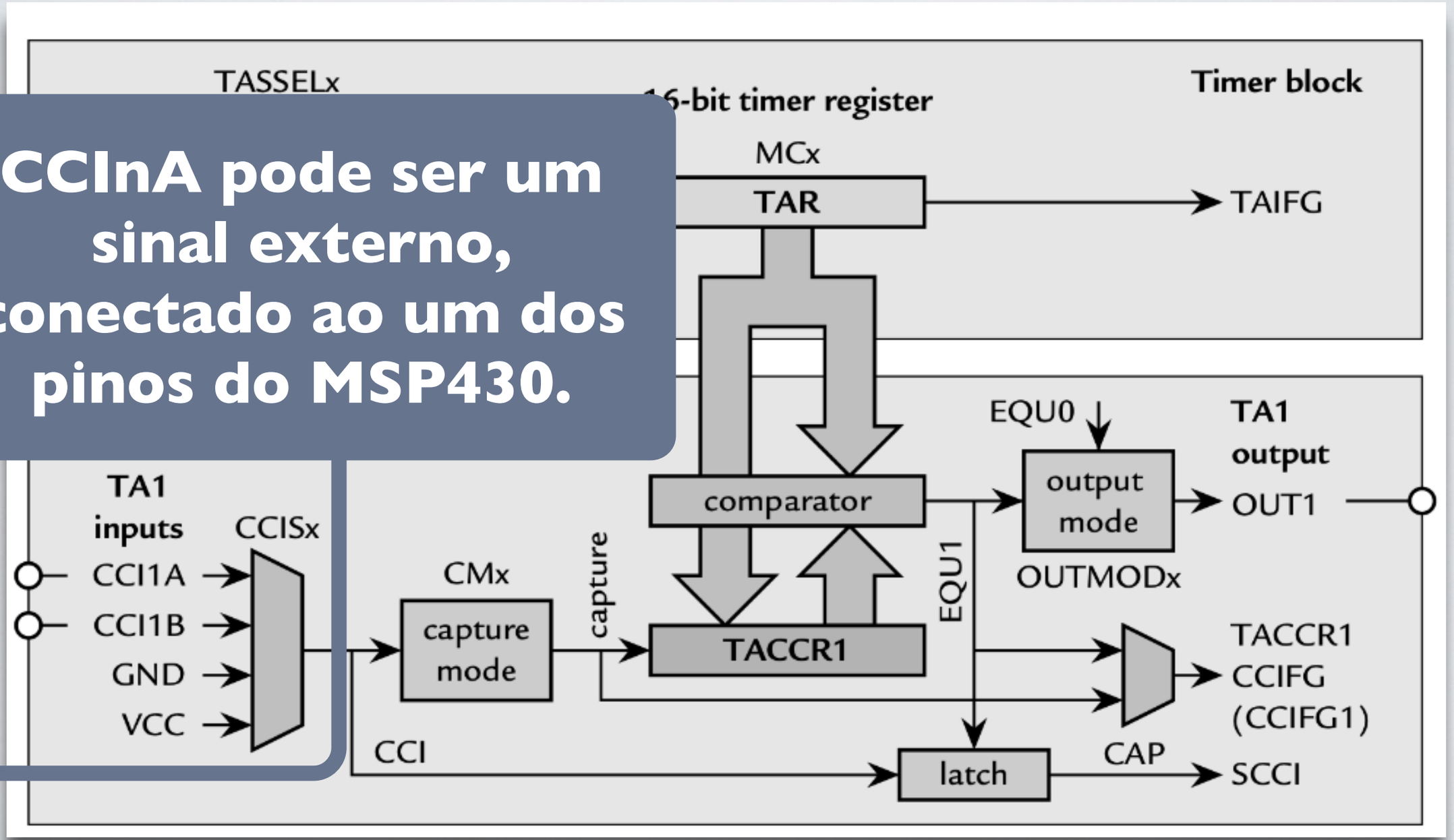
CAPTURA

No modo de captura, pode-se escolher entre 4 sinais, através do bits CCISx em TACCTLn.



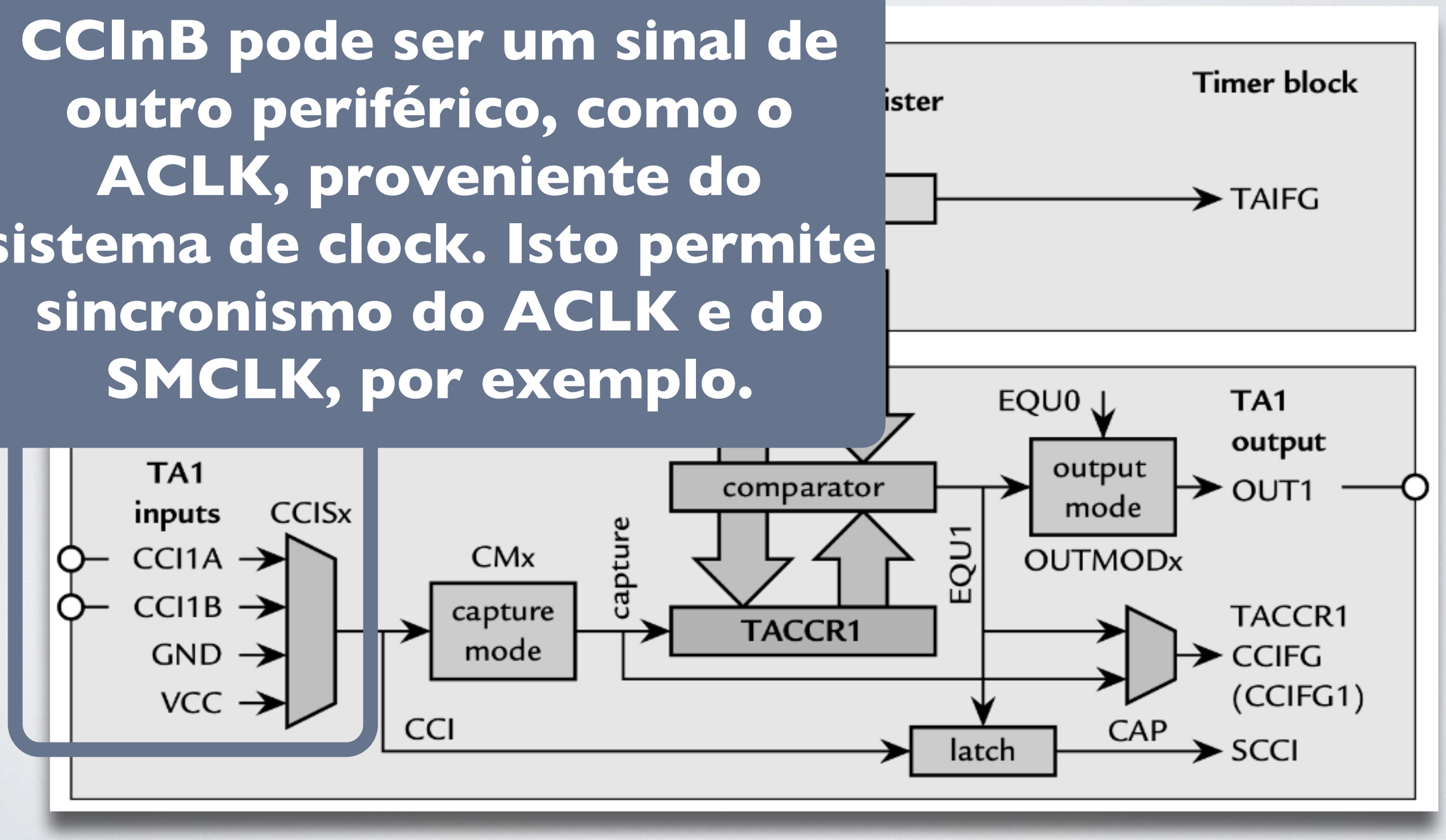
CAPTURA

CCInA pode ser um sinal externo, conectado ao um dos pinos do MSP430.



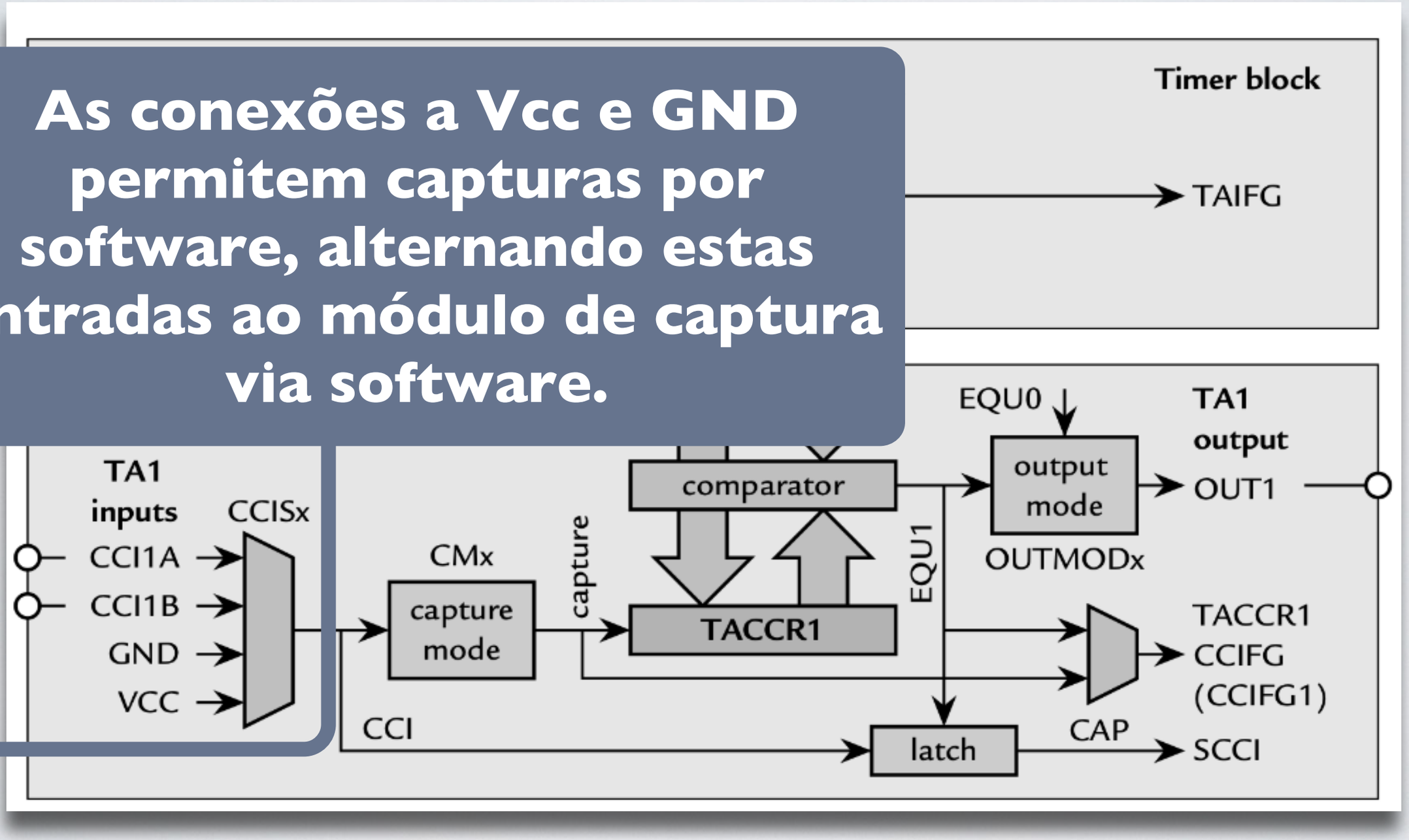
CAPTURA

CCInB pode ser um sinal de outro periférico, como o ACLK, proveniente do sistema de clock. Isto permite sincronismo do ACLK e do SMCLK, por exemplo.



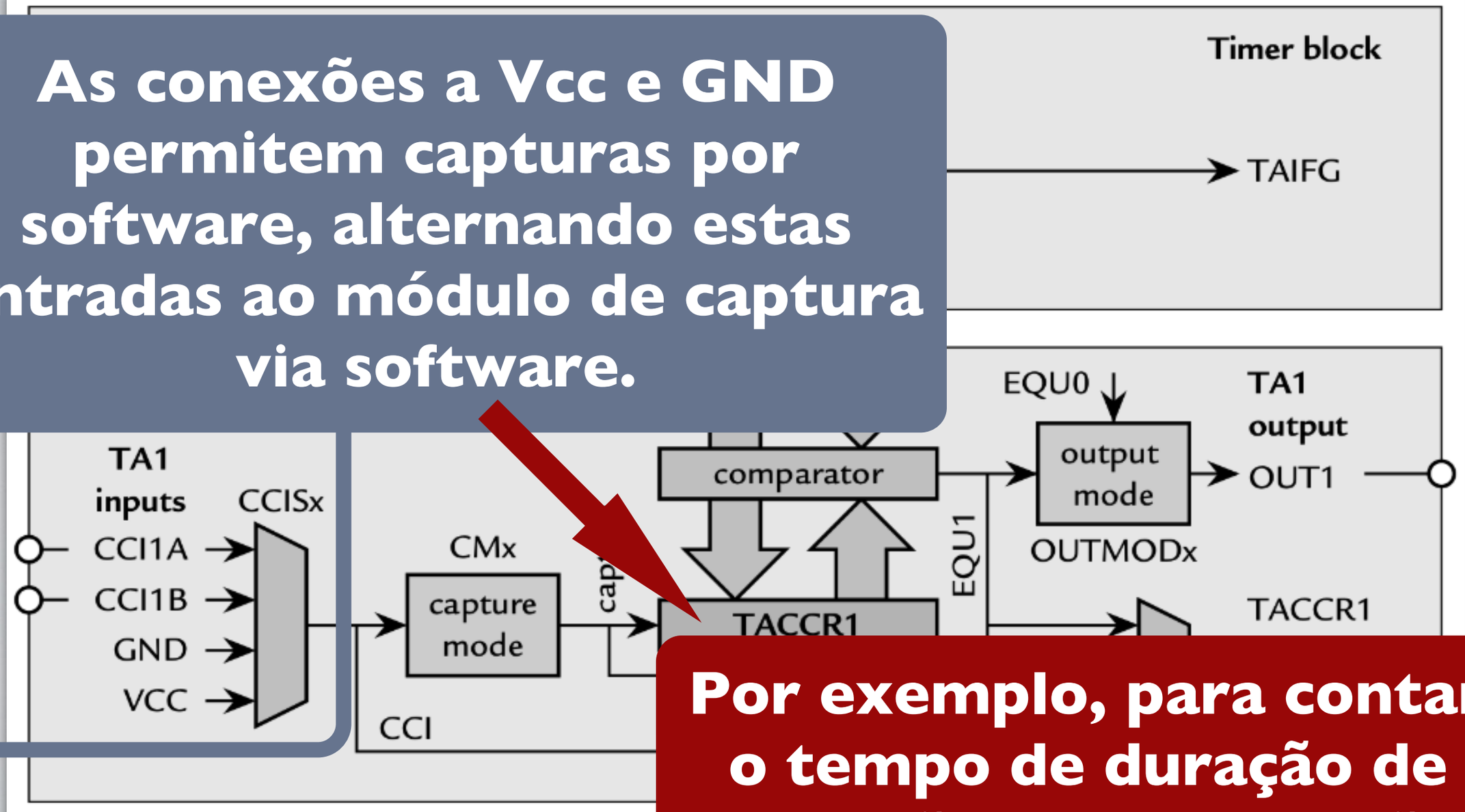
CAPTURA

As conexões a Vcc e GND permitem capturas por software, alternando estas entradas ao módulo de captura via software.



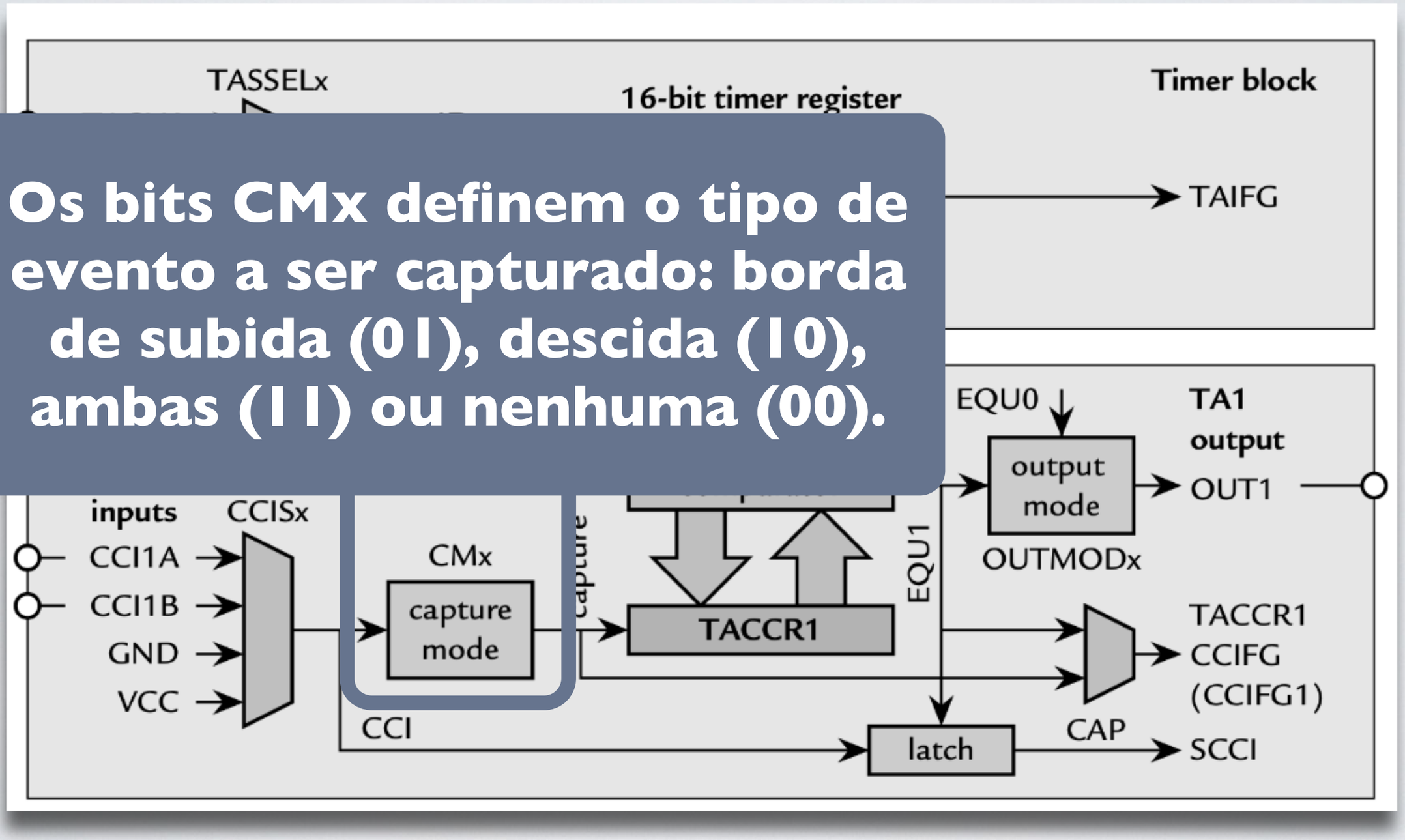
CAPTURA

As conexões a Vcc e GND permitem capturas por software, alternando estas entradas ao módulo de captura via software.



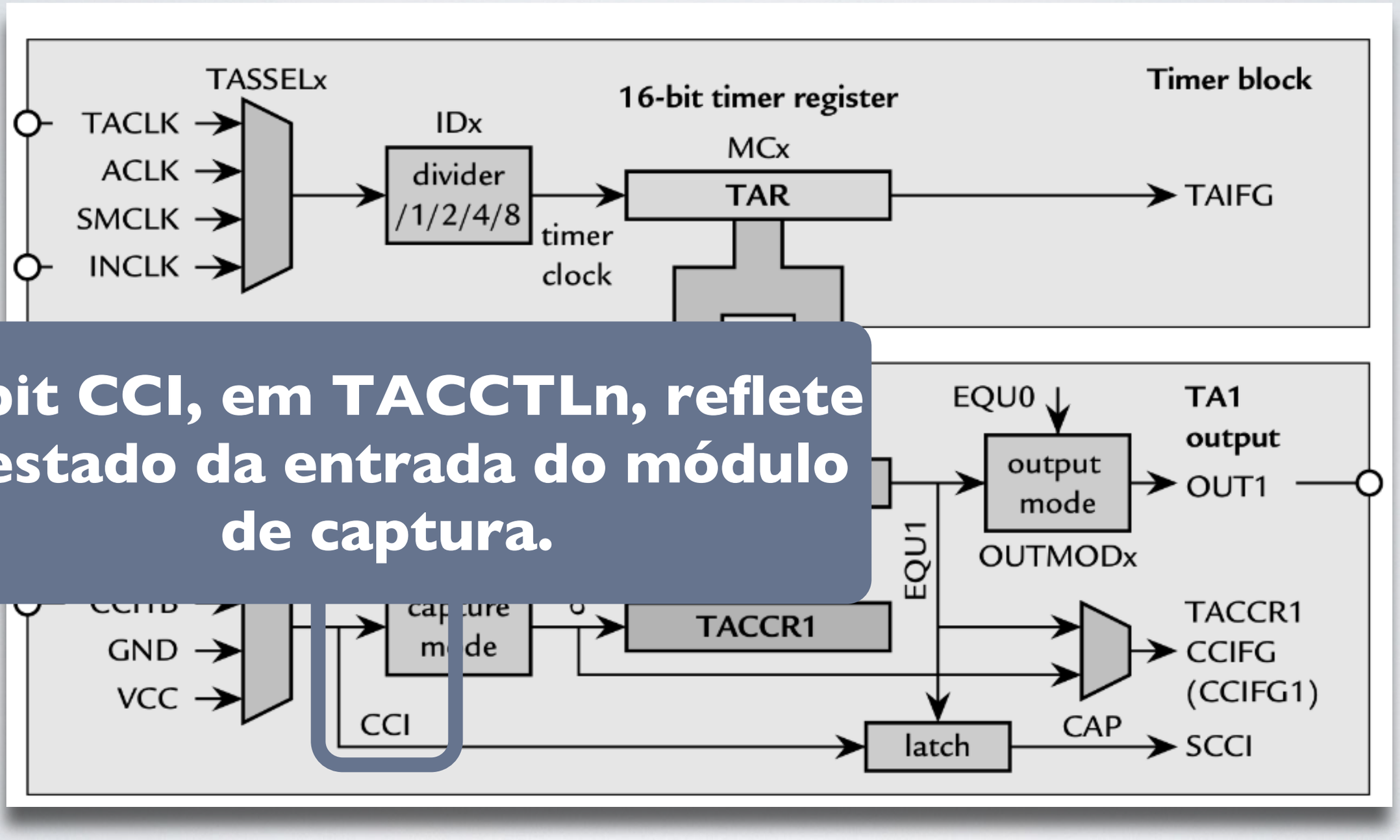
Por exemplo, para contar o tempo de duração de execução de uma função.

CAPTURA



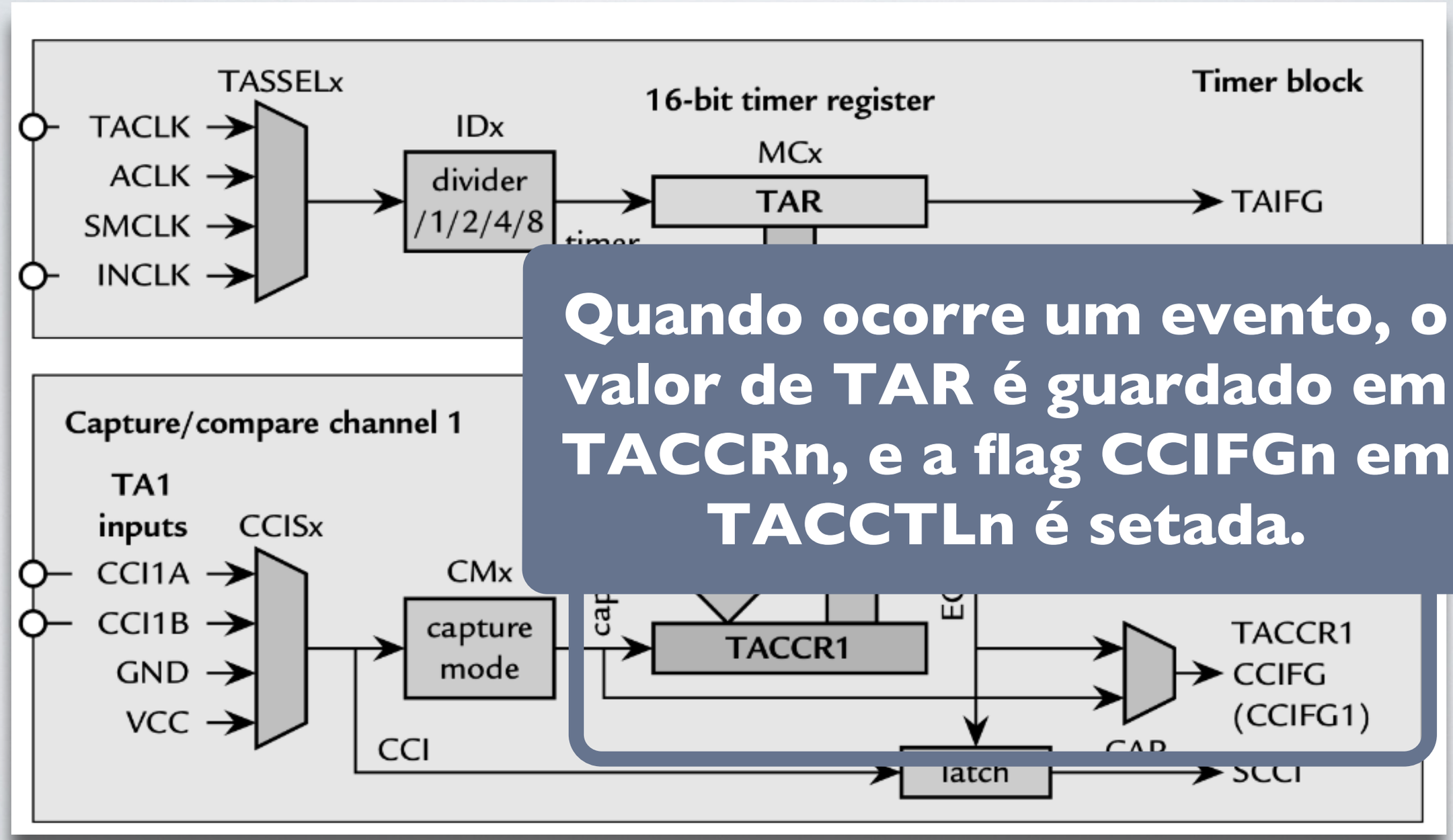
Os bits CMx definem o tipo de evento a ser capturado: borda de subida (01), descida (10), ambas (11) ou nenhuma (00).

CAPTURA



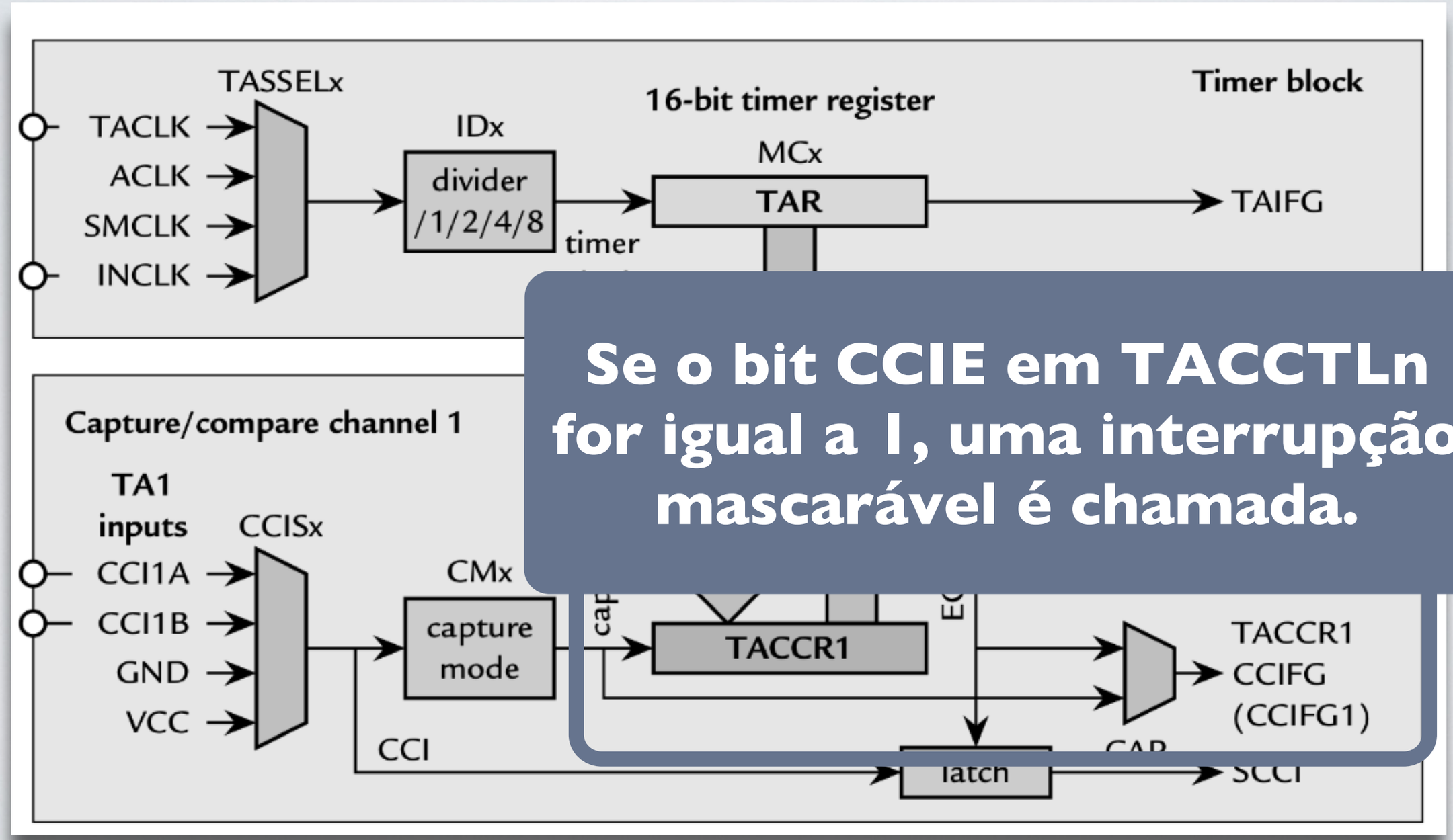
O bit CCI, em TACCTLn, reflete o estado da entrada do módulo de captura.

CAPTURA



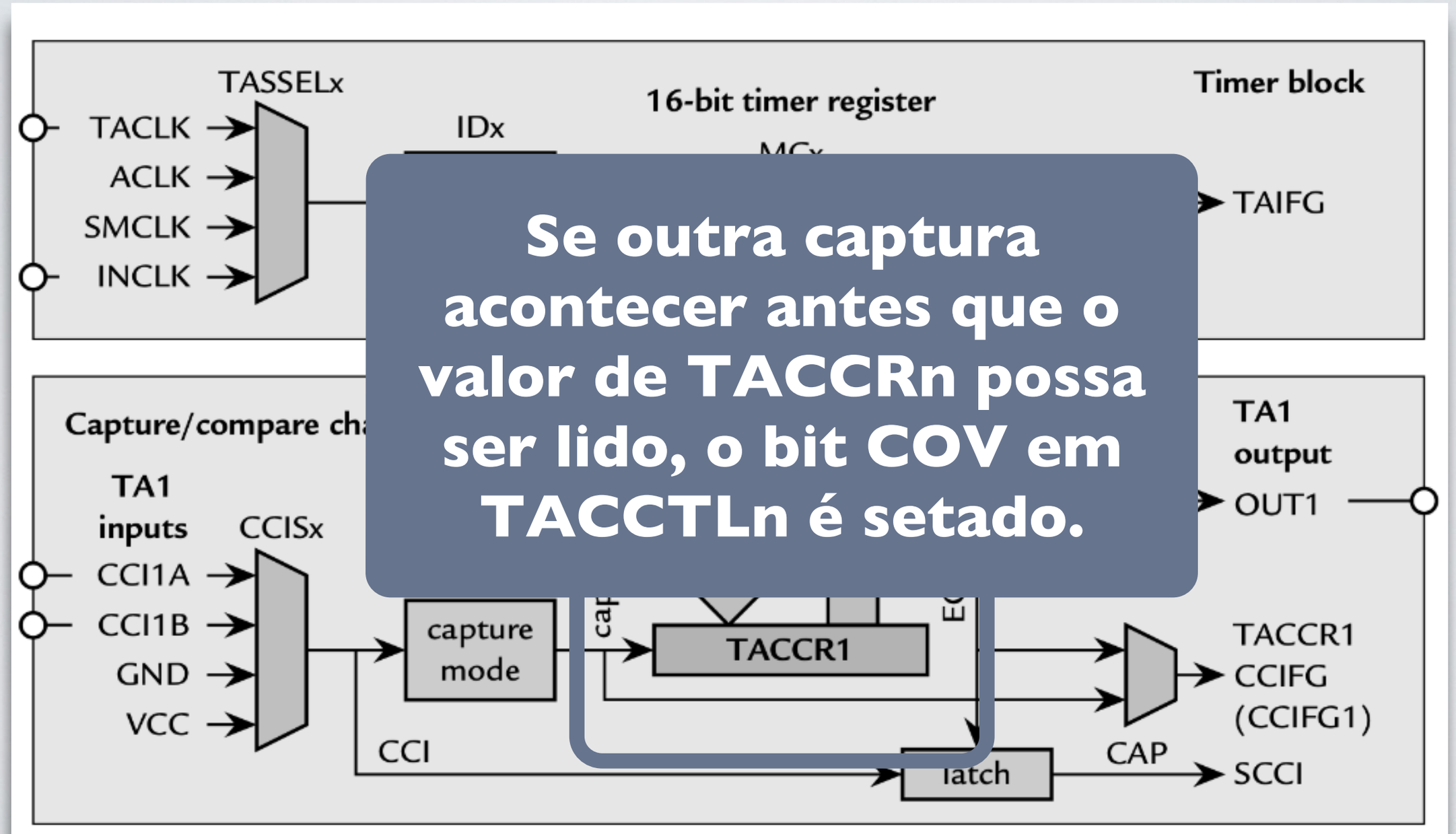
Quando ocorre um evento, o valor de TAR é guardado em TACCRn, e a flag CCIFGn em TACCTLn é setada.

CAPTURA



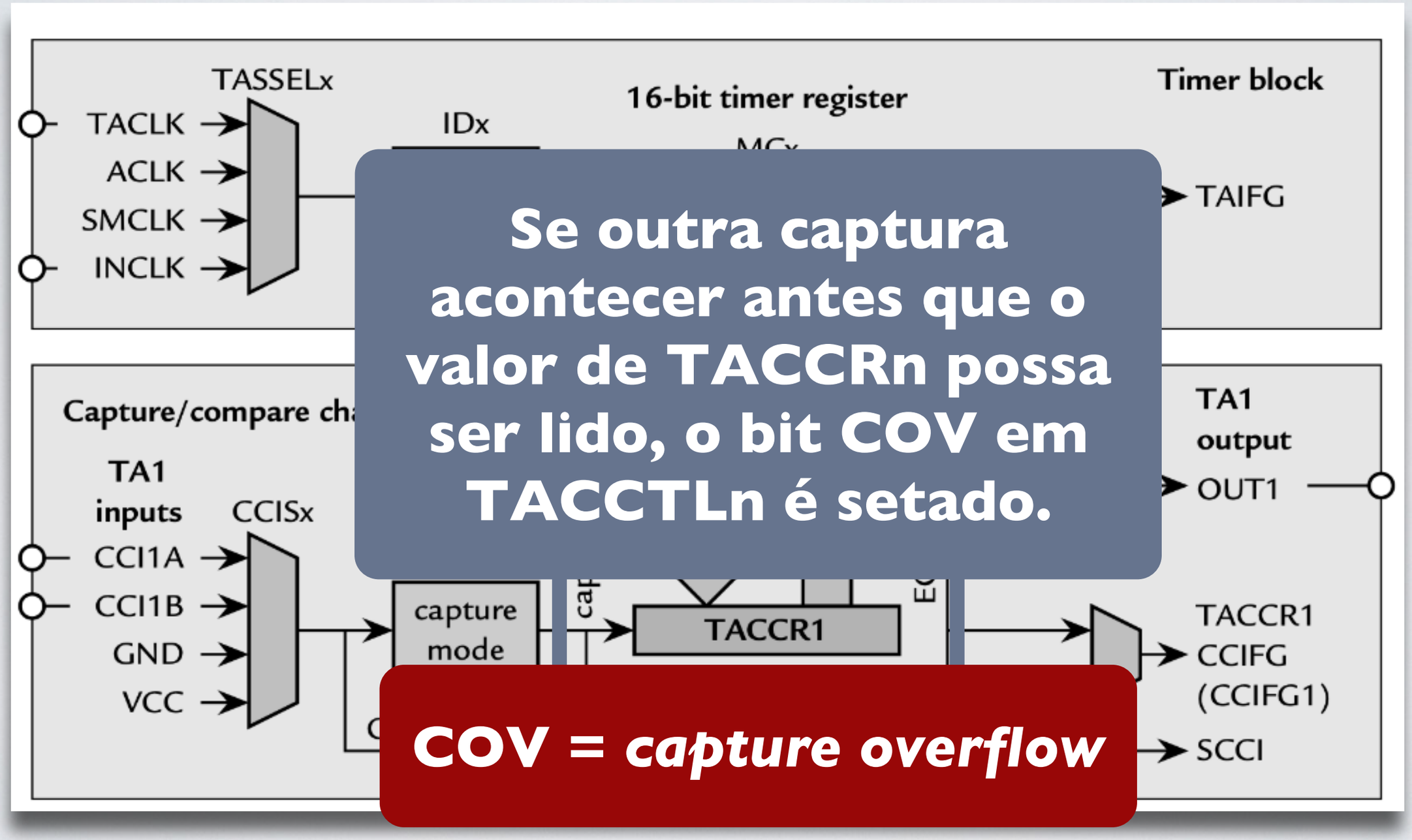
Se o bit CCIE em TACCTLn for igual a 1, uma interrupção mascarável é chamada.

CAPTURA



Se outra captura acontecer antes que o valor de TACCRn possa ser lido, o bit COV em TACCTLn é setado.

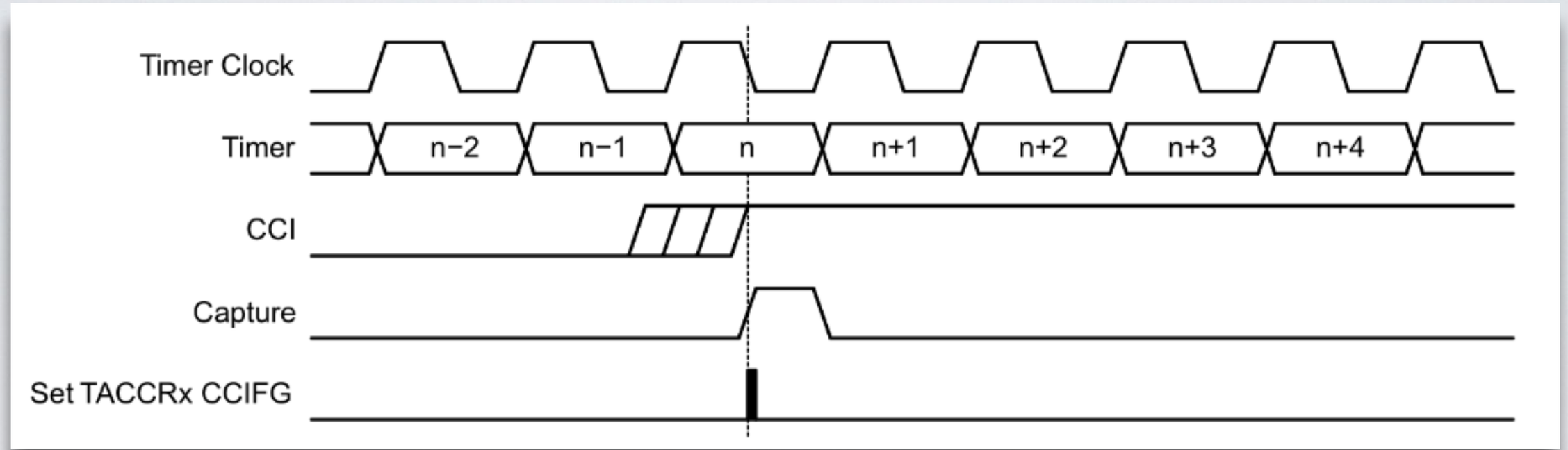
CAPTURA



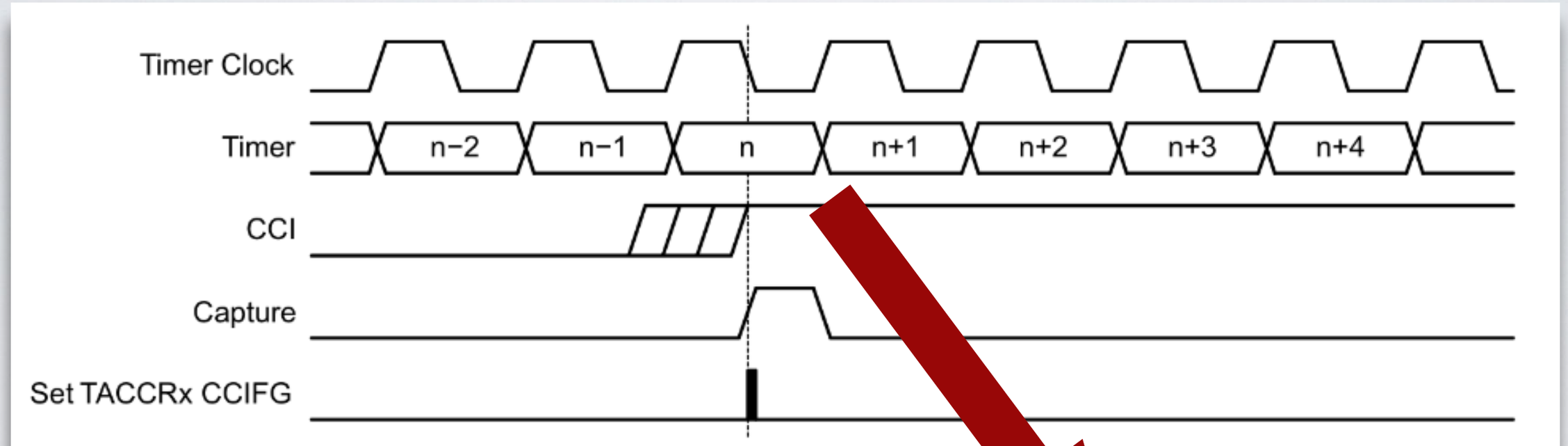
Se outra captura acontecer antes que o valor de TACCRn possa ser lido, o bit COV em TACCTLn é setado.

COV = *capture overflow*

CAPTURA

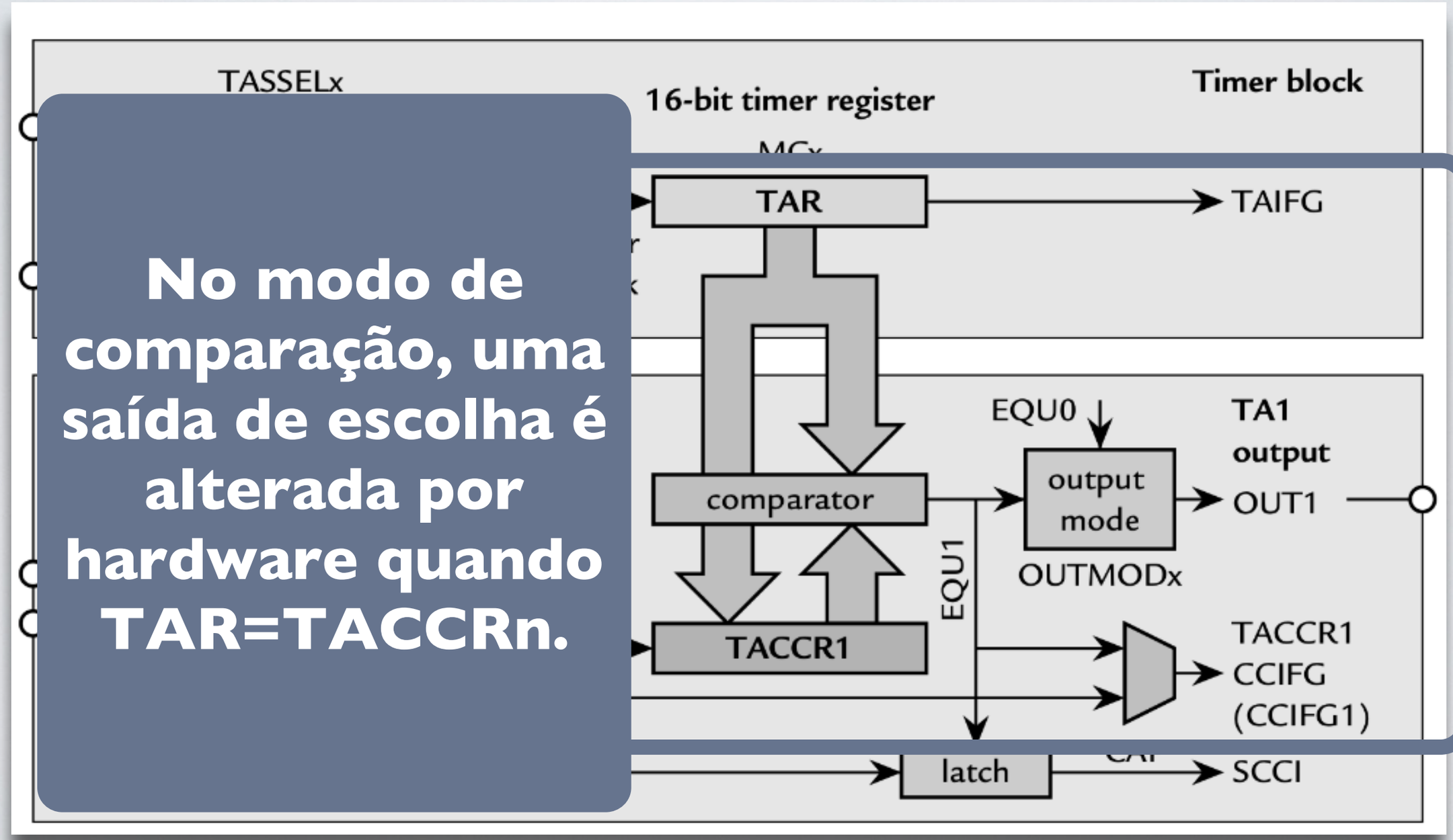

Timer Clock
Timer
n−2
n−1
n
n+1
n+2
n+3
n+4
CCI
Capture
Set TACCRx CCIFG

CAPTURA



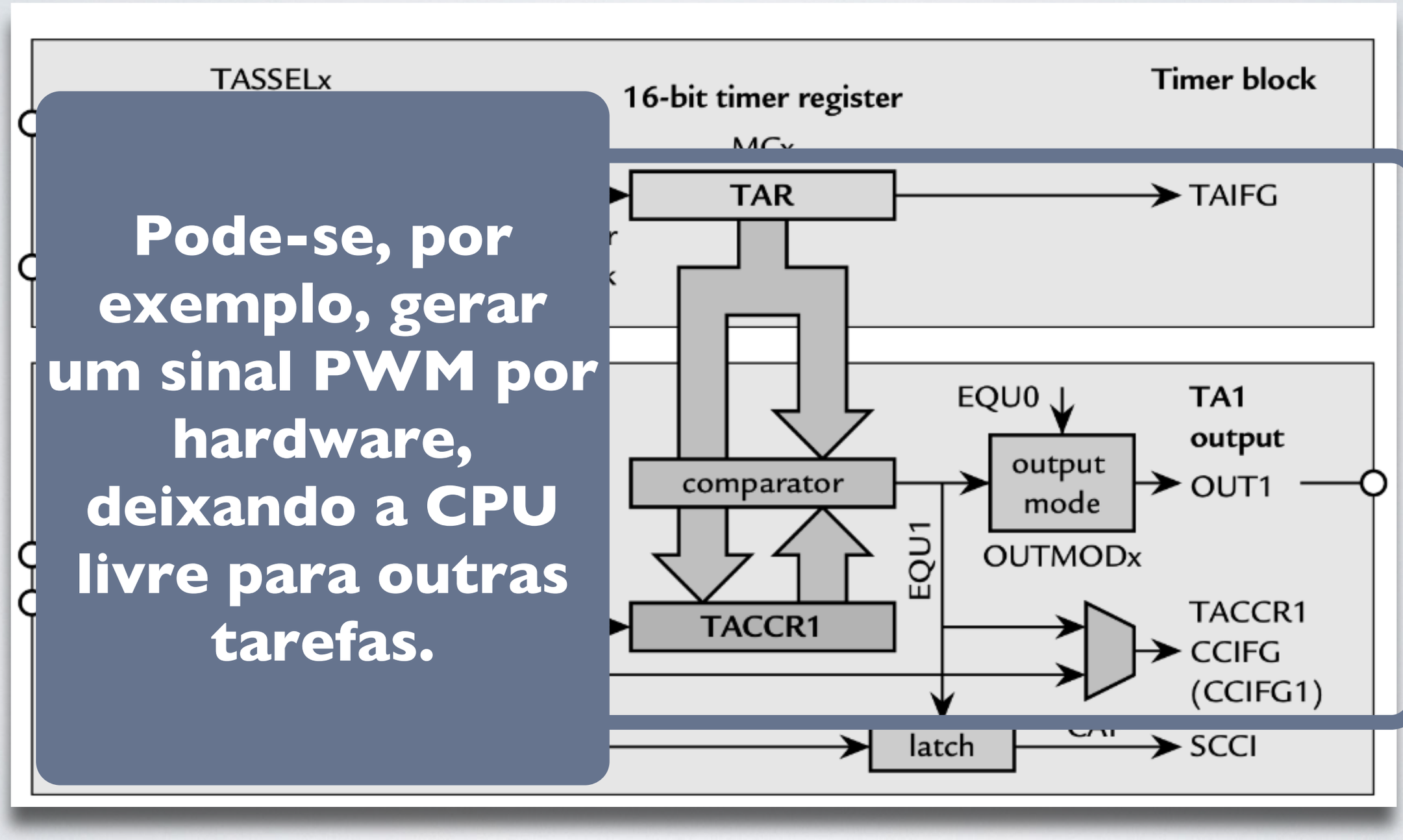
TACCRx = n

COMPARAÇÃO

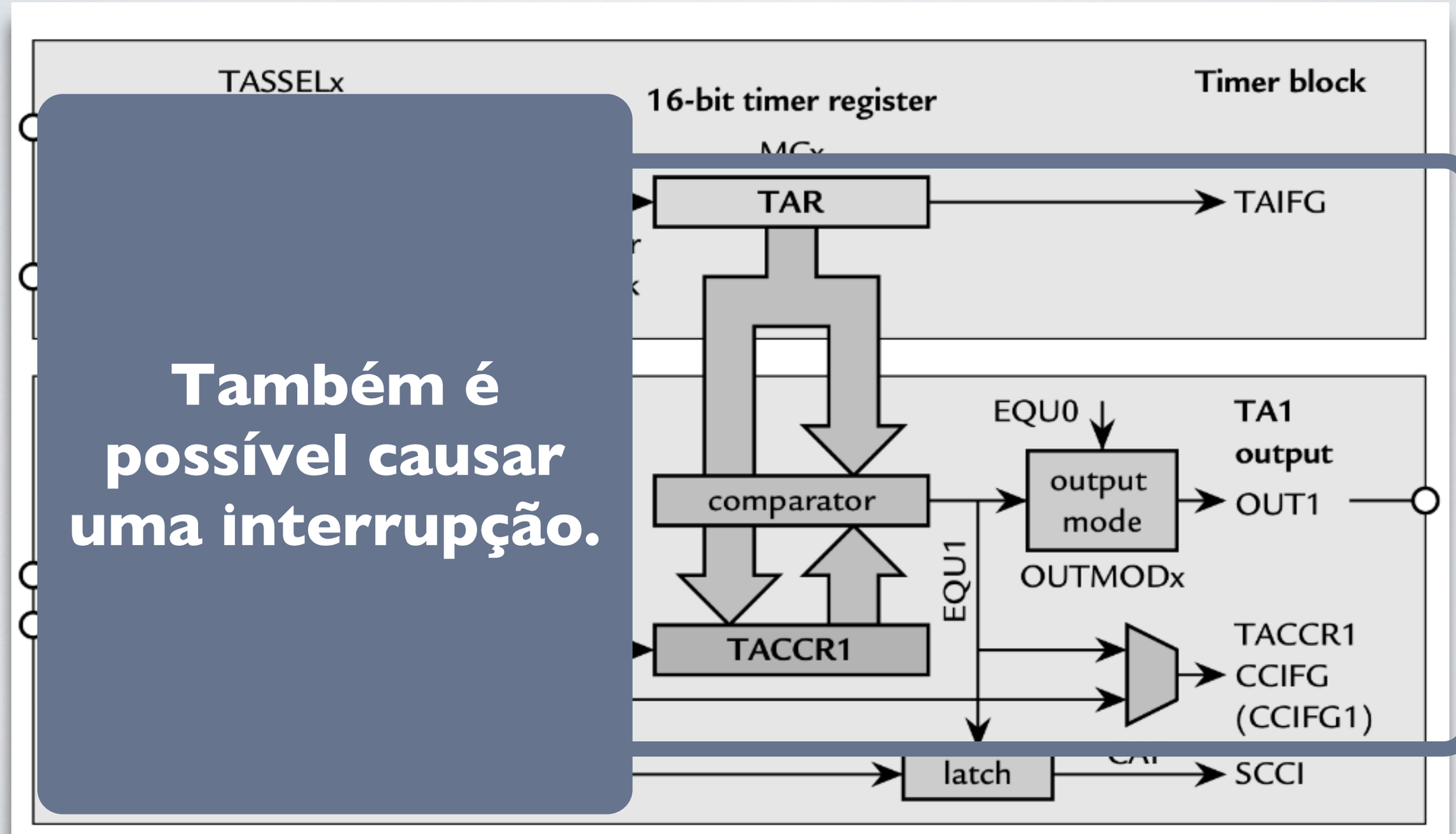


No modo de comparação, uma saída de escolha é alterada por hardware quando TAR=TACCRn.

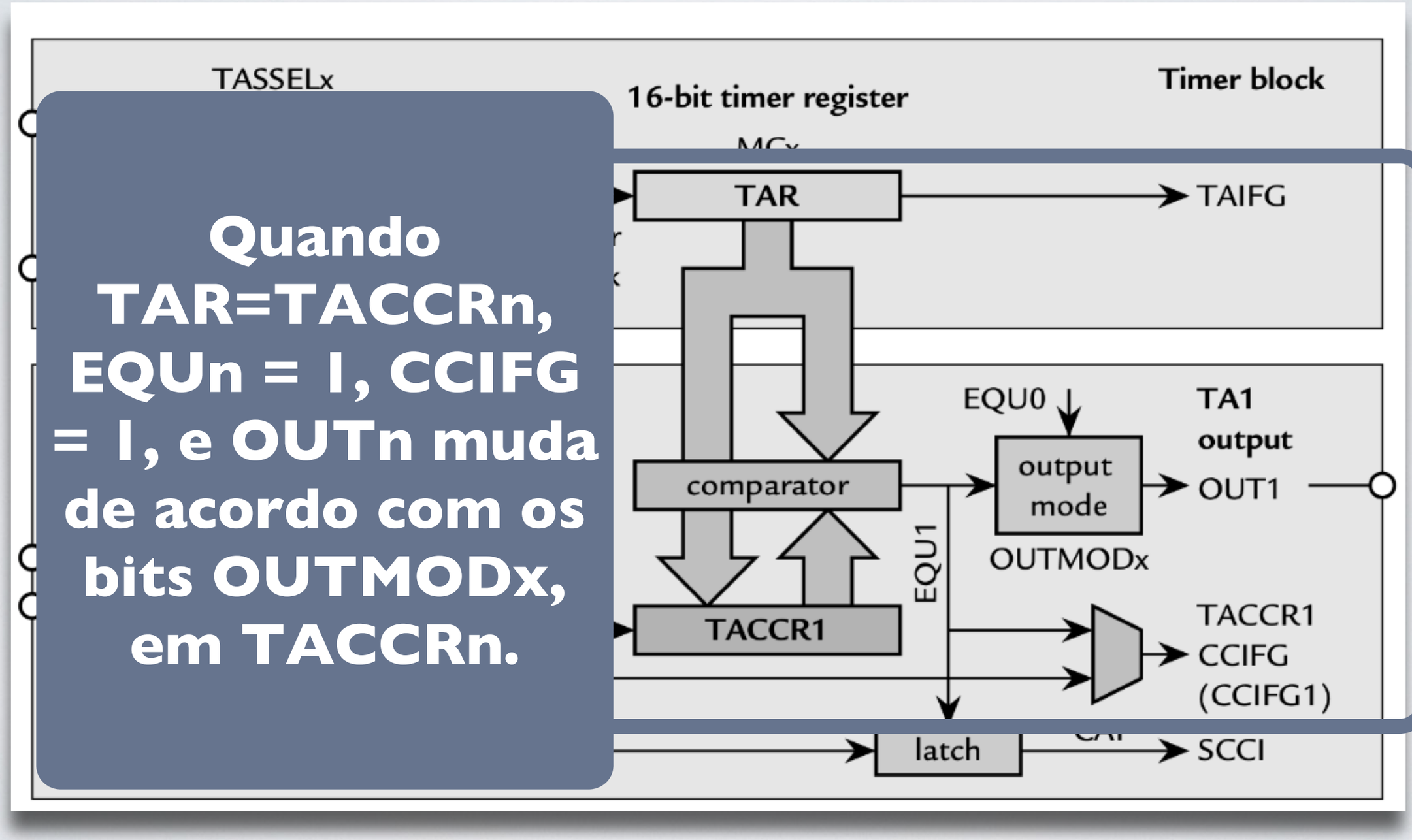
COMPARAÇÃO


TASSELx
16-bit timer register
Timer block
MCx
TAR
TAIFG
comparator
EQU0
TA1
output
output
mode
OUT1
OUTMODx
EQU1
TACCR1
TACCR1
CCIFG
(CCIFG1)
latch
SCCI
Pode-se, por exemplo, gerar um sinal PWM por hardware, deixando a CPU livre para outras tarefas.

COMPARAÇÃO

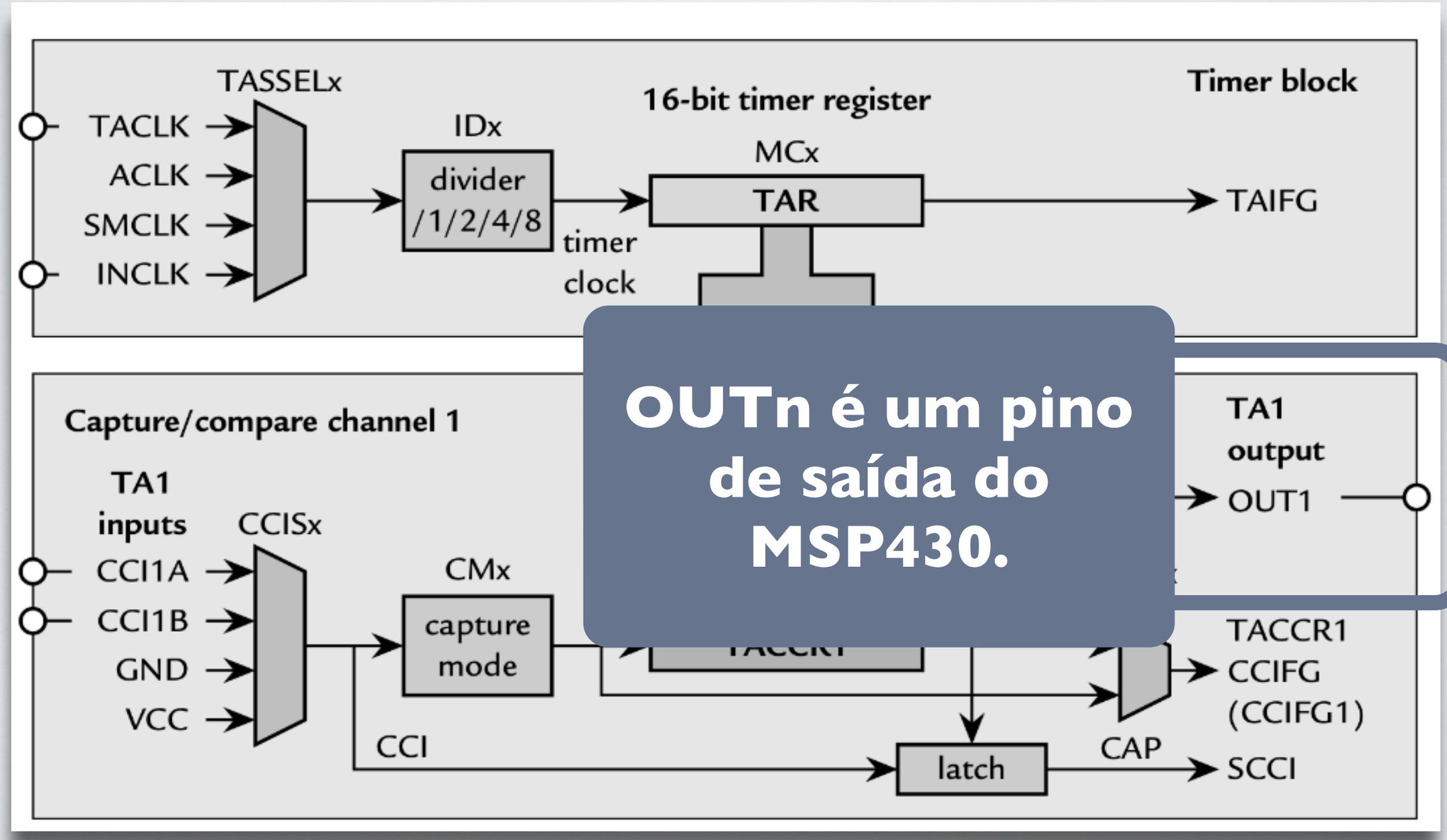

TASSELx
16-bit timer register
Timer block
MCx
TAR
TAIFG
EQU0
TA1
output
output mode
OUT1
comparator
OUTMODx
EQU1
TACCR1
TACCR1
CCIFG
(CCIFG1)
latch
SCCI
Também é possível causar uma interrupção.

COMPARAÇÃO



Quando TAR=TACCRn, EQUn = 1, CCIFG = 1, e OUTn muda de acordo com os bits OUTMODx, em TACCRn.

COMPARAÇÃO


TASSELx
TACLK
ACLK
SMCLK
INCLK
IDx
divider
/1/2/4/8
timer
clock
16-bit timer register
MCx
TAR
Timer block
TAIFG
Capture/compare channel 1
TA1
inputs
CCI1A
CCI1B
GND
VCC
CCISx
CMx
capture
mode
CCI
latch
CAP
TACCR1
CCIFG
(CCIFG1)
SCCI
TA1
output
OUT1
OUTn é um pino de saída do MSP430.

COMPARAÇÃO

OUTMODx	Modo	Descrição
OOO	Output	OUTn muda de acordo com o bit OUT em TACCTLn. O mesmo que usar uma porta de I/O.
OOI	Set	OUTn é setado quando TAR=TACCRn. Não é zerado posteriormente.
OIO	Toggle/ reset	OUTn é invertido quando TAR=TACCRn, e zerado quando TAR=TACCR0.
OII	Set/Reset	OUTn é setado quando TAR=TACCRn, e zerado quando TAR=TACCR0.

COMPARAÇÃO

OUTMODx	**Modo**	**Descrição**
100	Toggle	OUTn é invertido quando TAR=TACCRn, dobrando o período do sinal de saída.
101	Reset	OUTn é zerado quando TAR=TACCRn. Não é setado posteriormente.
110	Toggle/ set	OUTn é invertido quando TAR=TACCRn, e setado quando TAR=TACCR0.
111	Reset/set	OUTn é zerado quando TAR=TACCRn, e setado quando TAR=TACCR0.

COMPARAÇÃO

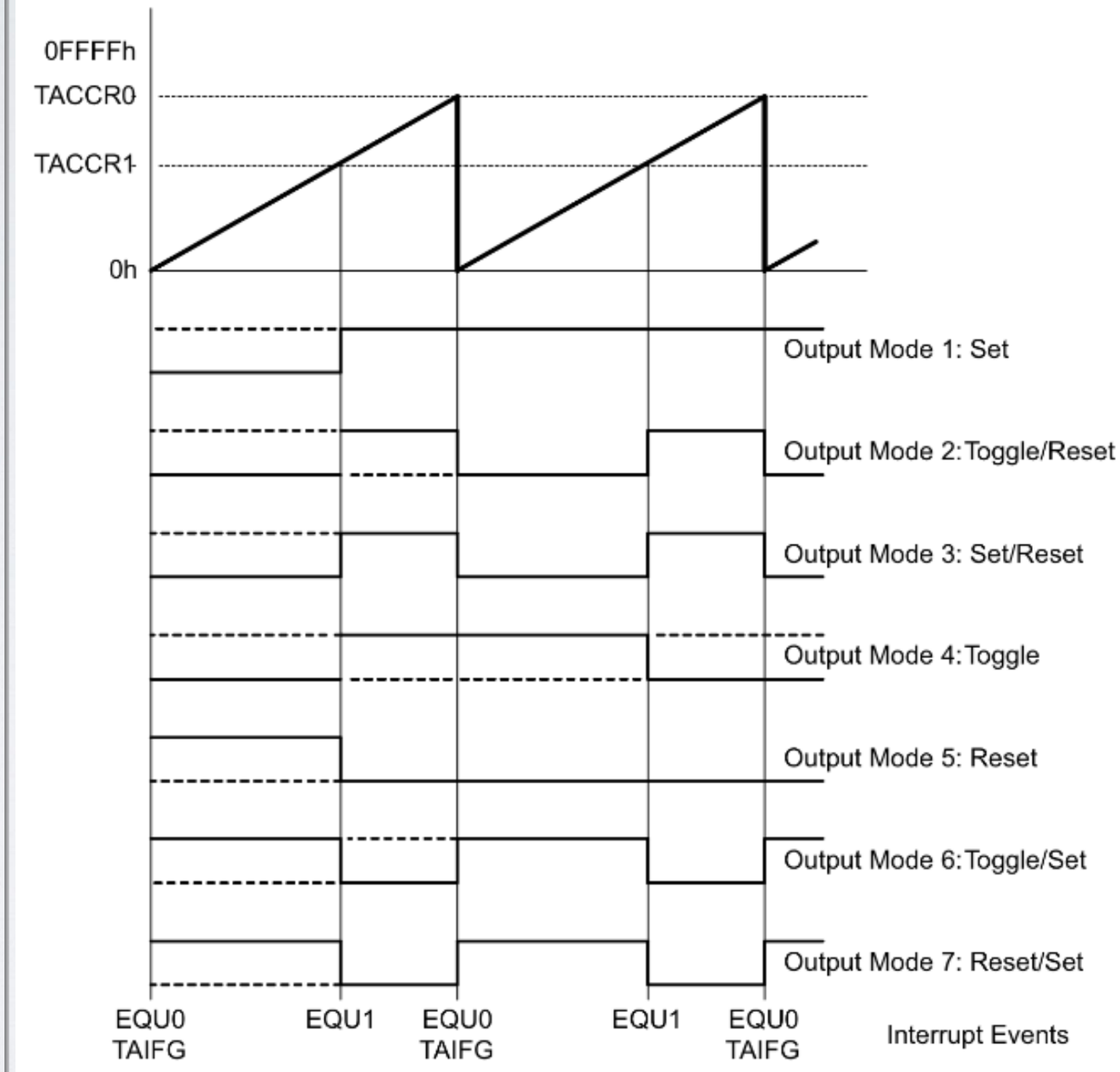


Figure 12-12. Output Example—Timer in Up Mode

COMPARAÇÃO

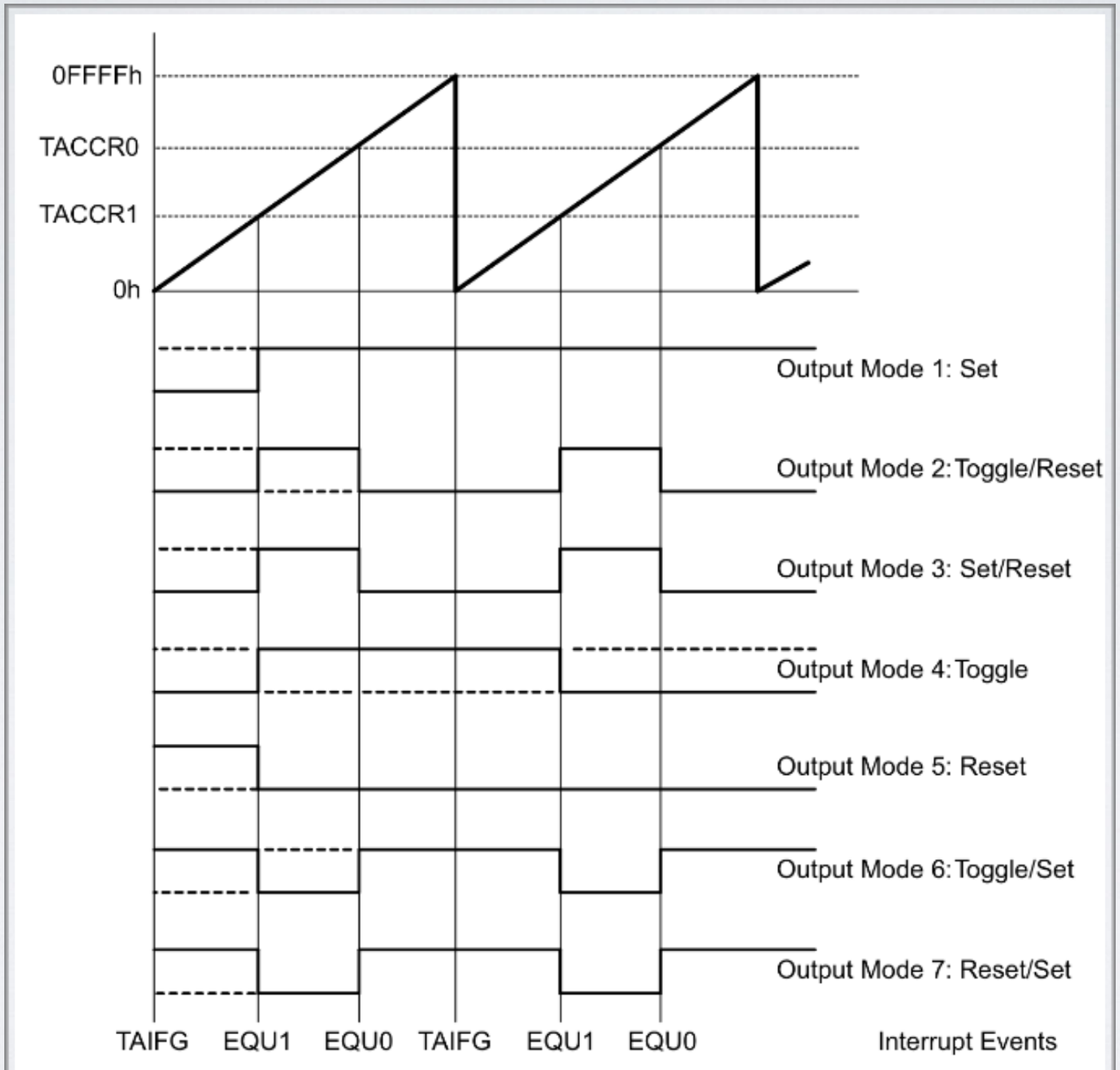


Figure 12-13. Output Example—Timer in Continuous Mode

COMPARAÇÃO

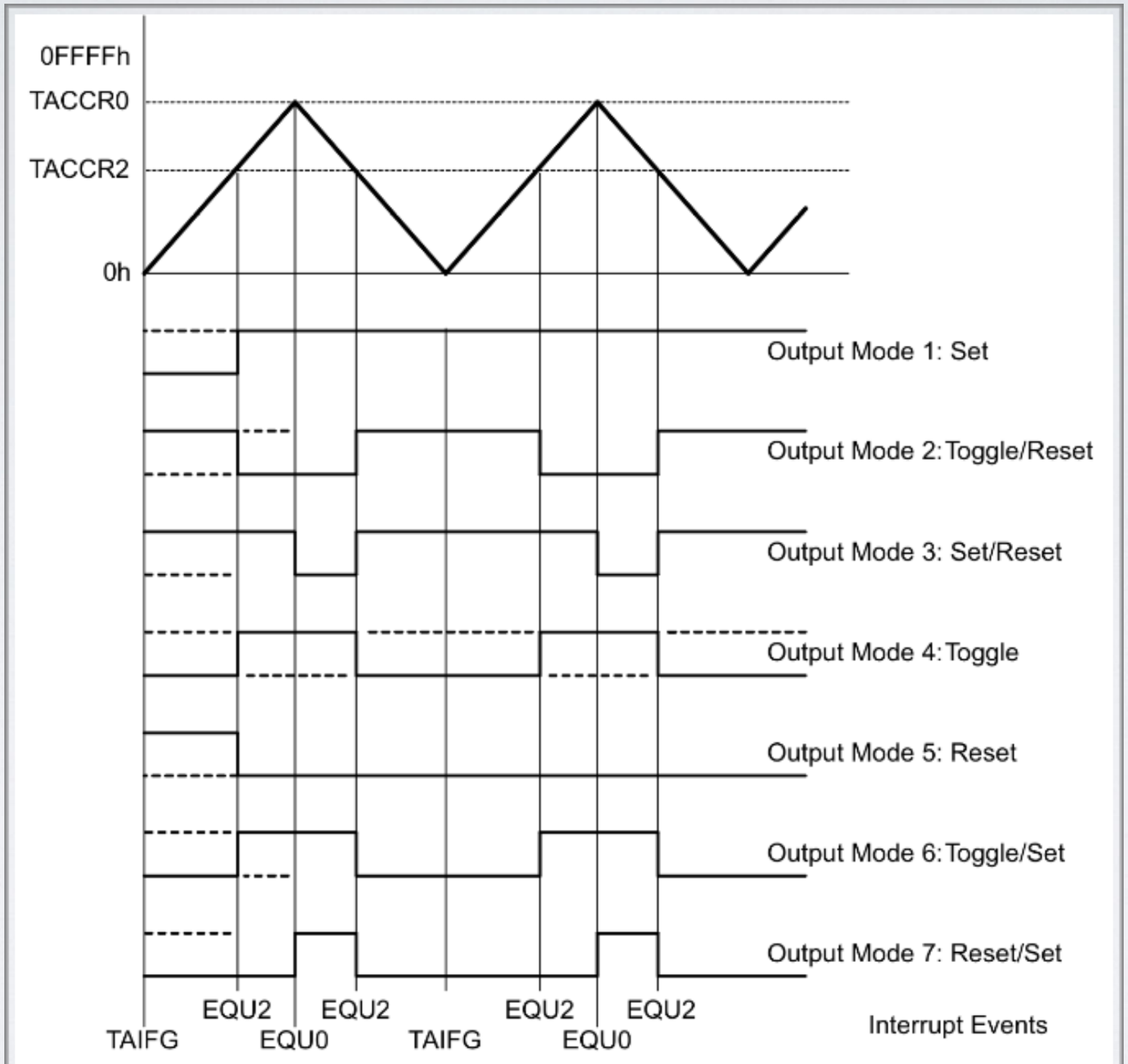


Figure 12-14. Output Example—Timer in Up/Down Mode

COMPARAÇÃO

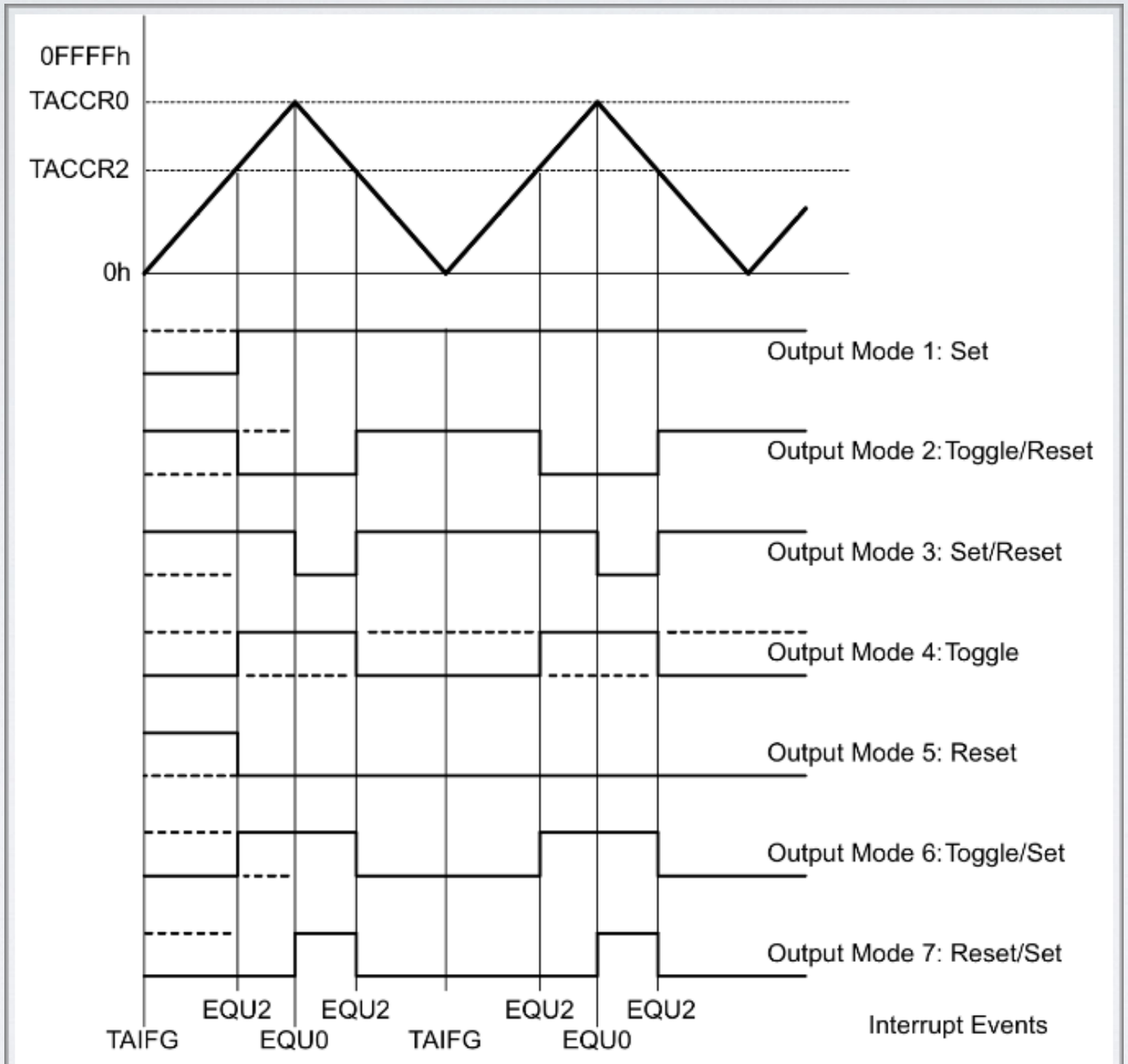


Figure 12-14. Output Example—Timer in Up/Down Mode

INTERRUPÇÕES

Timer_A pode gerar interrupções:

- quando TAR=0;
- nos canais de captura, por mudança no sinal de entrada;
- nos canais de comparação, quando TAR = TACCRn.

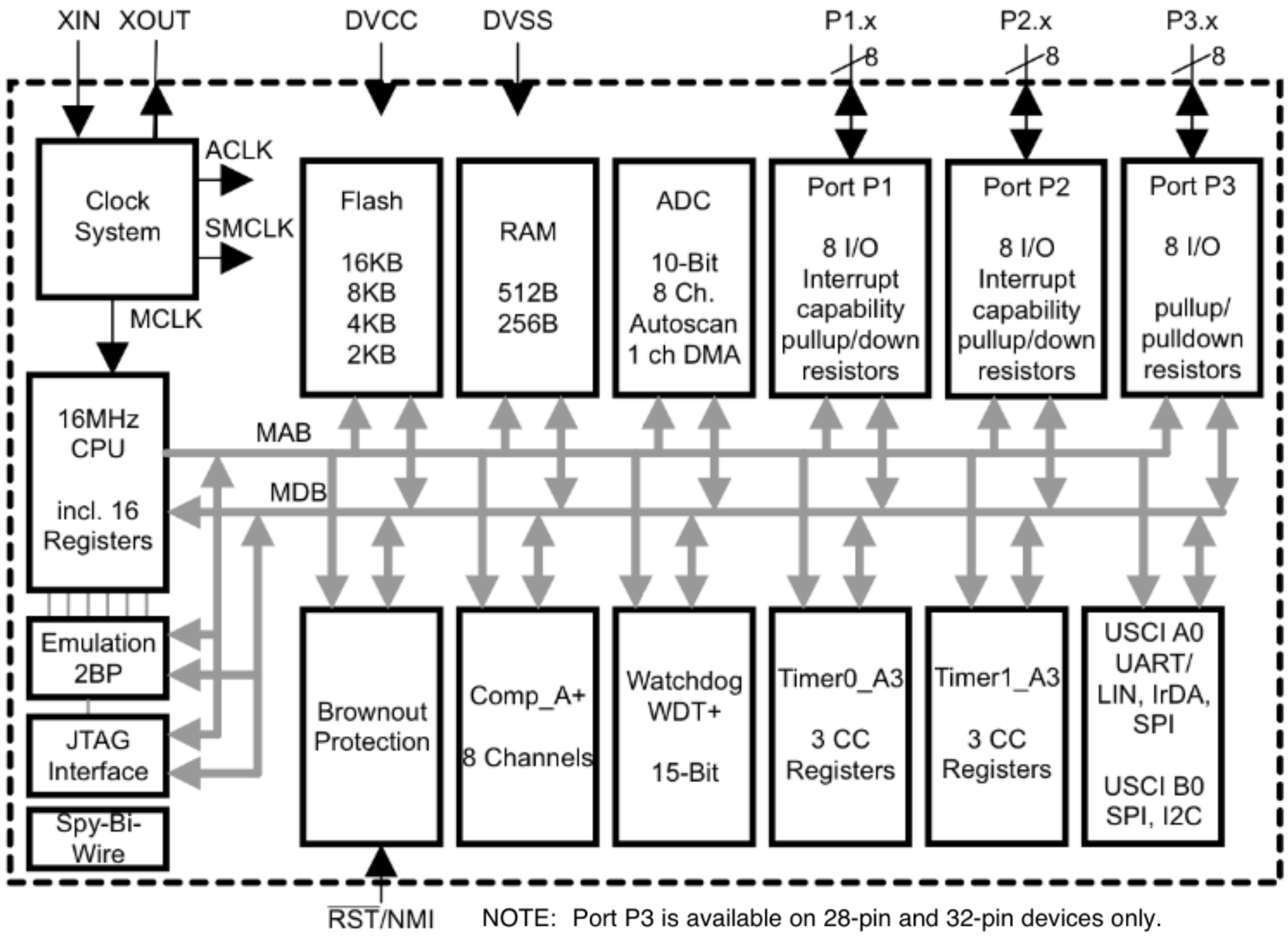
INTERRUPÇÕES

Pode-se diferenciar estas fontes de interrupção através do registrador TAIV.

Table 8.3: Interrupt vector register TAIV for Timer_A3.

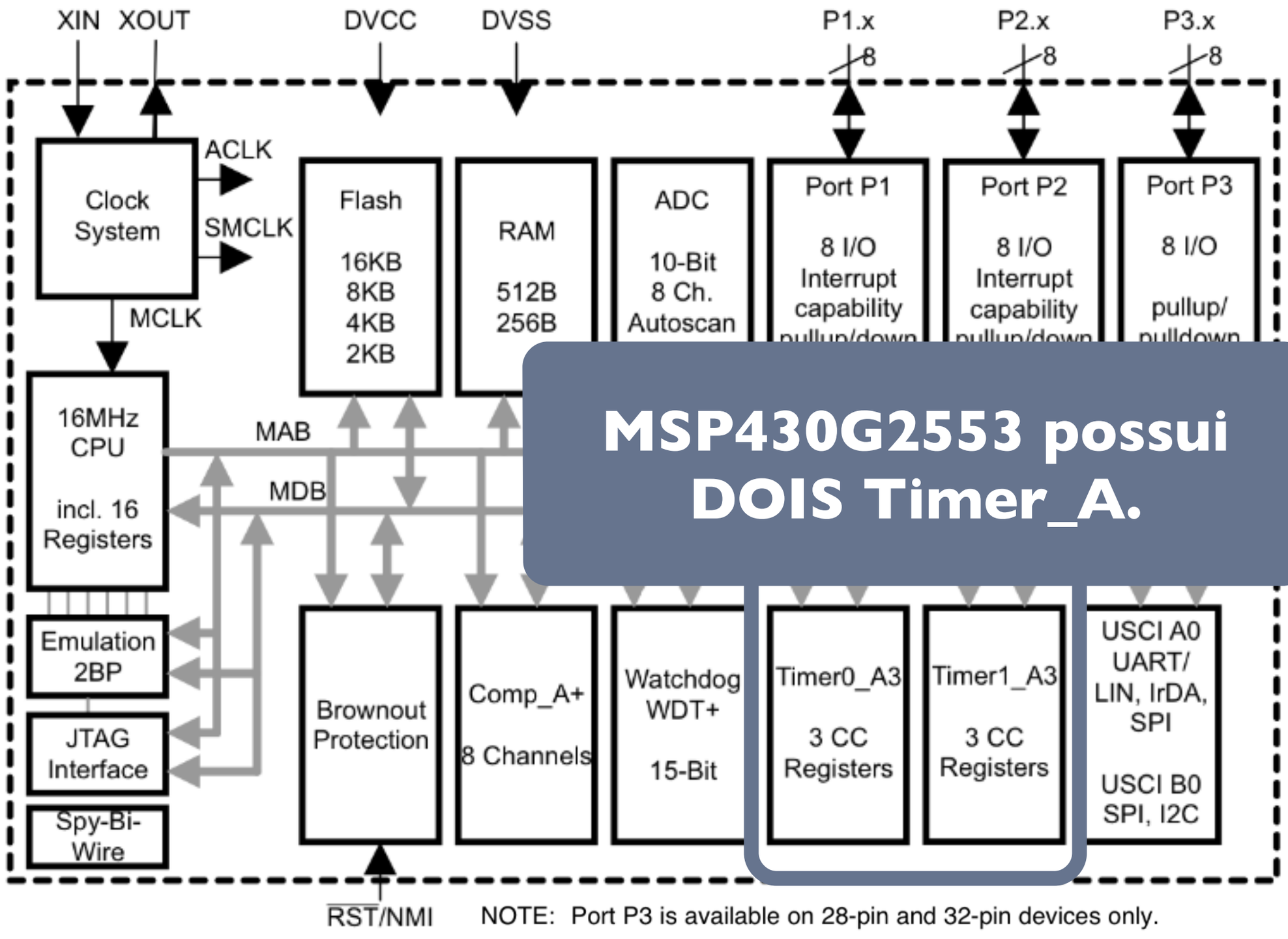
TAIV contents	Source	Flag	Priority
0x0000	No interrupt pending		
0x0002	Capture/compare channel 1	CCIFG1	Highest
0x0004	Capture/compare channel 2	CCIFG2	
0x0006	—		↑
0x0008	—		
0x000A	Timer overflow	TAIFG	Lowest

Functional Block Diagram, MSP430G2x53



NOTE: Port P3 is available on 28-pin and 32-pin devices only.

Functional Block Diagram, MSP430G2x53



MSP430G2553 possui DOIS Timer_A.

Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF8h	28
Comparator_A+	CAIFG(4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (7)			0FFDEh	15
See (8)			0FFDEh to 0FFC0h	14 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
(6) In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
(7) This location is used as bootstrap loader security key (BSLSKEY). A 0xAA55 at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.
(8) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Cada um desses timers tem endereços de interrupção separados.

Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2) (4)	maskable	0FFF8h	28
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24

(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.

Cada um desses timers tem endereços de interrupção separados.

Timer1_A3	TA1CCR0 CCIFG (4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG (2) (4)	maskable	0FFF8h	28

Timer0_A3	TA0CCR0 CCIFG (4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5) (4)	maskable	0FFF0h	24

(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.

Erro no datasheet: devia ser (2) (4)

Table 16. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	CAPD.y
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0CLK/		TA0.TACLK	0	1	0	0	0
ACLK/		ACLK	1	1	0	0	0
A0[2]/		A0	X	X	X	1 (y = 0)	0
CA0/		CA0	X	X	X	0	1 (y = 0)
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.1/	1	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.0/		TA0.0	1	1	0	0	0
		TA0.CCI0A	0	1	0	0	0
UCA0RXD/		UCA0RXD	from USCI	1	1	0	0
UCA0SOMI/		UCA0SOMI	from USCI	1	1	0	0
A1[2]/		A1	X	X	X	1 (y = 1)	0
CA1/		CA1	X	X	X	0	1 (y = 1)
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0
		TA0.CCI1A	0	1	0	0	0
UCA0TXD/		UCA0TXD	from USCI	1	1	0	0
UCA0SIMO/		UCA0SIMO	from USCI	1	1	0	0
A2[2]/		A2	X	X	X	1 (y = 2)	0
CA2/		CA2	X	X	X	0	1 (y = 2)
Pin Osc		Capacitive sensing	X	0	1	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Table 16. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	CAPD.y
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0CLK/		TA0.TACLK	0	1	0	0	0
ACLK/		ACLK	1	1	0	0	0
A0[2]/		A0	X	X	X	1 (y = 0)	0
CA0/		CA0	X	X	X	0	1 (y = 0)
Pin Osc		Capacitive sensing	X	0	1	0	0
						0	0
						0	0
						0	0
						0	0
						0	0
						1 (y = 1)	0
						0	1 (y = 1)
						0	0
						0	0
						0	0
		TA0.CCI1A	0	1	0	0	0
UCA0TXD/	2	UCA0TXD	from USCI	1	1	0	0
UCA0SIMO/		UCA0SIMO	from USCI	1	1	0	0
A2[2]/		A2	X	X	X	1 (y = 2)	0
CA2/		CA2	X	X	X	0	1 (y = 2)
Pin Osc		Capacitive sensing	X	0	1	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

O pino 2, que corresponde a P1.0, pode ser usado como entrada para o clock do Timer0_A3, fazendo:

P1DIR.0 = 0, P1SEL.0 = 1 e P1SEL2.0 = 0.

Table 16. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	CAPD.y
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0CLK/		TA0.TACLK	0	1	0	0	0
ACLK/		ACLK	1	1	0	0	0
A0[2]/		A0	X	X	X	1 (y = 0)	0
CA0/		CA0	X	X	X	0	1 (y = 0)
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.1/	1	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.0/		TA0.0	1	1	0	0	0
		TA0.CCI0A	0	1	0	0	0
UCA0RXD/		UCA0RXD	from USCI	1	1	0	0
UCA0SOMI/		UCA0SOMI	from USCI	1	1	0	0
A1[2]/		A1	X	X	X	1 (y = 1)	0
CA1/		CA1	X	X	X	0	1 (y = 1)
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0
		TA0.CCI1A	0	1	0	0	0
UCA0TXD/		UCA0TXD	from USCI	1	1	0	0
UCA0SIMO/		UCA0SIMO	from USCI	1	1	0	0
A2[2]/		A2	X	X	X	1 (y = 2)	0
CA2/		CA2	X	X	X	0	1 (y = 2)
Pin Osc		Capacitive sensing	X	0	1	0	0

O pino 3, que corresponde a P1.1, pode ser usado como saída do canal de comparação 0 do Timer0_A3, fazendo:

P1DIR.1 = 1, P1SEL.1 = 1 e P1SEL2.1 = 0.

Table 16. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1 [2]	CAPD.y
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0CLK/		TA0.TACLK	0	1	0	0	0
ACLK/		ACLK	1	1	0	0	0
A0[2]/		A0	X	X	X	1 (y = 0)	0
CA0/		CA0	X	X	X	0	1 (y = 0)
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.1/	1	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.0/		TA0.0	1	1	0	0	0
		TA0.CCI0A	0	1	0	0	0
UCA0RXD/		UCA0RXD	from USCI	1	1	0	0
UCA0SOMI/		UCA0SOMI	from USCI	1	1	0	0
A1[2]/		A1	X	X	X	1 (y = 1)	0
CA1/		CA1	X	X	X	0	1 (y = 1)
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0
		TA0.CCI1A	0	1	0	0	0
UCA0TXD/		UCA0TXD	from USCI	1	1	0	0
UCA0SIMO/		UCA0SIMO	from USCI	1	1	0	0
A2[2]/		A2	X	X	X	1 (y = 2)	0
CA2/		CA2	X	X	X	0	1 (y = 2)
Pin Osc		Capacitive sensing	X	0	1	0	0

O pino 3, que corresponde a P1.1, pode ser usado como entrada do canal de captura 0A do Timer0_A3, fazendo:

P1DIR.1 = 0, P1SEL.1 = 1 e P1SEL2.1 = 0.

Table 16. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	CAPD.y
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0CLK/		TA0.TACLK	0	1	0	0	0
ACLK/		ACLK	1	1	0	0	0
A0[2]/		A0	X	X	X	1 (y = 0)	0
						0	1 (y = 0)
						0	0
						0	0
						0	0
						0	0
						0	0
						1 (y = 1)	0
						0	1 (y = 1)
						0	0
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0
		TA0.CCI1A	0	1	0	0	0
UCA0TXD/		UCA0TXD	from USCI	1	1	0	0
UCA0SIMO/		UCA0SIMO	from USCI	1	1	0	0
A2[2]/		A2	X	X	X	1 (y = 2)	0
CA2/		CA2	X	X	X	0	1 (y = 2)
Pin Osc		Capacitive sensing	X	0	1	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

O pino 4, que corresponde a P1.2, pode ser usado como saída do canal de comparação 1 do Timer0_A3, fazendo:

P1DIR.2 = 1, P1SEL.2 = 1 e P1SEL2.2 = 0.

Table 16. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	CAPD.y
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0CLK/		TA0.TACLK	0	1	0	0	0
ACLK/		ACLK	1	1	0	0	0
A0[2]/		A0	X	X	X	1 (y = 0)	0
						0	1 (y = 0)
						0	0
						0	0
						0	0
						0	0
						0	0
						0	0
						1 (y = 1)	0
						0	1 (y = 1)
						0	0
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0
		TA0.CCI1A	0	1	0	0	0
UCA0TXD/		UCA0TXD	from USCI	1	1	0	0
UCA0SIMO/		UCA0SIMO	from USCI	1	1	0	0
A2[2]/		A2	X	X	X	1 (y = 2)	0
CA2/		CA2	X	X	X	0	1 (y = 2)
Pin Osc		Capacitive sensing	X	0	1	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

O pino 4, que corresponde a P1.2, pode ser usado como entrada do canal de captura 1A do Timer0_A3, fazendo:

P1DIR.2 = 0, P1SEL.2 = 1 e P1SEL2.2 = 0.

Table 18. Port P1 (P1.4) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]					
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	JTAG Mode	CAPD.y
P1.4/	4	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
SMCLK/		SMCLK	1	1	0	0	0	0
UCB0STE/		UCB0STE	from USCI	1	1	0	0	0
UCA0CLK/		UCA0CLK	from USCI	1	1	0	0	0
VREF+[2]/		VREF+	X	X	X	1	0	0
VEREF+[2]/		VEREF+	X	X	X	1	0	0
A4[2]/		A4	X	X	X	1 (y = 4)	0	0
CA4		CA4	X	X	X	0	0	1 (y = 4)
TCK/		TCK	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

E assim por diante.

Table 19. Port P1 (P1.5 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]					
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	JTAG Mode	CAPD.y
P1.5/	5	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
TA0.0/		TA0.0	1	1	0	0	0	0
UCB0CLK/		UCB0CLK	from USCI	1	1	0	0	0
UCA0STE/		UCA0STE	from USCI	1	1	0	0	0
A5[2]/		A5	X	X	X	1 (y = 5)	0	0
CA5		CA5	X	X	X	0	0	1 (y = 5)
TMS		TMS	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0	0
UCB0SOMI/		UCB0SOMI	from USCI	1	1	0	0	0
UCB0SCL/		UCB0SCL	from USCI	1	1	0	0	0
A6[2]/		A6	X	X	X	1 (y = 6)	0	0
CA6		CA6	X	X	X	0	0	1 (y = 6)
TDI/TCLK/		TDI/TCLK	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0
P1.7/	7	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
UCB0SIMO/		UCB0SIMO	from USCI	1	1	0	0	0
UCB0SDA/		UCB0SDA	from USCI	1	1	0	0	0
A7[2]/		A7	X	X	X	1 (y = 7)	0	0
CA7		CA7	X	X	X	0	0	1 (y = 7)
CAOUT		CAOUT	1	1	0	0	0	0
TDO/TDI/		TDO/TDI	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

E assim por diante.

Table 20. Port P2 (P2.0 to P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P2DIR.x	P2SEL.x	P2SEL2.x
P2.0/	0	P2.x (I/O)	I: 0; O: 1	0	0
TA1.0/		Timer1_A3.CCI0A	0	1	0
		Timer1_A3.TA0	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.1/	1	P2.x (I/O)	I: 0; O: 1	0	0
TA1.1/		Timer1_A3.CCI1A	0	1	0
		Timer1_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.2/	2	P2.x (I/O)	I: 0; O: 1	0	0
TA1.1/		Timer1_A3.CCI1B	0	1	0
		Timer1_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.3/	3	P2.x (I/O)	I: 0; O: 1	0	0
TA1.0/		Timer1_A3.CCI0B	0	1	0
		Timer1_A3.TA0	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.4/	4	P2.x (I/O)	I: 0; O: 1	0	0
TA1.2/		Timer1_A3.CCI2A	0	1	0
		Timer1_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.5/	5	P2.x (I/O)	I: 0; O: 1	0	0
TA1.2/		Timer1_A3.CCI2B	0	1	0
		Timer1_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1

(1) X = don't care

E assim por diante.

Table 21. Port P2 (P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P2DIR.x	P2SEL.6 P2SEL.7	P2SEL2.6 P2SEL2.7
XIN	6	XIN	0	1 1	0 0
P2.6		P2.x (I/O)	I: 0; O: 1	0 X	0 0
TA0.1		Timer0_A3.TA1	1	1 0	0 0
Pin Osc		Capacitive sensing	X	0 X	1 X

(1) X = don't care

E assim por diante.