FPGA Signal Processing: Direct Digital Synthesis

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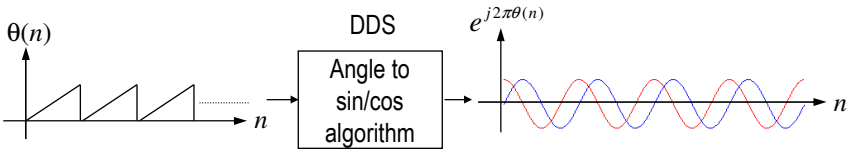
Direct Digital Synthesis (DDS)

- DDS Implementation Options
  - phase truncation DDS
  - CORDIC
  - series expansions
  - phase dithered DDS
  - error feed-forward
  - error feed-back

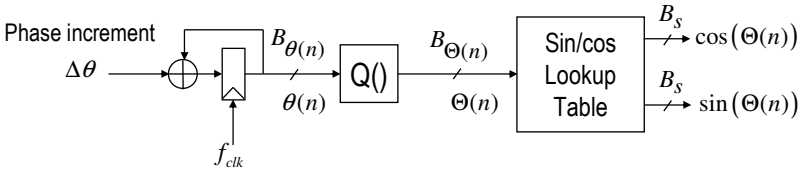


DDS maps a phase slope $\theta(n)$ to a (possible complex) sinusoid

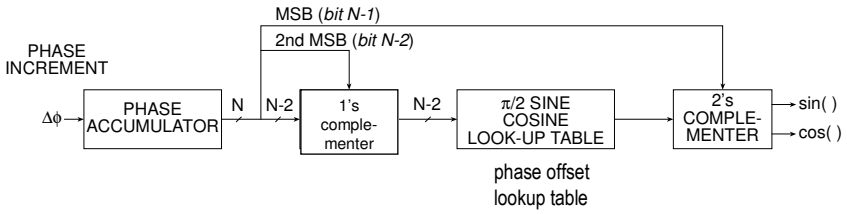
DDS Applications

- Digital receivers
  - digital down converter (DDC)
  - digital up converter (DUC)
  - local oscillator generation in a digital phase locked loop
  - generating an injection frequency (via an DAC) for use with an analog mixer
  - phase & frequency modulators
  - frequency hopping systems

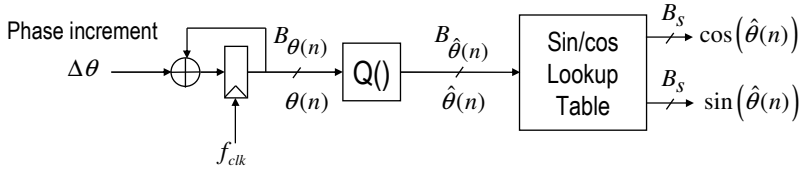
Phase Truncation DDS



DDS with Lookup table compression



DDS Frequency Resolution



$$f_{\text{out}} = \frac{f_{\text{clk}}\Delta\theta}{2^{B_{\theta(n)}}} \text{ Hz}$$

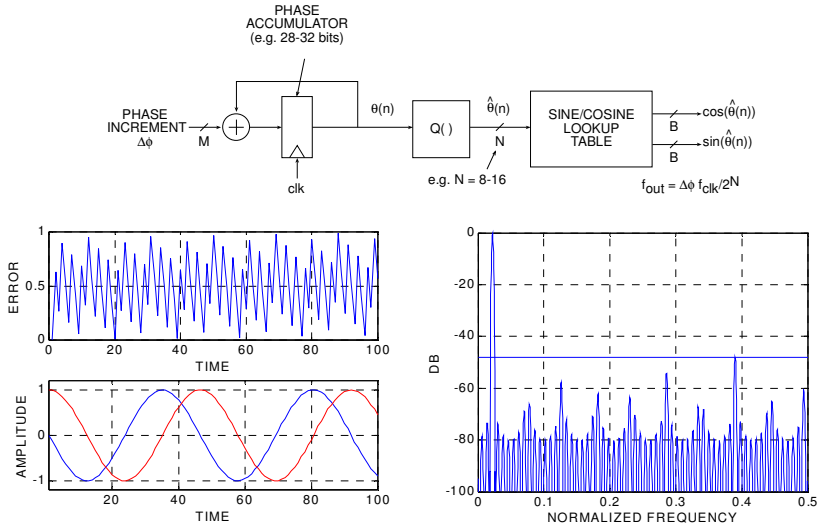
- Accumulator width must support enough precision to span the desired frequency resolution

Frequency resolution: $\Delta f = \frac{f_{clk}}{2^{B_{\theta(n)}}}$

DDS Frequency Resolution

- Example:
  - if the sampling clock is 100 MHz and accumulator width is 32-bits, the frequency resolution is ~0.02 Hz.

Phase Truncation DDS



DDS Noise

- The term contributing to the DDS noise component can be calculated by examining the effect of the phase accumulator quantizer

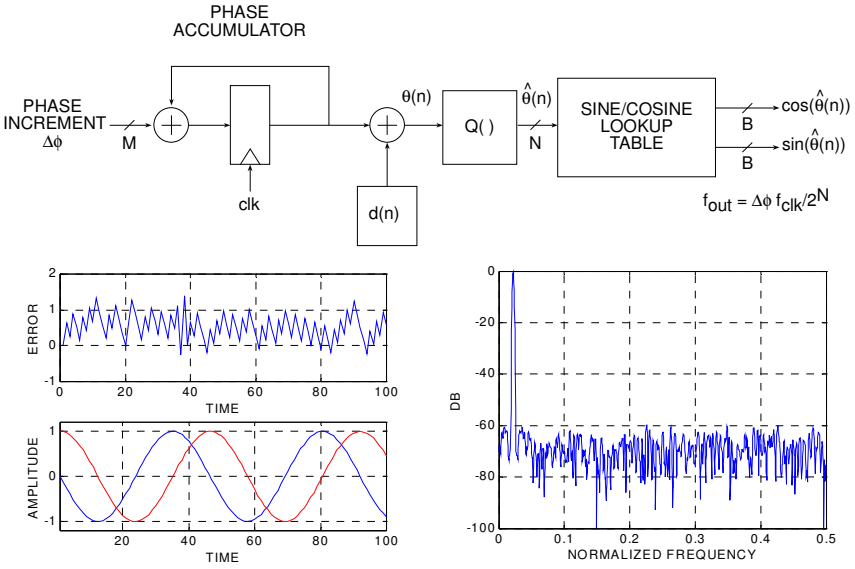
$$\hat{\theta}(n) = \theta(n) + \delta\theta(n)$$

$$e^{j\hat{\theta}(n)} = e^{j[\theta(n)+\delta\theta(n)]} = e^{j\theta(n)} e^{j\delta\theta(n)}$$

$$e^{j\hat{\theta}(n)} \approx e^{j\theta(n)}[1 + j\delta\theta(n)]$$

$$= \underbrace{e^{j\theta(n)}}_{\text{DESIRED COMPONENT}} + \underbrace{j\delta\theta(n)e^{j\theta(n)}}_{\text{UNDESIRED COMPONENT}}$$

Dithered DDS

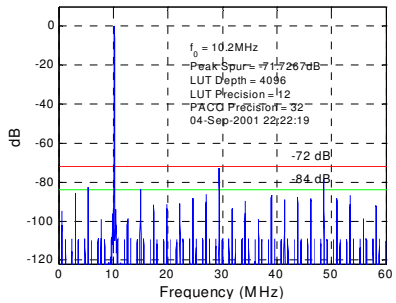


Generating the Dither Sequence

- Generate the dither sequence using *linear feedback shift register structure*

Performance: Single Tone

Dithering Disabled



$f_0 = 10.2$ MHz

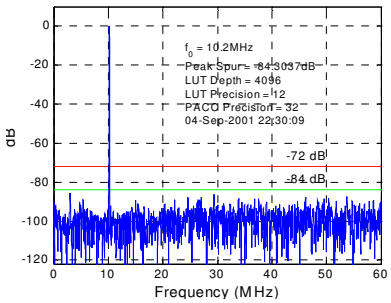
peak spur = -71.73 dB

LUT depth = 4096

LUT precision = 12b

PACC precision = 32b

Dithering Enabled



$f_0 = 10.2$ MHz

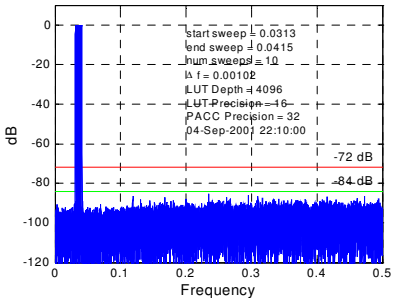
peak spur = -84.30 dB

LUT depth = 4096

LUT precision = 12b

PACC precision = 32b

Performance: Swept Tone



Start sweep = 0.0313

end sweep = 0.0415

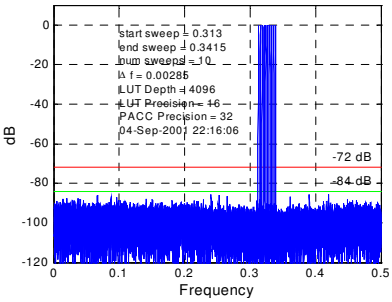
num sweeps = 10

$\Delta f = 0.00102$

LUT depth = 4096

LUT precision = 16b

PACC precision = 32b



Start sweep = 0.313

end sweep = 0.3415

num sweeps = 10

$\Delta f = 0.00285$

LUT depth = 4096

LUT precision = 16b

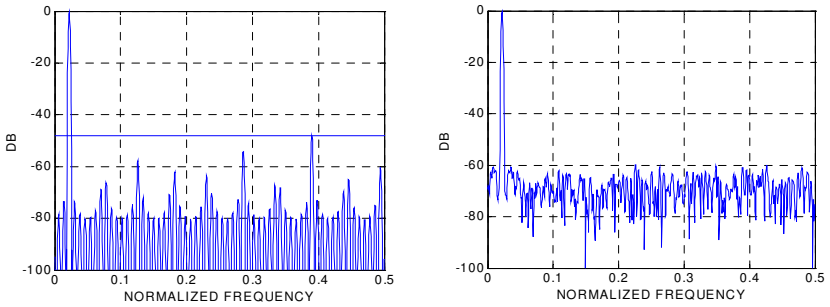
PACC precision = 32b

Implementation - Phase Trunc. DDS

- Phase truncation DDS: SFDR increases at a rate of 6 dB/bit of LUT address
- For modest SFDR requirements phase truncation is an option, e.g. SFDR=48 dB, 256 entry LUT
- Using 1/4-wave symmetry, 64 entry table is needed
- complex DDS employing distributed RAM will require 2 64 entry tables - one for I one for Q
- 10b samples $\Rightarrow$ 20 slices for I and 20 for Q
  - this is ok

Dithered DDS

- Phase dithering will purchase an additional 2 bits of address space



Implementation - Dithered DDS

- Dither signal generator requires only a modest amount of silicon
- can choose to *spend* this optimization in several ways
  - maintain table size and achieve higher spectral purity
  - minimize hardware by using a LUT that is 1/4 the size of that required by a phase truncation design
- This will still be a large amount of FPGA real-estate for high performance applications

Series-Corrected DDS

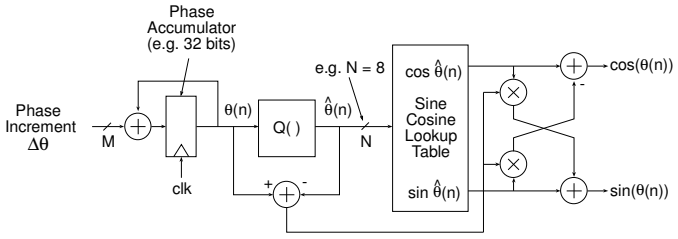
- Taylor series expansion

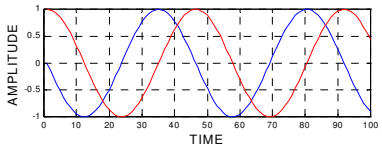
$$f(x) = f(a) + \frac{(x-a)f'(a)}{1!} + \frac{(x-a)^2 f''(a)}{2!} + \cdots \frac{(x-a)^N f^{(N)}(a)}{N!}$$

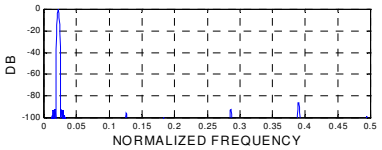
- Consider a two term expansion for $\sin(x)$ and $\cos(x)$

$$\sin(x) = \sin(a) + (x-a)\cos(a)$$
$$\cos(x) = \cos(a) - (x-a)\sin(a)$$

Taylor Series DDS

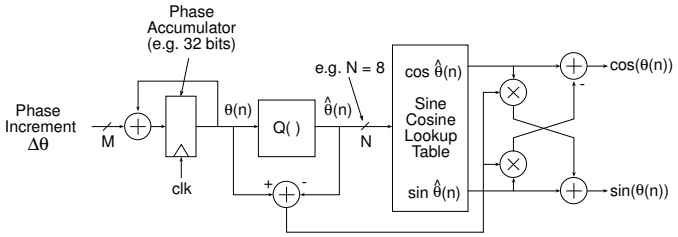






$\{+\cos(\theta(n)), -\sin(\theta(n))\}$

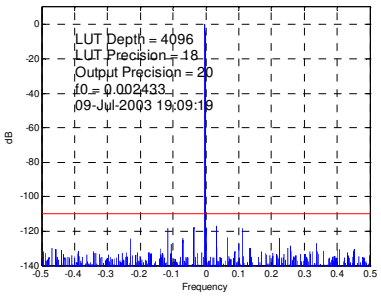
Implementation - Taylor Series DDS

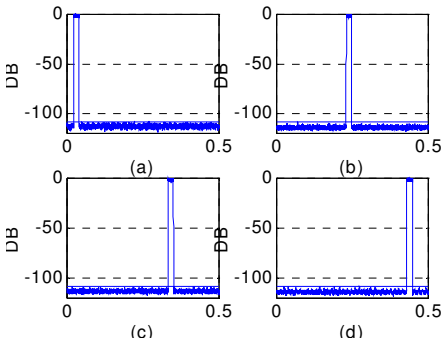


Several arithmetic units required ⇒consider for applications that require very high spur suppression

Virtex-II embedded multipliers well suited to this architecture

Implementation - Taylor Series DDS

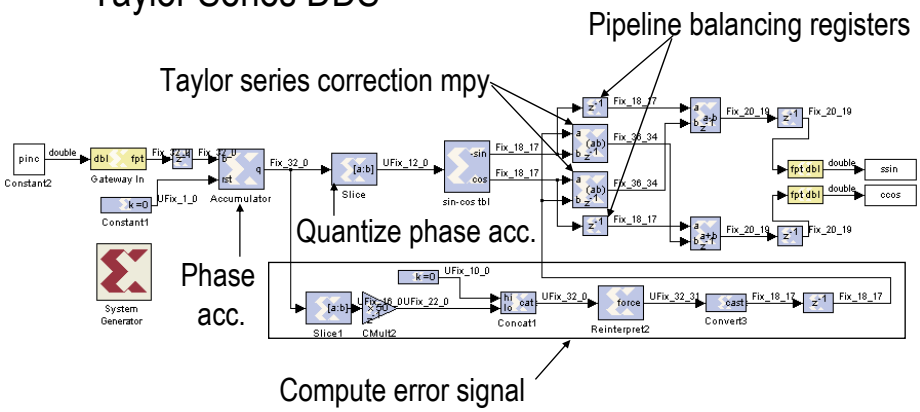




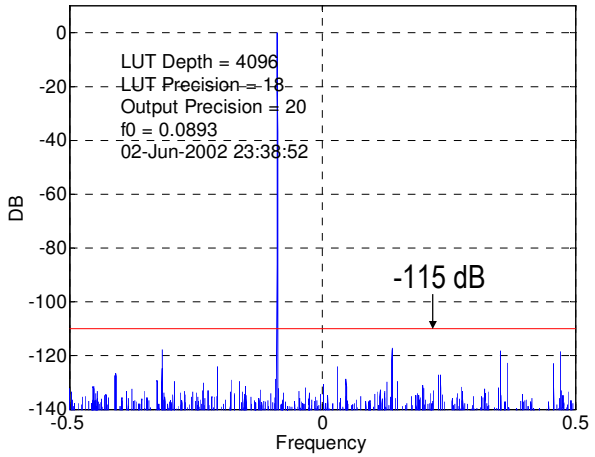
- 1 block RAM
- 2 MPY
- 1 MPY by a constant

System Generator DDS

- Taylor Series DDS



Performance



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Design Statistics

- Tools
  - System Generator v3.1
  - ISE 5.2.03i speedfile: ADVANCED 1.78 2003-05-0
- Device = XC2VP501152-7
- 216 logic slices (3-level pipelined mpys)
- 1 block RAM
- 2 18x18 embedded multipliers
- fclk max = 179 MHz

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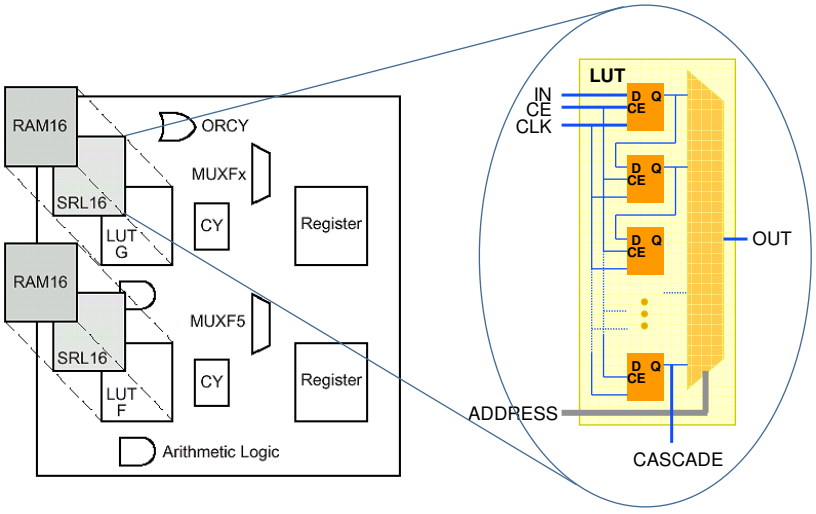
Multi-Channel DDS

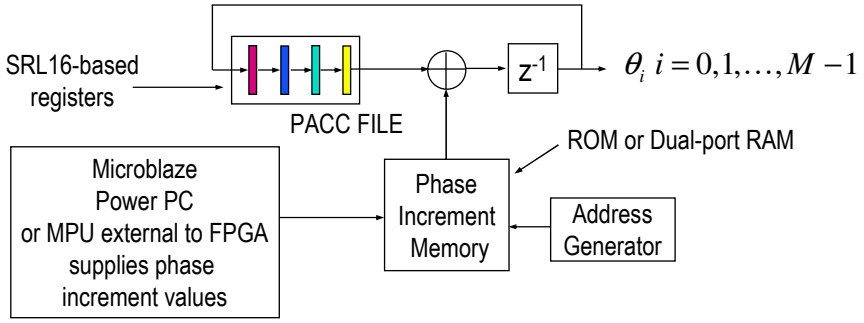
- Build M-channel DDS (M-ary DDS)
- Multi-channel DDS can be constructed for almost the same cost as a single DDS
- Time division multiplex the hardware
- Each DDS operates at 1/M'th the clock rate
- For fclk = 120 MHz and M=3, each DDS will operate at a rate of 40 MHz

Virtex Slice Revision



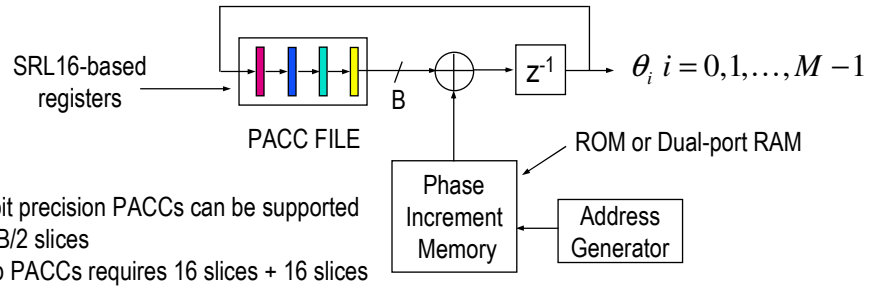
Multi-Channel DDS

- Make use of SRL16s to efficiently implement the M phase accumulators (PACCs)



Multi-Channel DDS

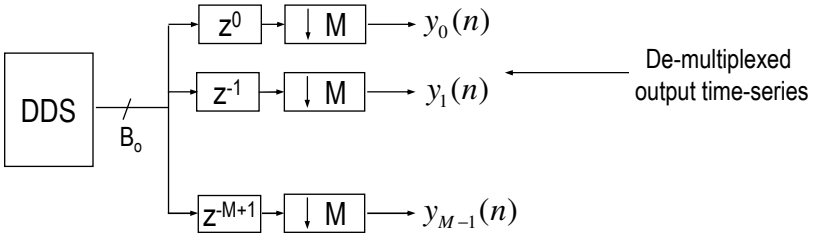
- PACC file is efficiently implemented using the SRL16 slice configuration



16 B-bit precision PACCs can be supported using B/2 slices
16 32b PACCs requires 16 slices + 16 slices for the adder and delay

Multi-Channel DDS

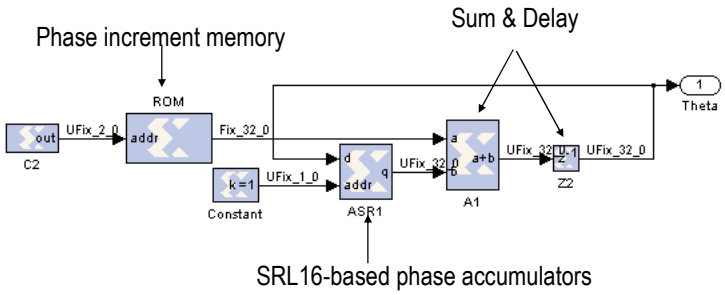
- Small cost to de-multiplex the outputs



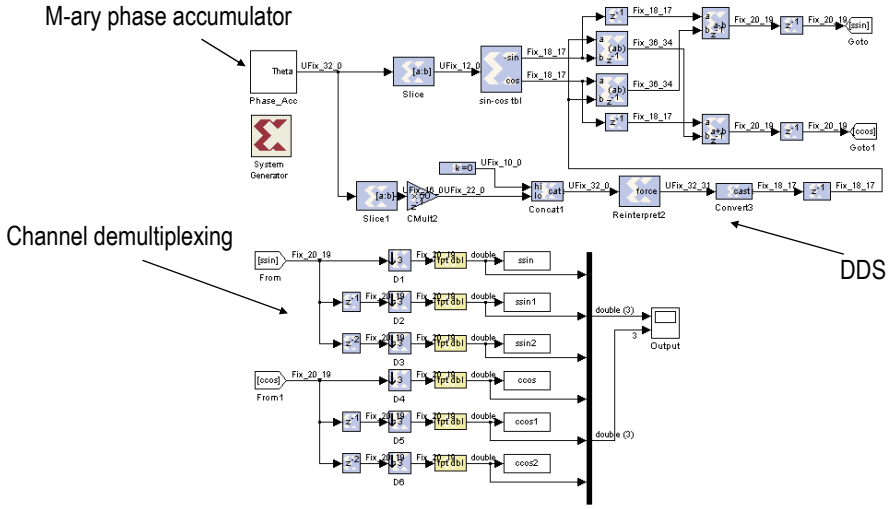
- The cost to demux each B_o-bit output is ~ $B_o/2$ slices

M-ary Phase Accumulator

- In this case the phase increment values are stored in ROM since they are known prior to run-time
- Alternatively dual-port memory could be used of the output frequencies need to be updated at run-time

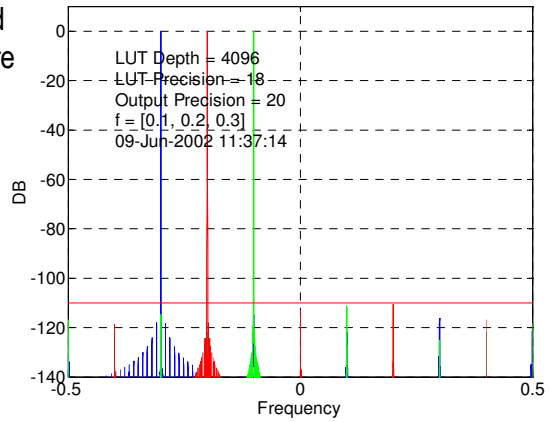


M-ary Taylor Series DDS

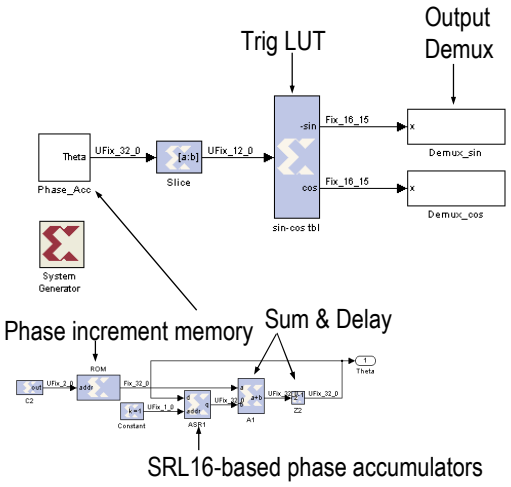


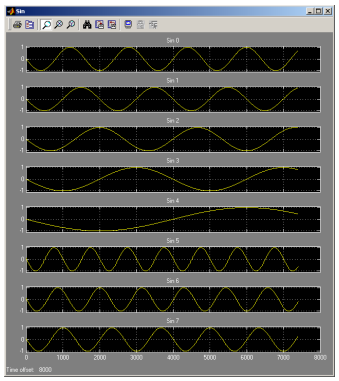
3-Channel Taylor Series DDS

- 3 tones efficiently generated by time sharing the hardware
- Sample-rate versus area tradeoff



M-ary Phase Truncation DDS





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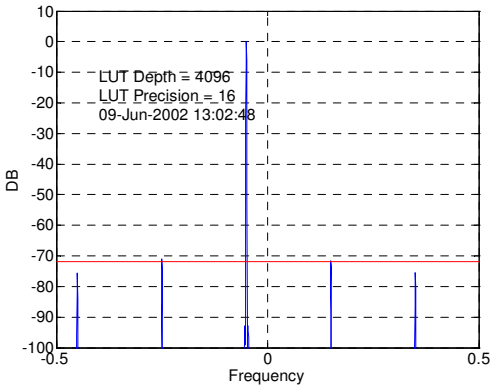
8-Channel Phase Truncation DDS

- 1 demultiplexed output
- Very compact design



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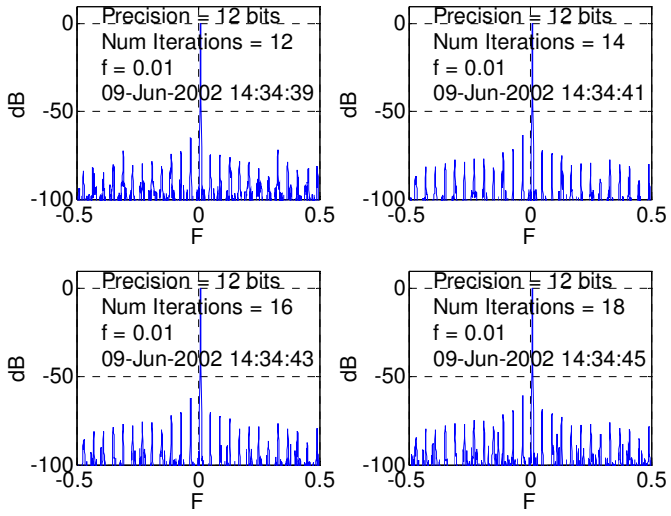
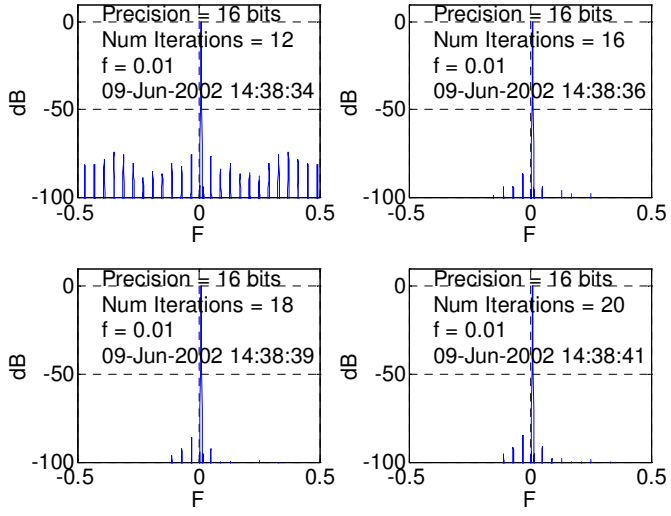
CORDIC DDS



CORDIC DDS



CORDIC DDS