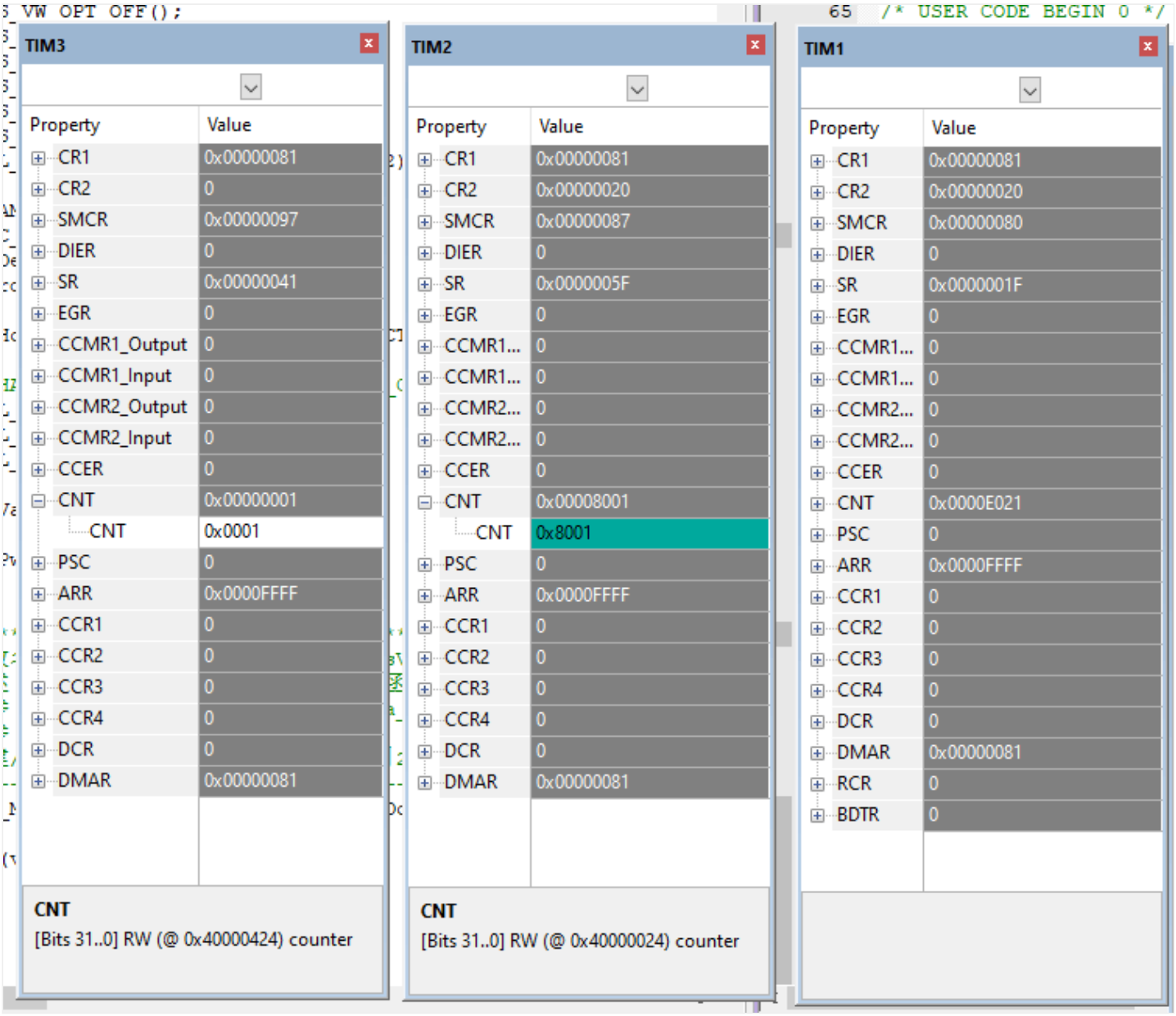
Stm32 timer cascade TIM cascade to form a 32-bit timer

tags: MCU stm32 Embedded Single chip microcomputer

Some low-cost stm32 chips (such as F1 series) do not have a 32-bit timer, and the built-in TIM is 16 bits. When you need to perform some timing content that requires both precision and duration, a 16-bit timer is not enough (72M frequency is directly counted without frequency division, then the 16-bit timer only needs 910us, if it is 32-bit, it needs 59.6s, for some millisecond-level high-precision timing, it is still necessary to use a 32-bit timer.

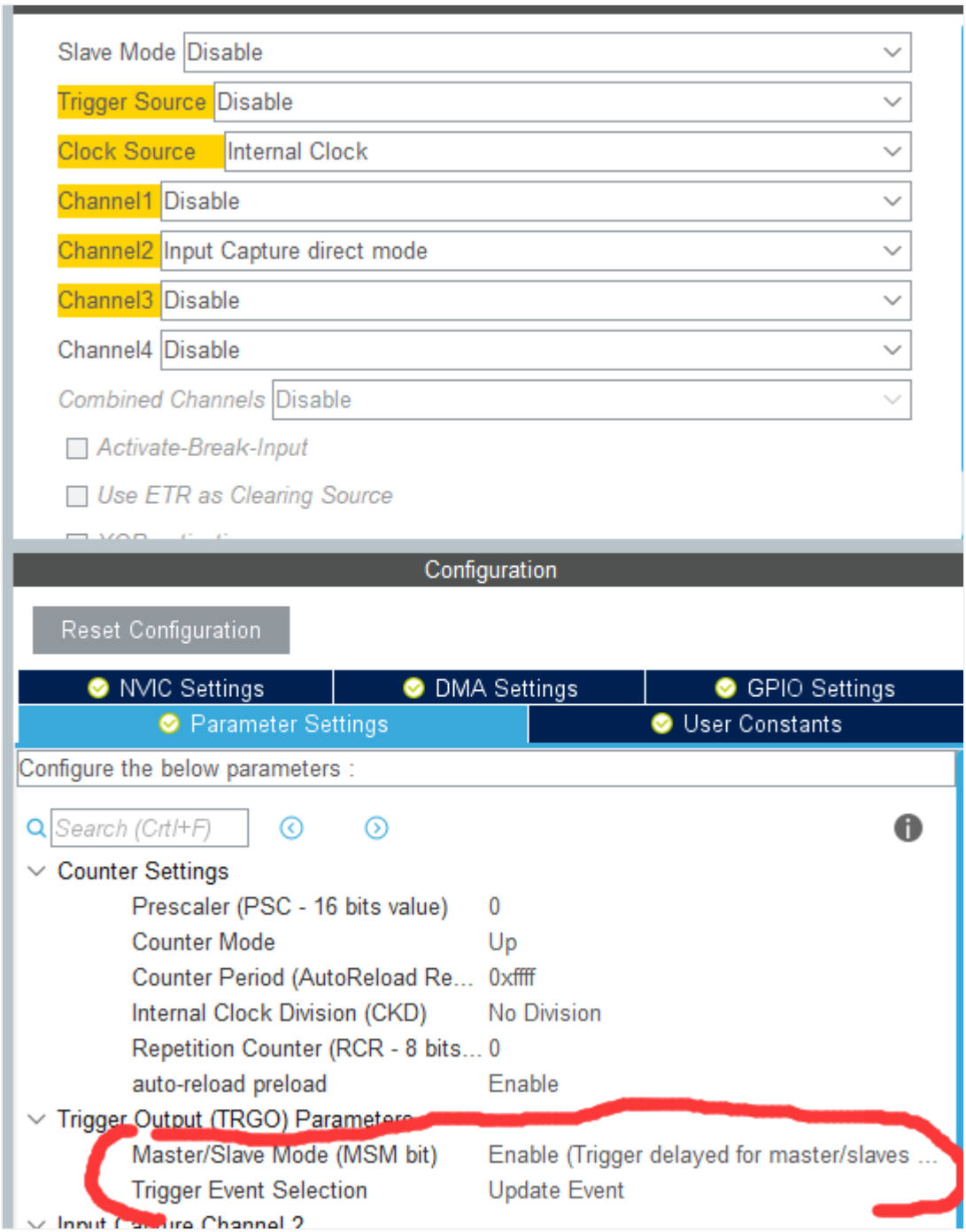
Even, you can continue to cascade, using three timers to form a 48-bit timer, of course, I only tested 48 bits, only 32 bits, more cascades to be tested.

Test effect: TIM1 is directly driven by the 72M system clock, TIM2 is driven by the signal generated by the TIM1 rollover, and TIM3 is driven by the signal generated by the TIM2 rollover.



Parameter setting: use cubemx+hal library to complete the setting,

The main timer (TIM1) parameters are set as follows:



Except for the red circle, the content is the same as the usual TIM usage setting. In addition, pay attention to the two parameters of counter period and auto-reload preload. Auto-reload should be turned on, otherwise the counting will stop after one cycle;

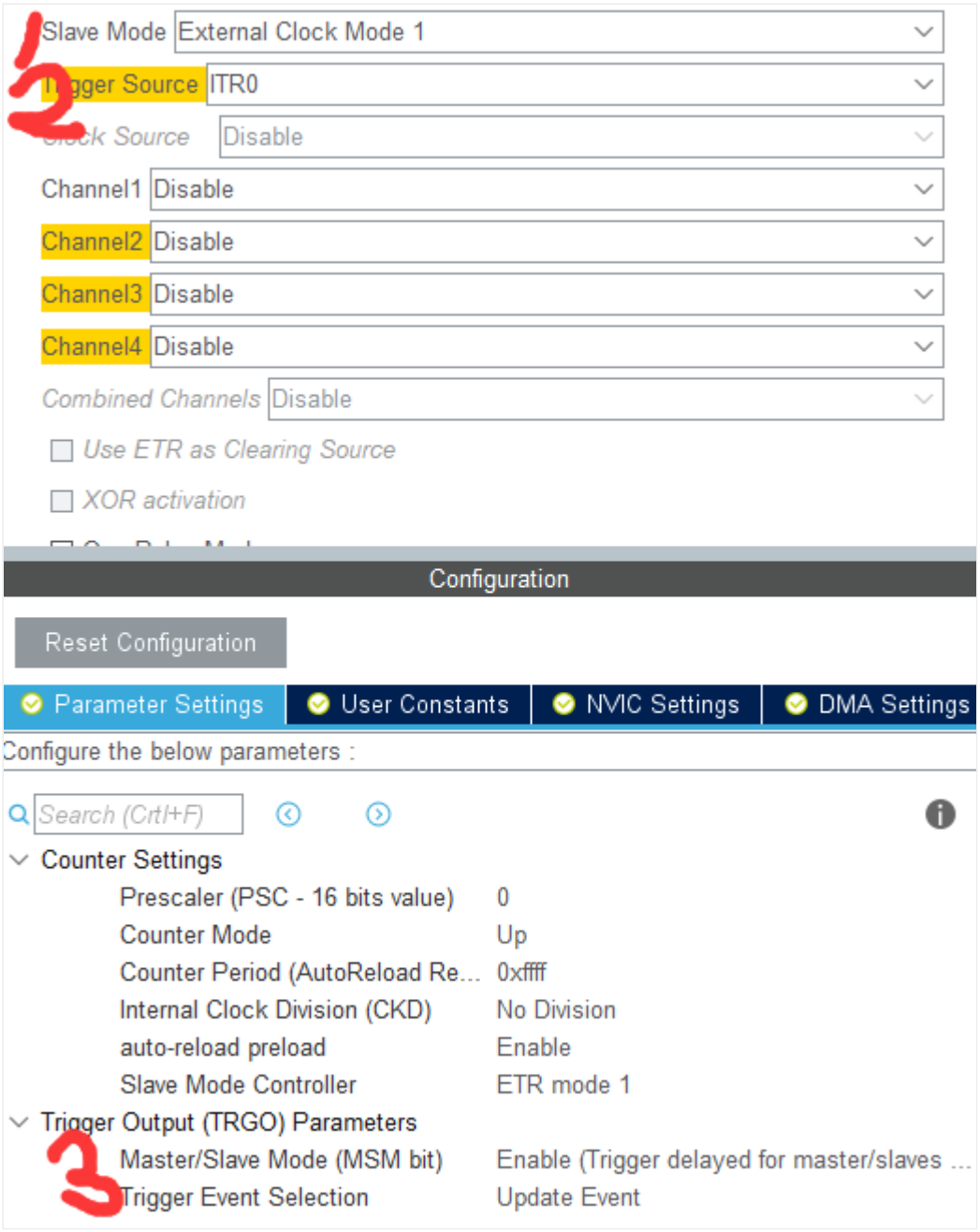
please explain:

The MSM bit should be the configuration register for the output cascade signal. Enabling this option can cause the timer to output a trigger signal. The main timer should enable this option.

Trigger event selection is a trigger signal option, I only tried two here: enable (cnt_en) is a synchronous count, that is, the main timer will output a signal every time it is triggered, suitable for the case of multiple timer linkage output; update event is The output is

updated, that is, the signal is output only when the timer is full. It is suitable for the case where multiple timers are linked to form a wider range of timers, such as 16-bit TIM + 16-bit TIM = 32-bit TIM...

The slave timer (TIM2) is set as follows:



please explain:

1. Parameter 1 must be set to external clock mode1, that is, the timer is driven by the input trigger signal;

2. Parameter 2 is the input source of the timer trigger signal. Please refer to this chart:

Table 86. TIMx Internal trigger connection(1)

Slave TIM	ITR0 (TS = 000)	ITR1 (TS = 001)	ITR2 (TS = 010)	ITR3 (TS = 011)
TIM2	TIM1	TIM8	TIM3	TIM4
TIM3	TIM1	TIM2	TIM5	TIM4
TIM4	TIM1	TIM2	TIM3	TIM8
TIM5	TIM2	TIM3	TIM4	TIM8

1. When a timer is not present in the product, the corresponding trigger ITRx is not available.

Take a chestnut: my slave timer is TIM2, then the slave TIM is TIM2, look at this line, TIM1 corresponds to ITR0, then the trigger source parameter in cubemx is ITR0; my second slave timer is TIM3, the third line TIM2 corresponds to ITR1, then the trigger source parameter of tim3 in cubemx should be ITR1.

3. Parameter 3 is related to whether the next cascade is to be performed. If you want to continue cascading the timer, please refer to the parameter setting of the position of TIM1 above; if you cascade the timer so far, then you can press cubemx by default.

In addition, the cascade timer can be used as an ordinary timer, input capture timer, can not be used as a PWM output I did not try, I feel that further settings are needed, welcome friends who have used to come to communicate.

Summary: 32-bit microcontrollers do not give 32-bit timers, really pull!