

ECE-442 Wireless Link Project Report – Receiver Team

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Abstract – This report will focus on discussing the results of the design of a wireless communications link. There were two teams, a transmitter and receiver group. We were the latter. Our frequency plan, carrier recovery scheme, and demodulation technique will be covered, along with the target specifications to meet. Furthermore, the challenges encountered along the way will serve to demonstrate the practical engineering challenges involved. The real-world parts needed to carry out the design will also be given. And finally, shortcomings in our design will be mentioned as well as the simple fixes needed for a second iteration.

I. Target Specifications

➤ Minimum SNR at Output	30dB
➤ Maximum Noise Figure	3.6dB
➤ Maximum Output Spurious	43dBc
➤ Maximum Phase Error	$\pm 2.25^\circ$

II. Assumed Priors

➤ Channel Loss	30dB
➤ Ambient Temperature	25° C
➤ Maximum Input Power	-18.36dB
➤ Minimum Input Power	-15.64dB
➤ Input Phase Error	$\pm 1.39^\circ$
○ QPSK Modulation	
○ 12.4 GHz Center Channel Frequency	
○ 3 GHz Data rate	

III. Introduction

We begin the analysis of our design based on what the transmitter team was able to achieve. In Sec. II we can see the maximum and minimum input powers we are dealing with. These values are given with reference to what our receiver antenna sees after the 30dB channel loss.

Setting up some more givens, we know that since we are dealing with QPSK modulation, each symbol represents 2 bits meaning that the symbol bandwidth is half of the 3GHz data bandwidth requirement. Thus, we plan to receive a signal bandwidth of 1.5GHz DSB centered at the 12.4GHz channel frequency. To avoid any confusion with this definition, there is 1.5GHz per sideband resulting in effectively 3GHz centered about 12.4GHz.

Lastly, there is an inherent phase error resulting from the phase error introduced by the transmitter team. Thus, a phase error of $\pm 2.25^\circ$ had already been incurred up until this point.

IV. Frequency Plan

Our frequency plan involved direct down-conversion to baseband. A spectral plan is shown on the following page. This made choosing the LO frequency very simple since it would be set equal to the channel center frequency of 12.4GHz. Furthermore, this got rid of the need for an image reject filter since there is no image frequency for direct conversion demodulation.

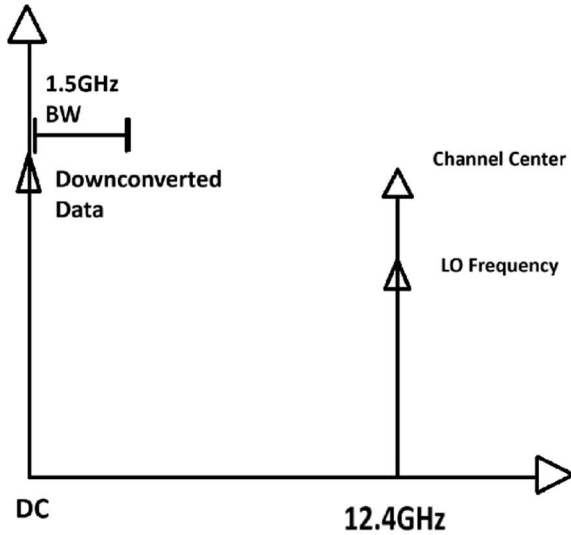


Fig 1. Frequency Plan

V. Receiver Architecture

Our receiver structure includes a main chain and a path for carrier recovery. We needed to pick an optimal architecture such that the total noise figure and phase error could be kept at a minimum. Meeting the target specifications essentially dictated which parts we could use.

A. Main Chain – Front End Components

The first object the information signal sees after being picked up by the antenna is the LNA. We experimented with adding a bandpass filter first before the LNA to reduce added noise from amplifying a larger signal bandwidth, but this unironically lead to a larger calculated noise figure after everything was put together. The choice of part here was crucial because the total noise figure is limited by the noise figure of the first element. We chose a *Qorvo* QPA2609 LNA [1] with a reasonably low noise figure of 1.1dB and small signal gain of 26dB within the 7 to 14GHz range.

Following the LNA came the *Mini Circuits* BFHKL-1252+ bandpass filter [2] with a very convenient passband from 10.9 to 13.9GHz. This was perfect for the 3GHz wide DSB information signal. Within the passband, typical insertion loss is 3.2dB; and in the stopband, typical rejection is

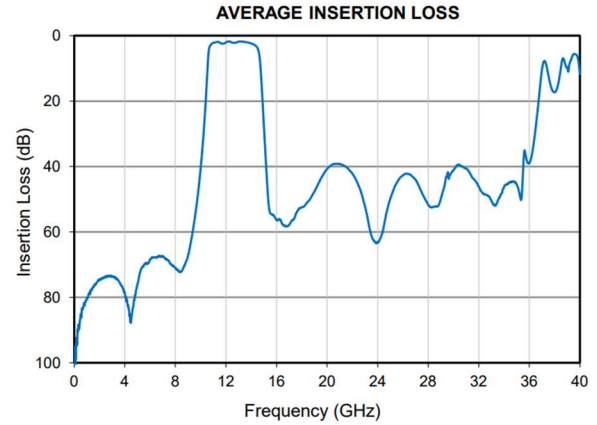


Fig 2. Filter Frequency Response

65dB below 10.9GHz and 38dB above 13.9GHz. For this application, close-to-precise filtering is necessary since we do not want to capture signals from neighboring channels.

B. Main Chain – Power Splitters for I and Q signal paths

The need for two power splitters is so that a sample of the **coherent** message signal can be brought to the carrier recovery path, and for the incoming message signal to be broken up into I/Q components. A *Mercury* AM4008 Power Divider [3] was chosen for this purpose. The downside to introducing power splitters is the inherent phase imbalance from the part. Notably, each power splitter introduced a $\pm 0.5^\circ$ phase imbalance when operating within the 10 to 18GHz range.

This phase inaccuracy was the first tradeoff in our design. By performing direct conversion, most of the parts chosen (before mixing) are required to operate at some RF frequency. Inherently, operating at this range limits the performance of the parts chosen which can lead to less and less ideality. By going to an IF instead, immediately after the LNA and BPF, we could pick parts with a better phase imbalance spec. For instance, the power splitter chosen has a phase imbalance of $\pm 0.15^\circ$ typically from 5 to 10GHz which shows how much of a saving this would yield.

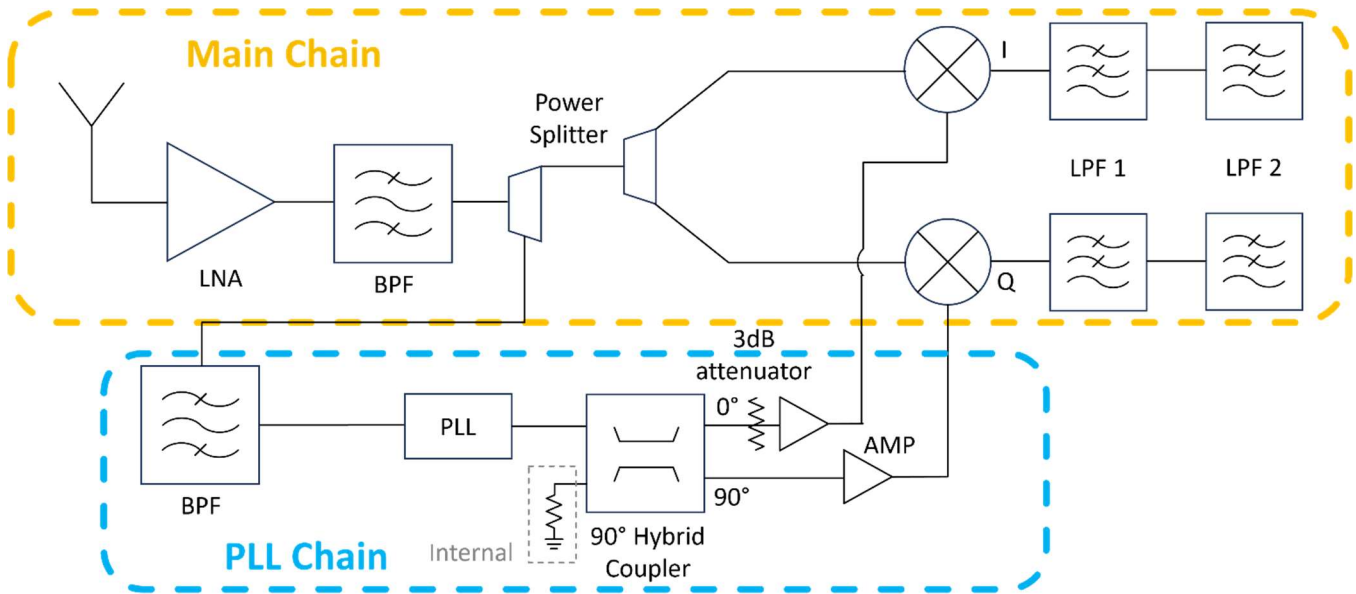


Fig 3. Receiver Functional Block Diagram

Alternatively, a 3-Way power divider could have been used instead of two, 2-Way power dividers, but this was not considered at the time. In the end, only a total of $\pm 0.5^\circ$ phase imbalance was incurred due to this power dividing stage. Note that we do not count the effect of the first power splitter since the “copied” signal used for carrier recovery, while at a $\pm 0.5^\circ$ offset from the incoming RF carrier, is still technically in-phase with the message signal being sent to the second power divider. Therefore, this does not contribute to “phase error” which is effectively the error due to mixing two out of phase signals.

C. PLL Chain – Carrier Recovery

To ensure proper signal recovery due to wireless transmission, it is important to establish *coherency*. It would be no good to mix the RF and LO out of phase with each other, as this would produce inaccuracies in the demodulation and decoding segments. Thus, a method must be developed to synchronize the mixing process with a coherent LO.

Our plan for carrier recovery involved three steps.

1. Produce a “sample” from the incoming carrier signal which we know is in-phase with the analog information sent.
2. Try to reproduce as close to an “ideal”, pure tone frequency as possible.
3. Create in-phase and quadrature components of this “synced up” signal, which will be needed for direct conversion to baseband.

It was demonstrated in the previous section how a “sample” of the incoming carrier signal was taken. Thus, Step 1 has been shown.

Step 2 first involved taking the sampled carrier signal and applying a super narrow passband filter centered about 12.4GHz. The idea is that we can rely on the fractional PLL to take an input signal and lock onto the phase while simultaneously producing an accurate frequency based on some stable/high Q reference oscillator. Thus, we figured “why not” to go ahead and supply the PLL with a more spectrally refined signal.

The *Sainty-Tech* SiMS12R45/R4-8D4 MEMS Bandpass Filter [4] was used here and featured a passband from 12.25 to 12.65 GHz! We were quite fascinated to have found this part

since it was incredibly precise and satisfied step 2.

Broadband Insertion Loss VS Frequency ($T_A=25^\circ\text{C}$)

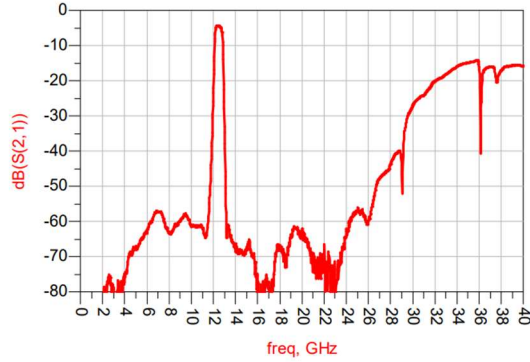


Fig 4. Sainty-Tech Bandpass Filter Frequency Response

D. PLL Chain – Introduction of the PLL

The PLL that was chosen specifically to hit the desired specifications. The chosen PLL was the HMC783LP6CE [12]. This chip was chosen for the specifications given in the data sheet as well as the 11 dBm typical output power. In order to have a coherent LO signal for our mixers we chose to use the PLL route, however there were oversights made.

Initially, assuming that the reference signal would be a crystal oscillator within the specifications of the PLL. Therefore, we would be trying to lock onto the wrong signal. This can be fixed through a pre-scaler for the signal we pull from the main line. This PLL supports the fractional-N mode to achieve finer frequency resolution. Using a division ratio of 40 for instance we can get a resolution frequency of 310 MHz fitting the PLL input range.

The PLL operates by comparing the phase of the prescaled reference signal (310 MHz) with the phase of the feedback signal from the VCO, divided down by the same factor (in this case, 40). The phase frequency detector (PFD) in the PLL will compare these two signals and generate an error signal based on any phase

difference. The error signal from the PFD adjusts the VCO, tuning its frequency to minimize phase error. Initially set to oscillate at or near the desired output frequency (12.4 GHz in our case), the VCO's exact frequency is fine-tuned by this process. The output of the VCO is then fed back through a frequency divider (set to divide by 40) back to the PFD, creating a closed loop. This feedback mechanism ensures that the VCO output stays locked to the 12.4 GHz target, matching the phase and frequency of the prescaled reference signal.

The output signal is coherent to the input signal because the phase of the VCO output remains locked to the phase of the input reference signal, despite the prescaling. The prescaler, while it divides the frequency, does not inherently alter the phase information, hence the output retains phase coherence with the input.

E. PLL Chain - 90° Hybrid Coupler

To meet our third and final step for carrier recovery, we had to prepare the 12.4GHz phase locked LO for mixing with the I/Q branches along the main chain. This required creating in-phase and quadrature components of the LO. Unfortunately, this process incurs some phase imbalance due to the imprecision of a 90° coupler. We are dealing with real parts here. Speaking of which, we used the *Marki Microwave* MQS-0518SM 90° Hybrid Coupler [5].

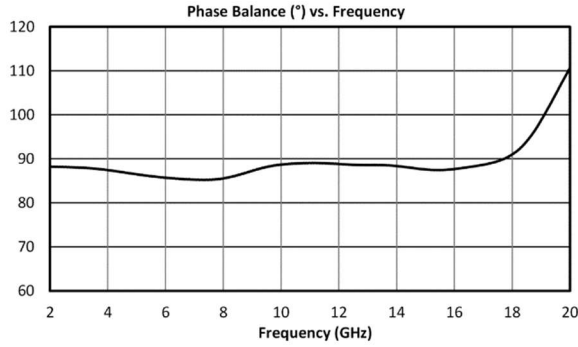
The phase imbalance for this part was given at $\pm 2.5^\circ$ which is substantial considering the $\pm 2.25^\circ$ target. A lot of time was spent trying to locate a part with a better phase imbalance, but this was the best we could find given the deadline. Otherwise, we could have been able to continue looking for better parts or adjust our strategy to compensate.

To briefly touch on an alternative strategy to the phase imbalance problem, if we chose to convert to an IF first (as was mentioned when discussing power dividers) we may have been able to find a hybrid coupler capable of operating

at a lower frequency with the benefit of better phase margin performance. The tradeoff would essentially be more stages and complexity, due to the addition of more IF processing, in exchange for a potential improvement in phase accuracy.

Analyzing the output signal power at the common and coupled port, insertion loss was

reported at 4.5dB and 7.5dB respectively. The datasheet reported a mean coupling of 3dB, hence the 3dB difference between the two ports. It was then necessary to add a 3dB fixed attenuator at the 0° port to ensure equal power between the two local oscillator paths. The *Marki Microwave* 3dB DC-40GHz MMIC Attenuator [6] was used for this.



Parameter	Port Configuration	Test Conditions	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Min	Typ	Max	Unit
Nominal Phase Shift ¹	A	-	5	18	-	90	-	°
Amplitude Balance ²	A	-	5	18	-	0.5	2.5	dB
Phase Balance	A	-	5	18	-	2.5	10	°
Excess Through Line Insertion Loss ³	A	-	5	18	-	4.5	6	dB
Isolation ⁴	A	-	5	18	10	17	-	dB
VSWR ⁵	A	-	5	18	-	1.2	-	-
Impedance	A	-	5	18	-	50	-	Ω
Mean Coupling ⁶	A	-	5	18	-	3	-	dB

Fig 5. 90° Hybrid Specifications

F. PLL Chain – LO Amplifiers

The final step before mixing is configuring the LO drive power to a certain level. In fact, this drive power was determined specifically so that we could rely on the specifications given in our mixer's datasheet. The mixer chosen gave performance specs based on a LO power of 15dBm meaning that we had to configure the LO power to be in the neighborhood of 15dBm. This was done using a *Mini Circuits* PMA2-133LN+ Monolithic Amplifier [7]. Operation is rated between 10 to 13GHz which is important because it falls within the range of our 12.4GHz LO. Based on the cascaded signal power analysis in Fig. 6 we determine that the amplifier must be tuned to a gain of +11.5dB to meet the 15dBm LO power requirement to the mixer.

G. Main Chain – Downconvert Mixers

Nearing the end of the main chain are the two double balanced mixers used for converting to baseband. A *Macom* MAMX-011035 5.5 to

19GHz mixer [8] was needed here. We could rely on a reasonable insertion loss of 6dB along with a solid LO to IF leakage of 45dB. Such large leakage is ideal for minimizing the output spurious content, which was another target spec to meet.

One last point to mention is the importance of operating mixers within their linear region. As stated in *Mini-Circuits* application notes on mixers (AN00009) [9]:

“When the RF signal power is within about 10 dB of the LO drive level, the IF output power no longer follows the increase in RF input exactly and the ratio between IF and RF power exhibits a change of about 0.1 dB. As the RF power increases further there will be a greater change in the ratio, with conversion loss increasing as the RF input power increases.”

- Sec. “Conversion Compression”

In our design considerations we made sure to follow this suggestion since there is greater than 10dB of separation between the LO and RF power levels – refer to Fig. 6.

H. Main Chain – Low Pass Filtering

The final component in the main chain is the low pass filtering stage. With an LO drive power of 15dBm and a LO to RF leakage of 45 dB, this yields a -30dBm signal at 12.4GHz after mixing. In our design, we included two low pass filters to combat this issue. First was a LPF with passband from DC to 1500MHz to

Electrical Specifications⁴: $F_{IF} = 100 \text{ MHz}$, $P_{LO} = 15 \text{ dBm}$, $T_A = +25^\circ\text{C}$, $Z_0 = 50 \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
LO and RF Frequency	—	GHz	5.5	—	19
IF Frequency	—	GHz	0	—	6
LO Power	—	dBm	—	15	—
Conversion Loss	5.5 - 19 GHz	dB	—	6	8
Input P1dB	5.5 - 10 GHz 10 - 19 GHz	dBm	—	8 11	—
Input IP3	$P_{REF} = -10 \text{ dBm/100 MHz}$, $\Delta f = 1 \text{ MHz}$ 5.5 - 10 GHz 10 - 19 GHz	dBm	—	18 20	—
Input IP2	$P_{REF} = -10 \text{ dBm/100 MHz}$, $\Delta f = 1 \text{ MHz}$ 5.5 - 10 GHz 10 - 19 GHz	dBm	—	45 45	—
LO-to-RF Isolation	5.5 - 10 GHz 10 - 19 GHz	dB	—	38 34	—
LO-to-IF Isolation	5.5 - 10 GHz 10 - 19 GHz	dB	28 32	40 45	—
RF-to-IF Isolation	5.5 - 10 GHz 10 - 19 GHz	dB	10 21	15 30	—

4. All specifications refer to down-conversion operation, unless otherwise noted.

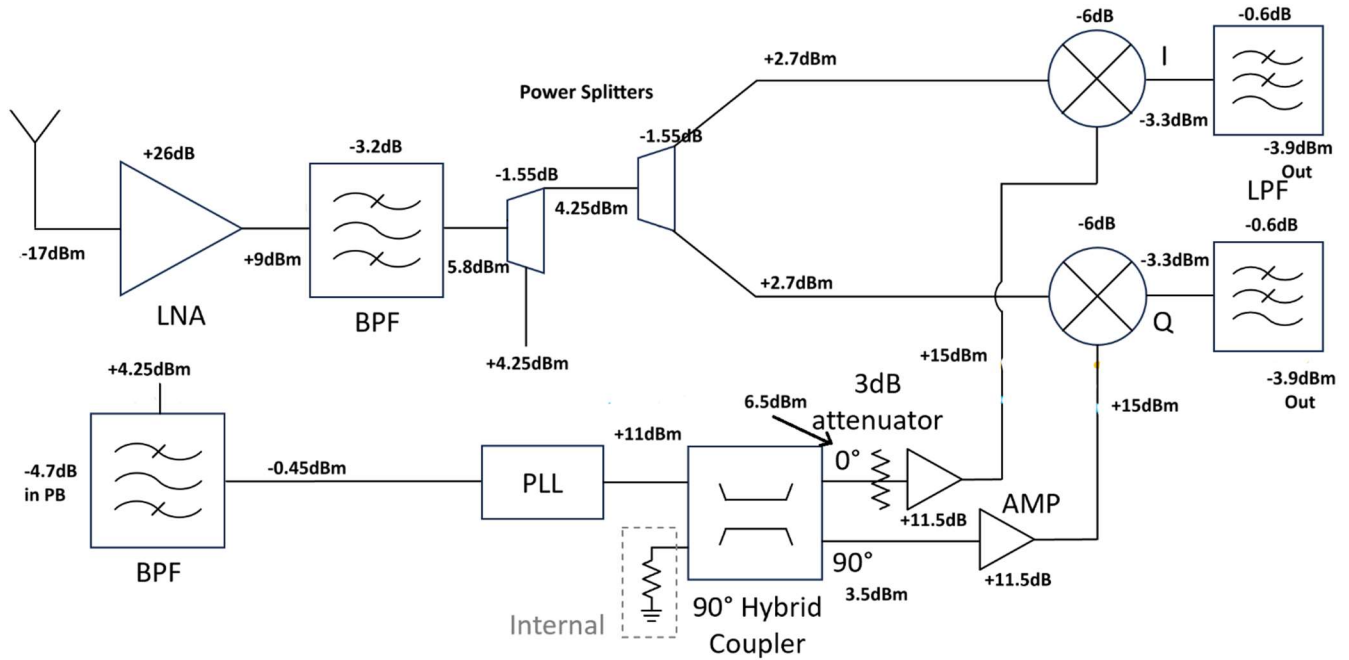


Fig 6. Cascade Signal Power Analysis

ensure proper inclusion of the entire message signal. Insertion loss was only 0.6dB. The part used for this was the *Mini Circuits* LFCN-1500D+ LPF [10]. The issue with this was that we did not have enough frequency response information to determine the attenuation at 12.4GHz (the location of the LO leakage power). Thus, we employed a second low pass filter to guarantee attenuation at 12.5GHz.

The final LPF used was the *Mini Circuits* LFCN-6000D+ [11]. Based on the information in the datasheet we could declare a “worst case” attenuation of 30.77dB at 12GHz (worst case as in perhaps our DC to 1.5GHz LPF had 5dB of attenuation at 12.4GHz, but was unconfirmable based on the given data). Furthermore, insertion loss was only 0.1dB in the DC to 1.5GHz region which is why it is negligible to include in the Fig 6. calculation.

VI. Results

Now that we have reached the end of the structure and the discussion of our design choices, we show the results in Fig 7. Beginning with receiver noise figure, we achieved a maximum of 2.76dB. Fairly solid as we beat the

Specification	Target	Achieved
Phase Error (including Tx)	$\pm 2.25^\circ$	$\pm 4.39^\circ$
Receiver Noise Figure	3.6dB	2.79dB
SNR at Output	30dB	61.04dB
Output Spurious	43dBc	56.97dBc

Fig 7. Project Results

target by roughly 1dB. Our minimum SNR at the output was determined by subtracting the output signal power [in dB] from the output noise power [in dB] since SNR is simply the ratio of the two. The output spurious content is determined by spectral analysis of the LO to IF leakage and is shown through more detail in Fig 8.

The only spec we did not meet was the phase error. On our side (excluding the phase error from the transceiver side) the phase imbalance was calculated by accumulating the inaccuracy in one of the two power dividers and the 90°

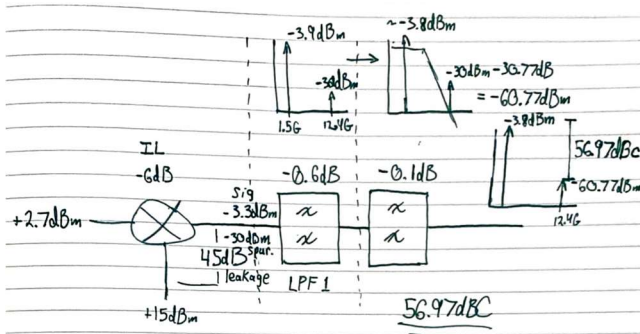


Fig 8. Output Spurious Calculation

hybrid coupler. In total, this was $\pm 2.5^\circ$ from the coupler and $\pm 0.5^\circ$ from the power divider, for $\pm 3.0^\circ$ overall. Including the phase error from the transceiver brings this error up even further to $\pm 4.39^\circ$. As stated throughout the explanation of the receiver structure, the solution would be to have more time to look for more accurate parts, or adjust our strategy entirely to incorporate down conversion to IF for more precise signal processing.

VII. Concluding Thoughts

From a purely academic standpoint, this project was a success in teaching us how to go about a system level design from start to finish. We also observed the typical challenges involved in sourcing different parts, adjusting the system architecture, etc. While we did not achieve the target spec for phase error, a lot can be said about what we took away from this project.

Upon presenting our design to the other design teams, we were able to get some critical feedback regarding how we could improve. For starters, the suggestion to phase lock the RF carrier to the 200MHz crystal, instead of the other way around, made a lot of sense and was something we overlooked.

Another helpful suggestion was to be careful with one of the assumptions made. During the presentation we made the assumption that with only the DC to 1.5GHz LPF at the output, the 12.4GHz LO leakage power would be attenuated by 20dB if following the trend

predicted in the datasheet. The issue was stopband information was only shown up to ~ 6 GHz meaning that there was really no guaranteeing what the attenuation would be at an octave away. This lead us to search for one final LPF to place after the initial LPF to guarantee that we met the output spurious spec rather than relying on a rather poor assumption.

In the end, the success of this project hinged on the combined effort from the three of us in order to tackle everything. Thanks to Professor Hausman, we were able to have some guidance along the way when we were stuck, as he really made us appreciate the design challenge.

VIII. Appendix

```
% 1st stage - LNA
F1 = db2pow(1.1)
G1_min = db2pow(23.5)
G1_typ = db2pow(26)
OIP3_1 = db2pow(23)*10^(-3)
% As Gain > 27dB at 25 degree celcius &
% @12GHz according to the chart, we
% can take typical value

% 2nd stage - BPF
% noise figure = loss factor when T=T0
F2 = db2pow(3.2)
G2 = db2pow(-3.2) % gain (dB to numerical
value)
OIP3_2 = db2pow(60)*10^(-3)

% 3rd stage - Power Splitter
F3 = db2pow(4.55)
G3 = db2pow(-1.55-3) %F=L
OIP3_3 = db2pow(Inf)

% 4rd stage - Power Splitter
F4 = db2pow(4.55)
G4 = db2pow(-1.55-3) %F=L, equal split ->
-3dB
OIP3_4 = db2pow(Inf)

% 5th stage - Mixer
```



```

F5_typ = db2pow(6)
G5_typ = db2pow(-6)
F5_max = db2pow(8)
G5_max = db2pow(-8)
OIP3_5 = db2pow(G5_max+20)*10^(-3) %IIP3 =
20dBm

% 6th stage - LPF1
F6_typ = db2pow(0.65)
F6_max = db2pow(1)
G6_typ_1500mhz = db2pow(-0.65)
G6_max = db2pow(-1)
OIP3_6 = db2pow(Inf)

% 7th stage - LPF2
F7_max = db2pow(0.1)
G7_max = db2pow(-0.1)
OIP3_7 = db2pow(Inf)

nf_component_typ = [F1, F2, F3, F4,
F5_max, F6_max, F7_max];
gain_component_typ = [G1_min, G2, G3, G4,
G5_max, G6_max, G7_max]
OIP3_list = [OIP3_1, OIP3_2, OIP3_3,
OIP3_4, OIP3_5, OIP3_6, OIP3_7]

%% Noise Figure

% noise_figure_total = F1 + (F2-1)/G1 +
(F3-1)/(G1*G2) + (F4-1)/(G1*G2*G3)
%                               + (F5-
1)/(G1*G2*G3*G4) + (F6-1)/(G1*G2*G3*G4*G5)
noise_fig = zeros(1, 7)
total_noise_figure = 0
for i=1:length(nf_component_typ)
    if i==1
        multiple_gain = 1;
        noise_fig(i) =
nf_component_typ(i);
    else
        multiple_gain =
multiple_gain*gain_component_typ(i-1);
        noise_fig(i) =
(nf_component_typ(i) - 1)/multiple_gain
    end

```

```

        total_noise_figure =
total_noise_figure+noise_fig(i)
    end
    total_noise_fig_dB =
pow2db(total_noise_figure)

%% Output SNR
% Assume all temperature = 25 degree
celcuis = 298K
TA = 298
T0 = 298
k = 1.38*10^(-23)
B = 1.5*10^9 %(BW of LPF = 1.5G)
G = 1
for i=1:length(gain_component_typ)
    G = G*gain_component_typ(i)
end

transmit_pw_max = 14.53374219 %(dBm)
transmit_pw_min = 11.73428104 %(dBm)

S_input = db2pow(transmit_pw_min -
30)*10^(-3) %(W) (-30 is channel loss)
Te = (total_noise_figure - 1)*T0

Noise_output = k*(TA + Te)*B*G
S_output = G * S_input
SNR = pow2db(S_output/Noise_output) %dB

%% Maximum Spurious Signal
OIP3_reciprocal = zeros(1, 7)
for i=1:length(OIP3_list)
    G = G/gain_component_typ(i)
    OIP3_reciprocal(i) = 1/(OIP3_list(i) *
G)
End

OIP3_total = 1/sum(OIP3_reciprocal)

% SFDR (dB) = 2/3*(OIP3 - Noise_output),
OIP3, Noise_output in dBm
%           = 10*log10(P_carrier_signal /
P_spurious) = 10*log10(S_output /
P_spurious)
% Thus S_output / P_spurious =
(10^((1/15)*(OIP3 - Noise_output)))

```

```
OPI3_total_dBm = pow2db(OPI3_total*(10^3))
Noise_output_dBm =
pow2db(Noise_output*(10^3))

Spurious_out_dBc =
pow2db(10^((1/15)*(OPI3_total_dBm -
Noise_output_dBm)))
```

IX. References

- [1] Qorvo, "7 – 14 GHz GaAs Low Noise Amplifier," QPA2609 datasheet, May 2020
- [2] Mini Circuits, "TCC SMT Band Pass Filter, 10.9 - 13.9 GHz, 50Ω," BFHKL-1252+ datasheet
- [3] Mercury, "Splitter 1.5 GHz to 26.5 GHz 2-Way 0 ° Splitter" AM4008 datasheet
- [4] Sainty-Tech Communications, "MEMS Bandpass Filter 12.25 to 12.65 GHz" SiMS12R45/R4-8D4 datasheet
- [5] Marki Microwave, "90° Splitter/Combiner MMIC 5-18GHz" MQS-0518SM datasheet
- [6] Marki Microwave, "MMIC Attenuator 3dB DC-40GHz" ATN03-0040PSM datasheet
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- [8] Macom, "Double-Balanced Mixer 5.5 - 19.0 GHz" datasheet
- [9] Mini Circuits, "AN00-009 Understanding Mixers – Terms Defined, and Measuring Performance," Application Notes [Online]. minicircuits.com/appdoc/AN00-009.html
- [10] Mini Circuits, "Ceramic Low Pass Filter DC to 1500 MHz, 50Ω" LFCN-1500D+ datasheet
- [11] Mini Circuits, "Ceramic Low Pass Filter DC to 6000 MHz, 50Ω" LFCN-6000D+ datasheet
- [12] Analog Devices, "HMC783LP6CE Fractional-N PLL with integrated VCO, 11.5 - 12.5 GHz" datasheet