DW9714

- 10bit Resolution VCM driver IC with I2C interface

Ver. 1.95
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CONTENTS

1. General Description

The DW9714 is single 10-bit DAC with 120mA output current sink capability. Designed for linear control of voice coil motors, the DW9714 is capable of operating voltage to 3.6V. The DAC is controlled via a I^2C serial interface that operates DAC by clock rates up to 400kHz.

The DW9714 incorporates with a power-on reset circuit, power-down function, and exactly matched sense resistor. Power-on reset circuit ensure when supply power up, DAC output is to 0V until valid write-bit value takes place. It has a power down features that reduces the current consumption of the device to 1uA maximum.

The DW9714 is designed for auto focus and optical zoom camera phones, digital still cameras, and camcorders applications. The I^2C address for the DW9714 is 0x18.

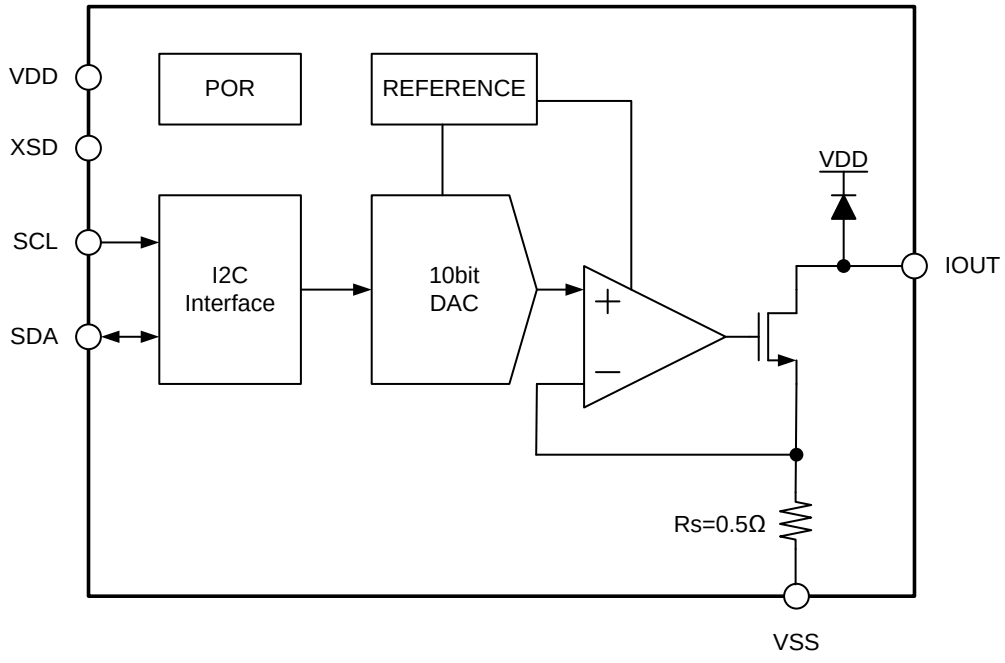
■ Features

VCM driver for auto-focus
10bit resolution current sinking of 120mA for VCM
VCM slew rate control (SRC) – Linear slope control, Dual level control
Supply voltage range (VDD) : 2.3V to 3.6V
Fast mode I2C interface (1.8V interface available)
Power on reset (POR)
Package : 0.80mm(W) X 1.20mm(H) X 0.3mm(T) 6pins WLCSP

■ Applications

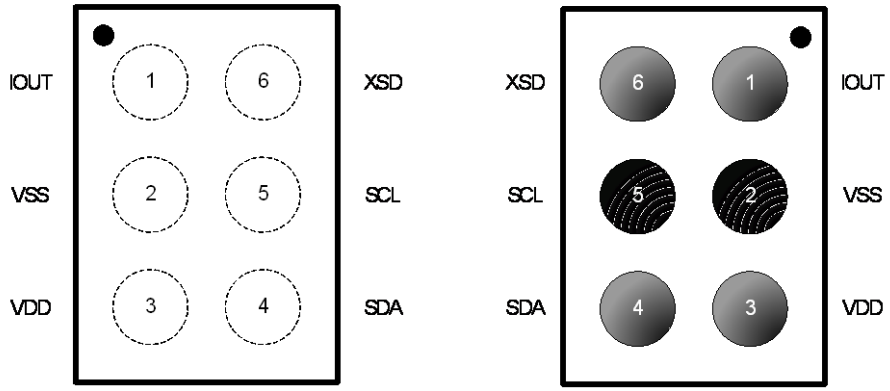
Digital camera
Cell phone
Lens auto focus
Web camera

2. Block Diagram



3. Pin Information

■ Pin placement and IC dimension



IC size : 0.80(W) X 1.20(L) X 0.30(T) (mm)
Minimum pin pitch = 0.4mm (6pins WLCSP)

■ Pin Description

No.	Pin Name	I/O	Description	Note
1	IOUT	O	Output current sink	
2	VSS	-	Ground	
3	VDD	-	Power supply	
4	SDA	I/O	I2C interface input (DATA)	
5	SCL	I	I2C interface input/output (CLOCK)	
6	XSD(1)	I	Shutdown mode (active low)	

(1) XSD : Shutdown mode (active low)
1: Normal operation mode
0: Shutdown mode
※ When XSD pin is floating, DW9714 is an unknown state. XSD pin must be controlled.

4. Absolute Maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VDD	Power supply voltage	-0.3	4.5	V
Vin	Control input voltage	-0.3	VDD+0.3	V
Vhbm	Human body model		2	KV
Vmm	Machine model		200	V
Topr	Operating temperature range	-40	85	℃
Tj	Junction temperature		150	℃

Note> Continuous Power Dissipation (Ta=25℃)
0.80mm X 1.20mm WLCSP, 100 ℃/W

5. Recommended Operating condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Power supply voltage	2.3	2.8	3.6	V
Vin	Control input voltage	0	2.8	VDD	V
SCL	I2C bus transmission rate			400	kHz

■ Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode when the absolute maximum ratings may be exceeded is anticipated.

6. Electrical Specification

(VDD=2.3 to 3.6V, Vin=1.8V to VDD, Ta= -40 to 85℃, unless otherwise specified. Typical values are at 25℃)

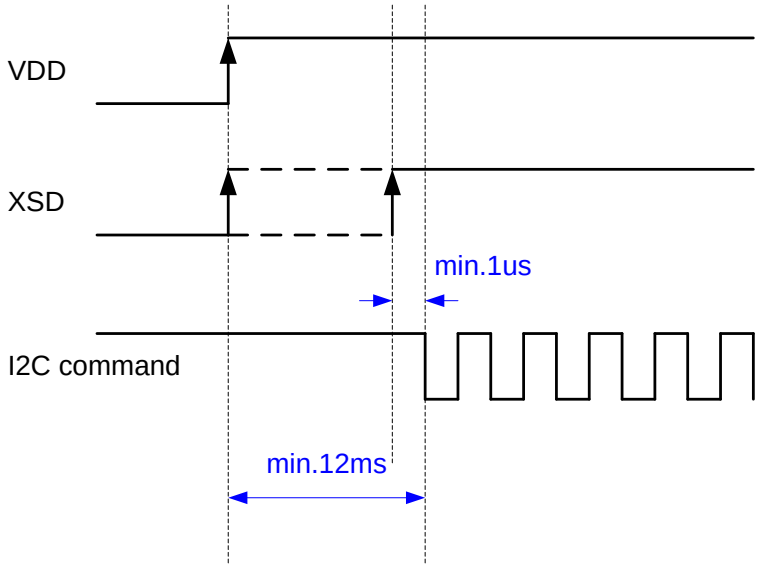
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Overall						
Supply Voltage	V_{DD}		2.3		3.6	V
V_{DD} Current	I_{SD}	Shutdown mode	-1		+1	uA
	I_{PD}	Power down mode	-1		+1	uA
	I_Q	Quiescent mode	0.24	-	0.35	mA
Logic input / output (XSD)						
Input current			-1		+1	uA
Low Level Input Voltage	V_{IL}				0.54	V
High Level Input Voltage	V_{IH}		1.26			V
Logic input / output (SCL,SDA)						
Input current			-1		+1	uA
Low Level Input Voltage	V_{IL}				0.54	V
High Level Input Voltage	V_{IH}		1.26			V
Low Level Output Voltage	V_{OL}	IIN=3mA(SDA)			0.4	V
Glitch rejection				50		ns
VCM driver						
Current resolution		117.3uA/LSB		10		bits
INL	INL		-4		+4	LSB
DNL	DNL		-1		+1	LSB
Zero code error	ZCE	Zero data loaded to DAC	-1		+1	mA
IOUT compliance voltage (1)		Output current = 100mA	150			mV
Maximum output current	Imax		115	120(3)	125	mA
Power on time (2)	TPON			12		ms

(1) The output compliance voltage is guaranteed by design and characterization, not mass production test.

(2) DW9714 requires waiting time of 12ms after power on. During this waiting time, the offset calibration of internal amplifier is operating for minimization of output offset current .

(3) Maximum output current can be set 60mA to 130mA.

7. Power on sequence

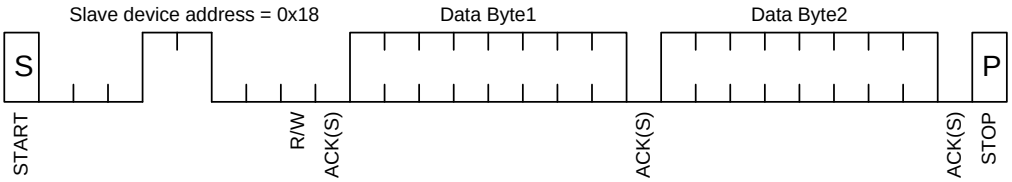


※ DW9714 required waiting time of 12ms after power on.
※ XSD have only to be set “high” before I2C command.
※ XSD can be connect to VDD.

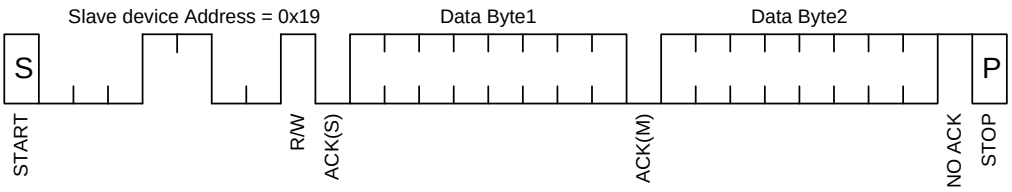
8. Register

8.1. I2C format

■ Write Operation



■ Read Operation



※ In I2C format, Master(ISP, AP etc.) have to check the ACK bit and send a next data.

8.2. Register Format

Byte1								Byte2							
PD	FLAG	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S3	S2	S1	S0

PD : Power down mode
1: Power down mode (active high)
0: Normal operation mode

FLAG : FLAG bit must be ”L” at DAC data are written.
During SRC operation, FLAG bit keep ”H”. While FLAG=”H”**,** the I2C command is ignored.

D[9:0] : Data input
Output current = (D[9:0]/1023) X 120mA

S[3:2] : Codes per step for “Linear slope control”

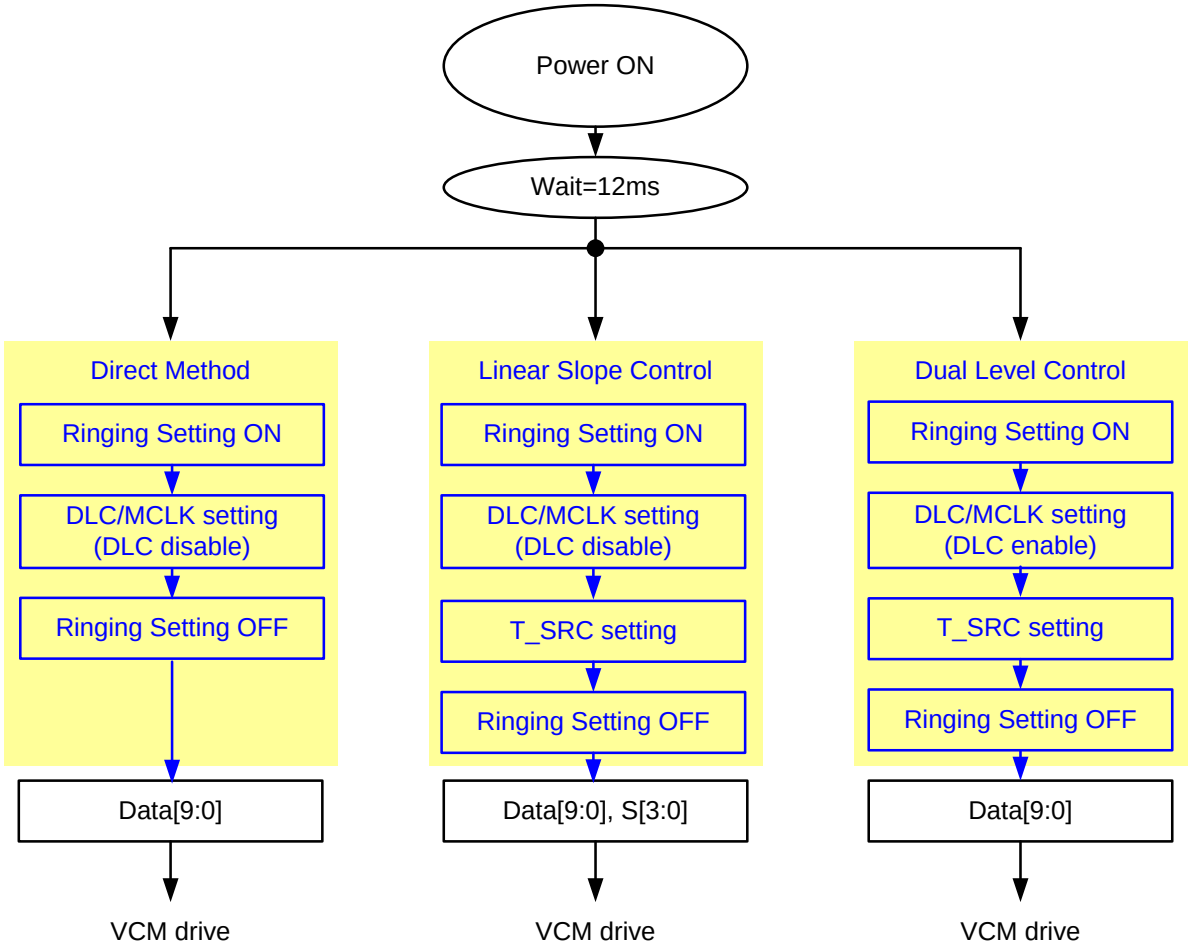
S[3:2]	Codes per step
00	0 (no SRC) – direct driving
01	1
10	2
11	4

S[1:0] : Step period is determined by S[1:0] and T_SRC[4:0] for “Linear slope control”

S[1:0]	Period [us]
00	Refer “Linear slope control”
01	Refer “Linear slope control”
10	Refer “Linear slope control”
11	Refer “Linear slope control”

9. Slew Rate Control Set up Method

9.1. Driving mode – Direct, Linear Slope Control, Dual Level Control



※ When you use direct mode after power on, you don't need register set. Because, DLC disable is default.

※ During a SRC setting sequence, DAC command does not update.

9.2. Direct mode Control set up method

▣ Ringing setting ON

Byte1 (0xEC)								Byte2 (0xA3)							
1	1	1	0	1	1	0	0	1	0	1	0	0	0	1	1

▣ DLC and MCLK[1:0] setting

Byte1 (0xA1)								Byte2(default = 0x05)							
1	0	1	0	0	0	0	1	0	0	0	0	DLC =0	1	MCL K1	MCL K0

DLC : Dual-level control mode

1: Dual-level control mode (active high)

0: Direct and linear slope control

▣ T_SRC[4:0] setting

Byte1 (0xF2)								Byte2(default = 0x00)							
1	1	1	1	0	0	1	0	T_ SRC 4	T_ SRC 3	T_ SRC 2	T_ SRC 1	T_ SRC 0	0	0	0

▣ Ringing setting OFF

Byte1 (0xDC)								Byte2 (0x51)							
1	1	0	1	1	1	0	0	0	1	0	1	0	0	0	1

※ When you use direct mode after power on, you don't need register set. Because, DLC disable is default.

9.3. Linear Slope Control set up method

▣ Ringing setting ON

Byte1 (0xEC)								Byte2 (0xA3)							
1	1	1	0	1	1	0	0	1	0	1	0	0	0	1	1

▣ DLC and MCLK[1:0] setting

Byte1 (0xA1)								Byte2(default = 0x05)							
1	0	1	0	0	0	0	1	0	0	0	0	DLC =0	1	MCL K1	MCL K0

DLC : Dual-level control mode

1: Dual-level control mode (active high)

0: Direct and linear slope control

▣ T_SRC[4:0] setting

Byte1 (0xF2)								Byte2(default = 0x00)							
1	1	1	1	0	0	1	0	T_ SRC 4	T_ SRC 3	T_ SRC 2	T_ SRC 1	T_ SRC 0	0	0	0

▣ Ringing setting OFF

Byte1 (0xDC)								Byte2 (0x51)							
1	1	0	1	1	1	0	0	0	1	0	1	0	0	0	1

※ During a SRC setting sequence, DAC command does not update.

■ Linear Slope Control – T_SRC[4:0] selection table

Linear Slope Control step period is set by S[1:0] and T_SRC[4:0]

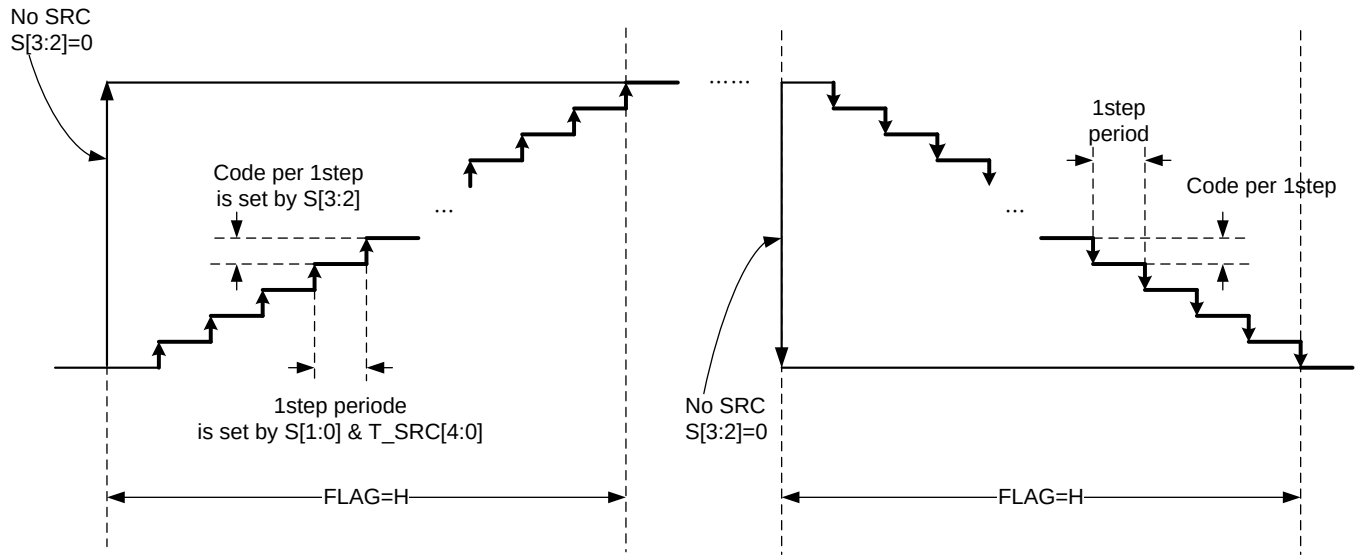
T_SRC[4:0] = 00000(default),(*)MCLK[1:0] = 01(default) Unit = [us]

1 Step period				
T_SRC[4:0]	S[1:0]			
	00	01	10	11
10000	136.0	272.0	544.0	1088.0
10001	130.0	260.0	520.0	1040.0
10010	125.0	250.0	500.0	1000.0
10011	120.0	240.0	480.0	960.0
10100	116.0	232.0	464.0	928.0
10101	112.0	224.0	448.0	896.0
10110	108.0	216.0	432.0	864.0
10111	104.0	208.0	416.0	832.0
11000	101.0	202.0	404.0	808.0
11001	98.0	196.0	392.0	784.0
11010	95.0	190.0	380.0	760.0
11011	92.0	184.0	368.0	736.0
11100	89.0	178.0	356.0	712.0
11101	87.0	174.0	348.0	696.0
11110	85.0	170.0	340.0	680.0
11111	83.0	166.0	332.0	664.0
00000 (default)	81.0	162.0	324.0	648.0
00001	79.0	158.0	316.0	632.0
00010	77.5	155.0	310.0	620.0
00011	76.0	152.0	304.0	608.0
00100	74.5	149.0	298.0	596.0
00101	73.0	146.0	292.0	584.0
00110	71.5	143.0	286.0	572.0
00111	70.0	140.0	280.0	560.0
01000	69.0	138.0	276.0	552.0
01001	68.0	136.0	272.0	544.0
01010	67.0	134.0	268.0	536.0
01011	66.0	132.0	264.0	528.0
01100	65.5	131.0	262.0	524.0
01101	65.0	130.0	260.0	520.0
01110	64.5	129.0	258.0	516.0
01111	64.0	128.0	256.0	512.0

※ (*) MCLK[1:0] = 00 : x2 (double) 01 : x1 (default)

10 : half 11 : quarter

■ Linear slope control scheme



9.4. Dual Level Control set up method

▣ Ringing setting ON

Byte1 (0xEC)								Byte2 (0xA3)							
1	1	1	0	1	1	0	0	1	0	1	0	0	0	1	1

▣ DLC and MCLK[1:0] setting

Byte1 (0xA1)								Byte2(default = 0x05)							
1	0	1	0	0	0	0	1	0	0	0	0	DLC =1	1	MCL K1	MCL K0

▣ DLC : Dual-level control mode

1: Dual-level control mode (active high)

0: Normal operation mode

▣ T_SRC[4:0] setting

Byte1 (0xF2)								Byte2(default = 0x00)							
1	1	1	1	0	0	1	0	T_ SRC 4	T_ SRC 3	T_ SRC 2	T_ SRC 1	T_ SRC 0	0	0	0

▣ Ringing setting OFF

Byte1 (0xDC)								Byte2 (0x51)							
1	1	0	1	1	1	0	0	0	1	0	1	0	0	0	1

※ During a SRC setting sequence, DAC command does not update.

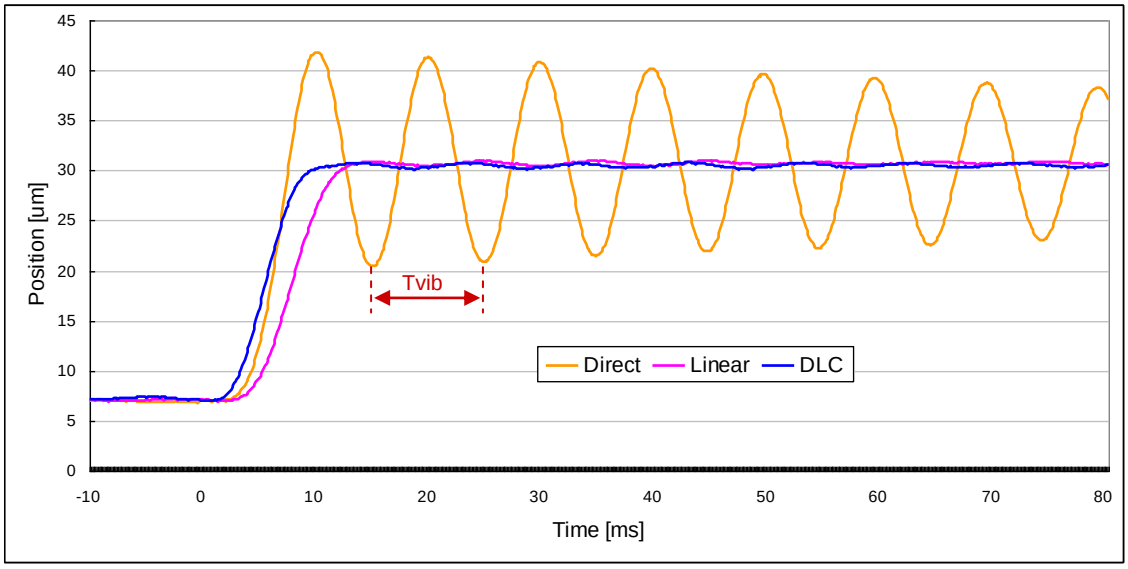
■ Dual Level Control (DLC) – T_SRC[4:0] & MCLK[1:0] selection table

DLC step period is set by MCLK[1:0] and T_SRC[4:0],
MCLK[1:0] default value is 2'b=01 and T_SRC[4:0] default value is 5'b=00000.
Recommended that DLC step period is set Tvib/2 (Tvib=VCM vibration period)

Unit = [ms]

Tvib/2				
T_SRC[4:0]	MCLK[1:0]			
	00	01	10	11
10000	21.25	10.63	5.31	2.66
10001	20.31	10.16	5.08	2.54
10010	19.53	9.77	4.88	2.44
10011	18.75	9.38	4.69	2.34
10100	18.13	9.06	4.53	2.27
10101	17.50	8.75	4.38	2.19
10110	16.88	8.44	4.22	2.11
10111	16.25	8.13	4.06	2.03
11000	15.78	7.89	3.95	1.97
11001	15.31	7.66	3.83	1.91
11010	14.84	7.42	3.71	1.86
11011	14.38	7.19	3.59	1.80
11100	13.91	6.95	3.48	1.74
11101	13.59	6.80	3.40	1.70
11110	13.28	6.64	3.32	1.66
11111	12.97	6.48	3.24	1.62
00000 (default)	12.66	6.33	3.16	1.58
00001	12.34	6.17	3.09	1.54
00010	12.11	6.05	3.03	1.51
00011	11.88	5.94	2.97	1.48
00100	11.64	5.82	2.91	1.46
00101	11.41	5.70	2.85	1.43
00110	11.17	5.59	2.79	1.40
00111	10.94	5.47	2.73	1.37
01000	10.78	5.39	2.70	1.35
01001	10.63	5.31	2.66	1.33
01010	10.47	5.23	2.62	1.31
01011	10.31	5.16	2.58	1.29
01100	10.23	5.12	2.56	1.28
01101	10.16	5.08	2.54	1.27
01110	10.08	5.04	2.52	1.26
01111	10.00	5.00	2.50	1.25

9.5. SRC Test Results – Comparison of Direct, Linear slope control, and Dual level control

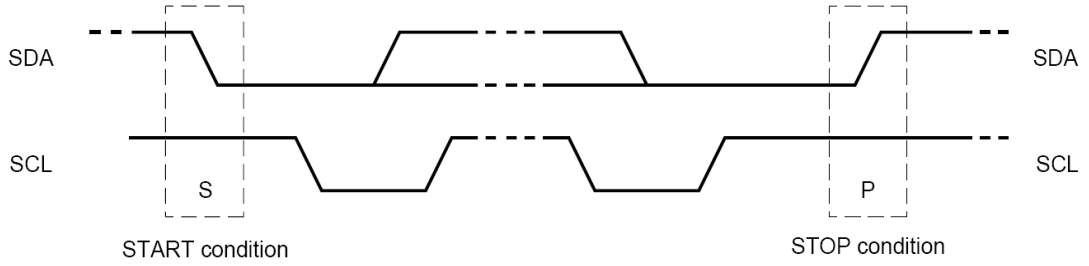


* Tvib : Vibration period of the VCM

DLC rising time = Tvib / 2
LSC rising time = Tvib

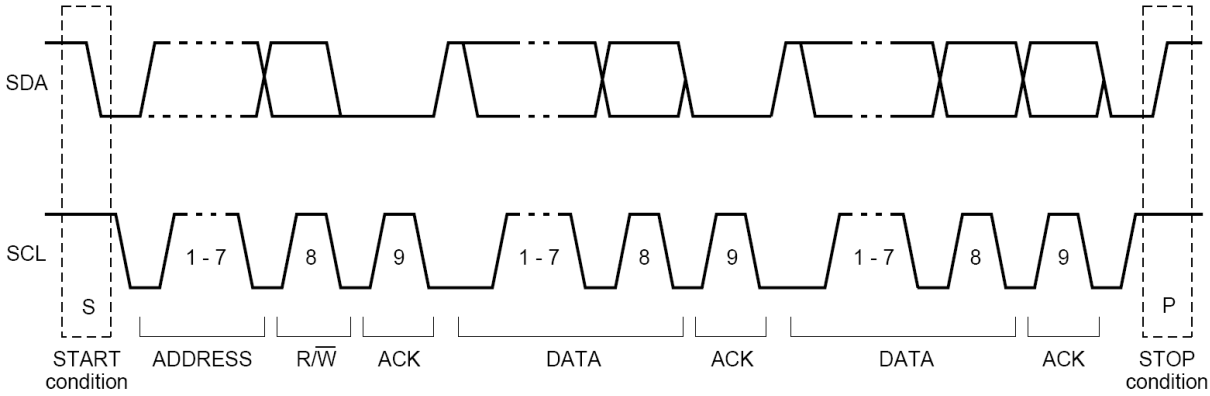
10. I2C Protocol

■ Start and Stop condition



Within the procedure of the I2C-bus, unique situations arise which are defined as START (S) and STOP (P) conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

■ Complete I2C Data Transfer

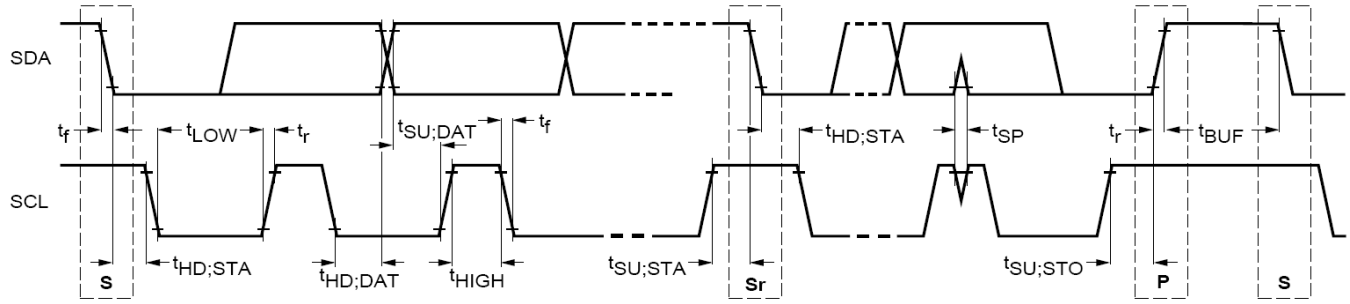


Data transfers follow the format. After the START condition (S), a slave address is sent. A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated

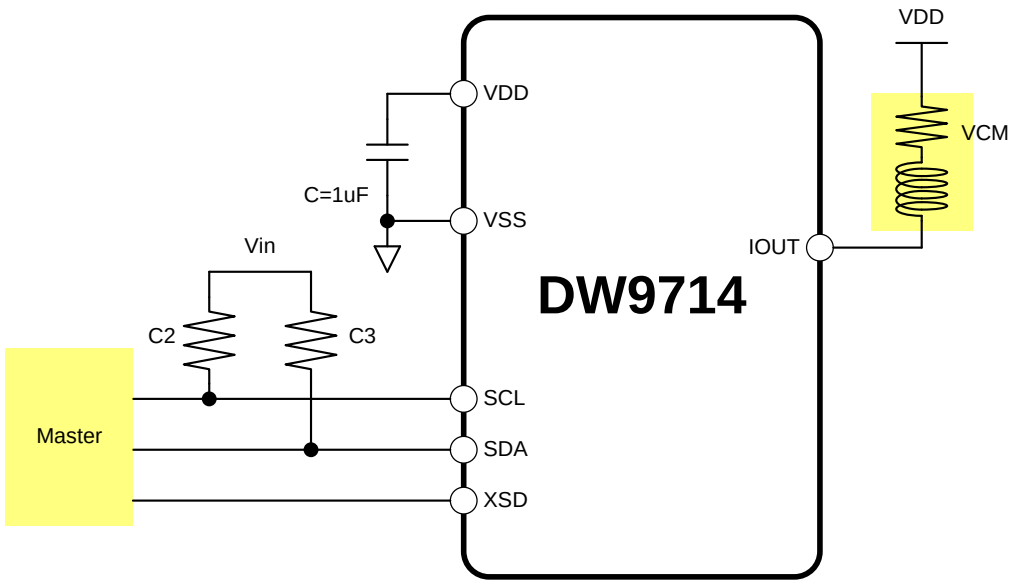
■ I2C timing

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time (repeated) START condition.	$t_{HD;STA}$	0.6	-	us
Low period of the SCL clock	t_{LOW}	1.3	-	us
High period of the SCL clock	t_{HIGH}	0.6	-	us
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	us
Data hold time	$t_{HD;DAT}$(1)	-	0.9	us
Data set-up time	$t_{SU;DAT}$	100	-	ns
Rise time of both SDA and SCL signals	t_r	20+0.1C_b(2)	300	ns
Fall time of both SDA and SCL signals	t_f	20+0.1C_b(2)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	us
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	us
Capacitive load for each bus line	C_b	-	400	pF
Pulse width of spike suppress	t_{SP}	0	50	ns

(1) A master device must provide a hold time of at least 100ns for the SDA signal to bridge the undefined region of the falling edge of SCL. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
(2) C_b is the total capacitance of one bus line in pF, t_r and t_f are measured between $0.3V_{DD}$ to $0.7V_{DD}$.



11. Recommended Application Circuit



※ XSD can be connected to VDD

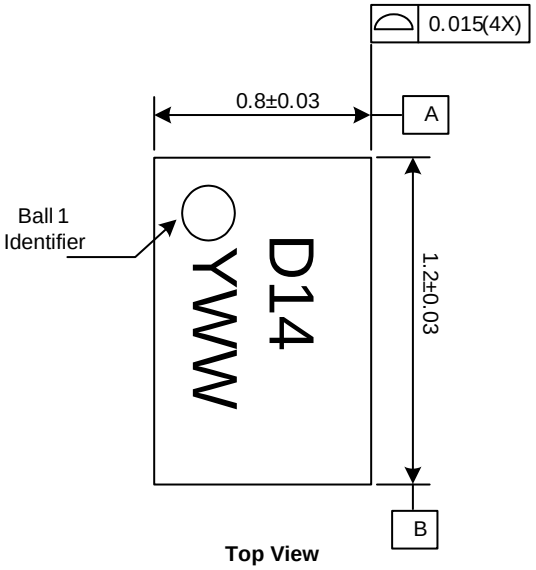
※ When XSD pin is floating, DW9714/14S/14N is an unknown state. XSD pin must be controlled.

※ Recommend Resistor value(C2,C3) - VIN 2.8V : 4.7K Ω / VIN 1.8V : 1.3K Ω ~ 4.7K Ω.

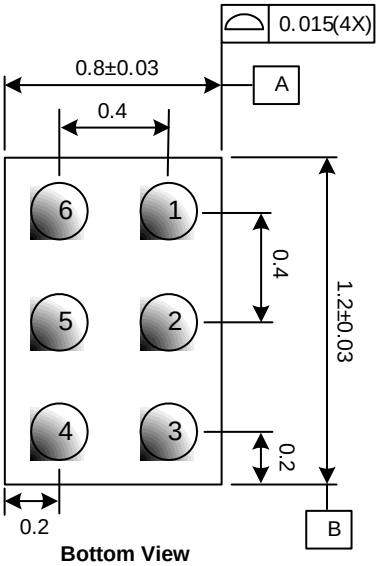
12. Package Dimension

12.1. DW9714 (0.8mm X 1.2mm X 0.3mm)

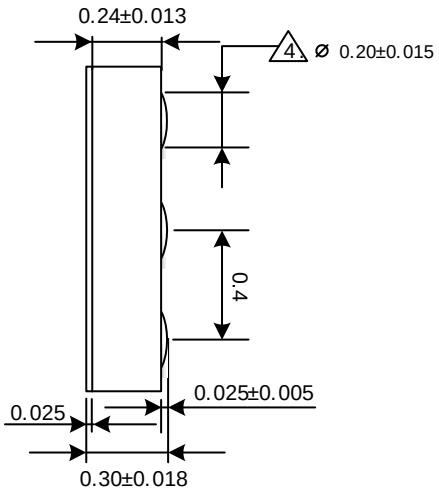
* Unit : mm



Top View



Bottom View



Side View

NO	NAME	I/O
1	IOUT	O
2	VSS	-
3	VDD	-
4	SDA	I/O
5	SCL	I
6	XSD	I