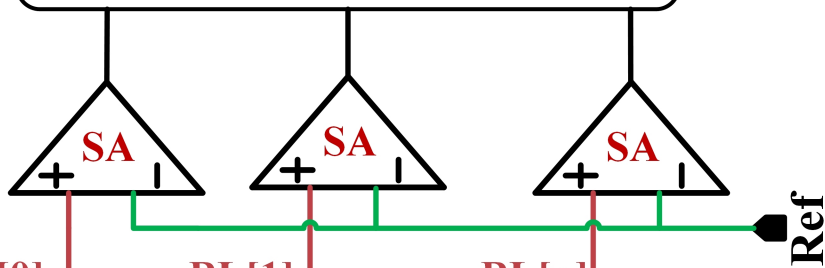


CCLG & Output



BL[0]

BL[1]

BL[n]

WL[0]

WLB[0]

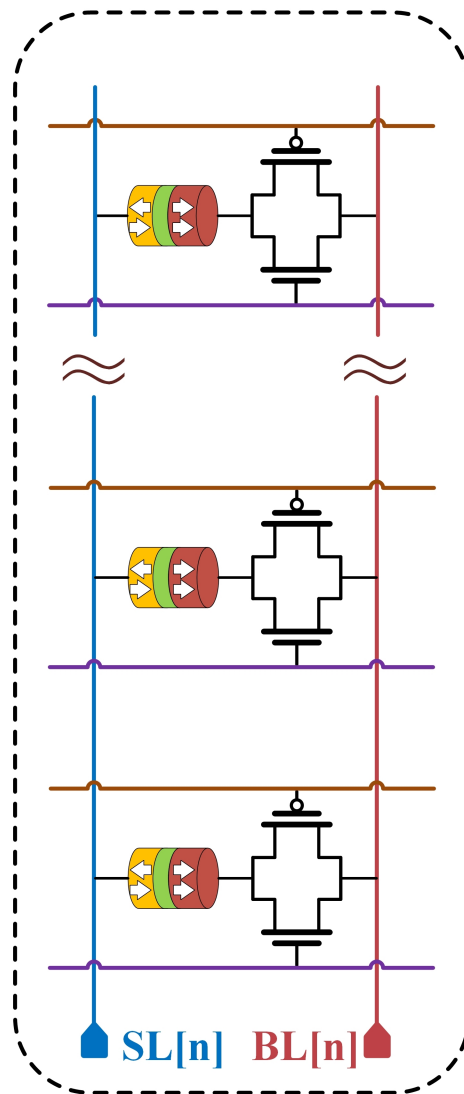
...

WL[m]

WLB[m]

row
[i] row
[i+1] row
[i+3]

Logic bank



SL[n]

BL[n]