Simulation of a 4-bit Analog-Digital Flash converter

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This report focuses on the creation and the simulation of a 4-bit Analog-Digital Flash converter.

The role of an ADC is to convert an analog signal into a digital signal that can be processed by digital logic.

Different types of ADCs exist :

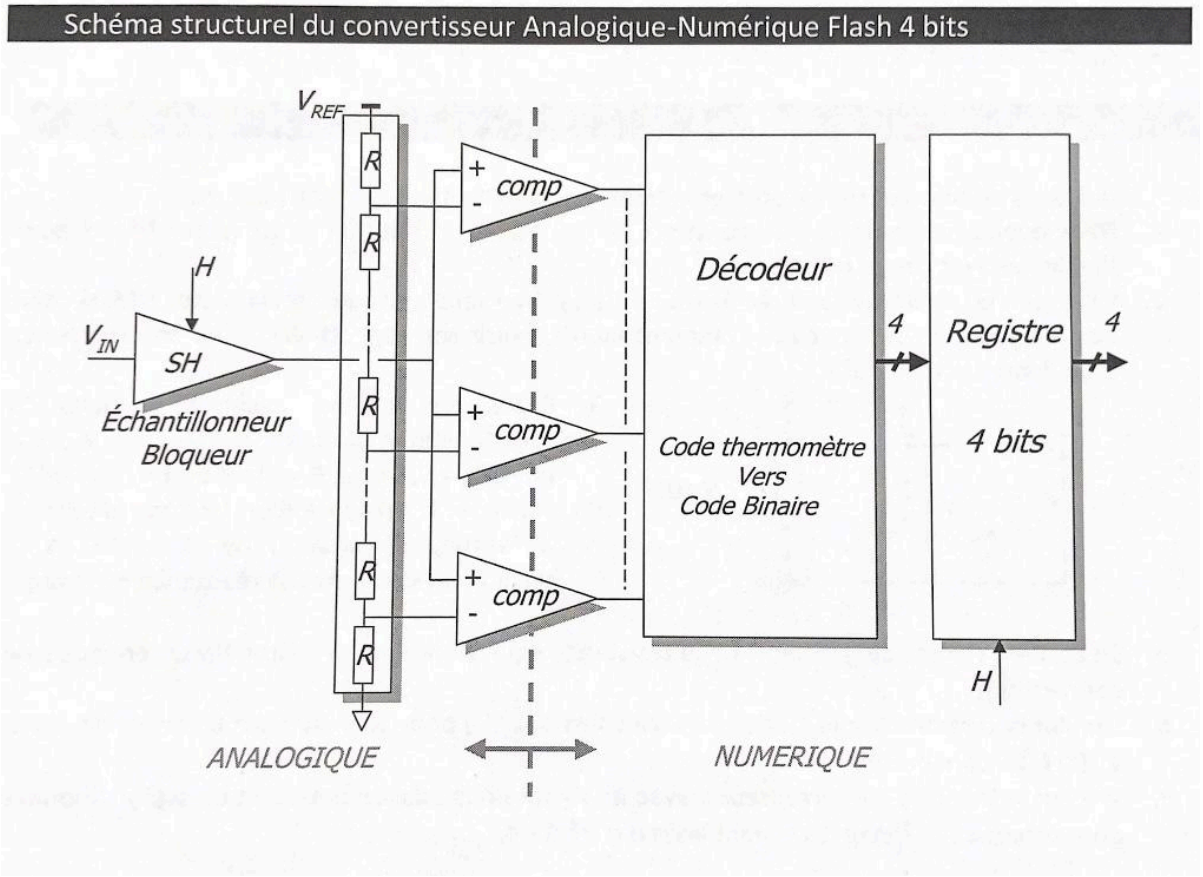
- Sigma-delta
- Successive approximation (SAR)
- Pipelined
- Dual-slope
- Flash

These converters have different sample rate and resolution despite the fact they all perform the same function. Therefore, they all have different applications depending on the needs of the constructor. A Flash ADC has the highest sample rate (about 10 GHz) but the lowest resolution. This project focused on the Flash architecture.

To carry out the project, several functions were created and then assembled together to sample, compare, decode and store the analog signal as a digital signal. The role of each of these functions is detailed to understand the overall operation.

Electrical signals were always between 0 V and 3.3 V, and a sinusoidal signal was used during the study.

Here is a structural diagram of the converter :

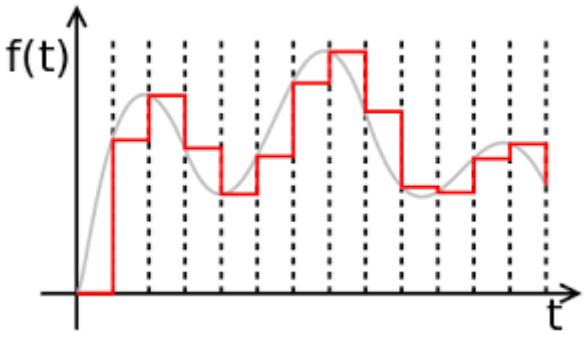


The structural diagram is divided into 4 blocks :

- A sampler-blocker
- A comparison block
- A decoder
- A 4-bit register

First of all, the input signal of the sampler is continuous and must be converted into a discrete signal. Therefore, it is defined as a succession of values that are actualised at a frequency called sampling frequency.

Here is the operating graph of the sampler-blocker :



Once this step was completed, it was necessary to give a binary association to the closest level. To do this, 15 comparators set to different reference values were used to frame the sampler's output value. Thus, the ADC has an accuracy of 3.3/16, so about 0.21 V.

Once the thermometer code was determined, its binary code had to be evaluated. This was possible by using logic gates for the 4 bits of the associated code.
C<i> is the logical signal associated with "the value is greater than $V_{ref,i}$", and here are the logical equations of the 4-bit S3 S2 S1 S0 :

$$S3 = C8$$

$$S2 = C4.\overline{C8} + C12$$

$$S1 = C2.\overline{C4} + C6.\overline{C8} + C10.\overline{C12} + C14$$

$$S0 = C1.\overline{C2} + C3.\overline{C4} + C5.\overline{C6} + C7.\overline{C8} + C9.\overline{C10} + C11.\overline{C12} + C13.\overline{C14} + C15$$

The decoder determined the value associated with the input signal at a given time. The next step was to record this value while a new sampling is done. For this, a 4-bit register based on Latch and Flip-Flop switches keeps the 4 bits of the signal in memory.

The sampler-blocker and MOSFET P transistors is the subject of this report and its results are presented in the conclusion.

Sample and Hold

For this study, analyzing the use of a sampler alone is necessary :

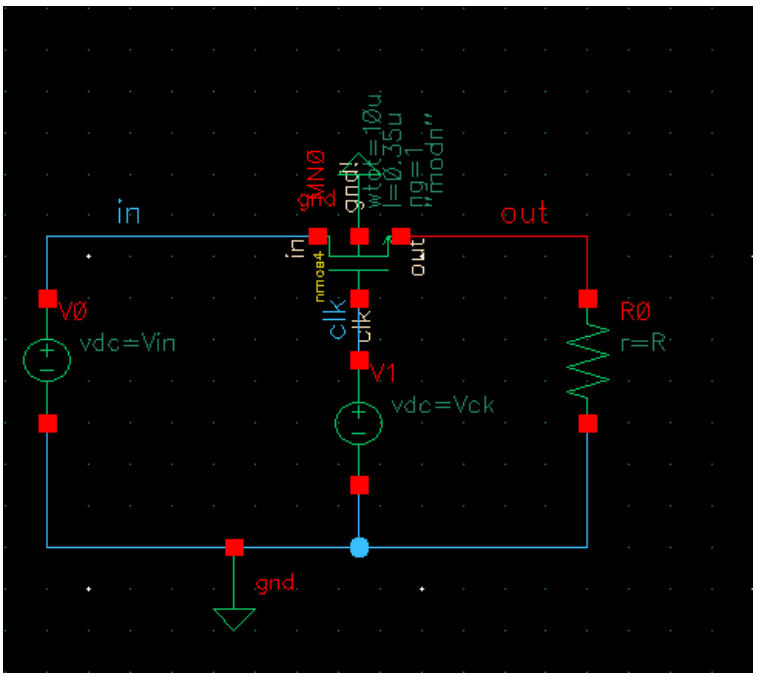


Figure 1 : Sampler using Nmos4 technology

The way it works is once $V_{gs} < V_T$, the presence of a nmos transistor makes the circuit “open”, which means that there is no more current in the “out” section. However, once it reaches $V_{gs} > V_T$, the current is not zero due to the transistor being in lineary mode which leads to the presence of R-dependent output as shown on the following graph :

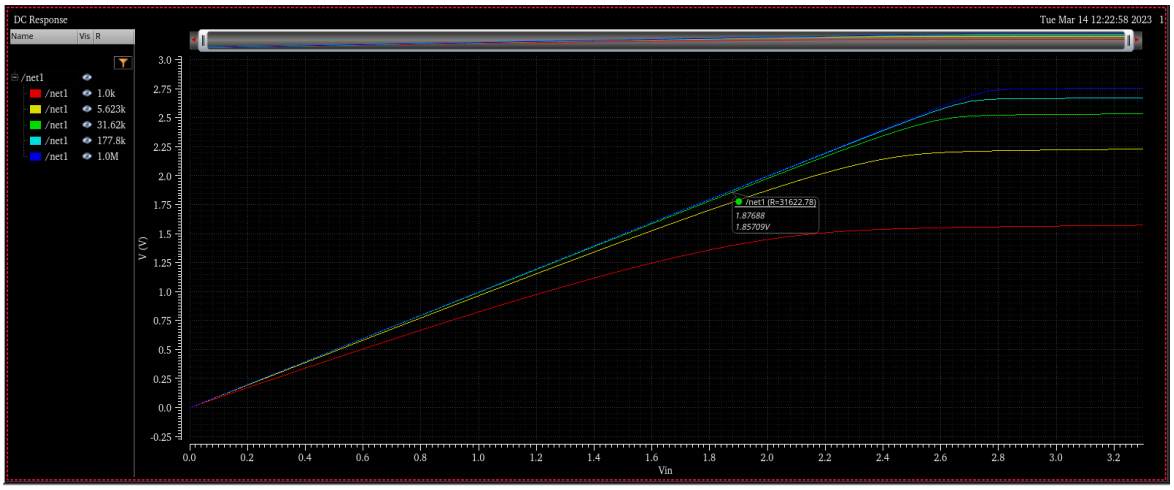


Figure 2 : Sampler simulation with different values of R using the nmos technology

As seen in Figure 2, once V_{in} reaches a certain voltage, the transistor enters a saturated state presenting a limitation on the current which causes an issue as it would lead to the incapacity of treating the higher voltage values. To resolve it, a study on a similar circuit using a different technology of transistors (pmos) will be held. If the R chosen has a very high value, only a small voltage, that can be measured in hundreds of microvolts, comes out of the circuit.

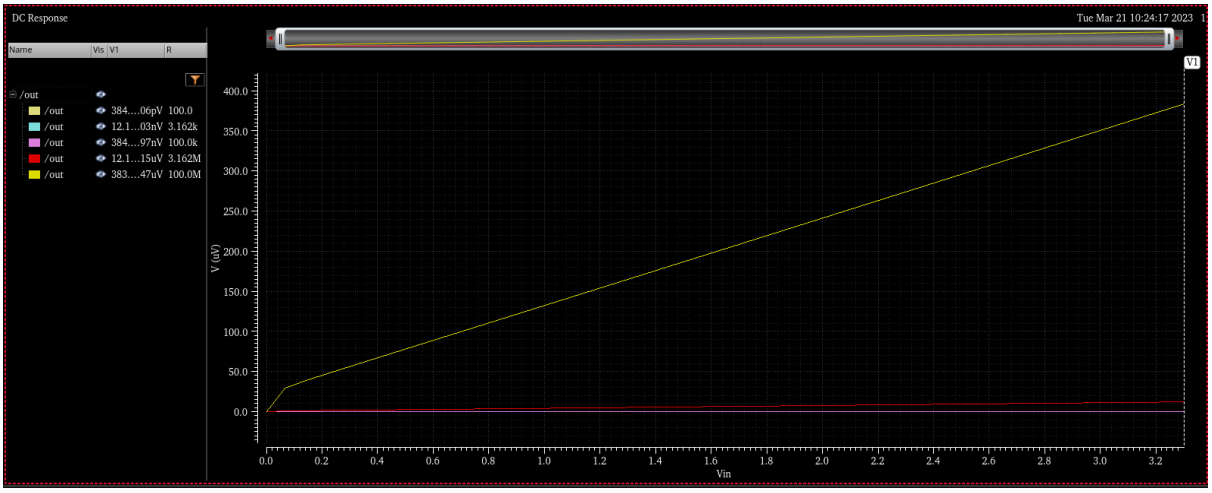


Figure 3 : Nmos Sampler simulation with high values of R

The graph here clearly shows the importance of choosing a low value of R. Therefore, choosing the right value of R is needed otherwise the cut-off mode is disturbed and is more likely to cause an issue for the rest of the project.

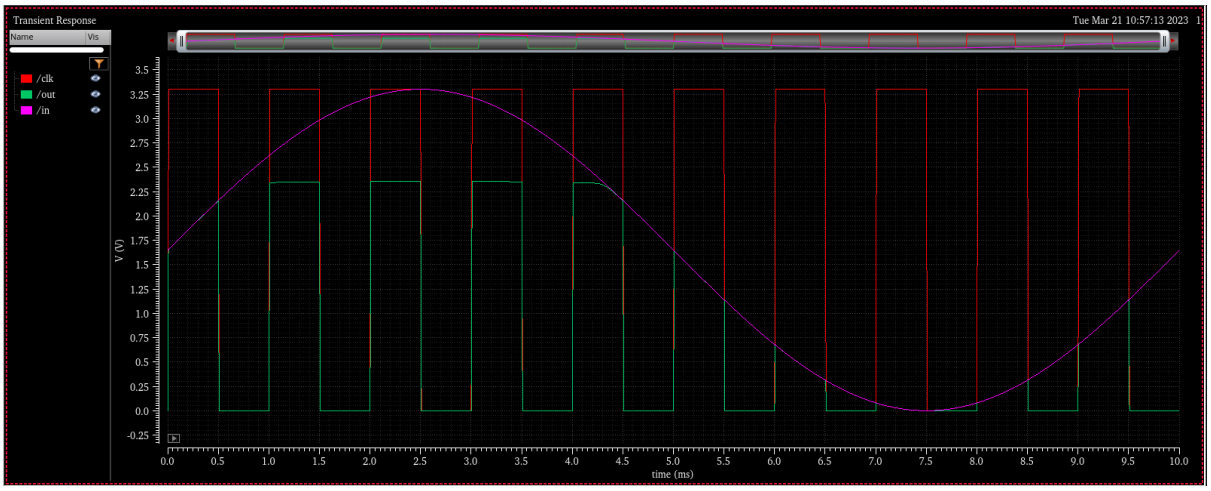


Figure 4 : Use of a nmos sampler with a sinus entry

As stated before, for the high values of V_{in} (Pink curve), when $V_{in} > 2.3V$, the sampler is unable to reach its values.

The following study is on a sampler using the pmos technology instead of the nmos one. As opposed to the previous study, once $V_{gs} > V_T$, the circuit becomes open whereas the linear mode is entered once $V_{gs} < V_T$. The following graph presents itself as a complementary of the previous circuit using the nmos technology:

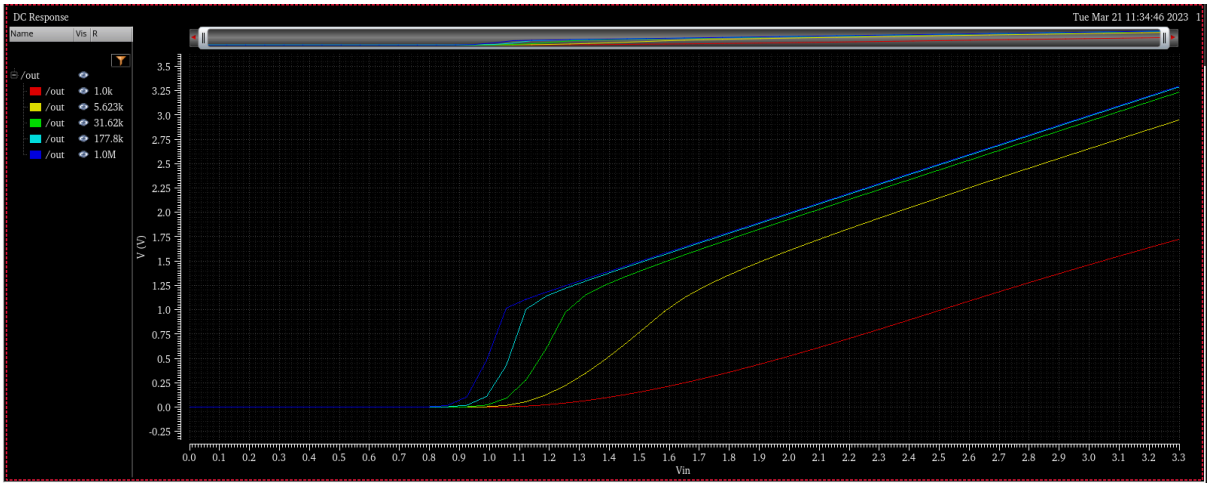


Figure 5 : Sampler simulation with different values of R using the pmos technology

This time, the pmos technology becomes useful for dealing with values of V_{in}. Meanwhile, the nmos technology struggled before but is unable to deal with values being lower than 1V that the nmos technology was able to sample before.

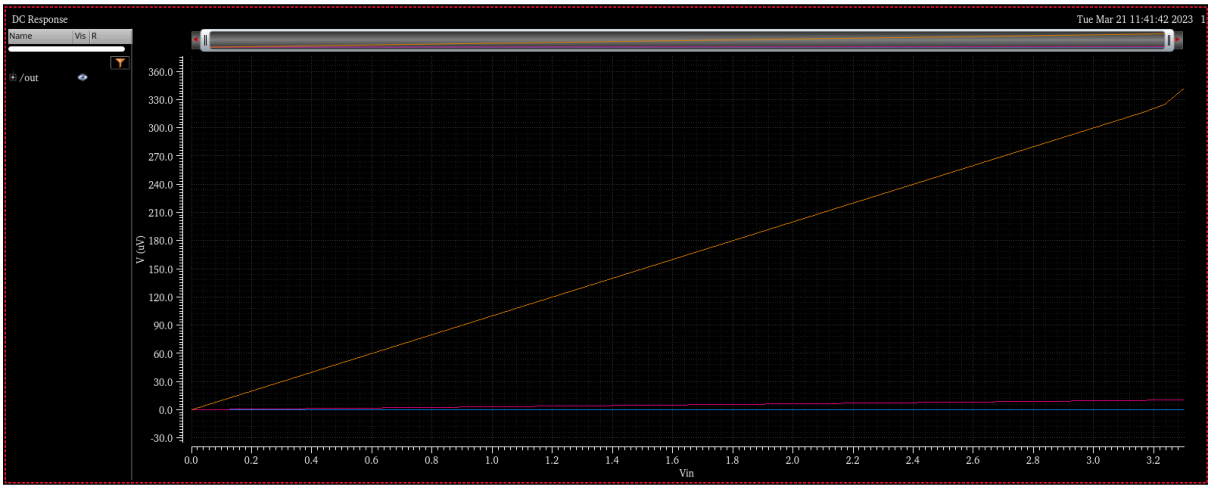


Figure 6 : Pmos Sampler simulation with high values of R

Figure 6 presents the same aspect as Figure 3. , meaning both the pmos and nmos technology share the same issue with the use of the high resistance component. In fact, it amplifies the importance of choosing a low value resistance for this sampler.

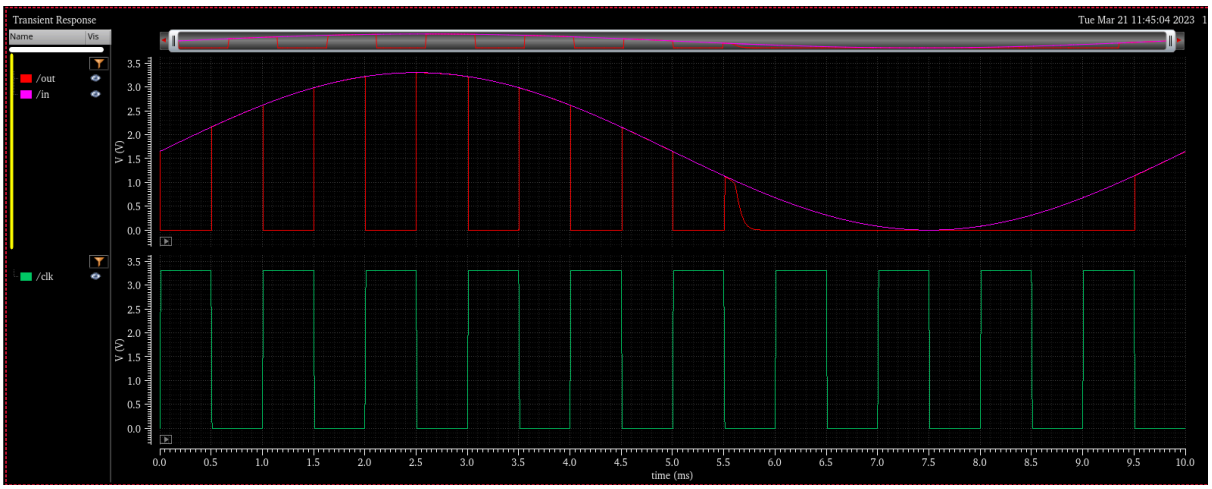


Figure 7 : Use of a pmos sampler with a sinus entry

As opposed to before for the same entrance, the circuit cannot sample lower values of V_{in}. Since Pmos technology is not able to sample lower values of V_{in} and nmos technology higher values of V_{in} , the use of both in parallel solves the issue like Figure 8 shows.

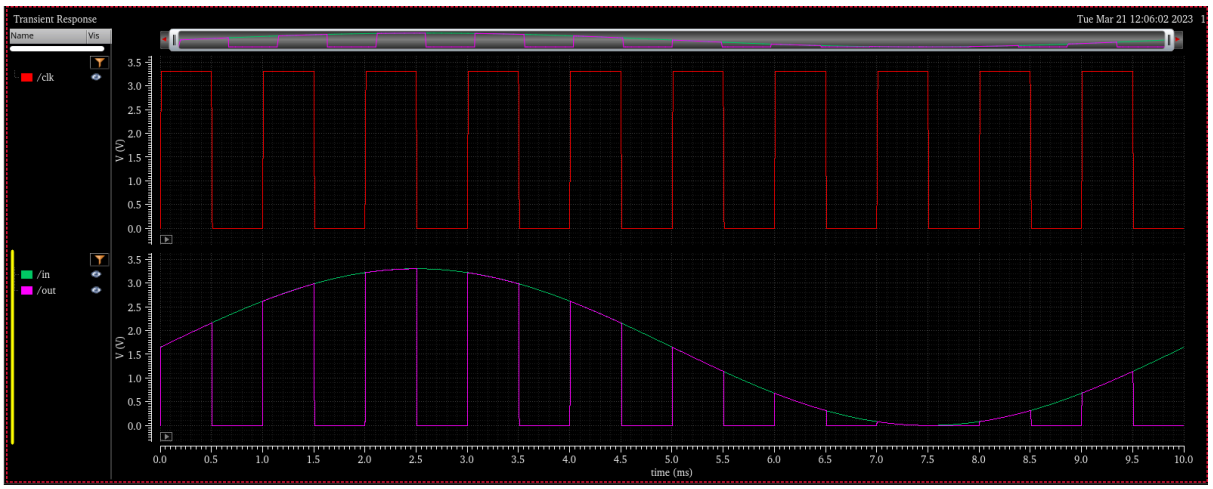


Figure 8 : Use of both pmos and pmos sampler in parallel with a sinus entry

The sample and hold circuit is the circuit of both a sampler using pmos and nmos technology in parallel in addition to a capacity in parallel to it as well. The point of adding a capacity to a sampler is to “memorize” the values and not reach zero each times the clock (Red curve on Fig8) reaches 0 because step values are needed.

Figure 9 : Use of sampler and different capacities

A capacity of 40 nF was chosen as it is the best compromise between deforming the signal and holding on to the value. If the capacity value is lower than this, holding values do not meet the requirements and if the value is too high, the signal becomes deformed and therefore too distinct from the input.

PMOS Differential Pair

A differential pair is used to amplify the difference between 2 input signals (V0 and V1 on Figure 10).There are formed by connecting the gates of two transistors together, with one input signal applied to the gate of one transistor and the other input signal applied to the gate of the other transistor. The two input signals produce an amplified output that is proportional to their difference.

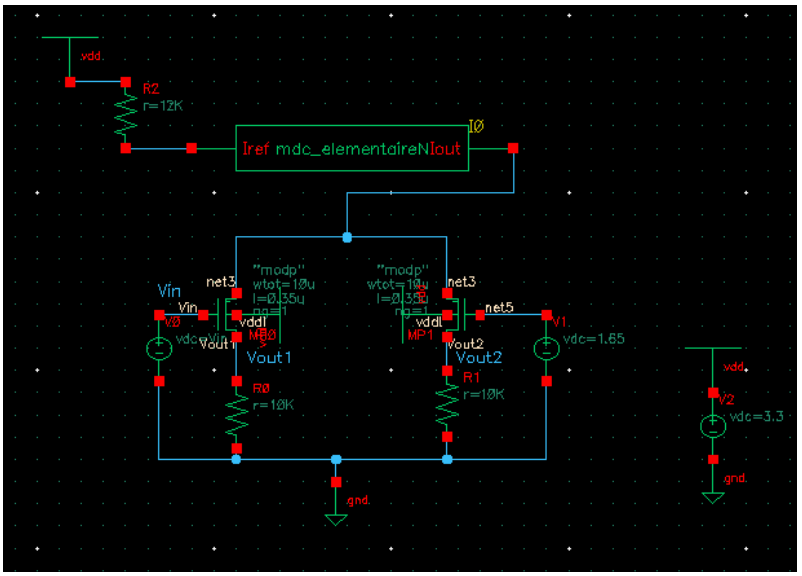


Figure 10 : PMOS differential pair wiring

A PMOS differential pair circuit uses two PMOS transistors to compare two input signals. The circuit is powered by a polarization current. The gates of the transistors are connected to the input signals. The difference between the input signals controls the current that goes through the transistors, creating a voltage difference between the two output signals, Vout1 and Vout2. The resistors (R1 and R2) in the circuit have the same value and are used to control the gain of the amplifier. By adjusting the current and resistor values, the circuit can provide an amplified voltage output that is proportional to the difference between the input signals. In simulations, a current generator is used to set the polarization current in a circuit. But in real life, a resistor with a voltage applied to it is used to create the same current. To make sure the current is well replicated, a current mirror is used. The current mirror makes a copy of the input current with a higher output current. This helps to ensure the current is the same on each side of the circuit.

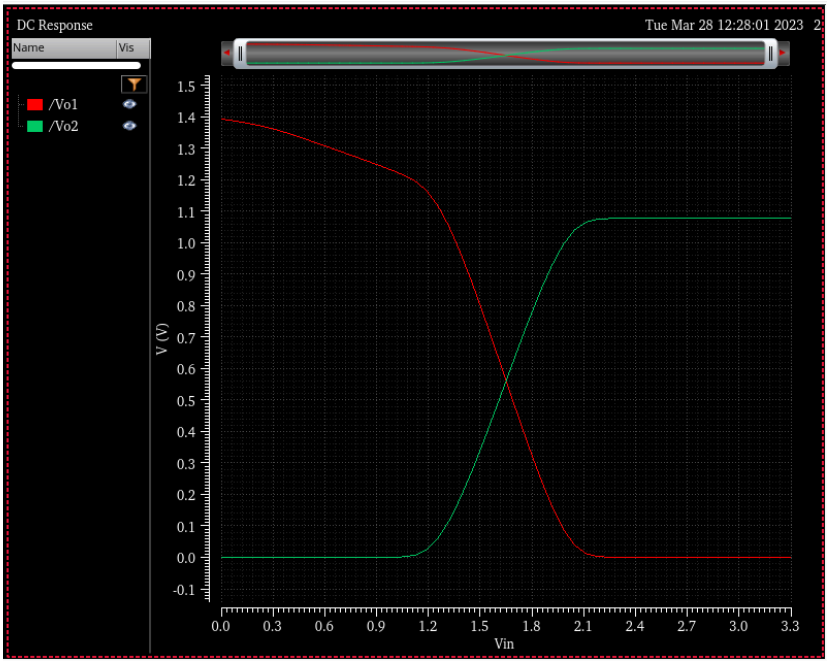


Figure 11 : transfert fonction

During the project, a reference voltage of 1.65V was defined for V1 in the simulation. The input voltage range, V2, was defined between 0 and 3.3V, which is represented by the X-axis labeled "Vin" in Figure 11. When Vin is lower than 1.65V, Vout1 is the output voltage. However, when Vin is higher than the reference voltage, Vout2 is high. In the final project, differential pairs are used to create a comparator that compares sampled voltages with reference voltages, allowing us to convert an analog signal to a digital one. This enables binary decisions (0 or 1) to be made based on the comparison of voltages. The comparator is able to tell whether an input voltage is higher or lower than a reference voltage.

Conclusion

During the course of this project, several functions were mapped, simulated and converted into symbols on the Cadence software. Finally they were put together in order to create the 4-bit flash ADC converter. This analogue converter whose schematic is on Figure 12 is composed of a sampler-blocker, a comparator, a transcoder and a 4-bit register. The input signal is first sampled and compared to fifteen values, then it is converted into binary value by the transcoder and finally registered before being displayed.

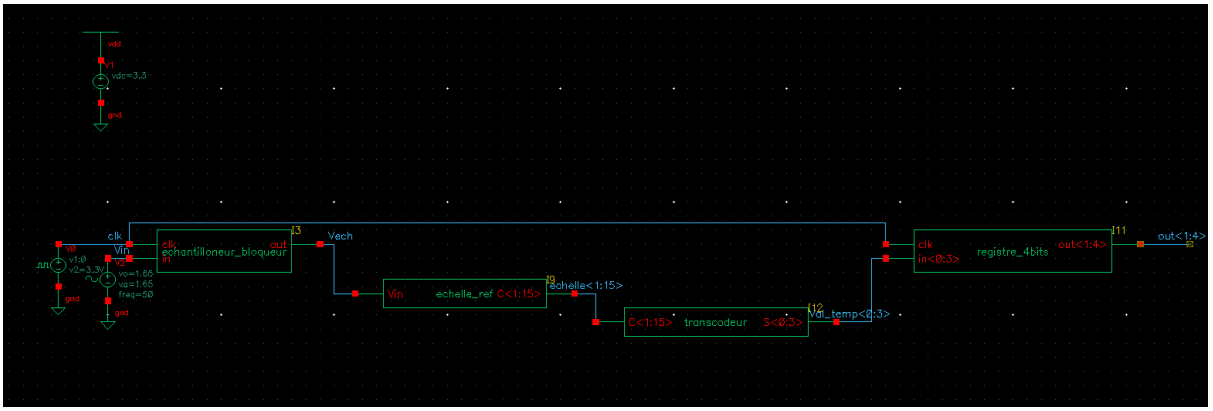


Figure 12: Analogue converter schematic

A final simulation was carried out as for the other functions. The results of this simulation are shown in Figure 13. The input signal is a sinus with a frequency of 100Hz and a sampling frequency of 1kHz.

The time is given on the X axis and the voltage on the Y axis. From the bottom to the top, there is the clock, the input signal, O0, O1, O2, O3.

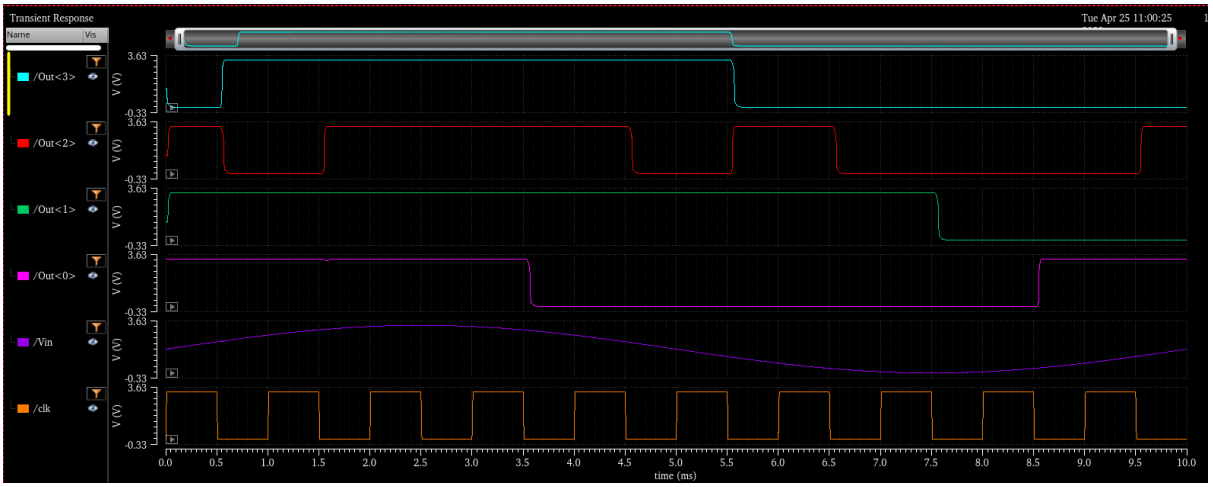


Figure 13: Final simulation results

An analogue converter allows for the quantization of a signal which means that it will transform an analog signal into a logic signal(O3, O2, O1, O0). The converter must approximate the input signal into sixteen different binary levels as explained in the introduction.The converter takes every binary value of the output signal for different corresponding values of the input signal. For example, when the input signal is at its highest, the output is ‘1111’ and at its lowest ‘0000’. Between those extreme values, the output takes values between 0 and 15.

However, a shift in the output signal can be observed, probably due to some mistakes made along the conception of the converter.

Through this project, the use of the CADENCE CAO software, its several tools and also how to conceive an electronic device was learned. In addition, notions learned in class were used and put into practice. Some time was needed to adapt to the use of the software and errors in the placement of components sometimes slowed down the project. Nonetheless, in spite of these mistakes and technical problems during this project, our results are rather satisfying.