CS354 p4B Worksheet: For given cach config, determine hits (H) and misses (M) for each instruction in the trace

csim-ref [-hv] -s <s> -E <E> -b <b> -t <tracefile>
-h: Optional help flag that prints usage info
-v: Optional verbose flag that displays trace info
-s <s>: Number of s bits for set index
-E <E>: number of lines per set (associativity)
-b <b>: Number of b bits for block offsets
-t <tracefile>: Name of the valgrind trace to replay

./csim -s 4 -E 2 -b 4 -t traces/trace1
operation address,size
 L 0,1 **0000 0000 Set 0, line 0. M**
 L 1,1 **0000 0001 Set 0, line 0. H**
 L 2,1 **0000 0010 Set 0, line 0. H**
 L 3,1 **0000 0011 Set 0, line 0. H**
 S 4,1 **0000 0100 Set 0, line 0. H**
 L 5,1 **0000 0101 Set 0, line 0. H**
 S 6,1 **0000 0110 Set 0, line 0. H**
 L 7,1 **0000 0111 Set 0, line 0. H**
 S 8,1 **0000 1000 Set 0, line 0. H**
 L 9,1 **0000 1001 Set 0, line 0. H**
 S a,1 **0000 1010 Set 0, line 0. H**
 L b,1 **0000 1011 Set 0, line 0. H**
 S c,1 **0000 1100 Set 0, line 0. H**
 L d,1 **0000 1101 Set 0, line 0. H**
 S e,1 **0000 1110 Set 0, line 0. H**
 M f,1 **0000 1111 Set 0, line 0. H twice**

./csim -s 4 -E 1 -b 4 -t traces/trace2
 L 10,1 **0001 0000 Set 1, M**
 M 20,1 **0010 0000 Set 2, M and then H**
 L 22,1 **0010 0010 Set 2, H**
 S 18,1 **0001 1000 Set 1, H**
 L 110,1 **0001 0001 0000 Set 1, M**
 L 210,1 **0010 0001 0000 Set 1, M**
 M 12,1 **0001 0010 Set 1, M when load and then H when store**

./csim -s 2 -E 3 -b 3 -t traces/trace3
 L 10,4 **0001 0000 Set 2, Line 0, M**
 S 18,4 **0001 1000 Set 3, Line 0, M**
 L 20,4 **0010 0000 Set 0, Line 0, M**
 S 28,4 **0010 1000 Set 1, Line 0, M**
 S 50,4 **0101 0000 Set 2, Line 1, M**

./csim -s 3 -E 4 -b 5 -t traces/trace4 (this only partical list of trace4)
 S 00600aa0,1 **0000 0000 0110 0000 0000 1010 1010 0000 Set 5, Line 0, M**
I 004005b6,5
 S 7ff000398,8 **0111 1111 1111 0000 0000 0000 0011 1001 1000 Set 4, Line 0, M**
I 0040051e,1
 S 7ff000390,8 **0111 1111 1111 0000 0000 0000 0011 1001 0000 Set 4, Line 0, H**
I 0040051f,3
I 00400522,4
 S 7ff000378,8 **0111 1111 1111 0000 0000 0000 0011 0111 1000 Set 3, Line 0, M**
I 00400526,4
 S 7ff000370,8 **0111 1111 1111 0000 0000 0000 0011 0111 0000 Set 3, Line 0, H**
I 0040052a,7
 S 7ff000384,4 **0111 1111 1111 0000 0000 0000 0011 1000 0100 Set 4, Line 0, H**
I 00400531,2
I 00400581,4
 L 7ff000384,4

Draw memory diagram of cache with S=4 and E=2.
Label memory type of each mem location: cache_line_t, cache_set_t, cache_t