

Demonstration of 99.9% single qubit control fidelity of a silicon quantum dot spin qubit made in a 300 mm foundry process

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Abstract – Commercially viable quantum computing will require large numbers of high-quality qubits. Therefore, leveraging the extensive capabilities of conventional CMOS technology is expected to accelerate the development of a fault-tolerant quantum computer. Here we report on the highest single-qubit control fidelity of 99.9% for any Si/SiO₂ spin qubit fabricated in a 300 mm wafer process. This result represents an important milestone towards a large-scale silicon quantum processor on a single chip.

INTRODUCTION Spin qubits formed at the Si/SiO₂ interface by charge accumulation with patterned gate electrodes are promising candidates for large-scale quantum computing due to their extensive overlap with existing CMOS technologies. Prototype spin qubit devices fabricated at academic cleanroom facilities with customized fabrication flows have shown to exhibit long coherence times and high-fidelity qubit control [1], even at elevated temperatures above 1 K [2]. However, to fully leverage the existing CMOS industry for scaling up spin qubit quantum processors, an important milestone is to demonstrate that spin qubits fabricated in a 300mm foundry environment can exhibit control fidelities compatible with quantum error correction thresholds. Here, we report the control fidelity of a single Si-MOS spin qubit surpassing 99.9% as analysed using two different and widely used benchmarking techniques. To achieve this high level of control, we employ real-time feedback protocols with state-of-the-art FPGA-based controllers and control pulse shaping [3,4].

RESULTS AND DISCUSSIONS - The device is fabricated in a planar 300 mm process using an epitaxially grown 800 ppm ²⁸Si substrate and a flexible hybrid DUV/electron-beam lithography fabrication flow which were extensively discussed before [5]. Key to the qubit performance is a 20 nm high-quality thermally grown Si/SiO₂ interface. The device layout, as sketched in Fig. 1, consists of a charge sensor, or single electron transistor (SET), which is patterned in proximity to a double quantum dot (QD). All measurements are performed in a ³He/⁴He cryostat with a base temperature of 180 mK [1,6]. SET transport measurements, Fig. 2, reveal Coulomb blockade and a lever arm of 0.04. The charge noise spectrum with a low level of 0.4 μ eV at 1 Hz, shown in Fig. 3, indicates a high quality Si/SiO₂ interface as explored previously in devices with SiO₂ thicknesses of 8 nm and 12 nm [3,4]. Qubit initialization and readout, using Pauli Spin Blockade (PSB), is performed at the (3,1)-(4,0) electron number transition with (P₁,P₂) indicating charge numbers under gates P1/P2, see Fig. 4 [2]. Fig. 5 shows coherent spin manipulation by applying and ac current to a patterned ESR-

antenna on resonance with the Larmor frequency of 18.89 GHz, set by the global magnetic field of 0.7 T. Coherent driving is observed with increasing applied microwave power showing Rabi frequencies (f_{Rabi}) up to 2 MHz and Q-factors, defined as the product between Rabi coherence time and f_{Rabi} , up to 100 as shown in Fig 6, and selected qubit metrics are given in Table 1. We employ a Gaussian single-sideband modulation control voltage pulse shape to minimize crosstalk, which would impact the second electron spin and PSB readout and analyse the single qubit control fidelity (F_{SQ}) using two community standard benchmarking techniques. With randomized benchmarking (RBM), Fig. 7., we extract a Clifford gate fidelity of 99.91 \pm 0.01%. Using Gate Set Tomography (GST) we extract single qubit fidelities of 99.97 $^{+0.03}_{-0.04}$ % and 99.97 \pm 0.03% for $X_{\pi/2}$ and $Y_{\pi/2}$ gates, respectively, summarized in Table 2. The low Hamiltonian and high stochastic contributions in the GST analysis suggest that further improvements can be made by increasing qubit coherence, for example by using a ²⁸Si substrate with increased purification levels - above the level currently used.

CONCLUSION - In this work, we demonstrated 99.9% single qubit gate fidelity measured by the two most used benchmarking techniques. This is the highest single qubit fidelity measured on a 300 mm Si/SiO₂ spin qubit to date and an important milestone towards fault-tolerant quantum computing by integrating large-scale quantum processors using industrial semiconductor facilities.

ACKNOWLEDGEMENTS

We acknowledge support from the Australian Research Council (FL190100167 and CE170100012).

REFERENCES

- [1] M. Veldhorst *et al.*, “A two-qubit logic gate in silicon,” *Nature*, vol. 526, no. 7573, pp. 410–414, 2015, doi: 10.1038/nature15263.
- [2] J. Y. Huang *et al.*, “High-fidelity spin qubit operation and algorithmic initialization above 1 K,” *Nature*, vol. 627, no. 8005, pp. 772–777, Mar. 2024, doi: 10.1038/s41586-024-07160-2.
- [3] N. Dumoulin Stuyck *et al.*, “Silicon spin qubit noise characterization using real-time feedback protocols and wavelet analysis,” *Appl. Phys. Lett.*, vol. 124, no. 11, p. 114003, Mar. 2024, doi: 10.1063/5.0179958.
- [4] L. M. K. Vandersypen and I. L. Chuang, “NMR techniques for quantum control and computation,” *Rev. Mod. Phys.*, vol. 76, no. 4, pp. 1037–1069, Jan. 2005, doi: 10.1103/RevModPhys.76.1037.
- [5] A. Elsayed *et al.*, “Low charge noise quantum dots with industrial CMOS manufacturing,” arXiv, 2022, doi: 10.48550/ARXIV.2212.06464.
- [6] A. Elsayed *et al.*, “Comprehensive 300 mm process for Silicon spin qubits with modular integration,” in *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Jun. 2023, pp. 1–2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185272.
- [7] T. N. Camenzind *et al.*, “High mobility SiMOSFETs fabricated in a full 300 mm CMOS process,” *Materials for Quantum Technology*, vol. 1, no. 4, IOP Publishing, p. 041001, Dec. 01, 2021, doi: 10.1088/2633-4356/ac40f4.

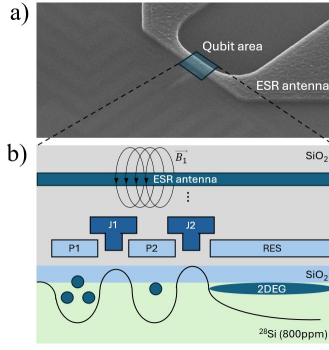


Figure 1. a) CDSEM of a 300 nm spin qubit device. b) Schematic cross-section of the device under test depicting the double quantum dot potentials (not to scale). We operate the qubit device by first loading 3 (1) electrons under the P1 (P2) gate and then depleting the two-dimensional electron gas (2DEG) under the J2 and RES gate [2]. Fabrication and device details can be found in [5,6].

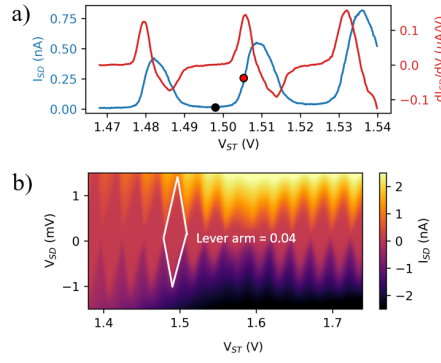


Figure 2. a) Charge sensor dc and conductance measurements. b) Coulomb diamonds with an extracted lever arm of 0.04, in line with results from 12 nm SiO₂ devices [5]. Details on the methods can be found in [5].

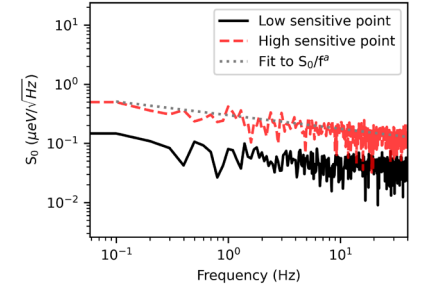


Figure 3. Noise spectral density of the charge sensor for two operation points indicated in Fig. 2a. SET current fluctuations are converted to energy level fluctuations using dI_{SD}/dV_{ST} and extracted lever arm, Fig. 2 [5]. Dotted line is a fit to S_0/f^α with $\alpha = 0.23$.

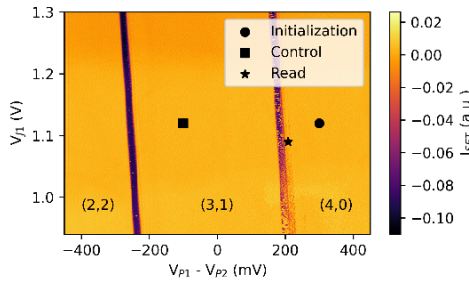


Figure 4. Charge stability map across the $(P_1, P_2) = (2,2)$ to $(4,0)$ charge occupation regimes [2]. The circle, square and star symbols indicate the initialization, control, and read point, respectively.

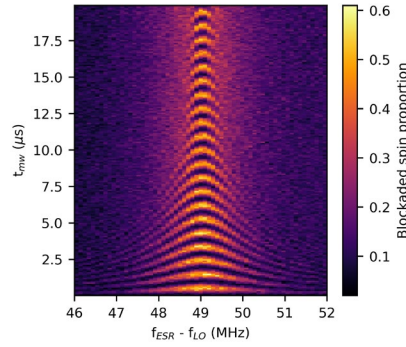


Figure 5. Single qubit Rabi chevron demonstrating coherence spin oscillations using the on-chip ESR antenna. f_{LO} is the microwave source local oscillation frequency of 18.44 GHz set by the global magnetic field of 0.7T.

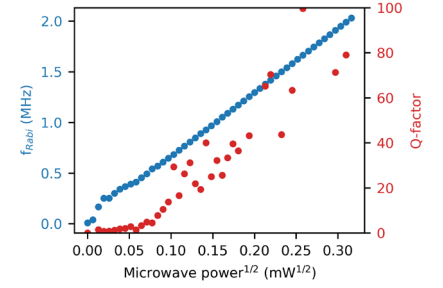


Figure 6. Rabi frequency and Q-factor vs applied microwave power to the electron spin resonance antenna on-chip. Q-factors are calculated from the fitted Rabi frequency and coherence as $f_{Rabi} \cdot T_2^{Rabi}$.

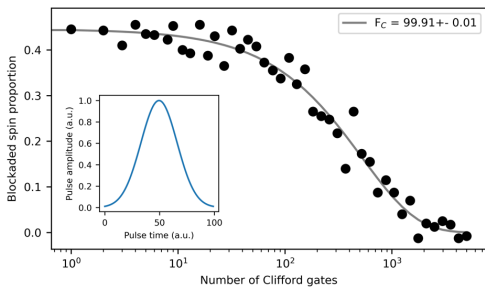


Figure 7. Randomized benchmarking data for 400 randomly generated sequences up to 5000 Clifford gates length with each Clifford comprise of $X_{\pi/2}$ and $Z_{\pi/2}$ single qubit gates. **Inset:** Gaussian pulse shape used for qubit gate control voltage pulses.

Table 1. Selected single qubit metrics; Ramsey (T_2^*), Hahn echo (T_2^{Hahn}) and Rabi (T_2^{Rabi}) coherence times [4].

Metric	Value (μs)
T_2^*	4.8 ± 0.7
T_2^{Hahn}	105 ± 11
T_2^{Rabi}	146 ± 8

Table 2. Single qubit gates fidelity and error contribution (EC) estimates using Gate Set Tomography (GST) analysis.

Qubit Gate	$X_{\pi/2}$	$Y_{\pi/2}$
Fidelity estimate	$99.98 \pm 0.04\%$	$99.95 \pm 0.07\%$
Total Hamiltonian EC	$2 \times 10^{-6} \pm 0.0002$	$(1 \pm 6) \times 10^{-5}$
Total stochastic EC	0.0002 ± 0.0007	0.0005 ± 0.002